# Quad MECL-to-TTL Translator

# Description

The MC10H125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic section of digital systems. The 10H part is a functional/pinout duplication of the standard MECL  $10K^{TM}$  family part, with 100% improvement in propagation delay, and no increase in power–supply current.

Outputs of unused translators will go to low state when their inputs are left open.

#### **Features**

- Propagation Delay, 2.5 ns Typical
- Voltage Compensated
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- MECL 10K Compatible
- Pb-Free Packages are Available\*

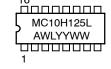


# ON Semiconductor®

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#### **MARKING DIAGRAMS\***





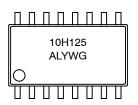
CDIP-16 L SUFFIX CASE 620A



PDIP-16 P SUFFIX CASE 648

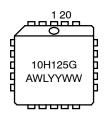


SOEIAJ-16 CASE 966









A = Assembly Location

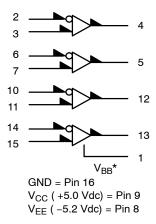
WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G = Pb-Free Package

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

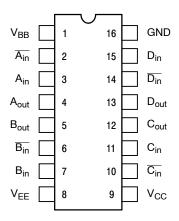
<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

<sup>\*</sup>For additional marking information, refer to Application Note AND8002/D.



\*V $_{BB}$  to be used to supply bias to the MC10H125 only and bypassed (when used) with 0.01  $\mu F$  to 0.1  $\mu F$  capacitor to ground (0 V). V $_{BB}$  can source < 1.0 mA.

Figure 1. Logic Diagram



Pin assignment is for Dual-in-Line Package. For PLCC pin assignment, see the Pin Conversion Tables.

Figure 2. Pin Assignment

# **Table 1. DIP CONVERSION TABLES**

# 16-Pin DIL to 20-Pin PLCC

16 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16				
20 PIN PLCC	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20				
20-Pin DIL to 20-Pin PLCC										-										
20 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
20 PIN PLCC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

**Table 2. MAXIMUM RATINGS** 

Symbol	Characteristic	Rating	Unit
V <sub>EE</sub>	Power Supply (V <sub>CC</sub> = 5.0 V)	-8.0 to 0	Vdc
V <sub>CC</sub>	Power Supply (V <sub>EE</sub> = -5.2 V)	0 to +7.0	Vdc
VI	Input Voltage (V <sub>CC</sub> = 5.0 V)	0 to V <sub>EE</sub>	Vdc
T <sub>A</sub>	Operating Temperature Range	0 to +75	°C
T <sub>stg</sub>	Storage Temperature Range - Plastic - Ceramic	-55 to +150 -55 to +165	°C °C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

Table 3. ELECTRICAL CHARACTERISTICS (V<sub>EE</sub> = -5.2 V +5%; V<sub>CC</sub> = 5.0 V + 5.0 %) (Note 2)

		<b>0</b> °		2	5°	75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
Ι <sub>Ε</sub>	Negative Power Supply Drain Current	-	44	-	40	_	44	mA
I <sub>CCH</sub>	Positive Power Supply	-	63	-	63	-	63	mA
I <sub>CCL</sub>	Drain Current	-	40	-	40	-	40	mA
I <sub>inH</sub>	Input Current	-	225	-	145	-	145	μΑ
I <sub>CBO</sub>	Input Leakage Current	-	1.5	-	1.0	-	1.0	μΑ
V <sub>OH</sub>	High Output Voltage I <sub>OH</sub> = -1.0 mA	2.5	-	2.5	-	2.5	-	Vdc
V <sub>OL</sub>	Low Output Voltage I <sub>OL</sub> = +20 mA	-	0.5	-	0.5	-	0.5	Vdc
$V_{IH}$	High Input Voltage (Note 1)	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
$V_{IL}$	Low Input Voltage (Note 1)	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
Ios	Short Circuit Current	60	150	60	150	50	150	mA
V <sub>BB</sub>	Reference Voltage	-1.38	-1.27	-1.35	-1.25	-1.31	-1.19	Vdc
$V_{CMR}$	Common Mode Range (Note 3)	_	-	-2.85 ·	to +0.3			V
	Typical					-		
V <sub>PP</sub>	Input Sensitivity (Note 4)			1	150			mV

When V<sub>BB</sub> is used as the reference voltage.
 Each MECL 10H™ series circuit has been designed to meet the specifications shown in the test table, after thermal equilibrium has been designed to meet the specifications shown in the test table, after thermal equilibrium has been designed to meet the specifications shown in the test table, after thermal equilibrium has been designed to meet the specifications shown in the test table, after thermal equilibrium has been designed to meet the specifications shown in the test table, after thermal equilibrium has been designed to meet the specifications shown in the test table, after thermal equilibrium has been designed to meet the specifications shown in the test table. established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

<sup>3.</sup> Differential input not to exceed 1.0 Vdc.

<sup>4. 150</sup> mV $_{p-p}$  differential input required to obtain full logic swing on output.

**Table 4. AC CHARACTERISTICS** 

		<b>0</b> °		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
t <sub>pd</sub>	Propagation Delay	0.8	3.3	0.85	3.35	0.9	3.4	ns
t <sub>r</sub>	Rise Time (Note 5)	0.3	1.2	0.3	1.2	0.3	1.2	ns
t <sub>f</sub>	Fall Time (Note 5)	0.3	1.2	0.3	1.2	0.3	1.2	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Output Voltage = 1.0 V to 2.0 V.  $R_L$  = 500  $\Omega$  to GND and  $C_L$  = 25 pF to GND. Refer to Figure 1.

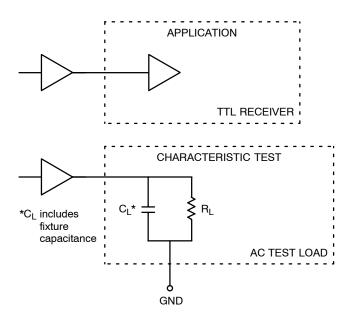


Figure 1. TTL Output Loading Used for Device Evaluation

#### **APPLICATION INFORMATION**

The MC10H125 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/non–inverting translator or as a differential line receiver. The  $V_{BB}$  reference voltage is available on Pin 1 for use in single–ended input biasing. The outputs of the MC10H125 go to a low–logic level whenever the inputs are left floating, and a high–logic output level is achieved with a minimum input level of 150 mV $_{p-p}$ .

An advantage of this device is that MECL-level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL-logic from the noisy TTL environment. Power supply requirements are ground, +5.0 V and -5.2 V.

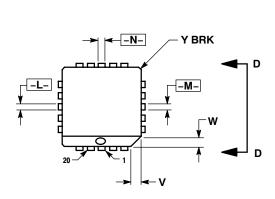
# **ORDERING INFORMATION**

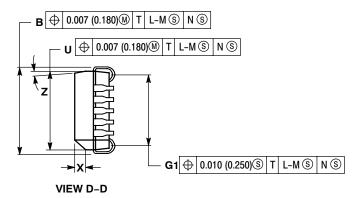
Device	Package	Shipping <sup>†</sup>
MC10H125FN	PLLC-20	46 Units / Rail
MC10H125FNG	PLLC-20 (Pb-Free)	46 Units / Rail
MC10H125FNR2	PLLC-20	500 / Tape & Reel
MC10H125FNR2G	PLLC-20 (Pb-Free)	500 / Tape & Reel
MC10H125L	CDIP-16	25 Unit / Rail
MC10H125M	SOEIAJ-16	50 Unit / Rail
MC10H125MG	SOEIAJ-16 (Pb-Free)	50 Unit / Rail
MC10H125MEL	SOEIAJ-16	2000 / Tape & Reel
MC10H125MELG	SOEIAJ-16 (Pb-Free)	2000 / Tape & Reel
MC10H125P	PDIP-16	25 Unit / Rail
MC10H125PG	PDIP-16 (Pb-Free)	25 Unit / Rail

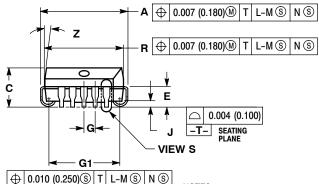
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

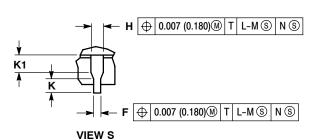
#### PACKAGE DIMENSIONS

# **20 LEAD PLLC** CASE 775-02 **ISSUE E**









- NOTES:
  1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
- 1982.

  DIMENSIONS IN INCHES.

  DIMENSIONS IN INCHES.

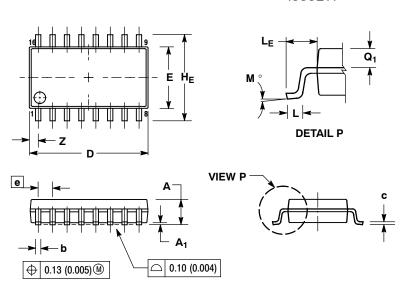
  DIFFERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.

- PARTING LINE.
  4. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM —T-, SEATING PLANE.
  5. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
  6. DIMENSIONS IN THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- PLASTIC BODY.
  7. DIMENSION H DOES NOT INCLUDE DAMBAR DIMIENSION H DUES NOT INCLUDE DAMBAR
  PROTRUSION OR INTRUSION. THE DAMBAR
  PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION
  TO BE GREATER THAN 0.037 (0.940). THE DAMBAR
  INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO
  BE SMALLER THAN 0.025 (0.635).

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.385	0.395	9.78	10.03
В	0.385	0.395	9.78	10.03
С	0.165	0.180	4.20	4.57
Е	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050	BSC	1.27	BSC
H	0.026	0.032	0.66	0.81
C	0.020		0.51	
K	0.025		0.64	
R	0.350	0.356	8.89	9.04
c	0.350	0.356	8.89	9.04
٧	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
Х	0.042	0.056	1.07	1.42
Υ		0.020	-	0.50
Z	2°	10°	2°	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040		1.02	

#### PACKAGE DIMENSIONS

# SOEIAJ-16 CASE 966-01 **ISSUE A**



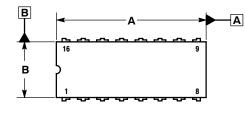
- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI

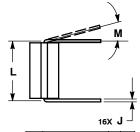
- NOTES:

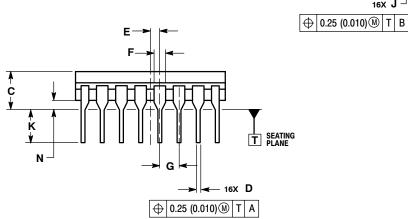
  1 DIMENSIONING AND TOLERANCING PER ANSI
  Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS DI AND E DO NOT INCLUDE MOLD
  FLASH OR PROTRUSIONS AND ARE MEASURED
  AT THE PARTING LINE. MOLD FLASH OR
  PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006)
  PER SIDE.
  4. TERMINAL NUMBERS ARE SHOWN FOR
  REFERENCE ONLY.
  5. THE LEAD WIDTH DIMENSION (b) DOES NOT
  INCLUDE DAMBAR PROTRUSION. ALLOWABLE
  DAMBAR PROTRUSION SHALL BE 0.08 (0.003)
  TOTAL IN EXCESS OF THE LEAD WIDTH
  DIMENSION AT MAXIMUM MATERIAL CONDITION.
  DAMBAR CANNOT BE LOCATED ON THE LOWER
  RADIUS OR THE FOOT. MINIMUM SPACE
  BETWEEN PROTRUSIONS AND ADJACENT LEAD
  TO BE 0.46 (0.018).

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α		2.05		0.081	
A <sub>1</sub>	0.05	0.20	0.002	0.008	
b	0.35	0.50	0.014	0.020	
C	0.10	0.20	0.007	0.011	
D	9.90	10.50	0.390	0.413	
Е	5.10	5.45	0.201	0.215	
е	1.27	BSC	0.050 BSC		
HE	7.40	8.20	0.291	0.323	
L	0.50	0.85	0.020	0.033	
LE	1.10	1.50	0.043	0.059	
M	0 °	10 °	0 °	10°	
Qī	0.70	0.90	0.028	0.035	
Z		0.78		0.031	

# CDIP-16 **L SUFFIX** CERAMIC DIP PACKAGE CASE 620A-01 **ISSUE O**







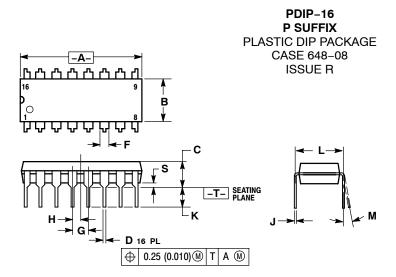
#### NOTES:

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION LTO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
- BODY.
  THIS DRAWING REPLACES OBSOLETE CASE OUTLINE 620-10.

	INC	HES	MILLIMETERS				
DIM	MIN	MAX	MIN	MAX			
Α	0.750	0.785	19.05	19.93			
В	0.240	0.295	6.10	7.49			
С		0.200		5.08			
D	0.015	0.020	0.39	0.50			
E	0.050	BSC	1.27 BSC				
F	0.055	0.065	1.40	1.65			
G	0.100	BSC	2.54 BSC				
Н	0.008	0.015	0.21	0.38			
K	0.125	0.170	3.18	4.31			
L	0.300	BSC	7.62 BSC				
M	0 °	15°	0 °	15°			
N	0.020	0.040	0.51	1.01			

#### PACKAGE DIMENSIONS



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION LTO CENTER OF LEADS WHEN FORMED PARALLEL.
  DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIMETERS			
DIM	MIN	MAX	MIN	MAX		
Α	0.740	0.770	18.80	19.55		
В	0.250	0.270	6.35	6.85		
С	0.145	0.175	3.69	4.44		
D	0.015	0.021	0.39	0.53		
F	0.040	0.70	1.02	1.77		
G	0.100	BSC	2.54 BSC			
Н	0.050	BSC	1.27 BSC			
J	0.008	0.015	0.21	0.38		
K	0.110	0.130	2.80	3.30		
L	0.295	0.305	7.50	7.74		
M	0°	10°	0°	10 °		
S	0.020	0.040	0.51	1.01		

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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