Ultralow Noise XFET Voltage References with Current Sink and Source Capability

Data Sheet

ADR430/ADR431/ADR433/ADR434/ADR435

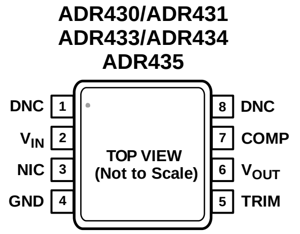
FEATURES

- **Low noise (0.1 Hz to 10.0 Hz): 3.5 µV p-p at 2.500 V output**
- **No external capacitor required**
- **Low temperature coefficient**
  - **A grade: 10 ppm/°C maximum**
  - **B grade: 3 ppm/°C maximum**
- **Load regulation: 15 ppm/mA**
- **Line regulation: 20 ppm/V**
- **Wide operating range**
  - **ADR430: 4.1 V to 18 V**
  - **ADR431: 4.5 V to 18 V**
  - **ADR433: 5.0 V to 18 V**
  - **ADR434: 6.1 V to 18 V**
  - **ADR435: 7.0 V to 18 V**
- **High output source and sink current: 30 mA and −20 mA**
- **Wide temperature range: −40°C to +125°C**

APPLICATIONS

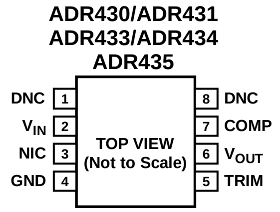
- **Precision data acquisition systems**
- **High resolution data converters**
- **Medical instruments**
- **Industrial process control systems**
- **Optical control circuits**
- **Precision instruments**

PIN CONFIGURATIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED.
THIS PIN IS NOT CONNECTED INTERNALLY.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 1. 8-Lead MSOP (RM-8)



NOTES
1. NIC = NOT INTERNALLY CONNECTED.
THIS PIN IS NOT CONNECTED INTERNALLY.
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Figure 2. 8-Lead SOIC_N (R-8)

GENERAL DESCRIPTION

The ADR430/ADR431/ADR433/ADR434/ADR435[1] series is a family of XFET® voltage references featuring low noise, high accuracy, and low temperature drift performance. Using Analog Devices, Inc., temperature drift curvature correction and extra implanted junction FET (XFET) technology, voltage change vs. temperature nonlinearity in the ADR430/ADR431/ADR433/ADR434/ADR435 is minimized.

The XFET references operate at lower current (800 µA) and lower supply voltage headroom (2 V) than buried Zener references. Buried Zener references require more than 5 V of headroom for operation. The ADR430/ADR431/ADR433/ADR434/ADR435 XFET references are low noise solutions for 5 V systems.

The ADR430/ADR431/ADR433/ADR434/ADR435 family has the capability to source up to 30 mA of output current and sink up to −20 mA. It also comes with a trim terminal to adjust the output voltage over a ±0.5% range without compromising performance.

The ADR430/ADR431/ADR433/ADR434/ADR435 are available in 8-lead MSOP and 8-lead narrow SOIC packages. All versions are specified over the extended industrial temperature range of −40°C to +125°C.

Table 1. Selection Guide

Model	Output Voltage (V)	Initial Accuracy (mV)	Temperature Coefficient (ppm/°C)
ADR430A	2.048	±3	10
ADR430B	2.048	±1	3
ADR431A	2.500	±3	10
ADR431B	2.500	±1	3
ADR433A	3.000	±4	10
ADR433B	3.000	±1.5	3
ADR434A	4.096	±5	10
ADR434B	4.096	±1.5	3
ADR435A	5.000	±6	10
ADR435B	5.000	±2	3

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[1] Protected by U.S. Patent Number 5,838,192.

Rev. N **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support **www.analog.com**

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REVISION HISTORY

2/2018—Rev. M to Rev. N

Changed V_O to V_{OUT} and ADR43x to ADR430/ADR431/ ADR433/ADR434/ADR435 ... Throughout
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Changes to Output Current Capacity Parameter and Trim Range Parameter, Table 3 ... 5
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2/2011—Rev. G to Rev. H
Updated Outline Dimensions 21
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7/2010—Rev. F to Rev. G
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6/2010—Rev. E to Rev. F
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12/2003—Revision 0: Initial Version

SPECIFICATIONS

ADR430 ELECTRICAL CHARACTERISTICS

V_{IN} = 4.1 V to 18 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}					
A Grade			2.045	2.048	2.051	V
B Grade			2.047	2.048	2.049	V
INITIAL ACCURACY[1]	V_{OERR}					
A Grade					±3	mV
					±0.15	%
B Grade					±1	mV
					±0.05	%
TEMPERATURE COEFFICIENT	TCV_{OUT}					
A Grade		−40°C < T_A < +125°C		2	10	ppm/°C
B Grade		−40°C < T_A < +125°C		1	3	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 4.1 V to 18 V, −40°C < T_A < +125°C		5	20	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$	I_L = 0 mA to 10 mA, V_{IN} = 5.0 V, −40°C < T_A < +125°C			15	ppm/mA
		I_L = −10 mA to 0 mA, V_{IN} = 5.0 V, −40°C < T_A < +125°C			15	ppm/mA
OUTPUT CURRENT CAPACITY	I_L					
Sourcing				30		mA
Sinking				−20		mA
QUIESCENT CURRENT	I_{IN}	No load, −40°C < T_A < +125°C		560	800	µA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10.0 Hz		3.5		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		60		nV/√Hz
TURN-ON SETTLING TIME	t_R	C_L = 0 µF		10		µs
LONG-TERM STABILITY[2]	ΔV_{OUT}	1000 hours		40		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{OUT_HYS}			20		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−70		dB
SHORT CIRCUIT TO GND	I_{SC}			40		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		4.1		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_{OUT}$		2			V
TRIM RANGE			−5		+5	%

[1] Initial accuracy does not include shift due to solder heat effect.

[2] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

ADR431 ELECTRICAL CHARACTERISTICS

V_{IN} = 4.5 V to 18 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}					
A Grade			2.497	2.500	2.503	V
B Grade			2.499	2.500	2.501	V
INITIAL ACCURACY[1]	V_{OERR}					
A Grade					±3	mV
					±0.12	%
B Grade					±1	mV
					±0.04	%
TEMPERATURE COEFFICIENT	TCV_{OUT}					
A Grade		$-40°C < T_A < +125°C$		2	10	ppm/°C
B Grade		$-40°C < T_A < +125°C$		1	3	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 4.5 V to 18 V, $-40°C < T_A < +125°C$		5	20	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$	I_L = 0 mA to 10 mA, V_{IN} = 5.0 V, $-40°C < T_A < +125°C$			15	ppm/mA
		I_L = −10 mA to 0 mA, V_{IN} = 5.0 V, $-40°C < T_A < +125°C$			15	ppm/mA
OUTPUT CURRENT CAPACITY	I_L					
Sourcing				30		mA
Sinking				−20		mA
QUIESCENT CURRENT	I_{IN}	No load, $-40°C < T_A < +125°C$		580	800	µA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10.0 Hz		3.5		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		80		nV/√Hz
TURN-ON SETTLING TIME	t_R	C_L = 0 µF		10		µs
LONG-TERM STABILITY[2]	ΔV_{OUT}	1000 hours		40		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{OUT_HYS}			20		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−70		dB
SHORT CIRCUIT TO GND	I_{SC}			40		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		4.5		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_{OUT}$		2			V
TRIM RANGE			−5		+5	%

[1] Initial accuracy does not include shift due to solder heat effect.
[2] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

ADR433 ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0 V to 18 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}					
A Grade			2.996	3.000	3.004	V
B Grade			2.9985	3.000	3.0015	V
INITIAL ACCURACY[1]	V_{OERR}					
A Grade					±4	mV
					±0.13	%
B Grade					±1.5	mV
					±0.05	%
TEMPERATURE COEFFICIENT	TCV_{OUT}					
A Grade		$-40°C < T_A < +125°C$		2	10	ppm/°C
B Grade		$-40°C < T_A < +125°C$		1	3	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 5 V to 18 V, $-40°C < T_A < +125°C$		5	20	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$	I_L = 0 mA to 10 mA, V_{IN} = 6 V, $-40°C < T_A < +125°C$			15	ppm/mA
		I_L = −10 mA to 0 mA, V_{IN} = 6 V, $-40°C < T_A < +125°C$			15	ppm/mA
OUTPUT CURRENT CAPACITY	I_L					
Sourcing				30		mA
Sinking				−20		mA
QUIESCENT CURRENT	I_{IN}	No load, $-40°C < T_A < +125°C$		590	800	μA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10.0 Hz		3.75		μV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		90		nV/√Hz
TURN-ON SETTLING TIME	t_R	C_L = 0 μF		10		μs
LONG-TERM STABILITY[2]	ΔV_{OUT}	1000 hours		40		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{OUT_HYS}			20		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−70		dB
SHORT CIRCUIT TO GND	I_{SC}			40		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		5.0		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_{OUT}$		2			V
TRIM RANGE			−5		+5	%

[1] Initial accuracy does not include shift due to solder heat effect.
[2] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

ADR434 ELECTRICAL CHARACTERISTICS

V_{IN} = 6.1 V to 18 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}					
A Grade			4.091	4.096	4.101	V
B Grade			4.0945	4.096	4.0975	V
INITIAL ACCURACY[1]	V_{OERR}					
A Grade					±5	mV
					±0.12	%
B Grade					±1.5	mV
					±0.04	%
TEMPERATURE COEFFICIENT	TCV_{OUT}					
A Grade		$-40°C < T_A < +125°C$		2	10	ppm/°C
B Grade		$-40°C < T_A < +125°C$		1	3	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 6.1 V to 18 V, $-40°C < T_A < +125°C$		5	20	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$	I_L = 0 mA to 10 mA, V_{IN} = 7 V, $-40°C < T_A < +125°C$			15	ppm/mA
		I_L = −10 mA to 0 mA, V_{IN} = 7 V, $-40°C < T_A < +125°C$			15	ppm/mA
OUTPUT CURRENT CAPACITY	I_L					
Sourcing				30		mA
Sinking				−20		mA
QUIESCENT CURRENT	I_{IN}	No load, $-40°C < T_A < +125°C$		595	800	µA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10.0 Hz		6.25		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		100		nV/√Hz
TURN-ON SETTLING TIME	t_R	C_L = 0 µF		10		µs
LONG-TERM STABILITY[2]	ΔV_{OUT}	1000 hours		40		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{OUT_HYS}			20		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−70		dB
SHORT CIRCUIT TO GND	I_{SC}			40		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		6.1		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_{OUT}$		2			V
TRIM RANGE			−5		+5	%

[1] Initial accuracy does not include shift due to solder heat effect.

[2] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

ADR435 ELECTRICAL CHARACTERISTICS

V_{IN} = 7.0 V to 18 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}					
A Grade			4.994	5.000	5.006	V
B Grade			4.998	5.000	5.002	V
INITIAL ACCURACY[1]	V_{OERR}					
A Grade					±6	mV
					±0.12	%
B Grade					±2	mV
					±0.04	%
TEMPERATURE COEFFICIENT	TCV_{OUT}					
A Grade		$-40°C < T_A < +125°C$		2	10	ppm/°C
B Grade		$-40°C < T_A < +125°C$		1	3	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 7 V to 18 V, $-40°C < T_A < +125°C$		5	20	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$	I_L = 0 mA to 10 mA, V_{IN} = 8 V, $-40°C < T_A < +125°C$			15	ppm/mA
		I_L = −10 mA to 0 mA, V_{IN} = 8 V, $-40°C < T_A < +125°C$			15	ppm/mA
OUTPUT CURRENT CAPACITY	I_L					
Sourcing				30		mA
Sinking				−20		mA
QUIESCENT CURRENT	I_{IN}	No load, $-40°C < T_A < +125°C$		620	800	µA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10 Hz		8		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		115		nV/√Hz
TURN-ON SETTLING TIME	t_R	C_L = 0 µF		10		µs
LONG-TERM STABILITY[2]	ΔV_{OUT}	1000 hours		40		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{OUT_HYS}			20		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−70		dB
SHORT CIRCUIT TO GND	I_{SC}			40		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		7.0		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_{OUT}$		2			V
TRIM RANGE			−5		+5	%

[1] Initial accuracy does not include shift due to solder heat effect.

[2] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
Supply Voltage	20 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

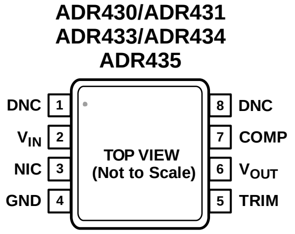
Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N (R)	130	43	°C/W
8-Lead MSOP (RM)	142	44	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

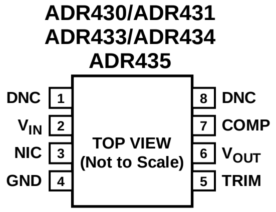
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED.
THIS PIN IS NOT CONNECTED INTERNALLY.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

04500-101

Figure 3. 8-Lead MSOP Pin Configuration



NOTES
1. NIC = NOT INTERNALLY CONNECTED.
THIS PIN IS NOT CONNECTED INTERNALLY.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

04500-141

Figure 4. 8-Lead SOIC Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DNC	Do Not Connect. Do not connect to this pin.
2	V_{IN}	Input Voltage Connection.
3	NIC	Not Internally Connected. This pin is not connected internally.
4	GND	Ground.
5	TRIM	Output Voltage Trim.
6	V_{OUT}	Output Voltage.
7	COMP	Compensation Input. Connect a series resistor and capacitor network from COMP to V_{OUT} to reduce overall noise.
8	DNC	Do Not Connect. Do not connect to this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

Default conditions: V_{IN} = 7 V, T_A = 25°C, C_{IN} = C_{OUT} = 0.1 μF, unless otherwise noted.

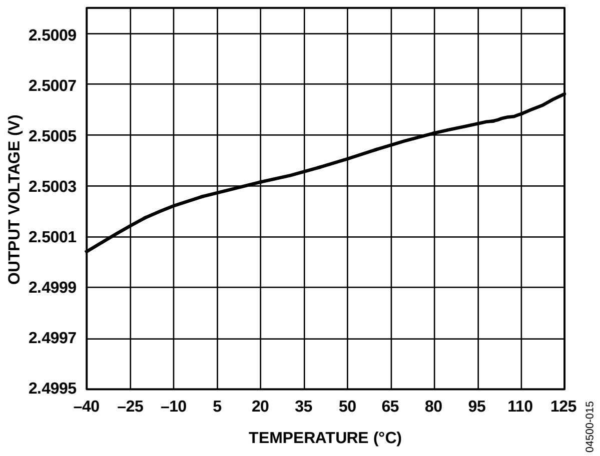


Figure 5. ADR431 Output Voltage vs. Temperature

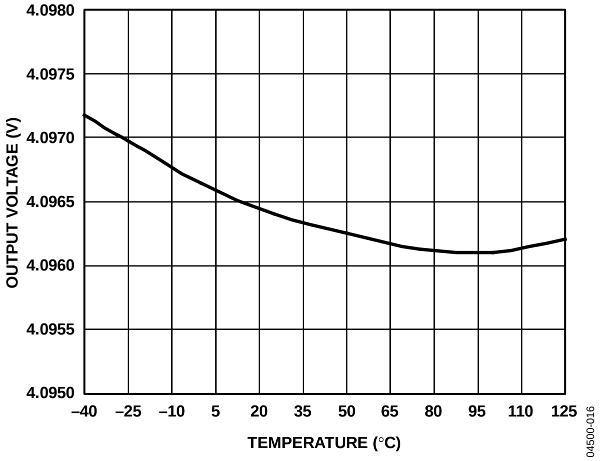


Figure 6. ADR434 Output Voltage vs. Temperature

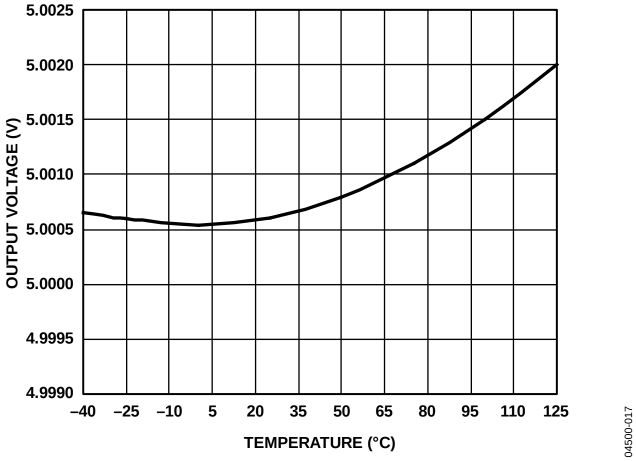


Figure 7. ADR435 Output Voltage vs. Temperature

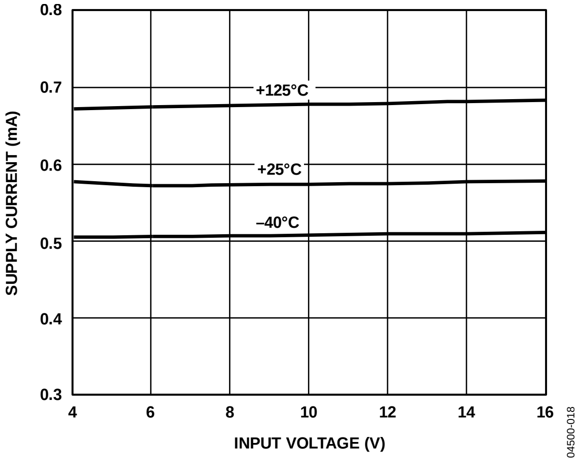


Figure 8. ADR435 Supply Current vs. Input Voltage

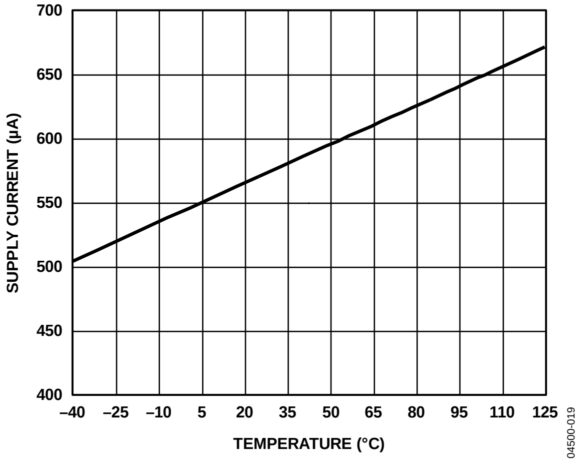


Figure 9. ADR435 Supply Current vs. Temperature

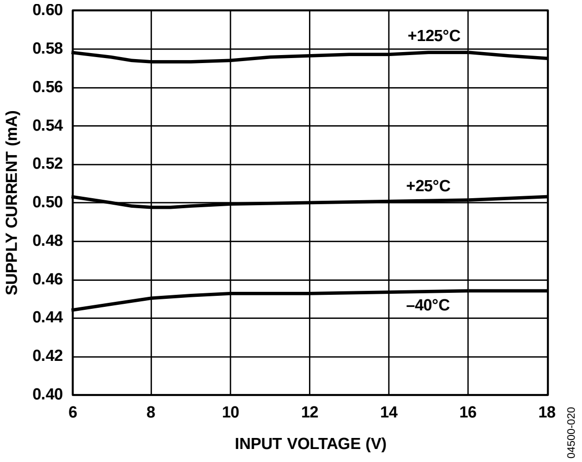


Figure 10. ADR431 Supply Current vs. Input Voltage

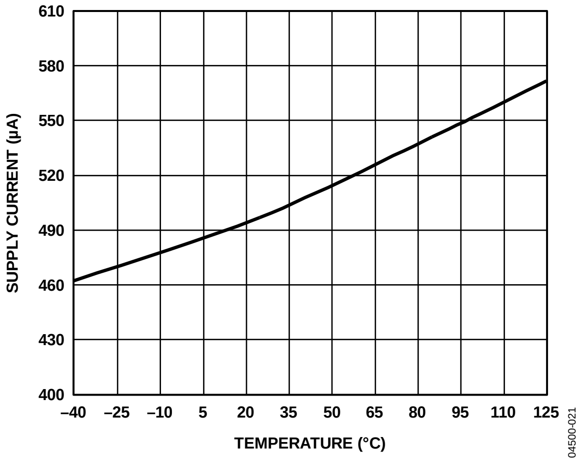


Figure 11. ADR431 Supply Current vs. Temperature

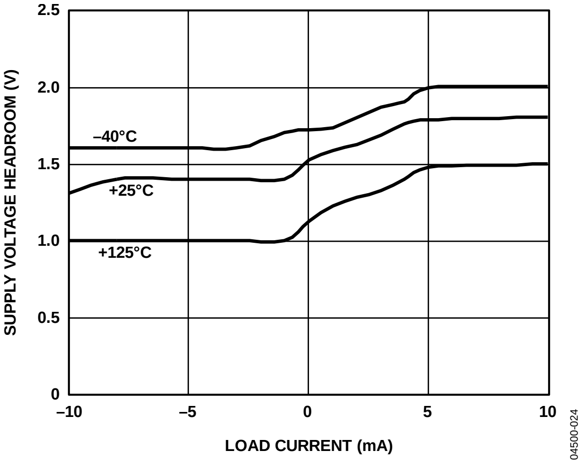


Figure 14. ADR431 Supply Voltage Headroom vs. Load Current over Temperature

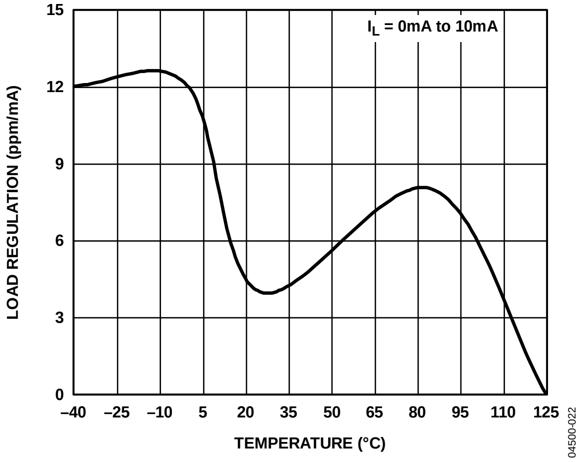


Figure 12. ADR431 Load Regulation vs. Temperature

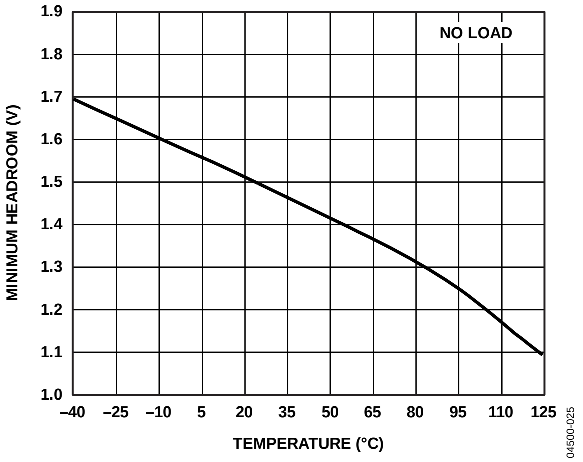


Figure 15. ADR431 Minimum Headroom vs. Temperature

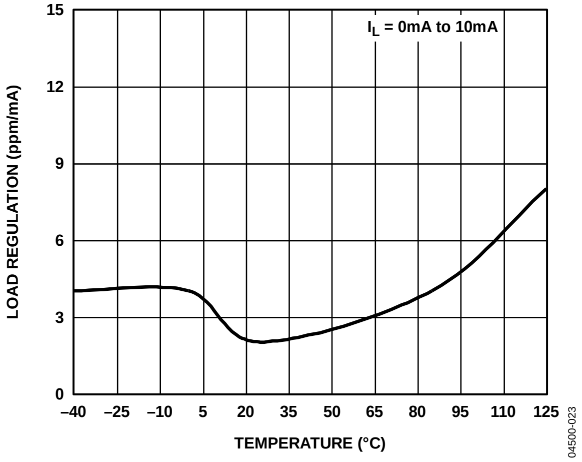


Figure 13. ADR435 Load Regulation vs. Temperature

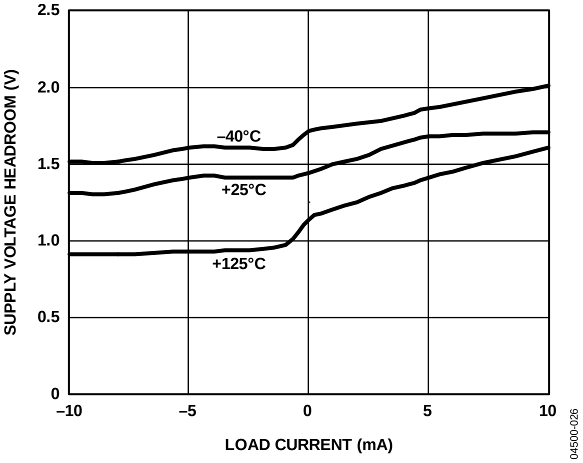


Figure 16. ADR435 Supply Voltage Headroom vs. Load Current over Temperature

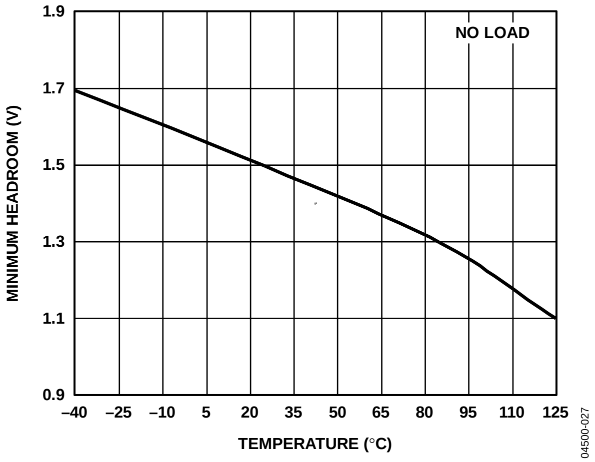


Figure 17. ADR435 Minimum Headroom vs. Temperature

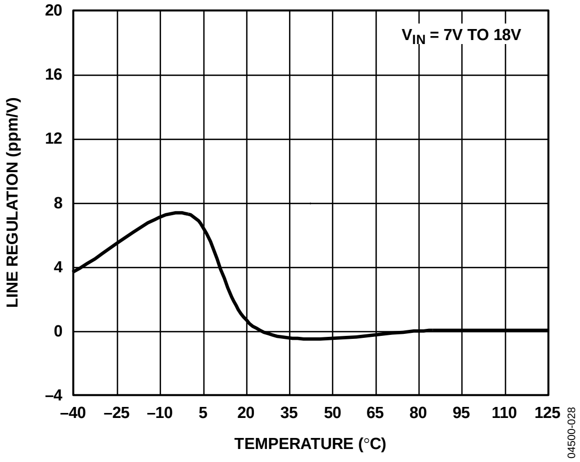


Figure 18. ADR435 Line Regulation vs. Temperature

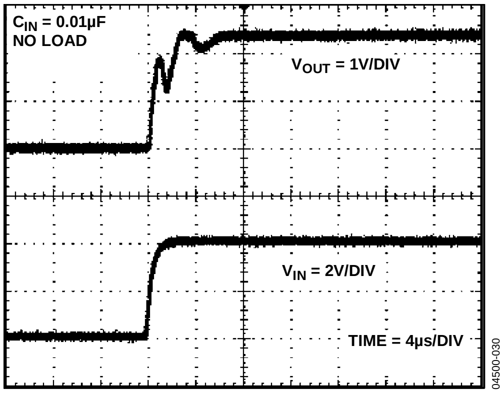


Figure 19. ADR431 Turn-On Settling Time Response, No Load

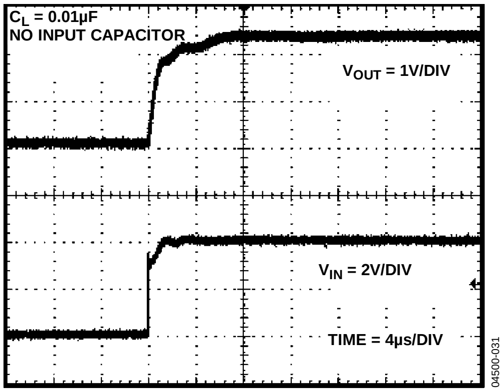


Figure 20. ADR431 Turn-On Response Settling Time, 0.01 µF Load Capacitor

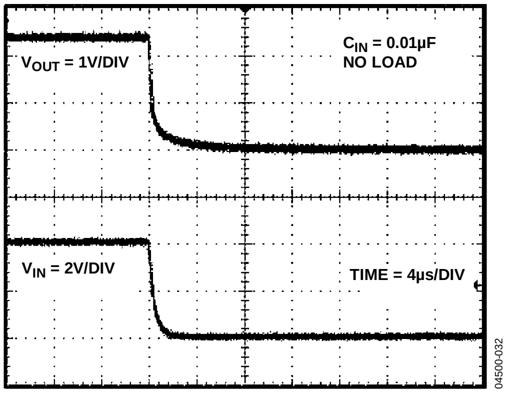


Figure 21. ADR431 Turn-Off Settling Time Response

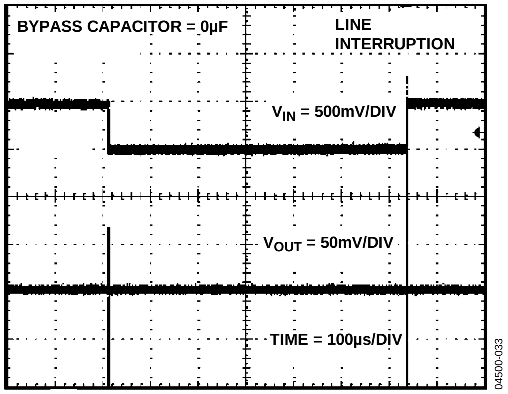


Figure 22. ADR431 Line Transient Response

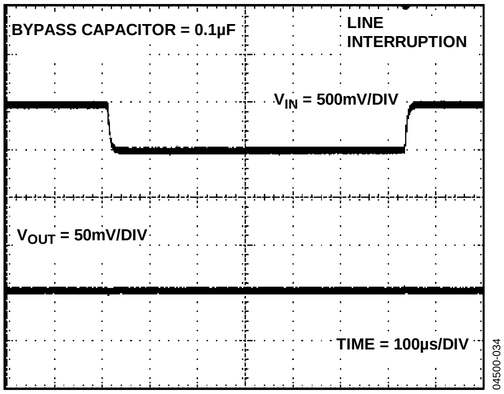


Figure 23. ADR431 Line Transient Response, 0.1 µF Bypass Capacitor

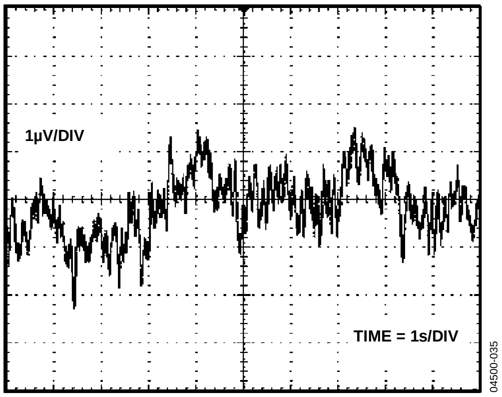


Figure 24. ADR431 0.1 Hz to 10.0 Hz Voltage Noise

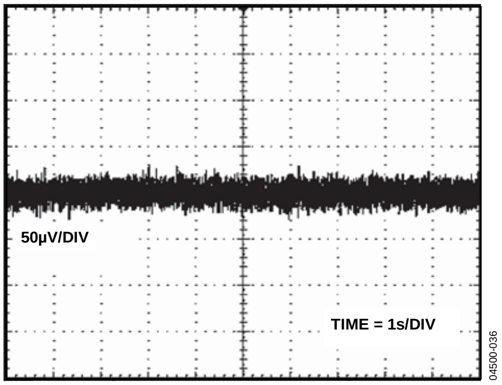


Figure 25. ADR431 10 Hz to 10 kHz Voltage Noise

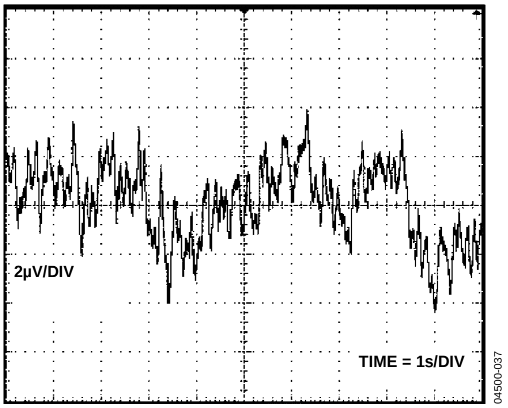


Figure 26. ADR435 0.1 Hz to 10.0 Hz Voltage Noise

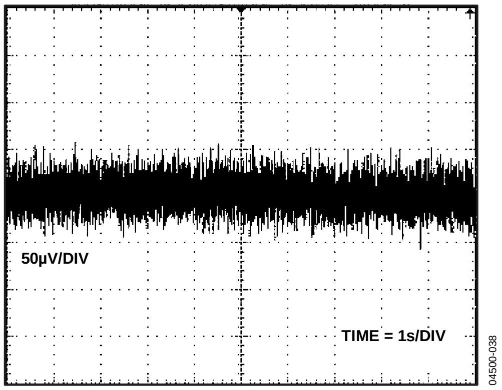


Figure 27. ADR435 10 Hz to 10 kHz Voltage Noise

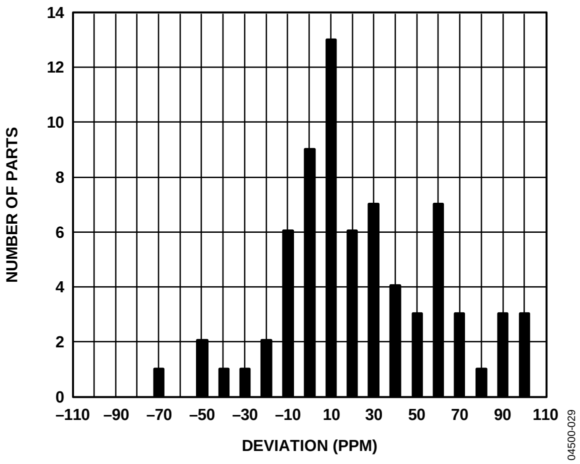


Figure 28. ADR431 Typical Hysteresis

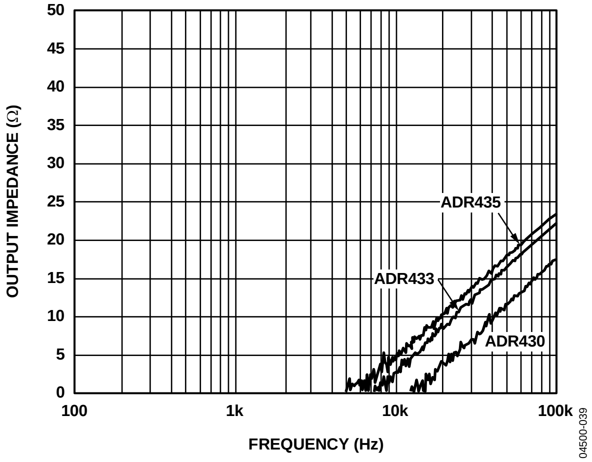


Figure 29. Output Impedance vs. Frequency

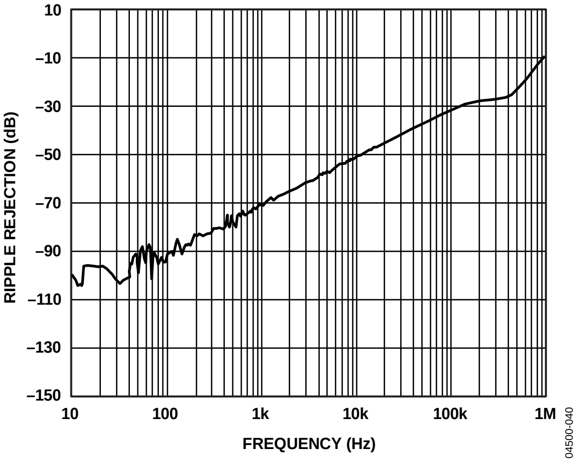


Figure 30. Ripple Rejection vs. Frequency

THEORY OF OPERATION

The ADR430/ADR431/ADR433/ADR434/ADR435 series of references uses a reference generation technique known as XFET. This technique yields a reference with low supply current, optimal thermal hysteresis, and exceptionally low noise. The core of the XFET reference consists of two junction field effect transistors (JFETs), one of which has an extra channel implant to raise its pinch off voltage. The two JFETs run at the same drain current, and the difference in pinch off voltage is amplified to form a highly stable voltage reference.

The intrinsic reference voltage is around 0.5 V with a negative temperature coefficient of about −120 ppm/°C. This slope is essentially constant to the dielectric constant of silicon and can be compensated closely by adding a correction term generated in the same fashion as the proportional to absolute temperature (PTAT) term used to compensate band gap references. The primary advantage of an XFET reference is its correction term, which is ~30 times lower and requires less correction than that of a band gap reference. Because most of the noise of a band gap reference comes from the temperature compensation circuitry, the XFET results in much lower noise.

Figure 31 shows the basic topology of the ADR430/ADR431/ADR433/ADR434/ADR435 series. The temperature correction term is provided by a current source with a value designed to be PTAT. The general equation is

$$V_{OUT} = G\,(\Delta V_P - R1 \times I_{PTAT}) \tag{1}$$

where:
G is the gain of the reciprocal of the divider ratio.
ΔV_P is the difference in pinch-off voltage between the two JFETs.
$R1$ is a resistor, as shown in Figure 31.
I_{PTAT} is the positive temperature coefficient correction current.

The ADR430/ADR431/ADR433/ADR434/ADR435 devices are created by on-chip adjustment of R2 and R3 to achieve 2.048 V to 5.000 V at the reference output.

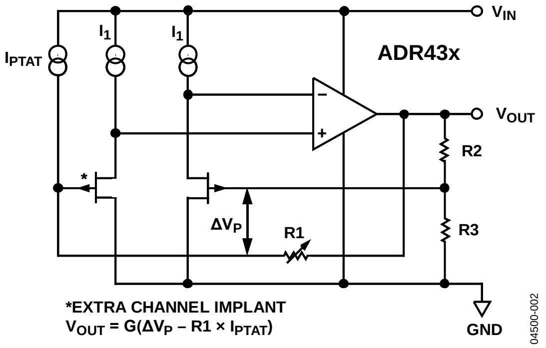


Figure 31. Simplified Schematic Device Power Dissipation Considerations

The ADR430/ADR431/ADR433/ADR434/ADR435 family of references is guaranteed to deliver load currents up to 10 mA with an input voltage that ranges from 4.1 V to 18 V.

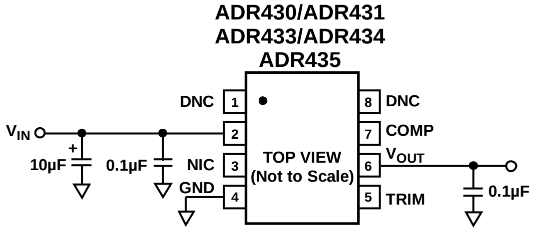
When these devices are used in applications at higher currents, use the following equation to account for the temperature effects due to the power dissipation increases:

$$T_J = P_D \times \theta_{JA} + T_A \tag{2}$$

where:
T_J and T_A are the junction and ambient temperatures, respectively.
P_D is the device power dissipation.
θ_{JA} is the device package junction to ambient thermal resistance.

BASIC VOLTAGE REFERENCE CONNECTIONS

Voltage references, in general, require a bypass capacitor connected from V_{OUT} to ground. The circuit in Figure 32 shows the basic configuration for the ADR430/ADR431/ADR433/ADR434/ADR435 family of references. Other than a 0.1 µF capacitor at the output to help improve noise suppression, a large output capacitor at the output is not required for circuit stability.



NOTES
1. NIC = NOT INTERNALLY CONNECTED. THIS PIN IS NOT CONNECTED INTERNALLY.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 32. Basic Voltage Reference Configuration

NOISE PERFORMANCE

The noise generated by the ADR430, ADR431, and ADR433 family of references is typically less than or equal to 3.75 µV p-p over the 0.1 Hz to 10.0 Hz band for. Figure 24 shows the 0.1 Hz to 10.0 Hz noise of the ADR431, which is only 3.5 µV p-p. The noise measurement is made with a band-pass filter composed of a two-pole, high-pass filter with a corner frequency at 0.1 Hz and a two-pole, low-pass filter with a corner frequency at 10.0 Hz.

HIGH FREQUENCY NOISE

The total noise generated by the ADR430/ADR431/ADR433/ADR434/ADR435 family of references is composed of the reference noise and the op amp noise. Figure 33 shows the wideband noise from 10 Hz to 25 kHz. An internal node of the op amp is available on Pin 7, and by overcompensating the op amp, the overall noise can be reduced.

Consider that, in a closed-loop configuration, the effective output impedance of an op amp is as follows:

$$R_O = \frac{r_O}{1 + A_{VO}\beta} \tag{3}$$

where:
R_O is the apparent output impedance.
r_O is the output resistance of the op amp.

A_{VO} is the open-loop gain at the frequency of interest.

β is the feedback factor.

Equation 3 shows that the apparent output impedance is approximately reduced by the excess loop gain; therefore, as the frequency increases, the excess loop gain decreases, and the apparent output impedance increases. A passive element whose impedance increases as its frequency increases is an inductor. When a capacitor is added to the output of an op amp or a reference, it forms a tuned circuit that resonates at a certain frequency and results in gain peaking. Gain peaking can be observed by using a model of an op amp with a single-pole response and some pure resistance in series with the output. Changing capacitive loads results in peaking at different frequencies. For most normal op amp applications with low capacitive loading (<100 pF), this effect is usually not observed.

However, references are used increasingly to drive the reference input of an analog-to-digital (ADC) that may present a dynamic, switching capacitive load. Large capacitors, in the microfarad range, reduce the change in reference voltage to less than one-half LSB. Figure 33 shows the ADR431 noise spectrum with various capacitive values to 50 µF. With no capacitive load, the noise spectrum is relatively flat at approximately 60 nV/√Hz to 70 nV/√Hz. With various values of capacitive loading, the predicted noise peaking becomes evident.

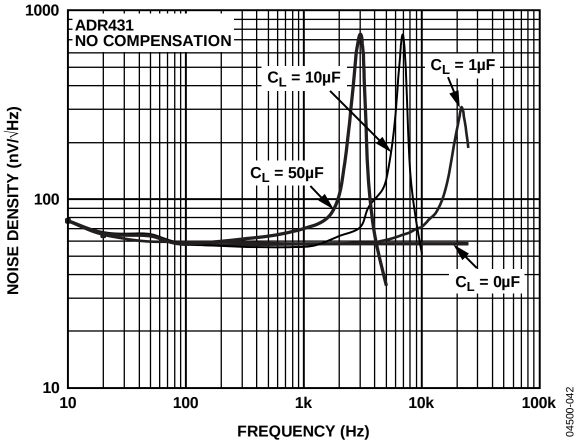


Figure 33. Noise Density vs. Frequency at Various Capacitive Loads

The op amp within the ADR430/ADR431/ADR433/ADR434/ADR435 family uses the classic resistor and capacitor (RC) compensation technique. Monolithic capacitors in an IC are limited to tens of picofarads. With very large external capacitive loads, such as 50 µF, it is necessary to overcompensate the op amp. The internal compensation node is available on Pin 7, and an external series RC network can be added between Pin 7 and the output, Pin 6, as shown in Figure 34.

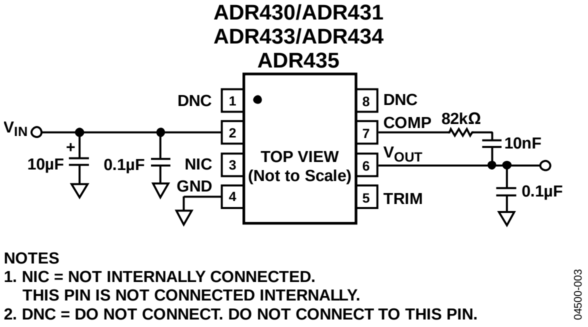


Figure 34. Compensated Reference

The 82 kΩ resistor and 10 nF capacitor eliminate noise peaking (see Figure 35). Leave the COMP pin unconnected if unused.

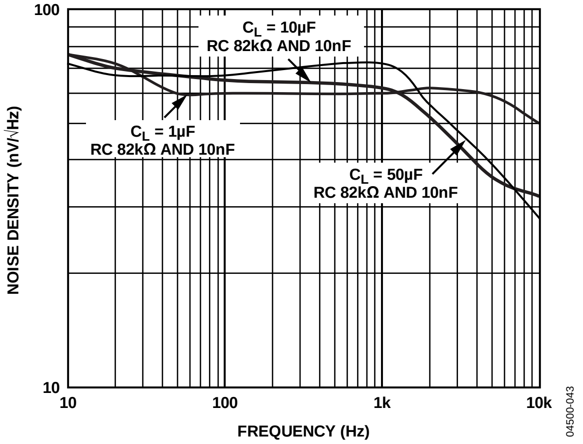


Figure 35. Noise with Compensation Network

TURN-ON SETTLING TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. Two components normally associated with this settling time are the time for the active circuits to settle and the time for the thermal gradients on the chip to stabilize. Figure 19 and Figure 20 show the turn-on settling time for the ADR431.

APPLICATIONS INFORMATION

OUTPUT ADJUSTMENT

The ADR430/ADR431/ADR433/ADR434/ADR435 trim terminal adjusts the output voltage over a ±0.5% range. This feature allows the system designer to trim system errors out by setting the reference to a voltage other than the nominal. This feature is also helpful if the device is used in a system at temperature to trim out any error. Adjustment of the output has a negligible effect on the temperature performance of the device. To avoid degrading temperature coefficients, both the trimming potentiometer and the two resistors need to be low temperature coefficient types, preferably <100 ppm/°C.

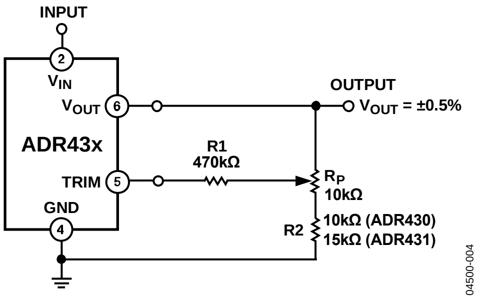


Figure 36. Output Trim Adjustment

REFERENCE FOR CONVERTERS IN OPTICAL NETWORK CONTROL CIRCUITS

In Figure 37, the high capacity, all optical router network employs arrays of micromirrors to direct and route optical signals from fiber to fiber without first converting them to electrical form, which reduces the communication speed. The tiny micromechanical mirrors are positioned so that each is illuminated by a single wavelength that carries unique information and can be passed to any desired input and output fiber. The mirrors are tilted by the dual-axis actuators, which are controlled by precision ADCs and DACs within the system. Due to the microscopic movement of the mirrors, not only is the precision of the converters important but the noise associated with these controlling converters is also extremely critical. Total noise within the system can be multiplied by the number of converters employed. Therefore, to maintain the stability of the control loop for this application, the exceptionally low noise performance of the ADR430/ADR431/ADR433/ADR434/ADR435 is necessary. (the ADR431 is shown in Figure 37 as an example).

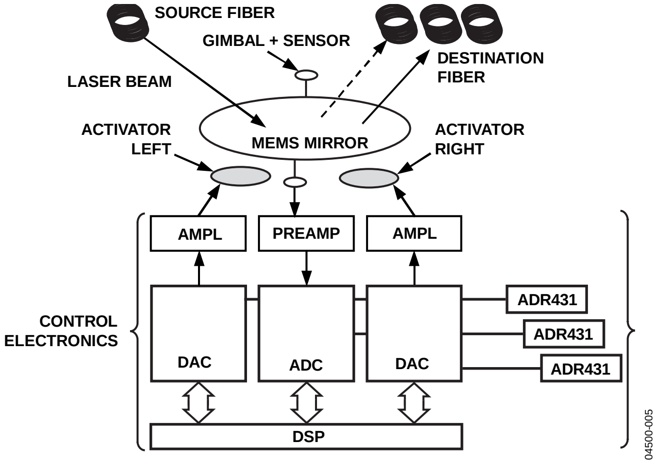


Figure 37. All Optical Router Network

HIGH VOLTAGE FLOATING CURRENT SOURCE

Use the circuit in Figure 38 to generate a floating current source with minimal self heating. This particular configuration can operate on high supply voltages determined by the breakdown voltage of the N-channel JFET.

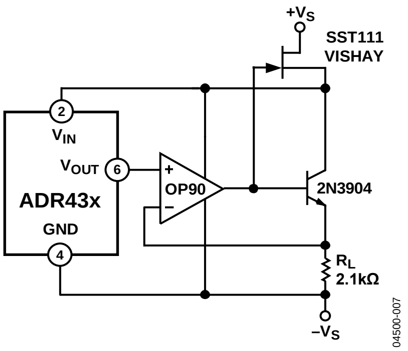


Figure 38. High Voltage Floating Current Source

KELVIN CONNECTION

In many portable instrumentation applications, where printed circuit board (PCB) cost and area are closely related, circuit interconnects are often of minimum width. These narrow lines can cause large voltage drops if the voltage reference is required to provide load currents to various functions. In fact, circuit interconnects can exhibit a typical line resistance of 0.45 mΩ/square (for example, 1 oz. copper). Force and sense connections, also referred to as Kelvin connections, offer a convenient method of eliminating the effects of voltage drops in circuit wires. Load currents flowing through wiring resistance produce an error ($V_{ERROR} = R \times I_L$) at the load. However, the Kelvin connection shown in Figure 39 overcomes the problem by including the wiring resistance within the forcing loop of the operational amplifier.

Because the amplifier senses the load voltage, the operational amplifier loop control forces the output to compensate for the wiring error and to produce the correct voltage at the load.

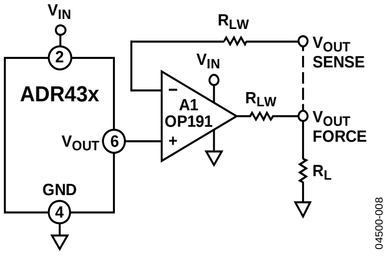


Figure 39. Advantage of Kelvin Connection

DUAL POLARITY REFERENCES

Dual polarity references can easily be made with an operational amplifier and a pair of resistors. To avoid defeating the accuracy obtained by the ADR430/ADR431/ADR433/ADR434/ADR435, it is imperative to match the resistance tolerance as well as the temperature coefficient of all the components.

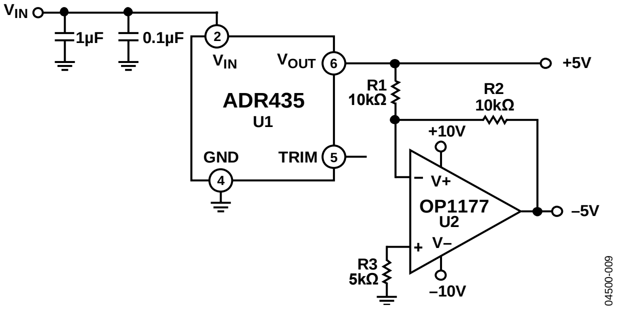


Figure 40. 5 V and –5 V References Using ADR435

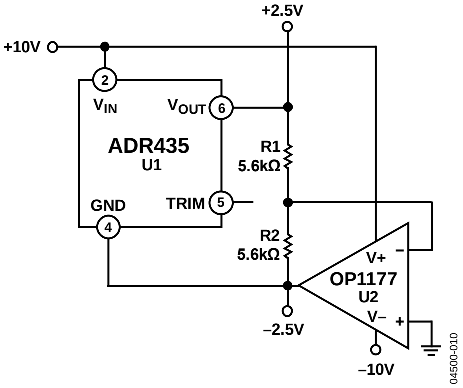


Figure 41. 2.5 V and –2.5 V References Using ADR435

PROGRAMMABLE CURRENT SOURCE

Together with a digital potentiometer and a Howland current pump, the ADR435 forms the reference source for a programmable current as

$$I_L = \left(\frac{R2_A + R2_B}{\frac{R1}{R2_B}} \right) \times V_W \tag{4}$$

and

$$V_W = \frac{D}{2^N} \times V_{REF} \tag{5}$$

where:
V_W is the voltage at Terminal W.
D is the decimal equivalent of the input code.
N is the number of bits.

In addition, R1' and R2' must be equal to R1 and ($R2_A$ + $R2_B$), respectively. In theory, $R2_B$ can be made as small as needed to achieve the necessary current within the A2 output current driving capability. In this example, the OP2177 can deliver a maximum current of 10 mA. Because the current pump employs both positive and negative feedback, the C1 and C2 capacitors are needed to ensure that the negative feedback prevails and, therefore, avoids oscillation. This circuit also allows bidirectional current flow if the A and B inputs of the digital potentiometer are supplied with the dual polarity references, as shown in Figure 42.

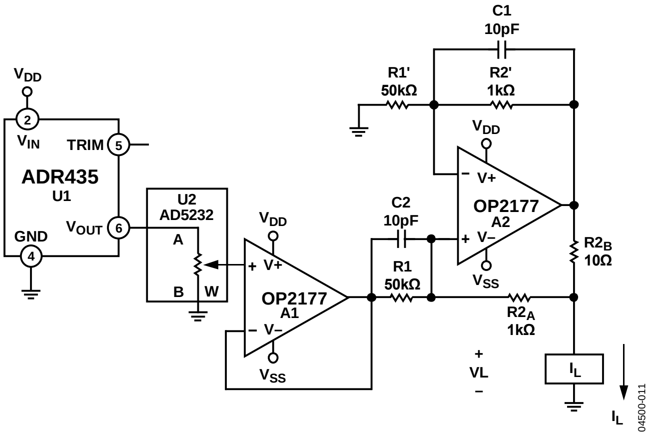


Figure 42. Programmable Current Source

PROGRAMMABLE DAC REFERENCE VOLTAGE

By employing a multichannel DAC, such as the AD7398, quad, 12-bit voltage output DAC, one of its internal DACs and an ADR430/ADR431/ADR433/ADR434/ADR435 voltage reference can be used as a common programmable V_{REFx} for the rest of the DACs. The circuit configuration is shown in Figure 43.

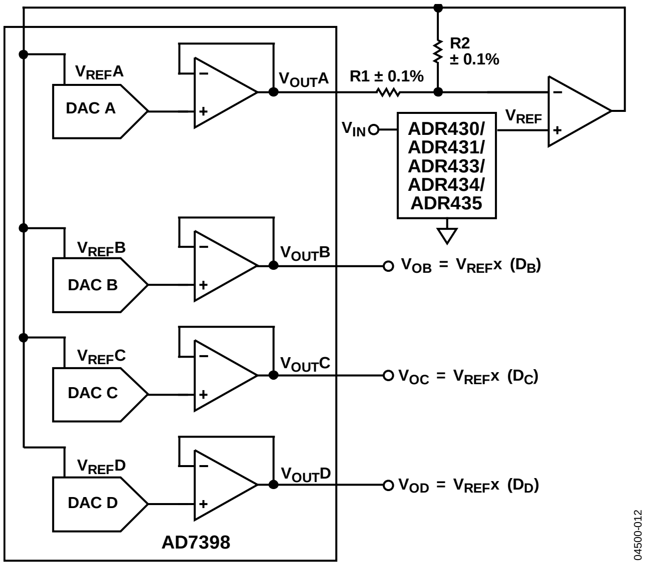


Figure 43. Programmable DAC Reference

The relationship of V_{REFx} to V_{REF} depends on the digital code and the ratio of R1 and R2, given by

$$V_{REFx} = \frac{V_{REF} \times \left(1 + \frac{R2}{R1}\right)}{\left(1 + \frac{D}{2^N} \times \frac{R2}{R1}\right)} \tag{6}$$

where:

V_{REFx} is the reference voltage for DAC A to DAC D.
D is the decimal equivalent of the input code.
V_{REF} is the applied external reference.
N is the number of bits.

Table 10. V_{REFx} vs. R1 and R2

R1, R2	Digital Code	V_{REFx}
R1 = R2	0000 0000 0000	2 × V_{REF}
R1 = R2	1000 0000 0000	1.3 × V_{REF}
R1 = R2	1111 1111 1111	V_{REF}
R1 = 3 × R2	0000 0000 0000	4 × V_{REF}
R1 = 3 × R2	1000 0000 0000	1.6 × V_{REF}
R1 = 3 × R2	1111 1111 1111	V_{REF}

PRECISION VOLTAGE REFERENCE FOR DATA CONVERTERS

The ADR430/ADR431/ADR433/ADR434/ADR435 family has a number of features that make it ideal for use with ADCs and DACs. The exceptional low noise, tight temperature coefficient, and high accuracy characteristics make the ADR430/ADR431/ADR433/ADR434/ADR435 ideal for low noise applications, such as cellular base station applications.

Another example of an ADC for which the ADR431 is well suited is the AD7701. Figure 44 shows the ADR431 used as the precision reference for this converter. The AD7701 is a 16-bit ADC with on-chip digital filtering intended for the measurement of wide dynamic range and low frequency signals, such as those representing chemical, physical, or biological processes. It contains a charge balancing Σ-Δ ADC, a calibration microcontroller with on-chip static random access memory (RAM), a clock oscillator, and a serial communications port.

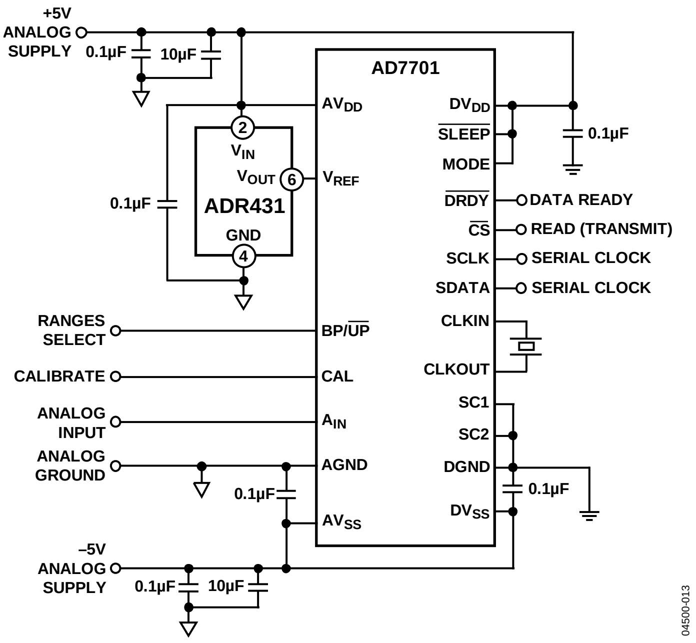


Figure 44. Voltage Reference for the AD7701 16-Bit ADC

PRECISION BOOSTED OUTPUT REGULATOR

A precision voltage output with boosted current capability can be achieved with the circuit shown in Figure 45. In this circuit, U2 forces V_O to be equal to V_{REF} by regulating gate voltage of N1. Therefore, the load current is supplied by V_{IN}. In this configuration, a 50 mA load is achievable at a V_{IN} of 5 V. Moderate heat is generated on the MOSFET, and higher current is achieved with a replacement of the larger device. In addition, for a heavy capacitive load with step input, add a buffer at the output to enhance the transient response.

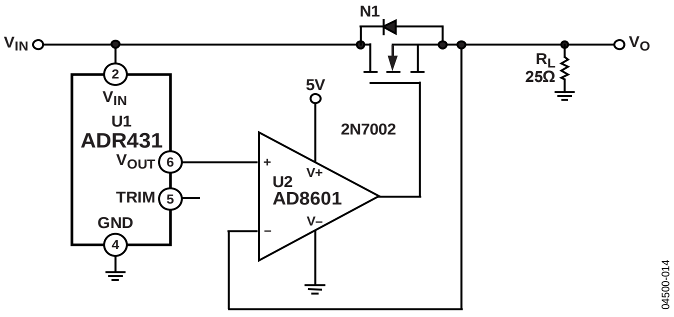
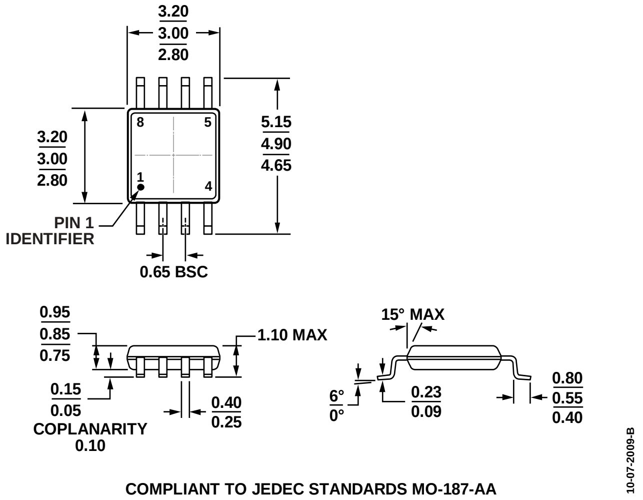


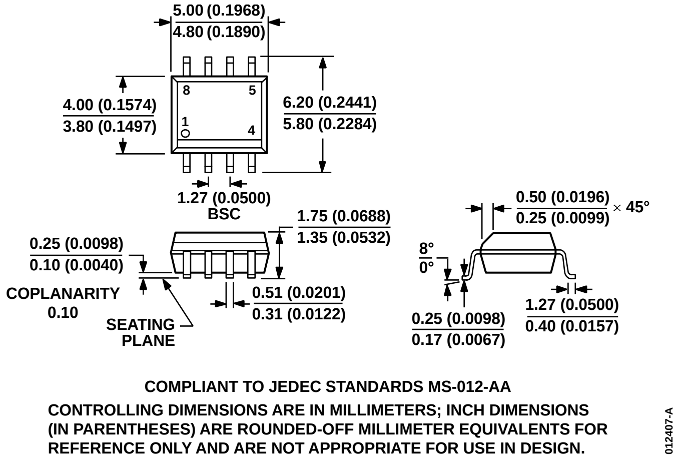
Figure 45. Precision Boosted Output Regulator

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 46. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 47. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Output Voltage (V)	Initial Accuracy, (mV)	(%)	Temperature Coefficient Package (ppm/°C)	Temperature Range	Package Description	Package Option	Ordering Quantity	Markin g Code
ADR430ARZ	2.048	±3	±0.15	10	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR430ARZ-REEL7	2.048	±3	±0.15	10	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR430ARMZ	2.048	±3	±0.15	10	−40°C to +125°C	8-Lead MSOP	RM-8	50	R10
ADR430ARMZ-REEL7	2.048	±3	±0.15	10	−40°C to +125°C	8-Lead MSOP	RM-8	1,000	R10
ADR430BRZ	2.048	±1	±0.05	3	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR430BRZ-REEL7	2.048	±1	±0.05	3	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR431ARZ	2.500	±3	±0.12	10	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR431ARZ-REEL7	2.500	±3	±0.12	10	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR431ARMZ	2.500	±3	±0.12	10	−40°C to +125°C	8-Lead MSOP	RM-8	50	R12
ADR431ARMZ-REEL7	2.500	±3	±0.12	10	−40°C to +125°C	8-Lead MSOP	RM-8	1,000	R12
ADR431BRMZ	2.500	±1	±0.04	3	−40°C to +125°C	8-Lead MSOP	RM-8	50	R13
ADR431BRMZ-R7	2.500	±1	±0.04	3	−40°C to +125°C	8-Lead MSOP	RM-8	1000	R13
ADR431BRZ	2.500	±1	±0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR431BRZ-REEL7	2.500	±1	±0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR433ARZ	3.000	±4	±0.13	10	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR433ARZ-REEL7	3.000	±4	±0.13	10	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR433ARMZ	3.000	±4	±0.13	10	−40°C to +125°C	8-Lead MSOP	RM-8	50	R14
ADR433ARMZ-REEL7	3.000	±4	±0.13	10	−40°C to +125°C	8-Lead MSOP	RM-8	1,000	R14
ADR433BRZ	3.000	±1.5	±0.05	3	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR433BRZ-REEL7	3.000	±1.5	±0.05	3	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR434ARZ	4.096	±5	±0.12	10	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR434ARZ-REEL7	4.096	±5	±0.12	10	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR434ARMZ	4.096	±5	±0.12	10	−40°C to +125°C	8-Lead MSOP	RM-8	50	R16
ADR434ARMZ-REEL7	4.096	±5	±0.12	10	−40°C to +125°C	8-Lead MSOP	RM-8	1,000	R16
ADR434BRZ	4.096	±1.5	±0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR434BRZ-REEL7	4.096	±1.5	±0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR435ARZ	5.000	±6	±0.12	10	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR435ARZ-REEL7	5.000	±6	±0.12	10	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR435ARMZ	5.000	±6	±0.12	10	−40°C to +125°C	8-Lead MSOP	RM-8	50	R18
ADR435ARMZ-REEL7	5.000	±6	±0.12	10	−40°C to +125°C	8-Lead MSOP	RM-8	1,000	R18
ADR435BRMZ	5.000	±2	±0.04	3	−40°C to +125°C	8-Lead MSOP	RM-8	50	R19
ADR435BRMZ-R7	5.000	±2	±0.04	3	−40°C to +125°C	8-Lead MSOP	RM-8	1,000	R19
ADR435BRZ	5.000	±2	±0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR435BRZ-REEL7	5.000	±2	±0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	

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[1] Z = RoHS Compliant Part.

D04500-0-2/18(N)

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.