

# MC74HC4051A, MC74HC4052A, MC74HC4053A



ON Semiconductor®

<http://onsemi.com>

## Analog Multiplexers / Demultiplexers

### High-Performance Silicon-Gate CMOS

The MC74HC4051A, MC74HC4052A and MC74HC4053A utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from  $V_{CC}$  to  $V_{EE}$ ).

The HC4051A, HC4052A and HC4053A are identical in pinout to the metal-gate MC14051AB, MC14052AB and MC14053AB. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

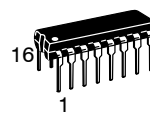
These devices have been designed so that the ON resistance ( $R_{on}$ ) is more linear over input voltage than  $R_{on}$  of metal-gate CMOS analog switches.

For a multiplexer/demultiplexer with injection current protection, see HC4851A and HC4852A.

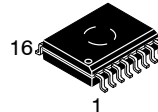
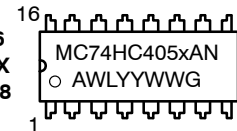
#### Features

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ( $V_{CC} - V_{EE}$ ) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ( $V_{CC} - GND$ ) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal-Gate Counterparts
- Low Noise
- In Compliance with the Requirements of JEDEC Standard No. 7A
- Chip Complexity: HC4051A — 184 FETs or 46 Equivalent Gates  
HC4052A — 168 FETs or 42 Equivalent Gates  
HC4053A — 156 FETs or 39 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

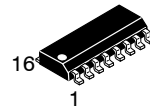
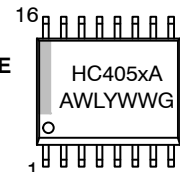
#### MARKING DIAGRAMS



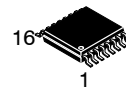
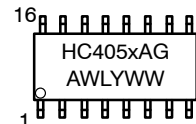
PDIIP-16  
N SUFFIX  
CASE 648



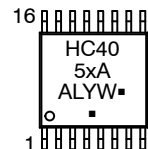
SOIC-16 WIDE  
DW SUFFIX  
CASE 751G



SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



x = Specific Device Code  
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G = Pb-Free Package  
▪ = Pb-Free Package

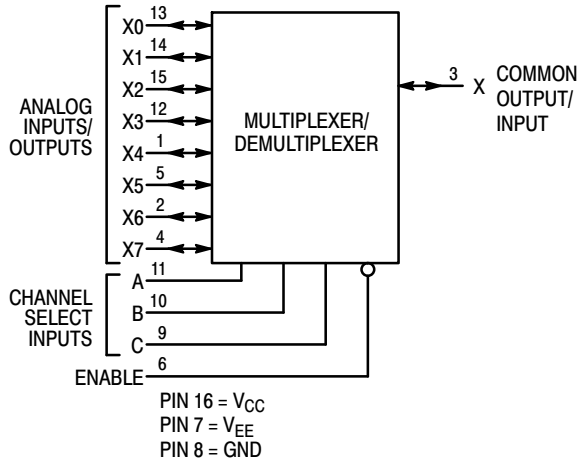
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

# MC74HC4051A, MC74HC4052A, MC74HC4053A

**LOGIC DIAGRAM  
MC74HC4051A  
Single-Pole, 8-Position Plus Common Off**

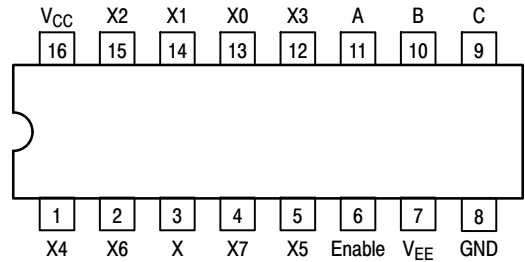


**FUNCTION TABLE - MC74HC4051A**

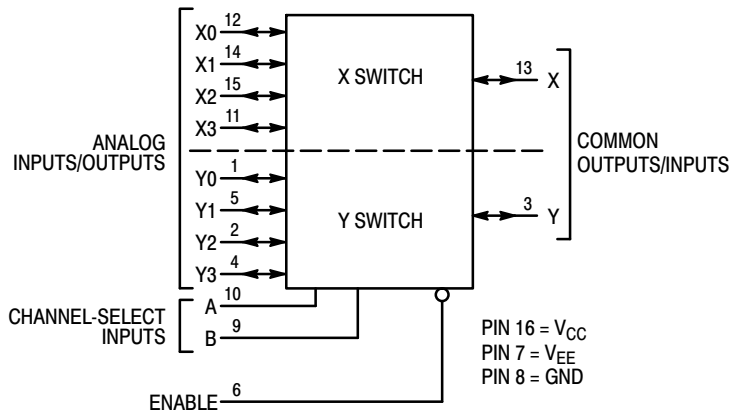
Control Inputs		Select			ON Channels
Enable		C	B	A	
L	L	L	L	L	X0
L	L	L	L	H	X1
L	L	L	H	L	X2
L	L	L	H	H	X3
L	H	L	L	L	X4
L	H	L	L	H	X5
L	H	H	L	L	X6
L	H	H	H	H	X7
H	X	X	X	X	NONE

X = Don't Care

**Pinout: MC74HC4051A (Top View)**



**LOGIC DIAGRAM  
MC74HC4052A  
Double-Pole, 4-Position Plus Common Off**

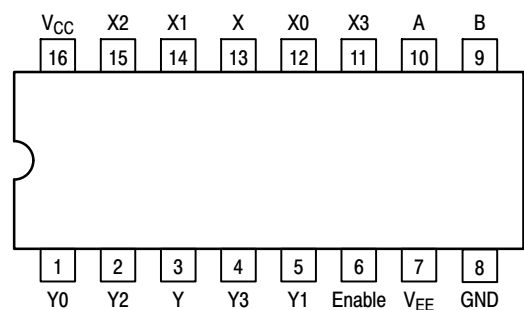


**FUNCTION TABLE - MC74HC4052A**

Control Inputs		Select		ON Channels	
Enable		B	A		
L	L	L	L	Y0	X0
L	L	L	H	Y1	X1
L	L	H	L	Y2	X2
L	L	H	H	Y3	X3
H	X	X	X	NONE	

X = Don't Care

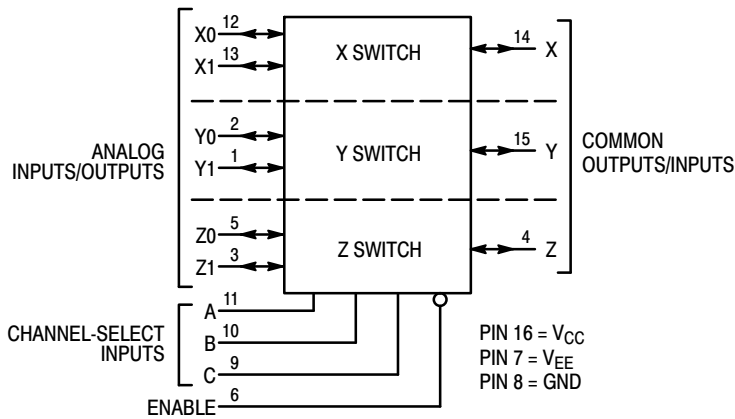
**Pinout: MC74HC4052A (Top View)**



# MC74HC4051A, MC74HC4052A, MC74HC4053A

FUNCTION TABLE – MC74HC4053A

**LOGIC DIAGRAM**  
**MC74HC4053A**  
**Triple Single-Pole, Double-Position Plus Common Off**

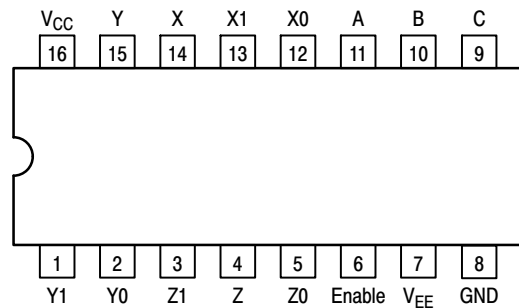


NOTE: This device allows independent control of each switch. Channel-Select Input A controls the X-Switch, Input B controls the Y-Switch and Input C controls the Z-Switch

Control Inputs		ON Channels			
Enable	Select	C	B	A	
L	L	L	L	L	Z0 Y0 X0
L	L	L	L	H	Z0 Y0 X1
L	L	L	H	L	Z0 Y1 X0
L	L	L	H	H	Z0 Y1 X1
L	H	L	L	L	Z1 Y0 X0
L	H	L	L	H	Z1 Y0 X1
L	H	H	L	L	Z1 Y1 X0
L	H	H	L	H	Z1 Y1 X1
H	X	X	X	X	NONE

X = Don't Care

Pinout: MC74HC4053A (Top View)



## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Positive DC Supply Voltage (Referenced to GND) (Referenced to V <sub>EE</sub> )	- 0.5 to + 7.0 - 0.5 to + 14.0	V
V <sub>EE</sub>	Negative DC Supply Voltage (Referenced to GND)	- 7.0 to + 5.0	V
V <sub>IS</sub>	Analog Input Voltage	V <sub>EE</sub> - 0.5 to V <sub>CC</sub> + 0.5	V
V <sub>in</sub>	Digital Input Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
I	DC Current, Into or Out of Any Pin	± 25	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP† EIAJ/SOIC Package† TSSOP Package†	750 500 450	mW
T <sub>stg</sub>	Storage Temperature Range	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
EIAJ/SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

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## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	Positive DC Supply Voltage (Referenced to GND) (Referenced to $V_{EE}$ )	2.0 2.0	6.0 12.0	V	
$V_{EE}$	Negative DC Supply Voltage, Output (Referenced to GND)	- 6.0	GND	V	
$V_{IS}$	Analog Input Voltage	$V_{EE}$	$V_{CC}$	V	
$V_{in}$	Digital Input Voltage (Referenced to GND)	GND	$V_{CC}$	V	
$V_{IO}^*$	Static or Dynamic Voltage Across Switch		1.2	V	
$T_A$	Operating Temperature Range, All Package Types	- 55	+ 125	°C	
$t_r, t_f$	Input Rise/Fall Time (Channel Select or Enable Inputs)	$V_{CC} = 2.0\text{ V}$ $V_{CC} = 3.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$	0 0 0 0	1000 600 500 400	ns

\*For voltage drops across switch greater than 1.2V (switch on), excessive  $V_{CC}$  current may be drawn; i.e., the current out of the switch may contain both  $V_{CC}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

## DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) $V_{EE} = \text{GND}$ , Except Where Noted

Symbol	Parameter	Condition	$V_{CC}$ V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
$V_{IH}$	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	$R_{on} = \text{Per Spec}$	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
$V_{IL}$	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	$R_{on} = \text{Per Spec}$	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
$I_{in}$	Maximum Input Leakage Current, Channel-Select or Enable Inputs	$V_{in} = V_{CC}$ or GND, $V_{EE} = - 6.0\text{ V}$	6.0	± 0.1	± 1.0	± 1.0	μA
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and $V_{IS} = V_{CC}$ or GND; $V_{EE} = \text{GND}$ $V_{IO} = 0\text{ V}$ $V_{EE} = - 6.0$	6.0	1	10	20	μA
			6.0	4	40	80	

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## DC CHARACTERISTICS — Analog Section

Symbol	Parameter	Condition	V <sub>CC</sub>	V <sub>EE</sub>	Guaranteed Limit			Unit
					-55 to 25°C	≤85°C	≤125°C	
R <sub>on</sub>	Maximum "ON" Resistance	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; V <sub>IS</sub> = V <sub>CC</sub> to V <sub>EE</sub> ; I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	4.5 4.5 6.0	0.0 - 4.5 - 6.0	190 120 100	240 150 125	280 170 140	Ω
		V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; V <sub>IS</sub> = V <sub>CC</sub> or V <sub>EE</sub> (Endpoints); I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	4.5 4.5 6.0	0.0 - 4.5 - 6.0	150 100 80	190 125 100	230 140 115	
ΔR <sub>on</sub>	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; V <sub>IS</sub> = 1/2 (V <sub>CC</sub> - V <sub>EE</sub> ); I <sub>S</sub> ≤ 2.0 mA	4.5 4.5 6.0	0.0 - 4.5 - 6.0	30 12 10	35 15 12	40 18 14	Ω
I <sub>off</sub>	Maximum Off-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; V <sub>IO</sub> = V <sub>CC</sub> - V <sub>EE</sub> ; Switch Off (Figure 3)	6.0	- 6.0	0.1	0.5	1.0	μA
	Maximum Off-Channel Leakage Current, Common Channel	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; V <sub>IO</sub> = V <sub>CC</sub> - V <sub>EE</sub> ; Switch Off (Figure 4)	6.0 6.0 6.0	- 6.0 - 6.0 - 6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	
I <sub>on</sub>	Maximum On-Channel Leakage Current, Channel-to-Channel	HC4051A	6.0	- 6.0	0.2	2.0	4.0	μA
		HC4052A HC4053A	6.0 6.0	- 6.0 - 6.0	0.1 0.1	1.0 1.0	2.0 2.0	

## AC CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit	
			-55 to 25°C	≤85°C	≤125°C		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Channel-Select to Analog Output (Figure 9)	2.0	270	320	350	ns	
		3.0	90	110	125		
		4.5	59	79	85		
		6.0	45	65	75		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0	40	60	70	ns	
		3.0	25	30	32		
		4.5	12	15	18		
		6.0	10	13	15		
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	160	200	220	ns	
		3.0	70	95	110		
		4.5	48	63	76		
		6.0	39	55	63		
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	245	315	345	ns	
		3.0	115	145	155		
		4.5	49	69	83		
		6.0	39	58	67		
C <sub>in</sub>	Maximum Input Capacitance, Channel-Select or Enable Inputs		10	10	10	pF	
C <sub>I/O</sub>	Maximum Capacitance (All Switches Off)	Analog I/O		35	35	35	pF
		Common O/I: HC4051A		130	130	130	
		HC4052A		80	80	80	
		HC4053A		50	50	50	
	Feed-through		1.0	1.0	1.0		
C <sub>PD</sub>	Power Dissipation Capacitance (Figure 13)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V, V <sub>EE</sub> = 0 V			pF		
		HC4051A	45				
	HC4052A	80					
	HC4053A	45					

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

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## ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V <sub>CC</sub> V	V <sub>EE</sub> V	Limit*			Unit
					25°C			
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 6)	f <sub>in</sub> = 1MHz Sine Wave; Adjust f <sub>in</sub> Voltage to Obtain 0dBm at V <sub>OS</sub> ; Increase f <sub>in</sub> Frequency Until dB Meter Reads -3dB; R <sub>L</sub> = 50Ω, C <sub>L</sub> = 10pF	2.25	-2.25	'51	'52	'53	MHz
			4.50	-4.50	80	95	120	
			6.00	-6.00	80	95	120	
-	Off-Channel Feed-through Isolation (Figure 7)	f <sub>in</sub> = Sine Wave; Adjust f <sub>in</sub> Voltage to Obtain 0dBm at V <sub>IS</sub> f <sub>in</sub> = 10kHz, R <sub>L</sub> = 600Ω, C <sub>L</sub> = 50pF	2.25	-2.25	-50			dB
		4.50	-4.50	-50				
-	Feedthrough Noise. Channel-Select Input to Common I/O (Figure 8)	V <sub>in</sub> ≤ 1MHz Square Wave (t <sub>r</sub> = t <sub>f</sub> = 6ns); Adjust R <sub>L</sub> at Setup so that I <sub>S</sub> = 0A; Enable = GND R <sub>L</sub> = 600Ω, C <sub>L</sub> = 50pF	2.25	-2.25	25			mV <sub>PP</sub>
			4.50	-4.50	105			
-	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to HC4051A)	f <sub>in</sub> = Sine Wave; Adjust f <sub>in</sub> Voltage to Obtain 0dBm at V <sub>IS</sub> f <sub>in</sub> = 10kHz, R <sub>L</sub> = 600Ω, C <sub>L</sub> = 50pF	2.25	-2.25	-50			dB
		4.50	-4.50	-50				
-	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to HC4051A)	f <sub>in</sub> = 1.0MHz, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 10pF	2.25	-2.25	-60			dB
		4.50	-4.50	-60				
THD	Total Harmonic Distortion (Figure 14)	f <sub>in</sub> = 1kHz, R <sub>L</sub> = 10kΩ, C <sub>L</sub> = 50pF THD = THD <sub>measured</sub> - THD <sub>source</sub> V <sub>IS</sub> = 4.0V <sub>PP</sub> sine wave V <sub>IS</sub> = 8.0V <sub>PP</sub> sine wave V <sub>IS</sub> = 11.0V <sub>PP</sub> sine wave	2.25	-2.25	0.10			%
			4.50	-4.50	0.08			
			6.00	-6.00	0.05			

\*Limits not tested. Determined by design and verified by qualification.

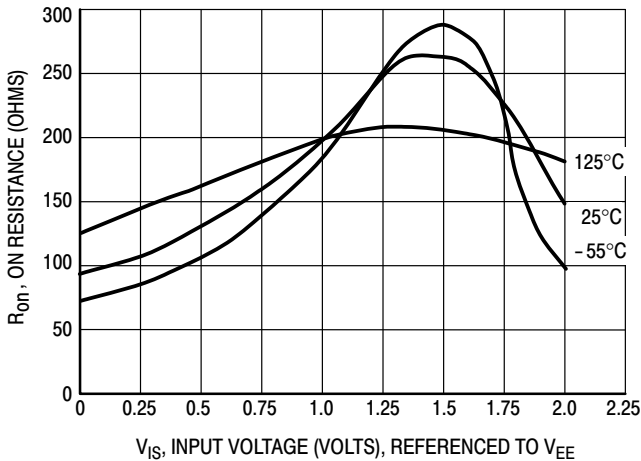


Figure 1a. Typical On Resistance, V<sub>CC</sub> - V<sub>EE</sub> = 2.0 V

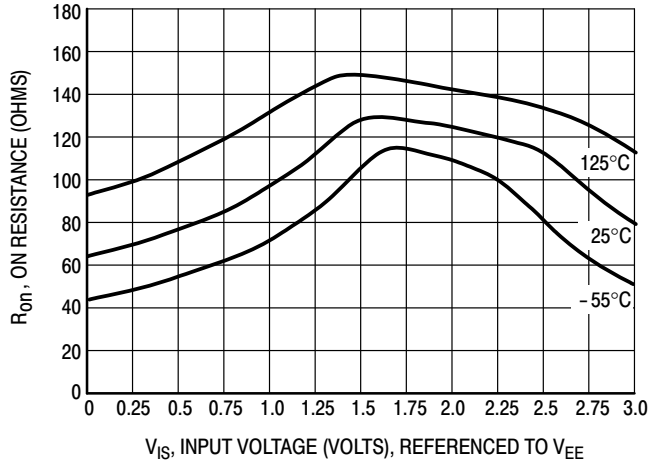


Figure 1b. Typical On Resistance, V<sub>CC</sub> - V<sub>EE</sub> = 3.0 V

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Figure 1c. Typical On Resistance,  $V_{CC} - V_{EE} = 4.5 \text{ V}$



Figure 1d. Typical On Resistance,  $V_{CC} - V_{EE} = 6.0 \text{ V}$

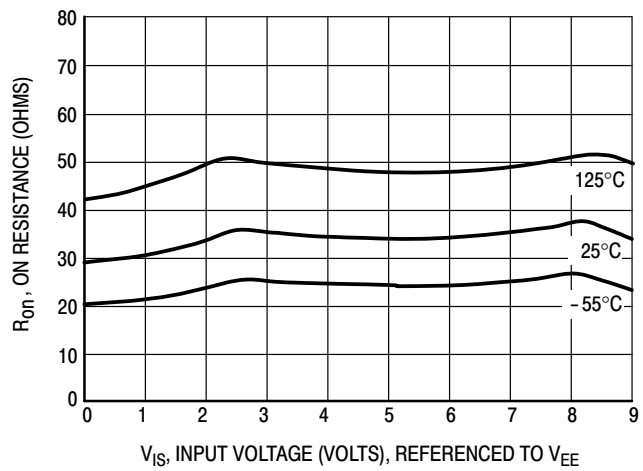


Figure 1e. Typical On Resistance,  $V_{CC} - V_{EE} = 9.0 \text{ V}$

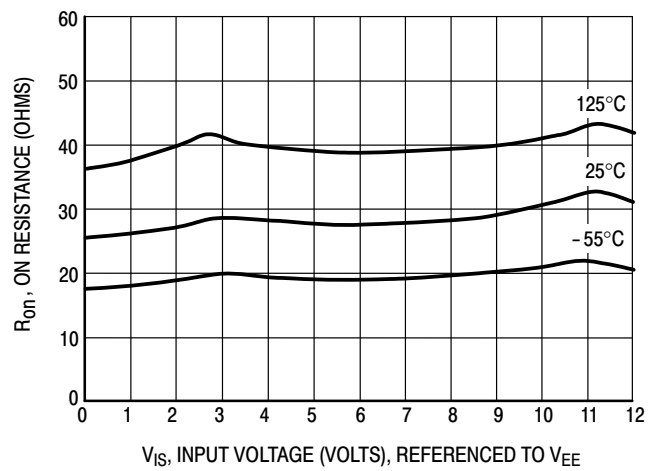


Figure 1f. Typical On Resistance,  $V_{CC} - V_{EE} = 12.0 \text{ V}$

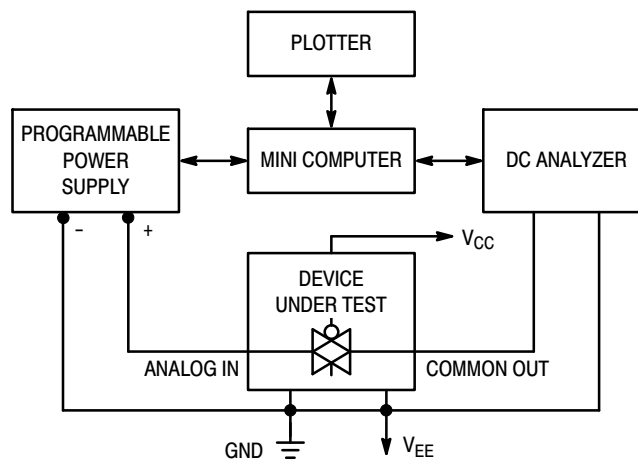


Figure 2. On Resistance Test Set-Up

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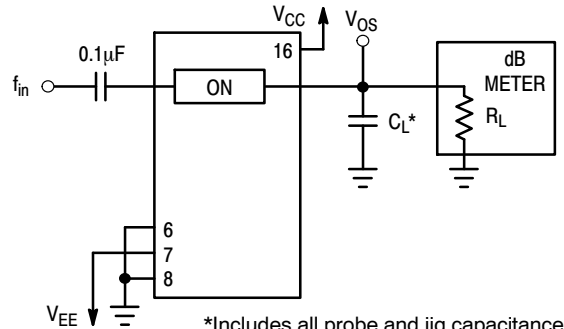
**Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up**



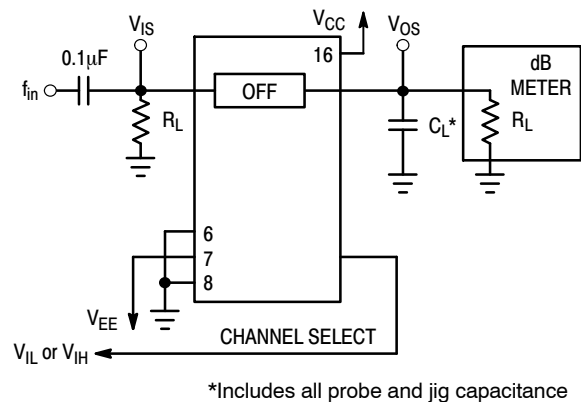
**Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up**



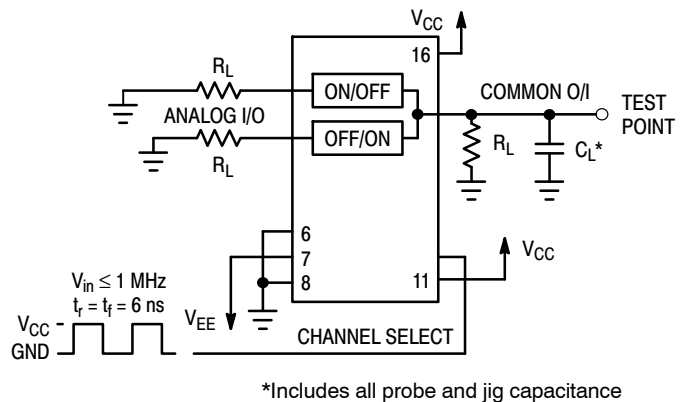
**Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up**



**Figure 6. Maximum On Channel Bandwidth, Test Set-Up**



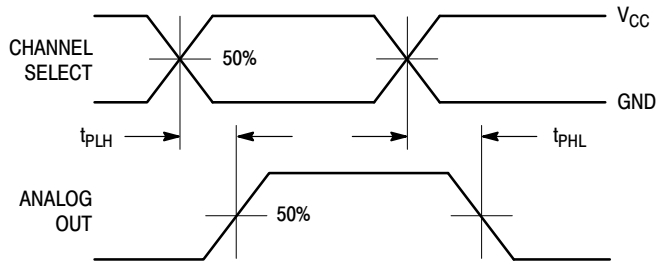
**Figure 7. Off Channel Feedthrough Isolation, Test Set-Up**



**Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set-Up**



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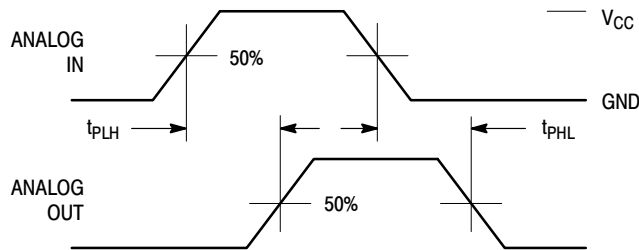


**Figure 9a. Propagation Delays, Channel Select to Analog Out**



\*Includes all probe and jig capacitance

**Figure 9b. Propagation Delay, Test Set-Up Channel Select to Analog Out**

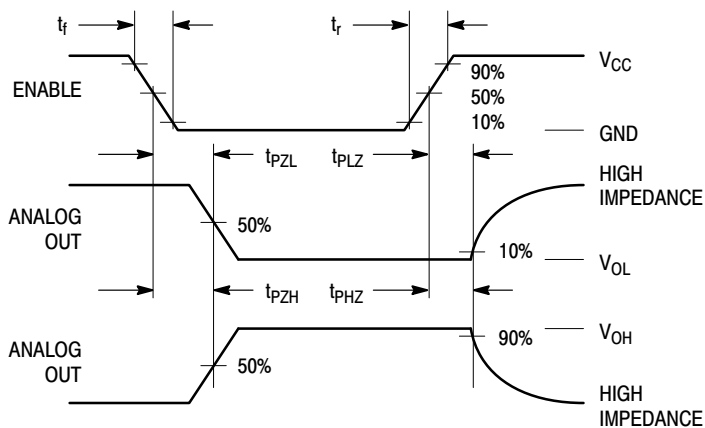


**Figure 10a. Propagation Delays, Analog In to Analog Out**

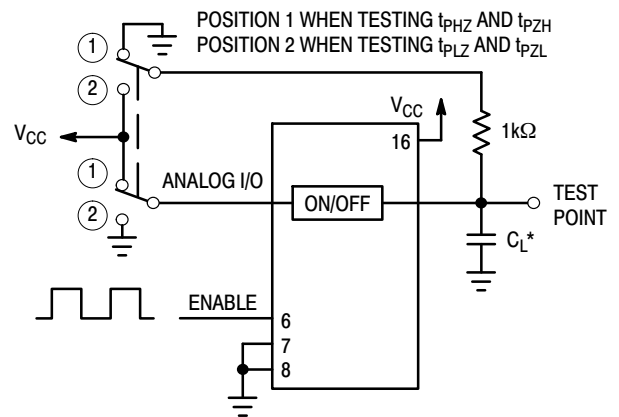


\*Includes all probe and jig capacitance

**Figure 10b. Propagation Delay, Test Set-Up Analog In to Analog Out**

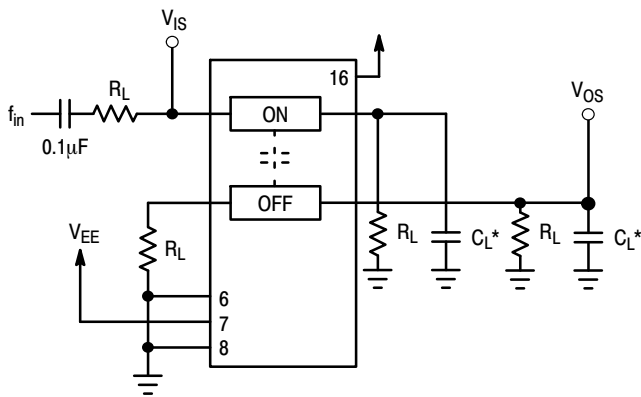


**Figure 11a. Propagation Delays, Enable to Analog Out**



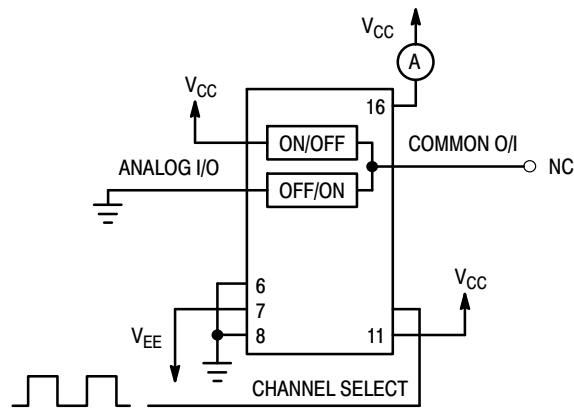
**Figure 11b. Propagation Delay, Test Set-Up Enable to Analog Out**

# MC74HC4051A, MC74HC4052A, MC74HC4053A

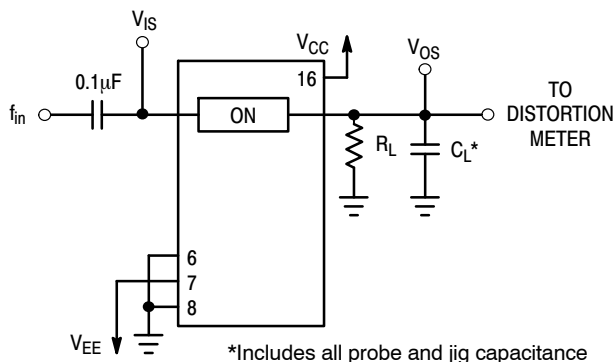


\*Includes all probe and jig capacitance

**Figure 12. Crosstalk Between Any Two Switches, Test Set-Up**

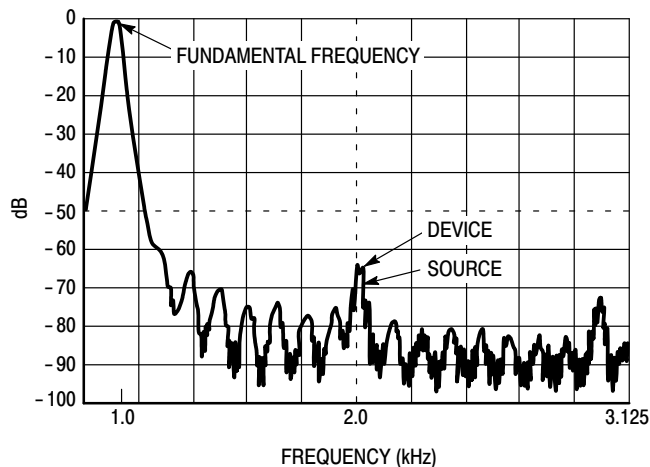


**Figure 13. Power Dissipation Capacitance, Test Set-Up**



\*Includes all probe and jig capacitance

**Figure 14a. Total Harmonic Distortion, Test Set-Up**



**Figure 14b. Plot, Harmonic Distortion**

## APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at  $V_{CC}$  or GND logic levels.  $V_{CC}$  being recognized as a logic high and GND being recognized as a logic low. In this example:

$$\begin{aligned} V_{CC} &= +5V = \text{logic high} \\ \text{GND} &= 0V = \text{logic low} \end{aligned}$$

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and  $V_{EE}$ . The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below  $V_{EE}$ . In this example, the difference between  $V_{CC}$  and  $V_{EE}$  is ten volts. Therefore, using the configuration of Figure 15, a maximum analog signal of ten volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and

outputs to  $V_{CC}$  or GND through a low value resistor helps minimize crosstalk and feed-through noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$\begin{aligned} V_{CC} - \text{GND} &= 2 \text{ to } 6 \text{ volts} \\ V_{EE} - \text{GND} &= 0 \text{ to } -6 \text{ volts} \\ V_{CC} - V_{EE} &= 2 \text{ to } 12 \text{ volts} \\ &\text{and } V_{EE} \leq \text{GND} \end{aligned}$$

When voltage transients above  $V_{CC}$  and/or below  $V_{EE}$  are anticipated on the analog channels, external Germanium or Schottky diodes ( $D_x$ ) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

# MC74HC4051A, MC74HC4052A, MC74HC4053A

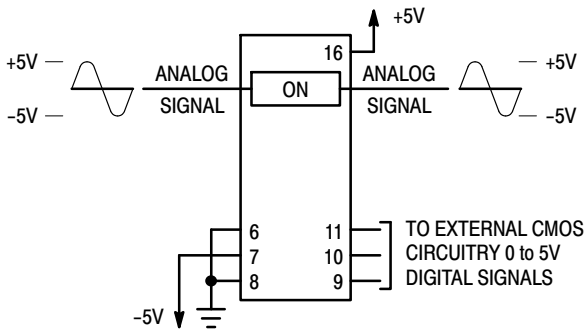


Figure 15. Application Example

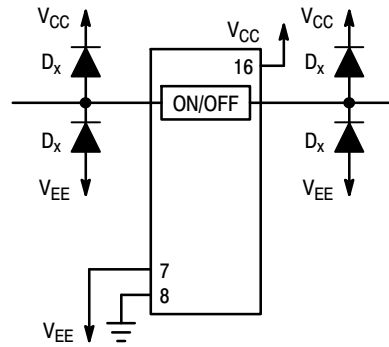
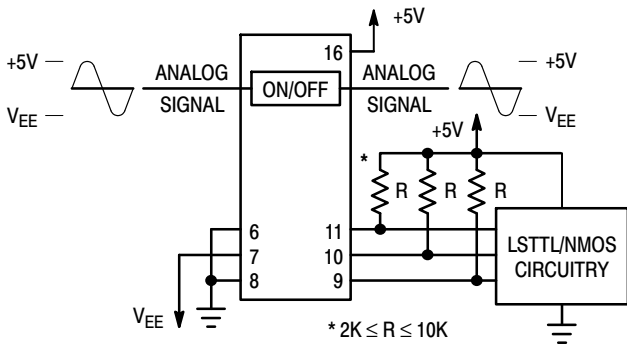
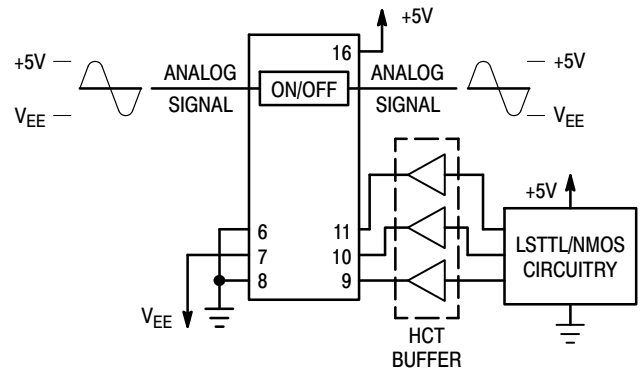


Figure 16. External Germanium or Schottky Clipping Diodes



a. Using Pull-Up Resistors



b. Using HCT Interface

Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

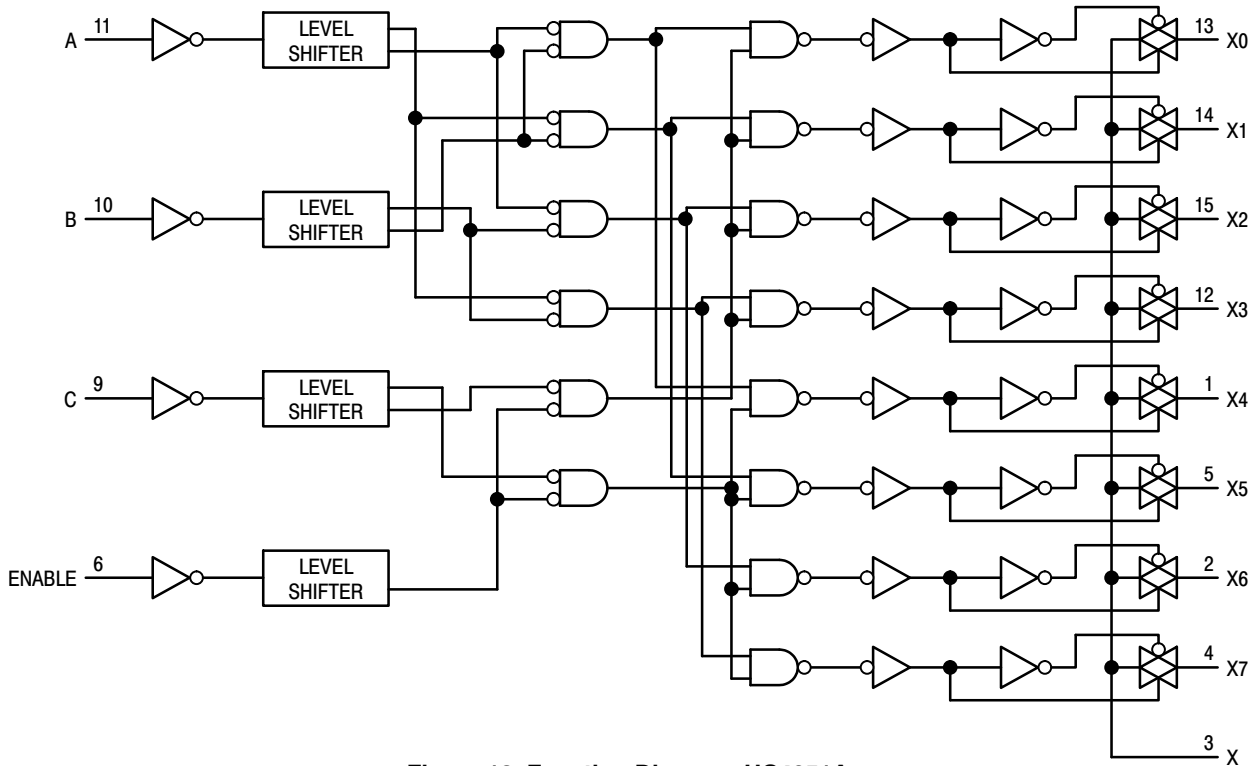


Figure 18. Function Diagram, HC4051A

MC74HC4051A, MC74HC4052A, MC74HC4053A



Figure 19. Function Diagram, HC4052A

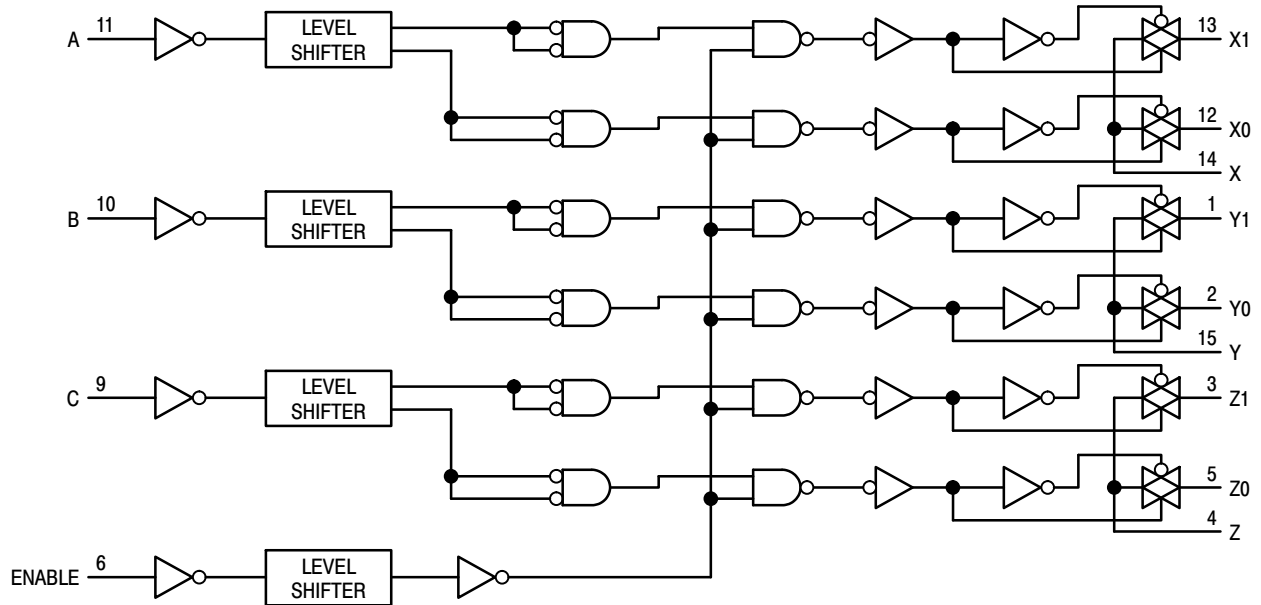


Figure 20. Function Diagram, HC4053A

## MC74HC4051A, MC74HC4052A, MC74HC4053A

### ORDERING INFORMATION

Device	Package	Shipping†
MC74HC4051ANG	PDIP-16 (Pb-Free)	500 Units / Box
MC74HC4051ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC4051ADR2G		2500 Units / Tape & Reel
NLV74HC4051ADR2G*		2500 Units / Tape & Reel
MC74HC4051ADWG	SOIC-16 WIDE (Pb-Free)	48 Units / Rail
MC74HC4051ADWR2G		1000 Units / Tape & Reel
NLVHC4051ADWR2G*		1000 Units / Tape & Reel
MC74HC4051ADTG	TSSOP-16 (Pb-Free)	96 Units / Rail
MC74HC4051ADTR2G		2500 Units / Tape & Reel
NLVHC4051ADTR2G*		2500 Units / Tape & Reel
MC74HC4052ANG	PDIP-16 (Pb-Free)	500 Units / Box
MC74HC4052ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC4052ADR2G		2500 Units / Tape & Reel
NLV74HC4052ADR2G*		2500 Units / Tape & Reel
MC74HC4052ADWG	SOIC-16 WIDE (Pb-Free)	48 Units / Rail
MC74HC4052ADWR2G		1000 Units / Tape & Reel
MC74HC4052ADTG	TSSOP-16 (Pb-Free)	96 Units / Rail
MC74HC4052ADTR2G		2500 Units / Tape & Reel
NLV74HC4052ADTR2G*		2500 Units / Tape & Reel
NLVHC4052ADTR2G*		2500 Units / Tape & Reel
MC74HC4053ANG	PDIP-16 (Pb-Free)	500 Units / Box
MC74HC4053ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC4053ADR2G		2500 Units / Tape & Reel
NLV74HC4053ADR2G*		2500 Units / Tape & Reel
MC74HC4053ADWG	SOIC-16 WIDE (Pb-Free)	48 Units / Rail
MC74HC4053ADWR2G		1000 Units / Tape & Reel
NLV74HC4053ADWR2G*		1000 Units / Tape & Reel
MC74HC4053ADTG	TSSOP-16 (Pb-Free)	96 Units / Rail
MC74HC4053ADTR2G		2500 Units / Tape & Reel
NLVHC4053ADTR2G*		2500 Units / Tape & Reel

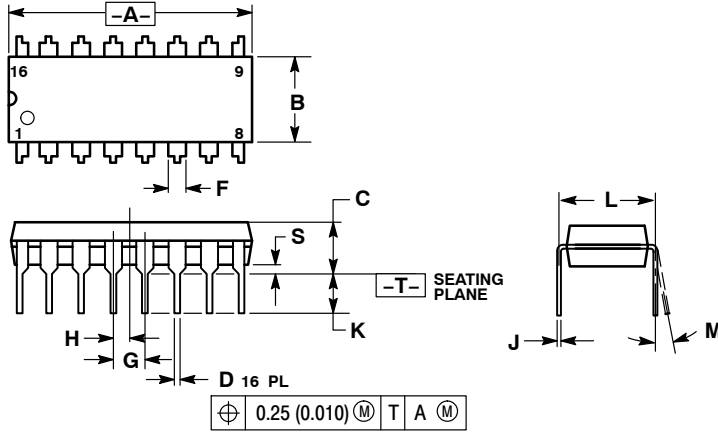
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MC74HC4051A, MC74HC4052A, MC74HC4053A

## PACKAGE DIMENSIONS

PDIP-16  
N SUFFIX  
CASE 648-08  
ISSUE T



NOTES:

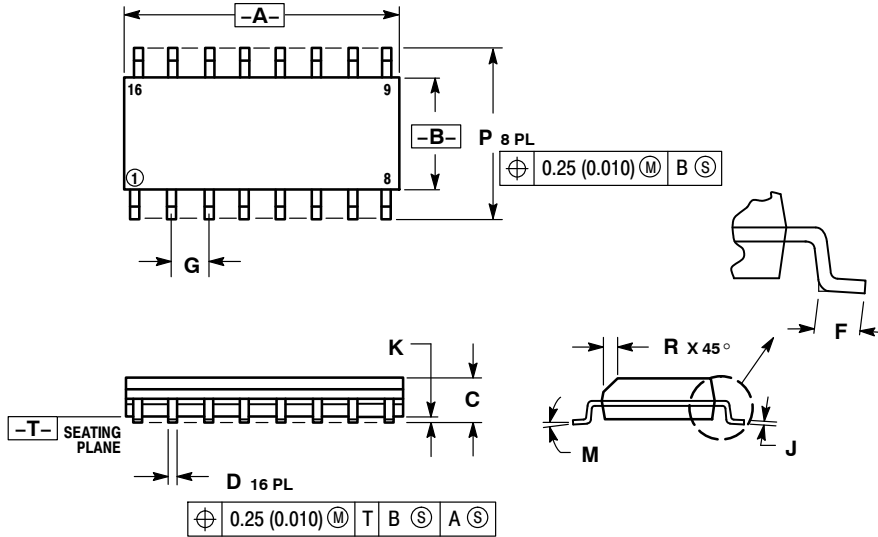
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 <sup>°</sup>	10 <sup>°</sup>	0 <sup>°</sup>	10 <sup>°</sup>
S	0.020	0.040	0.51	1.01

# MC74HC4051A, MC74HC4052A, MC74HC4053A

## PACKAGE DIMENSIONS

SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE K

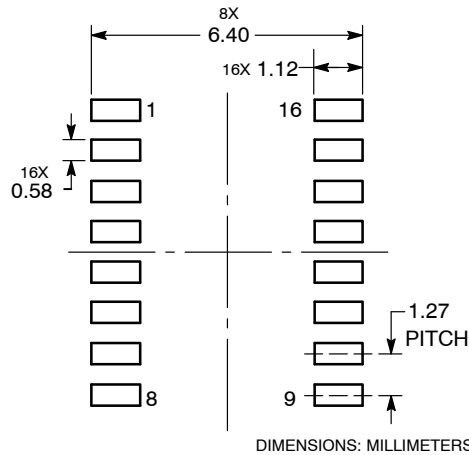


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

### SOLDERING FOOTPRINT\*

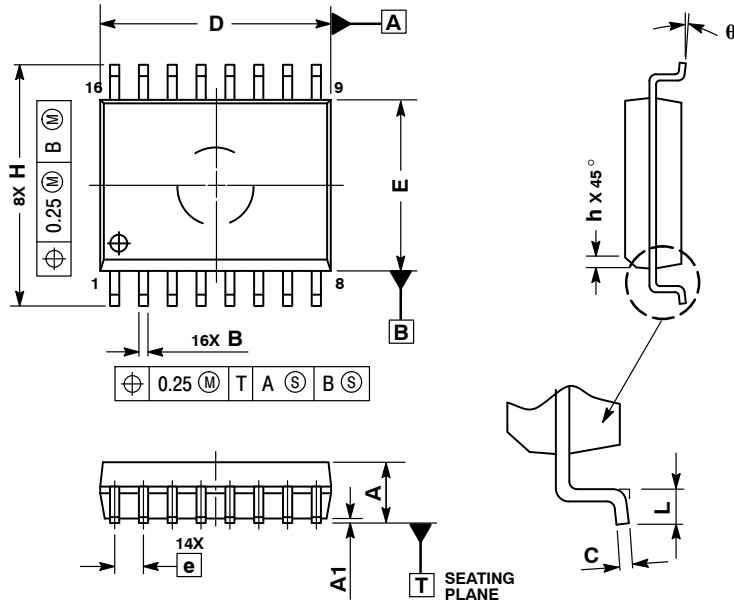


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74HC4051A, MC74HC4052A, MC74HC4053A

## PACKAGE DIMENSIONS

SOIC-16 WB  
DW SUFFIX  
CASE 751G-03  
ISSUE D

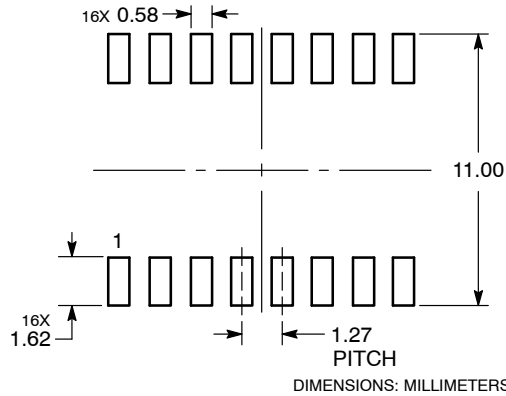


**NOTES:**

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0°	7°

### SOLDERING FOOTPRINT

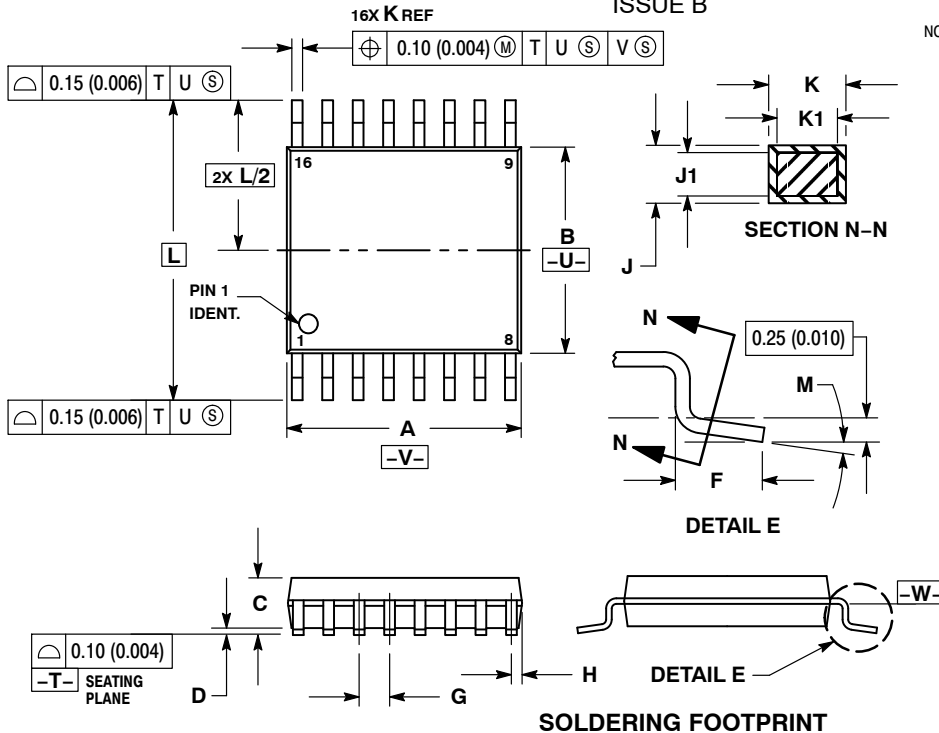




# MC74HC4051A, MC74HC4052A, MC74HC4053A

## PACKAGE DIMENSIONS

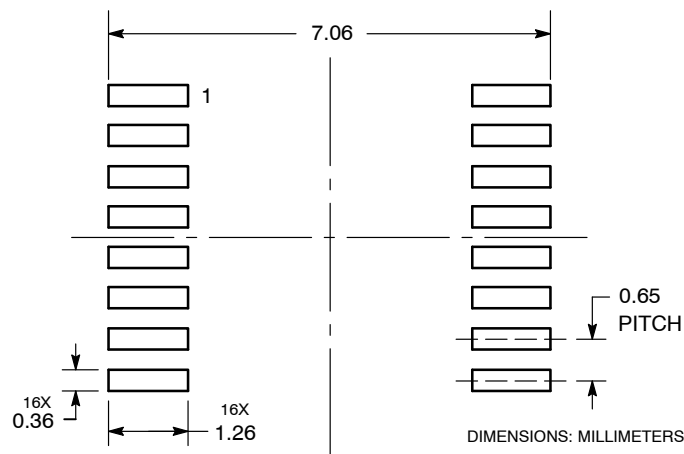
TSSOP-16  
DT SUFFIX  
CASE 948F  
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



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