

FDB28N30

N-Channel MOSFET

300V, 28A, 0.129Ω

Features

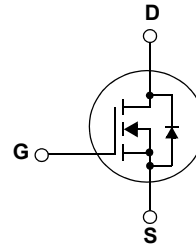
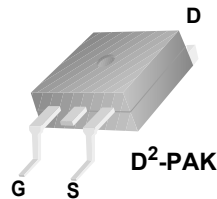
- $R_{DS(on)} = 0.108\Omega$ (Typ.) @ $V_{GS} = 10V, I_D = 14A$
- Low gate charge (Typ. 39nC)
- Low C_{rss} (Typ. 35pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant



Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted*

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	300	V
V_{GSS}	Gate to Source Voltage	±30	V
I_D	Drain Current	-Continuous ($T_C = 25^\circ\text{C}$)	28
		-Continuous ($T_C = 100^\circ\text{C}$)	19
I_{DM}	Drain Current	- Pulsed (Note 1)	112
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	588
I_{AR}	Avalanche Current	(Note 1)	28
E_{AR}	Repetitive Avalanche Energy	(Note 1)	25
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	250
		- Derate above 25°C	2.0
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}^*$	Thermal Resistance, Junction to Ambient*	40	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

*When mounted on the minimum pad size recommended (PCB Mount)

Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB28N30	FDB28N30TM	D2-PAK	330mm	24mm	800

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	300	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.4	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 300\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 240\text{V}, T_C = 125^\circ\text{C}$	-	-	1 10	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 14\text{A}$	-	0.108	0.129	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{V}, I_D = 14\text{A}$ (Note 4)	-	24.8	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	1690	2250	pF
C_{oss}	Output Capacitance		-	305	405	pF
C_{rss}	Reverse Transfer Capacitance		-	35	50	pF
Q_g	Total Gate Charge at 10V	$V_{DS} = 240\text{V}, I_D = 28\text{A}$ $V_{GS} = 10\text{V}$ (Note 4, 5)	-	39	50	nC
Q_{gs}	Gate to Source Gate Charge		-	12	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	17	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 150\text{V}, I_D = 28\text{A}$ $R_G = 25\Omega$ (Note 4, 5)	-	35	80	ns
t_r	Turn-On Rise Time		-	135	280	ns
$t_{d(off)}$	Turn-Off Delay Time		-	79	168	ns
t_f	Turn-Off Fall Time		-	69	148	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	28	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	112	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 28\text{A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 28\text{A}$ $di_F/dt = 100\text{A}/\mu\text{s}$ (Note 4)	-	279	-	ns
Q_{rr}	Reverse Recovery Charge		-	2.7	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 1.5\text{mH}, I_{AS} = 28\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 28\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

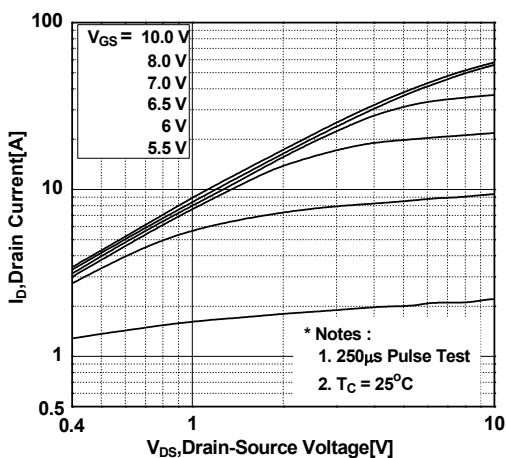


Figure 2. Transfer Characteristics

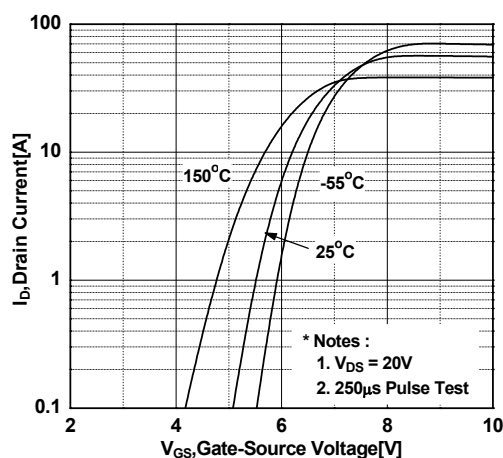


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

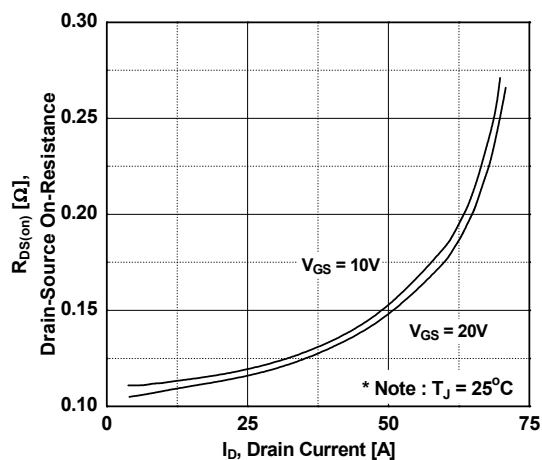


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

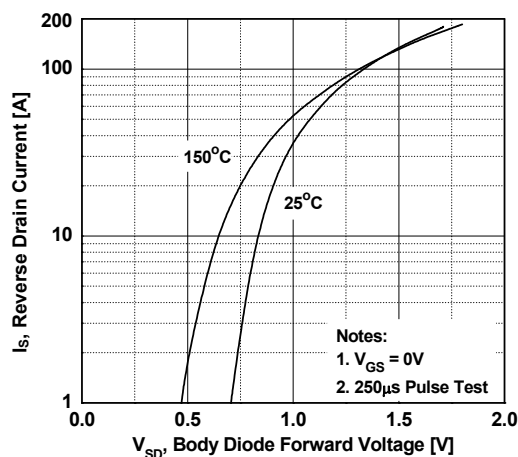


Figure 5. Capacitance Characteristics

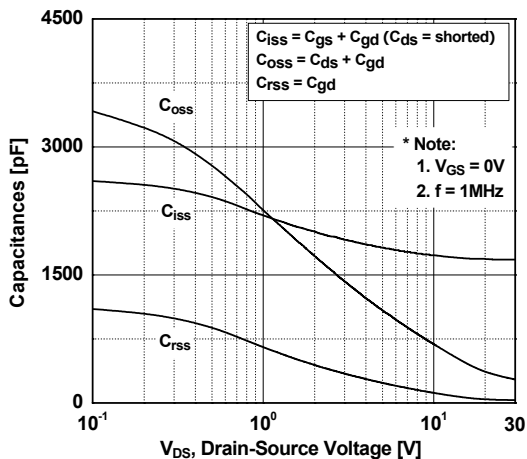
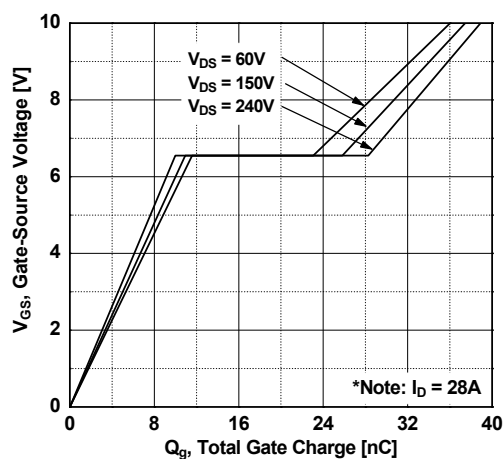


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

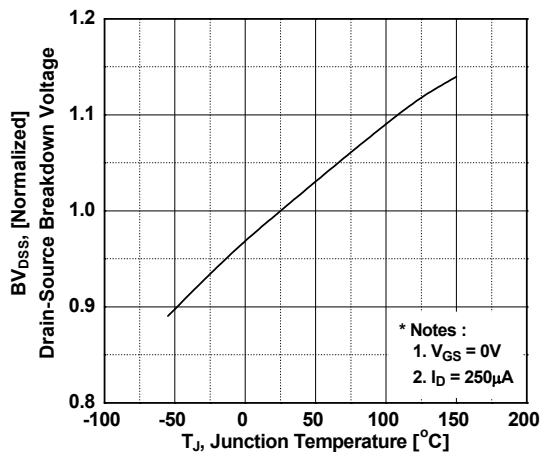


Figure 8. On-Resistance Variation vs. Temperature

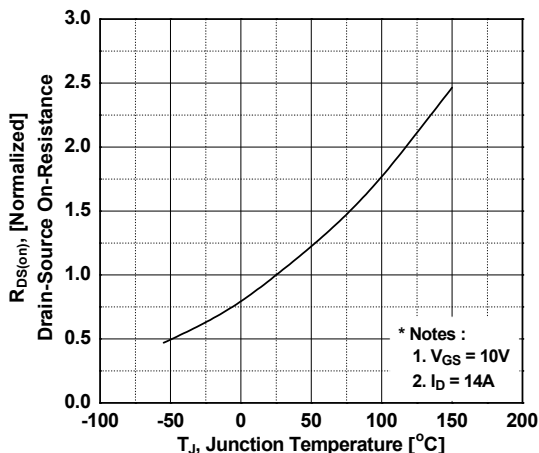


Figure 9. Maximum Safe Operating Area

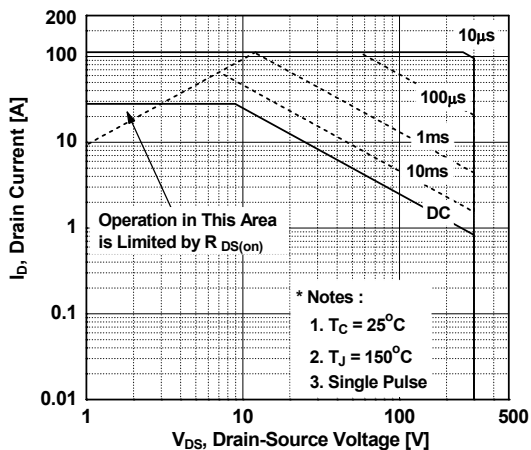


Figure 10. Maximum Drain Current vs. Case Temperature

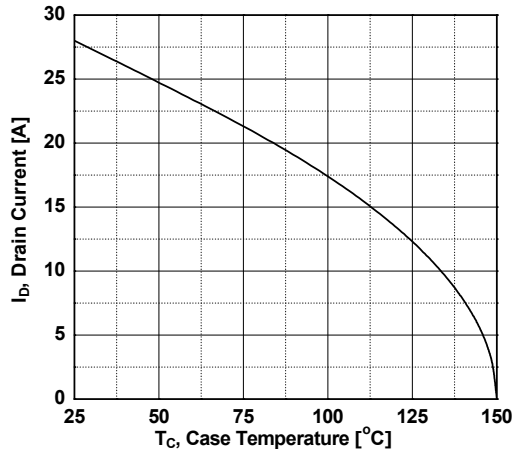
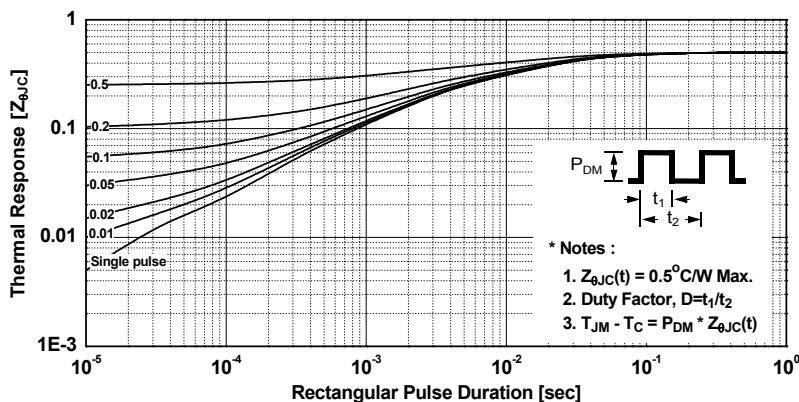
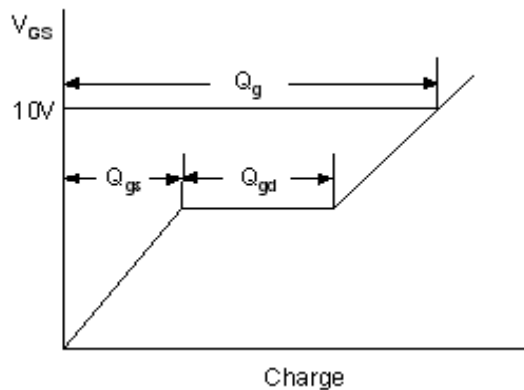
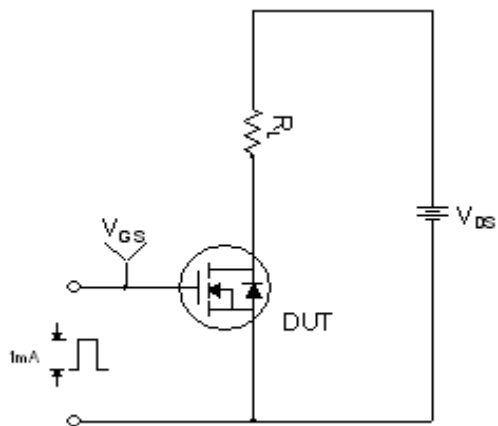


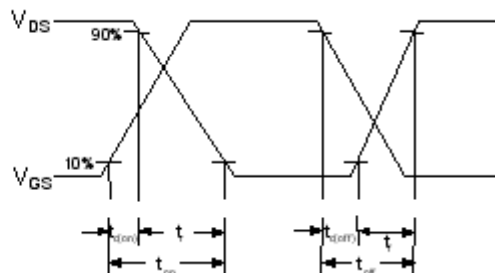
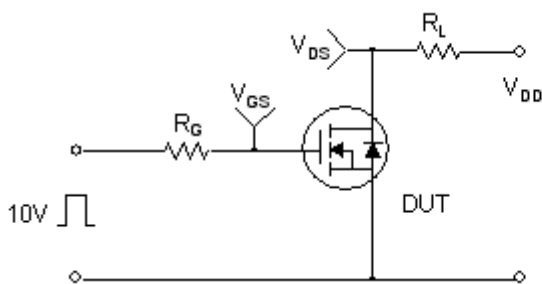
Figure 11. Transient Thermal Response Curve



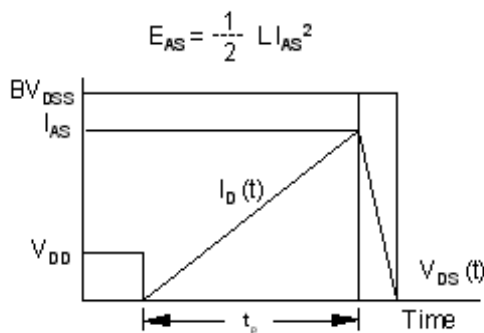
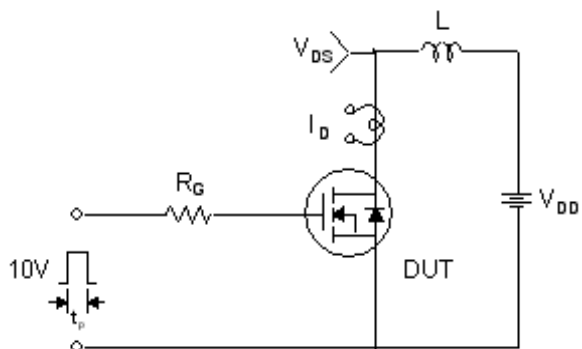
Gate Charge Test Circuit & Waveform



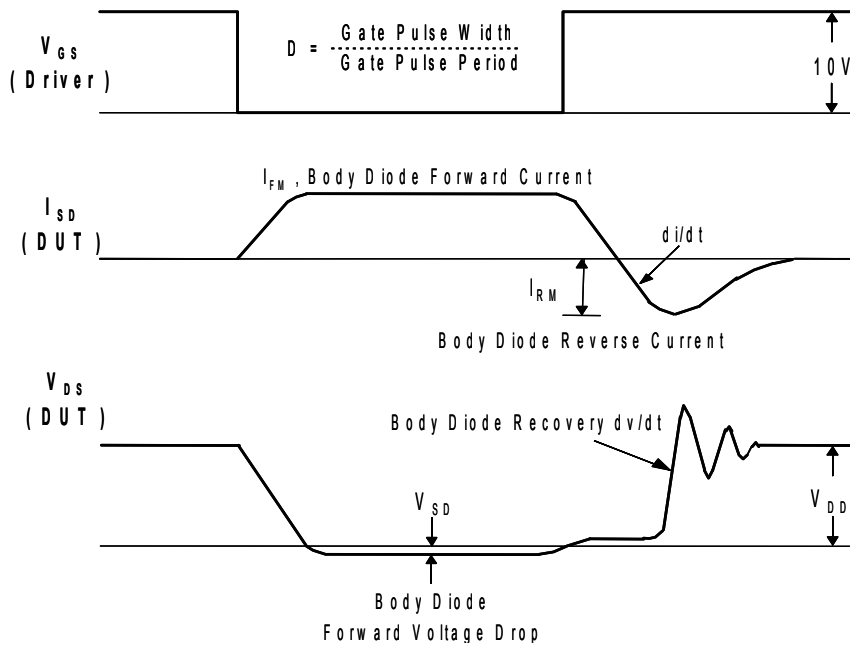
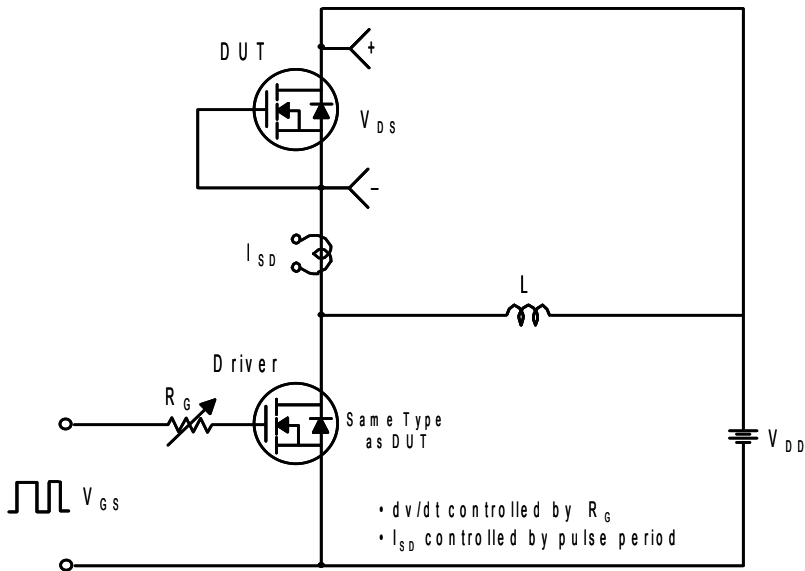
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

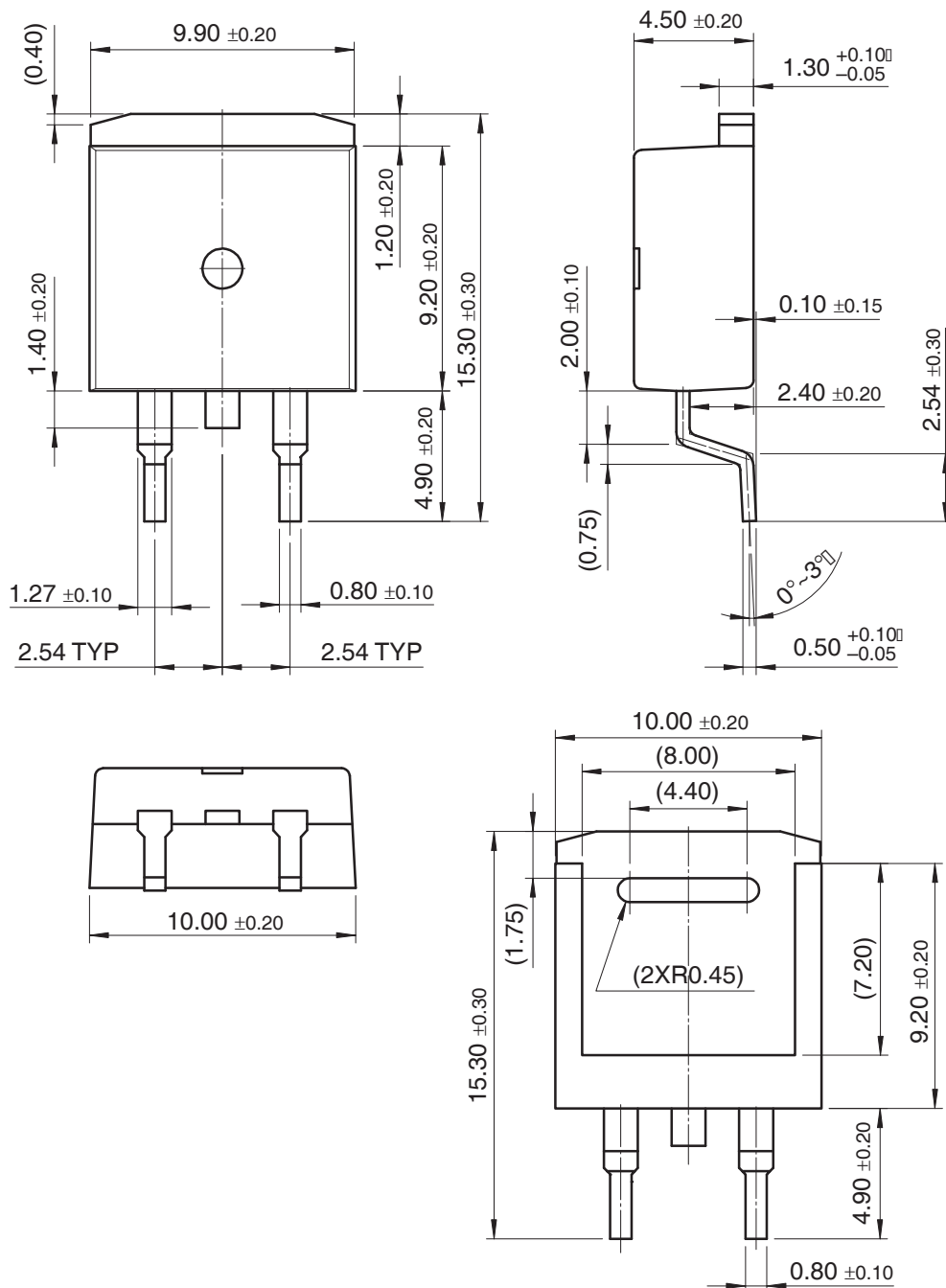


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions


D²PAK





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Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I26



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