# DS1077
# EconOscillator/Divider

www.maxim-ic.com

## FEATURES

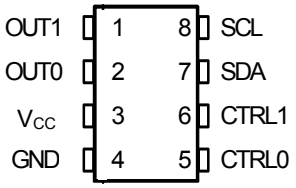
- Processor-controlled or standalone solid-state oscillator
- Frequency changes on-the-fly
- Dual low-jitter, synchronous fixed frequency outputs
- 2-wire serial interface
- Frequency outputs 8.1kHz to 133MHz
- ±0.5% variation over temp (+25°C to +70°C)
- ±0.5% initial tolerance
- Nonvolatile (NV) frequency settings
- Single 5V supply
- No external components
- Power-down mode
- Synchronous output gating

## STANDARD FREQUENCY OPTION

Note: x denotes package option

| | | | |
|---|---|---|---|
| DS1077x-133 | 133.333MHz | to | 16.2kHz |
| DS1077x-125 | 125.000MHz | to | 15.2kHz |
| DS1077x-120 | 120.000MHz | to | 14.6kHz |
| DS1077x-100 | 100.000MHz | to | 12.2kHz |
| DS1077x-66 | 66.666MHz | to | 8.1kHz |

## PIN ASSIGNMENT




150mil SO
118mil µSOP Package

## PIN DESCRIPTION

| | |
|---|---|
| OUT1 | - Main Oscillator Output |
| OUT0 | - Reference Output |
| $V_{CC}$ | - Power Supply Voltage |
| GND | - Ground |
| CTRL1 | - Control Pin for OUT1 |
| CTRL0 | - Control Pin for OUT0 |
| SDA | - 2-Wire Serial Data Input/Output |
| SCL | - 2-Wire Serial Clock |

## ORDERING INFORMATION

Note: XXX denotes frequency option

| | |
|---|---|
| DS1077Z-XXX | 8-Pin 150mil SO |
| DS1077U-XXX | 8-Pin 118mil µSOP |

## DESCRIPTION

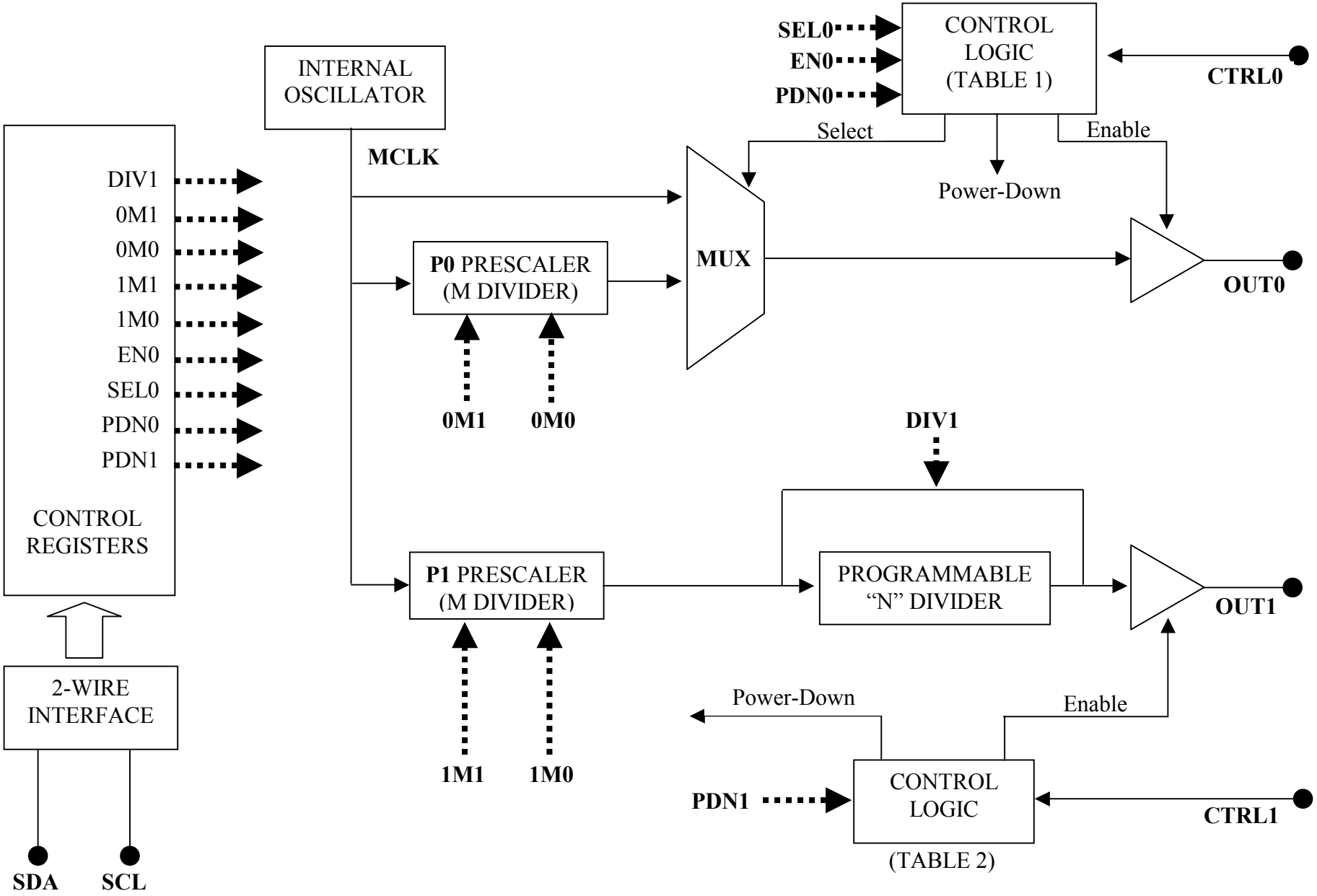
The DS1077 is a dual-output, programmable, fixed-frequency oscillator requiring no external components for operation. The DS1077 can be used as a processor-controlled frequency synthesizer or as a standalone oscillator. The two synchronous output operating frequencies are user-adjustable in submultiples of the master frequency through the use of two on-chip programmable prescalers and a divider. The specific output frequencies chosen are stored in NV (EEPROM) memory. The DS1077 defaults to these values upon power-up.

The DS1077 features a 2-wire serial interface that allows in-circuit on-the-fly programming of the programmable prescalers (P0 & P1) and divider (N) with the desired values being stored in NV (EEPROM) memory. Design changes can be accommodated in-circuit on-the-fly by simply programming different values into the device (or reprogramming previously programmed devices). Alternatively, for fixed frequency applications, previously programmed devices can be used and no connection to the serial interface is required. Pre-programmed devices can be ordered in customer-requested frequencies.

The DS1077 is available in 8-pin SO or µSOP packages, allowing the generation of a clock signal easily, economically, and using minimal board area. Chip-scale packaging is also available on request.

*EconOscillator is a trademark of Dallas Semiconductor.*

## **BLOCK DIAGRAM 1077** Figure1



## OVERVIEW

A block diagram of the DS1077 is shown in Figure 1. The DS1077 consists of four major components: 1) Internal Master Oscillator, 2) Prescalers, 3) Programmable Divider, and 4) Control Registers.

The internal oscillator is factory-trimmed to provide a master frequency (Master CLK) that can be routed directly to the outputs (OUT0 & OUT1) or through separate prescalers (P0 & P1). OUT1 can also be routed through an additional divider (N).

The Prescaler (P0) divides the Master Clock by 1, 2, 4, or 8 to be routed directly to the OUT0 pin.

The Prescaler (P1) divides the Master Clock by 1, 2, 4, or 8, which can be routed directly to the OUT1 pin or to the Divider (N) input, which is then routed to the OUT1 pin.

The Programmable Divider (N) divides the Prescaler Output (P1) by any number selected between 2 and 1025 to provide the Main Output (OUT1) or it can be bypassed altogether by use of the DIV1 register bit. The value of N is stored in the DIV register.

The Control Registers are user-programmable through a 2-wire serial interface to determine operating frequency (values of P0, P1, & N) and modes of operation. The register values are stored in EEPROM and therefore only need to be programmed to alter frequencies and operating modes.

## PIN DESCRIPTIONS

**Output 1 (OUT1)**—This pin is the main oscillator output; its frequency is determined by the control register settings for the prescaler P1 (mode bits 1M1 & 1M0) and divider N (DIV word).

**Output 0 (OUT0)**—A reference output, OUT0, is taken from the output of the reference select Mux. Its frequency is determined by the control register settings for CTRL0 and values of Prescaler P0 (mode bits 0M1 & 0M0) (see Table 1).

**Control Pin 0 (CTRL0)**—A multifunctional input pin that can be selected as a MUX SELECT, OUTPUT ENABLE and/or a POWER-DOWN. Its function is determined by the user-programmable control register values EN0, SEL0, and PDN0 (see Table 1).

**Control Pin 1 (CTRL1)**—A multifunctional input pin that can be selected as a OUTPUT ENABLE and/or a POWER-DOWN. Its function is determined by the user-programmable control register value of PDN1 (see Table 2).

**Serial Data Input/Output (SDA)—**Input/Output pin for the 2-wire serial interface used for data transfer.

**Serial Clock Input (SCL)**—Input pin for the 2-wire serial interface used to synchronize data movement on the serial interface.

## DEVICE MODE USING OUT0 Table 1

| EN0 (BIT) | SEL0 (BIT) | PDN0 (BIT) | CTRL0 (PIN) | OUT0 (PIN) | CTRL0 FUNCTION | DEVICE MODE |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | HI-Z | POWER-DOWN* | POWER-DOWN |
| | | | 0 | HI-Z | | ACTIVE |
| 0 | 1 | 0 | 1 | MCLK/M | MUX SELECT | ACTIVE |
| | | | 0 | MCLK | | |
| 1 | 0 | 0 | 1 | HI-Z | OUTPUT ENABLE | ACTIVE |
| | | | 0 | MCLK | | |
| 1 | 1 | 0 | 1 | HI-Z | OUTPUT ENABLE | ACTIVE** |
| | | | 0 | MCLK/M | | |
| X | 0 | 1 | 1 | HI-Z | POWER-DOWN | POWER-DOWN |
| | | | 0 | MCLK | | ACTIVE |
| X | 1 | 1 | 1 | HI-Z | POWER-DOWN | POWER-DOWN |
| | | | 0 | MCLK/M | | ACTIVE |

*This mode is for applications where OUT0 is not used, but CTRL0 is used as a device shutdown.
**Default Condition

## DEVICE MODE USING OUT1 Table 2

| PDN1 (BIT) | CTRL1 (PIN) | CTRL1 FUNCTION | OUT1 | DEVICE MODE |
|---|---|---|---|---|
| 0 | 0 | OUTPUT ENABLE | OUT CLK | ACTIVE** |
| 0 | 1 | OUTPUT ENABLE | HI-Z | ACTIVE** |
| 1 | 0 | POWER-DOWN | OUT CLK | ACTIVE |
| 1 | 1 | POWER-DOWN | HI-Z | POWER-DOWN |

**Default Condition

**NOTE:**
Both CTRL0 and CTRL1 can be configured as power-downs. They are internally "OR" connected so that either of the control pins can be used to provide a power-down function for the whole device, subject to appropriate settings of the PDN0 and PDN1 register bits (see Table 3).

## SHUTDOWN CONTROL WITH PDN0 AND PDN1 Table 3

| PDN0 (BIT) | PDN1 (BIT) | SHUTDOWN CONTROL |
|---|---|---|
| 0 | 0 | NONE* |
| 0 | 1 | CTRL1 |
| 1 | 0 | CTRL0 |
| 1 | 1 | CTRL0 OR CTRL1 |

*CTRL0 performs a power-down if SEL0 and EN0 are both 0 (see Table 1).

## REGISTER FUNCTIONS

The user programmable registers can be programmed by the user to determine the mode of operation (MUX), operating frequency (DIV), and bus settings (BUS). Details of how these registers are programmed can be found in a later section; in this section the functions of the registers are described. The register settings are nonvolatile, the values being stored automatically or as required in EEPROM when the registers are programmed via the SDA and SCL pins.

## MUX WORD

| | MSB | | | | | | | LSB | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Name** | * | **PDN1** | **PDN0** | **SEL0** | **EN0** | **0M1** | **0M0** | **1M1** | **1M0** | **DIV1** | - | - | - | - | - | - |
| Default setting | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | x | x | x | x | x | x |
| | | | | | | first data byte | | | | | second data byte | | | | | |

*This bit must be set to zero.

### DIV1 (bit)

This bit allows the output of the Prescaler P1 to be routed directly to the OUT1 pin (DIV1 = 1). The N divider is bypassed so the programmed value of N is ignored. If DIV1 = 0 (default) the N divider functions normally.

### 0M1, 0M0, 1M1, 1M0 (bits)

These bits set the prescalers P0 and P1, to divide by 1, 2, 4, or 8 (see Table 4).

## PRESCALER DIVISOR M SETTINGS Table 4

| 0M1 | 0M0 | Prescaler P0 Divisor "M" | 1M1 | 1M0 | Prescaler P1 Divisor "M" |
|---|---|---|---|---|---|
| 0 | 0 | 1** | 0 | 0 | 1** |
| 0 | 1 | 2 | 0 | 1 | 2 |
| 1 | 0 | 4 | 1 | 0 | 4 |
| 1 | 1 | 8 | 1 | 1 | 8 |

**Default Condition

## EN0 (bit) (Default EN0 = 1)

1) If EN0 = 1 and PDN0 = 0 the CTRL0 pin functions as an Output Enable for OUT0, the frequency of the output being determined by the SEL0 bit.
2) If PDN0 = 1, the EN0 bit is ignored, CTRL0 will function as a power-down, and output OUT0 will always be enabled on power-up, its frequency being determined by the SEL0 bit.
3) If EN0 = 0 the function of CTRL0 is determined by the SEL0 and PDN0 bits (see Table 1).

## SEL0 (Default SEL0 = 1)

1) If SEL0 = 1 and EN0 = PDN0 = 0, the CTRL0 pin determines the state of the MUX (i.e., the output frequency of OUT0).
2) If CTRL0 = 0 the output will be the Master clock frequency.
3) If CTRL0 = 1 the output will be the output frequency of the M prescaler.
4) If either EN0 or PDN0 = 1 then SEL0 determines the frequency of OUT0 when it is enabled.
5) If SEL0 = 0 the output will be the Master clock frequency.
6) If SEL0 = 1 the output will be the output frequency of the M prescaler (see Table 1).

## PDN0 (Default PDN0 = 0)

1) This bit (if set to 1) causes CTRL0 to perform a power-down function, regardless of the setting of the other bits.
2) If PDN0 = 0 the function of CTRL0 is determined by the values of EN0 and SEL0.

### NOTE:

When EN0 = SEL0 = PDN0 = 0, CTRL0 also functions as a power-down. This is a special case where all the OUT0 circuitry is disabled even when the device is powered up for power to saving when OUT0 is not used (see Table 1).

## PDN1 (Default PDN1 = 0)

1) If PDN1 = 1, CTRL1 will function as a power-down.
2) If PDN1 = 0, CTRL1 functions as an output enable for OUT1 only (see Table 2.)

### NOTE (ON OUTPUT ENABLE AND POWER-DOWN):

1) Both enables are “smart” and wait for the output to be low before going to Hi-Z.
2) Power-down sequence first disables both outputs before powering down the device.
3) On power-up the outputs are disabled until the clock has stabilized (~8000 cycles).
4) In power-down mode, the device cannot be programmed.
5) A power-down command must persist for at least two cycles of the lowest output frequency plus 10µs.

## DIV WORD

| MSB | | | | | | | LSB | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N9 | N8 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 | X | X | X | X | X | X |
| first data byte | | | | | | | | second data byte | | | | | | | |

### N

These ten bits determine the value of the programmable divider (N). The range of divisor values is from 2 to 1025, and is equal to the programmed value of N plus 2 (see Table 5).

## PROGRAMMABLE DIVISOR N VALUES Table 5

| BIT VALUE | DIVISOR (N) |
|---|---|
| 0 000 000 000** | 2 |
| 0 000 000 001 | 3 |
| - | - |
| - | - |
| - | - |
| - | - |
| 1 111 111 111 | 1025 |

**Default Condition

## BUS WORD

| Name | - | - | - | - | WC | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|
| Factory Default | 0* | 0* | 0* | 0* | 0 | 0 | 0 | 0 |

*These bits are reserved and must be set to zero.

### A0, A1, A2 (Default Setting = 000)

These are the device select bits that determine the address of the device.

### WC (Default Setting WC = 0)

This bit determines when/if the EEPROM is written to after register contents have been changed.
If WC = 0 the EEPROM is written automatically after a write register command.
If WC = 1 the EEPROM is only written when the “WRITE ” command is issued.
Regardless of the value of the WC bit, when the BUS register (A0, A1, A2) is written, the current value in all registers (DIV, MUX, and BUS) are immediately written to the EEPROM.

## 2-WIRE SERIAL DATA BUS

The DS1077 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1077 operates as a slave on the 2-wire bus. Connections to the bus are made via the open-drain I/O lines, SDA and SCL. A pull-up resistor (5kΩ) is connected to SDA.

The following bus protocol has been defined (See Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

**Bus not busy:** Both data and clock lines remain HIGH.

**Start data transfer:** A change in the state of the data line from HIGH to LOW while the clock is HIGH defines a START condition.

**Stop data transfer:** A change in the state of the data line from LOW to HIGH while the clock line is HIGH defines the STOP condition.

**Data valid:** The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS1077 works in both modes.

**Acknowledge:** Each receiving device, when addressed, is obliged to generate an acknowledge after the byte has been received. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. When the DS1077 EEPROM is being written to, it will not be able to perform additional responses. In this case, the slave DS1077 will send a not-acknowledge to any data transfer request made by the master. It will resume normal operation when the EEPROM operation is complete.

A master must signal an end-of-data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

## **DATA TRANSFER ON 2-WIRE SERIAL BUS** Figure 2

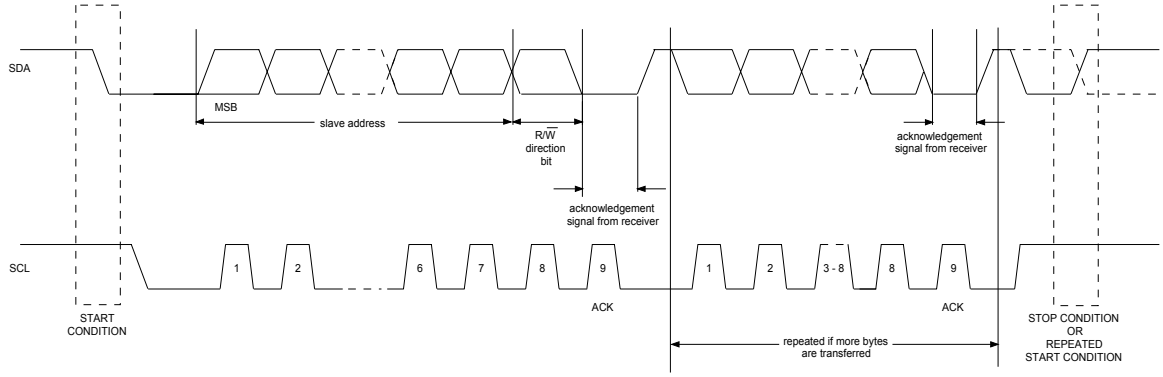



Figure 2 details how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next, follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

2) **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next, follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1077 may operate in the following two modes:

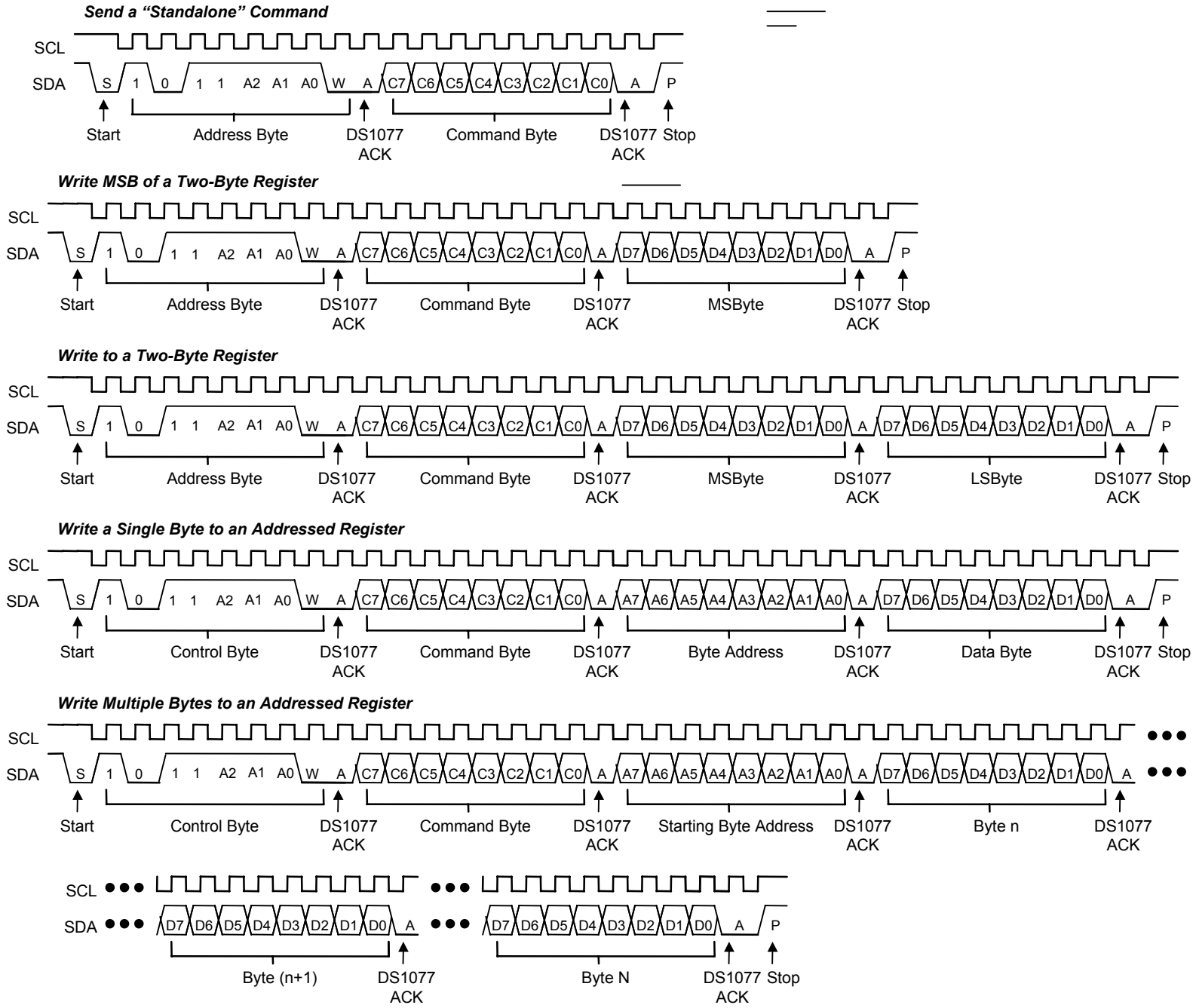
1) **Slave receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after the slave address and direction bit have been received.

2) **Slave transmitter mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1077 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

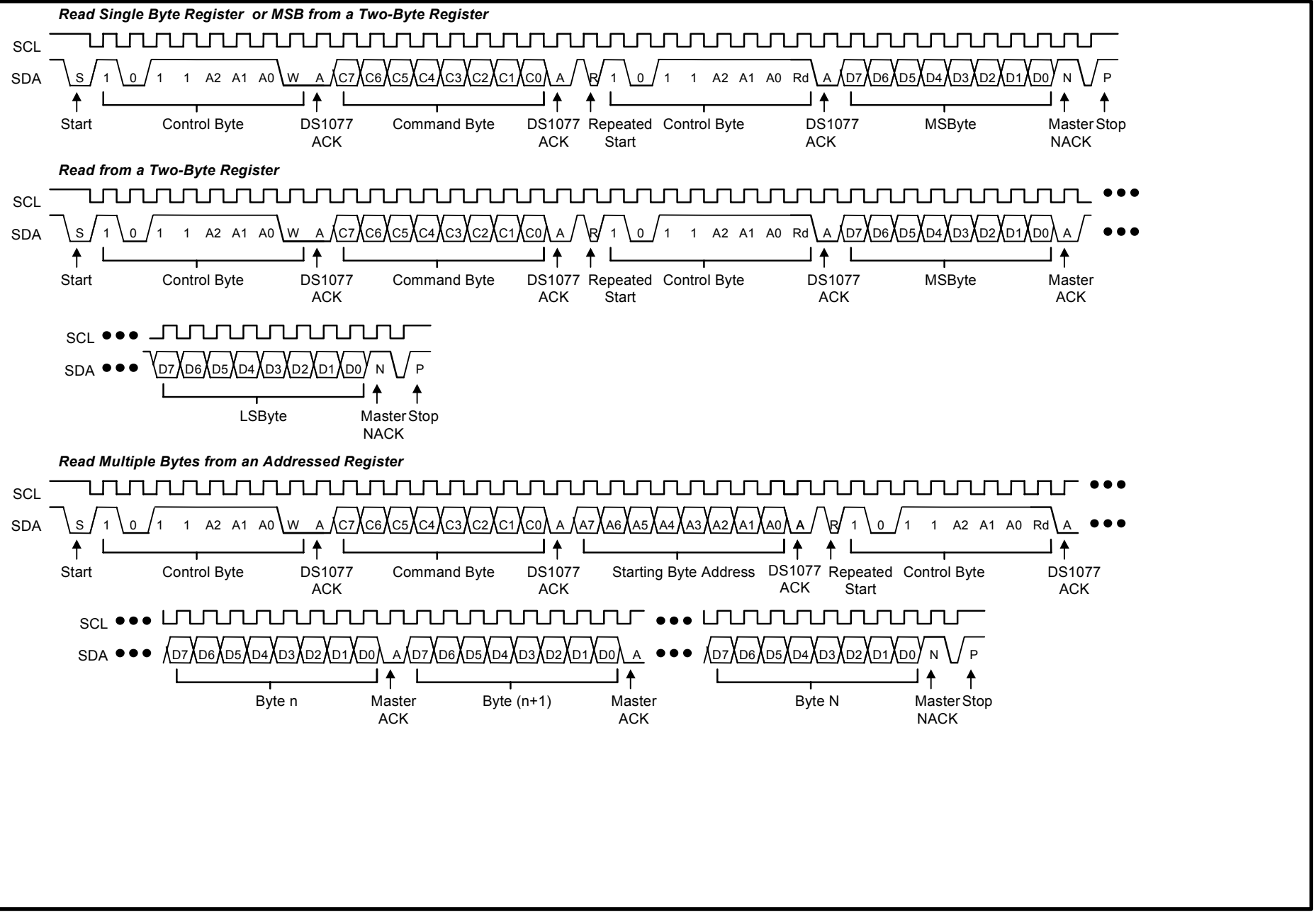
## SLAVE ADDRESS

A control byte is the first byte received following the START condition from the master device. The control byte consists of a 4-bit control code; for the DS1077, this is set as 1011 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0) and can be written to the EEPROM. They are used by the master device to select which of eight devices are to be accessed. The select bits are in effect the three least significant bits of the slave address. The last bit of the control byte ($R/\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero, a write operation is selected. Following the START condition, the DS1077 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving the 1011 code (changeable with one mask) and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line.

## 2-WIRE SERIAL COMMUNICATION WITH DS1077 Figure 3



## 2-WIRE SERIAL COMMUNICATION WITH DS1077 Figure 3 (continued)



## COMMAND SET

Data and control information is read from and written to the DS1077 in the format shown in Figure 3. To write to the DS1077, the master will issue the slave address of the DS1077 and the R/$\overline{W}$ bit will be set to 0. After receiving an acknowledge, the bus master provides a command protocol. After receiving this protocol, the DS1077 will issue an acknowledge, and then the master may send data to the DS1077. If the DS1077 is to be read, the master must send the command protocol as before, and then issue a repeat START condition and then the control byte again, this time with the R/W bit set to 1 to allow reading of the data from the DS1077. The command set for the DS1077 is as follows:

### Access DIV [01]

If R/$\overline{W}$ is 0, this command writes to the DIV register. After issuing this command, the next data byte value is to be written into the DIV register.

If R/$\overline{W}$ is 1, the next data byte read is the value stored in the DIV register.

### Access MUX [02]

If R/$\overline{W}$ is 0, this command writes to the MUX register. After issuing this command, the next data byte value is to be written into the MUX register.

If R/$\overline{W}$ is 1, the next data byte read is the value stored in the MUX register.

### Access BUS [0D]

If R/$\overline{W}$ is 0, this command writes to the BUS register. After issuing this command, the next data byte value is to be written into the BUS register.

If R/$\overline{W}$ is 1, the next data byte read is the value stored in the BUS register.

### Write E2 [3F]

If WC = 0 the EEPROM is automatically written to at the end of each command. This is a DEFAULT condition. In this case the command WRITE E2 is not needed.

If WC = 1, the EEPROM is written when the WRITE E2 command is issued. On receipt of the WRITE E2 command the contents of the BUS, DIV, and MUX registers are written into the EEPROM, thus locking in the register settings.

**EXCEPTION:** The BUS, DIV, and MUX registers are always automatically written to EEPROM after a write to the BUS register regardless of the value of the WC bit.

## APPLICATION INFORMATION

### Power-Supply Decoupling

To achieve best results, decouple the power supply with 0.01µF and 0.1µF high-quality, ceramic, surface-mount capacitors as close as possible to $V_{CC}$/GND of the device. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

### Current Consumption

The active supply current can be significantly reduced by disabling OUT0 when not required and setting its prescaler to divide by 8. Likewise, bypassing OUT1's divider (and using only the prescaler) also significantly reduces the supply current.

## ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Ground -0.5V to 6.0V
Operating Temperature Range -40°C to +85°C
Programming Temperature Range 0°C to +70°C
Storage Temperature Range -55°C to +125°C
Soldering Temperature See IPC/JEDEC J-STD-020A Specification

## DC ELECTRICAL CHARACTERISTICS ($T_A$ = -40°C to +85°C, $V_{CC}$ = 5V ±5%)

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | 4.75 | 5 | 5.25 | V | 1 |
| High-Level Output Voltage (OUT1,OUT0) | $V_{OH}$ | $I_{OH}$ = -4mA, $V_{CC}$ = min | 2.4 | | | V | |
| Low-Level Output Voltage (OUT1,OUT0) | $V_{OL}$ | $I_{OL}$ = 4mA | | | 0.4 | V | |
| High-Level Input Voltage (CTRL1, CTRL0) | $V_{IH}$ | | 2.1 | | $V_{CC}$+ 0.3V | V | |
| High-Level Input Voltage (SDA, SCL) | $V_{IH}$ | | 0.7Vcc | | $V_{CC}$+ 0.3V | V | |
| Low-Level Input Voltage (CTRL1, CTRL0) | $V_{IL}$ | | -0.3V | | 0.8 | V | |
| Low-Level Input Voltage (SDA, SCL) | $V_{IL}$ | | -0.3V | | 0.3Vcc | | |
| High-Level Input Current (CTRL1, CTRL0, SDA, SCL) | $I_{IH}$ | $V_{IH}$ = $V_{CC}$ = 5.25V | | | 1 | µA | |
| Low-Level Input Current (CTRL1, CTRL0, SDA, SCL) | $I_{IL}$ | $V_{CC}$ = 5.25V, $V_{IL}$ = 0 | -1 | | | µA | |
| Supply Current (Active) | $I_{CC}$ | $C_L$ = 15pF (Both Outputs) (-40°C to +85°C) | | | 50 | mA | 10 |
| Standby Current (Power-Down) | $I_{CCQ}$ | Power-Down Mode | | 2 | 5 | µA | |

## AC ELECTRICAL CHARACTERISTICS ($T_A$ = -40°C to +85°C; $V_{CC}$ = 5V ±5%)

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Output Frequency Tolerance Over Temperature | Δfo | $V_{CC}$ = 5V, 25°C | -0.5 | 0 | +0.5 | % | 11 |
| | | $V_{CC}$ = 5V, 70°C | -0.5 | 0 | +0.5 | | |
| | | $V_{CC}$ = 5V, -40°C to +25°C | -3.3 | | +2.7 | | |
| | | $V_{CC}$ = 5V, +25°C to +85°C | -1.4 | | +1.4 | | |
| Output Frequency Tolerance Over Voltage | Δfo | $V_{CC}$ = 4.75V, 25°C | -1.0 | -0.7 | | % | |
| | | $V_{CC}$ = 5.25V, 25°C | | +0.7 | +1.0 | | |
| Combined Freq. Variation | Δfo | Over Temp (0°C to +70°C) & Voltage | -1.65 | | +1.25 | % | |
| Output Frequency Min | $f_{OUT}$ | | 8.13 | | | kHz | 2 |
| Output Frequency Max | | | | | 133 | MHz | |
| Power-Up Time | $t_{POR}$ + $t_{STAB}$ | | | 0.1 | 1 | ms | 5 |
| Enable OUT1 from PDN | $t_{STAB}$ | | | 0.1 | 1 | ms | 3 |
| Enable OUT0 from PDN | $t_{STAB}$ | | | 0.1 | 1 | ms | 3 |
| OUT1 Hi-Z from PDN | $t_{HiZ}$ | | | | 1 | ms | 3 |
| OUT0 Hi-Z from PDN | $t_{HiZ}$ | | | | 1 | ms | 3 |
| Load Capacitance | $C_L$ | | | 15 | 50 | pF | 4 |
| Output Duty Cycle (OUT1, OUT0) | | | 40 | | 60 | % | |
| Output Jitter | | $f_{OUT}$=133MHz M=1; DIV1=1 $C_L$=12pF 3 sigma pk-to-pk | | 30 | | psec | |

## AC ELECTRICAL CHARACTERISTICS: 2-WIRE INTERFACE

(-40°C to +85°C; $V_{CC}$= 5V±5%)

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| SCL Clock Frequency | $f_{SCL}$ | Fast Mode | | | 400 | kHz | |
| | | Standard Mode | | | 100 | | |
| Bus Free Time Between a STOP and START Condition | $t_{BUF}$ | Fast Mode | 1.3 | | | µs | |
| | | Standard Mode | 4.7 | | | | |
| Hold Time (Repeated) START Condition | $t_{HD:STA}$ | Fast Mode | 0.6 | | | µs | 6 |
| | | Standard Mode | 4.0 | | | | |
| LOW Period of SCL | $t_{LOW}$ | Fast Mode | 1.3 | | | µs | |
| | | Standard Mode | 4.7 | | | | |
| HIGH Period of SCL | $t_{HIGH}$ | Fast Mode | 0.6 | | | µs | |
| | | Standard Mode | 4.0 | | | | |
| Set-Up Time for a Repeated START | $t_{SU:STA}$ | Fast Mode | 0.6 | | | µs | |
| | | Standard Mode | 4.7 | | | | |
| Data Hold Time | $t_{HD:DAT}$ | Fast Mode | 0 | | 0.9 | µs | 7,8 |
| | | Standard Mode | 0 | | | | |
| Data Set-Up Time | $t_{SU:DAT}$ | Fast Mode | 100 | | | ns | |
| | | Standard Mode | 250 | | | | |
| Rise Time of Both SDA and SCL Signals | $t_R$ | Fast Mode | $20 + 0.1C_B$ | | 300 | ns | 9 |
| | | Standard Mode | | | 1000 | | |
| Fall Time of Both SDA and SCL Signals | $t_F$ | Fast Mode | $20 + 0.1C_B$ | | 300 | ns | 9 |
| | | Standard Mode | | | | | |
| Set-Up Time For STOP | $t_{SU:STO}$ | Fast Mode | 0.6 | | | µs | |
| | | Standard Mode | 4.0 | | | | |
| Capacitive Load for Each Bus Line | $C_B$ | | | | 400 | pF | 9 |
| Input Capacitance | $C_I$ | | | 5 | | pF | |

## NONVOLATILE MEMORY CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Writes | | +85°C | 10,000 | | | | |

## NOTES:

1) All voltages are referenced to ground.
2) 8.13kHz is obtained from a -66MHz standard part.
3) PDN is a power-down signal applied to either CTRL0 or CTRL1 pins as appropriate.
4) Output voltage swings may be impaired at high frequencies combined with high output loading.
5) After this period, the first clock pulse is generated.
6) A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7) The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period ($t_{LOW}$) of the SCL signal.

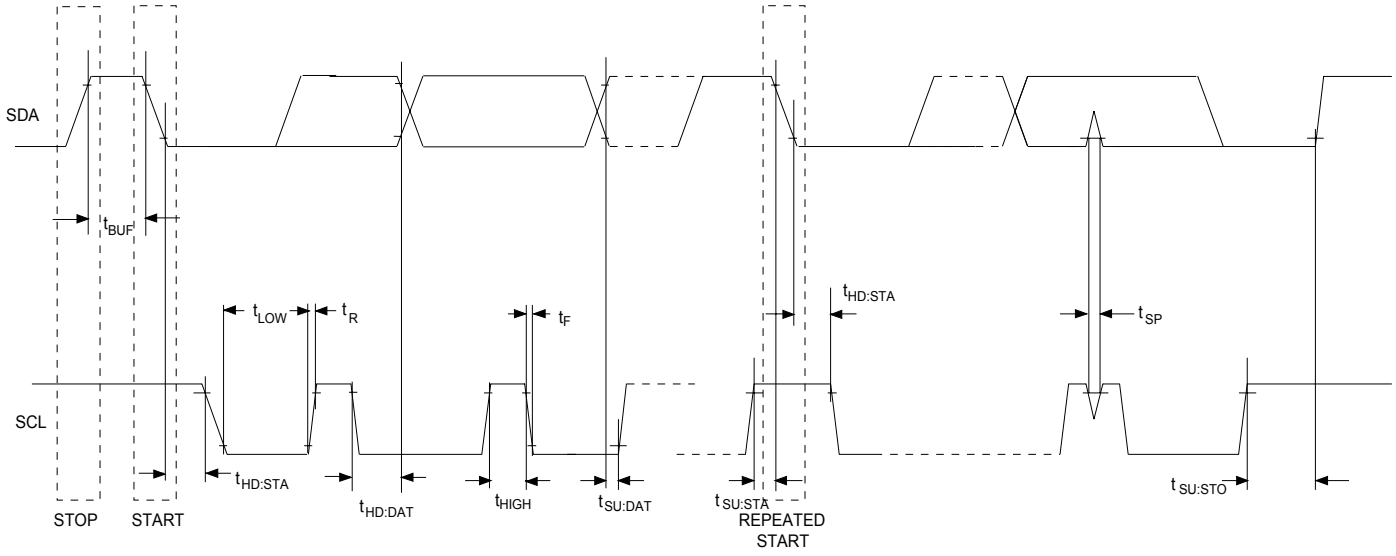
8) A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ MAX} + t_{SU:DAT} = 1000ns + 250ns = 1250ns$ before the SCL line is released.

9) $C_B$ is the total capacitance of one bus line in pF.

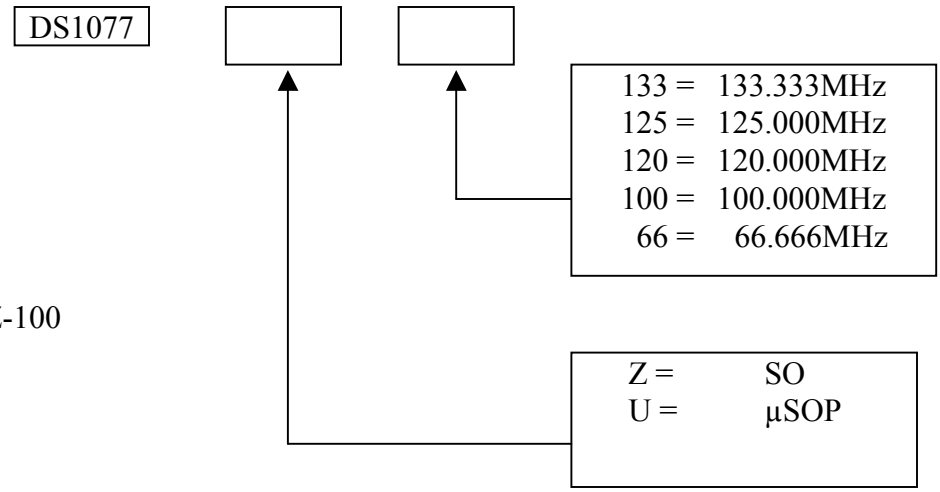
10) OUT0 and OUT1 are operating at oscillator master frequency without divider.

11) Typical frequency shift due to aging is ±0.5%. Aging stressing includes Level 3 preconditioning with 1000 temperature cycles of -55°C to +125°C, 336hr max $V_{CC}$ biased +125°C bake. Level 3 preconditioning consists of a 24hr +125°C storage bake, 192hr moisture soak at +30°C/60% R.H., and three solder reflow passes.

## TIMING DIAGRAM



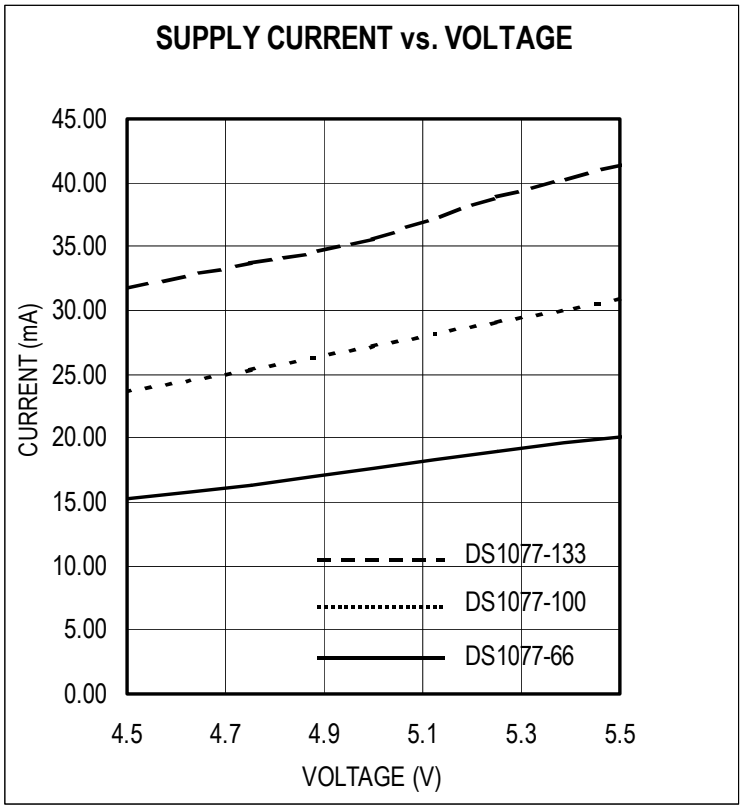

## ORDERING INFORMATION

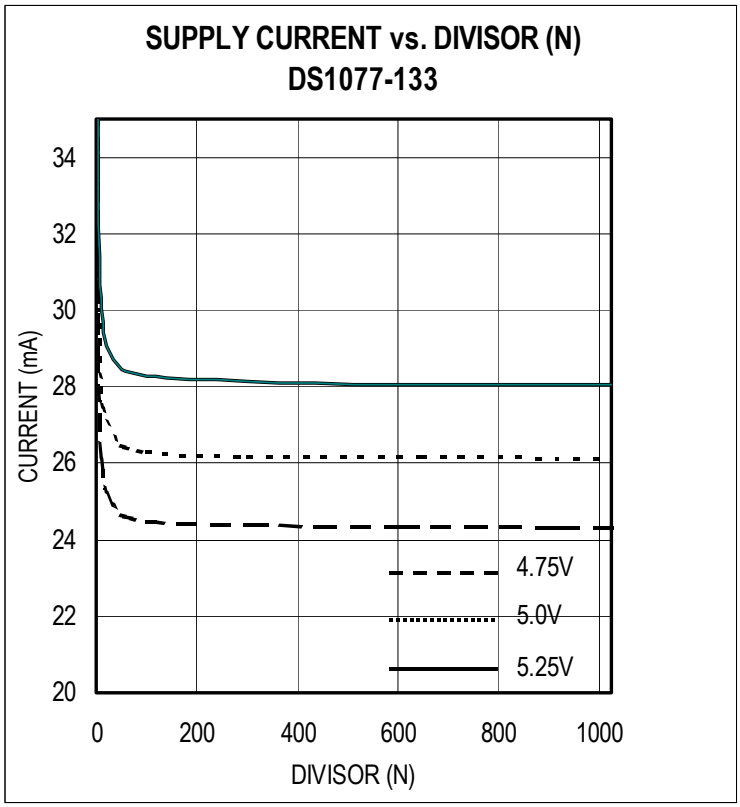



Example:
DS1077Z-100

## TYPICAL OPERATING CHARACTERISTICS

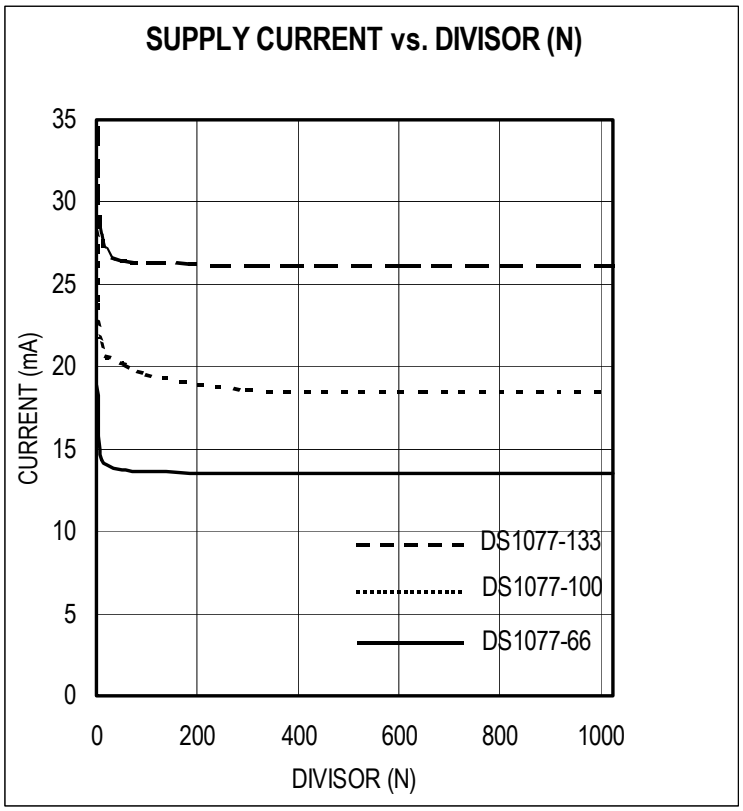
($V_{CC}$ = 5.0V, T = +25°C, unless otherwise specified)

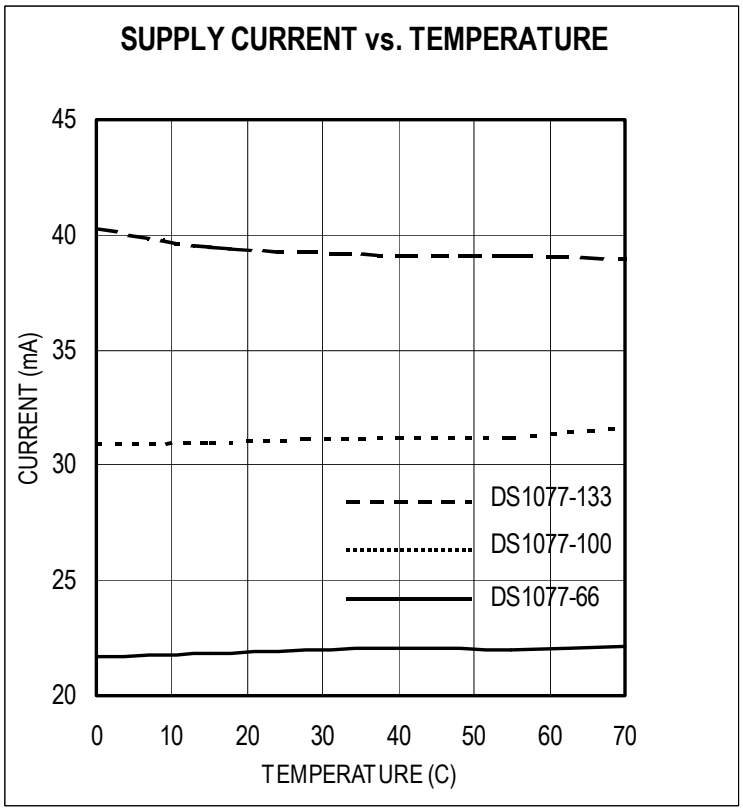


## TYPICAL OPERATING CHARACTERISTICS (continued)

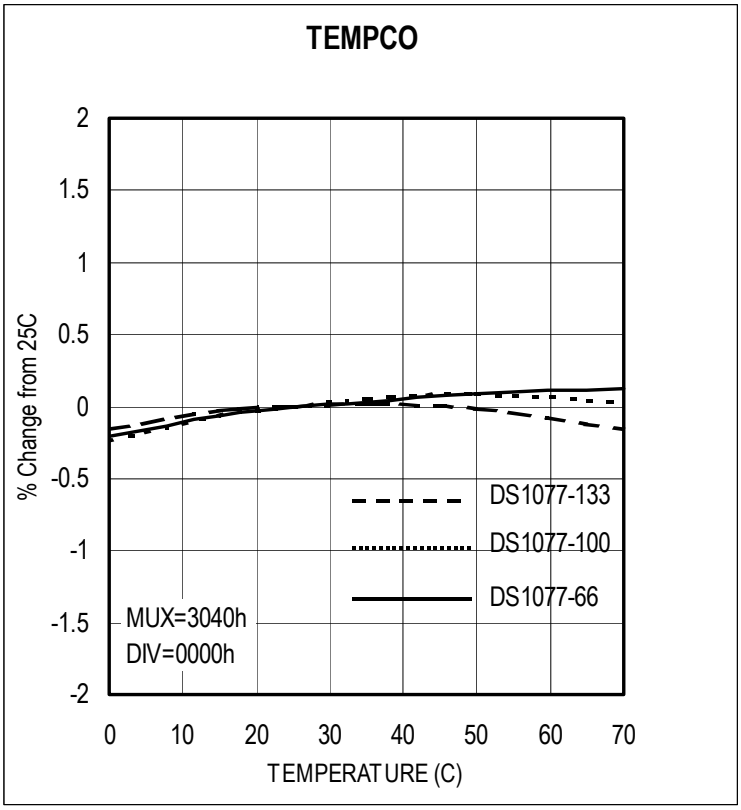
($V_{CC}$ = 5.0V, T = +25°C, unless otherwise specified)

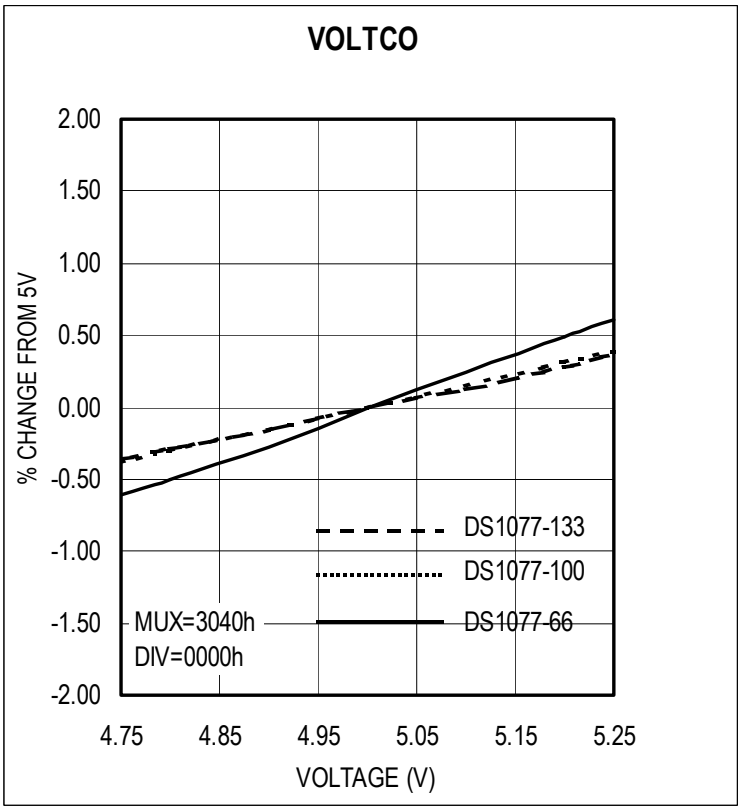


## TYPICAL OPERATING CHARACTERISTICS (continued)

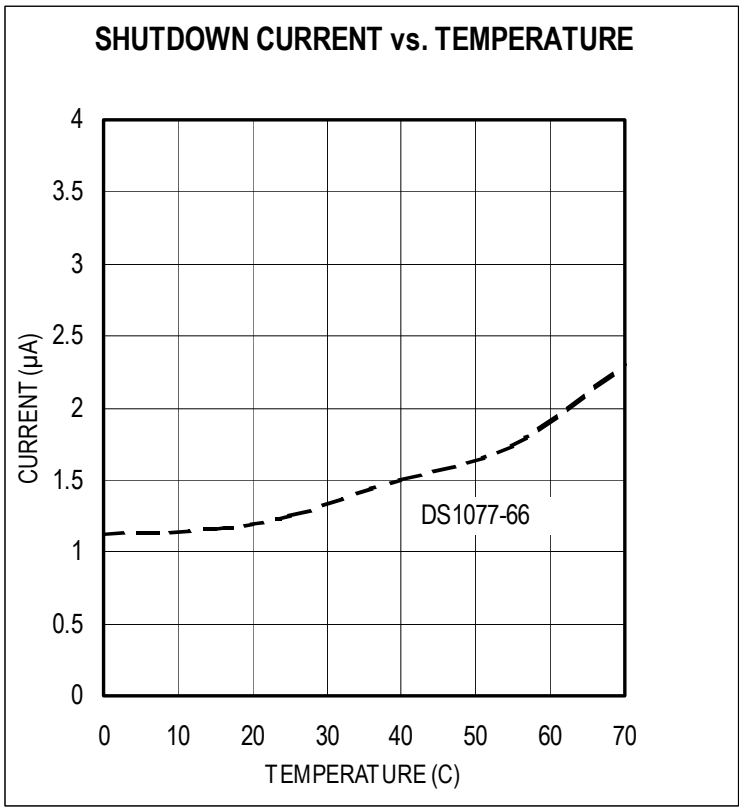
($V_{CC}$ = 5.0V, T = +25°C, unless otherwise specified)



## TYPICAL OPERATING CHARACTERISTICS (continued)

($V_{CC}$ = 5.0V, T = +25°C, unless otherwise specified)



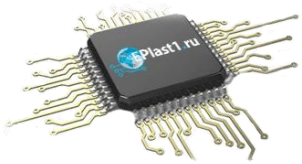
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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.




**Как с нами связаться**

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