

# 4.5V to 28V, 4A 1ch Synchronous Buck Converter Integrated FET

## BD95514MUV

### General Description

BD95514MUV is a switching regulator with current capability of 4A and the ability to achieve low output voltages of 0.7V to 5.0V from a wide input voltage range of 4.5V to 28V. Built-in NMOS power transistors and implementation of Simple Light Load Mode (SLLM™) technology make this device highly-efficient. SLLM™ improves efficiency when the device is used with light load, providing high efficiency over a wider range of loads. The device also uses a new technology called H<sup>3</sup>Reg™ proprietary control method to achieve ultra-fast transient response against load changes. BD95514MUV is especially designed for various applications and is integrated with protection features such as soft-start, variable frequency, short circuit protection with timer latch, over voltage protection, and power good function.

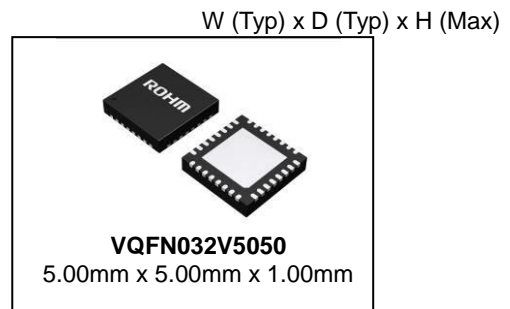
### Features

- Internal 5V Linear Voltage Regulator (100mA)
- Integrated H<sup>3</sup>Reg™ DC/DC Converter Controller
- Selectable Simple Light Load Mode (SLLM™), Quiet Light Load Mode (QLLM) and Forced Continuous Mode
- Built-in Thermal Shutdown, Low Input, Current Overload, Output Over/Under-Voltage Protection Circuitry
- Soft Start Function to Minimize Rush Current during Startup
- Adjustable Switching Frequency (f = 200kHz to 1000kHz:It changes depending on the setup condition.)
- Built-in Output Discharge Function
- Tracking Function
- Internal Bootstrap Diode

### Key Specifications

- Input Voltage Range: 4.5V to 28V
- Output Voltage Range: 0.7V to 5.0V
- Output Current: 4.0A(Max)
- High Side ON-Resistance: 120mΩ(Typ)
- Low Side ON-Resistance: 120mΩ(Typ)
- Standby Current: 0μA (Typ)
- Operating Temperature Range: -10°C to +100°C

### Package



### Application

Mobile PCs, desktop PCs, LCD-TV, Digital Household Electronics

### Typical Application Circuit

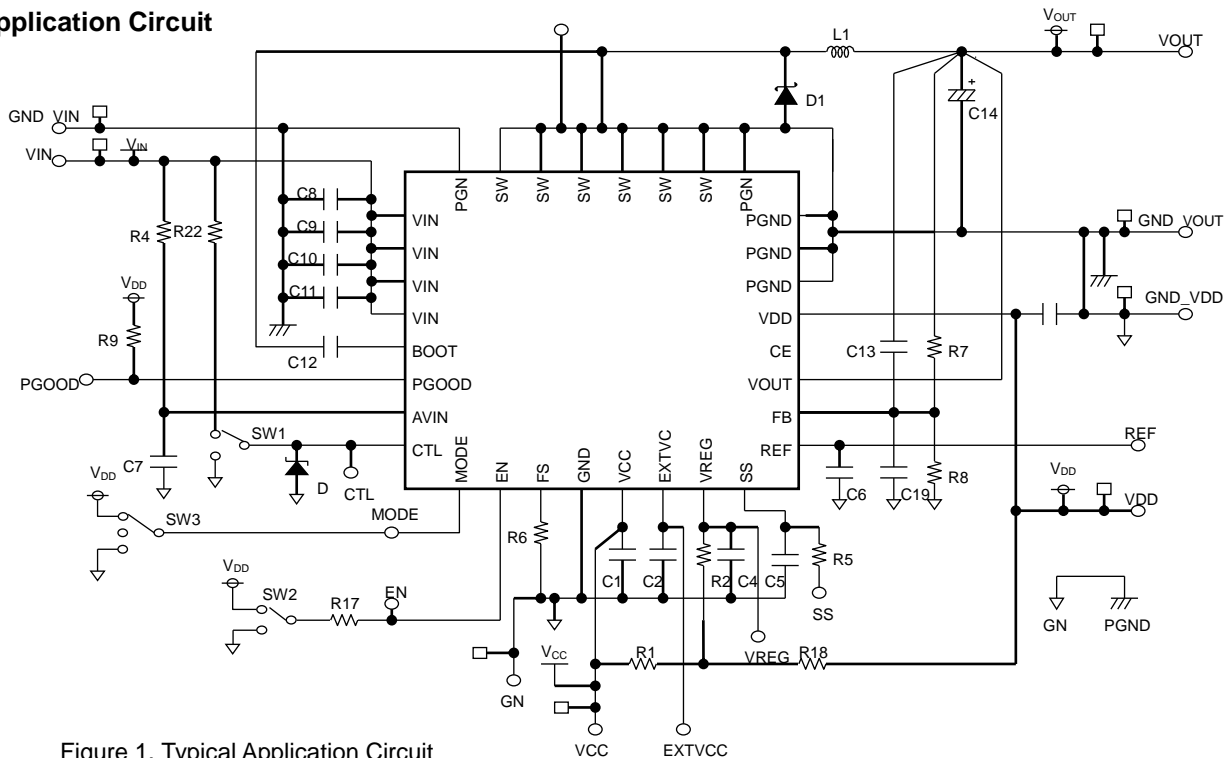
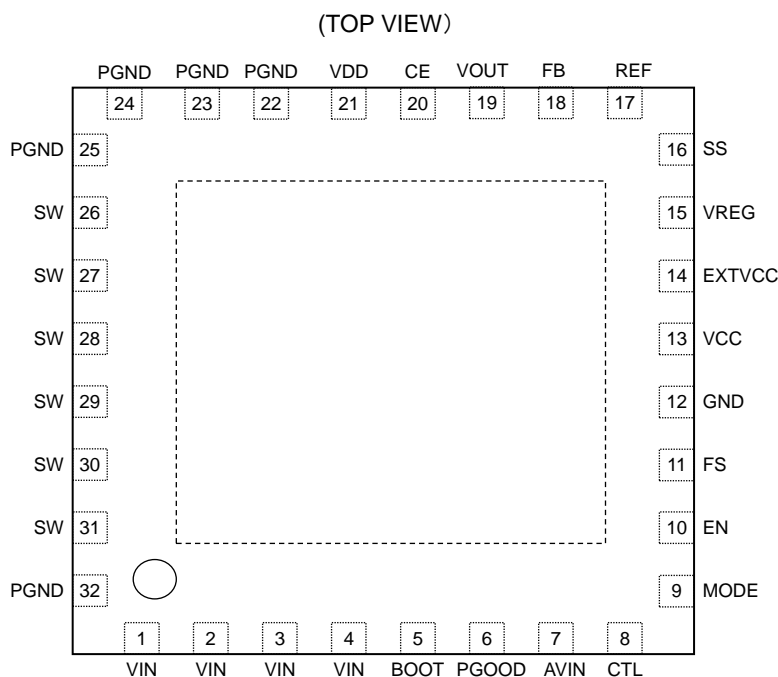


Figure 1. Typical Application Circuit

## Pin Configuration



Note: Connect the underside (FIN) to the ground terminal

Figure 2. Pin Configuration

## Pin Description

(Function Table)

Pin No.	Pin Name	Pin Function
1 to 4	VIN	Battery voltage input (4.5V to 28 V)
5	BOOT	HG driver power supply
6	PGOOD	Power good output (high when output $\pm 10\%$ of regulation)
7	AVIN	Battery voltage sense
8	CTL	Linear regulator ON/OFF (high = 5.0V, low = OFF)
9	MODE	Control mode selection GND : Continuous Mode 3.0V : QLLM VCC : SLLM™
10	EN	Enable output (high when VOUT ON)
11	FS	Switching frequency adjustment ( $R_{FS} = 30k\Omega$ to $300k\Omega$ )
12	GND	Sense ground
13	VCC	Power supply input
14	EXTVCC	External power supply input
15	VREG	IC reference voltage (5.0V / 100mA)
16	SS	Soft start condenser input
17	REF	Output reference voltage (0.7V)
18	FB	Feedback input (0.7V)
19	VOUT	Voltage discharge output
20	CE	Reversing HG output
21	VDD	Power supply input (5V)
22 to 25	PGND	Power ground
26 to 31	SW	Output to inductor
32	PGND	Power ground
Underside	FIN	Substrate connection

## Block Diagram

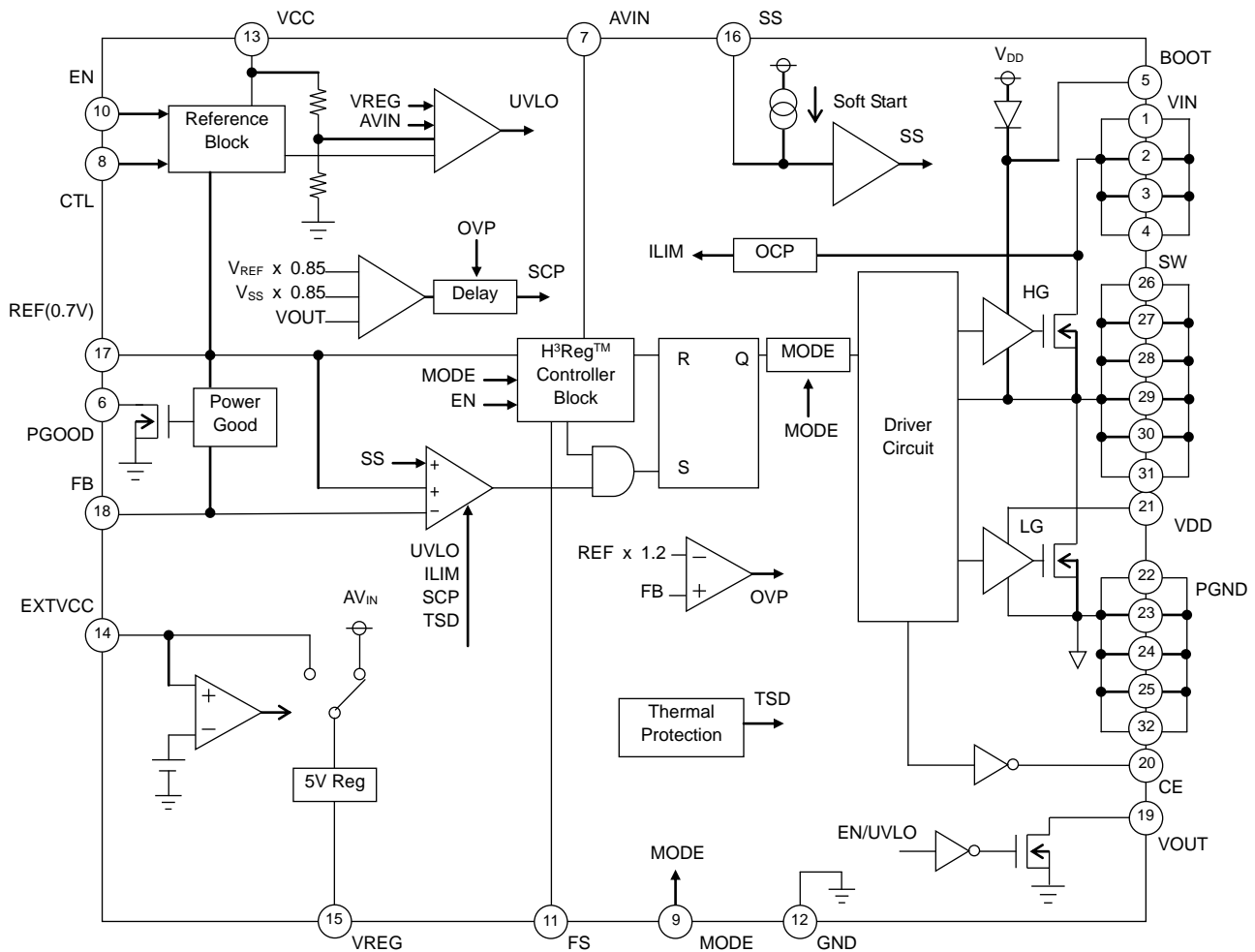


Figure 3. Block Diagram

## Description of Blocks

- VCC (Pin 13)**  
 This is the power supply pin for the IC's internal circuits, except for the FET driver. The input supply voltage ranges from 4.5V to 5.5 V. This pin should be bypassed with either a power capacitor or RC filter.
- EN (Pin 10)**  
 Enables or disables the switching regulator. When the voltage on this pin reaches 2.3V or higher, the internal switching regulator is turned ON. At voltages less than 0.8V, the regulator is turned OFF.
- VDD (Pin 21)**  
 This pin supplies power to the low side of the FET driver, as well as to the bootstrap diode. As the diode draws its peak current when switching on or off, this pin should be bypassed with a capacitance of approximately 1  $\mu$ F.
- VREG (Pin 15)**  
 Output pin of the 5V linear regulator. This pin also supplies power to the internal driver and control circuitry. VREG standby function is controlled by the CTL pin. The output supplies 5V at 100mA and should be bypassed to ground using a 10  $\mu$ F capacitor with a rating of X5R or X7R.
- EXTVCC (Pin 14)**  
 External power supply input for the linear regulator. When the voltage on the EXTVCC pin exceeds 4.4V, the regulator uses it in conjunction with other power sources to supply VREG. Connect the EXTVCC pin to GND when not in use.
- REF (Pin 14)**  
 Reference voltage output pin. The reference voltage is set internally by the IC to 0.7V, and the IC works to keep  $V_{REF}$  approximately equal to  $V_{FB}$ . Variations in voltage level on this pin affect the output voltage, so the pin should be bypassed with a 100pF to 0.1 $\mu$ F ceramic capacitor.

**Description of Blocks – continued**

7. SS (Pin 16)  
Soft start pin. When EN is set to high, the capacitor between the internal current source (typ:2.2μA) and SS-GND controls the startup time of the IC. When the voltage on the SS pin is lower than the REF output voltage (0.7V), the output voltage is held at the same voltage as the SS pin.
8. AVIN (Pin 7)  
The BD95514MUV controls the duty cycle and output voltage based on the input voltage at this pin, so voltage variations or oscillations on this line can cause unstable operation. This pin also acts as the voltage input for the switching block, so insufficient coupling impedance can also cause unstable operation. Therefore, this line should be bypassed with either a power capacitor or RC filter.
9. FS (Pin 11)  
Frequency-adjusting resistance input pin. Attaching a resistance of 30kΩ to 300kΩ adjusts the switching frequency from 200 kHz to 1MHz (p.11).
10. BOOT (Pin 5)  
This pin serves as the power source for the high side of the FET driver. A bootstrap diode is integrated within the IC. The maximum voltage on this pin should not exceed +30V with reference to GND or +7V with reference to SW. When operating the switching regulator, the operation of the bootstrap circuitry causes the BOOT voltage to swing from ( $V_{IN} + V_{DD}$ ) to  $V_{DD}$ .
11. PGOOD (Pin 6)  
Power good indicator. This open-drain output should be connected to a power supply via a 100kΩ pull-up resistor.
12. MODE (Pin 9)  
Mode selection pin. When low, the IC functions in forced-continuous mode; at voltages  $0V < V_{MODE} < 3V$ , QLLM mode; when high, SLLM™ mode.
13. CTL (Pin 8)  
Linear regulator control pin. When voltage is 2.3V or higher, a logic HIGH is recognized and the internal regulator ( $V_{REG} = 5V$ ) is switched ON. At voltages of 0.8V or lower, a logic LOW is recognized and the regulator is switched off. However, even if EN is logic HIGH, the switching regulator will not operate if CTL is logic LOW.
14. FB (Pin 18)  
Output voltage feedback input.  $V_{FB}$  is held at 0.7V by the IC.
15. SW (Pin 26 to Pin 31)  
Output from the switching regulator to the inductor. This output swings from  $V_{IN}$  to GND. The trace from the output to the inductor should be as short and wide as possible.
16. VOUT (Pin 19)  
Voltage output discharge pin. When EN is OFF, this output is pulled to low.
17. VIN (Pin 1 to Pin 4)  
Power supply input. The IC can accept any input from 4.5V to 28V. This pin should be bypassed directly to ground by a power capacitor.
18. PGND (Pin 22 to Pin 25, Pin 32)  
Power ground terminal.
19. CE  
Switching waveform inversion output terminal. Switches from GND to VCC. Use it at open in general.

## Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Input Voltage 1	V <sub>CC</sub>	7 (Note 1)	V
Input Voltage 2	V <sub>DD</sub>	7 (Note 1)	V
Input Voltage 3	AV <sub>IN</sub>	30 (Note 1)	V
Input Voltage 4	V <sub>IN</sub>	30 (Note 1)	V
External VCC Voltage	EXTV <sub>CC</sub>	7 (Note 1)	V
BOOT Voltage	V <sub>BOOT</sub>	35	V
BOOT-SW Voltage	V <sub>BOOT-SW</sub>	7 (Note 1)	V
Output Feedback Voltage	V <sub>FB</sub>	V <sub>CC</sub>	V
SS/FS/MODE Voltage	V <sub>SS</sub> /V <sub>FS</sub> /V <sub>MODE</sub>	V <sub>CC</sub>	V
VREG Voltage	V <sub>REG</sub>	V <sub>CC</sub>	V
EN/CTL Input Voltage	V <sub>EN</sub> /V <sub>CTL</sub>	7 (Note 1)	V
PGOOD Voltage	V <sub>PGOOD</sub>	7 (Note 1)	V
Output Current (Average)	I <sub>SW</sub>	4 (Note 1)	A
Power Dissipation 1	Pd1	0.38 (Note 2)	W
Power Dissipation 2	Pd2	0.88 (Note 3 and Note 6)	W
Power Dissipation 3	Pd3	2.06 (Note 4 and Note 6)	W
Power Dissipation 4	Pd4	4.56 (Note 5 and Note 6)	W
Operating Temperature Range	Topr	-10 to +100	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	+150	°C

(Note 1) Should not exceed Pd.

(Note 2) Ta ≥ 25°C (IC only), power dissipated at 3.0mW /°C.

(Note 3) Ta ≥ 25°C (single-layer board, 20.2 mm<sup>2</sup> copper heat dissipation pad), power dissipated at 7.0mW /°C.

(Note 4) Ta ≥ 25°C (4-layer board, 10.29 mm<sup>2</sup> copper heat dissipation pad on top layer, 5505 mm<sup>2</sup> pad on 2<sup>nd</sup> and 3<sup>rd</sup> layer), power dissipated at 16.5W /°C.

(Note 5) Ta ≥ 25°C (4-layer board, all layers with 5505 mm<sup>2</sup> copper heat dissipation pads), power dissipated at 36.5W /°C.

(Note 6) Values observed with chip backside soldered. When unsoldered, power dissipation is lower.

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

## Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Rating		Unit
		Min	Max	
Input Voltage 1	V <sub>CC</sub>	4.5	5.5	V
Input Voltage 2	V <sub>DD</sub>	4.5	5.5	V
Input Voltage 3	AV <sub>IN</sub>	4.5	28	V
Input Voltage 4	V <sub>IN</sub>	4.5	28	V
External VCC Voltage	EXTV <sub>CC</sub>	4.5	5.5	V
BOOT Voltage	V <sub>BOOT</sub>	4.5	33	V
SW Voltage	V <sub>SW</sub>	-0.7	+28	V
BOOT-SW Voltage	V <sub>BOOT-SW</sub>	4.5	5.5	V
MODE Input Voltage	V <sub>MODE</sub>	0	5.5	V
EN/CTL Input Voltage	V <sub>EN</sub> /V <sub>CTL</sub>	0	5.5	V
PGOOD Voltage	V <sub>PGOOD</sub>	0	5.5	V
Minimum On Time	tonMIN	-	100	nsec

## Electrical Characteristics

(Unless otherwise noted, Ta=25°C, AVIN=12V, VCC=VDD=VREG, VEN/VCTL=5V, VMODE=0V, RFS=180kΩ)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Whole Device Block]						
AVIN Bias Current 1	IIN1	-	1300	2000	μA	
AVIN Bias Current 2	IIN2	-	200	300	μA	EXTVCC=5V
AVIN Standby Current	IINSTB	-	0	10	μA	VCTL=VEN=0V
EN Low Voltage	VENLOW	GND	-	0.8	V	
EN High Voltage	VENHIGH	2.3	-	5.5	V	
EN Bias Current	IEN	-	12	20	μA	
CTL Low Voltage	VCTLOW	GND	-	0.8	V	
CTL High Voltage	VCTHIGH	2.3	-	5.5	V	
CTL Bias Current	ICTL	-	1	6	μA	
[5V Linear Regulator Block ]						
VREG Output Voltage	VREG	4.90	5.00	5.10	V	AVIN= 6.0V to 25V IREG= 0mA to 100mA
Maximum Current	IREG	200	-	-	mA	
[5V Switch Block ]						
EXTVCC Input Threshold Voltage	EVCC_UVLO	4.2	4.4	4.6	V	EXTVCC: Sweep up
Switch Resistance	REVCC	-	1.0	2.0	Ω	
[Under Voltage Locked Out Block ]						
AVIN Threshold Voltage	AVIN_UVLO	4.1	4.3	4.5	V	VCC: Sweep up
AVIN Hysteresis Voltage	dAVIN_UVLO	100	160	220	mV	VCC: Sweep down
VREG Threshold Voltage	VREG_UVLO	4.1	4.3	4.5	V	VREG: Sweep up
VREG Hysteresis Voltage	dVREG_UVLO	100	160	220	mV	VREG: Sweep down
[H <sup>3</sup> Reg™ Block]						
ON Time	ton	400	500	600	nsec	
MAX ON Time	tonMAX	5.0	11.0	22.0	μsec	
MIN OFF Time	toffMIN	-	450	550	nsec	

## Electrical Characteristics - continued

(Unless otherwise noted, Ta=25°C, AVIN=12V, VCC=VDD=VREG, VEN/VCTL=5V, VMODE=0V, RFS=180kΩ)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[FET Driver Block]						
High Side ON-Resistance	R <sub>ON_HIGH</sub>	-	120	200	mΩ	
Low Side ON-Resistance	R <sub>ON_LOW</sub>	-	120	200	mΩ	
[SCP Block]						
SCP Startup Voltage	V <sub>SCP</sub>	0.420	0.490	0.560	V	V <sub>FB</sub> :30%down
Delay Time	t <sub>SCP</sub>	0.5	1	2	ms	
[OVP Block]						
OVP Setting Voltage	V <sub>OVP</sub>	0.800	0.840	0.880	V	V <sub>FB</sub> :20%up
Delay Time	t <sub>OVP</sub>	0.5	1	2	ms	
[Soft Start Block]						
Charge Current	I <sub>SS</sub>	1.4	2.2	3.0	μA	
Standby Voltage	V <sub>SS_STB</sub>	-	-	100	mV	
[Current Limit Block]						
High Side FET Output Current Limit	I <sub>HOC</sub>	4.5	6.0	7.5	A	High peak detect
Low Side FET Output Current Limit	I <sub>LOC</sub>	3.0	4.0	5.0	A	Low peak detect
[Output Voltage Sense Block]						
Feedback Pin Voltage 1	V <sub>FB1</sub>	0.693	0.700	0.707	V	
Feedback Pin Voltage 2	V <sub>FB2</sub>	0.690	0.700	0.710	V	Ta=-10°C to +100°C I <sub>OUT</sub> =0A to 4A
Feedback Pin Bias Current	I <sub>FB</sub>	-100	0	+100	nA	
[Mode Block]						
SLLM™	V <sub>THSLLM</sub>	V <sub>CC</sub> -0.5	-	V <sub>CC</sub>	V	SLLM™ (Maximum LG OFF time:∞)
Forced Continuous Mode	V <sub>THCONT</sub>	GND	-	0.5	V	Continuous mode
QLLM	V <sub>THQLLM</sub>	2.5	3.0	3.5	V	QLLM (Maximum LG OFF time: 40μsec)
Open Voltage	V <sub>MODE</sub>	1.5	-	3.0	V	
[Power Good Block]						
VFB Power Good Low Voltage	V <sub>FB_PL</sub>	0.605	0.630	0.655	V	V <sub>FB</sub> : 10%down
VFB Power Good High Voltage	V <sub>FB_PH</sub>	0.745	0.770	0.795	V	V <sub>FB</sub> : 10%up

Typical Performance Curves

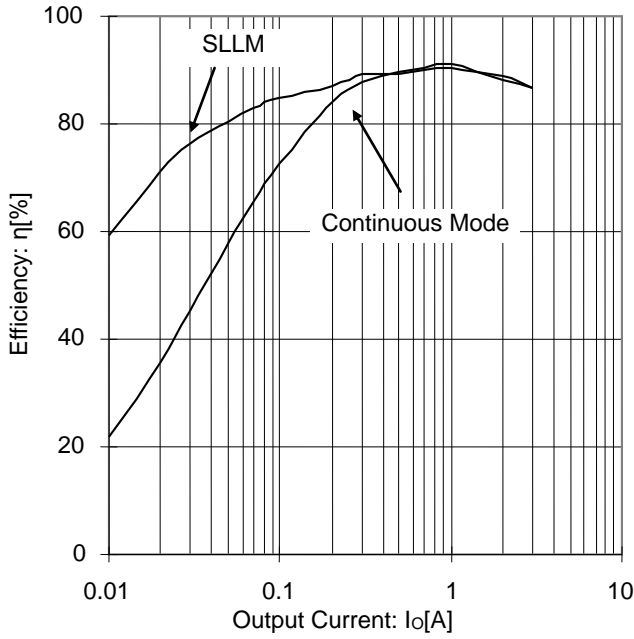


Figure 4. Efficiency vs Output Current ( $V_{IN}=7V, V_{OUT}=2.5V$ )

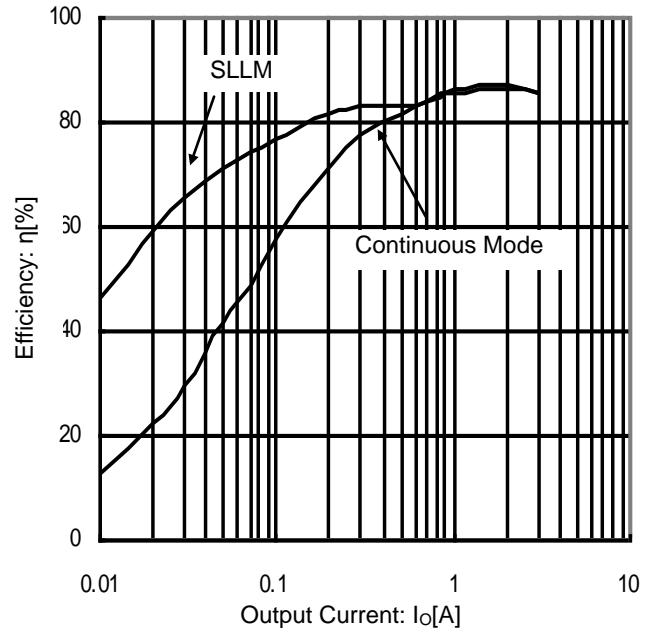


Figure 5. Efficiency vs Output Current ( $V_{IN}=12V, V_{OUT}=2.5V$ )

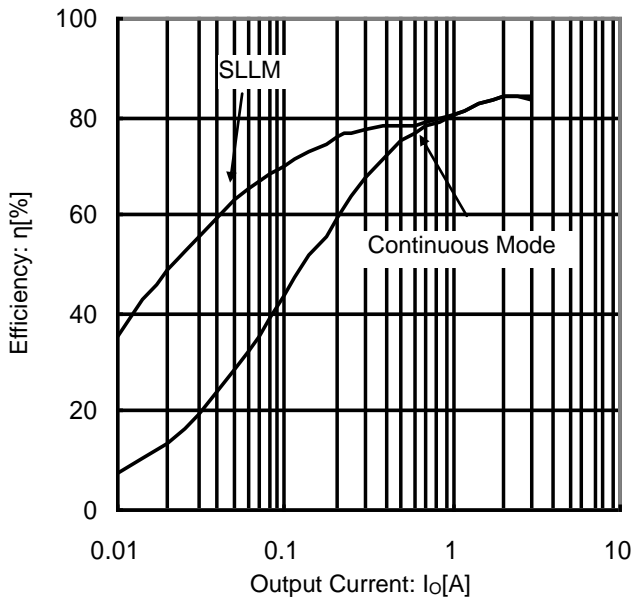


Figure 6. Efficiency vs Output Current ( $V_{IN}=19V, V_{OUT}=2.5V$ )

Typical Waveforms

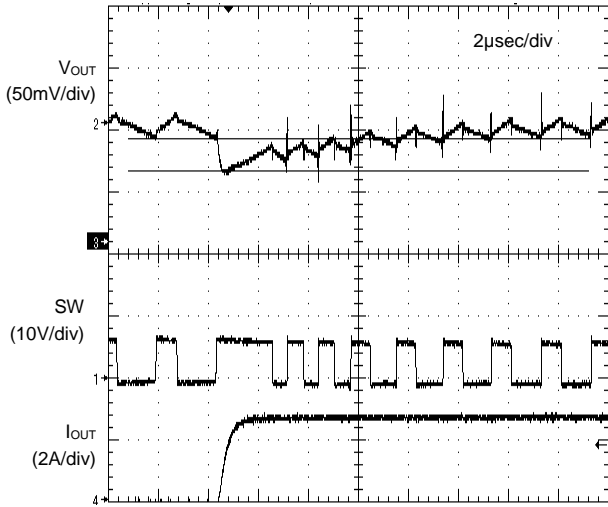


Figure 7. Transient Response  
(VIN=7V, VOUT=2.5V)

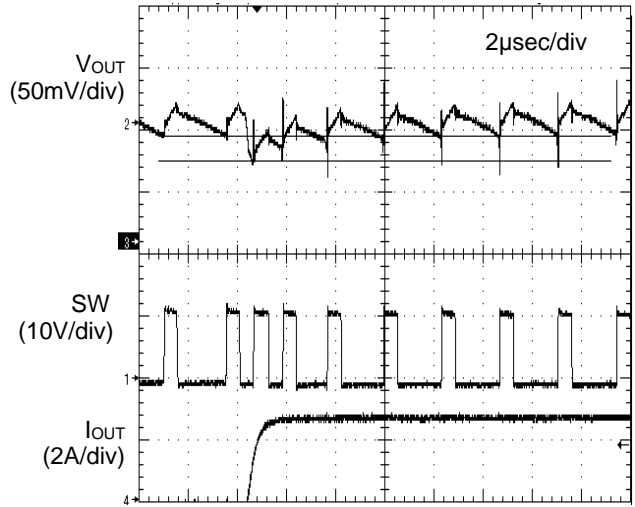


Figure 8. Transient Response  
(VIN=12V, VOUT=2.5V)

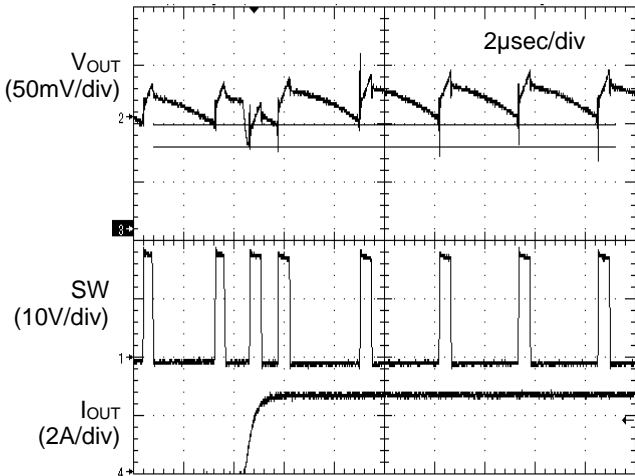


Figure 9. Transient Response  
(VIN=19V, VOUT=2.5V)

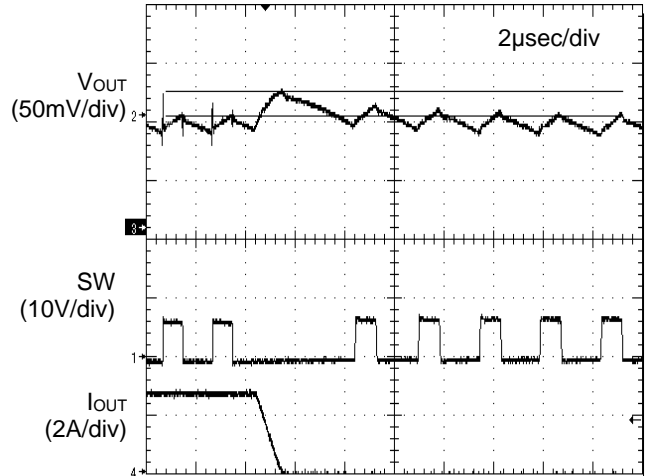


Figure 10. Transient Response  
(VIN=7V, VOUT=2.5V)

Typical Waveforms - continued

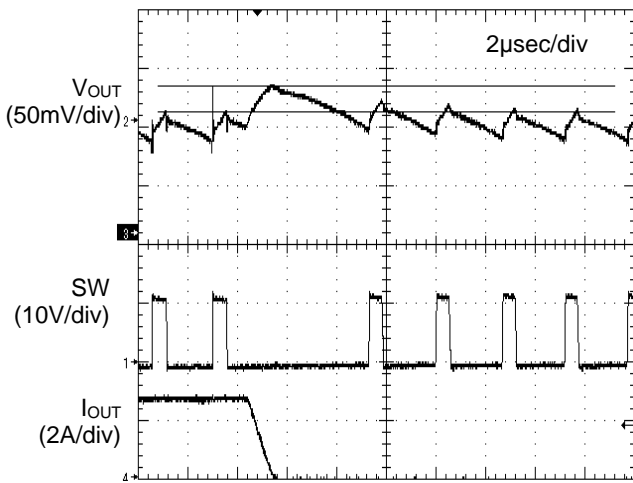


Figure 11. Transient Response  
( $V_{IN}=12V$ ,  $V_{OUT}=2.5V$ )

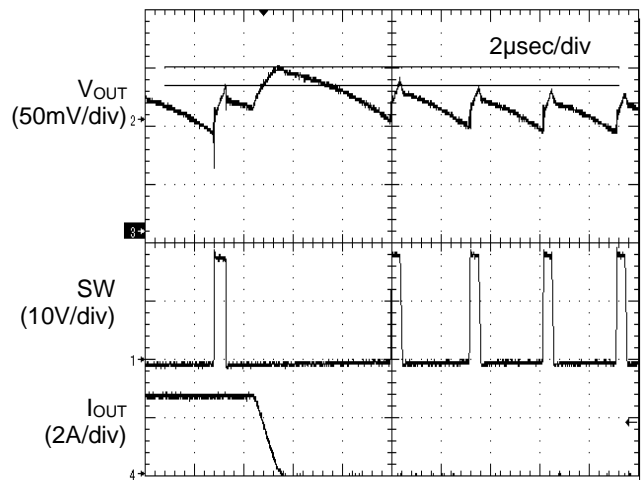


Figure 12. Transient Response  
( $V_{IN}=19V$ ,  $V_{OUT}=2.5V$ )

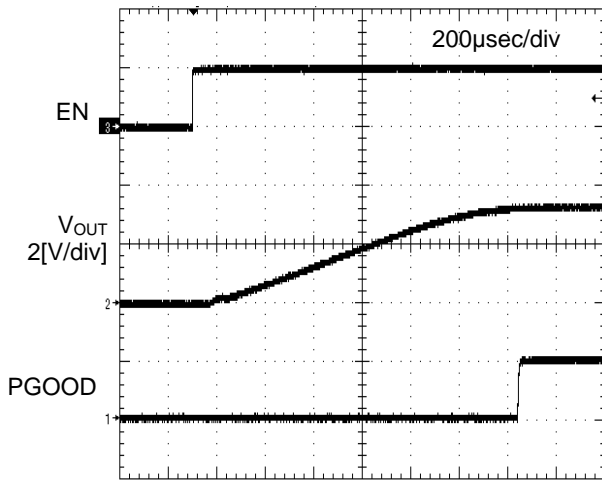


Figure 13. PGOOD Rising Waveform

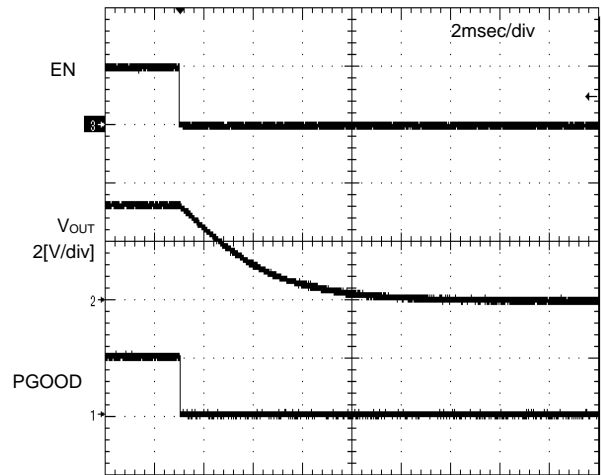


Figure 14. PGOOD Falling Waveform

Typical Waveforms - continued

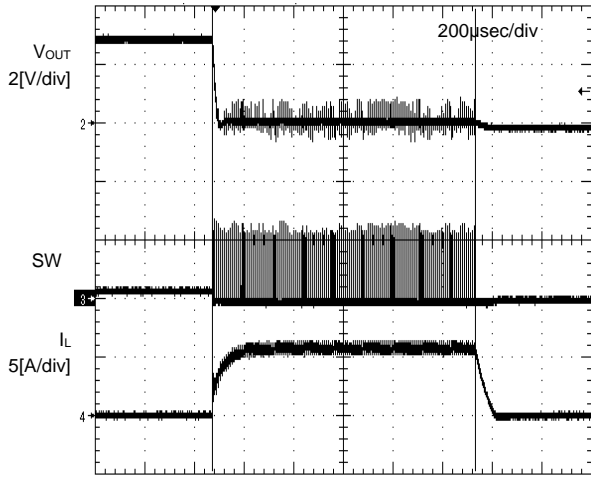


Figure 15. SCP Timer Latch Waveform

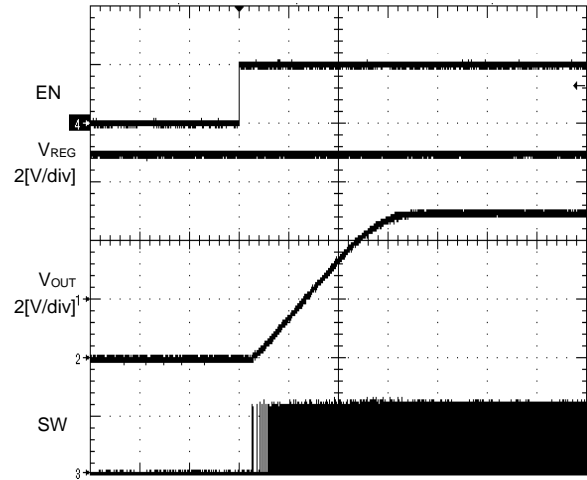


Figure 16. EN Wake Up

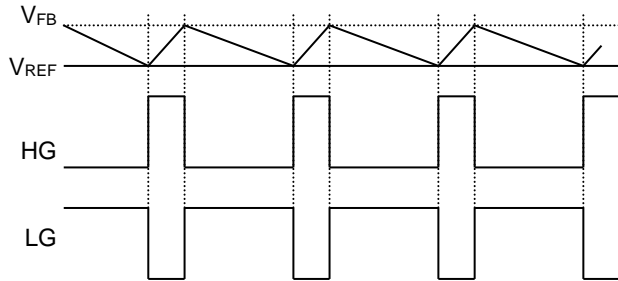
Application Information

1. Explanation of Operation

The BD95514MUV is a switching regulator that incorporates ROHM's proprietary H<sup>3</sup>Reg™ CONTROLLA control system. When V<sub>OUT</sub> drops suddenly due to changes in load, the system quickly restores the output voltage by extending the t<sub>ON</sub> time interval. This improves the regulator's transient response. When light-load mode is activated, the IC employs the Simple Light Load Mode (SLLM™) controller, further improving system efficiency.

(Note) HG stand for High side FET, and LG stand for Low side FET. It is a waveform to explain operation which can not be monitored.

H<sup>3</sup>Reg™ Control  
(Normal Operation)

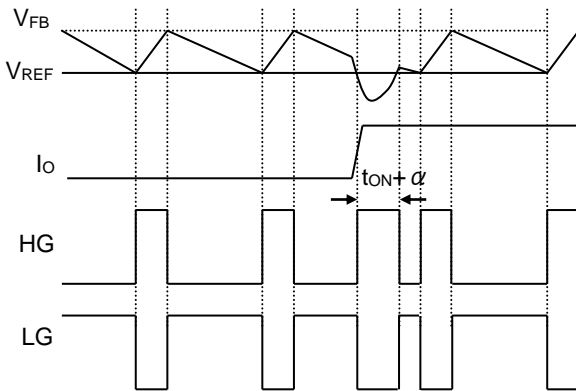


When V<sub>FB</sub> falls below the reference voltage (0.7V), the H<sup>3</sup>Reg™ CONTROLLA is activated;

$$t_{ON} = \frac{V_{REF}}{V_{IN}} \times \frac{1}{f} \quad [\text{sec}] \quad \dots (1)$$

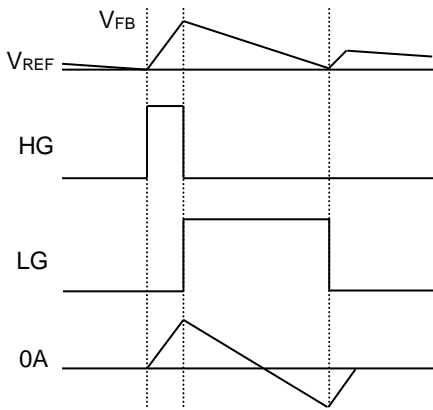
High gate output is determined by the above formula.

(Rapid Changes in Load)



When V<sub>OUT</sub> drops due to a sudden change in load and V<sub>FB</sub> remains below V<sub>REF</sub> after the preprogrammed t<sub>ON</sub> time interval has elapsed, the system quickly restores V<sub>OUT</sub> by extending the t<sub>ON</sub> time, thereby improving transient response.

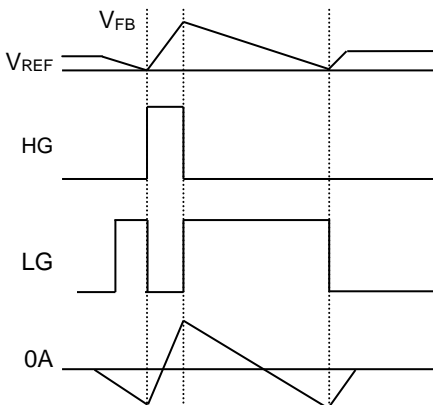
Light Load Control  
(SLLM Mode)



SLLM mode is enabled by setting the MODE pin to logic high. When the low gate is off and the current through the inductor is 0 (current flowing from V<sub>OUT</sub> to SW), the SLLM function is activated, disabling high gate output.

If V<sub>FB</sub> falls below V<sub>REF</sub> again, the high gate is switched back on, lowering the switching frequency of the regulator and yielding higher efficiency when powering light loads.

(QLLM Mode)



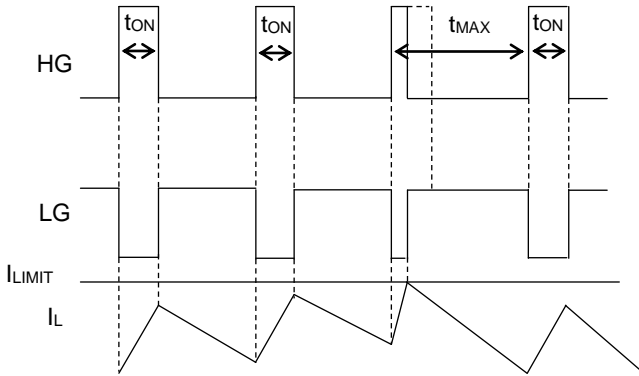
QLLM mode is enabled by setting the MODE pin to HiZ or middle voltage. When the lower gate is off and the current through the inductor is 0 (current flowing from V<sub>OUT</sub> to SW), QLLM mode is activated, disabling high gate output.

If V<sub>FB</sub> falls below V<sub>REF</sub> within a programmed time interval (typ 40µs), the high gate is switched on, but if V<sub>FB</sub> does not fall below V<sub>REF</sub>, the lower gate is forced on, dropping V<sub>FB</sub> and switching the high gate back on.

The minimum switching frequency is set to 25 kHz (T=40 µS), which keeps the regulator's frequency from entering the audible spectrum but yields less efficient results than SLLM mode.

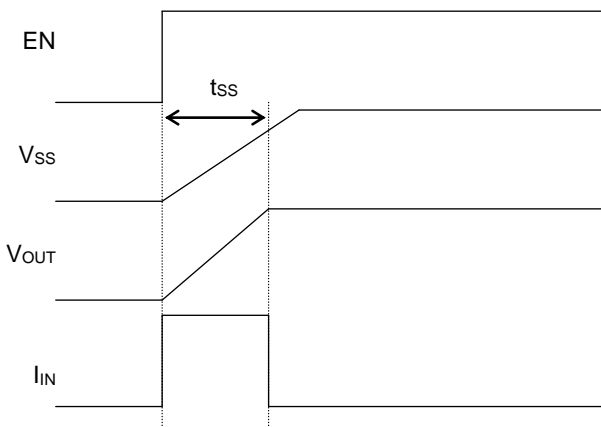
2. Timing Chart

(1) Over Current Protection



At normal operation, when V<sub>FB</sub> is at or below V<sub>REF</sub>, outputs HG at pulse range of t<sub>ON</sub> as in P8. But, if coil current exceed the limit point, it turns HG off. Next pulse returns to normal operation when output voltage decline after MAX ON TIME and I<sub>L</sub> is at or below I<sub>LIMIT</sub>.

(2) Soft Start Function



The soft start function is enabled when the EN pin is set to high. Current control circuitry takes effect at startup, yielding a moderate “ramping start” in output voltage. Soft start timing and incoming current are given by equation (2) and (3) below:

Soft start period:

$$t_{SS} = \frac{0.7(V) \times C_{SS}}{2.2\mu A(typ)} \quad [sec] \dots (2)$$

Rush current:

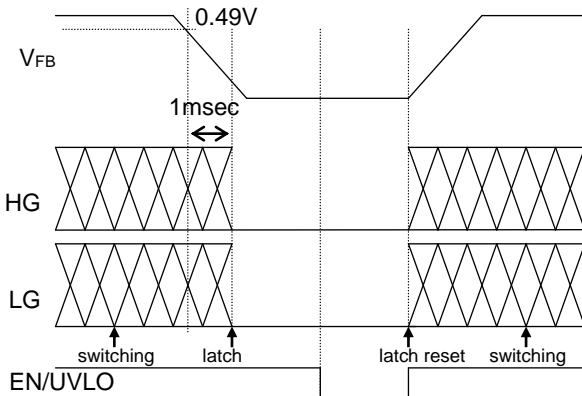
$$I_{IN}(ON) = \frac{C_o \times V_{OUT}}{t_{SS}} \quad [A] \dots (3)$$

Where:

C<sub>SS</sub> is the soft start capacitor

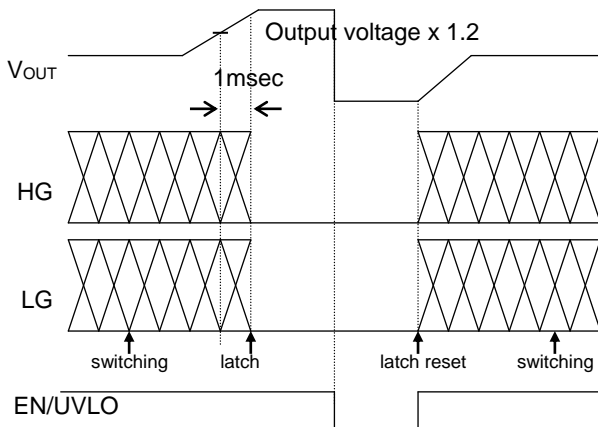
C<sub>o</sub> are all capacitors connected to V<sub>OUT</sub>

(3) Timer Latch-type Short Circuit Protection



When output voltage falls to 0.49V or less, the output short circuit protection is triggered, turning the IC OFF after a set period of time to prevent internal damage. When EN is switched back ON or when UVLO is cleared, output continues. The time period before shutting OFF is set internally at 1 ms.

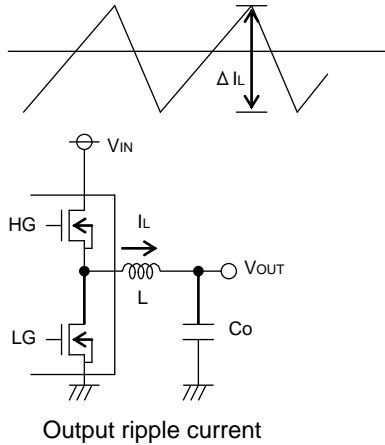
(4) Output Over-Voltage Protection



When output reaches or exceeds V<sub>REF</sub> × 1.2, the output over-voltage protection is triggered, turning the low-side FET completely ON to reduce the output (low gate ON, high gate OFF). When the output falls, it returns to standard mode.

3. External Component Selection

(1) Inductor (L) Selection



The inductor's value directly influences the output ripple current. As indicated by equation (4) below, the greater the inductance or switching frequency, the lower the ripple current:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f} \quad [A] \dots (4)$$

The proper output ripple current setting is about 30% of maximum output current.

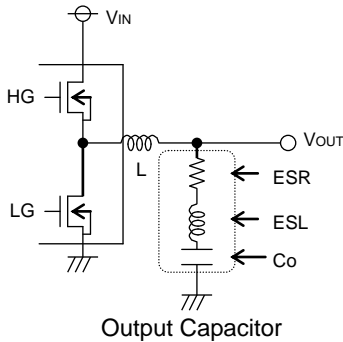
$$\Delta I_L = 0.3 \times I_{OUT\ MAX} \quad [A] \dots (5)$$

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I_L \times V_{IN} \times f} \quad [H] \dots (6)$$

Where:  
 $\Delta I_L$  is the output ripple current  
 $f$  is the switching frequency

- (a) Passing a current larger than the inductor's rated current will cause magnetic saturation in the inductor and decreases system efficiency. In selecting the inductor, be sure to allow enough margin to assure that peak current does not exceed the inductor's rated current value.
- (b) To minimize possible inductor damage and maximize efficiency, choose an inductor with low DCR and ACR.

(2) Output Capacitor Selection (Co)



When determining the proper output capacitor, be sure to consider the equivalent series resistance (ESR) and equivalent series inductance (ESL) required to set the output ripple voltage to 20 mV or more.

When selecting the limit of the inductor, be sure to allow enough margin for the output voltage. Output ripple voltage is determined by equation (7) below:

$$\Delta V_{OUT} = \Delta I_L \times ESR + ESL \times \Delta I_L / T_{ON} \dots (7)$$

Where:  
 $\Delta I_L$  is the output ripple current  
 $ESR$  is the equivalent series resistance  
 $ESL$  is the equivalent series inductance

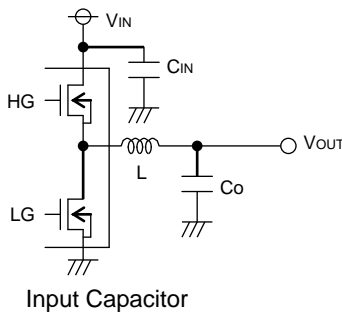
Give special consideration to the conditions of equation (8) for output capacitance. Also, keep in mind that the output rise time must be established within the soft start timeframe.

$$C_O \leq \frac{t_{SS} \times (I_{limit} - I_{OUT})}{V_{OUT}} \dots (8)$$

Where:  
 $t_{SS}$  is the soft-start timeframe (see p. 13, equation (2))  
 $I_{limit}$  is the maximum output current.  
 $I_{OUT}$  is the load current

Choosing a capacitance that is too large can cause startup malfunctions, or in some cases, may trigger the short circuit protection.

(3) Input Capacitor Selection (CIN)



In order to prevent extreme over-current conditions, the input capacitor must have a low enough ESR to fully support a large ripple in the output.

The formula for RMS ripple current ( $I_{RMS}$ ) is given by equation (9) below:

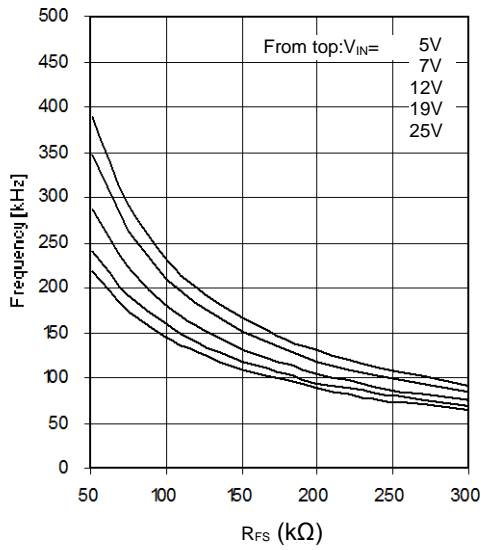
$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{IN} (V_{IN} - V_{OUT})}}{V_{IN}} \quad [A] \dots (9)$$

When,  $V_{IN} = 2 \times V_{OUT}$       $I_{RMS} = \frac{I_{OUT}}{2}$

A low-ESR capacitor is recommended to reduce ESR loss and maximize efficiency.

External Component Selection – continued

(4) Frequency Adjustment



The resistance connected to the FS terminal adjusts the on-time ( $t_{ON}$ ) during normal operation as illustrated on the left. When  $t_{ON}$ , input voltage and  $V_{REF}$  voltage are known, the switching frequency can be determined by the following equation:

$$F = \frac{V_{REF}}{V_{IN} \times t_{ON}} \dots (10)$$

$$V_{REF} = 0.7V$$

However, real-life considerations (such as external MOSFET gate capacitance and switching time) must be considered as they affect the overall switching rise and fall time. This leads to an increase in  $t_{ON}$ , and slight lowering of the total frequency.

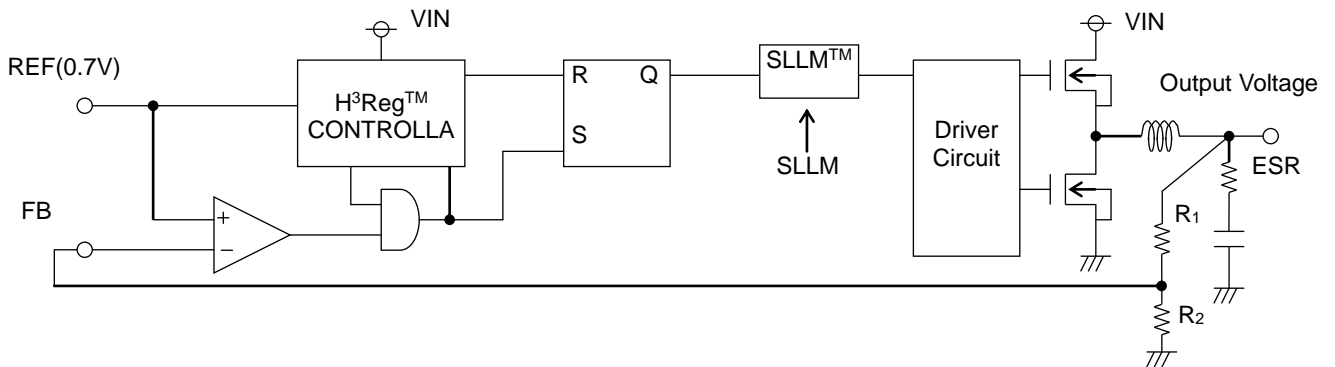
Additionally, when output current is around 0A in continuous mode, this “dead time” also has an effect on  $t_{ON}$ , further lowering the switching frequency. Confirm the switching frequency by measuring the current through the coil (at the point where current does not flow backwards) during normal operation.

The BD95514MUV operates by feeding the output voltage back through a resistive voltage divider. The output voltage is set by the following equation (see schematic below):

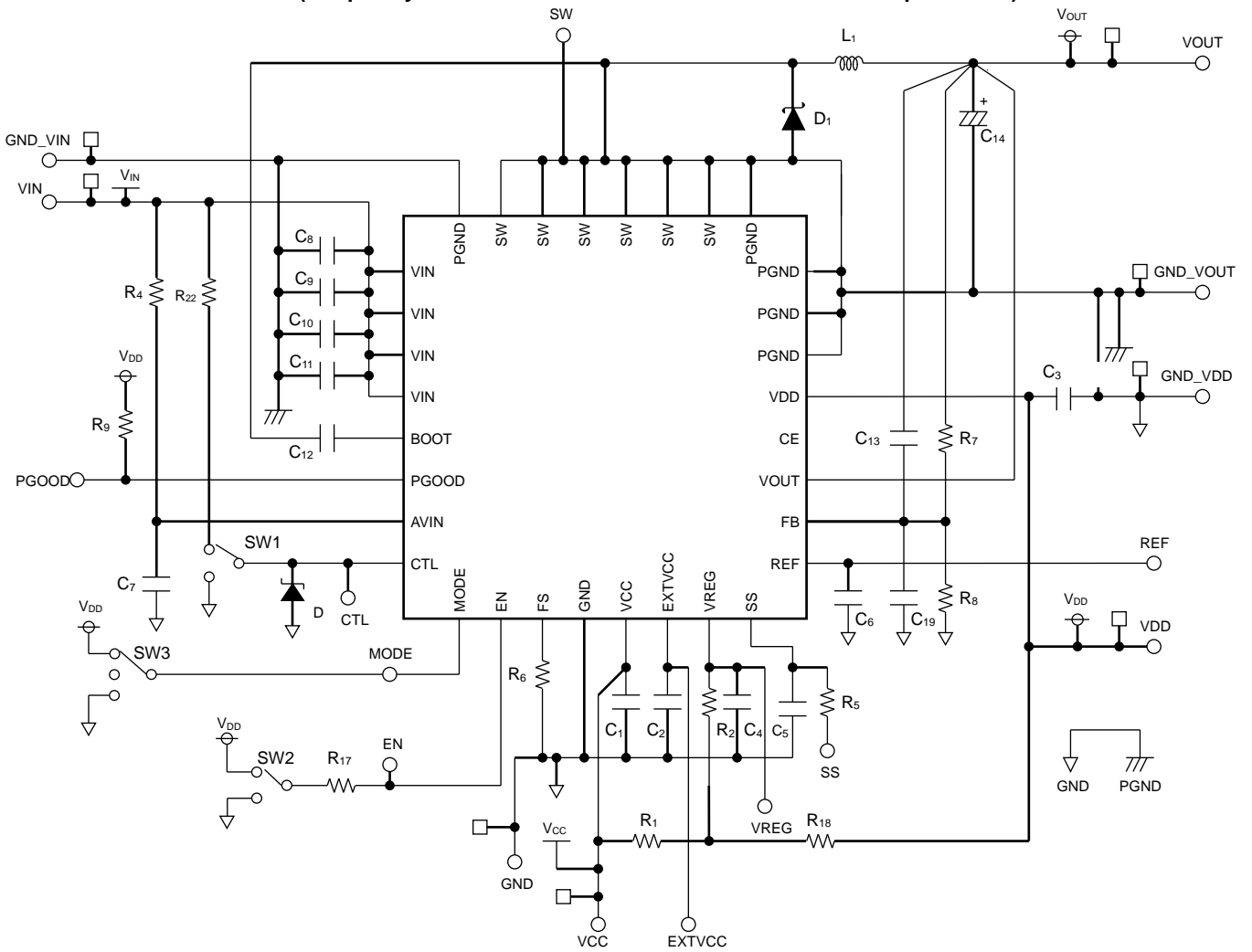
$$\text{Output Voltage} = \frac{R_1 + R_2}{R_2} \times V_{REF} (0.7V) + \frac{1}{2} \times \Delta I_L \times ESR \dots (11)$$

The switching frequency is also amplified by the same resistive voltage divider network:

$$f_{SW} = \frac{R_1 + R_2}{R_2} \times (\text{frequency set by } R_{FS}) \quad [Hz] \dots (12)$$



4. Evaluation Board Circuit (Frequency=300kHz Continuous Mode/QLLM/SLLM™ Sample Circuit)



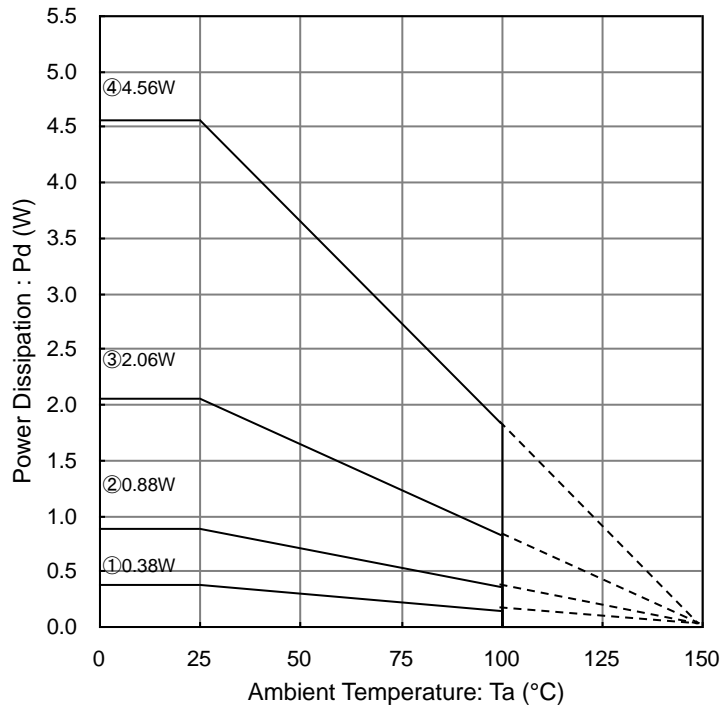
5. Evaluation Board Parts List

Designation	Rating	Part No.	Company
R1	10Ω	MCR03	ROHM
R2	0Ω	MCR03	ROHM
R4	10Ω	MCR03	ROHM
R5	10KΩ	MCR03	ROHM
R6	270KΩ	MCR03	ROHM
R7	10kΩ	MCR03	ROHM
R8	3.07kΩ	MCR03	ROHM
R9	100KΩ	MCR03	ROHM
R4	10Ω	MCR03	ROHM
R5	10KΩ	MCR03	ROHM
R17	0Ω	MCR03	ROHM
R18	0Ω	MCR03	ROHM
R18	0Ω	MCR03	ROHM
R22	510kΩ	MCR03	ROHM
C1	1μF	ceramic capacitor	-
C2	-	-	-
C3	1μF	ceramic capacitor	-

Designation	Rating	Part No.	Company
C4	1μF	ceramic capacitor	-
C5	3300pF	ceramic capacitor	-
C6	0.1μF	ceramic capacitor	-
C7	0.1μF	ceramic capacitor	-
C8	-	-	-
C9	-	-	-
C10	-	-	-
C11	22μF	ceramic capacitor	-
C12	0.1μF	ceramic capacitor	-
C13	1000pF	ceramic capacitor	-
C14	220μF	4TPE220MF	SANYO
C19	470pF	ceramic capacitor	-
C4	1μF	ceramic capacitor	-
C5	3300pF	ceramic capacitor	-
C6	0.1μF	ceramic capacitor	-
C7	0.1μF	ceramic capacitor	-

## Power Dissipation

VQFN032V5050



① IC Only

$$\theta_{j-a} = 328.9 \text{ }^{\circ}\text{C/W}$$

② IC mounted on 1-layer board (with 20.2 mm<sup>2</sup> copper thermal pad)

$$\theta_{j-a} = 142.0 \text{ }^{\circ}\text{C/W}$$

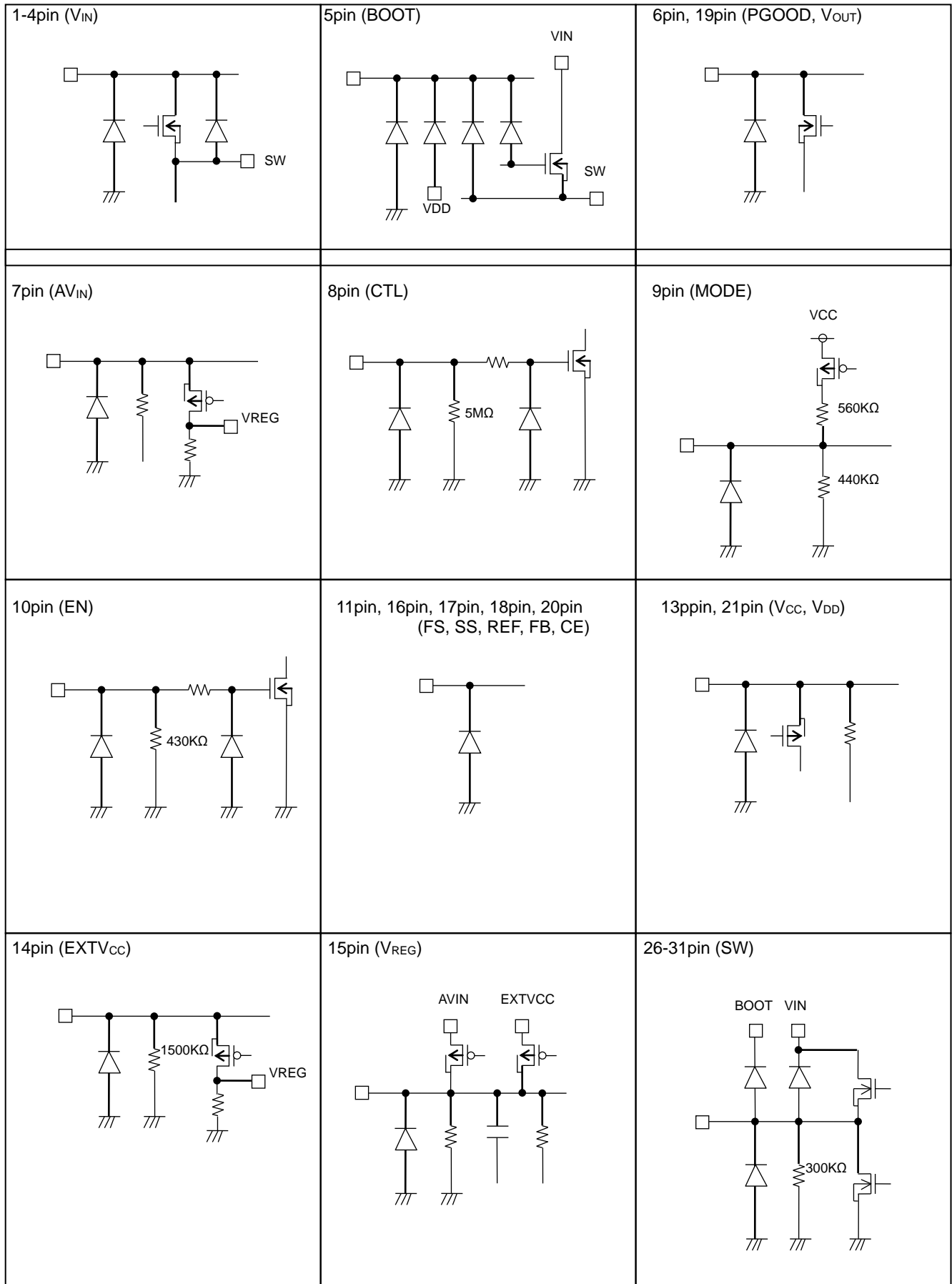
③ IC mounted on 4-layer board (with 20.2 mm<sup>2</sup> pad on top layer, 5505 mm<sup>2</sup> pad on layers 2,3)

$$\theta_{j-a} = 60.7 \text{ }^{\circ}\text{C/W}$$

④ IC mounted on 4-layer board (with 5505mm<sup>2</sup> pad on all layers)

$$\theta_{j-a} = 27.4 \text{ }^{\circ}\text{C/W}$$

I/O Equivalent Circuit



## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

### 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.  
 When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

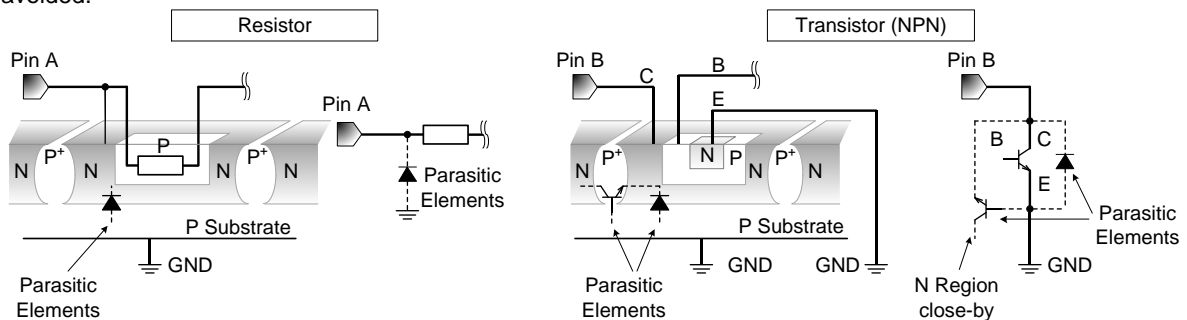


Figure 17. Example of monolithic IC structure

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF all output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

	TSD ON Temp. [°C] (typ)	Hysteresis Temp. [°C] (typ)
BD95514MUV	175	15

15. Ground wiring traces

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage.





**Revision History**

Date	Revision	Changes
27.Nov.2014	001	New Release

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CLASS IV		CLASS III	

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  - Sealing or coating our Products with resin or other coating materials
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  - Use of the Products in places subject to dew condensation
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- Confirm that operation temperature is within the specified range described in the product specification.
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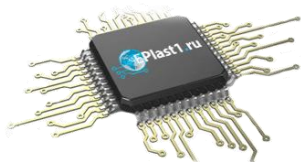
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