

# DAC7614

## Quad, Serial Input, 12-Bit, Voltage Output DIGITAL-TO-ANALOG CONVERTER

### FEATURES

- LOW POWER: 20mW
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 10 $\mu$ s to 0.012%
- 12-BIT LINEARITY AND MONOTONICITY:  
-40°C to +85°C
- USER SELECTABLE RESET TO MID-  
SCALE OR ZERO-SCALE
- SECOND-SOURCE for DAC8420
- SMALL 20-LEAD SSOP PACKAGE

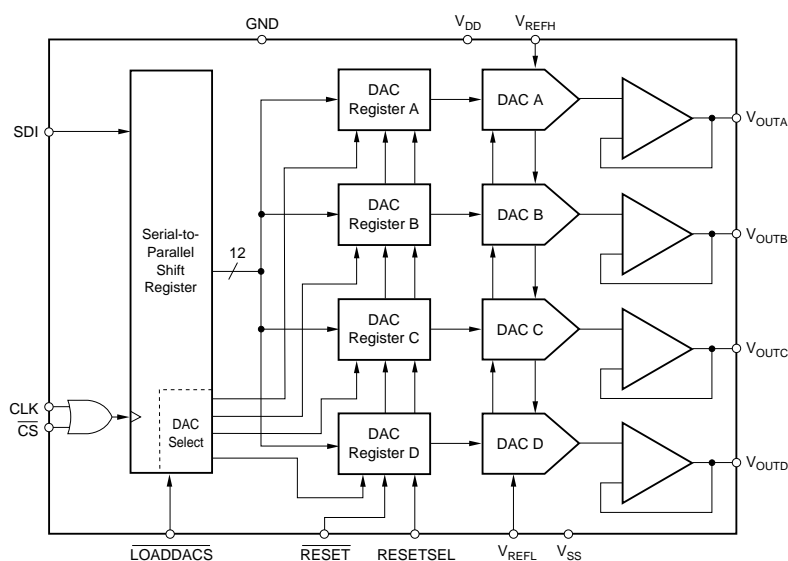
### APPLICATIONS

- ATE PIN ELECTRONICS
- PROCESS CONTROL
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS

### DESCRIPTION

The DAC7614 is a quad, serial input, 12-bit, voltage output digital-to-analog converter (DAC) with guaranteed 12-bit monotonic performance over the -40°C to +85°C temperature range. An asynchronous reset clears all registers to either mid-scale (800<sub>H</sub>) or zero-scale (000<sub>H</sub>), selectable via the RESETSEL pin. The device can be powered from a single +5V supply or from dual +5V and -5V supplies.

Low power and small size makes the DAC7614 ideal for process control, data acquisition systems, and closed-loop servo-control. The device is available in 16-pin plastic DIP, 16-lead SOIC, or 20-lead SSOP packages, and is guaranteed over the -40°C to +85°C temperature range.



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Twx: 910-952-1111 • Internet: <http://www.burr-brown.com/> • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = +5\text{V}$ ,  $V_{SS} = -5\text{V}$ ,  $V_{REFH} = +2.5\text{V}$ , and  $V_{REFL} = -2.5\text{V}$ , unless otherwise noted.

| PARAMETER                          | CONDITIONS  | DAC7614E, P, U      |            |                   | DAC7614EB, PB, UB |     |         | UNITS                   |
|------------------------------------|---|---------------------|------------|-------------------|-------------------|-----|---------|-------------------------|
|                                    |   | MIN                 | TYP        | MAX               | MIN               | TYP | MAX     |                         |
| <b>ACCURACY</b>                    |   |                     |            |                   |                   |     |         |                         |
| Linearity Error <sup>(1)</sup>     | $V_{SS} = 0\text{V}$ or $-5\text{V}$                                | 12                  |            | $\pm 2$           | *                 |     | $\pm 1$ | LSB <sup>(2)</sup>      |
| Linearity Matching <sup>(3)</sup>  | $V_{SS} = 0\text{V}$ or $-5\text{V}$                                |                     |            | $\pm 2$           |                   |     | $\pm 1$ | LSB                     |
| Differential Linearity Error       | $V_{SS} = 0\text{V}$ or $-5\text{V}$                                |                     |            | $\pm 1$           |                   |     | $\pm 1$ | LSB                     |
| Monotonicity                       |   |                     |            |                   |                   |     |         | Bits                    |
| Zero-Scale Error                   | Code = $000_H$  |                     |            | $\pm 4$           |                   |     | *       | LSB                     |
| Zero-Scale Drift                   |   |                     | 2          | 5                 |                   | *   | *       | ppm/ $^{\circ}\text{C}$ |
| Zero-Scale Matching <sup>(3)</sup> |   |                     |            | $\pm 2$           |                   |     | $\pm 1$ | LSB                     |
| Full-Scale Error                   | Code = $FFF_H$  |                     |            | $\pm 4$           |                   |     | *       | LSB                     |
| Full-Scale Matching <sup>(3)</sup> |   |                     |            | $\pm 2$           |                   |     | $\pm 1$ | LSB                     |
| Zero-Scale Error                   | Code = $00A_H$ , $V_{SS} = 0\text{V}$                               |                     |            | $\pm 8$           |                   |     | *       | LSB                     |
| Zero-Scale Drift                   | $V_{SS} = 0\text{V}$  |                     | 5          | 10                |                   | *   | *       | ppm/ $^{\circ}\text{C}$ |
| Zero-Scale Matching <sup>(3)</sup> | $V_{SS} = 0\text{V}$  |                     |            | $\pm 4$           |                   |     | $\pm 2$ | LSB                     |
| Full-Scale Error                   | Code = $FFF_H$ , $V_{SS} = 0\text{V}$                               |                     |            | $\pm 8$           |                   |     | *       | LSB                     |
| Full-Scale Matching <sup>(3)</sup> | $V_{SS} = 0\text{V}$  |                     |            | $\pm 4$           |                   |     | $\pm 2$ | LSB                     |
| Power Supply Rejection             |   |                     | 30         |                   |                   | *   |         | ppm/V                   |
| <b>ANALOG OUTPUT</b>               |   |                     |            |                   |                   |     |         |                         |
| Voltage Output <sup>(4)</sup>      | $V_{SS} = 0\text{V}$ or $-5\text{V}$                                | $V_{REFL}$          |            | $V_{REFH}$        | *                 |     | *       | V                       |
| Output Current                     |   | $-1.25$             |            | $+1.25$           | *                 |     | *       | mA                      |
| Load Capacitance                   | No Oscillation  |                     | 100        |                   |                   | *   |         | pF                      |
| Short-Circuit Current              |   |                     | $+5, -15$  |                   |                   | *   |         | mA                      |
| Short-Circuit Duration             |   |                     | Indefinite |                   |                   | *   |         |                         |
| <b>REFERENCE INPUT</b>             |   |                     |            |                   |                   |     |         |                         |
| $V_{REFH}$ Input Range             | $V_{SS} = 0\text{V}$ or $-5\text{V}$                                | $V_{REFL} + 1.25$   |            | $+2.5$            | *                 |     | *       | V                       |
| $V_{REFL}$ Input Range             | $V_{SS} = 0\text{V}$  | 0                   |            | $V_{REFH} - 1.25$ | *                 |     | *       | V                       |
| $V_{REFL}$ Input Range             | $V_{SS} = -5\text{V}$   | $-2.5$              |            | $V_{REFH} - 1.25$ | *                 |     | *       | V                       |
| <b>DYNAMIC PERFORMANCE</b>         |   |                     |            |                   |                   |     |         |                         |
| Settling Time <sup>(5)</sup>       | To $\pm 0.012\%$  |                     | 5          | 10                |                   | *   | *       | $\mu\text{s}$           |
| Channel-to-Channel Crosstalk       | Full-Scale Step   |                     | 0.1        |                   |                   | *   |         | LSB                     |
| Output Noise Voltage               | On Any Other DAC, $R_L = 2\text{k}\Omega$<br>Bandwidth: 0Hz to 1MHz |                     | 40         |                   |                   | *   |         | nV/ $\sqrt{\text{Hz}}$  |
| <b>DIGITAL INPUT/OUTPUT</b>        |   |                     |            |                   |                   |     |         |                         |
| Logic Family                       |   | TTL-Compatible CMOS |            |                   |                   |     | *       |                         |
| Logic Levels                       |   |                     |            |                   |                   |     |         |                         |
| $V_{IH}$                           | $ I_{IH}  \leq 10\mu\text{A}$                                       | 2.4                 |            | $V_{DD} + 0.3$    | *                 |     | *       | V                       |
| $V_{IL}$                           | $ I_{IL}  \leq 10\mu\text{A}$                                       | $-0.3$              |            | 0.8               | *                 |     | *       | V                       |
| Data Format                        |   | Straight Binary     |            |                   |                   | *   |         |                         |
| <b>POWER SUPPLY REQUIREMENTS</b>   |   |                     |            |                   |                   |     |         |                         |
| $V_{DD}$                           | If $V_{SS} \neq 0\text{V}$  | 4.75                |            | 5.25              | *                 |     | *       | V                       |
| $V_{SS}$                           |   | $-5.25$             |            | $-4.75$           | *                 |     | *       | V                       |
| $I_{DD}$                           |   |                     | 1.5        | 1.9               |                   | *   | *       | mA                      |
| $I_{SS}$                           |   | $-2.1$              | $-1.6$     |                   | *                 | *   | *       | mA                      |
| Power Dissipation                  | $V_{SS} = -5\text{V}$   |                     | 15         | 20                |                   | *   | *       | mW                      |
|                                    | $V_{SS} = 0\text{V}$  |                     | 7.5        | 10                |                   | *   | *       | mW                      |
| <b>TEMPERATURE RANGE</b>           |   |                     |            |                   |                   |     |         |                         |
| Specified Performance              |   | $-40$               |            | $+85$             | *                 |     | *       | $^{\circ}\text{C}$      |

\* Specification same as grade to the left.

NOTES: (1) If  $V_{SS} = 0\text{V}$ , specification applies at code  $00A_H$  and above. (2) LSB means Least Significant Bit, with  $V_{REFH}$  equal to  $+2.5\text{V}$  and  $V_{REFL}$  equal to  $-2.5\text{V}$ , one LSB is  $1.22\text{mV}$ . (3) All DAC outputs will match within the specified error band. (4) Ideal output voltage, does not take into account zero or full-scale error. (5) If  $V_{SS} = -5\text{V}$ , full-scale step from code  $000_H$  to  $FFF_H$  or vice-versa. If  $V_{SS} = 0\text{V}$ , full-scale positive step from code  $000_H$  to  $FFF_H$  and negative step from code  $FFF_H$  to  $00A_H$ .

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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

|   |                                |
|---|--------------------------------|
| $V_{DD}$ to $V_{SS}$ .....              | –0.3V to +11V                  |
| $V_{DD}$ to GND .....                   | –0.3V to +5.5V                 |
| $V_{REFL}$ to $V_{SS}$ .....            | –0.3V to ( $V_{DD} - V_{SS}$ ) |
| $V_{DD}$ to $V_{REFH}$ .....            | –0.3V to ( $V_{DD} - V_{SS}$ ) |
| $V_{REFH}$ to $V_{REFL}$ .....          | –0.3V to ( $V_{DD} - V_{SS}$ ) |
| Digital Input Voltage to GND .....      | –0.3V to $V_{DD} + 0.3V$       |
| Maximum Junction Temperature .....      | +150°C                         |
| Operating Temperature Range .....       | –40°C to +85°C                 |
| Storage Temperature Range .....         | –65°C to +150°C                |
| Lead Temperature (soldering, 10s) ..... | +300°C                         |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

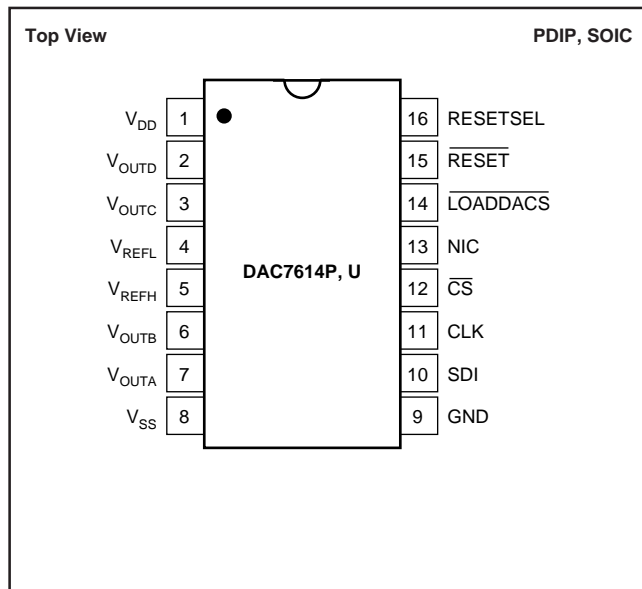
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

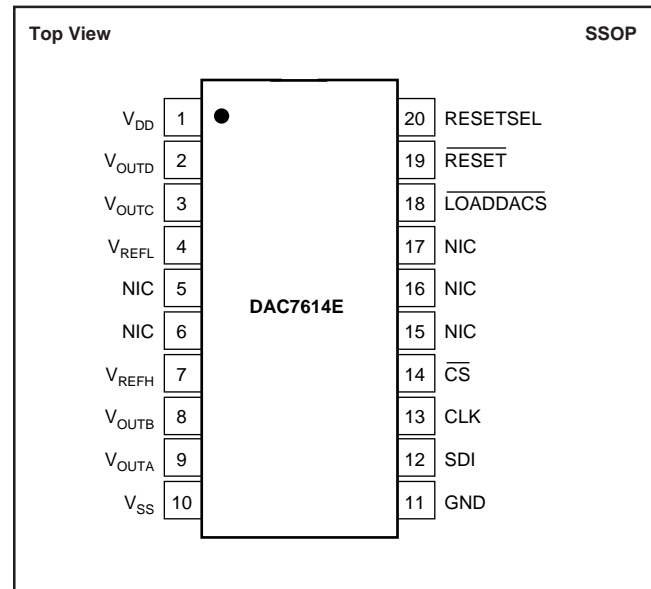
| PRODUCT   | MAXIMUM LINEARITY ERROR (LSB) | MAXIMUM DIFFERENTIAL LINEARITY (LSB) | PACKAGE      | PACKAGE DRAWING NUMBER <sup>(1)</sup> | SPECIFICATION TEMPERATURE RANGE | ORDERING NUMBER <sup>(2)</sup> | TRANSPORT MEDIA |
|-----------|-------------------------------|--------------------------------------|--------------|---------------------------------------|---------------------------------|--------------------------------|-----------------|
| DAC7614P  | ±2                            | ±1                                   | 16-Pin DIP   | 180                                   | –40°C to +85°C                  | DAC7614P                       | Rails           |
| DAC7614PB | ±1                            | "                                    | "            | "                                     | "                               | DAC7614PB                      | Rails           |
| DAC7614U  | ±2                            | ±1                                   | 16-Lead SOIC | 211                                   | –40°C to +85°C                  | DAC7614U                       | Rails           |
| "         | "                             | "                                    | "            | "                                     | "                               | DAC7614U/1K                    | Tape and Reel   |
| DAC7614UB | ±1                            | ±1                                   | 16-Lead SOIC | 211                                   | –40°C to +85°C                  | DAC7614UB                      | Rails           |
| "         | "                             | "                                    | "            | "                                     | "                               | DAC7614UB/1K                   | Tape and Reel   |
| DAC7614E  | ±2                            | ±1                                   | 20-Lead SSOP | 334                                   | –40°C to +85°C                  | DAC7614E                       | Rails           |
| "         | "                             | "                                    | "            | "                                     | "                               | DAC7614E/1K                    | Tape and Reel   |
| DAC7614EB | ±1                            | ±1                                   | 20-Lead SSOP | 334                                   | –40°C to +85°C                  | DAC7614EB                      | Rails           |
| "         | "                             | "                                    | "            | "                                     | "                               | DAC7614EB/1K                   | Tape and Reel   |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DAC7614EB/1K" will get a single 1000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

## PIN CONFIGURATION—P, U Packages



## PIN CONFIGURATION—E Package



## PIN DESCRIPTIONS—P, U Packages

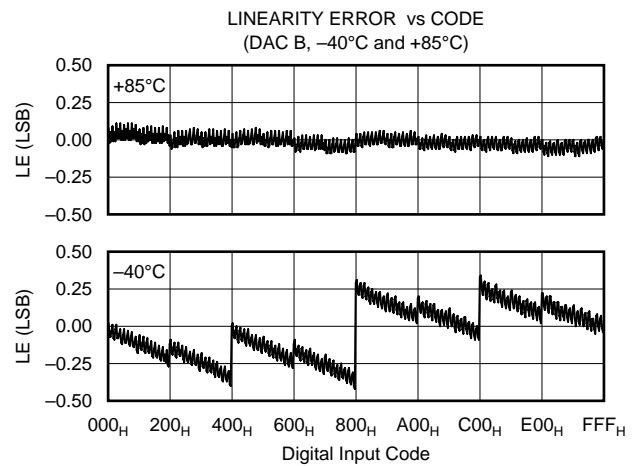
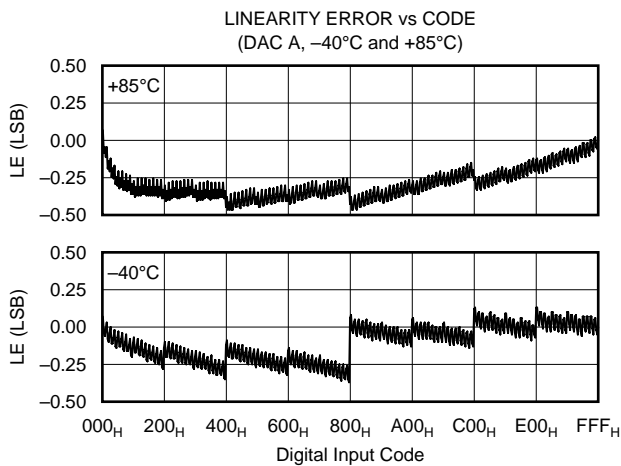
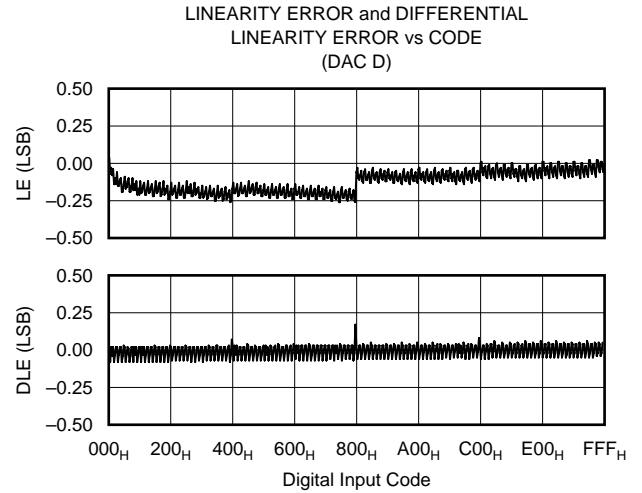
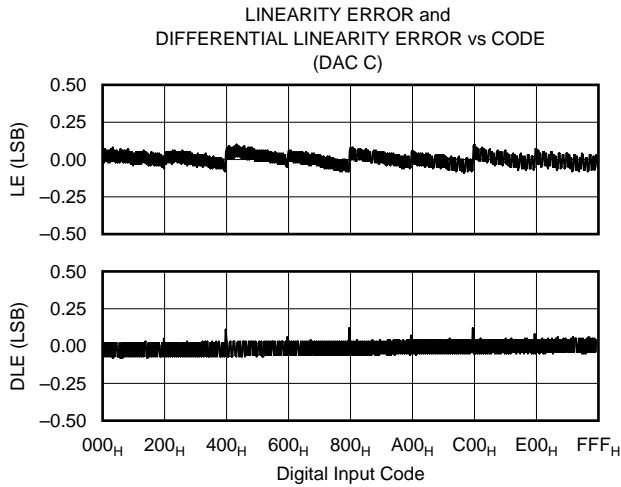
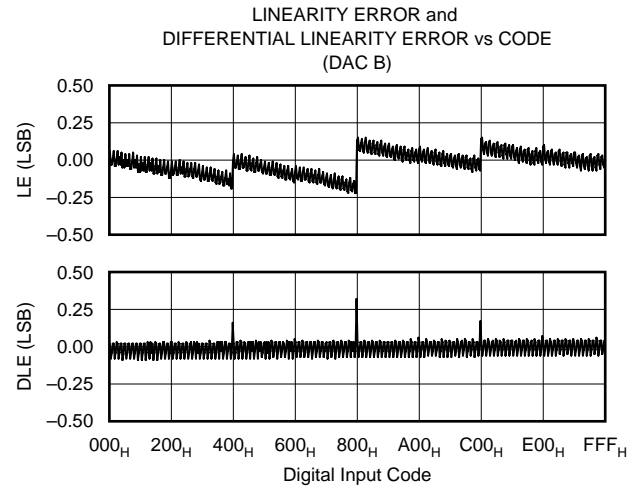
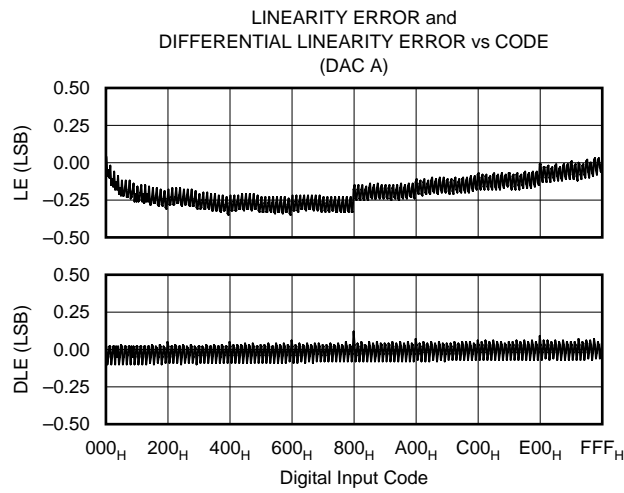
| PIN | LABEL                 | DESCRIPTION  |
|-----|-----------------------|--|
| 1   | $V_{DD}$              | Positive Analog Supply Voltage, +5V nominal.   |
| 2   | $V_{OUTD}$            | DAC D Voltage Output   |
| 3   | $V_{OUTC}$            | DAC C Voltage Output   |
| 4   | $V_{REFL}$            | Reference Input Voltage Low. Sets minimum output voltage for all DACs.   |
| 5   | $V_{REFH}$            | Reference Input Voltage High. Sets maximum output voltage for all DACs.  |
| 6   | $V_{OUTB}$            | DAC B Voltage Output   |
| 7   | $V_{OUTA}$            | DAC A Voltage Output   |
| 8   | $V_{SS}$              | Negative Analog Supply Voltage, 0V or –5V nominal.   |
| 9   | GND                   | Ground   |
| 10  | SDI                   | Serial Data Input  |
| 11  | CLK                   | Serial Data Clock  |
| 12  | $\overline{CS}$       | Chip Select Input  |
| 13  | NIC                   | Not Internally Connected.  |
| 14  | $\overline{LOADDACs}$ | The selected DAC register becomes transparent when $\overline{LOADDACs}$ is LOW. It is in the latched state when $\overline{LOADDACs}$ is HIGH.  |
| 15  | $\overline{RESET}$    | Asynchronous Reset Input. Sets all DAC registers to either zero-scale (000 <sub>H</sub> ) or mid-scale (800 <sub>H</sub> ) when LOW. RESETSEL determines which code is active.                               |
| 16  | RESETSEL              | When LOW, a LOW on $\overline{RESET}$ will cause all DAC registers to be set to code 000 <sub>H</sub> . When RESETSEL is HIGH, a LOW on $\overline{RESET}$ will set the registers to code 800 <sub>H</sub> . |

## PIN DESCRIPTIONS—E Package

| PIN | LABEL                 | DESCRIPTION  |
|-----|-----------------------|--|
| 1   | $V_{DD}$              | Positive Analog Supply Voltage, +5V nominal.   |
| 2   | $V_{OUTD}$            | DAC D Voltage Output   |
| 3   | $V_{OUTC}$            | DAC C Voltage Output   |
| 4   | $V_{REFL}$            | Reference Input Voltage Low. Sets minimum output voltage for all DACs.   |
| 5   | NIC                   | Not Internally Connected.  |
| 6   | NIC                   | Not Internally Connected.  |
| 7   | $V_{REFH}$            | Reference Input Voltage High. Sets maximum output voltage for all DACs.  |
| 8   | $V_{OUTB}$            | DAC B Voltage Output.  |
| 9   | $V_{OUTA}$            | DAC A Voltage Output.  |
| 10  | $V_{SS}$              | Negative Analog Supply Voltage, 0V or –5V nominal.   |
| 11  | GND                   | Ground   |
| 12  | SDI                   | Serial Data Input  |
| 13  | CLK                   | Serial Data Clock  |
| 14  | $\overline{CS}$       | Chip Select Input  |
| 15  | NIC                   | Not Internally Connected.  |
| 16  | NIC                   | Not Internally Connected.  |
| 17  | NIC                   | Not Internally Connected.  |
| 18  | $\overline{LOADDACs}$ | The selected DAC register becomes transparent when $\overline{LOADDACs}$ is LOW. It is in the latched state when $\overline{LOADDACs}$ is HIGH.  |
| 19  | $\overline{RESET}$    | Asynchronous Reset Input. Sets all DAC registers to either zero-scale (000 <sub>H</sub> ) or mid-scale (800 <sub>H</sub> ) when LOW. RESETSEL determines which code is active.                               |
| 20  | RESETSEL              | When LOW, a LOW on $\overline{RESET}$ will cause all DAC registers to be set to code 000 <sub>H</sub> . When RESETSEL is HIGH, a LOW on $\overline{RESET}$ will set the registers to code 800 <sub>H</sub> . |

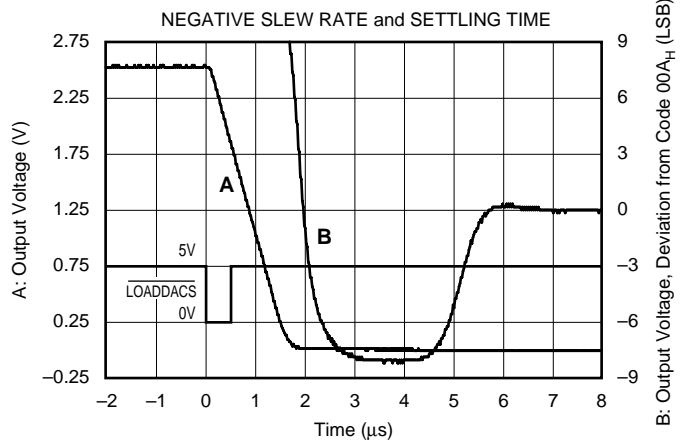
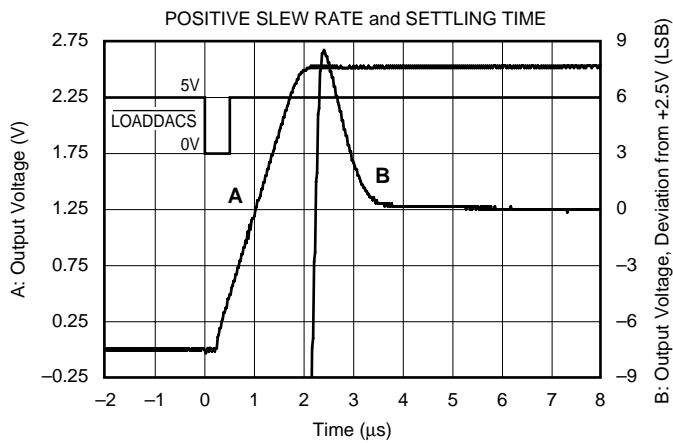
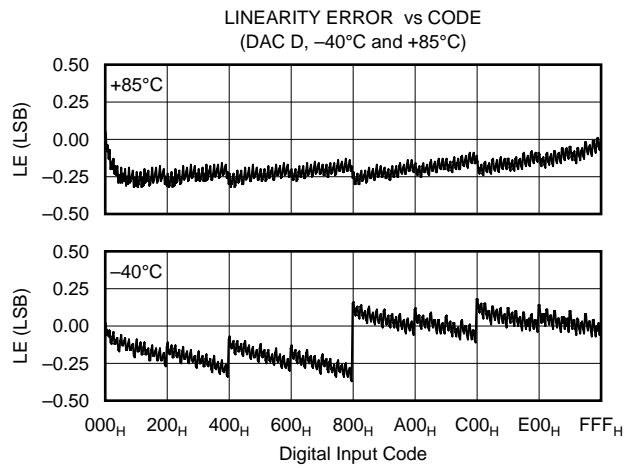
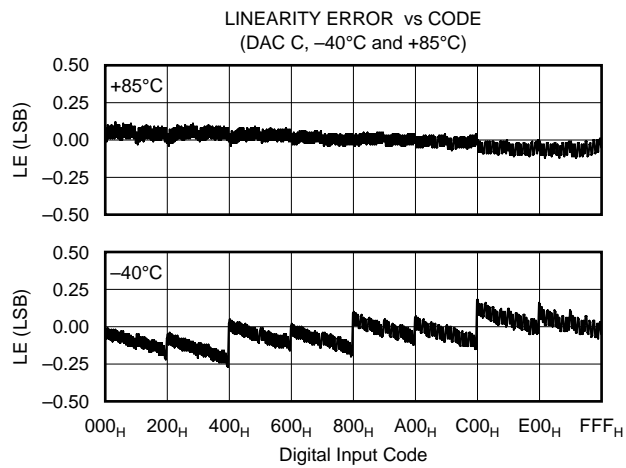
# TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$

At  $T_A = +25^\circ C$ ,  $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{REFH} = +2.5V$ , and  $V_{REFL} = 0V$ , representative unit, unless otherwise specified.



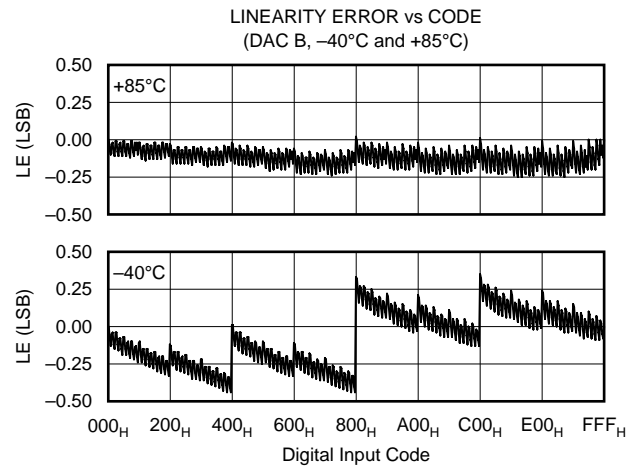
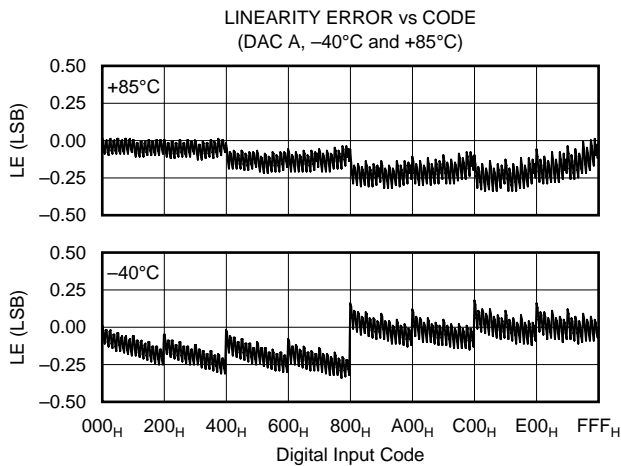
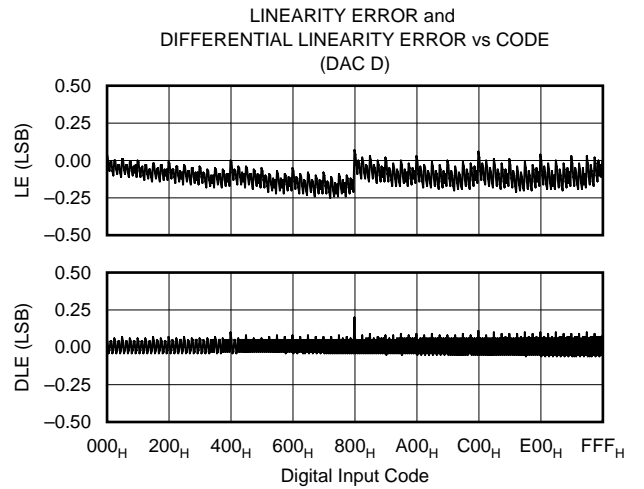
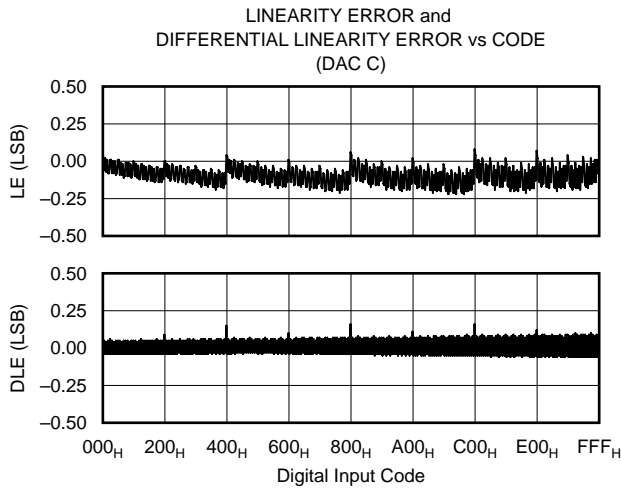
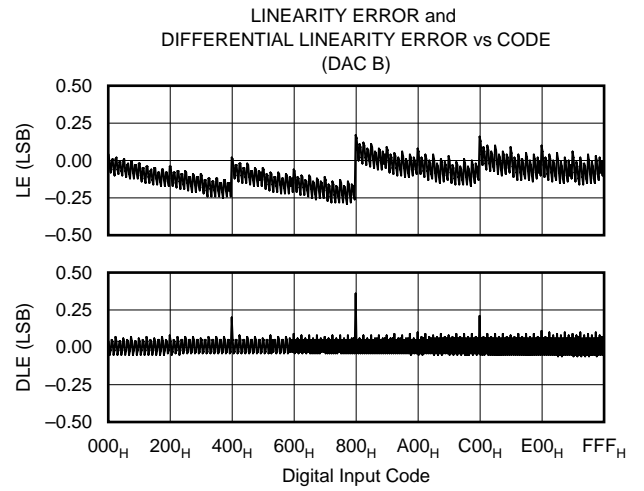
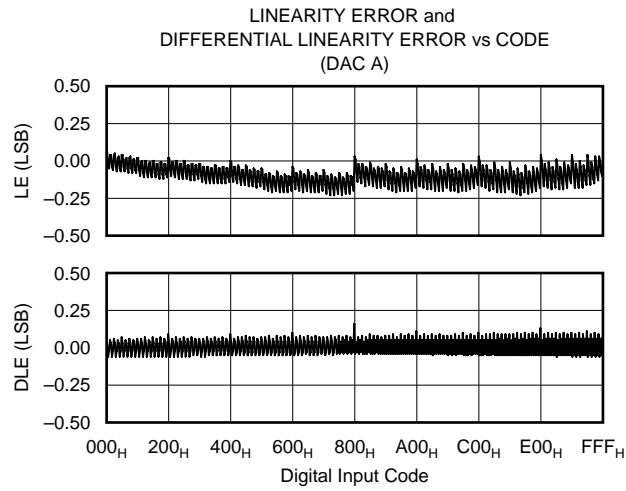
# TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (CONT)

At  $T_A = +25^\circ C$ ,  $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{REFH} = +2.5V$ , and  $V_{REFL} = 0V$ , representative unit, unless otherwise specified.



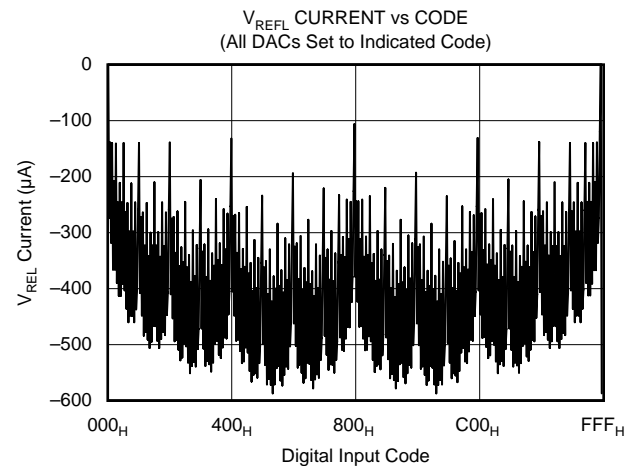
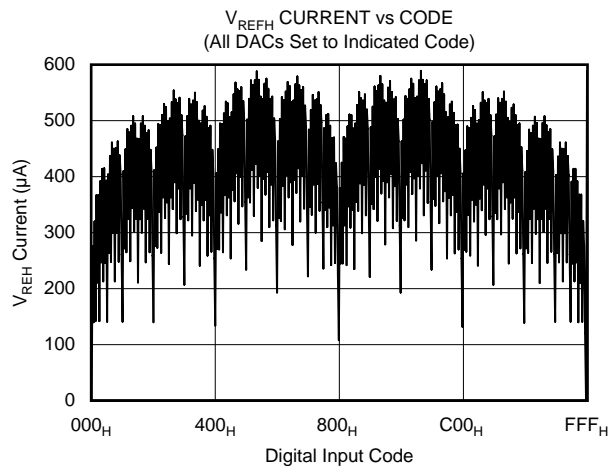
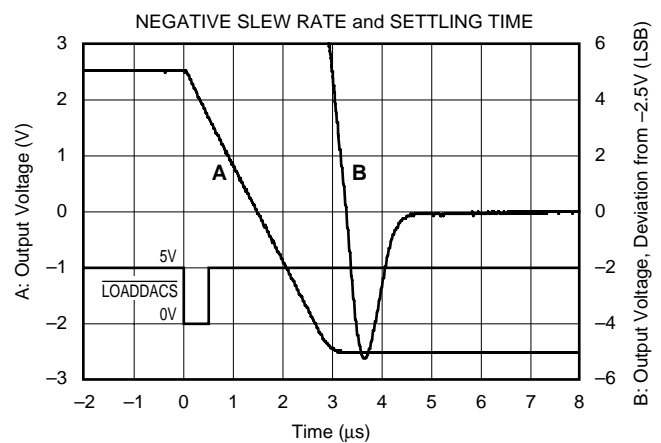
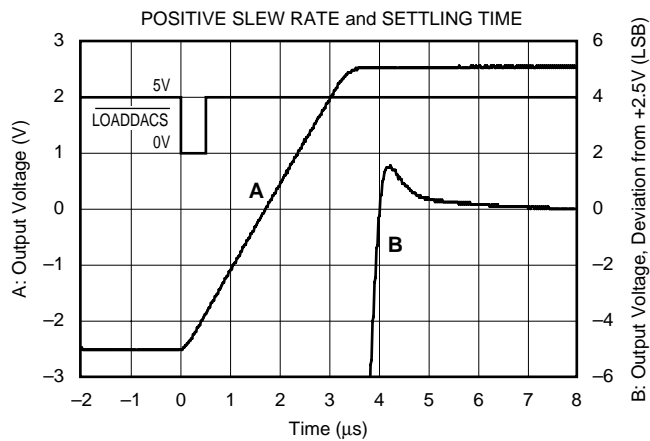
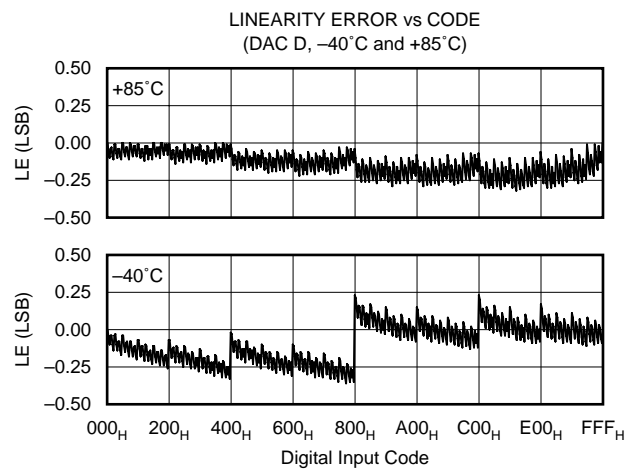
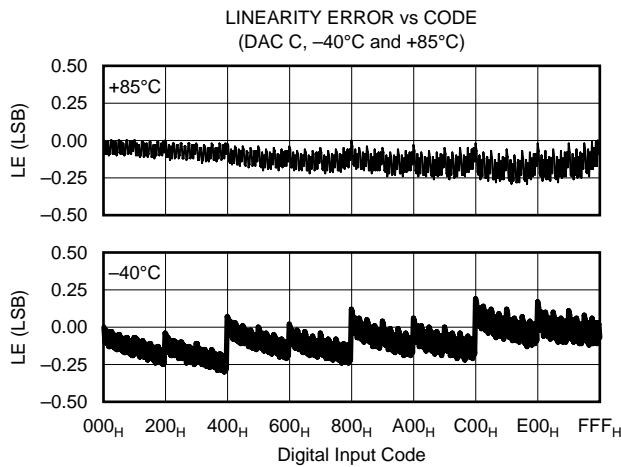
# TYPICAL PERFORMANCE CURVES: $V_{SS} = -5V$

At  $T_A = +25^\circ C$ ,  $V_{DD} = +5V$ ,  $V_{SS} = -5V$ ,  $V_{REFH} = +2.5V$ , and  $V_{REFL} = -2.5V$ , representative unit, unless otherwise specified.



# TYPICAL PERFORMANCE CURVES: $V_{SS} = -5V$ (CONT)

At  $T_A = +25^\circ C$ ,  $V_{DD} = +5V$ ,  $V_{SS} = -5V$ ,  $V_{REFH} = +2.5V$ , and  $V_{REFL} = -2.5V$ , representative unit, unless otherwise specified.





# THEORY OF OPERATION

The DAC7614 is a quad, serial input, 12-bit, voltage output DAC. The architecture is a classic R-2R ladder configuration followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network and output op amp, but all share the reference voltage inputs. The minimum voltage output (“zero-scale”) and maximum voltage output (“full-scale”) are set by external voltage references ( $V_{REFL}$  and  $V_{REFH}$ , respectively). The digital input is a 16-bit serial word that contains the 12-bit DAC code and a 2-bit address code that selects one of the four DACs (the two remaining bits are unused). The converter can be powered from a single +5V supply or a dual  $\pm 5V$  supply. Each device offers a reset function which immediately sets all DAC output voltages and internal registers to either zero-scale (code 000<sub>H</sub>) or mid-scale (code 800<sub>H</sub>). The reset code is selected by the state of the RESETSEL pin (LOW = 000<sub>H</sub>, HIGH = 800<sub>H</sub>). See Figures 1 and 2 for the basic operation of the DAC7614.

## ANALOG OUTPUTS

When  $V_{SS} = -5V$  (dual supply operation), the output amplifier can swing to within 2.25V of the supply rails, over the  $-40^{\circ}C$  to  $+85^{\circ}C$  temperature range. With  $V_{SS} = 0V$  (single-supply operation), the output can swing to ground. Note that the settling time of the output op amp will be longer with voltages very near ground. Also, care must be taken when measuring the zero-scale error when  $V_{SS} = 0V$ . If the output amplifier has a negative offset, the output voltage may not change for the first few digital input codes (000<sub>H</sub>, 001<sub>H</sub>, 002<sub>H</sub>, etc.) since the output voltage cannot swing below ground.

The behavior of the output amplifier can be critical in some applications. Under short-circuit conditions (DAC output shorted to ground), the output amplifier can sink a great deal more current than it can source. See the Specifications table for more details concerning short-circuit current.

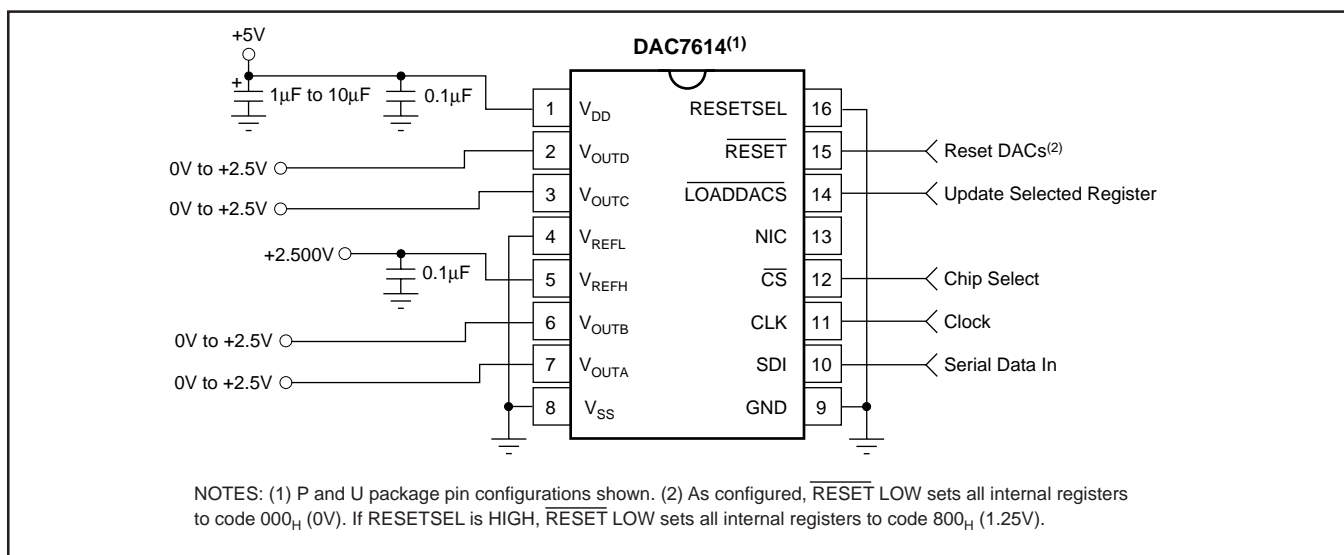


FIGURE 1. Basic Single-Supply Operation of the DAC7614.

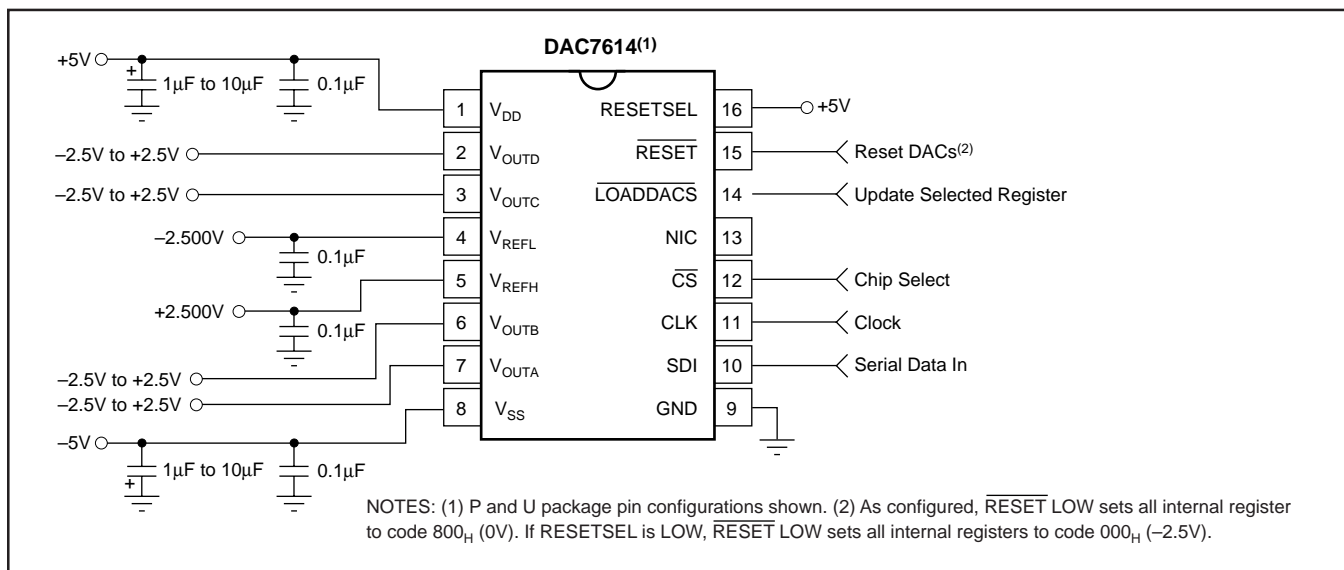


FIGURE 2. Basic Dual-Supply Operation of the DAC7614.

## REFERENCE INPUTS

The reference inputs,  $V_{REFL}$  and  $V_{REFH}$ , can be any voltage between  $V_{SS} + 2.25V$  and  $V_{DD} - 2.25V$  provided that  $V_{REFH}$  is at least 1.25V greater than  $V_{REFL}$ . The minimum output of each DAC is equal to  $V_{REFL} - 1LSB$  plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to  $V_{REFH}$  plus a similar offset voltage. Note that  $V_{SS}$  (the negative power supply) must either be connected to ground or must be in the range of  $-4.75V$  to  $-5.25V$ . The voltage on  $V_{SS}$  sets several bias points within the converter. If  $V_{SS}$  is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the reference inputs depends on the DAC output voltages and can vary from a few microamps to approximately 0.6 milliamp. Bypassing the reference voltage or voltages with a  $0.1\mu F$  capacitor placed as close as possible to the DAC7614 package is strongly recommended.

## DIGITAL INTERFACE

Figure 3 and Table I provide the basic timing for the DAC7614. The interface consists of a serial clock (CLK), serial data (SDI), and a load DAC signal ( $\overline{LOADDAC}$ ). In addition, a chip select ( $\overline{CS}$ ) input is available to enable serial communication when there are multiple serial devices. An

| SYMBOL     | DESCRIPTION                              | MIN | TYP | MAX | UNITS   |
|------------|--|-----|-----|-----|---------|
| $t_{DS}$   | Data Valid to CLK Rising                 | 25  |     |     | ns      |
| $t_{DH}$   | Data Held Valid after CLK Rises          | 20  |     |     | ns      |
| $t_{CH}$   | CLK HIGH                                 | 30  |     |     | ns      |
| $t_{CL}$   | CLK LOW                                  | 50  |     |     | ns      |
| $t_{CSS}$  | $\overline{CS}$ LOW to CLK Rising        | 55  |     |     | ns      |
| $t_{CSH}$  | CLK HIGH to $\overline{CS}$ Rising       | 15  |     |     | ns      |
| $t_{LD1}$  | $\overline{LOADDAC}$ HIGH to CLK Rising  | 40  |     |     | ns      |
| $t_{LD2}$  | CLK Rising to $\overline{LOADDAC}$ LOW   | 15  |     |     | ns      |
| $t_{LDDW}$ | $\overline{LOADDAC}$ LOW Time            | 45  |     |     | ns      |
| $t_{RSSH}$ | RESETSEL Valid to $\overline{RESET}$ LOW | 25  |     |     | ns      |
| $t_{RSTW}$ | $\overline{RESET}$ LOW Time              | 70  |     |     | ns      |
| $t_s$      | Settling Time                            | 10  |     |     | $\mu s$ |

TABLE I. Timing Specifications ( $T_A = -40^\circ C$  to  $+85^\circ C$ ).

asynchronous reset input ( $\overline{RESET}$ ) is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state.

The DAC code and address are provided via a 16-bit serial interface as shown in Figure 3. The first two bits select the DAC register that will be updated when  $\overline{LOADDAC}$  goes LOW (see Table II). The next two bits are not used. The last 12 bits is the DAC code which is provided, most significant bit first.

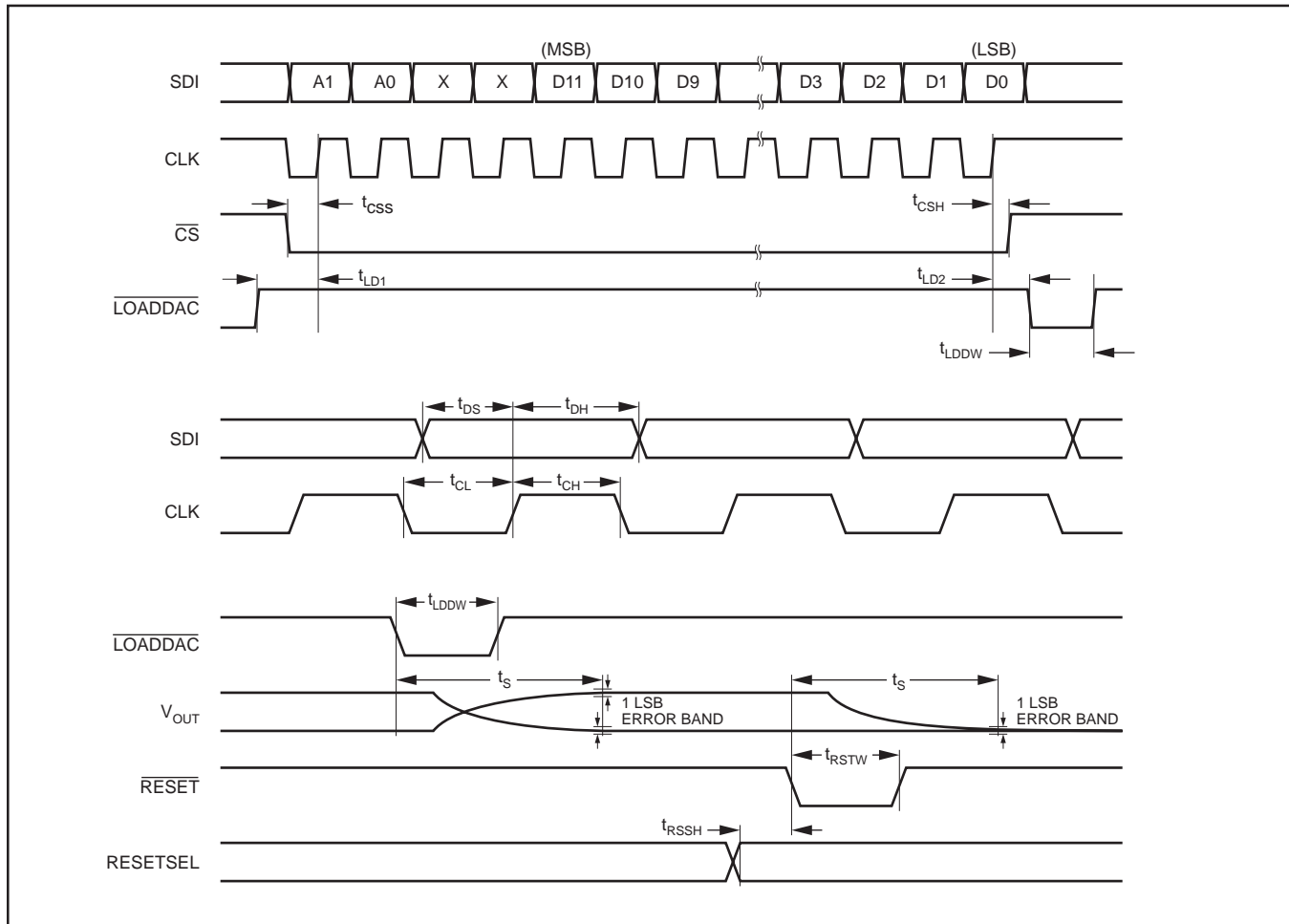


FIGURE 3. DAC7614 Timing.

| A1               | A0 | LOADDAC $\overline{\text{S}}$ | RESET | SELECTED DAC REGISTER | STATE OF SELECTED DAC REGISTER |
|------------------|----|-------------------------------|-------|-----------------------|--------------------------------|
| L <sup>(1)</sup> | L  | L                             | H     | A                     | Transparent                    |
| L                | H  | L                             | H     | B                     | Transparent                    |
| H                | L  | L                             | H     | C                     | Transparent                    |
| H                | H  | L                             | H     | D                     | Transparent                    |
| X <sup>(2)</sup> | X  | H                             | H     | NONE                  | (All Latched)                  |
| X                | X  | X                             | L     | ALL                   | Reset <sup>(3)</sup>           |

NOTES: (1) L = Logic LOW. (2) X = Don't Care. (3) Resets to either 000H or 800H, per the RESETSEL state (LOW = 000H, HIGH = 800H). When RESET rises, all registers that are in their latched state retain the reset value.

TABLE II. Control Logic Truth Table.

| $\overline{\text{CS}}$ <sup>(1)</sup> | CLK <sup>(1)</sup>        | LOADDAC $\overline{\text{S}}$ | RESET            | SERIAL SHIFT REGISTER |
|---------------------------------------|---------------------------|-------------------------------|------------------|-----------------------|
| H <sup>(2)</sup>                      | X <sup>(3)</sup>          | H                             | H                | No Change             |
| L <sup>(4)</sup>                      | L                         | H                             | H                | No Change             |
| L                                     | $\uparrow$ <sup>(5)</sup> | H                             | H                | Advanced One Bit      |
| $\uparrow$                            | L                         | H                             | H                | Advanced One Bit      |
| H <sup>(6)</sup>                      | X                         | L <sup>(7)</sup>              | H                | No Change             |
| H <sup>(6)</sup>                      | X                         | H                             | L <sup>(8)</sup> | No Change             |

NOTES: (1)  $\overline{\text{CS}}$  and CLK are interchangeable. (2) H = Logic HIGH. (3) X = Don't Care. (4) L = Logic LOW (5) = Positive Logic Transition. (6) A HIGH value is suggested in order to avoid a "false clock" from advancing the shift register and changing the shift register. (7) If data is clocked into the serial register while LOADDAC $\overline{\text{S}}$  is LOW, the selected DAC register will change as the shift register bits "flow" through A1 and A0. This will corrupt the data in each DAC register that has been erroneously selected. (8) RESET LOW causes no change in the contents of the serial shift register.

TABLE III. Serial Shift Register Truth Table.

Note that  $\overline{\text{CS}}$  and CLK are combined with an OR gate and the output controls the serial-to-parallel shift register internal to the DAC7614 (see the block diagram on the front of this data sheet). These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when  $\overline{\text{CS}}$  rises at the end of a serial transfer. If CLK is LOW when  $\overline{\text{CS}}$  rises, the OR gate will provide a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong DAC.

If both  $\overline{\text{CS}}$  and CLK are used, then  $\overline{\text{CS}}$  should rise only when CLK is HIGH. If not, then either  $\overline{\text{CS}}$  or CLK can be used to operate the shift register. See Table III for more information.

## Digital Input Coding

The DAC7614 input data is in Straight Binary format. The output voltage is given by the following equation:

$$V_{\text{OUT}} = V_{\text{REFL}} + \frac{(V_{\text{REFH}} - V_{\text{REFL}}) \cdot N}{4096}$$

where N is the digital input code (in decimal). This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

## LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. As the DAC7614 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to achieve good performance from the converter.

Because the DAC7614 has a single ground pin, all return currents, including digital and analog return currents, must flow through the GND pin. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system (see Figure 4).

The power applied to  $V_{DD}$  (as well as  $V_{SS}$ , if not grounded) should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection,  $V_{DD}$  should be connected to a +5V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the  $1\mu\text{F}$  to  $10\mu\text{F}$  and  $0.1\mu\text{F}$  capacitors shown in Figure 4 are strongly recommended. In some situations, additional bypassing may be required, such as a  $100\mu\text{F}$  electrolytic capacitor or even a “Pi” filter made up of inductors and capacitors—all designed to essentially lowpass filter the +5V supply, removing the high frequency noise (see Figure 4).

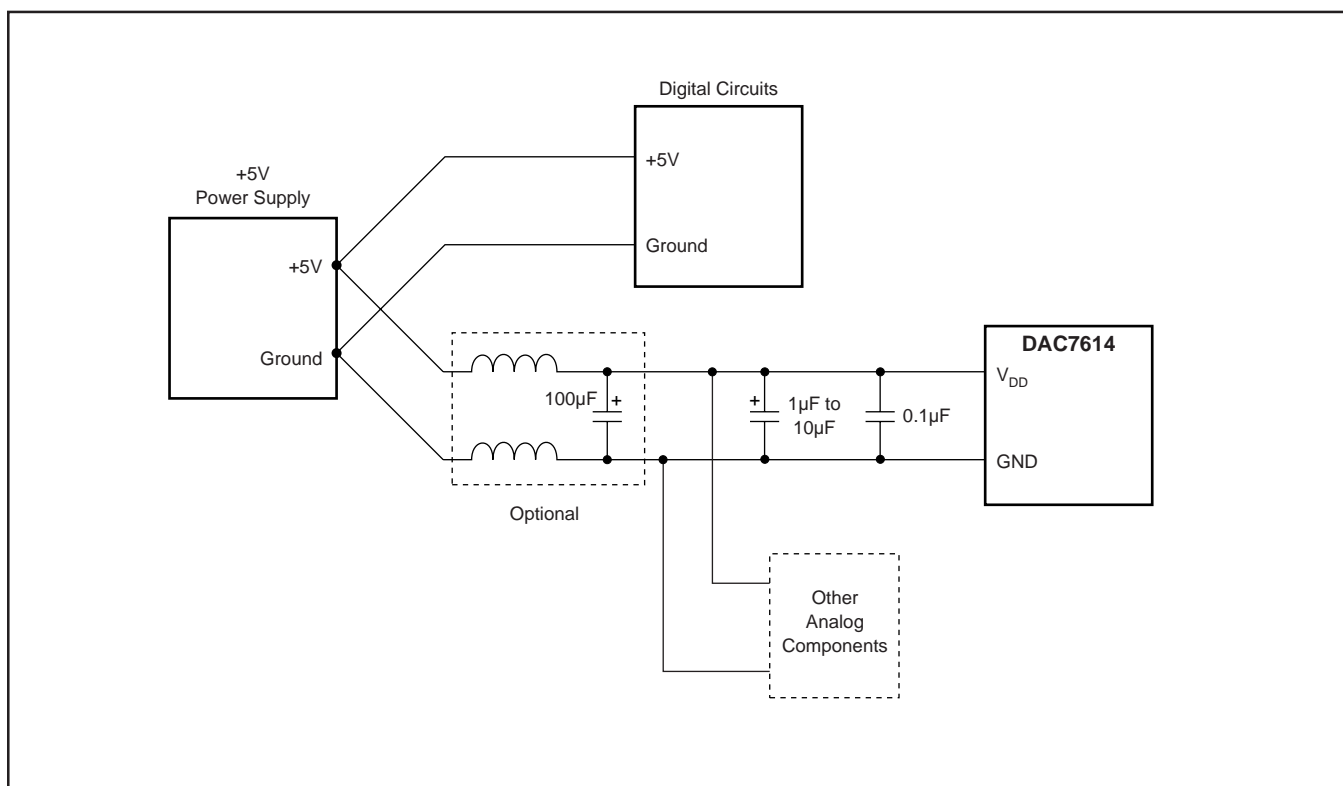


FIGURE 4. Suggested Power and Ground Connections for a DAC7614 Sharing a +5V Supply with a Digital System.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| DAC7614E         | ACTIVE                | SSOP         | DB              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614E/1K      | ACTIVE                | SSOP         | DB              | 20   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614E/1KG4    | ACTIVE                | SSOP         | DB              | 20   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614EB        | ACTIVE                | SSOP         | DB              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614EB/1K     | ACTIVE                | SSOP         | DB              | 20   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614EB/1KG4   | ACTIVE                | SSOP         | DB              | 20   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614EBG4      | ACTIVE                | SSOP         | DB              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614EG4       | ACTIVE                | SSOP         | DB              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614P         | NRND                  | PDIP         | N               | 16   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | N / A for Pkg Type           |
| DAC7614PB        | NRND                  | PDIP         | N               | 16   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | N / A for Pkg Type           |
| DAC7614PBG4      | NRND                  | PDIP         | N               | 16   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | N / A for Pkg Type           |
| DAC7614PG4       | NRND                  | PDIP         | N               | 16   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | N / A for Pkg Type           |
| DAC7614U         | ACTIVE                | SOIC         | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614U/1K      | ACTIVE                | SOIC         | DW              | 16   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614U/1KG4    | ACTIVE                | SOIC         | DW              | 16   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614UB        | ACTIVE                | SOIC         | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614UB/1K     | ACTIVE                | SOIC         | DW              | 16   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614UB/1KG4   | ACTIVE                | SOIC         | DW              | 16   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614UBG4      | ACTIVE                | SOIC         | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7614UG4       | ACTIVE                | SOIC         | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |

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**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DAC7614E/1K  | SSOP         | DB              | 20   | 1000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| DAC7614EB/1K | SSOP         | DB              | 20   | 1000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| DAC7614U/1K  | SOIC         | DW              | 16   | 1000 | 330.0              | 16.4               | 10.85   | 10.8    | 2.7     | 12.0    | 16.0   | Q1            |
| DAC7614UB/1K | SOIC         | DW              | 16   | 1000 | 330.0              | 16.4               | 10.85   | 10.8    | 2.7     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DAC7614E/1K  | SSOP         | DB              | 20   | 1000 | 346.0       | 346.0      | 33.0        |
| DAC7614EB/1K | SSOP         | DB              | 20   | 1000 | 346.0       | 346.0      | 33.0        |
| DAC7614U/1K  | SOIC         | DW              | 16   | 1000 | 346.0       | 346.0      | 33.0        |
| DAC7614UB/1K | SOIC         | DW              | 16   | 1000 | 346.0       | 346.0      | 33.0        |



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- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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