Freescale Semiconductor
Technical Data

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MC1323x

Package Information
Case 2124-02
LGA-48 [7x7 mm]

Ordering Information

Device	Device Marking	Package
MC13233C[1]	MC13233C	LGA-48

[1] See Table 1 for more details

MC1323x

Low Cost SoC Remote Control Platform for the 2.4 GHz IEEE® 802.15.4 Standard

1 Introduction

The MC1323x family is Freescale's low cost System-on-Chip (SoC) platform for the IEEE® 802.15.4 Standard that incorporates a complete, low power, 2.4 GHz radio frequency transceiver with Tx/Rx switch, an 8-bit HCS08 CPU, and a functional set of MCU peripherals into a 48-pin LGA package. This family of products is targeted for wireless RF remote control and other cost-sensitive applications ranging from home TV and entertainment systems such as ZigBee BeeStack Consumer (RF4CE) to low cost, low power, IEEE 802.15.4 and ZigBee end nodes. The MC1323x is a highly integrated solution, with very low power consumption.

The MC1323x contains an RF transceiver which is an 802.15.4 Standard - 2006 compliant radio that operates in the 2.4 GHz ISM frequency band. The transceiver includes a low noise amplifier, 1mW nominal output power amplifier (PA), internal voltage controlled oscillator (VCO), integrated transmit/receive switch, on-board power supply regulation, and full spread-spectrum encoding and decoding.

Contents

1 Introduction 1
2 Features 2
3 Integrated IEEE 802.15.4 Transceiver (Radio and Modem) 7
4 HCS08 8-Bit Central Processing Unit (CPU) 9
5 System Clocks 10
6 Memory 10
7 System and Power Management 11
8 MCU Peripherals 12
9 Development Environment 16
10 Pin Assignment and Connections 17
11 Electrical Specifications 20
12 Applications Information 32
13 Mechanical Diagrams (Case 2124-02, Non-JEDEC) 34

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The on-chip CPU is based on the Freescale HCS08 family of Microcontroller Units (MCU) and has 82 kilobyte (KB) of FLASH memory and 5KB of RAM. The onboard MCU peripheral set has been defined to support the targeted applications. A dedicated DMA block transfers packet data between RAM and the transceiver to off-load the CPU and allow higher efficiency and increased performance.

1.1 Ordering Information

Table 1 provides additional details about the MC1323x

Table 1. Orderable Parts Details

Device	Operating Temp Range (TA.)	Package	Memory Options	Description
MC13233C	-40° to 85° C	LGA-48	5KB RAM, 82KB Flash	Intended for smaller memory footprint applications.
MC13233CR2	-40° to 85° C	LGA-48 Tape and Reel	5KB RAM, 82KB Flash	Intended for smaller memory footprint applications.

2 Features

This section provides a simplified block diagram and highlights MC1323x features.

2.1 Block Diagram

Figure 1 shows a simplified block diagram of the MC1323x.

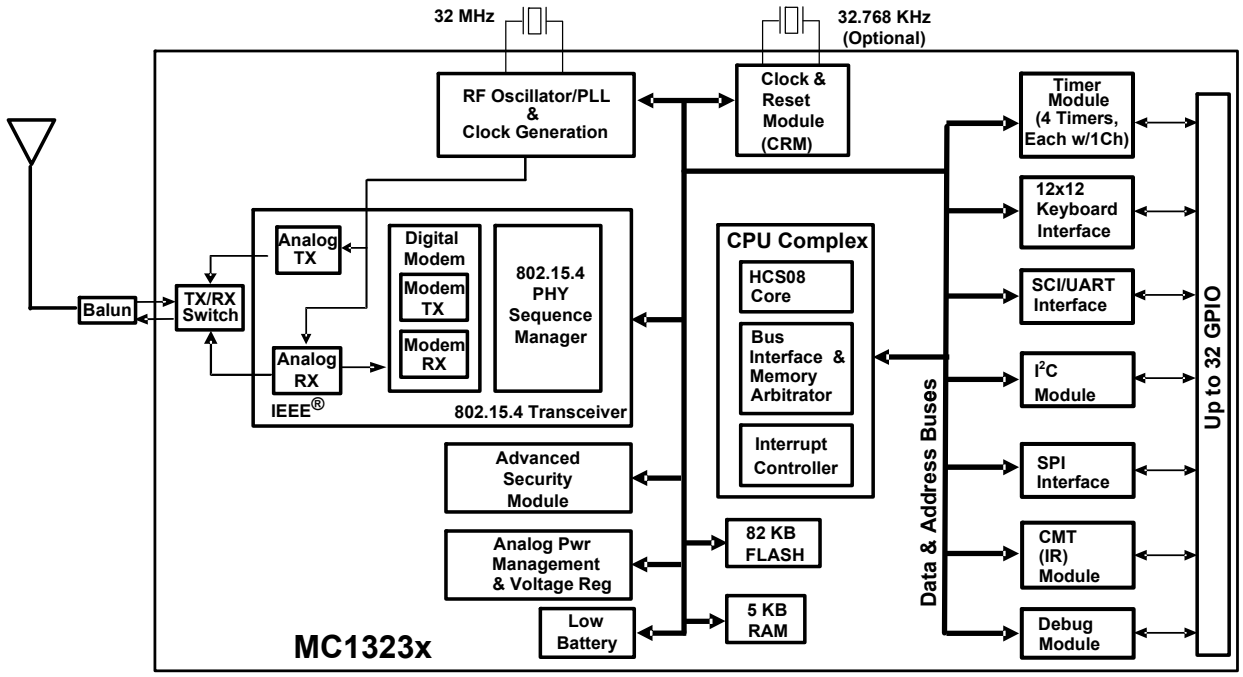

Figure 1. MC1323x Simplified Block Diagram

2.2 Features Summary

- Fully compliant IEEE 802.15.4 Standard 2006 transceiver supports 250 kbps O-QPSK data in 5.0 MHz channels and full spread-spectrum encode and decode
  - 2.4GHz
  - Operates on one of 16 selectable channels per IEEE 802.15.4
  - Programmable output power with 0 dBm nominal output power, programmable from -30 dBm to +2 dBm typical
  - Receive sensitivity of -94 dBm (typical) at 1% PER, 20-byte packet, much better than the IEEE 802.15.4 Standard of -85 dBm
  - Partial Power Down (PPD) “listen” mode available to reduce current while in receive mode and waiting for an incoming frame
- Small RF footprint
  - Integrated transmit/receive switch
  - Differential input/output port (typically used with a balun)
  - Low external component count
- Hardware acceleration for IEEE® 802.15.4 applications
  - DMA interface
  - AES-128 Security module
  - 16-Bit random number generator
  - 802.15.4 Auto-sequence support
  - 802.15.4 Receiver Frame filtering
- 32 MHz crystal reference oscillator; onboard load trim capability supplements external load capacitors
- Onboard 1 kHz oscillator for wake-up timing or an optional 32.768 kHz crystal for accurate low power timing
- Transceiver Event Timer module has 4 timer comparators available to help manage the auto-sequencer and to supplement MCU TPM resources
- HCS08 8-bit, 32 MHz CPU
- 82 KB (81920_{dec}) FLASH memory
  - 81920_{dec} Bytes organized as 80 segments by 1024 bytes
  - Programmable over the full power supply range of 1.8 - 3.6 V
  - Automated program and erase algorithms
  - Flexible protection scheme to prevent accidental program or erase
  - Security feature to prevent unauthorized access to the FLASH
- 5 KB RAM
- Powerful In-circuit debug and FLASH programming available via on-chip module (BDM)
  - Two comparator and 9 trigger modes
  - Eight deep FIFO for storing change-of-flow addresses and event-only data

  - Tag and force breakpoints
  - In-circuit debugging with single breakpoint
- Multiple low power modes (less than 1 μA in STOP3)
- Keyboard interrupt (KBI) modules
  - Two Keyboard control modules capable of supporting up to a 12x12 keyboard matrix
  - 12 Dedicated KBI pins support a 6x6 matrix without impacting other IO resources
  - 12 KBI interrupts with selectable polarity
- Serial communication interface (SCI)
  - Full duplex non-return to zero (NRZ)
  - Baud rates as high as 1 Mbps can be supported
  - LIN master extended break generation
  - LIN slave extended break detection
  - Wake-up on active edge
- Serial peripheral interface (SPI)
  - Full-duplex or single-wire bidirectional
  - Double-buffered transmit and receive
  - Master or Slave mode; MSB-first or LSB-first shifting
- Inter-integrated circuit (IIC) interface -
  - Up to 100 kbps baud rate with maximum bus loading
  - Baud rates as high as 800 kbps can be programmed
  - Multi-master operation
  - Programmable slave address
  - Interrupt driven byte-by-byte data transfer;
  - Supports broadcast mode and 10-bit addressing
- Four 16-bit timer/pulse width modulators (TPM[4:1]) - each TPM module has an assigned GPIO pin and provides
  - Single channel capability
  - Input capture
  - Output compare
  - Buffered edge-aligned or center-aligned PWM
- Carrier Modulator Timer (CMT) - IR Remote carrier generator, modulator, and transmitter.
- Real-time counter (RTC)
  - 16-bit modulus counter with binary or decimal based prescaler;
  - External clock source for precise time base, time-of-day, calendar or task scheduling functions
  - Capable of greater than one day interrupt.
- System protection features
  - Programmable low voltage warning and interrupt (LVI)

  - Optional watchdog timer (COP)
  - Illegal opcode detection
- 1.8V to 3.6V operating voltage with on-chip voltage regulators.
- Up to 32 GPIO
  - Hysteresis and selectable pull-up resistors on all input pins
  - Configurable slew rate and drive strength on all output pins.
- -40°C to +85°C temperature range
- RoHS-compliant 7x7 mm 48-pin LGA package

2.3 Software Solutions

Freescale provides a powerful software environment called the Freescale BeeKit Wireless Connectivity Toolkit. BeeKit is a comprehensive codebase of wireless networking libraries, application templates, and sample applications. The BeeKit Graphical User Interface (GUI), part of the BeeKit Wireless Connectivity Toolkit, allows users to create, modify, and update various wireless networking implementations. A wide range of software functionality is available to complement the MC1323x and these are provided as codebases within BeeKit. The following sections describe the available tools.

2.3.1 Simple Media Access Controller (SMAC)

The Freescale Simple Media Access Controller (SMAC) is a simple ANSI C based code stack available as sample source code. The SMAC can be used for developing proprietary RF transceiver applications using the MC1323x.

- Supports point-to-point and star network configurations
- Proprietary networks
- Source code and application examples provided

2.3.2 IEEE® 802.15.4 2006 Standard-Compliant MAC

The Freescale 802.15.4 Standard-Compliant MAC is a code stack available as object code. The 802.15.4 MAC can be used for developing MC1323x networking applications based on the full IEEE® 802.15.4 Standard that use custom Network Layer and application software.

- Supports star, mesh and cluster tree topologies
- Supports beaconed networks
- Supports GTS for low latency
- Multiple power saving modes
- AES-128 Security module
- 802.15.4 Sequence support
- 802.15.4 Receiver Frame filtering.

2.3.3 SynkroRF Platform

The SynkroRF Network is a general purpose, proprietary networking layer that sits on top of the IEEE® 802.15.4 MAC and PHY layers. It is designed for Wireless Personal Area Networks (WPANs) and conveys information over short distances among the participants in the network. It enables small, power efficient, inexpensive solutions to be implemented for a wide range of applications. Some key characteristics of an SynkroRF Network are:

- An over-the-air data rate of 250 kbit/s in the 2.4 GHz band.
- 3 independent communication channels in the 2.4 GHz band (15, 20, and 25).
- 2 network node types, controller and controlled nodes.
- Channel Agility mechanism.
- Low Latency Tx mode automatically enabled in conditions of radio interference.
- Fragmented mode transmission and reception, automatically enabled in conditions of radio interference.
- Robustness and ease of use.
- Essential functionality to build and support a CE network.

The SynkroRF Network layer uses components from the standard HC(S)08 Freescale platform, which is also used by the Freescale's implementations of 802.15.4. MAC and ZigBee™ layers. For more details about the platform components, see the *Freescale Platform Reference Manual*.

2.3.4 BeeStack Consumer

Freescale's ZigBee RF4CE stack, called BeeStack Consumer, is a networking layer that sits on top of the IEEE® 802.15.4 MAC and PHY layers. It is designed for standards-based Wireless Personal Area Networks (WPANs) of home entertainment products and conveys information over short distances among the participants in the network. It enables small, power efficient, inexpensive solutions to be implemented for a wide range of applications. Targeted applications include DTV, set top box, A/V receivers, DVD players, security, and other consumer products.

Some key characteristics of a BeeStack Consumer network are:

- An over-the-air data rate of 250 kbit/s in the 2.4 GHz band
- 3 independent communication channels in the 2.4 GHz band
- 2 network node types, controller node and target node
- Channel Agility mechanism
- Provides robustness and ease of use
- Includes essential functionality to build and support a CE network

The BeeStack Consumer layer uses components from the standard HCS08 Freescale platform, which is also used by the Freescale implementations of 802.15.4. MAC or ZigBee™ layers. For more details about the platform components, see the *Freescale Platform Reference Manual*.

2.3.5 ZigBee-Compliant Network Stack

Freescale's BeeStack architecture builds on the ZigBee protocol stack. Based on the OSI Seven-Layer model, the ZigBee stack ensures inter-operability among networked devices. The physical (PHY), media access control (MAC), and network (NWK) layers create the foundation for the application (APL) layers. BeeStack defines additional services to improve the communication between layers of the protocol stack.

At the Application Layer, the application support layer (ASL) facilitates information exchange between the Application Support Sub-Layer (APS) and application objects. Finally, ZigBee Device Objects (ZDO), in addition to other manufacturer-designed applications, allow for a wide range of useful tasks applicable to home and industrial automation.

BeeStack uses the IEEE 802.15.4-compliant MAC/PHY layer that is not part of ZigBee itself. The NWK layer defines routing, network creation and configuration, and device synchronization. The application framework (AF) supports a rich array of services that define ZigBee functionality. ZigBee Device Objects (ZDO) implement application-level services in all nodes via profiles. A security service provider (SSP) is available to the layers that use encryption (NWK and APS), i.e., Advanced Encryption Standard (AES) 128-bit security.

The complete Freescale BeeStack protocol stack includes the following components:

- ZigBee Device Objects (ZDO) and ZigBee Device Profile (ZDP)
- Application Support Sub-Layer (APS)
- Application Framework (AF)
- Network (NWK) Layer
- Security Service Provider (SSP)
- IEEE 802.15.4-compliant MAC and Physical (PHY) Layer

3 Integrated IEEE 802.15.4 Transceiver (Radio and Modem)

The MC1323x IEEE 802.15.4 fully-compliant transceiver provides a complete 2.4 GHz radio with 250 kbps Offset-Quadrature Phase Shift Keying (O-QPSK) data in 5.0 MHz channels and full spread-spectrum encode and decode. The modem supports the full requirement of the IEEE 802.15.4 Standard functionality to transmit, receive, and do clear channel assessment (CCA), Energy Detect (ED), and Link Quality Indication (LQI).

- Programmable output power with 0 dBm nominal output power, programmable from -30 dBm to +2 dBm typical
- Receive sensitivity of -94 dBm (typical) at 1% PER, 20-byte packet
- Differential bi-directional RF input/output port
- Integrated transmit/receive switch
- Receive current can be reduced while waiting or "listening" for an incoming frame using partial power down (PPD) mode

3.1 RF Interface and Usage

The MC1323x RF interface provides a bi-directional, differential port that connects directly to a balun. The balun connects directly to a single-ended antenna and converts that interface to a full differential, bi-directional, on-chip interface with transmit/receive switch, LNA, and complementary PA outputs.This combination allows for a small footprint and low cost RF solution.

3.2 Transceiver Register Interface and Operation

The transceiver is controlled by set of interface registers that are memory-mapped into the CPU address space. The transceiver is capable of independent operation to perform transmit, receive, or perform CCA/ED operations and combinations. Additional features of the transceiver include:

- DMA function moves data directly between RAM and transceiver buffers during transmit and receive on a cycle-steal basis. This off loads the data transfer from the CPU and provides higher performance.
- Interrupt capability dependent on RX packet data availability. An interrupt can be generated based on a programmed count of RX data bytes that have been received and moved to RAM. This allows CPU filtering of RX data before completion of the packet reception to accelerate response to the packet.
- Four transceiver Event Timer comparators are available to supplement MCU peripheral timer resources for PHY and MAC timing requirements.

3.3 IEEE 802.15.4 Acceleration Hardware

The 802.15.4 transceiver has several hardware features that reduce the software stack size, off load the function from the CPU, and improve performance

- Fully supports 2003 & 2006 versions of the IEEE 802.15 Standard.
- Supports slotted and unslotted modes
- Supports beacon enabled and non-beacon enabled networks
- DMA data transfer between RAM and radio
- Separate AES-128 Security module
- 16-bit random number generator
- 802.15.4 Sequence support
  - RX (conditionally followed by TXAck)
  - TX
  - CCA (used for CCA and ED cycles)
  - Tx/Rx (Tx followed by unconditional Rx or RCACK)
  - Continuous CCA
- 802.15.4 Receiver Frame filtering.

3.4 Unique Partial Power Down (PPD) or “Listen” Receive Mode

The MC1323x provides a unique Partial Power Down receive (PPD_RX) mode. When this mode is selected:

- Whenever a receive cycle is initiated, the receiver is not turned fully on to save current until receive energy of a preset level is detected
- The receiver will turn fully on only when triggered by energy at the preset level, and then receives the expected frame. The full-on state is the same as the standard receive state
- The preset level can be programmed for various RX input power levels

Use of the PPD_RX mode provides two distinct advantages:

1. Reduced “listen” mode current - The receive current is significantly reduced while waiting for a frame. If a node is a coordinator, router, or gateway and it spends a significant percentage of its RF-active time waiting for incoming frames from clients or other devices, the net power savings can be significant.
2. Reduced sensitivity as a desired effect - The PPD_RX mode provides different levels of reduced sensitivity. If a node operates in a densely populated area, it may be desirable to de-sensitize the receiver such that the device does not respond to incoming frames with an energy level below the desired threshold. This could be useful for security, net efficiency, reduced noise triggering and many other purposes.

4 HCS08 8-Bit Central Processing Unit (CPU)

The onboard CPU is a 32 MHz 8-bit HCS08 core. It executes a super set of the 68HC08 instruction set with added BGND instructions. The HCS08 CPU is fully source and object code compatible with the M68HC08 CPU. Several instructions and enhanced addressing modes are added to improve C compiler efficiency and to support a new background debug system. It has an 8-bit data bus, a 16-bit address bus and a 2-stage instruction pipe that facilitates the overlapping of instruction fetching and execution. There are 29 vectors for internal interrupt sources and one vector for an external interrupt pin. The debug or BDM module provides a serial one-wire interface for non-intrusive debugging of application programs.

Features of the HCS08 CPU include:

- Object code fully upward-compatible with M68HC05 and M68HC08 Families
- 64-KB CPU address space with banked memory management unit for greater than 64 KB
- 16-bit stack pointer (any size stack anywhere in 64-KB CPU address space)
- 16-bit index register (H:X) with powerful indexed addressing modes
- 8-bit accumulator (A)
- Many instructions treat X as a second general-purpose 8-bit register
- Seven addressing modes:
  - — Inherent — Operands in internal registers
  - — Relative — 8-bit signed offset to branch destination
  - — Immediate — Operand in next object code byte(s)

— Direct — Operand in memory at 0x0000–0x00FF
— Extended — Operand anywhere in 64-KB address space
— Indexed relative to H:X — Five submodes including auto increment
— Indexed relative to SP — Improves C efficiency dramatically

- Memory-to-memory data move instructions with four address mode combinations
- Overflow, half-carry, negative, zero, and carry condition codes support conditional branching on the results of signed, unsigned, and binary-coded decimal (BCD) operations
- Efficient bit manipulation instructions
- Fast 8-bit by 8-bit multiply and 16-bit by 8-bit divide instructions
- STOP and WAIT instructions to invoke low-power operating modes

5 System Clocks

The primary system reference frequency is a 32 MHz crystal oscillator. The crystal requirements for the oscillator and oscillator performance must support a +/-40 ppm frequency accuracy to meet the IEEE 802.15.4 Standard requirements. All system clocks are generated from this source. Features of the clock system include:

- The 32 MHz reference oscillator has onboard programmable capacitive loading that allows software tuning of frequency accuracy
- CPU clock as high as 32 MHz
- Bus clock (and peripheral clock) equals 1/2 CPU clock
- Clocks to individual peripherals can be independently disabled for best power management.
- CPU clock can be lowered to 500 kHz for lower power (250 kHz bus clock)

An optional 32.768 kHz crystal oscillator is available for accurate low power timing and the Real Time Clock (RTC). Also, an onboard, low accuracy 1 kHz oscillator is available for sleep timing wake-up.

6 Memory

The MC1323x memory resources consist of RAM, FLASH program memory for nonvolatile data storage, and control/status registers for I/O, peripherals, management, and the transceiver. Features include:

- 80 KB FLASH (81920_{dec}) bytes organized as 80 segments of 1024 byte/segment)
- 5 KB RAM
- Security circuitry to prevent unauthorized access to RAM and FLASH contents

7 System and Power Management

The MC1323x is inherently a low power device, but it also has extensive system control and power management to maximize battery life and provide system protection.

7.1 Modes of Operation

The MC1323x modes of operation include:

- Active background mode for code development
- Run mode — CPU clocks can be run at full speed and the internal supply is fully regulated.
- LPRun mode — CPU clock is set to 500 kHz and peripheral clocks (bus clock) to 250 kHz and the internal voltage regulator is in standby
- Wait mode — CPU shuts down to conserve power; system clocks are running and full regulation is maintained
- LPWait mode — CPU shuts down to conserve power; peripheral clocks are restricted to 250 kHz and the internal voltage regulator is in standby
- STOP modes — System clocks are stopped and voltage regulator is in standby
  - STOP3 — All internal circuits are powered for fast recovery (32 MHz oscillator on-off optional)
  - STOP2 — Partial power down of internal circuits, RAM content is retained; I/O states are held

7.2 Power Management

The MC1323x power management is controlled through programming of the modes of operation. Different modes allow for different levels of power-down. Additional features include:

- The transceiver is powered as required
- The analog radio is only powered-up as required to do a TX, RX, or CCA/ED operation
- Peripheral control clock gating can be disabled on an MCU module-by-module basis to provide lowest power
- Programmed mode manages
  - Degree of chip power down
  - Retention of programmed parameters
  - Clock management
- Power-down and wake-up (clocks and analog blocks) are gracefully controlled
- RTC can be used as wake-up timer
- Wake-up available through KBI and UART Rx asynchronous interrupts
- Real-time counter (RTC) module
  - 16-bit modulus counter with binary or decimal based prescaler for precise time base, time-of-day, calendar or task scheduling functions.
  - Capable of greater than one day interrupt.
  - Can also be used for device wake-up.

7.3 System Protection

The MC1323x provides several vehicles to maintain security or a high level of system robustness:

- Watchdog computer operating properly (COP) reset with option to run from dedicated internal clock source or bus clock
- Low-voltage warning and detection with reset or interrupt; selectable trip points
- Illegal opcode detection with reset
- FLASH block protection

8 MCU Peripherals

The MC1323x has a functional set of MCU peripherals focused for intended applications.

8.1 Parallel Input/Output (GPIO)

The MC1323x has four I/O ports that provide up to 31 general-purpose I/O signals and 1 output only signal. Many of these pins are shared with on-chip peripherals such as timer systems, communication ports, or keyboard interrupts. When these other modules are not controlling the port pins, they revert to general-purpose I/O control. For each I/O pin, a port data bit provides access to input (read) and output (write) data, a data direction bit controls the direction of the pin, and a pullup enable bit enables an internal pullup device (provided the pin is configured as an input), and a slew rate control bit controls the rise and fall times of the pins.Parallel I/O features include

Parallel I/O features include:

- A total of 32 general-purpose I/O pins in four ports (PTA2 is output only)
- Hysteresis input buffers
- Software-controlled pull-ups on each input pin
- Software-controlled slew rate output buffers
- Eight port A pins shared with 32.768 kHz oscillator, IRQ, IIC, and BKGD
- Eight port B pins shared with KBI1[7:0]
- Eight port C pins shared with KBI2[3:0] and SPI
- Eight port D pins shared with TPM0, TPM1, TPM2, TPM3, CMT (with 20mA drive), UART, and 32MOUT (reference frequency clock output)

8.2 Keyboard Interrupt Modules (KBI)

The MC1323x has two KBI modules; KBI1 shares eight Port A pins and KBI2 shares the lower four pins of Port C. Any KBI pin can be enabled as a keyboard input that can act as an interrupt request. As a result, the total 12 KBI inputs allows as large as a 12x12 keyboard matrix with use of other GPIO pins as outputs to the matrix.

All enabled KBI inputs can be configured for edge-only sensitivity or edge-and-level sensitivity. They also can be configured for either rising edge / high-level or falling-edge/low-level sensitivity. When enabled

for rising edge / high level sensitivity, a pulldown resistor is enabled, and when enabled for falling edge / low level sensitivity, a pull-up resistor is enabled.

The KBI features include:

- KBI1 has eight keyboard interrupt pins with individual pin enable bits.
- KBI2 has four keyboard interrupt pins with individual pin enable bits.
- Supports up to a 12x12 keyboard matrix. A 6x6 matrix can be supported without impacting other I/O functions.
- Each keyboard interrupt pin is programmable as falling edge (or rising edge) only, or both falling edge and low level (or both rising edge and high level) interrupt sensitivity. Pull-ups and pull-downs enabled by selected mode.
- Individual signal software enabled interrupts for both KBI1 and KBI2.
- Can be used for device wake-up

8.3 Serial Communications Interface (SCI) Module

The MC1323x has one serial communications interface module — sometimes called a universal asynchronous receiver/transmitter (UART). Typically, this port is used to connect to the RS232 serial input/output (I/O) port of a personal computer or workstation, and it can also be used to communicate with other embedded controllers.

The SCI module has a single, flexible frac-N (13-bit modulo counter, 5-bit fractional counter) baud rate generator used both for transmit and receive. With a maximum 16 MHz peripheral clock, baud rates as high as 1 Mbps can be supported (standard is 921,600 baud).

This SCI system offers many advanced features not commonly found on other asynchronous serial I/O peripherals on other embedded controllers. The receiver employs an advanced data sampling technique that ensures reliable communication and noise detection. Hardware parity, receiver wake-up, and double buffering on transmit and receive are also included.

Features of SCI module include:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Double-buffered transmitter and receiver with separate enables
- Programmable high accuracy baud rates (frac-N generator)
- Interrupt-driven or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
- Hardware parity generation and checking
- Programmable 8-bit or 9-bit character length

- Receiver wake-up by idle-line or address-mark
- Optional 13-bit break character generation / 11-bit break character detection
- Selectable transmitter output polarity

8.4 Serial Peripheral Interface (SPI) Module

The MC1323x has one serial peripheral interface module. The SPI is a synchronous serial data input/output port used for interfacing with serial memories, peripheral devices, or other processors. The SPI allows an 8-bit serial bit stream to be shifted simultaneously into and out of the device at a programmed bit-transfer rate (called 4-wire mode). There are four pins associated with the SPI port (SPCLK, MOSI, MISO, and SS).

The SPI module can be programmed for master or slave operation. It also supports a 3-wire mode where for master mode the MOSI becomes MOMI, a bidirectional data pin, and for slave mode the MISO becomes SISO, a bidirectional data pin. In 3-wire mode, data is only transferred in one direction at a time.

The SPI bit clock is derived from the peripheral input clock with a maximum 16 MHz operation. A programmable prescaler (maximum divide-by-8) drives a second baud rate programmable divider (maximum divide-by-256) to develop the bit clock. The maximum SPI transfer rate is 8 MHz.

Features of SPI module include:

- Master or slave mode operation
- Full-duplex or single-wire bidirectional option
- 8-Bit only transfer size
- Programmable transmit bit rate (8 MHz max)
- Double-buffered transmit and receive
- Serial clock phase and polarity options (supports all 4 options)
- Optional slave select output
- Selectable MSB-first or LSB-first shifting

8.5 Inter-integrated Circuit (IIC) Interface Module

The MC1323x has one inter-integrated circuit interface module that provides a method of communication between a number of other integrated circuits. The IIC Bus interface provides a bidirectional, 2-pin (SDA bus data and SCL bus clock) serial bus designed to operate up to 100 kbps with maximum bus loading and timing. The module is capable of operating at higher baud rates, up to a maximum of peripheral clock/20 (800 kbps), with reduced bus loading.

Features of IIC module include:

- Compatible with IIC bus standard
- Multi-master operation
- Software programmable clock frequencies
- Software selectable acknowledge bit
- Interrupt driven byte-by-byte data transfer

- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus busy detection
- General call recognition
- 10-bit address extension

8.6 Timer/PWM (TPM) Modules

The MC1323x has four independent timer/PWM modules, each with one channel. Each TPM module is based on a 16-bit counter and provides input capture, output compare, and pulse width modulation. Each TPM module has one associated I/O pin for input capture or counter/PWM output.

TPM module features include:

- Each TPM may be configured for buffered, center-aligned pulse-width modulation (CPWM) on all channels
- Module clock source is peripheral clock or reference oscillator divided-by-1024
- Clock prescaler taps for divide by 1, 2, 4, 8, 16, 32, 64, or 128
- 16-bit free-running or up/down (CPWM) count operation
- 16-bit modulus register to control counter range
- Module enable
- One interrupt per channel plus a terminal count interrupt for each TPM module
- Channel features:
  - Each channel may be input capture, output compare, or buffered edge-aligned PWM
  - Rising-edge, falling-edge, or any-edge input capture trigger
  - Set, clear, or toggle output compare action
  - Selectable polarity on PWM outputs

8.7 Carrier Modulator Timer (CMT) Module

The MC1323x carrier modulator timer module is intended as an IR LED driver for remote control “blaster” applications. The module consists of a carrier generator, modulator, and transmitter that drives data to the output (IRO) pin either in baseband or in FSK mode. The IRO pin drives (modulates) the IR diode directly or through a buffer depending on the required current. The IRO pin is specified for 20mA drive.

The CMT module features include:

- Four modes of operation
  - Time with independent control of high and low times
  - Baseband

- — Frequency shift key (FSK)
- — Direct software control of IRO pin
- Extended space operation in time, baseband, and FSK modes
- Module clock source is peripheral clock (16 MHz max)
- Interrupt on end of cycle
- Ability to disable IRO pin and use as timer interrupt

8.8 Real-time Counter (RTC) Module

The MC1323x real-time counter module consists of one 16-bit counter, one 16-bit comparator, several binary-based and decimal-based prescaler dividers, three clock sources, and one programmable periodic interrupt. This module can be used for time-of-day, calendar or any task scheduling functions. It can also serve as a cyclic wake-up from low power modes (STOP2, STOP3 and WAIT). RTC can be clocked from bus clock, the optional 32.768 kHz oscillator or the onboard 1 kHz low power oscillator.

Features of the RTC module include:

- 16-bit up-counter
  - — 16-bit modulo match limit
  - — Software controllable periodic interrupt on match
- Three software selectable clock sources for input to prescaler with programmable 16 bit prescaler
  - — 32.768 kHz optional crystal oscillator.
  - — 32 MHz reference oscillator
  - — 1 kHz low power RC oscillator
- Useful for time base tick or time-of-day clock
- Can be used for device wake-up; capable of greater than one day time-out period.

9 Development Environment

Development support for the HCS08 on the MC1323x includes the background debug controller (BDC) and the on-chip debug module (DBG). The BDC provides a single-wire (signal BKGD) debug interface to the MCU that provides a convenient interface for programming the on-chip FLASH and other storage. The BDC is also the primary debug interface for development and allows non-intrusive access to memory data and traditional debug features such as CPU register modify, breakpoints, and single instruction trace commands.

Address and data bus signals are not available on external pins. Debug is done through commands fed into the MCU via the single-wire background debug interface. The debug module provides a means to selectively trigger and capture bus information so an external development system can reconstruct what happened inside the MCU on a cycle-by-cycle basis without having external access to the address and data signals. Features include:

- Single-wire background debug interface

- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- On-chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes.
- Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints.

10 Pin Assignment and Connections

10.1 Device Pin Assignment

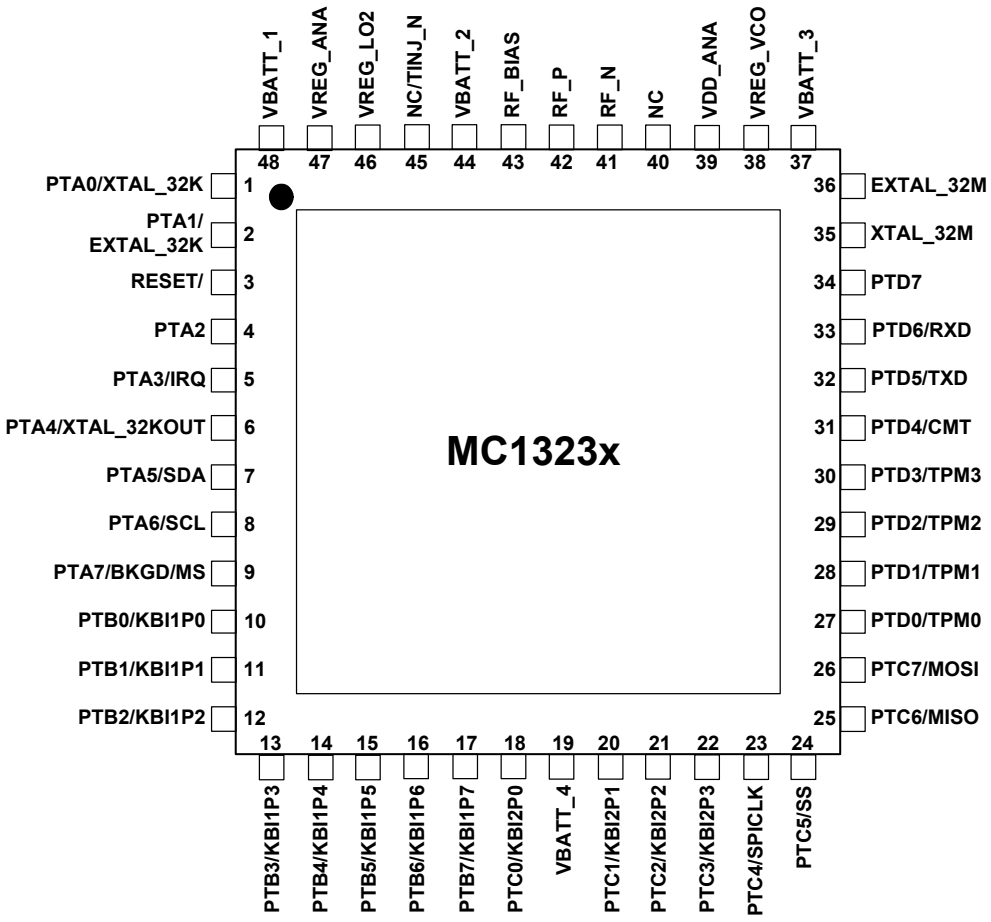

Figure 2. MC1323x Pinout

10.2 Pin Definitions

Table 2 details the MC1323x pinout and functionality.

Table 2. Pin Function Description

Pin #	Pin Name	Type	Description	Functionality
1	PTA0/XTAL_32K	Digital Input/Output	Port A Bit 2 / 32.768 kHz oscillator output	
2	PTA1/EXTAL_32K	Digital Input/Output	Port A Bit 3 / 32.768 kHz oscillator input	For normal use, 10Kohm resistor to ground recommended
3	$\overline{\text{RESET}}$	Digital Input/Output	Device asynchronous hardware reset. Active low. Onboard Pullup	Normally input; gets driven low for a period after a reset
4	PTA2	Digital Output	Port A Bit 2 / Test Mode enable.	TM mode input. MUST BE BIASED LOW EXITING POR FOR NORMAL OPERATION
5	PTA3/IRQ	Digital Input/Output	Port A Bit 3 / IRQ.	
6	PTA4/ XTAL_32KOUT	Digital Input/Output	Port A Bit 4 / Buffered 32.768 kHz clock output	Optional 32.768 kHz output clock for measuring 32 kHz oscillator accuracy (ppm)
7	PTA5/SDA	Digital Input/Output	Port A Bit 5 / IIC Bus data	Defaults to open drain for IIC
8	PTA6/SCL	Digital Input/Output	Port A Bit 6 / IIC Bus clock	Defaults to open drain for IIC
9	PTA7/BKGD/MS	Digital Input/Output	Port A Bit 7 / Background / Mode Select	Debug Port signal
10	PTB0/KBI1P0	Digital Input/Output	Port B Bit 0 / KBI1 Input Bit 0	Wake-up capability
11	PTB1/KBI1P1	Digital Input/Output	Port B Bit 1 / KBI1 Input Bit 1	Wake-up capability
12	PTB2/KBI1P2	Digital Input/Output	Port B Bit 2 / KBI1 Input Bit 2	Wake-up capability
13	PTB3/KBI1P3	Digital Input/Output	Port B Bit 3 / KBI1 Input Bit 3	Wake-up capability
14	PTB4/KBI1P4	Digital Input/Output	Port B Bit 4 / KBI1 Input Bit 4	Wake-up capability
15	PTB5/KBI1P5	Digital Input/Output	Port B Bit 5 / KBI1 Input Bit 5	Wake-up capability
16	PTB6/KBI1P6	Digital Input/Output	Port B Bit 6 / KBI1 Input Bit 6	Wake-up capability
17	PTB7/KBI1P7	Digital Input/Output	Port B Bit 7 / KBI1 Input Bit 7	Wake-up capability
18	PTC0/KBI2P0	Digital Input/Output	Port C Bit 0 / KBI2 Input Bit 0	Wake-up capability
19	VBATT_4	Power Input	VDD supply input [1]	Connect to system VDD supply
20	PTC1/KBI2P1	Digital Input/Output	Port C Bit 1 / KBI2 Input Bit 1	Wake-up capability
21	PTC2/KBI2P2	Digital Input/Output	Port C Bit 2 / KBI2 Input Bit 2	Wake-up capability
22	PTC3/KBI2P3	Digital Input/Output	Port C Bit 3 / KBI2 Input Bit 3	Wake-up capability
23	PTC4/SPICLK	Digital Input/Output	Port C Bit 4 / SPI clock	
24	PTC5/SS	Digital Input/Output	Port C Bit 5 / SPI slave select	
25	PTC6/MISO	Digital Input/Output	Port C Bit 6 / SPI MISO	
26	PTC7/MOSI	Digital Input/Output	Port C Bit 7 / SPI MOSI	

Table 2. Pin Function Description (continued)

Pin #	Pin Name	Type	Description	Functionality
27	PTD0/TPM0	Digital Input/Output	Port D Bit 0 / TPM0 signal	TPM1 timer output / gate input signal
28	PTD1/TPM1	Digital Input/Output	Port D Bit 1/ TPM1 signal	TPM2 timer output / gate input signal
29	PTD2/TPM2	Digital Input/Output	Port D Bit 2 / TPM2 signal	TPM3 timer output / gate input signal
30	PTD3/TPM3	Digital Input/Output	Port D Bit 3 / TPM3 signal	TPM4 timer output / gate input signal
31	PTD4/CMT	Digital Input/Output	Port D Bit 4/ CMT output	Hi drive output for IR diode
32	PTD5/TXD	Digital Input/Output	Port D Bit 5 / UART TXD output	UART has no hardware flow control
33	PTD6/RXD	Digital Input/Output	Port D Bit 6 / UART RXD input	UART has no hardware flow control
34	PTD7	Digital Input/Output	Port D Bit 7	
35	XTAL_32M	Analog Output	32 MHz reference oscillator output	
36	EXTAL_32M	Analog input	32 MHz reference oscillator input	
37	VBATT_3	Power Input	VDD supply input[1]	Connect to system VDD supply
38	VREG_VCO	VCO Reg Out / in	VCO regulator output and input to VCO 1.8 Vdc VDD	Bypass to ground with 220 nF capacitor.
39	VDD_ANA	Analog Power Input	Analog 1.8 Vdc Input	Connect to VREG_ANA
40	NC		No connection to device	May be left open or connect to ground
41	RF_N	RF Input/Output	Modem RF input/output negative	Bi-directional RF port for the internal LNA and PA
42	RF_P	RF Input/Output	Modem RF input/output negative	Bi-directional RF port for the internal LNA and PA
43	RF_BIAS	RF Voltage Output	Switched RF bias voltage (1.8 Vdc)	High for TX; low for RX
44	VBATT_2	Power Input	VDD supply input[1]	Connect to system VDD supply
45	NC/TINJ_N	Input	Reserved; analog test input	May be left open or connect to ground
46	VREG_LO2	LO2 Reg Out	LO2 regulator output @ 1.8 Vdc	Bypass to ground with 220 nF capacitor.
47	VREG_ANA	ANA Reg Out	Analog regulator output @ 1.8 Vdc	Bypass to ground with 220 nF capacitor. Connect to VDD_ANA
48	VBATT_1	Power Input	VDD supply to Analog regulator[1]	Connect to system VDD supply
Flag	GND	Power Input	System ground	

[1] VBATT_1, VBATT_2, VBATT_3 and VBATT_4 signals are not connected onboard MC1323x.

11 Electrical Specifications

This section details maximum ratings for the 48-pin LGA package, recommended operating conditions, DC characteristics, and AC characteristics.

11.1 Package Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum rating is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{BATT}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3 shows the maximum ratings for the 48-Pin LGA package.

Table 3. LGA Package Maximum Ratings

Rating	Symbol	Value	Unit
Maximum Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	125	°C
Moisture Sensitivity Level		MSL3-260	
Reflow Soldering Temperature		260	°C
Power Supply Voltage	V_{BATT}	-0.3 to 3.7	Vdc
Digital Input Voltage	Vin	-0.3 to (V_{DD} + 0.3)	Vdc
RF Input Power	P_{max}	10	dBm

Note: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.

Note: All pins meets ESD Human Body Model (HBM) = 2 kV

11.2 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with the JESD22 Stress Test Qualification for Commercial Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

All latchup test testing is in conformity with the JESD78 IC Latch-Up Test.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification.

Table 4. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin[1]	—	1	
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin[1]	—	1	
Latch-up	Minimum input voltage limit		– 1.8	V
	Maximum input voltage limit		4.32	V

[1] This number represents a minimum number for both positive pulse(s) and negative pulse(s)

Table 5. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	± 2000	—	V
2	Machine model (MM)	V_{MM}	± 200	—	V
3	Charge device model (CDM)	V_{CDM}	± 750	—	V
4	Latch-up current at T_A = 85°C	I_{LAT}	± 100	—	mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

11.3 Recommended Operating Conditions

NOTE

The MC13233 transceiver provides an IEEE® 802.15.4 Standard PHY compliant node over all recommended operating conditions.

Table 6. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (V_{BATT})	V_{BATT}	1.8[1]	2.7	3.6	Vdc
Input Frequency	f_{in}	2.405	-	2.480	GHz
Operating Temperature Range	T_A	-40	25	85	°C
Logic Input Voltage Low	V_{IL}	0	-	30% V_{BATT}	V
Logic Input Voltage High	V_{IH}	70% V_{BATT}	-	V_{BATT}	V

Table 6. Recommended Operating Conditions (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Load Current (with specified V_{OLmax} and V_{OHmin}) All standard GPIO CMT output IRO	I_O	- -	- -	3 20	mA
RF Input Power	P_{max}	-	-	10	dBm
Crystal Reference Oscillator Frequency (±40 ppm over operating conditions to meet the 802.15.4 Standard.)	f_{ref}	32 MHz Only			

[1] Although the device functions at V_{DD}min, the supply must first rise above V_{LVDL}. As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

11.4 DC Electrical Characteristics

Table 7. DC Electrical Characteristics

(VBATT = 2.7 V, T_A = 25 °C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (voltage applied to power input pins; VBATT_1, VBATT_2, VBATT_3, and VBATT_4)	V_{DD}	1.8[1]	2.7	3.6	Vdc
Minimum CPU RUN voltage (Radio and peripherals not guaranteed operational; CPU, RAM, and Flash operational)	V_{DD_RUN}	1.6			Vdc
Minimum RAM retention voltage (voltage applied to VBATT power input pins)	V_{RAM}	V_{POR}			Vdc
Low-voltage detection threshold - high range (all conditions[2]) V_{DD} falling V_{DD} rising	V_{LVDH}	2.18 2.20	2.23 2.26	2.32 2.32	Vdc
Low-voltage detection threshold - low range (all conditions) V_{DD} falling V_{DD} rising	V_{LVDL}	1.67 1.68	1.70 1.77	1.80 1.96	Vdc
Low-voltage warning threshold - high range (all conditions) V_{DD} falling V_{DD} rising	V_{LVWH}	2.25 2.30	2.32 2.36	2.45 2.42	Vdc
Low-voltage warning threshold - low range (all conditions) V_{DD} falling V_{DD} rising	V_{LVWL}	1.79 1.74	1.81 1.84	1.91 1.99	Vdc
Power-on reset (POR) voltage	VPOR	-	1.0	-	Vdc
High impedance (off-state) leakage current (per pin) (V_{In} = V_{DD} or V_{SS}, all input/outputs, device must not be in low power mode)	$\|I_{OZ}\|$	-	-	1.0	µA
Input Current (V_{IN} = 0 V or V_{DDINT}) (V_{In} = V_{DD} or V_{SS}, all input/outputs, device must not be in low power mode)	I_{IN}	-	-	±1.0	µA
Input Low Voltage (All digital inputs)	V_{IL}	0	-	30% V_{BATT}	V
Input High Voltage (all digital inputs)	V_{IH}	70% V_{BATT}	-	V_{BATT}	V

Table 7. DC Electrical Characteristics (continued)
(VBATT = 2.7 V, T_A = 25 °C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input hysteresis (all digital inputs)	V_{hys}	0.06 × V_{DD}		—	V
Internal pullup resistors[3] (all port pins and IRQ except CMT)	R_{PU}	-	20	-	kohm
Internal CMT pullup resistor[3]	R_{PU}	-	10	-	kohm
Internal pulldown resistors[3] (KBI pins and IRQ)	R_{PD}	-	20	-	kohm
Output High Voltage All standard GPIO = 3mA CMT output IRO = 20 mA	V_{OH}	80% V_{BATT}	-	V_{BATT}	V
Output Low Voltage (All digital outputs) All standard GPIO = 3mA CMT output IRO = 20 mA	V_{OL}	0	-	20% V_{BATT}	V
Input capacitance (all non-supply pins)	C_{In}	—	3	—	pF

1 Although the device functions at V_{DD}min, the supply must first rise about V_{LVDL}. As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

2 Denotes full voltage supply and temperature ranges.

3 Measurement condition for pull resistors: $V_{IN} = V_{SS}$ for pullup and $V_{IN} = V_{DD}$ for pulldown.

11.5 Supply Current Characteristics

Table 8. Supply Current Characteristics
(VBATT = 2.7 V, T_A = 25 °C, unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
STOP2 • All internal circuitry off, RAM retained, reference oscillator off, KBI active. I/O values are latched to preserve state. RTC off. RF in reset. • All internal circuitry off, RAM retained, reference oscillator off, KBI active. I/O values are latched to preserve state. RTC on with 1 kHz osc. RF in reset. • All internal circuitry off, RAM retained, reference oscillator off, KBI active. I/O values are latched to preserve state. RTC on with 32.768 kHz osc. RF in reset.	$S2I_{DD}$		0.29 0.40 0.40	1 1 3	μA
STOP3 • All internal circuitry off, RAM, I/O, internal registers & selectable peripheral registers retained, 32MHz ref oscillator off, RTC off, LVD off. RF in reset. • All internal circuitry off, RAM, I/O, internal registers & selectable peripheral registers retained, 32MHz ref oscillator off, RTC on with 1 kHz osc, LVD off. RF in reset. • All internal circuitry off, RAM, I/O, internal registers & selectable peripheral registers retained, 32MHz ref oscillator off, RTC on with 32.768 kHz osc, LVD off. RF in reset. • All internal circuitry off, RAM, I/O, internal registers & selectable peripheral registers retained, 32MHz ref oscillator on, RTC on with 32 MHz osc, LVD off. RF in reset	$S3I_{DD}$		0.45 0.55 2.65 330		μA

Table 8. Supply Current Characteristics (continued)

(VBATT = 2.7 V, T_A = 25 °C, unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
LPWAIT Low Power Wait • Entered from LPRUN • Processor off, bus clock @ 250 kHz, voltage regulator is standby. • Peripherals and modem clocks disabled. RF in reset.	$LPWI_{DD}$	0.50	0.56	0.62	mA
LPRUN Low Power Run • Processor forced to 500 kHz and bus clock@ 250 kHz • Peripheral state & RAM retained. Voltage regulators in standby. • Peripherals and modem clocks disabled. RF in reset.	$LPRI_{DD}$	0.53	0.76	0.85	mA
RUN • Processor running at 32 MHz and peripheral clock @ 16 MHz • All peripheral clocks disabled[1]& RAM active, voltage regulators fully on. • RF in reset.	$RUNI_{DD}$	4.0	4.7	4.9	mA
TX • MCU in LPRUN (peripheral clock @ 250 kHz) • RF in Transmit mode (nominal power out)[2]	TXI_{DD}	21.3	26.6	28.2	mA
RX_PPD • MCU in LPRUN (peripheral clock @ 250 kHz) • RF in Receive Partial Power Down mode	$RXPPDI_{DD}$		22.3		mA
RX • MCU in LPRUN (peripheral clock @ 250 kHz) • RF in Receive mode either 1) waiting @ full sensitivity or 2) receiving actual frame	RXI_{DD}	26.8	34.2	35.0	mA

1 Registers SCGC1 and SCGC2 = 0x00

2 TX output power set to nominal (0 dBm).

Table 9. Typical Current Adders for Enabled Functions (32MHz CPU clock)

(VBATT = 2.7 V, T_A = 25 °C, unless otherwise noted)

Parameter	Description	Typical Current	Unit
LVD/LVW	Low Voltage Detect / Warning	60	µA
TPM	TPM module enabled (each)	90	µA
KBI	KBI enabled	25	µA
IIC	IIC enabled	175	µA
SCI	SCI Enabled	150	µA
SPI	SPI enabled	70	µA
CMT	CMT enabled	78	µA
IRQ	IRQ clock enabled	23	µA
DEBUG	DEBUG module clock enabled	135	µA

Table 9. Typical Current Adders for Enabled Functions (32MHz CPU clock)

(VBATT = 2.7 V, T_A = 25 °C, unless otherwise noted)

Parameter	Description	Typical Current	Unit
MODEM	Modem (transceiver) clock enabled	285	µA
AES	AES clock enabled	65	µA

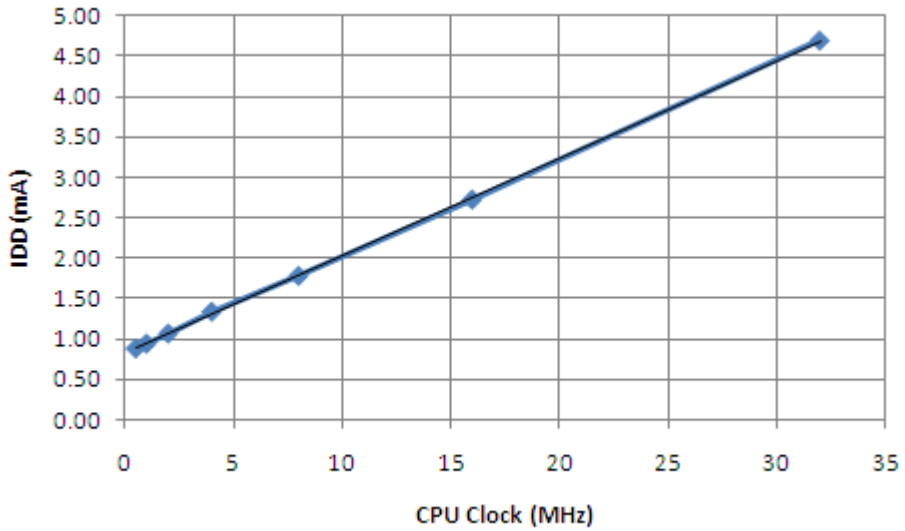

Figure 3. Typical RUN Current versus CPU Clock (only 0.5, 1, 2, 4, 8, 16, and 32 MHz available)

11.6 RF AC Electrical Characteristics

NOTE

All specified RF parameters are referenced to the package pins and are the result of measurements in the reference circuit shown in Figure 5.

Table 10. Receiver AC Electrical Characteristics for 802.15.4 Modulation Mode

(VBATT = 2.7 V, TA = 25 °C, f_{ref} = 32MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Sensitivity for 1% Packet Error Rate (PER) (+25 °C, @ package interface)[1]	$SENS_{25\ °C}$		-94	-91	dBm
Sensitivity for 1% Packet Error Rate (PER) (Over all conditions)[2]	SENS			-89	dBm
Saturation (maximum input level)	$SENS_{max}$	10			dBm
Channel Rejection for 1% PER +5 MHz (adjacent channel)[3] -5 MHz (adjacent channel)[3] +10 MHz (alternate channel)[4] -10 MHz (alternate channel)[4] >= 15 MHz[5]			 39 35 46 46 53		dB

Table 10. Receiver AC Electrical Characteristics for 802.15.4 Modulation Mode

(VBATT = 2.7 V, TA = 25 °C, f_{ref} = 32MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Error Tolerance[6]		200	-	-	kHz
Symbol Rate Error Tolerance[6]		80	-	-	ppm

1 Measured at f_c = 2450 MHz; see Figure 4 for RX performance vs. channel frequency
2 All conditions includes -40°C to +85°C, VBATT = 1.8V to 3.6V, and full frequency range
3 IEEE 802.15.4 Standard specifies minimum adjacent channel rejection as 0 dB
4 IEEE 802.15.4 Standard specifies minimum alternate channel rejection as 30 dB
5 This parameter represents an average of all readings across all channels
6 Minimum set by IEEE 802.15.4 Standard

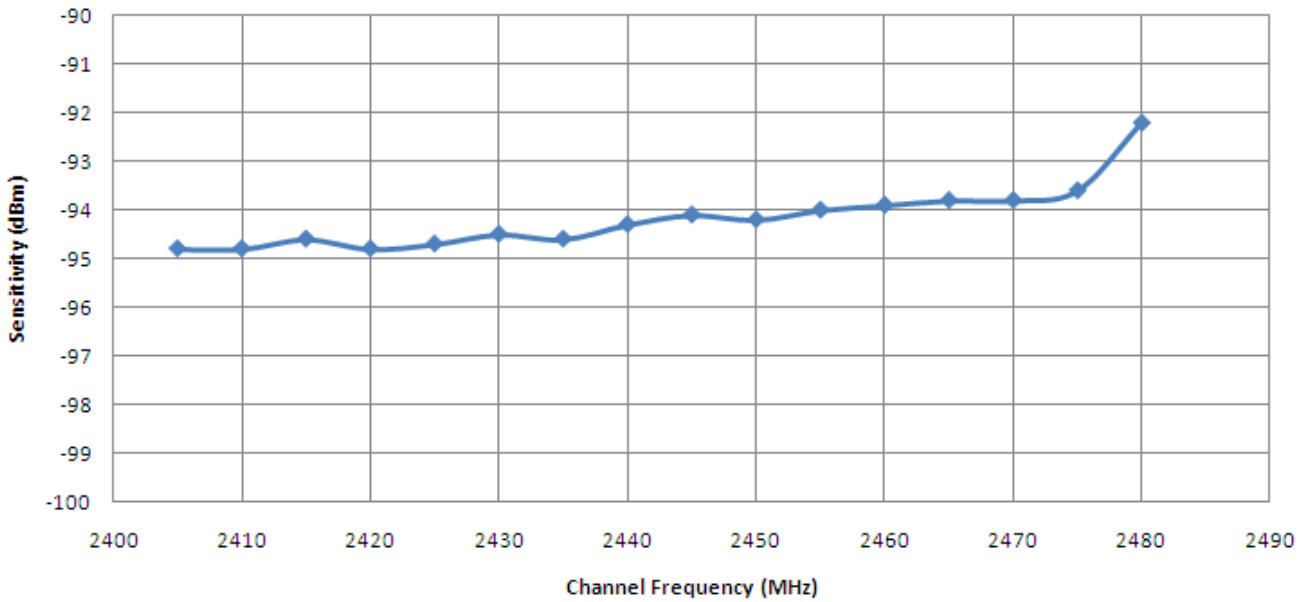

Figure 4. Typical RX Sensitivity vs. Channel Frequency @ 25°C

Table 11. Transmitter AC Electrical Characteristics for 802.15.4 Modulation Mode

(VBATT = 2.7 V, T_A = 25 °C, f_{ref} = 32 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Nominal Output Power[1]	P_{out}	-2.5	0	2.3	dBm
Maximum Output Power[2]		-	+2	-	dBm
Error Vector Magnitude	EVM		<16	18	%
Output Power Control Range		-	30	-	dB
Over the Air Data Rate		-	250	-	kbps
2nd Harmonic[3]		-	-44[4]	-	dBm/(100 kHz)

Table 11. Transmitter AC Electrical Characteristics (continued)for 802.15.4 Modulation Mode

(VBATT = 2.7 V, T_A = 25 °C, f_{ref} = 32 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
3rd Harmonic and greater[3]		-	-54[4]	-	dBm/(100kHz)
Spurious Emissions[5] <1 GHz (quasi-peak detection mode) >1 GHz (peak detection mode) Lower Band Edge (peak detection mode) Upper Band Edge (peak detection mode)			 -66 -40 -34 -23		 dBm dBm/Mhz dBm/Mhz dBm/Mhz

1 Register sets output power to nominal (0 dBm).

2 Register sets output power to maximum.

3 Measurements taken at output of evaluation circuit set for maximum power out and averaged over 100ms.

4 With use of external filtering / harmonic trap as implemented in reference circuit.

5 Derived from measured radiated values in units of dBuV/m and converted to EIRP (dBm).

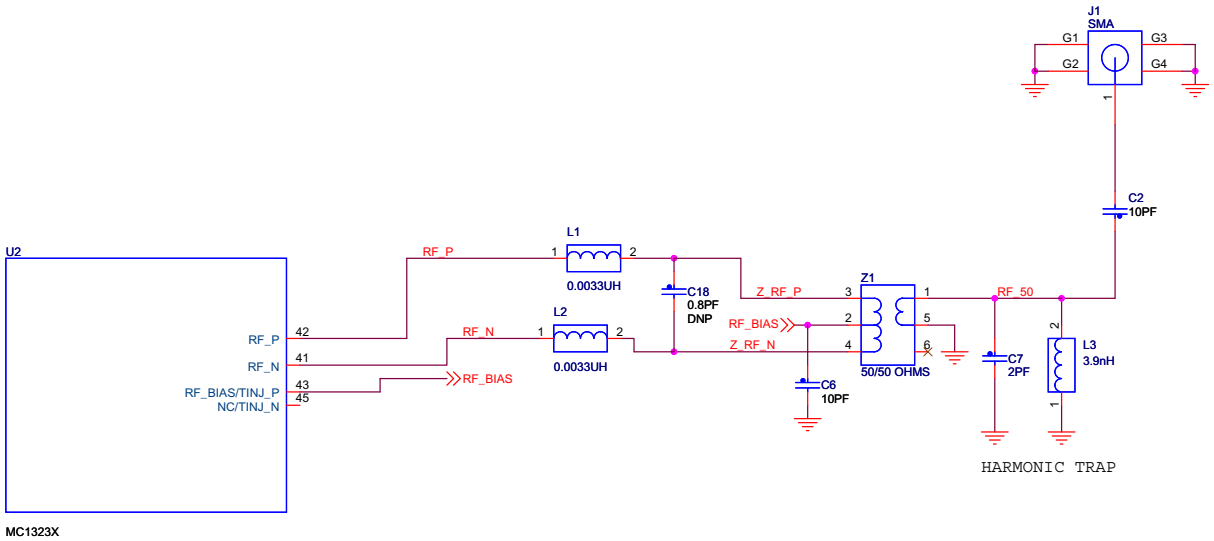

Figure 5. RF Parameter Reference Circuit

Table 12. RF Port Impedance, Pin RF_P and RF_N

Description	Frequency	Symbol	Typical	Unit
Series equivalent effective device impedance across the differential port derived from characterization of match network	2.405 GHz 2.442 GHz 2.480 GHz	Z_{in}	22.2 - j74.8 20.6 - j89.9 20.2 - j98.4	Ω

11.7 Crystal Reference Clock Oscillator Characteristics

The reference oscillator model including external crystal in shown in Figure 6. The IEEE 802.15.4 Standard requires a frequency tolerance less than or equal to +/- 40 ppm as shown in the oscillator specification Table 13. With a suitable crystal (refer to Table 14), the device frequency tolerance can typically trimmed to be held to +/- 30 ppm over all conditions.

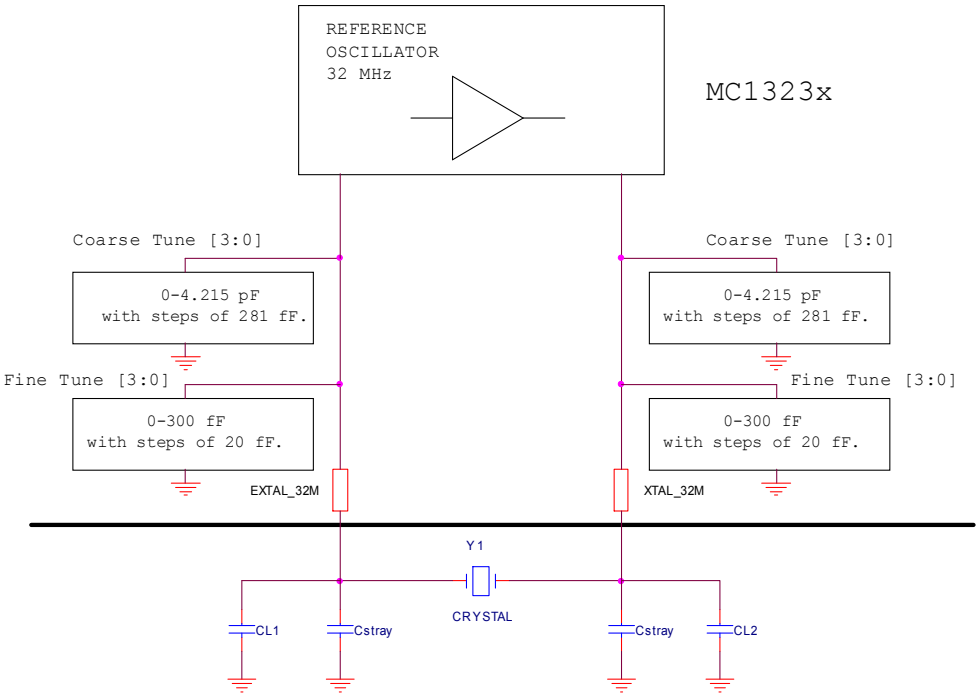

Figure 6. 32MHz Reference Oscillator Model

Table 13. Reference Oscillator Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency (nominal)			32.000000		MHz
Oscillator frequency tolerance over temperature range.			+/- 30	+/- 40	ppm
External load capacitance	C_{Lext}		8		pF
Internal Osc startup time[1]	t_{cst}		800		µs

[1] This is part of device wake-up time.

Table 14. Recommended 32 MHz Crystal Specifications

Parameter	Value	Unit	Condition
Frequency	32.000000	MHz	
Frequency tolerance (cut tolerance)	± 10	ppm	max at 25 °C
Frequency stability (temperature drift)	± 16-18	ppm	Over desired temperature range

Table 14. Recommended 32 MHz Crystal Specifications (continued)

Parameter	Value	Unit	Condition
Aging	± 2	ppm	max
Equivalent series resistance	60	Ω	max
Load capacitance	9	pF	
Shunt capacitance	<2	pF	max
Mode of oscillation			fundamental

11.8 Optional 32.768 kHz Crystal Oscillator Specifications

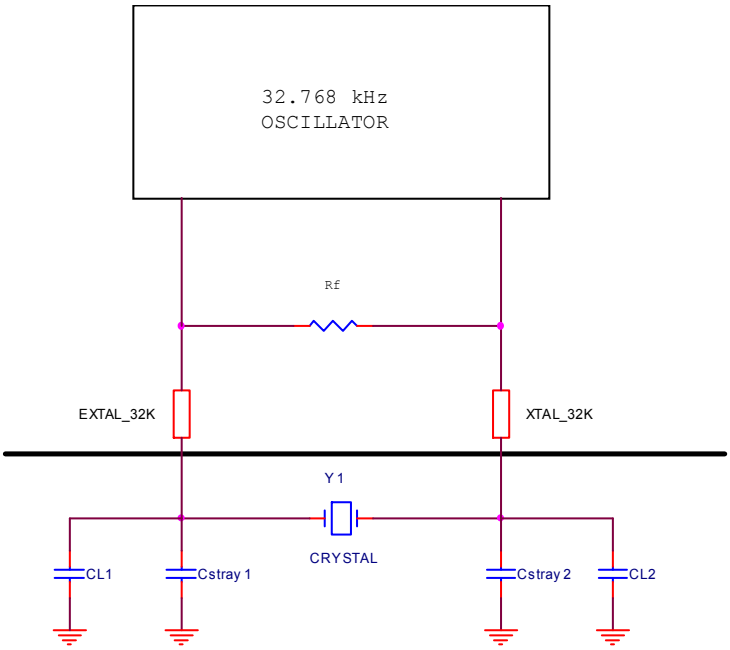

Figure 7. 32.768 kHz Oscillator Mode

Table 15. 32.768 Oscillator Crystal Typical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Crystal frequency			32.768		kHz
Frequency tolerance @ 25 °C			± 20		ppm
Load capacitance		12	12.5	16	pF
Equivalent series resistance (ESR)		40		130	kΩ
Shunt capacitance				2	pF
Tolerated drive level				1	μW

11.9 Internal Low Speed Reference Oscillator Specifications

Table 16. Internal 1 kHz Oscillator Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Default Frequency @ 25 °C		0.80	1.0	1.40	kHz
Oscillator frequency variation over temperature[1] Deviation at -40 °C from 25 °C frequency Deviation at +85 °C from 25 °C frequency		-	 -13 +6	-	%

[1] This percentage deviation is typical change from the individual device oscillator frequency at 25 °C

11.10 Control Timing and CPU Bus Specifications

Table 17. MCU Control Timing

(VBATT = 2.7 V, T_A = 25 °C, f_{ref} = 32MHz, unless otherwise noted.)

Parameter	Symbol	Min	Typical	Max	Unit
CPU frequency (t_{cyc} = 1/RDIV)	f_{CPU}	$f_{ref}/64$[1]	—	32 [1]	MHz
Bus Frequency (always 1/2 CPU clock) (t_{cyc} = f_{BUS})	f_{BUS}		$f_{CPU}/2$		MHz
External reset pulse width		100	—	—	ns
External asynchronous minimum interrupt pulse width (KBI or IRQ)[2]		100	—	—	ns
External synchronous minimum interrupt pulse width (KBI or IRQ)[3] [4]		1.5 t_{cyc}	—	—	ns
Wake-up time from STOP2 or STOP3			800		µs

[1] The 32MHz reference clock.

[2] Minimum pulse to recognize a asynchronous transition

[3] Minimum pulse to recognize a level sensitive

[4] For determination of an actual key/push button in a matrix, this pulse with must remain present for the keyboard scan routine duration. Thus, the minimum pulse width would be determined by the software, not the detection hardware.

11.11 SPI Timing

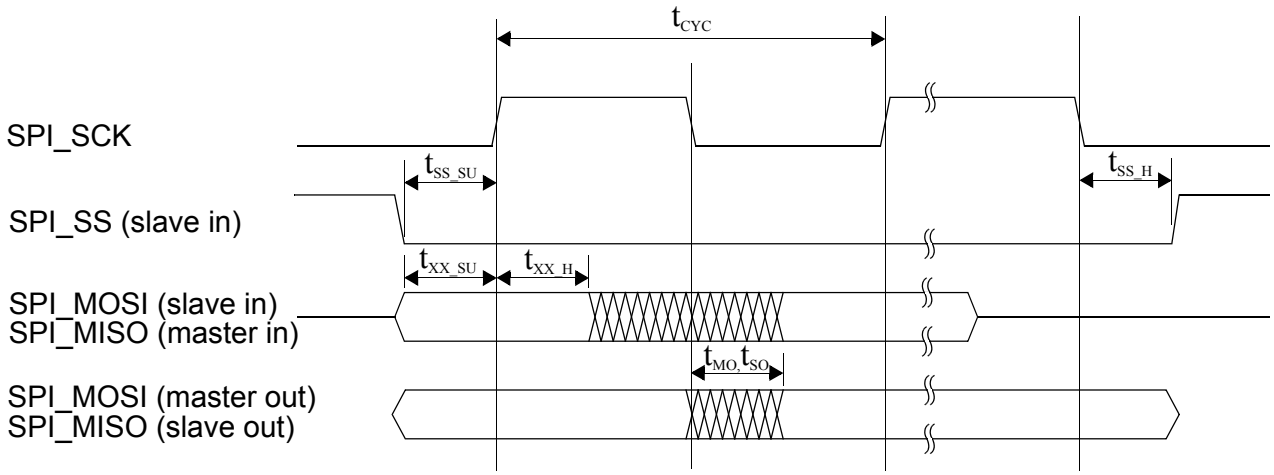

Figure 8. SPI Timing Diagram

Table 18 describes the timing requirements for the SPI system.

Table 18. SPI Timing

Parameter	Symbol	Min	Typical	Max	Unit
Master SPI_SCK Period	t_{CYC}	bus_Clk*2	38	bus_Clk *256	ns
Slave SPI_SCK Period	t_{CYC}	10			ns
Slave SPI_SS Setup Time	t_{SS_SU}	10			ns
Slave SPI_SS Hold Time	t_{SS_H}	10			ns
Slave SPI_MOSI Setup Time	t_{SI_SU}	10			ns
Slave SPI_MOSI Hold Time	t_{SI_H}	10			ns
Master SPI_MISO Setup Time	t_{MI_SU}	20			ns
Master SPI_MISO Hold Time	t_{MI_H}	0			ns
Master SPI_MOSI Output Time	t_{MO}			5	ns
Slave SPI_MISO Output Time (with 15 pf load)	t_{SO}			20	ns

11.12 I²C Specifications

Table 19 describes the timing requirements for the I²C system.

The I²C module is driven by the peripheral bus clock (typically max 16 MHz) and the SCL bit clock is generated from a prescaler.

Table 19. I²C Signal DC Specifications (I2C_SDA and I2C_SCL)

Parameter	Symbol	Min	Typical	Max	Unit
Input Low Voltage	V_{IL}	-0.3	-	0.3 V_{DDINT}	V
Input High Voltage	V_{IH}	0.7 VBATT	-	VBATT + 0.3	V
Input hysteresis	V_{hys}	0.06 × VBATT		—	V
Output Low Voltage[1] (I_{OL} = 5 mA)	V_{OL}	0	-	0.2 VBATT	V
Input Current (V_{IN} = 0 V or V_{DDINT})	I_{IN}	-	-	±1	µA
Pin capacitance	C_{in}			<10	pF

[1] SDA and SCL are open drain outputs

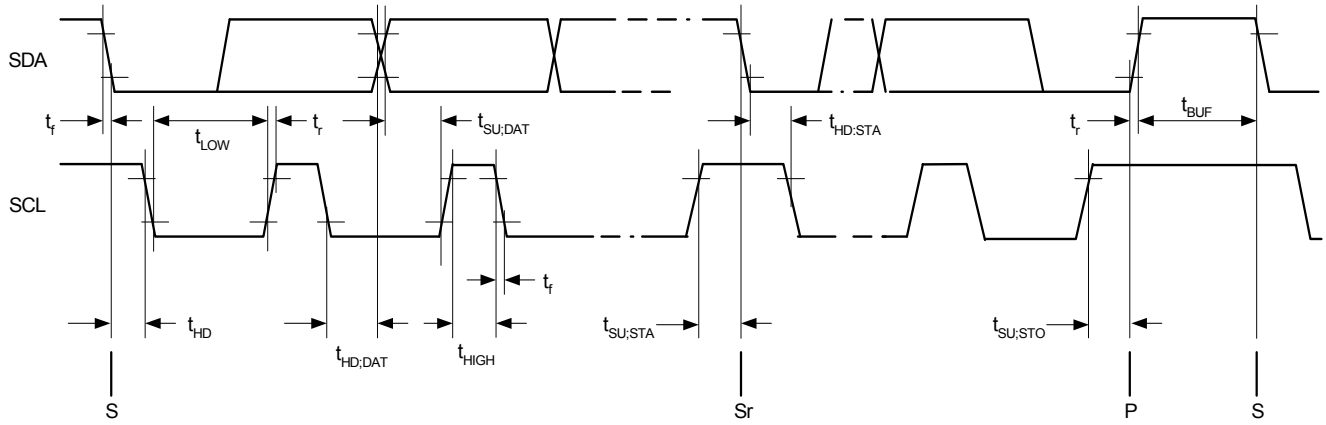

Figure 9. I²C Timing Diagram

NOTE

The I²C timing limits reflect values that are necessary meet to the I²C Bus specification.

Table 20. I²C Signal AC Specifications[1]

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency (when source)	f_{SCL}	0	100	0	150	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data hold time	$t_{SHD;DAT}$	0[2]	3.45[3]	0[2]	0.9[3]	µs
Data setup time	$t_{SU:DAT}$	250	-	100[4]	-	ns
Rise time for both SDA and SCL signals	t_r	-	1000	20 + $0.1C_b$[5]	300	ns
Fall time for both SDA and SCL signals	t_f	-	300	20 + $0.1C_b$[5]	300	ns
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b	-	400	-	400	pF

[1] All values referred to V_{IHmin} and V_{ILmax} levels

[2] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[3] The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

[4] A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{SU;DAT}$ >= 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\ max}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.

[5] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, the faster fall-times are allowed.

11.13 FLASH Specifications

This section provides details about program/erase times and program-erase endurance for the FLASH memory. Program and erase operations do not require any special power sources other than the normal V_{DD} supply. The FLASH is 81920 bytes organized as 80 pages by 1024 bytes. FLASH erase and program may only be executed with CPU clock programmed for 32 MHz (default)

NOTE

FLASH erase and program may only be executed with CPU clock programmed for 32 MHz (default). FLASH operations are hardware state machine controlled. User code need not count cycles. The following information is supplied for calculating approximate time to program and erase.

Table 21. FLASH Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage for program/erase/read operation	V_{BATT}	1.6		3.6	V
Byte program time (random location)	t_{prog}	40			µs
Per Byte program time (burst mode) - excludes start/end overhead	t_{Burst}	20			µs
Sector erase time	t_{Sector}	20			ms
Mass erase time	t_{Mass}	20.1			ms
Program/erase endurance T_L to T_H = –40°C to + 85°C T = 25°C		20,000	 100,000	— —	cycles
Data retention @ 25°C	t_{D_ret}	100		—	years

12 Applications Information

NOTE

Freescale provides a complete suite of design support material including development hardware and software, reference manuals, and hardware references designs for the MC1323x. The applications material presented here is primarily for illustrative purposes.

Figure 10 illustrates a basic applications circuit based on the 123x-MRB development board. Features of the circuit include:

- 32 MHz reference oscillator crystal (Y1) is required, and must meet defined specifications
- Pulldown resistor on signal PTA2 assures that devices does not enter factory test mode on power-up
- Power supply voltage (V_IC) can range from 1.8 Vdc to 3.6 Vdc (see Table 7 for usage notes)
- RF Interface circuitry -
  - — 50/100 (unbal/bal) balun converts device differential, bidirectional RF port to single-ended 50-ohm antenna port
  - — Control signal RF_Bias switches RF reference voltage to the balun as required for TX or RX
  - — L1 provides impedance matching for MC1323x RF port
  - — C4 and L2 network provides a harmonic trap for out-of-band harmonics and spurs on TX
  - — A low-cost, copper pcb “F” antenna is shown. This is a common option, although other antennas such as a chip antenna or antenna module may also be used

NOTE

- RF circuitry at 2.4 GHz is very dependent on board layout and component usage. Figure 10 shows a typical RF configuration, however component value and use can vary based on customer application.
- Mechanical design information for the MC1323x package and assembly recommendations can be found in the *Freescale IEEE 802.15.4 / ZigBee*

Package and Hardware Layout Considerations Reference Manual, Doc No. ZHDCRM.pdf.

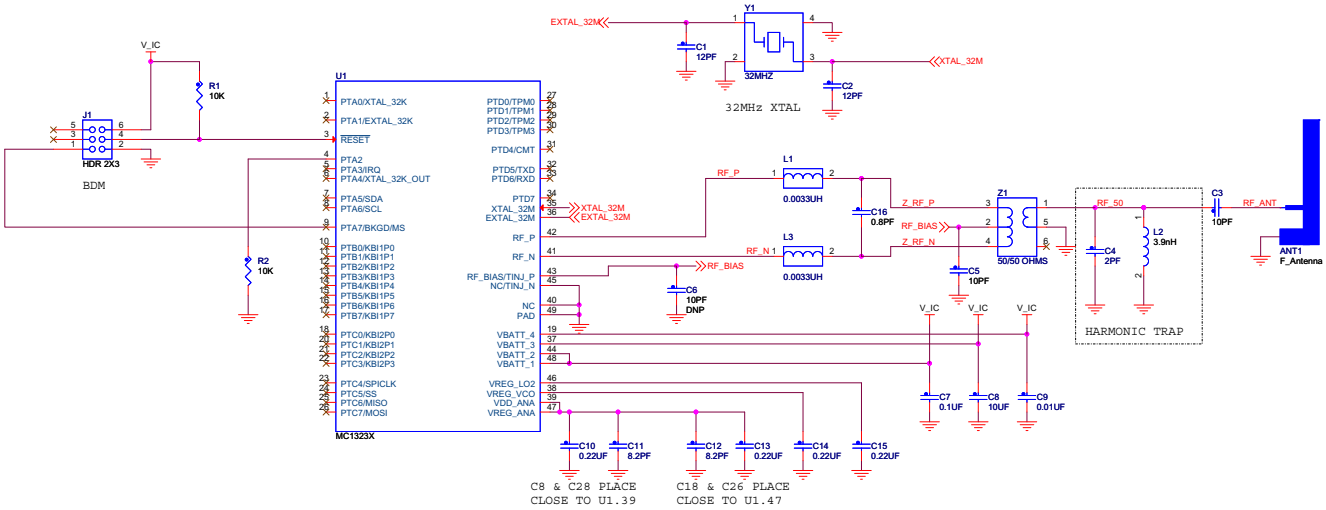

Figure 10. MC13233x Basic Applications Circuit

13 Mechanical Diagrams (Case 2124-02, Non-JEDEC)

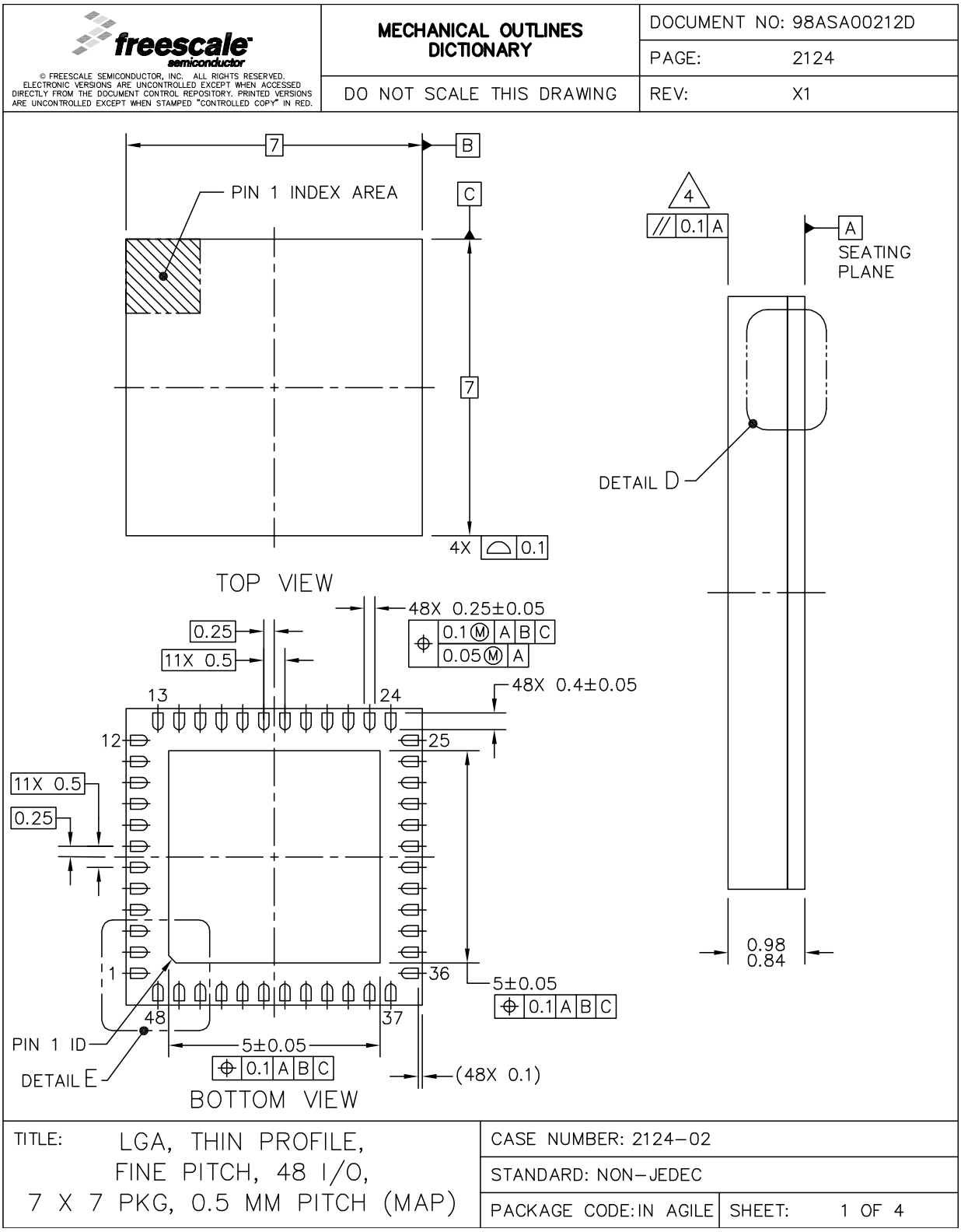

Figure 11. Mechanical Diagram (1 of 2)

NOTES

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		PAGE: 2124
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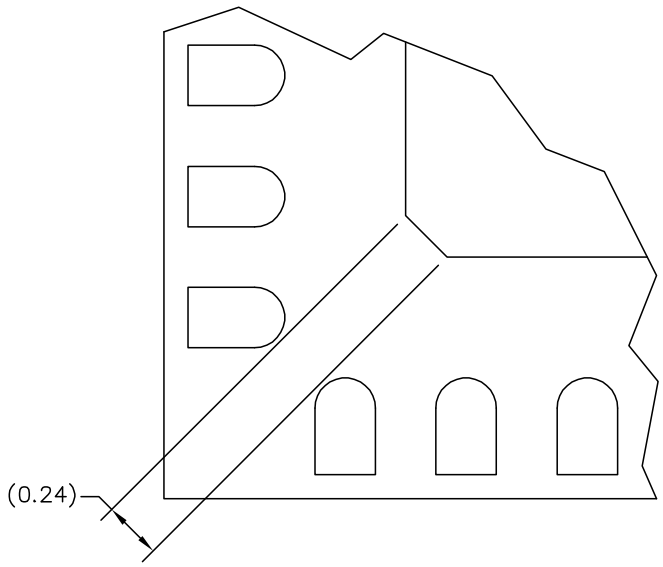
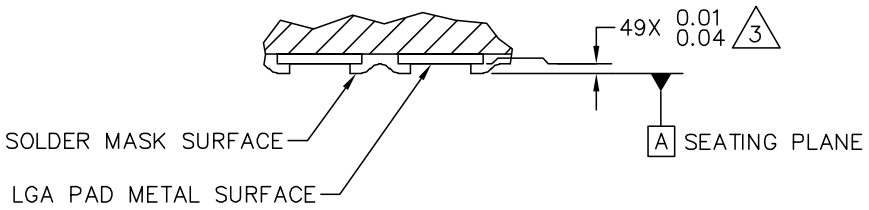


DETAIL E



DETAIL D
VIEW ROTATED 90° CW

TITLE: LGA, THIN PROFILE, FINE PITCH, 48 I/O, 7 X 7 PKG, 0.5 MM PITCH (MAP)	CASE NUMBER: 2124-02	
	STANDARD: NON-JEDEC	
	PACKAGE CODE: IN AGILE	SHEET: 2

Figure 12. Mechanical Diagram (2 of 2)

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