

# 1A Fixed Output LDO Regulators



## BDxxHC0WEFJ

### ●General Description

BDxxHC0WEFJ series devices are LDO regulators with an output current of 1.0A. The output accuracy is  $\pm 1\%$  of the output voltage. Various fixed output voltage devices that do not use external resistors are available. It can be used for a wide range of digital appliance applications. It has a small package type: HTSOP-J8 (4.90mm x 6.00mm x 1.00mm). These devices have built in over current protection to protect the device when output is shorted, 0 $\mu$ A shutdown mode and thermal shutdown circuit to protect the device during over load conditions. These LDO regulators are usable with ceramic capacitors that enable a smaller layout and longer life.

### ●Features

- $\pm 1\%$  output voltage accuracy
- Built-in Over Current Protection circuit (OCP)
- Built-in Thermal Shut Down circuit (TSD)
- Zero  $\mu$ A shutdown mode

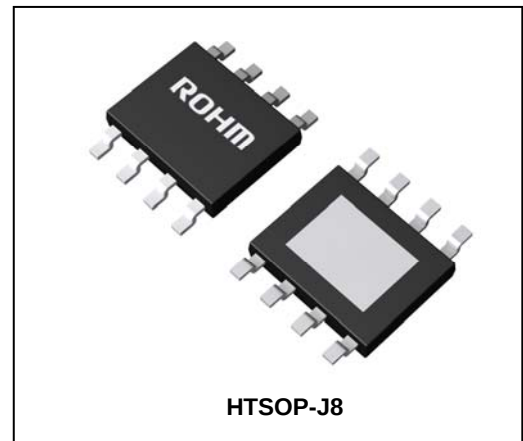
### ●Key Specifications

- Input Power Supply Voltage range: 4.5V to 8.0V
- Output voltage: 1.5V/1.8V/2.5V/3.0V/3.3V/5V/6V/7V
- Output current: 1.0A(Max.)
- Shutdown current: 0 $\mu$ A(Typ.)
- Operating temperature range: -25°C to +85°C

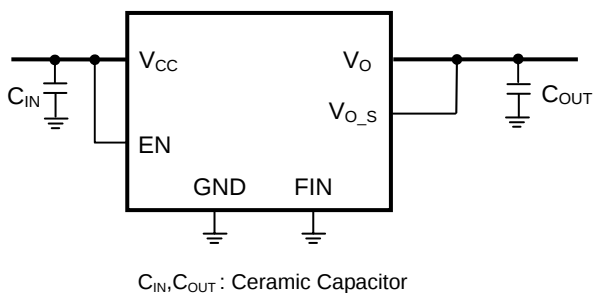
### ●Package

HTSOP-J8

(Typ.) (Typ.) (Max.)  
4.90mm x 6.00 mm x 1.00mm



### ●Typical Application Circuit



●Ordering Information

|                       |                                                                                      |                     |                |               |              |                                     |     |
|-----------------------|--------------------------------------------------------------------------------------|---------------------|----------------|---------------|--------------|-------------------------------------|-----|
| B D x x H C 0 W E F J |                                                                                      |                     |                |               |              | -                                   | E 2 |
| Part Number           | Output voltage                                                                       | Input voltage range | Output current | Shutdown mode | Package      | Packaging and forming specification |     |
|                       | 15:1.5V<br>18:1.8V<br>25:2.5V<br>30:3.0V<br>33:3.3V<br>50:5.0V<br>60:6.0V<br>70:7.0V | H:10V               | C0:1.0A        | "W":Included  | EFJ:HTSOP-J8 | E2:Emboss tape reel                 |     |

●Block Diagram  
BDxxHC0WEFJ

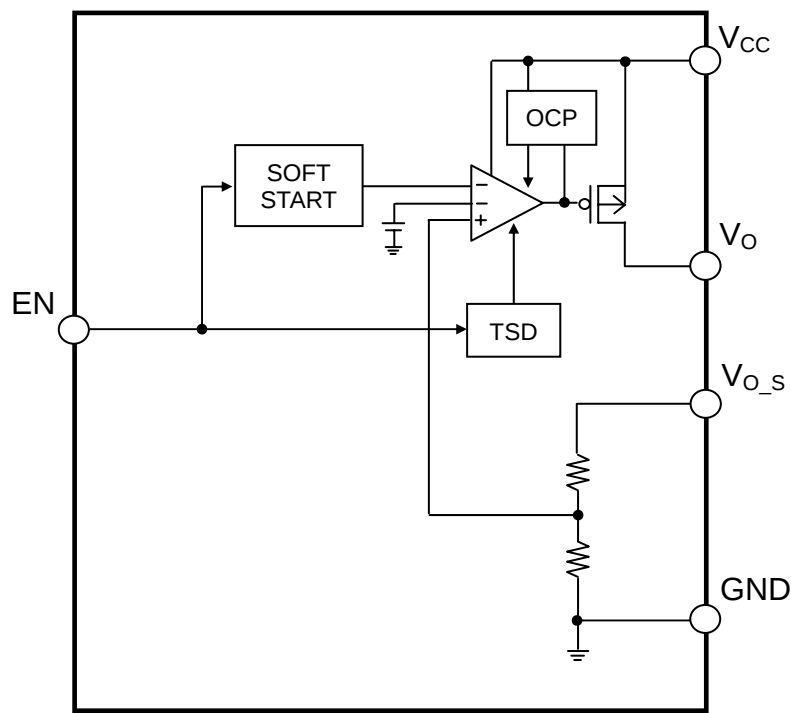
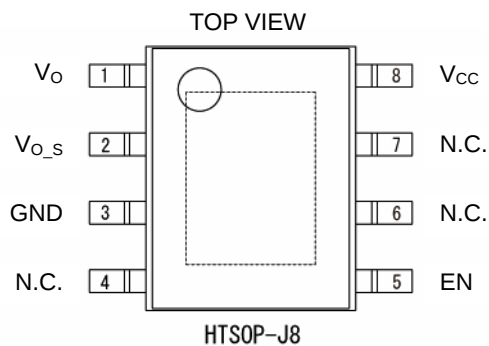


Fig.1 Block Diagram

●Pin Configuration



●Pin Description

| Pin No. | Pin name         | Pin Function                              |
|---------|------------------|-------------------------------------------|
| 1       | V <sub>O</sub>   | Output pin                                |
| 2       | V <sub>O_S</sub> | Output voltage monitor pin                |
| 3       | GND              | GND pin                                   |
| 4       | N.C.             | No Connect (Connect to GND or leave OPEN) |
| 5       | EN               | Enable pin                                |
| 6       | N.C.             | No Connect (Connect to GND or leave OPEN) |
| 7       | N.C.             | No Connect (Connect to GND or leave OPEN) |
| 8       | V <sub>CC</sub>  | Input pin                                 |
| Reverse | FIN              | Substrate(Connect to GND)                 |

### ●Absolute Maximum Ratings (Ta=25°C)

| Parameter                   |          | Symbol            | Ratings             | Unit |
|-----------------------------|----------|-------------------|---------------------|------|
| Power supply voltage        |          | V <sub>CC</sub>   | 10.0 * <sup>1</sup> | V    |
| EN voltage                  |          | V <sub>EN</sub>   | 10.0                | V    |
| Power dissipation           | HTSOP-J8 | Pd* <sup>2</sup>  | 2110 * <sup>2</sup> | mW   |
| Operating Temperature Range |          | T <sub>opr</sub>  | -25 to +85          | °C   |
| Storage Temperature Range   |          | T <sub>stg</sub>  | -55 to +150         | °C   |
| Junction Temperature        |          | T <sub>jmax</sub> | +150                | °C   |

\*1 Not to exceed Pd

\*2 Reduced by 16.9mW/°C for each increase in Ta of 1°C over 25°C. (when mounted on a board 70mm × 70mm × 1.6mm glass-epoxy board, two layer)

### ●Recommended Operating Ratings (Ta=25°C)

| Parameter                  | Symbol          | Ratings |      | Unit |
|----------------------------|-----------------|---------|------|------|
|                            |                 | Min.    | Max. |      |
| Input power supply voltage | V <sub>CC</sub> | 4.5     | 8.0  | V    |
| EN voltage                 | V <sub>EN</sub> | 0.0     | 8.0  | V    |
| Output current             | I <sub>O</sub>  | 0.0     | 1.0  | A    |

### ●Electrical Characteristics (Unless otherwise noted, Ta=25°C, EN=3V, V<sub>CC</sub>=6V)

| Parameter                        | Symbol                 | Limits                |                |                       | Unit | Conditions                                    |
|----------------------------------|------------------------|-----------------------|----------------|-----------------------|------|-----------------------------------------------|
|                                  |                        | Min.                  | Typ.           | Max.                  |      |                                               |
| Circuit current at shutdown mode | I <sub>SD</sub>        | -                     | 0              | 5                     | μA   | V <sub>EN</sub> =0V, OFF mode                 |
| Bias current                     | I <sub>CC</sub>        | -                     | 600            | 900                   | μA   |                                               |
| Line regulation                  | Reg.I                  | -1                    | -              | 1                     | %    | V <sub>CC</sub> =(V <sub>O</sub> +0.92V)→8.0V |
| Load regulation                  | Reg I <sub>O</sub>     | -1.5                  | -              | 1.5                   | %    | I <sub>O</sub> =0→1.0A                        |
| Minimum dropout voltage1         | V <sub>CO1</sub>       | -                     | 0.15           | 0.23                  | V    | V <sub>CC</sub> =5V, I <sub>O</sub> =250mA    |
| Minimum dropout voltage2         | V <sub>CO2</sub>       | -                     | 0.30           | 0.46                  | V    | V <sub>CC</sub> =5V, I <sub>O</sub> =500mA    |
| Minimum dropout voltage3         | V <sub>CO3</sub>       | -                     | 0.45           | 0.69                  | V    | V <sub>CC</sub> =5V, I <sub>O</sub> =750mA    |
| Minimum dropout voltage4         | V <sub>CO4</sub>       | -                     | 0.60           | 0.92                  | V    | V <sub>CC</sub> =5V, I <sub>O</sub> =1.0A     |
| Output voltage                   | V <sub>O</sub>         | V <sub>O</sub> × 0.99 | V <sub>O</sub> | V <sub>O</sub> × 1.01 | V    | I <sub>O</sub> =0A                            |
| EN Low voltage                   | V <sub>EN</sub> (Low)  | 0                     | -              | 0.8                   | V    |                                               |
| EN High voltage                  | V <sub>EN</sub> (High) | 2.4                   | -              | 8.0                   | V    |                                               |
| EN Bias current                  | I <sub>EN</sub>        | 1                     | 3              | 9                     | μA   |                                               |

### ●Typical Performance Curves

(Unless otherwise noted,  $T_a=25^{\circ}\text{C}$ ,  $\text{EN}=3\text{V}$ ,  $V_{\text{CC}}=6\text{V}$ )

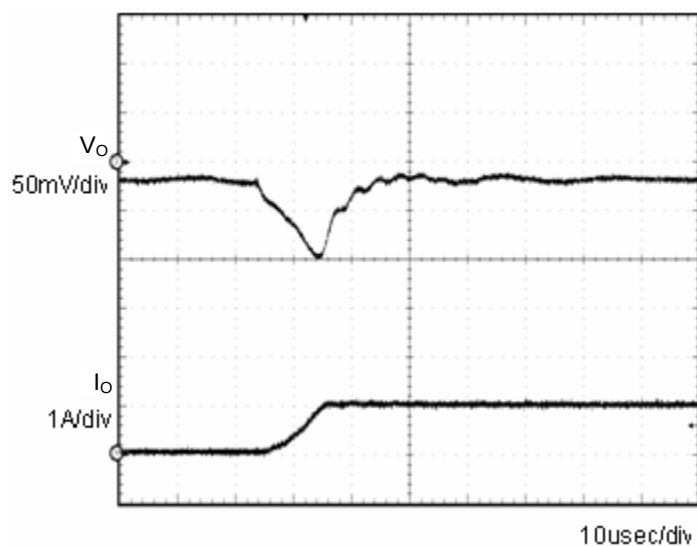


Fig.2  
Transient Response  
(0→1.0A)  
 $C_o=1\mu\text{F}$

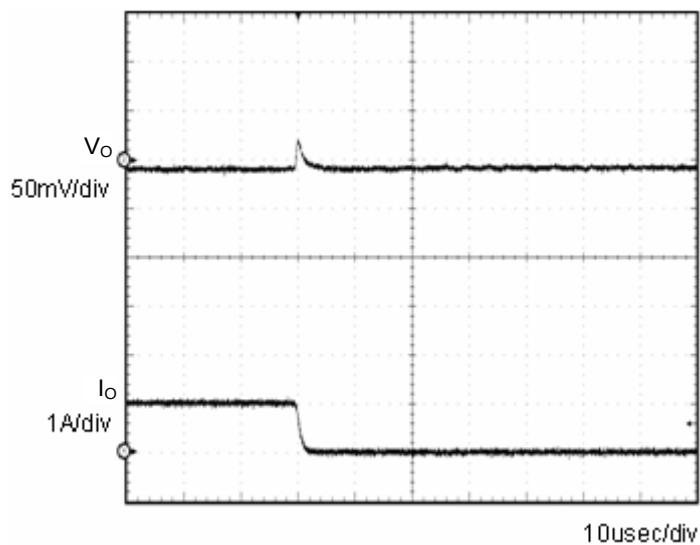


Fig.3  
Transient Response  
(1.0→0A)  
 $C_o=1\mu\text{F}$

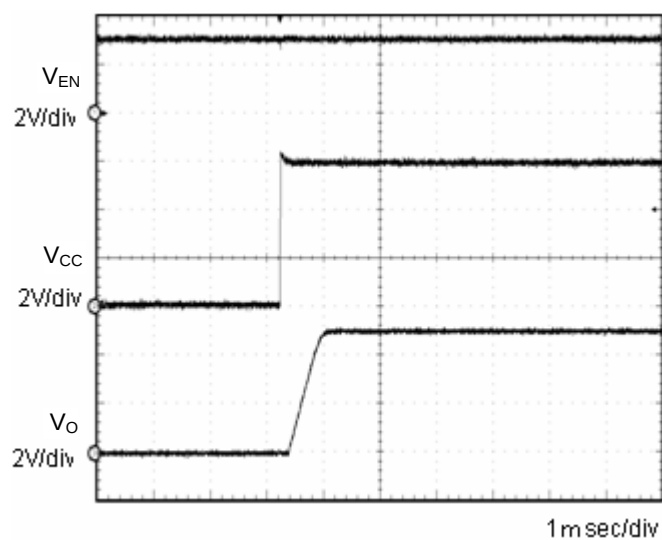


Fig.4  
Input sequence 1  
 $C_o=1\mu\text{F}$

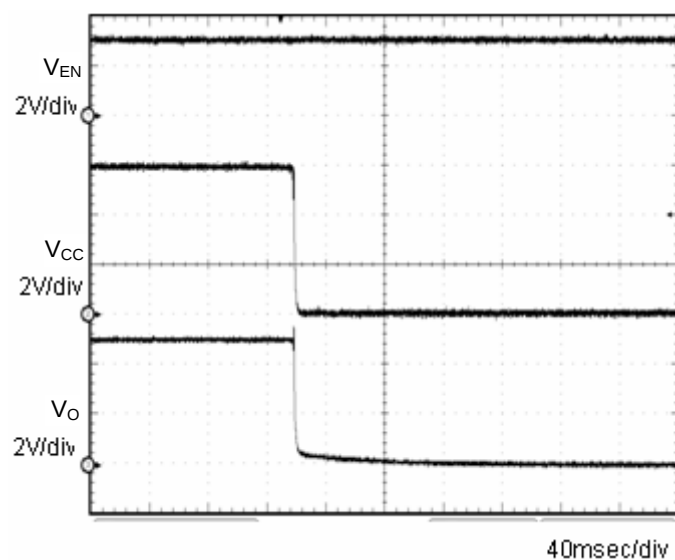


Fig.5  
OFF sequence 1  
 $C_o=1\mu\text{F}$

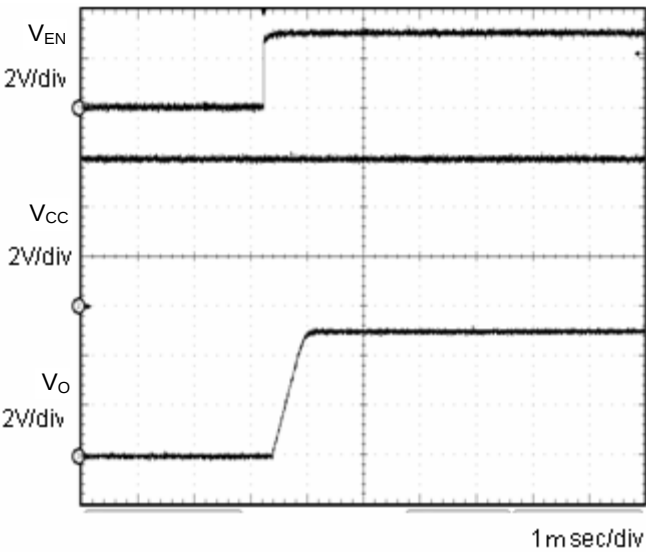


Fig.6  
Input sequence 2  
 $C_o=1\mu F$

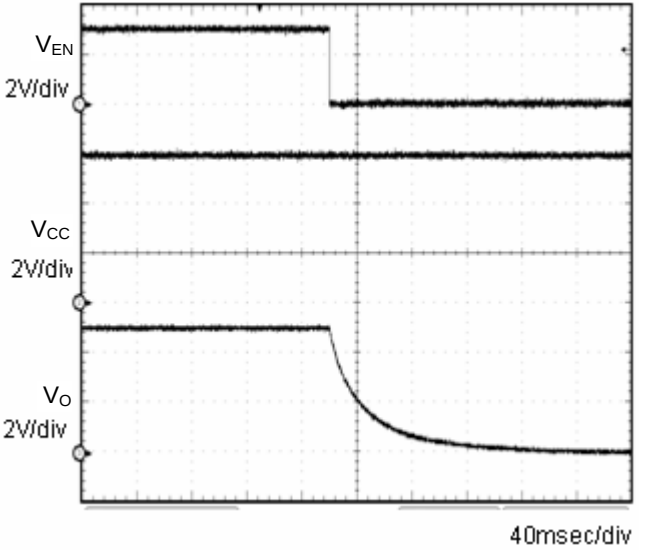


Fig.7  
OFF sequence 2  
 $C_o=1\mu F$

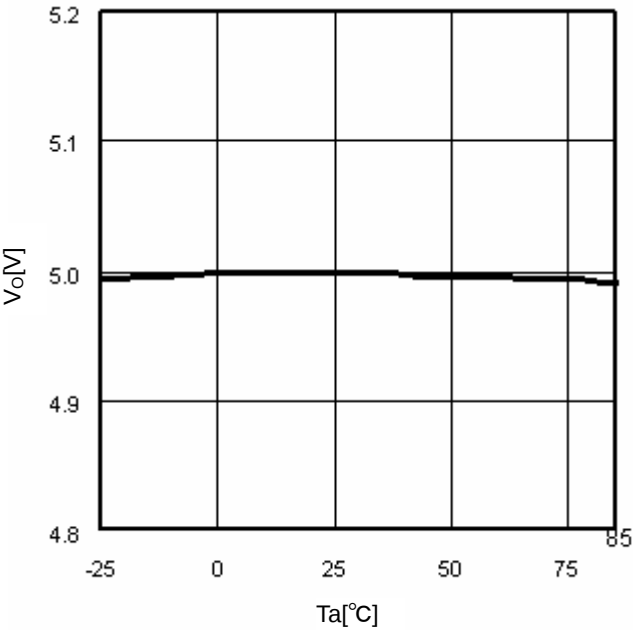


Fig.8  
 $T_a-V_O$  ( $I_o=0mA$ )

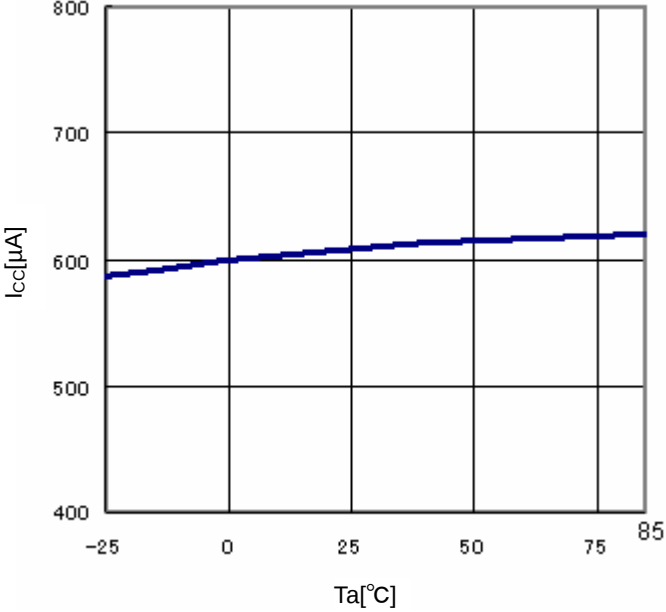


Fig.9  
 $T_a-I_{CC}$

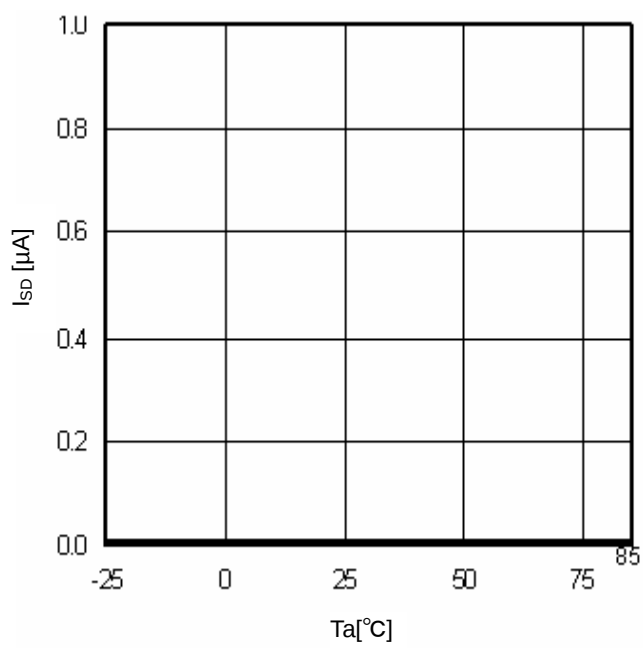


Fig.10  
 $T_a$ - $I_{SD}$   
( $V_{EN}=0V$ )

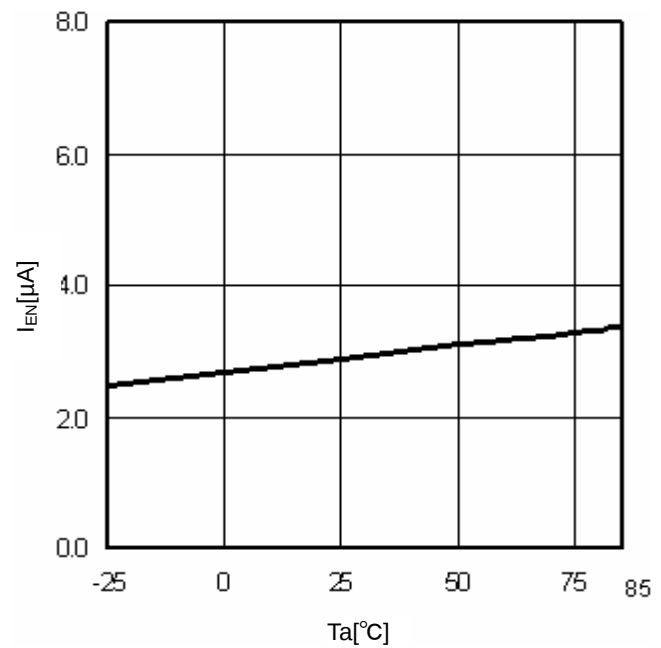


Fig.11  
 $T_a$ - $I_{EN}$

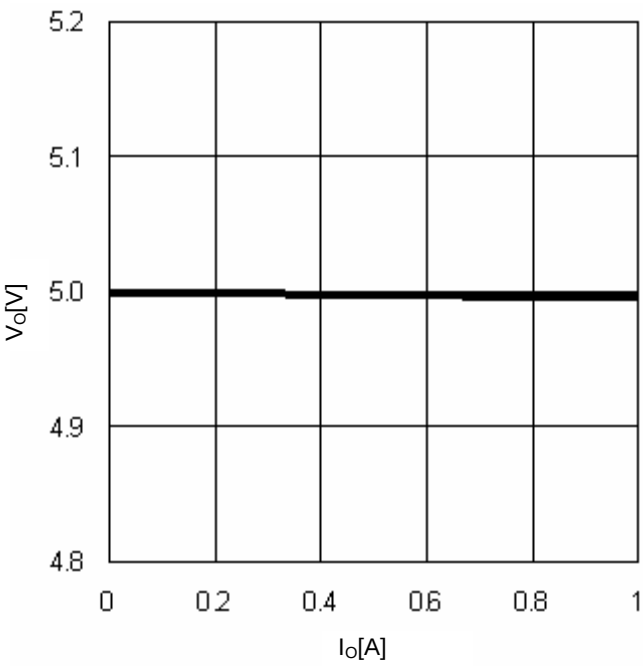


Fig.12  
 $I_O$ - $V_O$

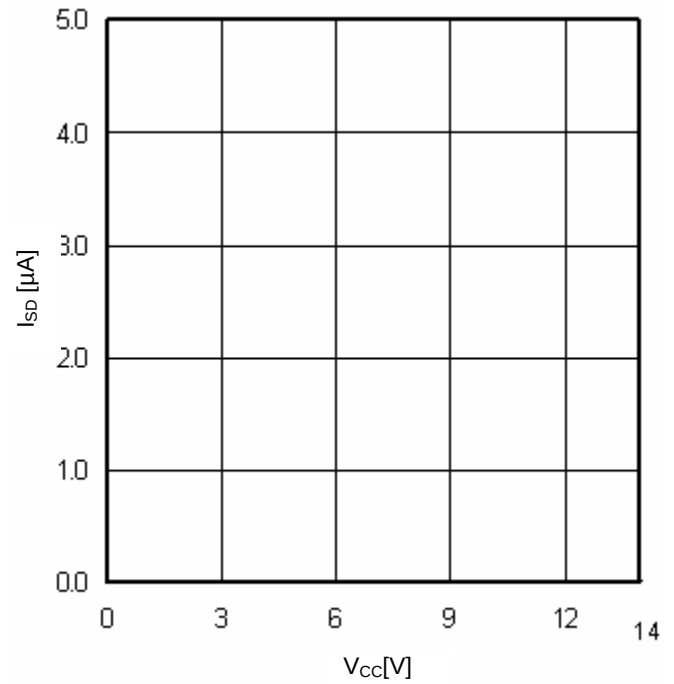


Fig.13  
 $V_{CC}$ - $I_{SD}$   
( $V_{EN}=0V$ )

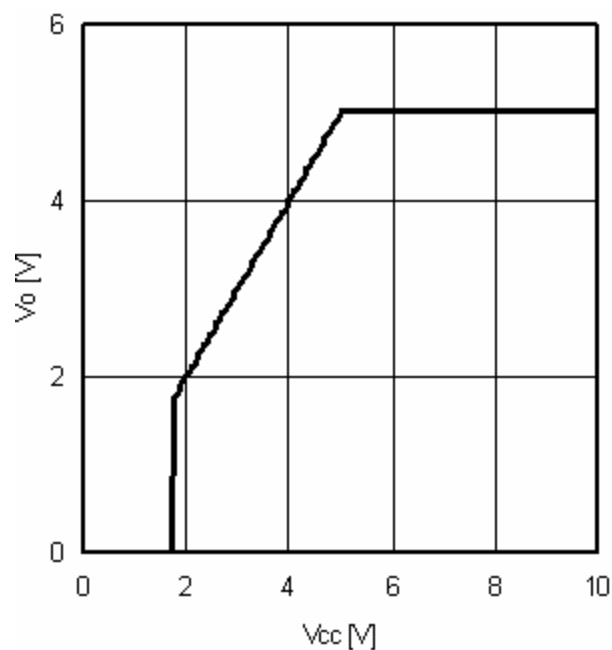


Fig.14  
 $V_{cc}-V_o$  ( $I_o=0\text{mA}$ )

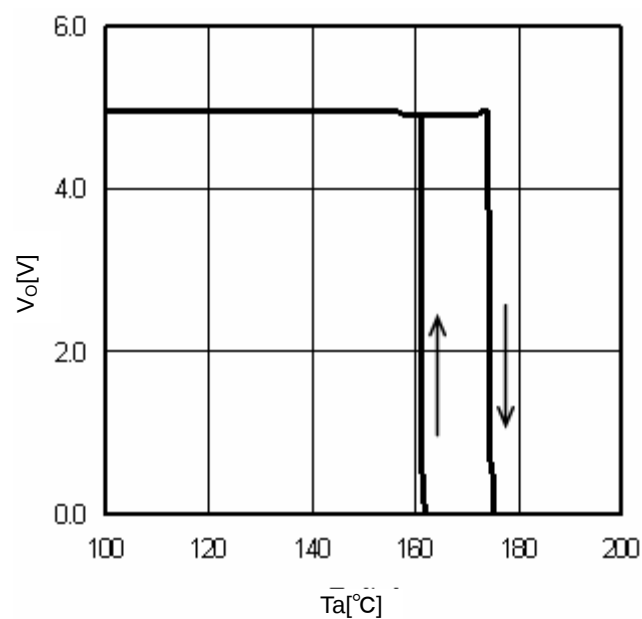


Fig.15  
TSD ( $I_o=0\text{mA}$ )

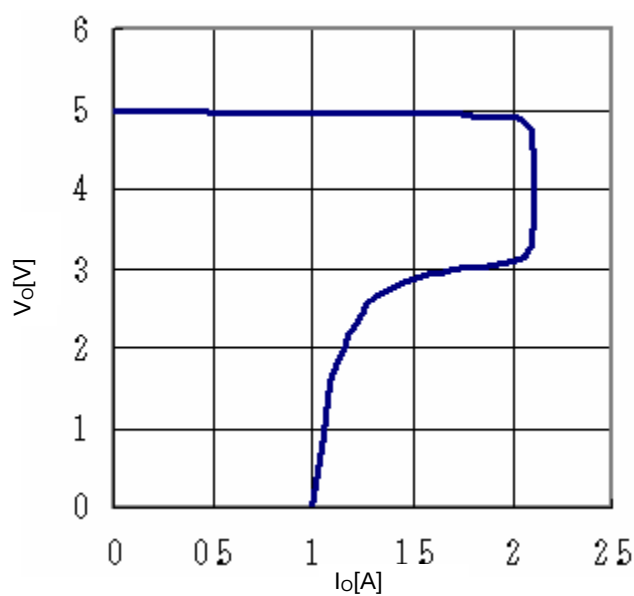


Fig.16  
OCP

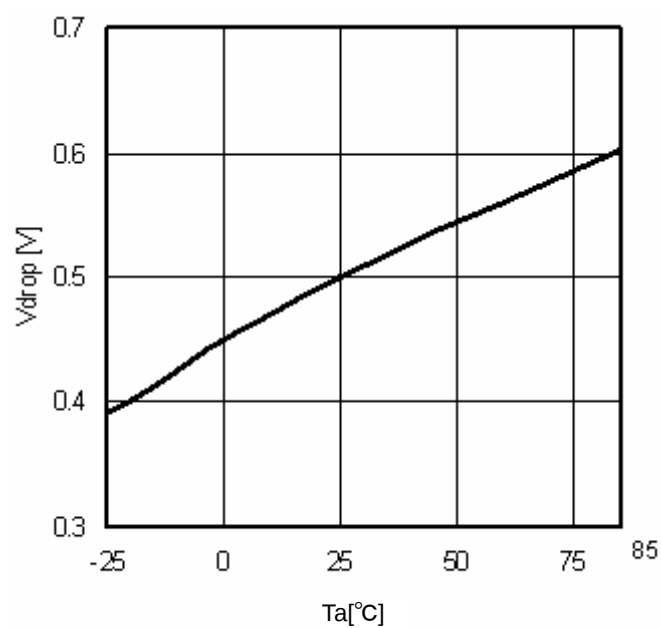


Fig.17  
Minimum dropout Voltage 1  
( $V_{cc}=5\text{V}$ ,  $I_o=-1.0\text{A}$ )

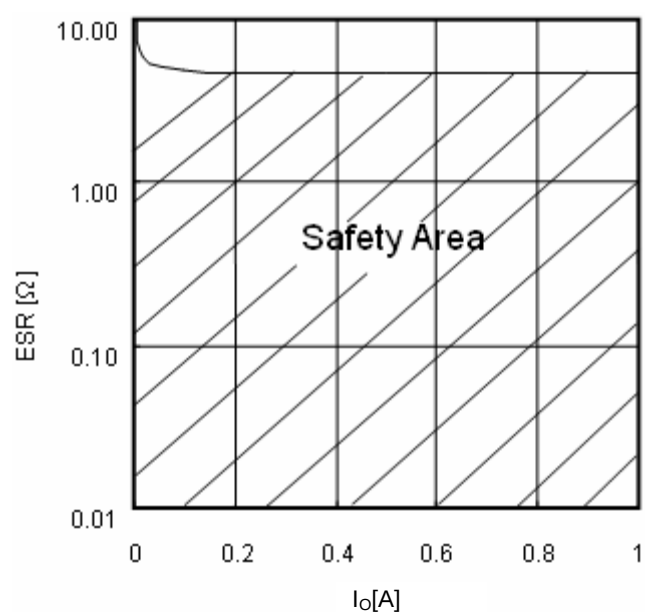


Fig.18  
ESR condenser

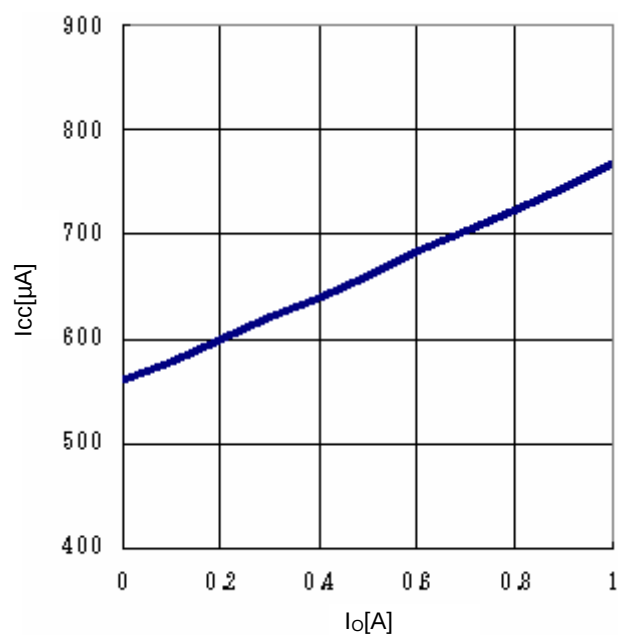


Fig.19  
 $I_o$ - $I_{cc}$

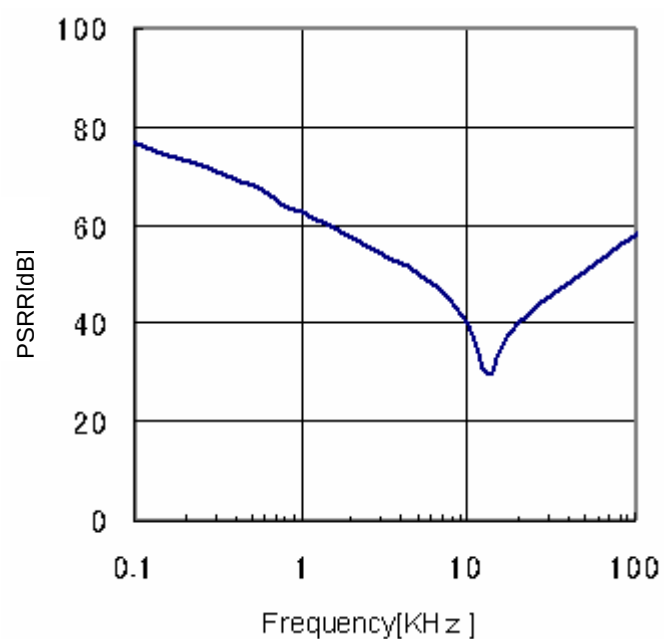


Fig.20  
PSRR ( $I_o=0\text{mA}$ )

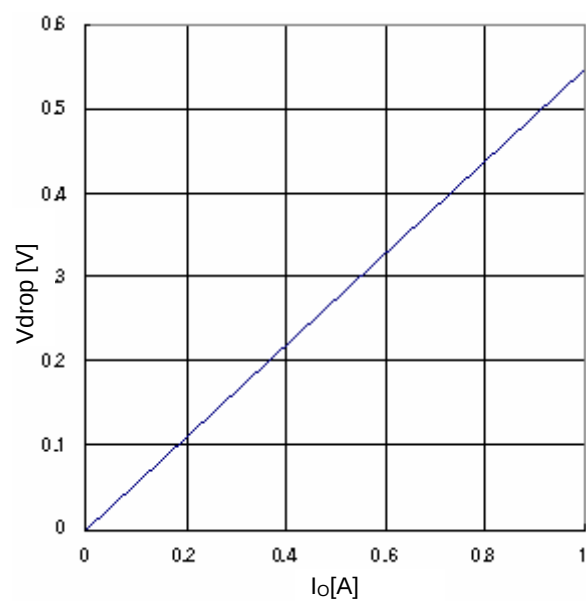


Fig.21  
Minimum dropout Voltage 2  
( $V_{CC}=4.5\text{V}$ ,  $T_a=25^\circ\text{C}$ )

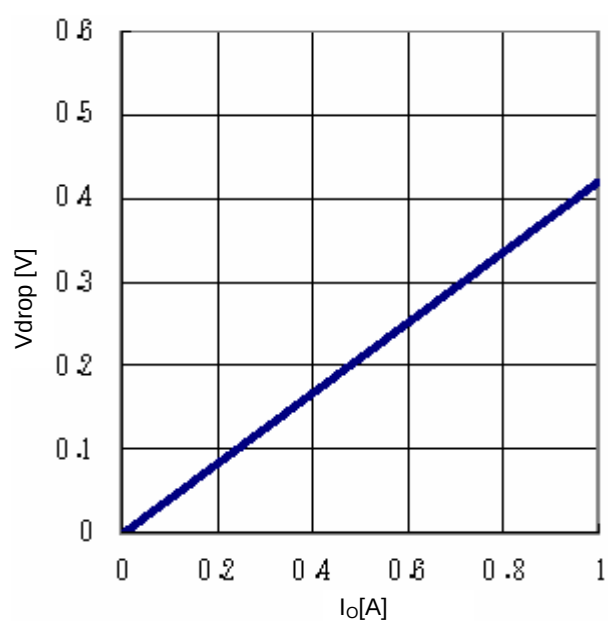


Fig.22  
Minimum dropout Voltage 3  
( $V_{CC}=6V$ ,  $T_a=25^{\circ}C$ )

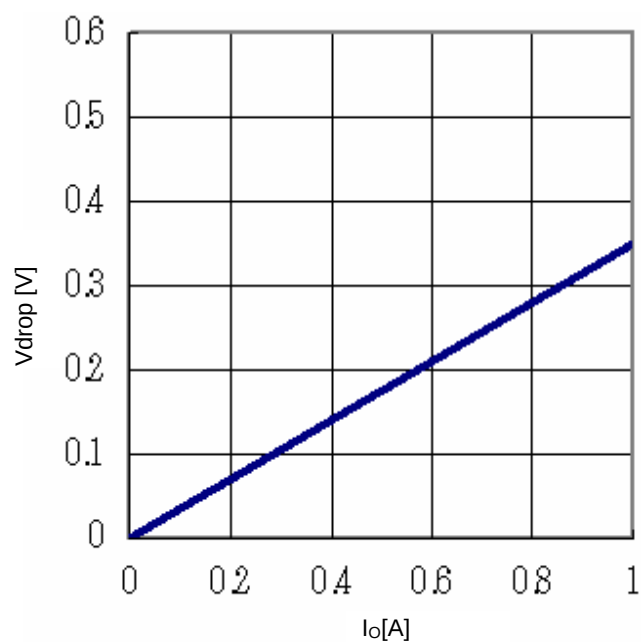
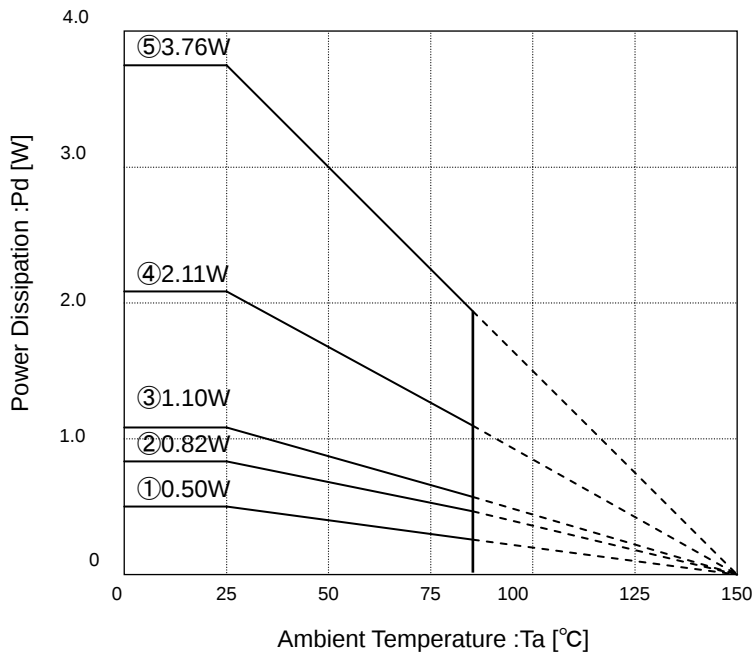


Fig.23  
Minimum dropout Voltage 4  
( $V_{CC}=8V$ ,  $T_a=25^{\circ}C$ )

# **Power Dissipation**

◎HTSOP-J8



Measurement condition: mounted on a ROHM board, and IC

Substrate size: 70mm × 70mm × 1.6mm  
(Substrate with thermal via)  
• Solder the thermal pad to Ground

- ① IC only  
 $\theta_{j-a}=249.5^{\circ}\text{C/W}$
- ② 1-layer (copper foil are :0mm × 0mm)  
 $\theta_{j-a}=153.2^{\circ}\text{C/W}$
- ③ 2-layer (copper foil are :15mm × 15mm)  
 $\theta_{j-a}=113.6^{\circ}\text{C/W}$
- ④ 2-layer (copper foil are :70mm × 70mm)  
 $\theta_{j-a}=59.2^{\circ}\text{C/W}$
- ⑤ 4-layer (copper foil are :70mm × 70mm)  
 $\theta_{j-a}=33.3^{\circ}\text{C/W}$

Thermal design should ensure operation within the following conditions. Note that the temperatures listed are the allowed temperature limits and thermal design should allow sufficient margin beyond these limits.

1. Ambient temperature  $T_a$  can be no higher than  $85^{\circ}\text{C}$ .
2. Chip junction temperature ( $T_j$ ) can be no higher than  $150^{\circ}\text{C}$ .

Chip junction temperature can be determined as follows:

Calculation based on ambient temperature ( $T_a$ )

$$T_j = T_a + \theta_{j-a} \times P$$

<Reference values>

|                                                                  |           |                                                     |
|------------------------------------------------------------------|-----------|-----------------------------------------------------|
| $\theta_{j-a}$ : HTSOP-J8                                        | 153.2°C/W | 1-layer substrate (copper foil density 0mm × 0mm)   |
|                                                                  | 113.6°C/W | 2-layer substrate (copper foil density 15mm × 15mm) |
|                                                                  | 59.2°C/W  | 2-layer substrate (copper foil density 70mm × 70mm) |
|                                                                  | 33.3°C/W  | 4-layer substrate (copper foil density 70mm × 70mm) |
| Substrate size: 70mm × 70mm × 1.6mm (substrate with thermal via) |           |                                                     |

Most of the heat loss that occurs in the BDxxHC0WEFJ series is generated from the output Pch FET. Power loss is determined by the total  $V_{CC}-V_O$  voltage and output current. Be sure to confirm the system input and output voltage as well as the output current conditions in relation to the heat dissipation characteristics of the  $V_{CC}$  and  $V_O$  in the design. Bearing in mind that heat dissipation may vary substantially depending on the substrate employed (due to the power package incorporated in the BDxxHC0WEFJ series) make certain to factor conditions such as substrate size into the thermal design.

$$\text{Power consumption [W]} = \{ \text{Input voltage (} V_{CC} \text{) - Output voltage (} V_O \text{)} \} \times I_O(\text{Ave})$$

Example) Where  $V_{CC}=5.0\text{V}$ ,  $V_O=3.3\text{V}$ ,  $I_O(\text{Ave}) = 0.1\text{A}$ ,

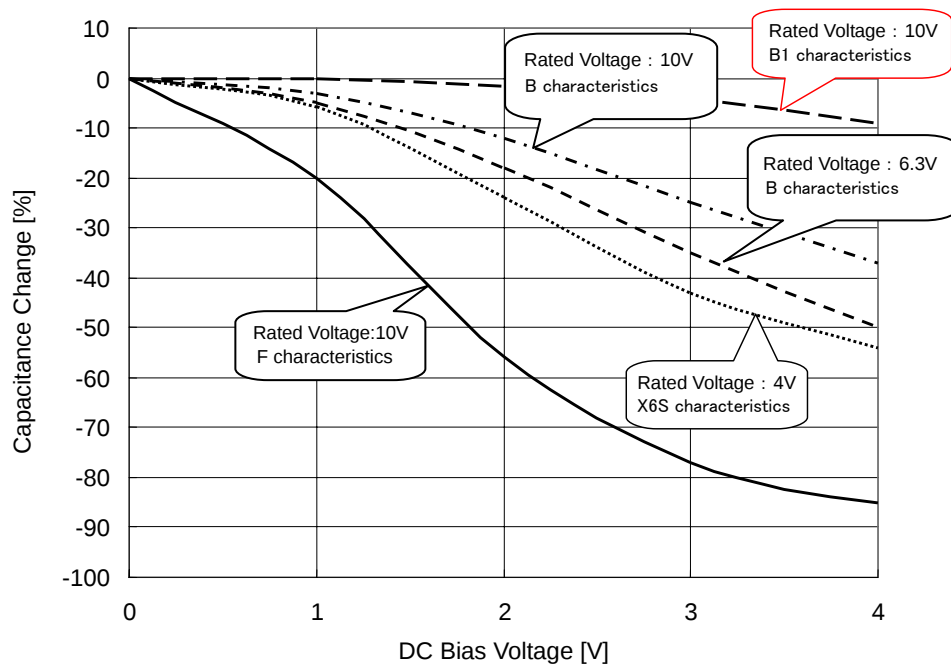
$$\text{Power consumption [W]} = \{ 5.0\text{V} - 3.3\text{V} \} \times 0.1\text{A}$$

$$=0.17[\text{W}]$$

### ●Input-to-Output Capacitor

It is recommended that a capacitor (over 1 $\mu$ F) is placed near pins between the input pin and GND as well as the output pin and GND. A capacitor, between input pin and GND, is valid when the power supply impedance is high or trace is long. Also, as for the capacitor between the output pin and GND, the greater the capacitance, the more sustainable the line regulation will be and the capacitor will make improvements of characteristics depending on the load. However, please check the actual functionality of this part by mounting it on a board for the actual application. Ceramic capacitors usually have different, thermal and equivalent series resistance characteristics, and moreover capacitance decreases gradually in use.

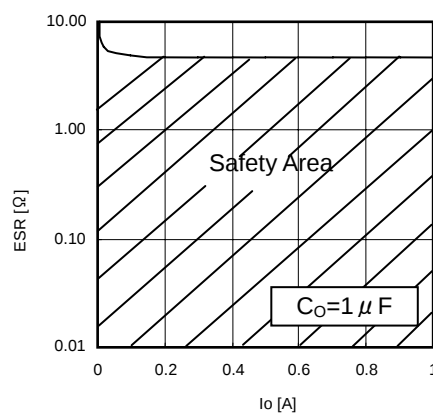
For additional details, please check with the manufacturer, and select the best ceramic capacitor for your application.



Ceramic capacitor capacity – DC bias characteristics  
(Characteristics example)

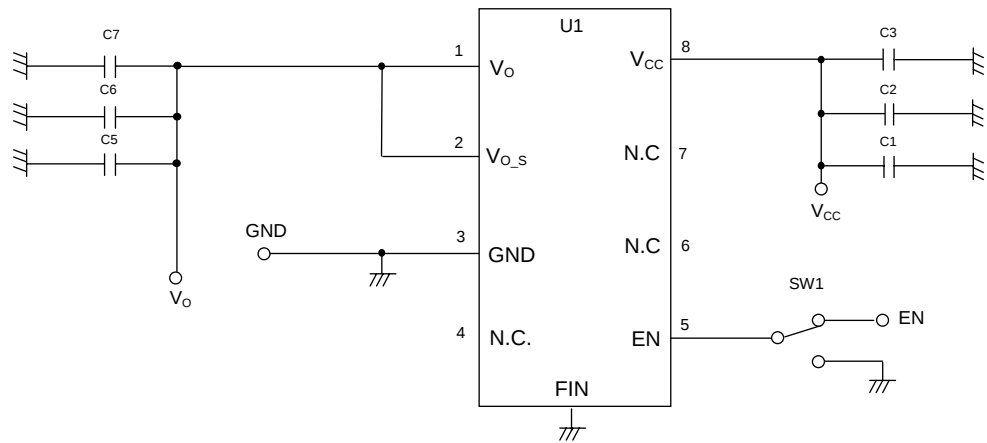
### ●Equivalent Series Resistance ESR (Output capacitor)

To prevent oscillations, please attach a capacitor between  $V_O$  and GND. Capacitors usually have ESR (Equivalent Series Resistance). Operation will be stable in the ESR- $I_O$  range shown to the right. Ceramic, tantalum and electrolytic Capacitors have different ESR values, so please ensure that you are using a capacitor that operates in the stable operating region shown on the right. Finally, please evaluate in the actual application.



ESR –  $I_O$  characteristics

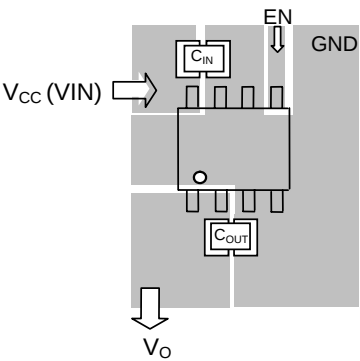
●Evaluation Board Circuit



●Evaluation Board Parts List

| Designation | Value | Part No.      | Company | Designation | Value | Part No.      | Company |
|-------------|-------|---------------|---------|-------------|-------|---------------|---------|
| C1          | 1μF   | CM105B105K16A | KYOCERA | C5          | 1μF   | CM105B105K16A | KYOCERA |
| C2          | -     | -             | -       | C6          |       |               |         |
| C3          | -     | -             | -       | C7          | -     | -             | -       |
| C4          | -     | -             | -       | U1          | -     | BDxxHC0WEFJ   | ROHM    |

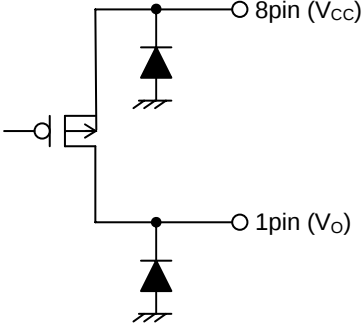
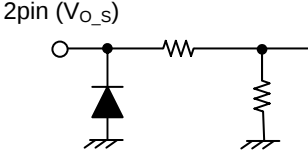
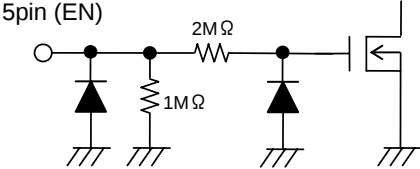
●Board Layout



PCB layout considerations:

- Input capacitor  $C_{IN}$  connected to  $V_{CC}$  ( $V_{IN}$ ) should be placed as close to  $V_{CC}$  ( $V_{IN}$ ) pin as possible. Output capacitor  $C_{OUT}$  also should be placed close to IC pin as possible. In case connected to inner layer GND plane, please use several through hole.
- $V_{O\_S}$  pin has comparatively high impedance, and can be affected by noise, so stray capacitance should be as small as possible. Please take care of this during layout.
- Please make GND pattern wide enough to handle thermal dissipation.

●I/O Equivalent Circuits

| 8pin (V <sub>CC</sub> ) / 1pin (V <sub>O</sub> )                                  | 2pin (V <sub>O_s</sub> )                                                          | 5pin (EN)                                                                           |
|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
|  |  |  |

## ● Operational Notes

### (1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the device, thus making it impossible to identify the damage mode, such as a short circuit or an open circuit. If there is any possibility of exposure over the rated values, please consider adding circuit protection devices such as fuses.

### (2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage the IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

### (3) Power supply lines

Design the PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and GND terminal. When using electrolytic capacitors in a circuit, note that capacitance values are reduced at low temperatures and over time.

### (4) GND voltage

The potential of the GND pin must be minimum potential under all operating conditions.

### (5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

### (6). Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

### (7). Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

### (8). ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

### (9). Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

|             | TSD ON Temperature[°C] (typ.) | Hysteresis Temperature [°C] (typ.) |
|-------------|-------------------------------|------------------------------------|
| BDxxHC0WEFJ | 175                           | 15                                 |

### (10). Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

## (11). Regarding input pin of the IC

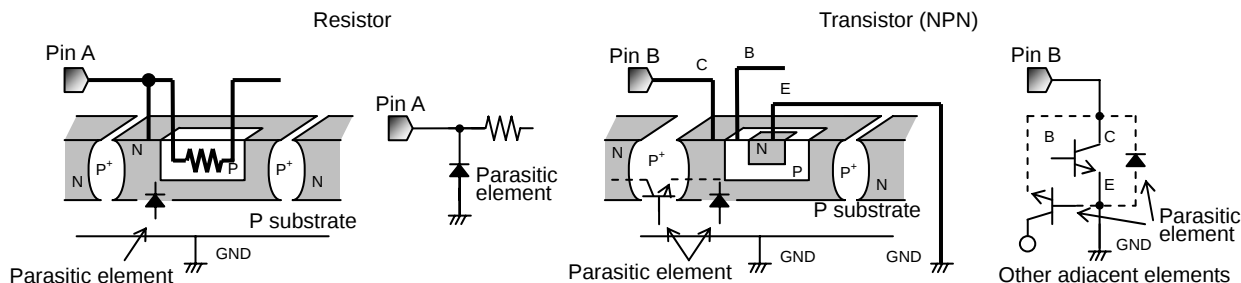
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When  $GND > Pin\ A$  and  $GND > Pin\ B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin\ B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC.

The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

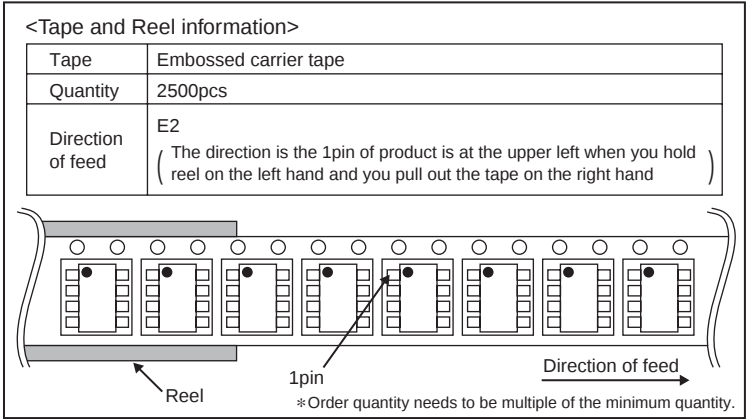
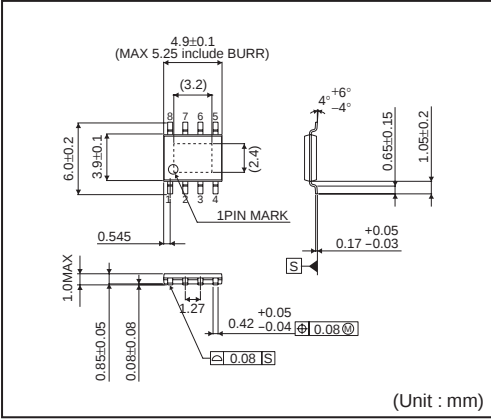


## (12). Ground Wiring Pattern.

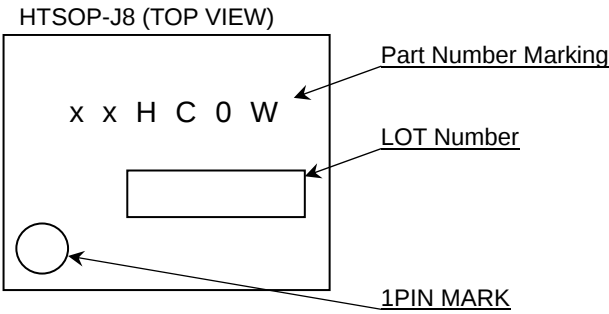
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

●Physical Dimension Tape and Reel Information

HTSOP-J8



●Marking Diagram



| xx | Product Name |
|----|--------------|
| 15 | BD15HC0WEFJ  |
| 18 | BD18HC0WEFJ  |
| 25 | BD25HC0WEFJ  |
| 30 | BD30HC0WEFJ  |
| 33 | BD33HC0WEFJ  |
| 50 | BD50HC0WEFJ  |
| 60 | BD60HC0WEFJ  |
| 70 | BD70HC0WEFJ  |

## ●Revision History

| Date        | Revision | Changes                       |
|-------------|----------|-------------------------------|
| 24.Aug.2012 | 001      | New Release                   |
| 28.Dec.2012 | 002      | The description was modified. |

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  - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - [f] Sealing or coating our Products with resin or other coating materials
  - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - [h] Use of the Products in places subject to dew condensation
- 4) The Products are not subject to radiation-proof design.
- 5) Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6) In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse) is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
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- 8) Confirm that operation temperature is within the specified range described in the product specification.
- 9) ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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- 1) When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- 2) In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
- 2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
- 3) Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4) Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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