WCFS1016V1C

64K x 16 Static RAM

Features

- 3.3V operation (3.0V–3.6V)
- High speed
  - — t_{AA} = 12 ns
- CMOS for optimum speed/power
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Available in 400-mil SOJ

Functional Description

The WCFS1016V1C is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

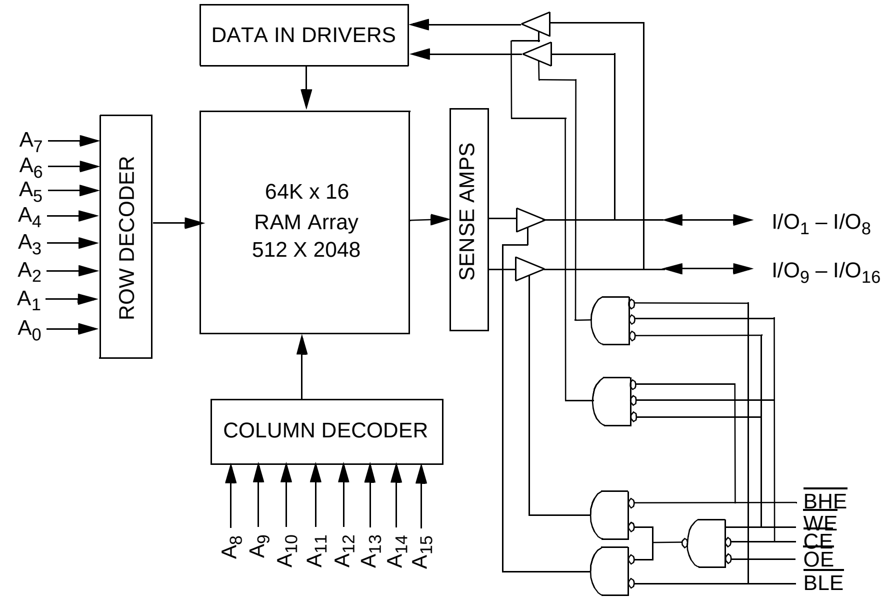
Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O_9 to I/O_{16}. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (CE LOW, and WE LOW).

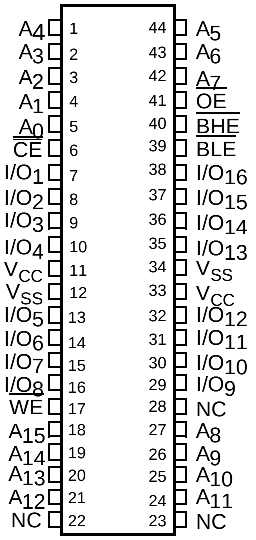
The WCFS1016V1C is available in 400-mil-wide SOJ packages.

Logic Block Diagram



Pin Configurations

SOJ
Top View



Selection Guide

	WCFS1016V1C-12
Maximum Access Time (ns)	12
Maximum Operating Current (mA)	150
Maximum CMOS Standby Current (mA)	5

Revised April 19, 2002

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied..–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .... –0.5V to +4.6V

DC Voltage Applied to Outputs
in High Z State[1] ....–0.5V to V_{CC}+0.5V

DC Input Voltage[1]..................................–0.5V to V_{CC}+0.5V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage..>2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current..>200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	3.3V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	WCFS1016V1C 12ns		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}+ 0.3V	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	–1	+1	µA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = $f_{MAX} = 1/t_{RC}$		150	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}		40	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC}$ – 0.3V, $V_{IN} \geq V_{CC}$ – 0.3V, or $V_{IN} \leq$ 0.3V, f = 0		5	mA

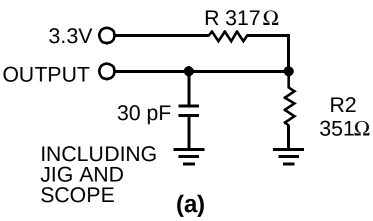
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance		8	pF

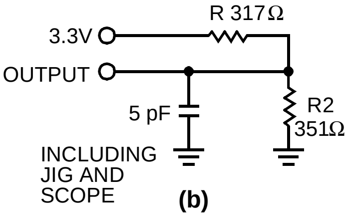
Note:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. T_A is the “instant on” case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.

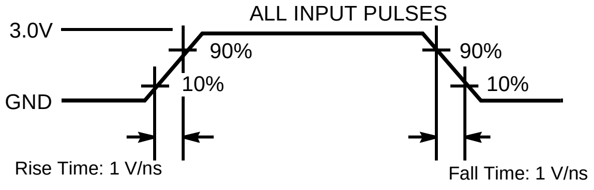
AC Test Loads and Waveforms



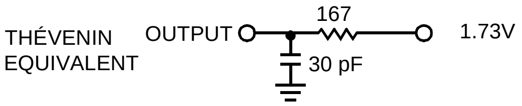
(a)



(b)



Equivalent to:



Switching Characteristics[4] Over the Operating Range

Parameter	Description	WCFS1016V1C 12ns		Unit
		Min.	Max.	
READ CYCLE				
t_{RC}	Read Cycle Time	12		ns
t_{AA}	Address to Data Valid		12	ns
t_{OHA}	Data Hold from Address Change	3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5, 6]		6	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]		6	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12	ns
t_{DBE}	Byte Enable to Data Valid		6	ns
t_{LZBE}	Byte Enable to Low Z	0		ns
t_{HZBE}	Byte Disable to High Z		6	ns
WRITE CYCLE[7]				
t_{WC}	Write Cycle Time	12		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	9		ns
t_{AW}	Address Set-Up to Write End	8		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		ns
t_{SD}	Data Set-Up to Write End	6		ns
t_{HD}	Data Hold from Write End	0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]		6	ns
t_{BW}	Byte Enable to End of Write	8		ns

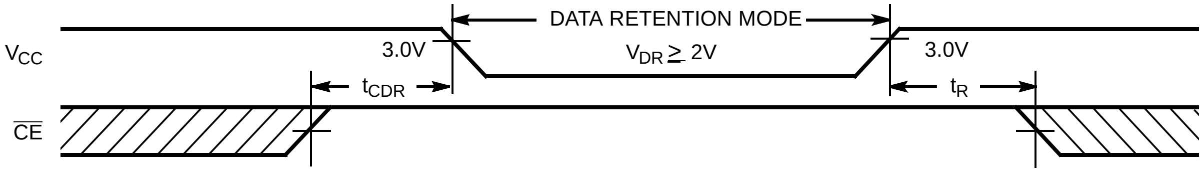
Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions[8]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
t_{CDR}[9]	Chip Deselect to Data Retention Time	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
t_R[10]	Operation Recovery Time		t_{RC}		ns

Notes:

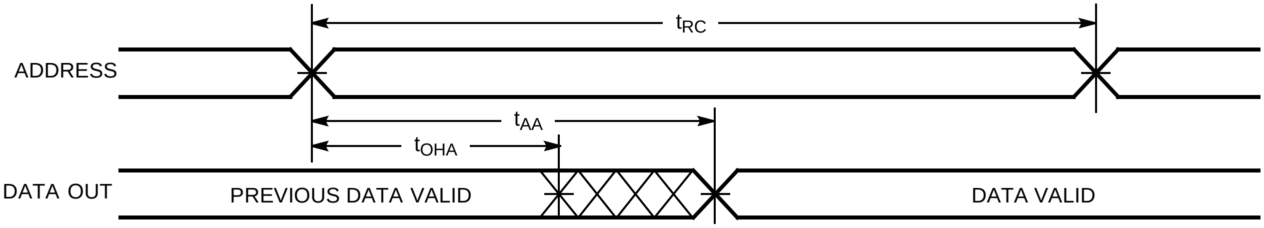
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}$ / $\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}$ / $\overline{BLE}$ must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
8. No input may exceed V_{CC} + 0.5V.
9. Tested initially and after any design or process changes that may affect these parameters.
10. $t_r \leq 3$ ns for the -12 and -15 speeds. $t_r \leq 5$ ns for the -20 and slower speeds.

Data Retention Waveform

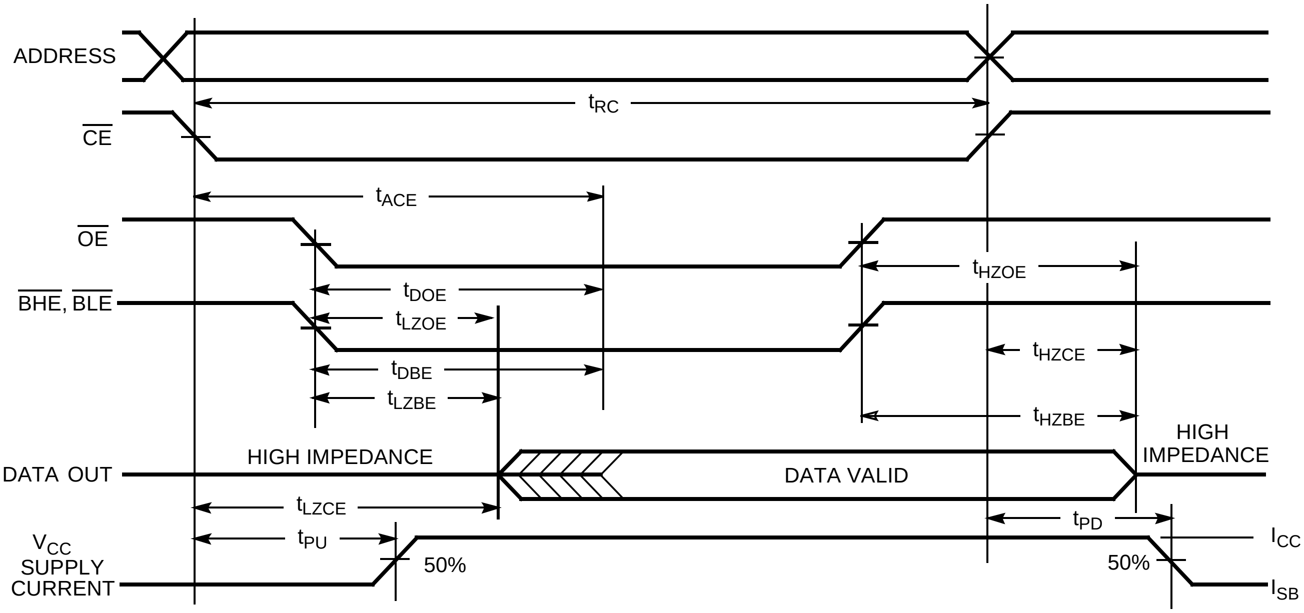


Switching Waveforms

Read Cycle No. 1[11, 12]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[12, 13]

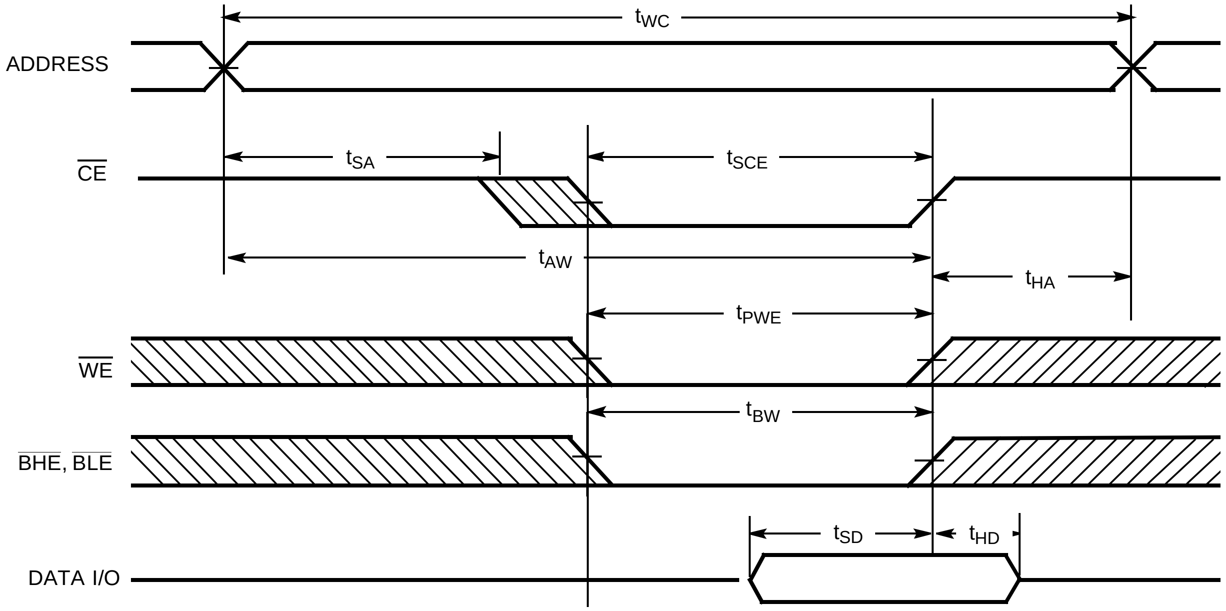


Notes:

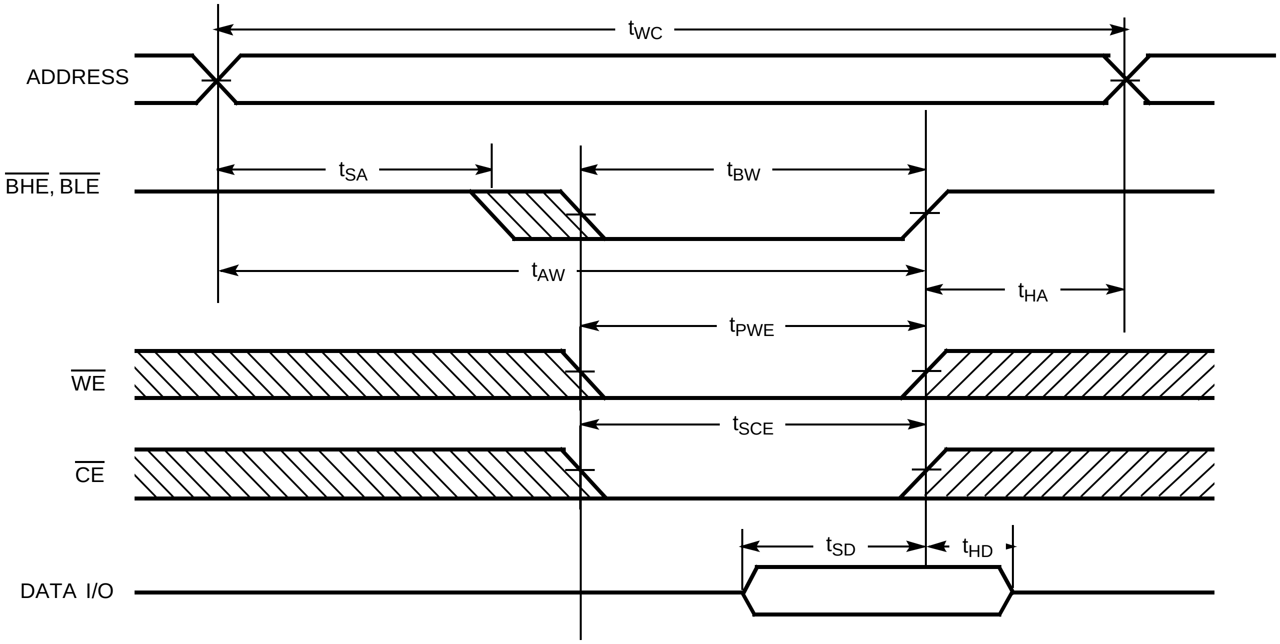
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BHE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled) [14, 15]



Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)

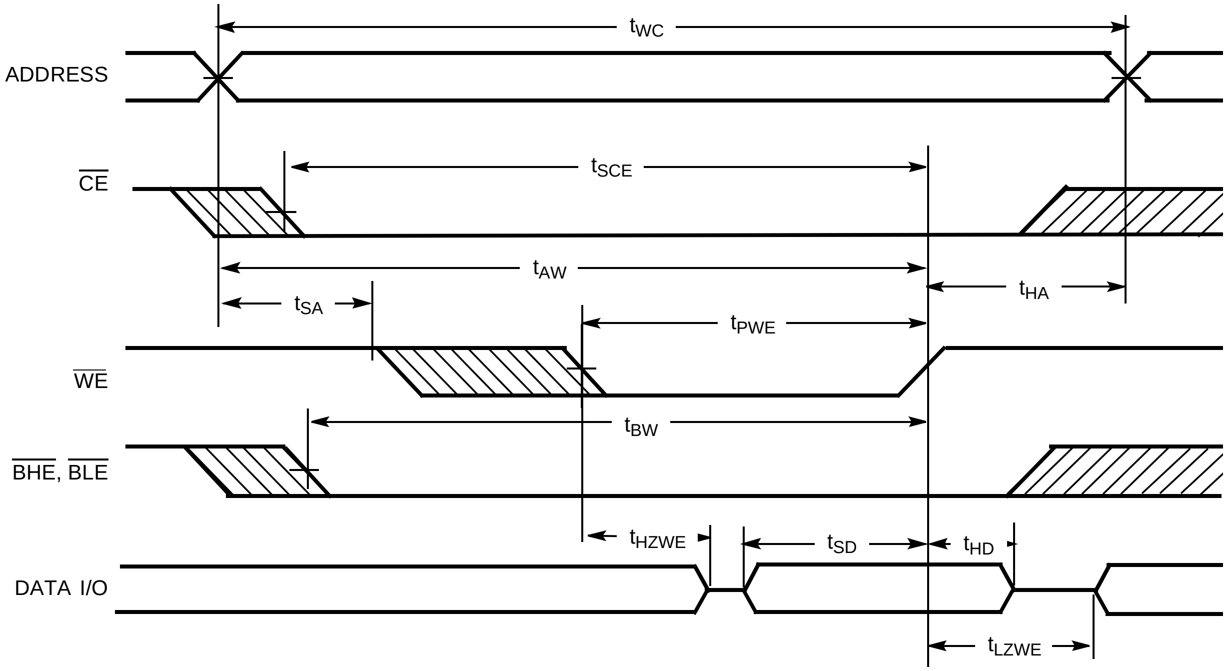


Notes:

14. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$= V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, LOW)



Truth Table

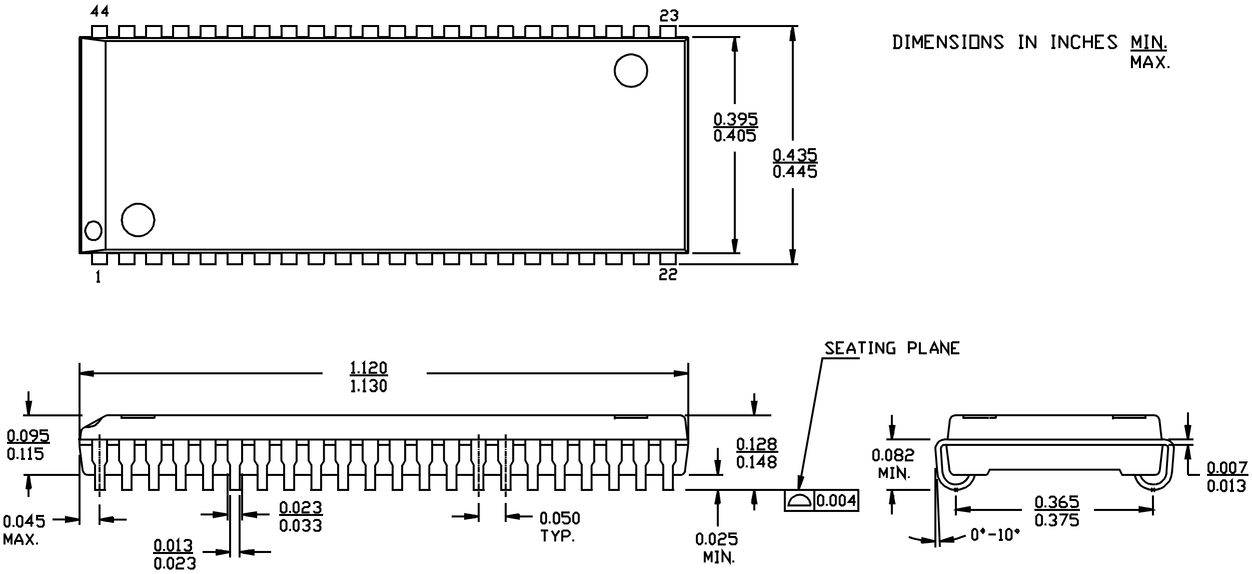
$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O_1–I/O_8	I/O_9–I/O_{16}	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read - Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read - Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write - All bits	Active (I_{CC})
			L	H	Data In	High Z	Write - Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write - Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	WCFS1016V1C-JC12	J	44-Lead (400-Mil) Molded SOJ	Commercial

Package Diagrams

44-Lead (400-Mil) Molded SOJ J



Document Title: WCFS1016V1C 64K x 16 Static RAM			
REV.	**Issue Date**	**Orig. of Change**	**Description of Change**
**	4/19/02	XFL	NEW DATASHEET

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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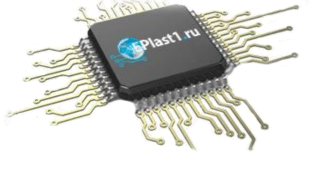
- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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