2/3/4-PHASE PWM CONTROLLER WITH DYNAMIC VOLTAGE & FREQUENCY SCALING

IDTP62000

Description

The IDTP62000 is a multiphase interleaved synchronous buck controller ideal for personal computer applications where high efficiency and high power density are required. It contains three integrated MOSFET driver pairs to enable a 3-phase regulator solution that allows load currents up to 150A for low voltage microprocessor power requirements. It also provides a 4th PWM output phase to drive a low cost IDTP67111 single phase driver to become a full 4 phase solution.

The VID logic can be configured for applications compliant to the Intel VR11.1, Intel VR10 or AMD PVI/SVI specifications.

The maximum number of operating phases (2/3/4) is pin programmable, and depending on output loading conditions, the active number of phases can be dynamically reduced. The Dynamic Efficiency Control (DEC) feature enables all configured phases when full current output is required, and dynamically reduces the number of active phases at reduced current levels. Combined with Dynamic Voltage Change (DVC) and Dynamic Frequency Change (DFC) this allows full output current while also providing for more efficient operation at lower power output.

The design allows a positive or negative offset to the VID voltage being used for regulation and supports both external, resistor based, and internal, register based, programming of this offset voltage.

An internal soft start (SS) is included in the design to prevent large inrush currents at power on. The ramp rate of the soft start can be adjusted with an external resistor.

A DCR current sensing method combined with rapid transient response architecture enables superior phase current matching, accurate current limit and precise load-line control. Furthermore, this device incorporates a proprietary scheme for fast and accurate transient-response performance, as well as precise load sharing.

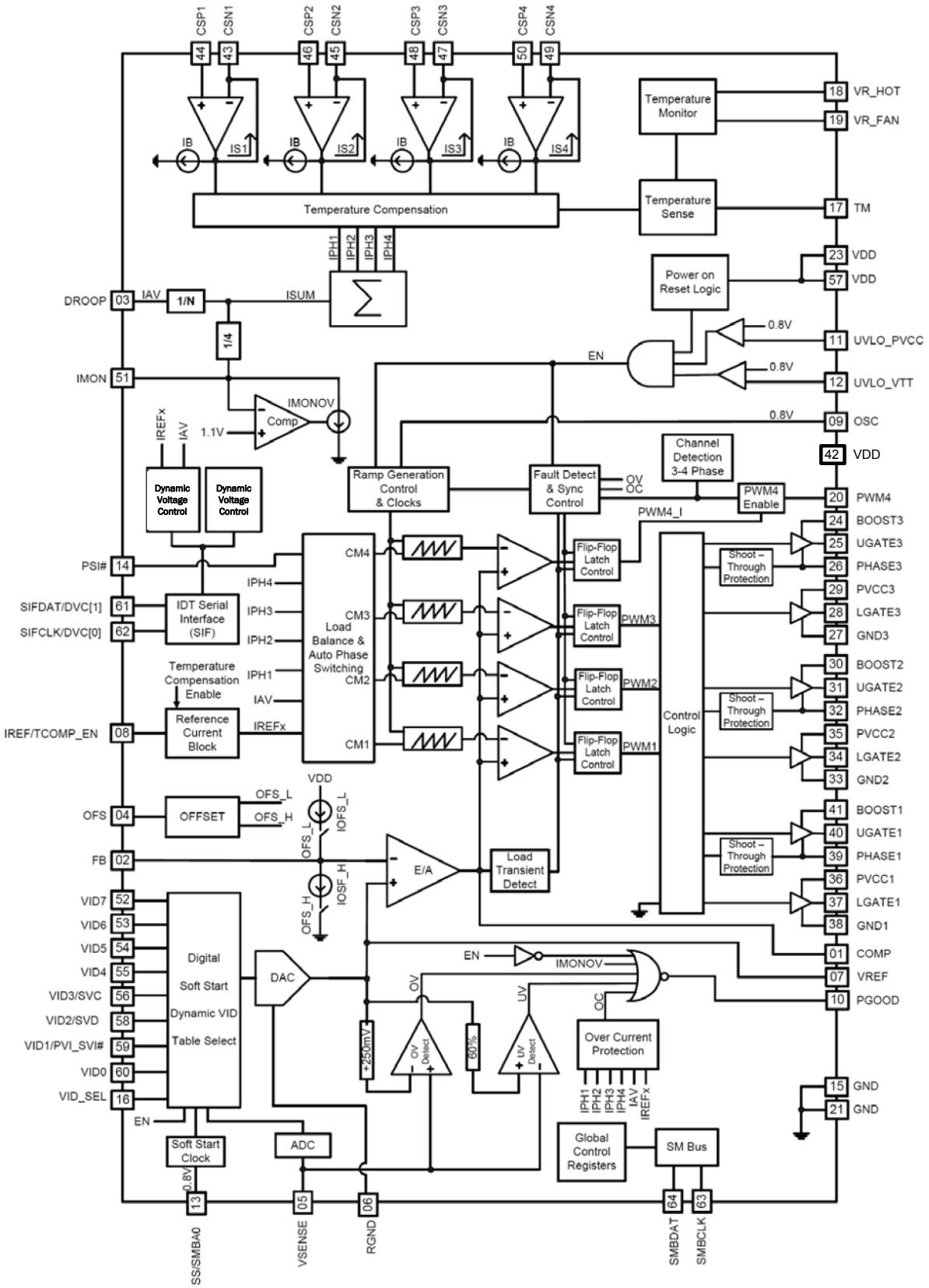
Features

- **Proprietary Dynamic Voltage & Frequency Scaling providing efficiency and performance optimization**
  - **– Dynamic Voltage Change (DVC) as a standalone capability**
  - **– Dynamic Frequency Change (DFC) when combined with 9CPS4592 clock generator**
  - **– SIF interface to communicate with clock sub-system**
- **Dynamic Efficiency Control (DEC) for improved efficiency at light loads**
- Intel VR11.1, Intel VR10 or AMD PVI/SVI operating modes
- Three integrated drivers with additional fourth phase PWM output
- 2, 3 or 4-phase operation with automatic selection at power-on
- Ability to communicate with the clock subsystem using a Serial Interface (SIF)
- User configurability through SMBus
- Overshoot and Undershoot transient suppression
- Adjustable operating frequency (up to 1 MHz per phase)
- Pb Free, RoHS compliant 64-pin QFN-64 package

Applications

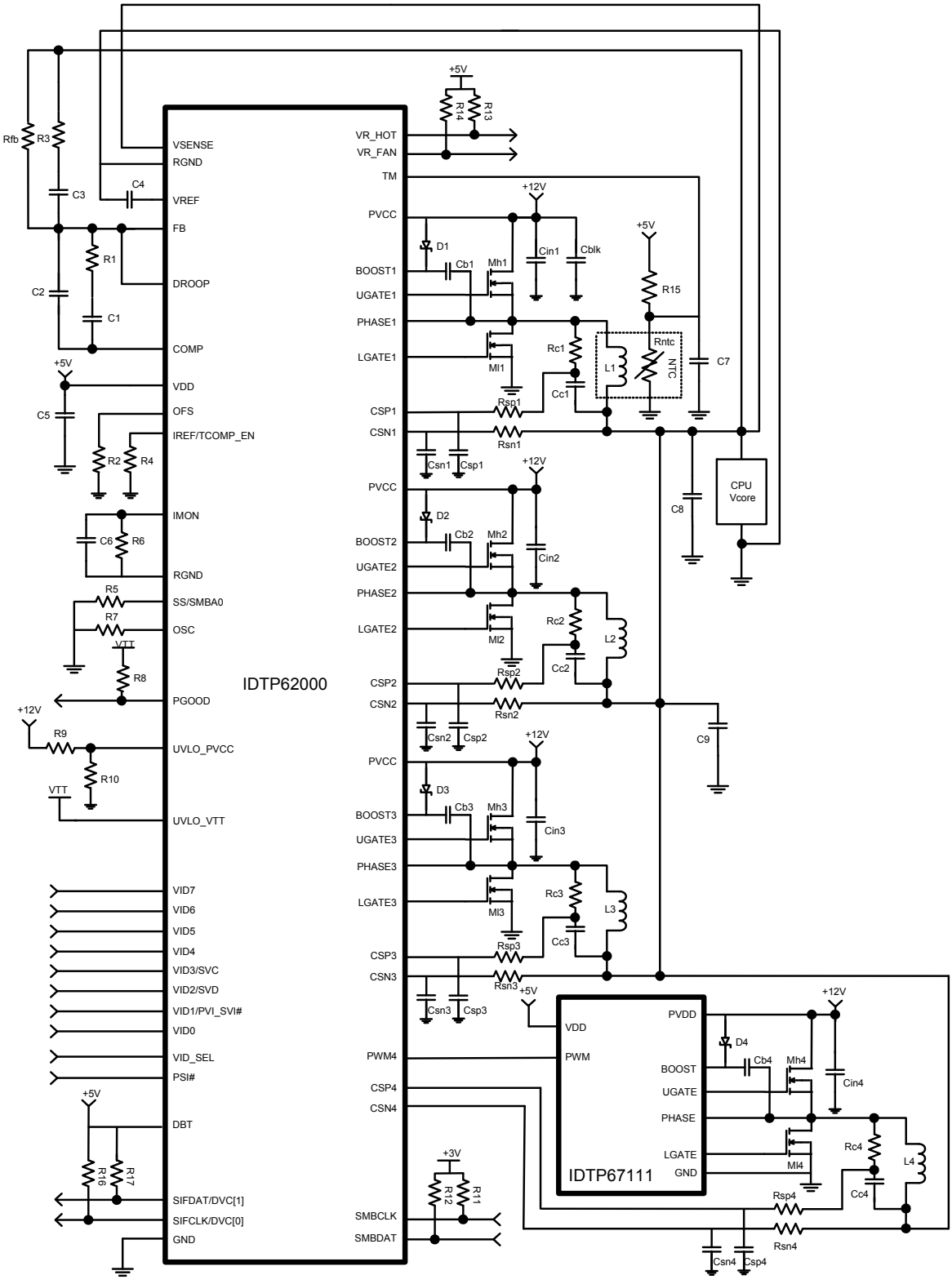
- Gaming Machine
- Server, Workstations
- All-in-one LCD PCs
- Voltage Regulator Modules

Block Diagram



Applications Information

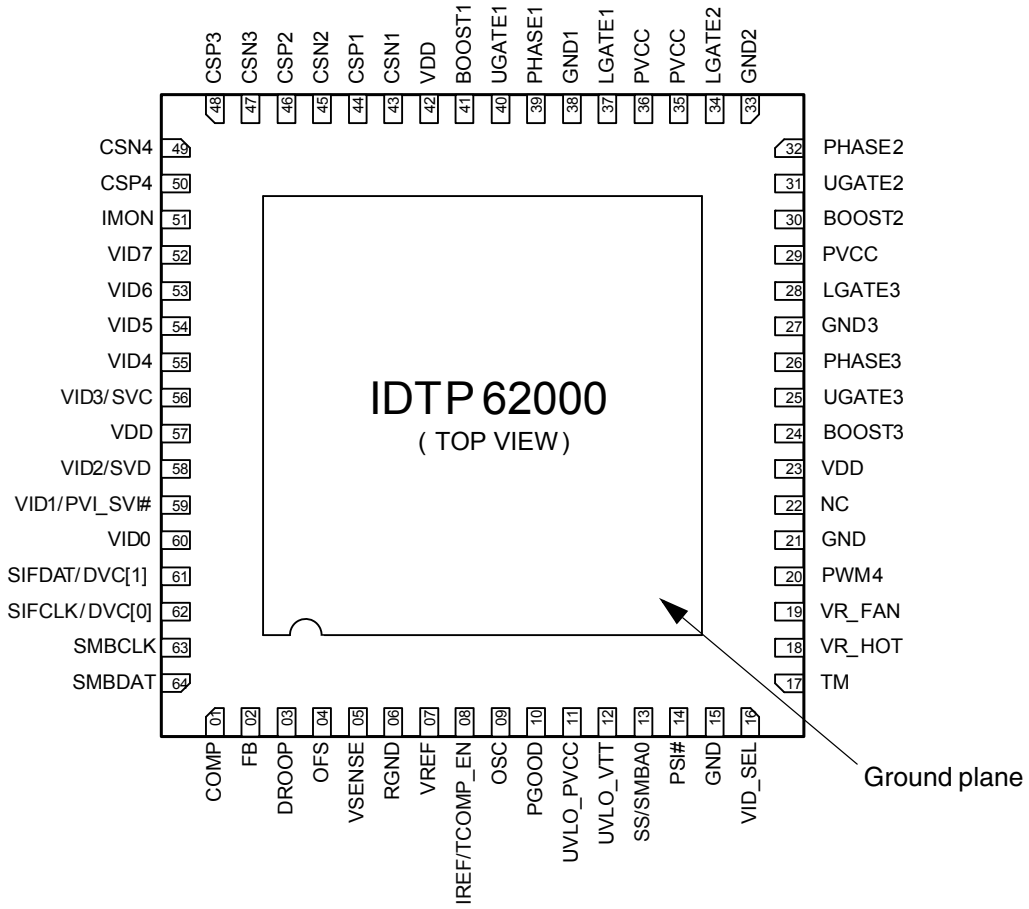
Figure: 4-Phase Applications Reference Circuit



4-Phase Component Values

Component	Pin	Value	Package	Description
R1	FB, COMP	10k	0603	10kΩ 1% Resistor
R2	OFS	52k	0603	52kΩ 1% Resistor
R3	FB	500	0603	500Ω 1% Resistor
Rfb	FB	2.5k	0603	2.5kΩ 1% Resistor
R4	IREF/TCOMP_EN	40.2k	0603	40.2kΩ 1% Resistor
R5	SS/SMBA0	100k	0603	100kΩ 1% Resistor
R6	IMON	22.6k	0603	22.6kΩ 1% Resistor
R7	OSC	82k	0603	82kΩ 1% Resistor
R8	PGOOD	1k	0603	5kΩ 5% Resistor
R9	UVLO_PVCC	27k	0603	27kΩ 1% Resistor
R10	UVLO_PVCC	3.01k	0603	3.01kΩ 1% Resistor
R11	SMCLK	4.7k	0603	4.7kΩ 5% Resistor
R12	SMBDAT	4.7k	0603	4.7kΩ 5% Resistor
R13	VR_HOT	1k	0603	1kΩ 5% Resistor
R14	VR_FAN	1k	0603	1kΩ 5% Resistor
R15	TM	1k	0603	1kΩ 1% Resistor
R16	SIFCLK	Do not populate	0603	
R17	SIFDAT	Do not populate	0603	
Rntc	TM	R_{25C} = 6.8kΩ	0805	Vishay 6.8kΩ 3% NTC Thermistor, Beta = 3477
Rc1, Rc2, Rc3, Rc4	PHASEx, CSPx	6k	0603	6kΩ 1% Resistor
Rsp1. Rsp2, Rsp3, Rsp4	PHASEx, CSPx	625	0603	625Ω 1% Resistor
Rsn1. Rsn2. Rsn3. Rsn4	CSNx	625	0603	625Ω 1% Resistor
C1	FB, COMP	2n	0603	2nF 10V X7R Ceramic capacitor
C2	FB, COMP	36p	0603	36pF 10V NPO Ceramic capacitor
C3	FB	0.5n	0603	0.5nF 10V NPO Ceramic capacitor
C4	VREF	1n	0603	1nF 10V X7R Ceramic capacitor
C5	VDD	1µ (x2)	0603	1µF 10V X5R Ceramic capacitor
C6	IMON	20n	0603	20nF 10V X7R Ceramic capacitor
C7	TM	Do not populate	0603	
C8	vcore	820µF (x12) = 9,840µF	Radial Capacitor	
C9	vcore	22µF (x18) = 396µF	0805	X5R 25V Ceramic capacitor
Cb1, Cb2, Cb3, Cb4	BOOSTn	1µ	0603	1µF X5R 25V Ceramic capacitor
Cc1, Cc2, Cc3, Cc4	CSPn	0.1µ	0603	0.1µF 10V X7R Ceramic capacitor
Csn1, Csn2, Csn3, Csn4	CSNn	36p	0603	X7R 10V Ceramic capacitor
Csp1, Csp2, Csp3, Csp4	CSPn	36p	0603	X7R 10V Ceramic capacitor
Cin1, Cin2, Cin3, Cin4	PVDD	4.7µ (x2 per Mh1-Mh4 mosfet = 8 total)	0805	4.7µF X5R 25V Ceramic capacitor
cblk		470µ (x2) = 940 µF	Radial Capacitor	470µF 16V
L1, L2, L3, L4	PHASEn	0.6µ	Through hole	0.60µH 35A 1.0mΩ DCR Inductor
Mh1, Mh2, Mh3, Mh4	PHASEn	P0903BDG	TO-252	Upper Drive Mosfet
MI1, MI2, MI3, MI4	PHASEn	P75N02LDG	TO-252	Lower Drive Mosfet
D1 - D4		BAT54A	SOT-23	Schottky Bootstrap Diode

Pin Assignment



64 Pin VFQFP-64 (9x9 mm)

Pin Types

I/O Type	Description
A-I, A-O & A-IO	Analog Levels: Input, Output & Input/Output
D-I, D-O	Digital Levels: Input, Output. Voltage levels are all digital levels
GND	Ground: Any connection to Ground
GP-IN, GP-OUT, GPIO	General Purpose: Input, Output, Input/Output. Inputs are 3.3 V (5 V tolerant) Outputs are open-drain capable
I2C-I, I2C-O & I2CIO	I²C: Input, Output & Input/Output Inputs are CMOS Outputs are open-drain capable.
P-I, P-O	Power Supply: Input, Output

Pin Descriptions

Pin #	Pin Name	Pin Type	Pin Description
1	COMP	A-I/O	Connected to the internal error amplifier. It is used with the FB pin to compensate the error amplifier. It is the output of the error amplifier.
2	FB	A-I/O	Negative input terminal to the internal differential error amplifier. It is used with the COMP pin to compensate the error amplifier.
3	DROOP	A-I/O	A current proportional to the total output current is sourced from this pin. Connecting this pin to FB allows the controller to compensate output voltage droop in the output.
4	OFS	A-I/O	The OFS pin provides a means to program a DC current for generating an offset voltage across the resistor between FB and VSENSE. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VDD. For no offset, the OFS pin should be left unconnected.
5	VSENSE	A-I	Connect directly to VCORE. It used only by the OVP and UVP blocks.
6	RGND	GND	Reference ground for the load, which is used for remote sensing to offset the internal DAC voltage.
7	VREF	A-O	Analog output of the DAC after the DAC voltage has been referenced to RGND.
8	IREF/TCOMP_EN	A-I/O	Dual purpose pin that is used to provide: 1.Internal accurate current reference (IREF) 2.Enable for sensed load current temperature compensation (TCOMP_EN) The reference current is provided by placing a resistor from the IREF pin to GND or VDD with an internally generated bandgap reference voltage of 0.8 V applied across it. Temperature compensation is enabled if the IREF resistor is tied to GND and it is disabled if the IREF resistor is tied to VDD.
9	OSC	A-I/O	A resistor from this pin to ground selects the nominal switching frequency of the regulator. Using 100 kΩ will result in a switching frequency of 250 kHz.
10	PGOOD	D-O	The PGOOD signal is an active high signal that indicates whether or not the controller is regulating the output voltage within the proper levels, and whether any fault conditions exist. During shutdown and soft-start the PGOOD signal is pulled low and will go high after the soft-start sequence completes and the output voltage is between the over-voltage and under-voltage limits. (approximately 1 ms after the end of soft-start). During an under-voltage, over-voltage, over-current condition or when the controller output enable UVLO_PVCC is pulled low, PGOOD will go low. Moreover, PGOOD will also be pulled low when a no-CPU VID (or OFF) code is selected or during any reset event.
11	UVLO_PVCC	A-I	Pin should be externally connected to a resistor divider between PVCC and GND. It is used to detect that the PVCC level has come up. When the voltage at the pin rises above its threshold (0.8V) then the internal power on reset is released provided that the internal VDD based POR level has been also reached. It is recommended that the user bias this pin with a resistor divider that generates the POR threshold voltage when PVCC is at 2/3 of its maximum value.
12	UVLO_VTT	A-I	Another threshold-sensitive enable input for the controller. It's typically connected to the VTT output of the VTT voltage regulator in the computer mother board.
13	SS/SMBA0	A-I/O	Multiple purpose pin. One of its functions is to set the soft start ramp slope for the Intel DAC modes of operation by a resistor connected to ground. The pin also determines the value of the SMBus address A0 bit. The A0 logic level is determined by the level on this pin at power up. If the resistor is connected to VDD, the A0 bit is set to high. If the resistor is connected GND, the A0 bit is set to low.
14	PSI#	A-I	The power state indicator mode pin (PSI#) is a logical input to initiate a phase dropping scheme for higher efficiency at light load. The input conforms to the 1.2 V CMOS levels defined in the VRD11.1 specification (nominally 1.2v high, 0v low).

Pin #	Pin Name	Pin Type	Pin Description
15	GND	GND	System Ground. IC reference and bias ground.
16	VID_SEL	D-I	Select pin for the different VID modes. For VR10, this signal needs to be grounded. For VR11.1, the signal needs to be floating (>0.8 V and <1.8 V). For AMD PVI/SVI compliance the pin needs to be tied high (>1.8 V).
17	TM	A-I	Thermal monitor input pin. Its input is connected to a negative thermal coefficient (NTC) thermistor network to set the temperature thresholds for VR_HOT and VR_FAN. The TM pin is also for internal temperature compensation.
18	VR_HOT	D-O	Over-temperature alarm signal logical output. Signal is active high when the TM pin (thermal monitor) passes a set threshold. This pin is open-drain.
19	VR_FAN	D-O	Over-temperature warning signal logical output. Signal is active high when the TM pin (thermal monitor) passes a set threshold. This pin is open-drain.
20	PWM4	A-I/O	Dual function pin. In normal operation, it will act as the pulse width modulated 3-stateable output signal for an external fourth channel driver. On power-up, this pin will also act as a 3-state input pin to select the number of required phases.
21	GND	GND	System Ground. IC reference and bias ground.
22	NC	NC	No Connect
23	VDD	P-I	+5V (nominal) supply pin for “lower” voltage circuits.
24	BOOST3	P-I	Voltage supply for the upper power MOSFET gate drive. An external bootstrap capacitor is also required. An internal diode is connected to this pin for the bootstrap charge.
25	UGATE3	A-I/O	Connect this pin to the gate of upper power MOSFET 3
26	PHASE3	A-I/O	Return path for the corresponding upper power MOSFET gate driver for phase 3.
27	GND3	GND	Gate Driver 3 Ground.
28	LGATE3	A-I/O	Connect to the gates of lower power MOSFET 3.
29	PVCC	P-I	One of three supply input pins for the corresponding channel MOSFET drive. Connect to +12V supply.
30	BOOST2	P-I	Voltage supply for the upper power MOSFET gate drive. An external bootstrap capacitor is also required. An internal diode is connected to this pin for the bootstrap charge.
31	UGATE2	A-I/O	Connect this pin to the gate of upper power MOSFET 2.
32	PHASE2	A-I/O	Return path for the corresponding upper power MOSFET gate driver for phase 2.
33	GND2	GND	Gate Driver 2 Ground.
34	LGATE2	A-I/O	Connected this pin to the gates of lower power MOSFET 2.
35	PVCC	P-I	One of three supply input pins for the corresponding channel MOSFET drive. Connect to +12V supply.
36	PVCC	P-I	One of three supply input pins for the corresponding channel MOSFET drive. Connect to +12V supply.
37	LGATE1	A-I/O	Connected to the gates of lower power MOSFET 1.
38	GND1	GND	Gate Driver 1 Ground.
39	PHASE1	A-I/O	Return path for the corresponding upper power MOSFET gate driver for phase 1.
40	UGATE1	A-I/O	Connect this pin to the gate of upper power MOSFET 1.
41	BOOST1	P-I	Voltage supply for the upper power MOSFET gate drive. An external bootstrap capacitor is also required. An internal diode is connected to this pin for the bootstrap charge.
42	VDD	P-I	+5V (nominal) supply pin for “lower” voltage circuits.
43	CSN1	A-I	Phase 1 current sense - negative input.
44	CSP1	A-I	Phase 1 current sense - positive input.

Pin #	Pin Name	Pin Type	Pin Description
45	CSN2	A-I	Phase 2 current sense - negative input.
46	CSP2	A-I	Phase 2 current sense - positive input.
47	CSN3	A-I	Phase 3 current sense - negative input.
48	CSP3	A-I	Phase 3 current sense - positive input.
49	CSN4	A-I	Phase 4 current sense - negative input.
50	CSP4	A-I	Phase 4 current sense - positive input.
51	IMON	A-O	Total load current monitoring output pin. It is used with the PSI# to properly handle the dynamic phase switching for higher efficiency. IMON is limited to a max voltage of 1.1 V so as not to damage the CPU input.
52	VID7	D-I/O	The voltage identification pin VID7, connects to CPU. (See Note 1)
53	VID6	D-I/O	The voltage identification pin VID6, connects to CPU. (See Note 1)
54	VID5	D-I/O	The voltage identification pin VID5, connects to CPU. (See Note 1)
55	VID4	D-I/O	The voltage identification pin VID4, connects to CPU. (See Note 1)
56	VID3/SVC	D-I/O	The voltage identification pin VID3, connects to CPU. (See Note 1)
57	VDD	P-I	+5V (nominal) supply pin for “lower” voltage circuits.
58	VID2/SVD	D-I/O	The voltage identification pin VID2, connects to CPU. (See Note 1)
59	VID1/PVI_SVI#	D-I/O	The voltage identification pin VID1, connects to CPU. (See Note 1)
60	VID0	D-I/O	The voltage identification pin VID0, connects to CPU. (See Note 1)
61	SIFDAT/DVC[1]	I2C-O GP-OUT	Serial data output pin for the SIF bus. When in GPO mode, this pin serves as the DVC[1] logical output and requires a 4 kΩ pull-down resistor.
62	SIFCLK/DVC[0]	I2C-O GP-OUT	Serial clock output pin for the SIF bus. When in GPO mode, this pin serves as the DVC[0] logical output and requires a 4 kΩ pull-down resistor.
63	SMBCLK	A-I/O	Clock input pin for the system management bus and is compliant with the SMBus specification.
64	SMBDAT	A-I/O	Data input pin for the system management bus and is compliant with the SMBus specification.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDTP62000. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Rating	Units
Supply Voltage, VDD [Note 2]	-0.3 to 6	V
All Inputs and Outputs	GND -0.3 to VDD +0.3	V
Boost To Phase	15	V
Boost To Ground	30	V
ESD (HBM)	2000	V
Junction Temperature	0 to +150	°C
Storage Temperature	-65 to +150	°C
Soldering Temperature	260	°C

Note 2: If used in conjunction with a IDTP67111 single phase driver for the fourth phase, it must be powered with the same supply as the IDTP62000.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
VDD Power Supply Voltage (measured with respect to GND)	4.75	5	5.25	V
PVCC Power Supply Voltage (measured with respect to GND)	10.8	12	13.2	V
Power Supply Ramp-Up Time			4	ms
Ambient Operating Temperature	0		+70	°C
Junction Temperature	0		+100	°C

General I²C Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address $78_{(H)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledged**
- Controller (host) starts sending Byte **N through Byte N+X-1(note 2)**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address 78 (H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address $78_{(H)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledged**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address $79_{(H)}$
- IDT clock will **acknowledged**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address 78 (H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address 79 (H)			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not		
P	stoP bit		

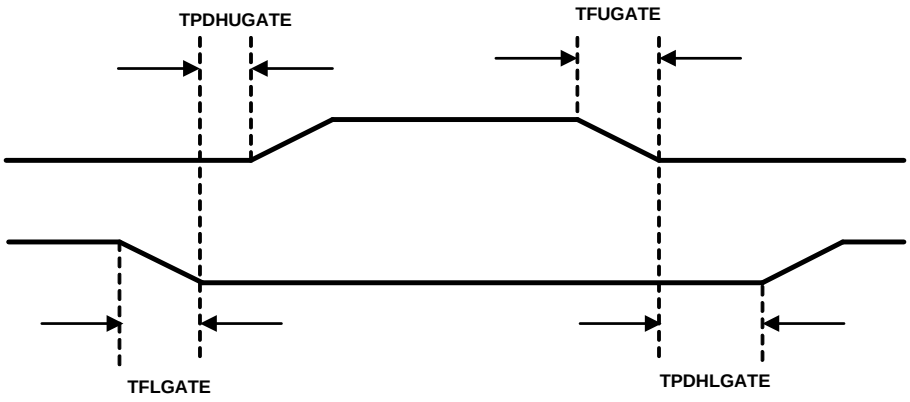
Power MOSFET Driver Electrical Characteristics

Table 1: MOSFET Driver Characteristics

Unless stated otherwise, VDD = 5.0 V ± 5 %, Junction Temperature = 0 to +100 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Current						
PVCC Quiescent Curr.	IPVCC	Switching frequency = 250 kHz (12V input pins)		30		mA
Power-On Reset						
POR threshold	PVCCRTH	PVCC Rising		6.4	6.5	V
Hysteresis	PVCCHYS			80	200	mV
Gate Output						
Output Resistance		UGATE Source 15 mA	1.25	2.0	3.0	Ω
		UGATE Sink 15 mA	0.9	1.65	3.0	Ω
		LGATE Source 15 mA	0.85	1.25	2.2	Ω
		LGATE Sink 15 mA	0.60	0.80	1.35	Ω
Output Switching Time						
UGATE Fall Time	TFUGATE	VPVCC = 12V, 3 nF load, 10% - 90%		40		ns
LGATE Fall Time	TFLGATE	VPVCC = 12V, 3 nF load, 10% - 90%		25		ns
UGATE Turn-On Non-Overlap	TPDHUGATE	VPVCC = 12V, 3 nF load		18		ns
LGATE Turn-On Non-Overlap	TPDHLGATE	VPVCC = 12V, 3 nF load		18		ns
Bootstrap diode						
Reverse Leakage		At 12 V		0.1		µA
Forward Voltage Drop		At 10 mA		0.7		V
Over-voltage Protection						
Trip Voltage		Enter OVP (VCC=12 V)		3.6		V
		Exit OVP (PVCC=12 V)		0.75		V

Figure 1: Output Switching TImes



Controller Electrical Characteristics

Unless stated otherwise, VDD = 5.0 V ± 5 %, Junction Temperature = 0 to +100 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Current						
IDDQ	IVDD	PWM 1,2,3 open (5V input pins)		18	25	mA
Power-On Reset						
POR threshold	VDDRTH	VDD Rising	4.1	4.2	4.3	V
	VDDFTH	VDD Falling		3.8		V
Hysteresis	VDDHYS			0.5		V
UVLO_PVCC Rising Threshold			0.76	0.8	0.84	V
UVLO_PVCC Hysteresis				65		mV
UVLO_VTT Rising Threshold			0.76	0.8	0.84	V
UVLO_VTT Hysteresis				65		mV
Master Oscillator						
Frequency Accuracy	F_{SW}	Rosc = 100 kΩ ± 0.1%	225	250	275	kHz
Adjustment Range of Switching Frequency	F_{SWAR}		100		1000	kHz
OSC Voltage	V_{OSC}		0.76	0.8	0.84	V
Ramp Generator						
Ramp Amplitude	V_{RA}			2.4		V
Max PWM Duty Cycle	DC_{PWM}		90			%
Reference and DAC						
System Accuracy (1.000V - 1.600V)			-0.5		+0.5	%
System Accuracy (0.800V - 1.000V)			-1.0		+1.0	%
System Accuracy (0.5V - 0.800)			-2.0		+2.0	%
VID Input Low Voltage (VR10, VR11.1)	V_{ILVIDI}		-0.3		0.3	V
VID Input High Voltage (VR10, VR11.1)	V_{IHVIDI}		0.8		VDD + 0.3	V
OFS Source Current Accuracy (Negative Offset)	I_{OFFSET}	R_{OFS} = 10 kΩ from OFS to GND	37.0	40.0	43.0	µA
OFS Sink Current Accuracy (Positive Offset)	I_{OFFSET}	R_{OFS} = 30 kΩ from OFS to VDD	50.5	53.5	56.5	µA
OFS Range		± 10% Accuracy at limits of range	-150		150	µA
VID Input Pull-up to 1.2V (Intel)	I_{VID}	Input = 0.0V		30	50	µA
Current Reference						
IREF Current	I_{REF}	R_{IREF} = 40 kΩ ±1% from IREF to GND	19	20	21	µA
IREF Current Range	I_{REF-R}		19.0	20.0	33.6	µA
IREF Voltage	V_{IREFL}	R_{IREF} = 40 kΩ from IREF to GND	0.76	0.8	0.84	V
	V_{IREFH}	R_{IREF} = 40 kΩ from IREF to VDD	VDD -0.76	VDD -0.8	VDD -0.84	V
Soft-Start Ramp						
Soft-Start Reference Voltage, (Intel modes)	V_{SS}	Rss = 100 kΩ	0.76	0.8	0.84	V
Soft-Start Ramp Rate, (Intel modes)	SS_{INTEL}	VR10/VR11.1, Rss= 100 kΩ		1.5		mV/µs
		Adjustment Range of SS ramp rate	0.6		6.0	mV/µs
	R_{SS}	Soft Start Resistor Value	25		250	kΩ
Soft-Start Step Voltage (AMD mode)	SS_{AMD}	Rate = 6.25 mV every 3.03 µs		6.25		mV
Soft-Start Step Time (AMD mode)				3.03		µs
PWM Output						
PWM Output Voltage Low Threshold		Load = ± 1 mA			0.4	V
PWM Output Voltage High Threshold		Load = ± 1 mA	4.0			V

Controller Electrical Characteristics (cont.)

Unless stated otherwise, VDD = 5.0 V ± 5 %, Junction Temperature = 0 to +100 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
OV and UV Protection						
UV Threshold Rise	V_{UVR}	FB rising	66	70	74	%VID
UV Threshold Fall	V_{UVF}	FB falling	57	60	63	%VID
OV Threshold		Intel mode (SS Prior to Vboot period end)	1.30	1.35	1.40	V
		Intel mode (SS after Vboot period end) Greater of:	1.30	1.35	1.40	V
			-5%	V_{DAC} + 250 mV	+5%	V
		Intel mode (After SS complete)	-5%	V_{DAC} + 250 mV	+5%	V
		AMD mode	1.75	1.8	1.85	V
Thermal Monitor						
VR_FAN Fall Threshold	V_{FANF}	VTM falling (assert)		0.394 x VDD		V
VR_FAN Rise Threshold	V_{FANR}	VTM rising (de-assert)		0.445 x VDD		V
VR_HOT Fall Threshold	V_{HOTF}	VTM falling (assert)		0.333 x VDD		V
VR_HOT Rise Threshold	V_{HOTR}	VTM rising (de-assert)		0.394 x VDD		V
Over-Current Protection						
Dead-Zone Bias Current	I_{OCDZ}	Normal operation = 0.6 * (I_{REF} @ 20µA)	11.3	12.0	12.7	µA
Average Over-Current Threshold Level	I_{OCAVG}	Normal operation = 2.5 * (I_{REF} @ 20 µA)	44	50	56	µA
Individual Phase Over-Current Threshold Level	I_{OCPH}	Normal operation = 3.0 * (I_{REF} @ 20 µA)	52	60	67	µA
PSI Input						
Input High	V_{IHPSI}		0.8			V
Input Low	V_{ILPSI}				0.3	V
VID_SEL Input						
VID_SEL V_{IH}	$V_{IHVIDSEL}$		2			V
VID_SEL V_{IL}	$V_{ILVIDSEL}$				0.8	V
VID_SEL Leakage	$V_{IOVIDSEL}$			100		µA
PWM4 Input						
Input High	V_{IHPWM}		0.8 x VDD			V
Input Low	V_{ILPWM}				0.2 x VDD	V
Error Amplifier						
DC Gain		R_L = 10 kΩ to ground		70		dB
Gain-Bandwidth Product		C_L = 100 pF, R_L = 10k to ground		12		MHz
Slew Rate		C_L = 100 pF, Load = ± 400 µA		8		V/µs
Maximum Output Voltage			3.9	4.2		V
Minimum Output Voltage				1.30	1.5	V

SIFDAT and SIFCLK Line Characteristics

Unless stated otherwise, VDD = 5.0 V ± 5 %, Junction Temperature = 0 to +100 °C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Timing					
SIFCLK clock frequency	F_{SIFCLK}	500	667	833	kHz
LOW period of the SIFCLK clock	t_{LOW}	700	875		ns
HIGH period of the SIFCLK clock	t_{HIGH}	500	625		ns
Set-up time for a repeated START condition	$t_{SU;STA}$	200			ns
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	200			ns
Data hold time (provided when SIFDAT is output)	$t_{HD;DAT}$	200	250	450	ns
Data set-up time (provided when SIFDAT is output)	$t_{SU;DAT}$	200	250		ns
Rise time of both SIFDAT and SIFCLK signals	t_r	5		50	ns
Fall time of both SIFDAT and SIFCLK signals	t_f	5		50	ns
Set-up time for a STOP condition	$t_{SU;STO}$	200			ns
Bus free time between a STOP and START condition	t_{BUF}	500			ns
Capacitive load for each bus line	C_b			30	pF
Input parameters					
Noise margin at the LOW level for each connected device	V_{nL}	0.1 x VDD			V
Noise margin at the HIGH level for each connected device	V_{nH}	0.2 x VDD			V
LOW level input voltage	V_{IL}	0		0.3 x VDD	V
HIGH level input voltage	V_{IH}	0.7 x VDD		VDD + 0.5	V
Capacitance for each I/O pin	C_i			10	pF
Output parameters					
LOW level output voltage @ ± 1 mA load	V_{OLSIF}			0.15 x VDD	V
HIGH level output voltage @ ± 1 mA load	V_{OHSIF}	0.85 x VDD			V

Typical Operating Characteristics

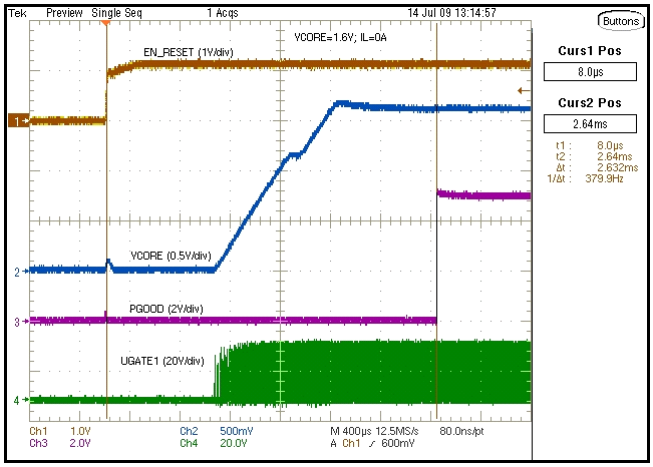


Figure 3: Startup vs. Time (Load = 0 A)

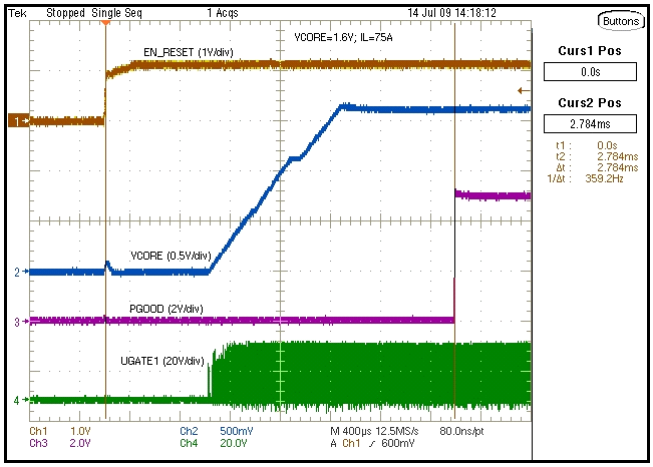


Figure 4: Startup vs. Time (Load = 75 A)

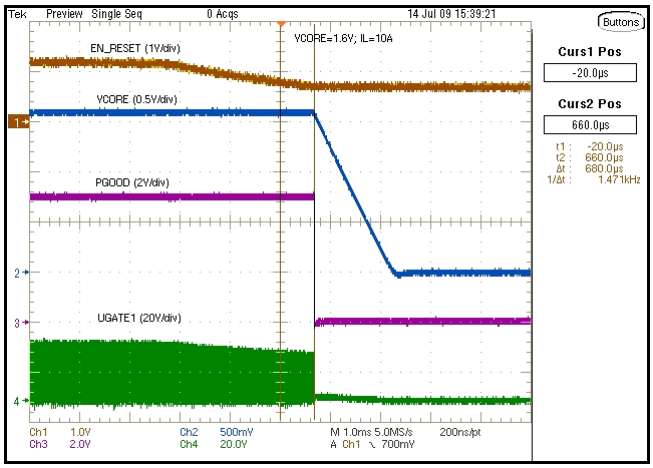


Figure 5: Shutdown vs. Time (10 A)

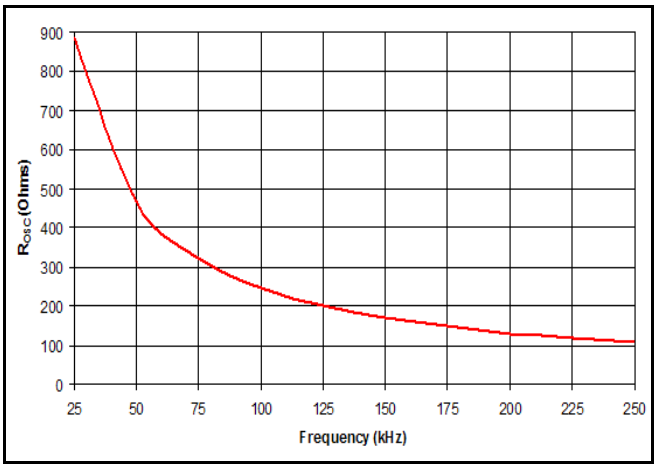


Figure 6: Oscillator Frequency vs. R_{OSC} Resistance

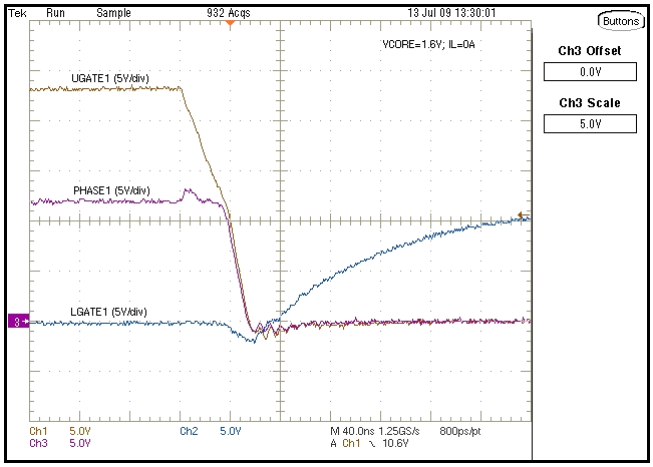


Figure 7: Gate Drive vs. Time (Load = 0 A, Falling Edge)

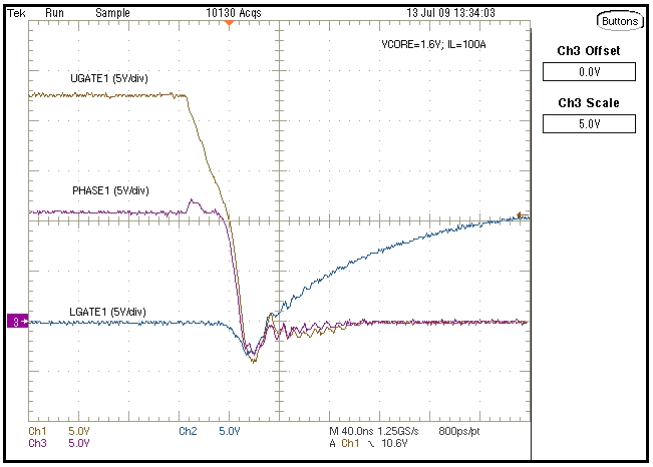


Figure 8: Gate Drive vs. Time (Load=100 A, Falling Edge)

Typical Operating Characteristics (cont.)

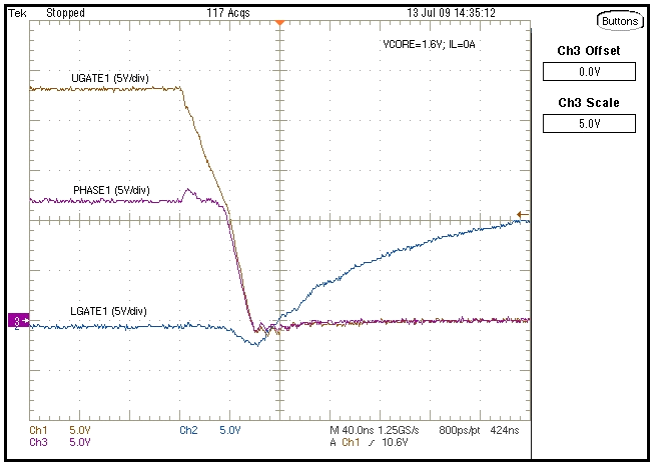


Figure 9: Gate Drive vs. Time (Load = 0 A, Rising Edge)

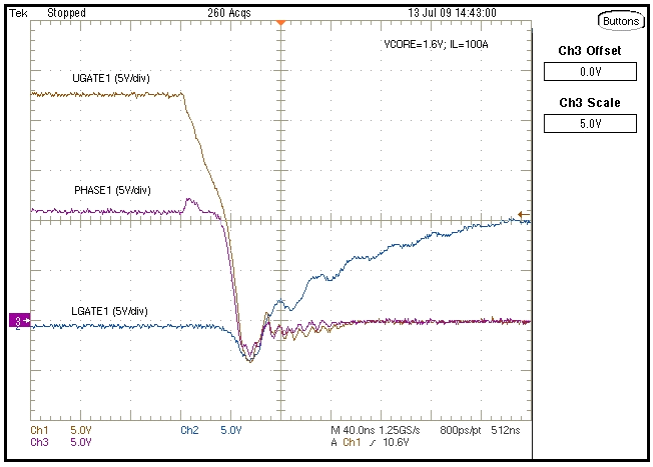


Figure 10: Gate Drive vs. Time (Load =100 A, Rising Edge)

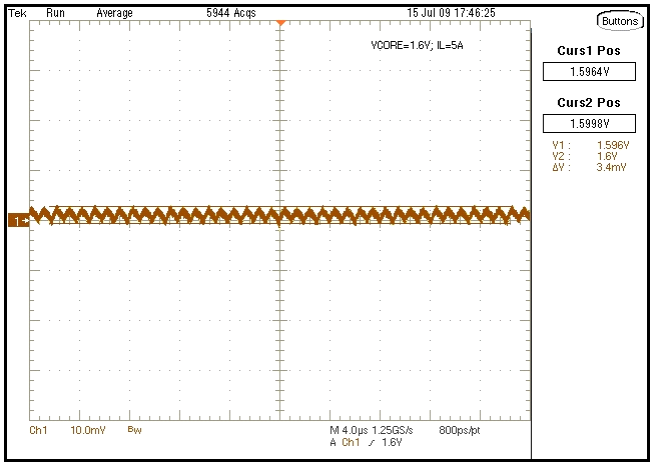


Figure 11: Steady State Output Ripple vs. Time (Load = 5 A)

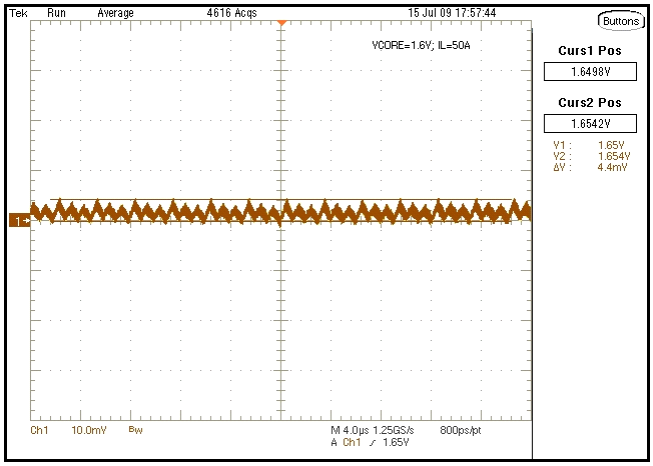


Figure 12: Steady State Output Ripple vs. Time (Load = 50 A)

Introduction

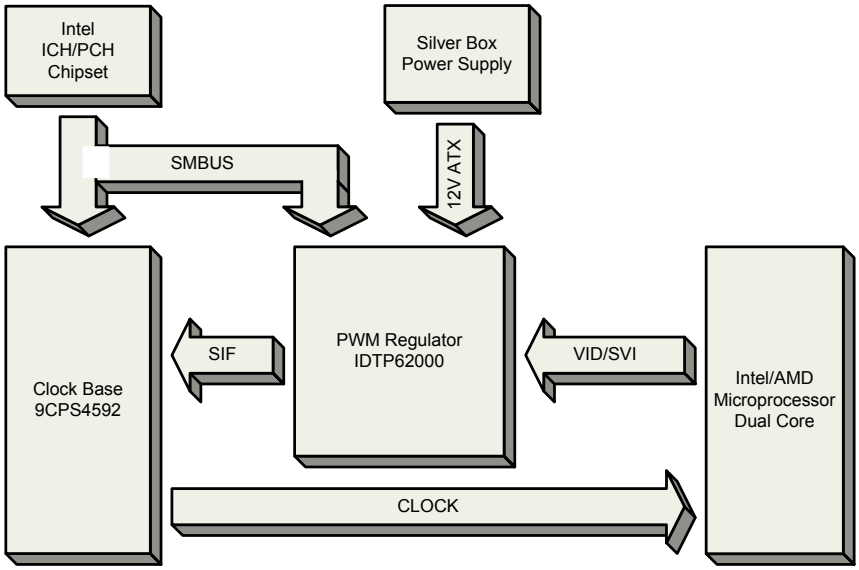
The IDTP62000 is a 2/3/4 phase PWM control IC that is compliant with Intel VR10.x, VR11.x, and AMD PVI/SVI CPU power specifications. The IDTP62000 integrates three MOSFET gate drivers to minimize total solution size, parts count, and cost. Four phase operation is supported with the addition of an IDTP67111 single phase driver IC.

The IDTP62000 includes many features and capabilities in addition those required by Intel and AMD CPUs. Proprietary Hypergear™ dynamic control provides programmable scaling of CPU voltage and clock frequency to enable system level performance and efficiency improvements. Complete Hypergear™ implementation includes an IDT SCPC (system clock power console) IC and related software. Programmable Dynamic Voltage Control (DVC) and Dynamic Frequency Control (DFC) allow performance and power consumption to be optimized as a function of load CPU current. Dynamic Efficiency Control (DEC) enables all configured phases to operate when full current output is required and dynamically reduces the number of active phases at reduced current levels.

An SMBus interface allows programming of IC configuration parameters and provides diagnostic and operational telemetry data to the host system. The output voltage can be offset either in a positive or negative manner using a single external resistor or by programming through the SMBUS interface. The IDTP62000 device contains an advanced control loop algorithm that allows all phases to respond to load steps to minimize output capacitacnce.

The IDTP62000 can operate in stand-alone mode or it can be one part of a two chipset solution for implementing a high performance, energy saving, computing system. The IDTP62000 PWM controller and 9CPS4592 clock generator coordinate adjustments to the output voltage with changes in the clock frequency to optimize system performance. Figure 13 provdes a simplified view of this system.

Figure 13: Two Part System using the IDTP62000 and the 9CPS4592



Operation

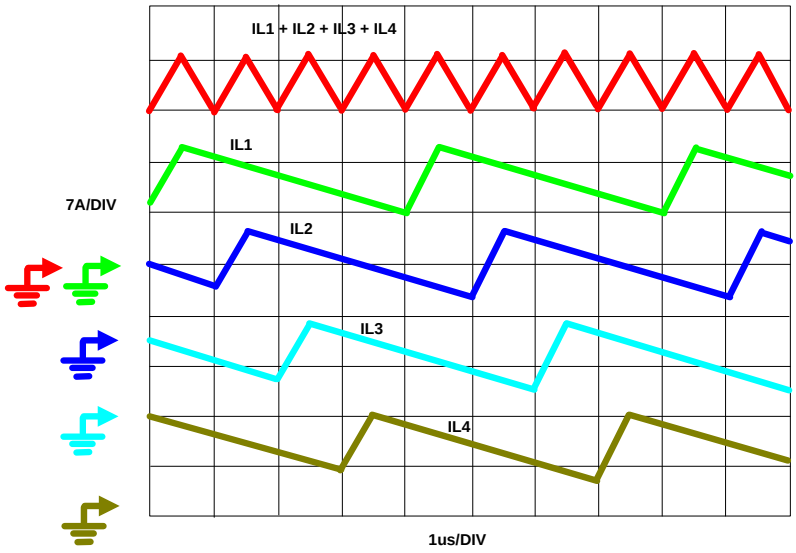
Multi-phase Power Conversion

As microprocessors have evolved in computing power so have PWM V_{CORE} regulators. Single phase operation regulators are no longer feasible for desktop power supplies. Although multi-phase power management regulators has been in existence for decades, recent strides in computing power have mandated that it be applied to microprocessors. These processors are no longer powered by low supply currents but can easily crest to 150A or more during heavy loading transients. The only way to satisfy such heavy demands is to implement a multi-phase power supply. With very little design effort the high current required can be obtained by breaking up the supply into smaller segments, thus realizing an improved component count and minimizing heat dissipation.

Interleaving

In multi-phase PWM regulators the individual channels switching periods are evenly distributed over the PWM clock period. In a four phase PWM regulator, for example, each channel will have time slots equally spaced exactly $T_{Period}/4$ from each other. Additionally, the combined ripple frequency will be 4x higher than for a single channel. The total ripple frequency will have a peak-to-peak amplitude less than 1/4 that of a single phase. The translated benefit is that much smaller inductors are required and the output capacitors can be of a much smaller size (as compared to a single channel PWM regulator.) Figure 14 depicts this combined multi-phase behavior where the total output ripple current is much smaller and thus much smaller input and output capacitors are required. Although passive components have natural variation from one phase to another, the IDTP62000 is able to balance the load even if the inductor DCRs are mismatched by up to 40%.

Figure 14: Inductor–Current Waveforms for a 4-Phase Converter



Voltage Regulation

Load Line (DROOP) Regulation (Adaptive Voltage Positioning)

During power supply operation, the load current of the microprocessor changes often. Due to the equivalent series resistance of the output capacitor, an output voltage spike may occur in the load transient. To optimize the system's reliability, performance and cost trade-offs, it is necessary that the voltage regulator adjust the output voltage proportional to changes in the load current. This feature is called adaptive voltage positioning or droop.

By connecting the DROOP and FB pins together, a current IDROOP which is proportional to the average load current flows from FB through the feedback resistor RFB to generate the droop voltage. The output voltage is then adjusted by the droop voltage which is proportional to the load current. The output voltage can be effectively adjusted in the direction to eliminate spikes or drops or to implement load regulation dependency.

In order to avoid abrupt changes in IDROOP in DEC mode when the number of active phases changes, the I_{DROOP} is defined as the total current divided by the number of configured phases rather than active phases. This ensures that the load line will not change when phases are shed.

At light load conditions, a negative inductor current may occur which can cause the current in the current sense amplifier negative input to fall to zero. This is called the “dead zone” of the load line regulation. The IDTP62000 implements an internal bias current on each phase I_{OCDZ} that is a scaled-down version of IREF. This bias current is used to shift the current level up to compensate for negative current during light load operation, which effectively eliminates the dead zone. As shown in Figure 15, there is no dead zone and the load line resistance RLL is 1 mΩ

(Eq.)
Vdroop = Rfb x (DCR / Rsn) x (Iload /n)
where n = # of configured phases

Figure 15: Load Line showing no “Dead Zone”

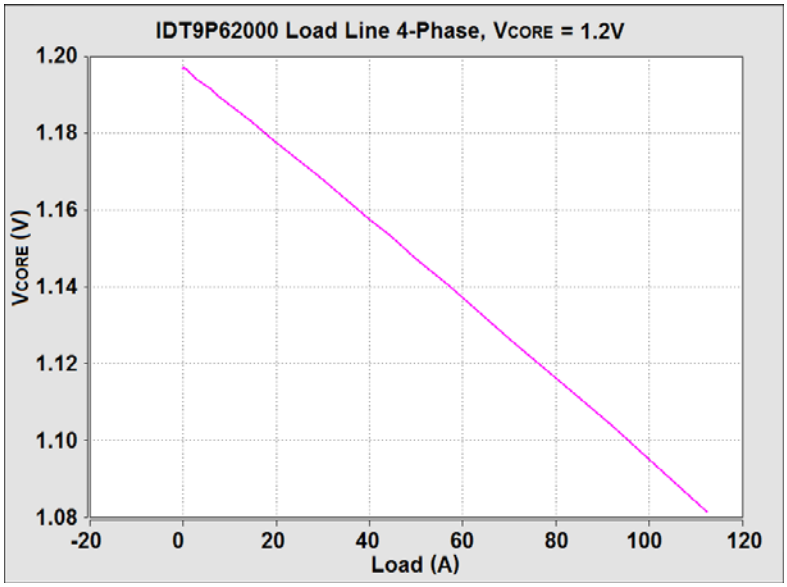
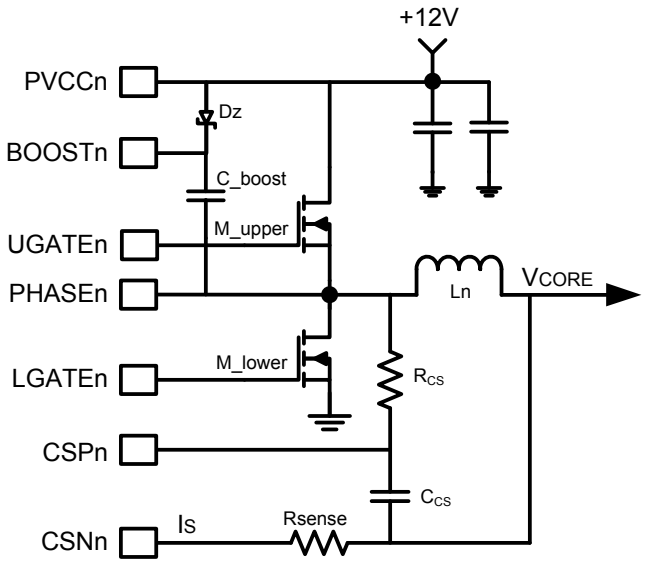


Figure 16: Inductor DCR Current Sensing Configuration



Continuous Current Sensing

The IDTP62000 uses a DCR-based load current sensing for each phase. This sensing scheme uses a pole-zero cancellation technique to allow sensing across the inductor DCR. By doing this, efficiency loss due to an additional sense resistor in the high current path is avoided. The DCR scheme requires a low pass filter consisting of an external resistor and capacitor to be placed across the inductor. See Figure 16. The relationship between the sensed current IS and the inductor current IL is as follows:

(Eq. 1)

$$I_S = \frac{R_{DCR}}{R_{ISENS}} \times \left[\frac{1 + sL / R_{DCR}}{1 + sC_{CS}R_{CS}} \right] \times I_L$$

When the inductor's L/RDCR time constant is set equal to the $C_{CS}R_{CS}$ time constant the term in the square brackets becomes a “1” and effectively disappears from the equation.

The internal sense currents for each phase are used for calculating the droop current, the IMON current, the over-current trip points (average and per phase) and to correct load imbalance among the phases. Furthermore, the average of the sensed currents is used to determine the threshold for transitioning between DVC offsets or DEC modes.

PWM Function and Current Balance Adjustment

The load balance among different phases in IDTP62000 is achieved by modulating the duty cycle of the PWM pulses of the corresponding phase. The IDTP62000 uses trailing edge modulation of the internal triangular waveform by the error amplifier output. The duty cycle of the PWM pulse for a phase is determined by the difference between error signal with the common mode of that phase's triangular waveform.

Load balancing among the active phases is achieved by controlling the duty cycle of each phase through current mode feedback loop derived from the sensed current.

IMON Resistor Calculation (R6 in “4-Phase Applications Reference Circuit” diagram)

R6 = 0.9 x (Sum of sensed currents of all configured phases) / 4

Dynamic Efficiency Control (DEC) Mode of Operation

For efficiency optimization, the IDTP62000 contains a unique and proprietary technique to monitor and adjust the number of active phases based on the sensed load current. An internal determination is used to judge when phases should be turned on and off. Traditional PWM regulators are typically programmed to satisfy the highest load demand. Lighter loads suffer the most inefficiency due to the fixed nature of classic PWM architectures.

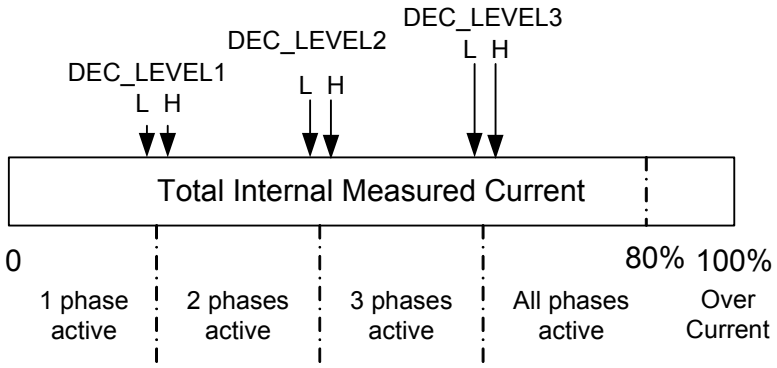
DEC is implemented to improve switching efficiency during light processor loads. In DEC mode, the controller continuously monitors the current load and turns on/off one or more phases according to the load current requirements. The minimum number of phases in DEC mode is configurable and the controller has 3 DEC threshold levels which can each be configured independently.

All DEC levels are defined as a percentage of the scaled average phase current level that triggers an over current protection condition.

The equation for each DEC trip point is given by:
(Eq. 2)

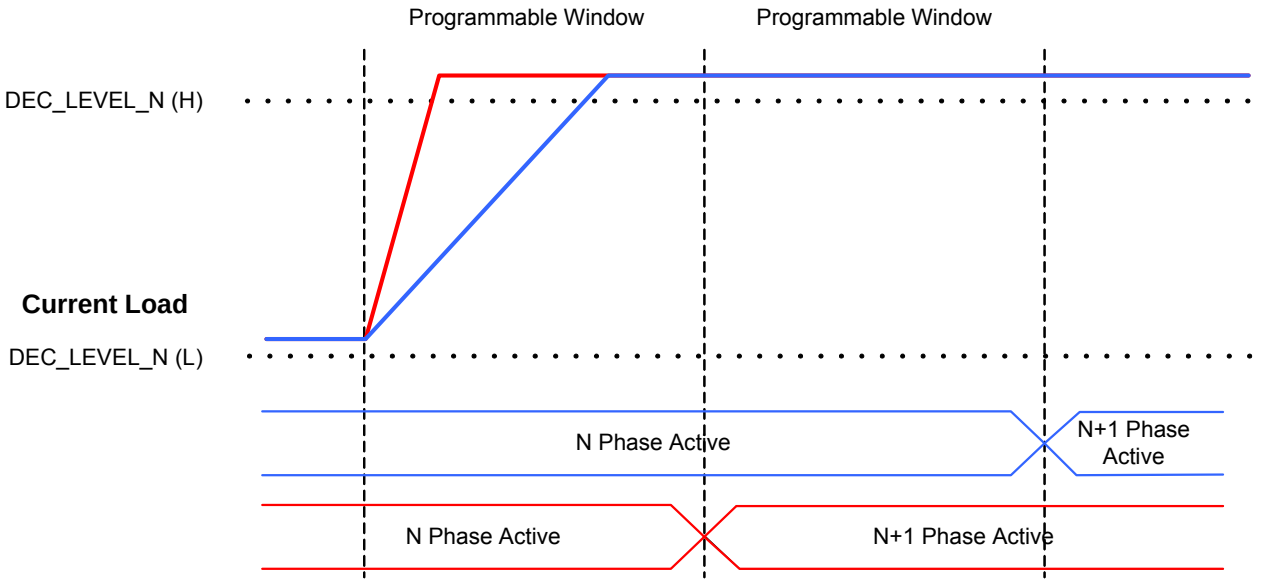
$$\frac{I_{OCAVG} \times (LEVEL[4:0]+1)}{64}$$

Figure 17: DEC Levels showing Hysteresis



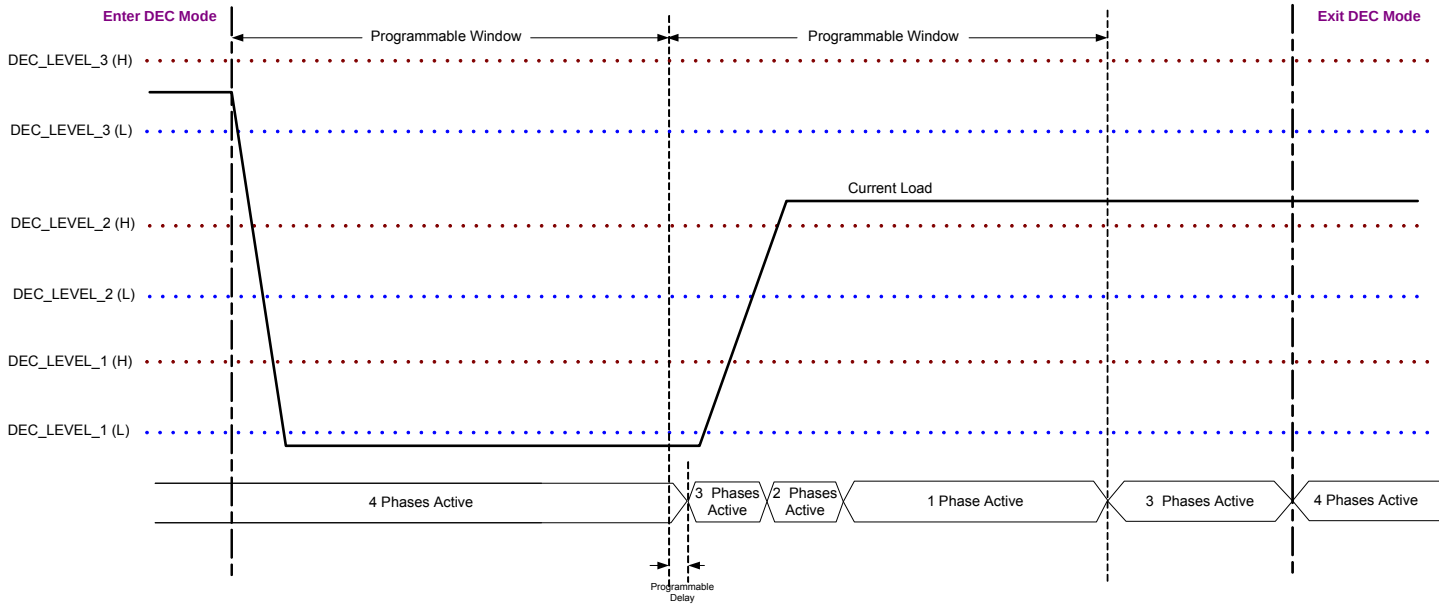
DEC mode is not enabled by default. DEC mode is enabled when the DEC_EN field of the DEC_CTRL register is set to 1b and the maximum number of available phases (based on the total number of configured phases) are turned on. Within a programmable window delay, the controller compares the current load with the three programmed DEC thresholds (all DEC H levels above the current level and all DEC L levels below the current level). No DEC L levels are checked when only 1 phase is enabled, and no DEC H levels are checked when all phases are enabled. If a DEC level transitions across a threshold and remains there for more than 50% of the programmed window period then the number of active phases will be adjusted accordingly.

Figure 18: A Change Across a DEC Threshold Level for >50% Time Duration is Necessary to Trigger Transition



If the load demand increases, all the necessary phases are turned on at the same time. However as the processor load decreases, DEC disables one phase at a time (after a programmable delay) as each DEC level is crossed. The delay comparison period is separately programmable to ensure that the load current remains at the new level long enough to justify a change in the active number of phases.

Figure 19: Normal Operation in DEC Mode

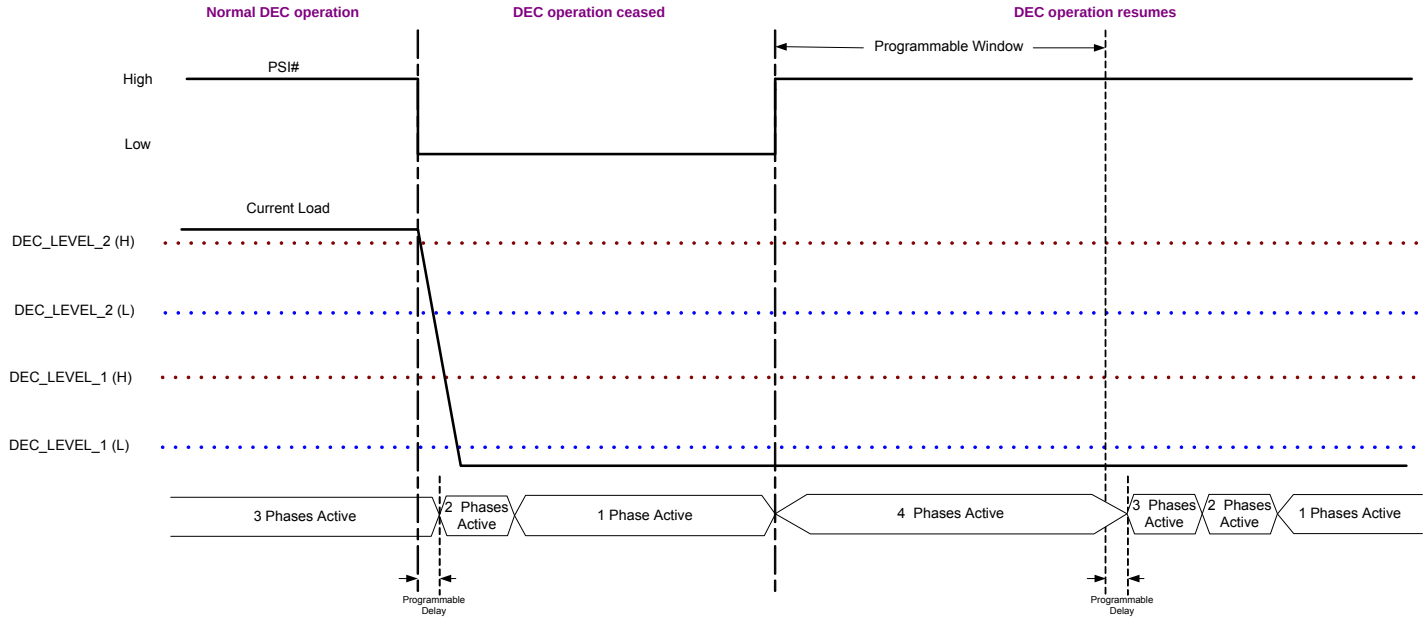


If either an undershoot in VCORE or 50% of the OCP average is detected, DEC mode is exited and the maximum number of phases is immediately reactivated. Once both of these conditions no longer exist, normal DEC operation automatically

resumes.

If PSI and DEC are both enabled, PSI# low indicates that the minimum number of DEC phases is used regardless of the current load. When PSI# is raised from low to high, all phases are used and then normal DEC operation resumes.

Figure 20: DEC Level with PSI Assertion/De-assertion



Oscillator Frequency Selection

The IDTP62000 oscillator can be programmed by an external Rosc resistor. The resistor can be calculated from the following equation:
(Eq. 3)

$$R_{OSC} = 43839 \times f_{SW}^{-1.0971}$$

where f_{sw} is the switching frequency of the PWM regulator in kHz, and R_{osc} is in kΩ

Conversely a given R_{osc} will yield a specific frequency:
(Eq. 4)

$$f_{SW} = 17015 \times R_{OSC}^{-0.9114}$$

Example 1: Given a required switching frequency of 250 kHz and using Equation 3 the resulting R_{osc} value is 102.6 kΩ Using Equation 4 and selecting the closest standard 1% value of 102 kΩ results in a switching frequency of 251.3 kHz.

Example 2: Given a required switching frequency of 500 kHz and using Equation 3 the resulting R_{osc} value is 47.95 kΩ Using Equation 4 and selecting the closest standard 1% value of 47.5 kΩ results in a switching frequency of 504.3 kHz.

Dynamic Voltage Change

The IDTP62000 incorporates a feature whereby the V_{CORE} voltage can be dynamically changed based on the sensed load current. It also supports the existing DFC capability of the clock generator design.

There are four DFC states available in the 9CPS4592 clock generator design. IDTP62000 has four DVC states to match the 9CPS4592. The controller compares the sensed dynamic load current of the processor and compares this sensed level with three load thresholds (DVC_LEVEL) that are register programmed through the SMBUS. As shown in Figure 17, each threshold has one value for rising currents (called “H” for high) and another for falling currents (called “L” for low), so that hysteresis can be implemented in DVC level changes. In addition, each DVC level has an associated register programmed VID code offset value.

The DVC function of IDTP62000 combined with the 9CPS4592 DFC function in a system provides a solution for system design to have optimal performance enhancement and power saving features.

Output-Voltage Offset Programming

Converter output voltage can be offset either higher or lower than the VID voltage. If a resistor is connected between the OFS pin and Vdd the IDTP62000 regulates the voltage across the resistor to 1.6 V. The resulting current is mirrored and will flow from FB pin to ground creating a positive off set in converter output voltage. If a resistor is connected between the OFS pin and ground the voltage across the resistor is regulated to 0.4V and the resulting current is mirrored into the FB pin creating a negative offset voltage. The max offset voltage in either direction is 150µA multiplied by the resistance of RFB. If the OFS pin is left floating then no offset is applied. Equations 7 and 8 describe pin programming of offset voltage. Offset voltage can also be programmed using the SMBus. This works by modifying the VID code and adjusting the under voltage and over voltage thresholds accordingly

Voffset (+) = RFB x (VDD - 1.6) / ROFS (equation 7)
Voffset (-) = RFB x 0.4 / ROFS (equation 8)

DVC Programming

The DVC registers should only be programmed when the DVC mode is disabled i.e. when the DVC_EN bit of the DVC_CTRL register is low. By default, the DVC feature is disabled. It can be enabled by setting the DVC_EN bit to high in the DVC_CTRL register.

Sensed Load Current Thresholds and Filters

IDTP62000 has four output voltage offset values which are delineated by three pairs of sensed load current levels. Each level has user programmable upper and lower threshold level that facilitates the addition of hysteresis. The threshold levels and offsets are illustrated below. When a threshold crossing has been detected, the filter timer DVC_WIN is initiated. The current level has to stay above (or below) the threshold for at least 50% of the timer duration in order for it to be recognized as a DVC trigger event. All DVC levels are defined as a percentage of the average phase current level that triggers an over-current condition (IOCAVG), and are given by IOCAVG*(LEVEL[4:0] + 1)/32.

AMD PVI/SVI Dynamic VID Transitions

In AMD mode, D-VID can “jump” or change by more than one bit step at a time. If the new VID code is stable for 200 ns, the controller will recognize the change and begin to adjust the DAC at a rate of 3.125 mV per 1 µs until the VID and DAC are equal. This means that the total time for a change is dependant on the size of the D-VID change.

Chip Enable and Disable

Proper function of both the controller and the driver requires that the bias voltage applied at VDD, UVLO_PVCC and UVLO_VTT must reach the appropriate threshold voltages as defined in Table 1 and Table 2. The hysteresis between the rising and falling thresholds assures that once enabled, the product will not turn off unless there is a substantial drop in supply voltage bias. A recommended connection for the UVLO_PVCC pin is a voltage divider on the 12 volt supply such that when UVLO_PVCC goes above 0.8 V, the driver will already have been powered up. A fixed hysteresis of 65 mV is internally added such that UVLO_PVCC will not be deactivated until the level drops to 0.735 V.

Similarly, UVLO_VTT uses a voltage divider on the motherboard's VTT supply such that when UVLO_VTT goes above 0.8 V, the driver will already have been powered up. Hysteresis of 65 mV (typical) is again added such that UVLO_VTT will not be deactivated until the level drops to 0.735 V.

There are two means by which the controller can be reset: the internal power-on (POR) reset and the external reset pins, UVLO_PVCC and UVLO_VTT. The internal power-on reset is asserted when the device determines that VDD has reached the voltage defined in Table 2. The external UVLO_PVCC and UVLO_VTT are asserted when each pin has reached the voltage defined in Table 2. POR and both reset pins must be asserted to allow normal operation. Deasserting and then reasserting either one will cause the IDTP62000 to immediately reset and perform a soft start. For a POR reset, all CSR registers are returned to their initial, power-on condition (including fuse and OTP values). For a reset cycle caused by either UVLO_PVCC or UVLO_VTT (called a soft reset) the only registers that will be reset are the status registers in DEV_STAT1 and DEV_STAT2. A soft reset can also be induced by writing a 1 to the SOFT_RESET CSR bit.

Initialization

During power up, the device is tolerant of any permutation of power ramping of the 5 V and 12 V supplies.

It is important to properly determine the number of phases and the appropriate VID table selection before the system starts up. This is done by appropriately connecting VID_SEL and PWM4 pins.

During internal power-on reset, the VID_SEL pin state shall determine which VID table is used. Its value is set by an external pull-up or pull-down resistor where pull-up selects the VRD11 8-bit VID table; pull-down selects the VRD10 6-bit VID table; and floating selects AMD PVI or SVI VID table.

Selection of Phase Number

The IDTP62000 determines the number of phases to be enabled by evaluating the state of the PWM4 pin at power-up. If PWM4 is pulled high, 3 phase mode is selected. If PWM4 is pulled low, 2-phase mode is selected. When used in a 4 phase configuration, an external single phase driver must be used and connected to PWM4. Leakage resistors on this driver's input must cause the PWM4 signal to float to midrail during power up. When this midrail condition is detected, 4 phase mode is selected. The external single phase driver must be powered with the same VDD that is used to power the IDTP62000. The number of phases can be changed using the PhaseN fields in DEV_CTRL1[3:0] register.

The selection table is shown below:

Table 4: PWM4 Level vs. Number of Phases

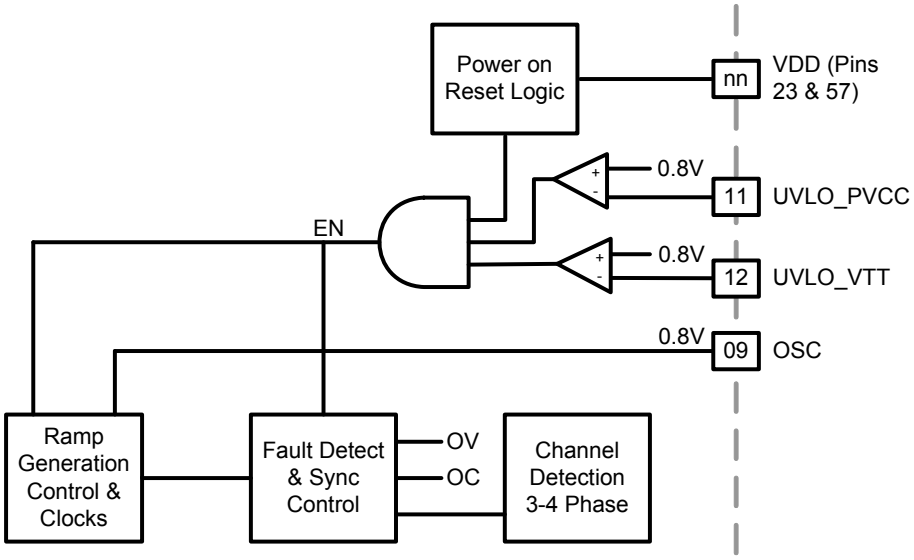
PWM4 Level	High	MID Voltage	Low
Number of Phases	3-phase	4-phase	2-phase

Input Under Voltage and Enable/Disable

The IDTP62000 is enabled once the voltage on the VDD, UVLO_PVCC, and UVLO_VTT pins exceed their thresholds. The VDD threshold is fixed but the UVLO_PVCC and UVLO_VTT thresholds can be programmed with a resistor divider. In most applications UVLO_PVCC will monitor the 12V input while UVLO_VTT is used as the converter Enable input. Any sequence of 5V and 12V input supplies is acceptable.

Deassertion of VDD, UVLO_PVCC, or UVLO_VTT pins will result in converter shutdown. If VDD is deasserted all digital registers will revert to their default settings. Deassertion of either UVLO_PVCC or UVLO_VTT will reset the SMBus status registers only. Figure 21 provides a block diagram of the Input under voltage and enable functions.

Figure 21: Input Under Voltage and Enable Block Diagram



Soft-Start and SMBus Address Programming

The soft-start function of the IDTP62000 enables a smooth charge of the output capacitors in order to limit the inrush input current during startup. The soft-start function is enabled approximately 1 ms after Enable. The SS/SMBA0 pin also determines the value of the SMBus address A0 bit. Connect a resistor from the SS/SMBA0 pin to either VDD or ground. If the resistor is connected to VDD, the A0 bit is set to high. If the resistor is connected to ground, the A0 bit is set to low.

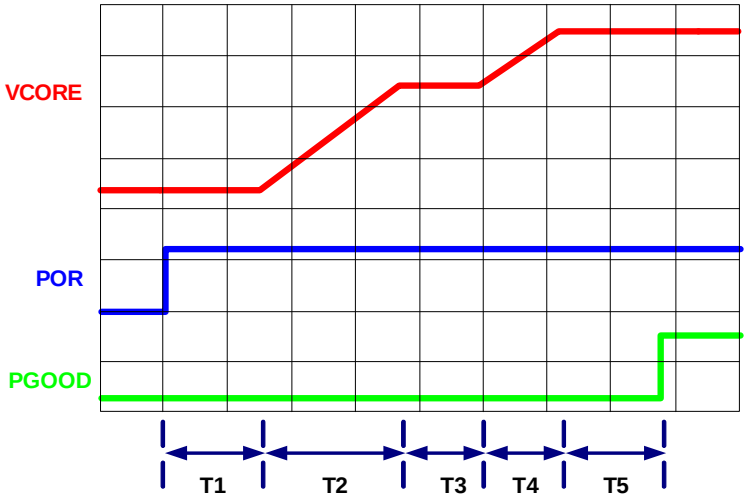
Intel Soft-Start

In Intel modes, the soft-start ramp is set by the R_{SS} resistor. The IDTP62000 regulates the voltage across the resistor to 0.8V.Output voltage first ramps to Vboot and waits for a period of time, T3, (approximately 100 µs). It then ramps to the value determined by the active VID code. Equation 9 determines soft start rate frequency of each 6.25 mV step. The range of RSS is 25 to 250 kohm.

$F_{SS} = 25x10^6 / R_{SS}$ kHz (equation 9)

The complete Intel mode soft start sequence is depicted in Figure 22. The POR signal occurs when all 3 enable inputs become valid.

Figure 22: Intel Mode Soft Start



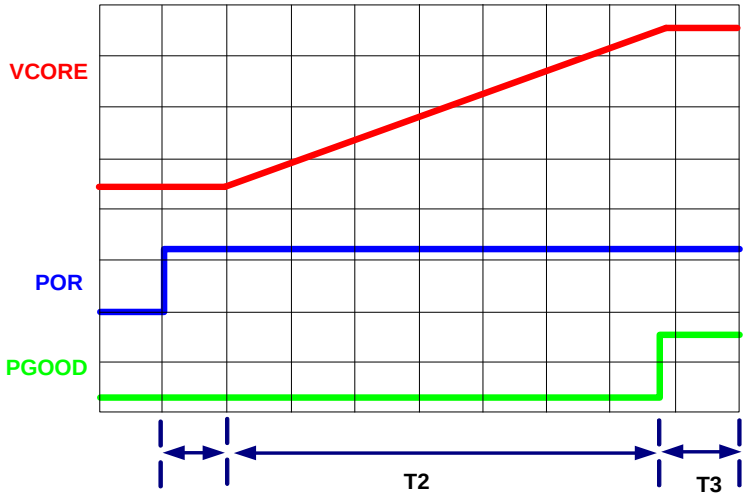
The POR signal indicated in Figure 22 represents the later of the de-assertion of VDD power on reset, the UVLO_PVCC pin and the UVLO_VTT pin.

T1 (ms)	T2 (ms)	T3 (ms)	T4 (ms)	T5 (ms)
1.0	$\frac{1.1V \times R_{SS}}{6.25mV \times 25 \times 10^6}$	0.1	$\frac{\lvert 1.1V - VID \rvert \times R_{SS}}{6.25mV \times 25 \times 10^6}$	1.0

AMD PVI/SVI Mode Soft Start

In AMD PVI/SVI mode, the reference voltage ramps directly to the value determined by the active VID code at a rate of 6.25 mV every 3.03 µs or 330 kHz.

Figure 23: AMD PVI/SVI Soft-Start Waveforms



The timings for T1, T2 and T3 are shown below:

T1 (ms)	T2 (ms)	T3 (ms)
1.0	$\frac{VID \times 3030}{6.25}$	1.0

Pre-Biased Soft Start

In order to prevent reverse inductor current when starting up into pre-charged output capacitors the IDTP62000 will not activate its low side gate drivers until the voltage on the FB pin exceeds the Error Amplifier's reference voltage.

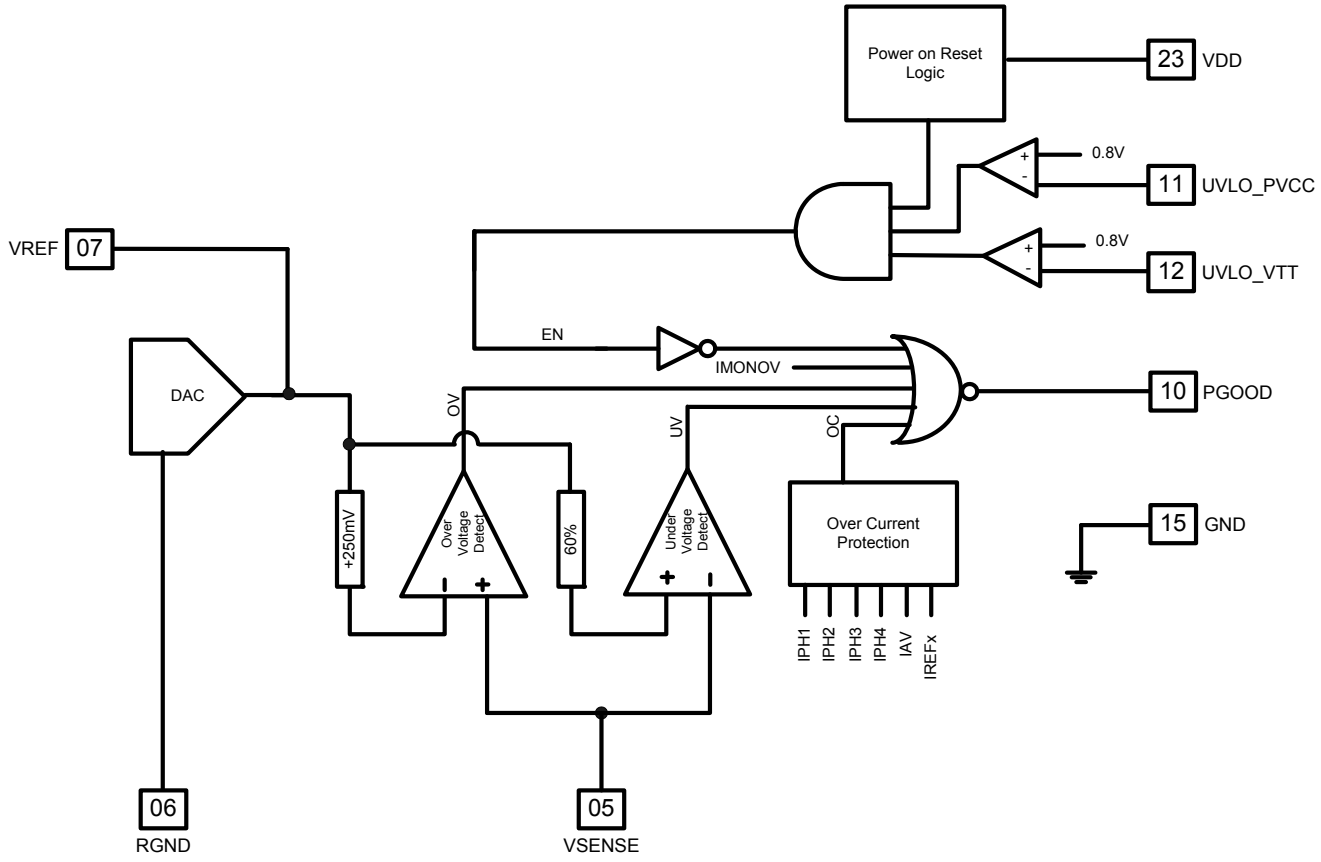
Fault Monitoring Protection

Power Good Signal (VR_READY)

The PGOOD pin is an open drain output that should be pulled up to the system appropriate voltage with an external resistor. PGOOD indicates to the rest of the system that the voltage regulator has completed its startup cycle and that all operating parameters are within normal conditions. PGOOD is then used to transmit to the rest of the system the condition of the PWM and especially when a fault condition exists.

During shutdown and soft-start the PGOOD signal is low and will go high after the soft-start sequence completes and the output voltage is between the over-voltage and under-voltage limits (approximately 1 ms after the end of soft-start). During an under-voltage, over-voltage, over-current condition or when the controller output enable UVLO_PVCC is pulled low, PGOOD will drive low. PGOOD will also be pulled low when a no-CPU VID (or OFF) code is selected or during any reset event. During an over-voltage or over-current event, PGOOD will be latched low and will not go high until after a successful soft-start. In the case of an under-voltage condition, PGOOD will transition high when the output voltage returns to above the under-voltage threshold.

Figure 24: Power Good Function



Under Voltage Detection

The VSENSE pin provides ultra-fast under voltage detection. An under voltage event occurs when the output voltage falls below 60% of the target VID code voltage. The VID code voltage is represented by the voltage present at the VREF pin. UVD detection is blanked during a D-VID/DVC operation so as not to give false triggers. During an UVD event the PGOOD pin will be low, thus indicating that a fault condition in the system exists.

Overvoltage Detection

An overvoltage condition is defined as when the output voltage coming from the PWM is higher than the OVP level for more than 250 ns. The trip level value is dependent on which mode of operation the PWM is in. A dedicated VSENSE pin is used to enable ultra-fast response. In Intel mode, the OVP level depends on whether it's in normal running mode or if it's in the pre/post soft-start cycle.

During the boot period but prior to the soft-start cycle (before the completion of TC) the OVP trip_level is set to ~1.35 V (nominal 1.1 V + 250 mV OVP_OFFSET). During the time between the boot period and when PGOOD is asserted, the trip_voltage will equal the greater of the boot period trip voltage or the normal operation trip_level.

During normal operation, the OVP trip level is set to the voltage of the DAC output (VREF) plus OVP_OFFSET.

It is critical for the OVP circuitry to respond quickly and accurately to an over voltage condition. Even a small time exposure to high voltages could easily cause damage to sub-micron geometry processes such as a 32 nm CPU. If an over-voltage condition is detected (either during normal operation or during soft start) the controller will switch on all low-side power MOSFETs and switch off all the high-side MOSFETs in order to protect the load. If the OVP event occurs during normal operation executing a power cycle or performing a reset will be required to restart the controller. If the OVP event occurs during soft start and the part is in Intel mode, the OVP event will not be latched. Instead, the controller will bias the power MOSFETs as described above until the OVP condition disappears, and then will begin the soft start sequence again.

Pre-POR Overvoltage Protection

In the event that the 12 V rail collapses during an OVP event (thus causing a POR reset to occur) the IDTP62000 will hold the low-side N-FETs in asserted state and thus the V_{CORE} will never be exposed to high voltage conditions. In the most severe case of an OVP condition, the CPU will always be protected.

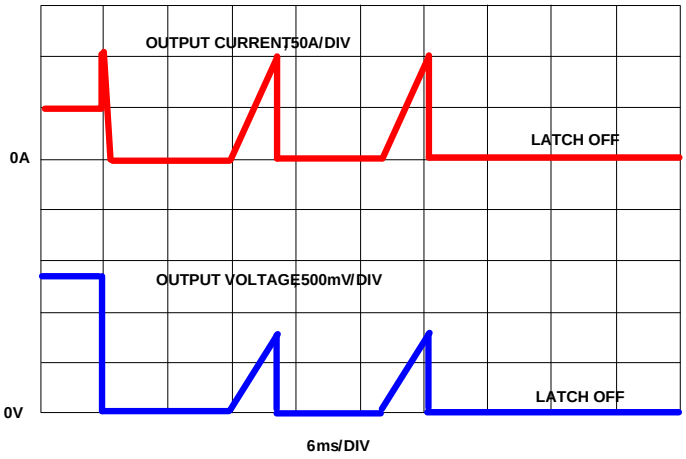
Overcurrent Detection

The IDTP62000 contains two methods to protect the system from dangerous system events. The first method involves comparing the average of the sensed active phase currents with I_{OCAVG} = 2.5*IREF.

If a converter over current event is detected and is present for more than 15 microseconds the IDTP62000 will turn off all the MOSFET drivers, and will de-assert the PGOOD pin. The IDTP62000 will stay in this mode for 12 ms. At the end of this fixed time, a soft-start will be attempted. If the over current condition still exists at the end of soft-start, the IDTP62000 will repeat for one more cycle by waiting for another 12 ms and re-entering soft-start again (otherwise normal operation will resume). If an OCP condition is encountered during the second attempt the IDTP62000 will latch off all the internal power MOSFET gate drivers as well as pin PWM 4 for the external MOSFET gate driver. Once in this OCP state, the PWM must be power cycled (or soft reset) in order to bring it out of latched off mode. This sequence of detection of OCP, attempts at a soft-start, and checking for another OCP is defined as a Auto Retry Mode.

The second over current protection method is cycle by cycle termination of a PWM pulse if any individual sensed phase current exceeds IOCPH = 3*IREF.

Figure 25: Overcurrent Behavior in Auto Retry Mode



Output Voltage Setting (VID)

The IDTP62000 supports a standard 6-bit DAC for Intel VR10 with the addition of an extra LSB bit (VID6) to provide 6.25 mV steps over the range 1.6 V down to 0.83125 mV.

Intel R11.1 VID Mode Codes

IDTP62000 supports an 8-bit DAC for Intel VR11.1. Each step is 6.25 mV from 1.6 V down to 0.5 V.

Table 5: VID Mapping for Intel VR11.1 Mode

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
800 mV	400 mV	200 mV	100 mV	50 mV	25 mV	12.5 mV	6.25 mV

Table 6: VID for Intel VR11.1 Mode

HEX Code		Output Voltage	Hex Code		Output Voltage	Hex Code		Output Voltage	Hex Code		Output Voltage
0	0	OFF	3	0	1.31250	6	0	1.01250	9	0	0.71250
0	1	OFF	3	1	1.30625	6	1	1.00625	9	1	0.70625
0	2	1.60000	3	2	1.30000	6	2	1.00000	9	2	0.70000
0	3	1.59375	3	3	1.29375	6	3	0.99375	9	3	0.69375
0	4	1.58750	3	4	1.28750	6	4	0.98750	9	4	0.68750
0	5	1.58125	3	5	1.28125	6	5	0.98125	9	5	0.68125
0	6	1.57500	3	6	1.27500	6	6	0.97500	9	6	0.67500
0	7	1.56875	3	7	1.26875	6	7	0.96875	9	7	0.66875
0	8	1.56250	3	8	1.26250	6	8	0.96250	9	8	0.66250
0	9	1.55625	3	9	1.25625	6	9	0.95625	9	9	0.65625
0	A	1.55000	3	A	1.25000	6	A	0.95000	9	A	0.65000
0	B	1.54375	3	B	1.24375	6	B	0.94375	9	B	0.64375
0	C	1.53750	3	C	1.23750	6	C	0.93750	9	C	0.63750
0	D	1.53125	3	D	1.23125	6	D	0.93125	9	D	0.63125
0	E	1.52500	3	E	1.22500	6	E	0.92500	9	E	0.62500
0	F	1.51875	3	F	1.21875	6	F	0.91875	9	F	0.61875
1	0	1.51250	4	0	1.21250	7	0	0.91250	A	0	0.61250
1	1	1.50625	4	1	1.20625	7	1	0.90625	A	1	0.60625
1	2	1.50000	4	2	1.20000	7	2	0.90000	A	2	0.60000
1	3	1.49375	4	3	1.19375	7	3	0.89375	A	3	0.59375
1	4	1.48750	4	4	1.18750	7	4	0.88750	A	4	0.58750
1	5	1.48125	4	5	1.18125	7	5	0.88125	A	5	0.58125
1	6	1.47500	4	6	1.17500	7	6	0.87500	A	6	0.57500
1	7	1.46875	4	7	1.16875	7	7	0.86875	A	7	0.56875
1	8	1.46250	4	8	1.16250	7	8	0.86250	A	8	0.56250
1	9	1.45625	4	9	1.15625	7	9	0.85625	A	9	0.55625
1	A	1.45000	4	A	1.15000	7	A	0.85000	A	A	0.55000
1	B	1.44375	4	B	1.14375	7	B	0.84375	A	B	0.54375
1	C	1.43750	4	C	1.13750	7	C	0.83750	A	C	0.53750
1	D	1.43125	4	D	1.13125	7	D	0.83125	A	D	0.53125
1	E	1.42500	4	E	1.12500	7	E	0.82500	A	E	0.52500
1	F	1.41875	4	F	1.11875	7	F	0.81875	A	F	0.51875
2	0	1.41250	5	0	1.11250	8	0	0.81250	B	0	0.51250
2	1	1.40625	5	1	1.10625	8	1	0.80625	B	1	0.50625
2	2	1.40000	5	2	1.10000	8	2	0.80000	B	2	0.50000
2	3	1.39375	5	3	1.09375	8	3	0.79375	F	E	OFF
2	4	1.38750	5	4	1.08750	8	4	0.78750	F	F	OFF
2	5	1.38125	5	5	1.08125	8	5	0.78125			
2	6	1.37500	5	6	1.07500	8	6	0.77500			
2	7	1.36875	5	7	1.06875	8	7	0.76875			
2	8	1.36250	5	8	1.06250	8	8	0.76250			
2	9	1.35625	5	9	1.05625	8	9	0.75625			
2	A	1.35000	5	A	1.05000	8	A	0.75000			
2	B	1.34375	5	B	1.04375	8	B	0.74375			
2	C	1.33750	5	C	1.03750	8	C	0.73750			
2	D	1.33125	5	D	1.03125	8	D	0.73125			
2	E	1.32500	5	E	1.02500	8	E	0.72500			
2	F	1.31875	5	F	1.01875	8	F	0.71875			

Intel VR10 VID Codes

Table 7: VID for Intel VR10 Mode

VID Input Bits							Output	VID Input Bits							Output
4	3	2	1	0	5	6	Voltage	4	3	2	1	0	5	6	Voltage
0	1	0	1	0	1	1	1.60000	1	1	0	1	0	1	1	1.20000
0	1	0	1	0	1	0	1.59375	1	1	0	1	0	1	0	1.19375
0	1	0	1	1	0	1	1.58750	1	1	0	1	1	0	1	1.18750
0	1	0	1	1	0	0	1.58125	1	1	0	1	1	0	0	1.18125
0	1	0	1	1	1	1	1.57500	1	1	0	1	1	1	1	1.17500
0	1	0	1	1	1	0	1.56875	1	1	0	1	1	1	0	1.16875
0	1	1	0	0	0	1	1.56250	1	1	1	0	0	0	1	1.16250
0	1	1	0	0	0	0	1.55625	1	1	1	0	0	0	0	1.15625
0	1	1	0	0	1	1	1.55000	1	1	1	0	0	1	1	1.15000
0	1	1	0	0	1	0	1.54375	1	1	1	0	0	1	0	1.14375
0	1	1	0	1	0	1	1.53750	1	1	1	0	1	0	1	1.13750
0	1	1	0	1	0	0	1.53125	1	1	1	0	1	0	0	1.13125
0	1	1	0	1	1	1	1.52500	1	1	1	0	1	1	1	1.12500
0	1	1	0	1	1	0	1.51875	1	1	1	0	1	1	0	1.11875
0	1	1	1	0	0	1	1.51250	1	1	1	1	0	0	1	1.11250
0	1	1	1	0	0	0	1.50625	1	1	1	1	0	0	0	1.10625
0	1	1	1	0	1	1	1.50000	1	1	1	1	0	1	1	1.10000
0	1	1	1	0	1	0	1.49375	1	1	1	1	0	1	0	1.09375
0	1	1	1	1	0	1	1.48750	1	1	1	1	1	0	1	OFF
0	1	1	1	1	0	0	1.48125	1	1	1	1	1	0	0	OFF
0	1	1	1	1	1	1	1.47500	1	1	1	1	1	1	1	OFF
0	1	1	1	1	1	0	1.46875	1	1	1	1	1	1	0	OFF
1	0	0	0	0	0	1	1.46250	0	0	0	0	0	0	1	1.08750
1	0	0	0	0	0	0	1.45625	0	0	0	0	0	0	0	1.08125
1	0	0	0	0	1	1	1.45000	0	0	0	0	0	1	1	1.07500
1	0	0	0	0	1	0	1.44375	0	0	0	0	0	1	0	1.06875
1	0	0	0	1	0	1	1.43750	0	0	0	0	1	0	1	1.06250
1	0	0	0	1	0	0	1.43125	0	0	0	0	1	0	0	1.05625
1	0	0	0	1	1	1	1.42500	0	0	0	0	1	1	1	1.05000
1	0	0	0	1	1	0	1.41875	0	0	0	0	1	1	0	1.04375
1	0	0	1	0	0	1	1.41250	0	0	0	1	0	0	1	1.03750
1	0	0	1	0	0	0	1.40625	0	0	0	1	0	0	0	1.03125
1	0	0	1	0	1	1	1.40000	0	0	0	1	0	1	1	1.02500
1	0	0	1	0	1	0	1.39375	0	0	0	1	0	1	0	1.01875
1	0	0	1	1	0	1	1.38750	0	0	0	1	1	0	1	1.01250
1	0	0	1	1	0	0	1.38125	0	0	0	1	1	0	0	1.00625
1	0	0	1	1	1	1	1.37500	0	0	0	1	1	1	1	1.00000
1	0	0	1	1	1	0	1.36875	0	0	0	1	1	1	0	0.99375
1	0	1	0	0	0	1	1.36250	0	0	1	0	0	0	1	0.98750
1	0	1	0	0	0	0	1.35625	0	0	1	0	0	0	0	0.98125
1	0	1	0	0	1	1	1.35000	0	0	1	0	0	1	1	0.97500
1	0	1	0	0	1	0	1.34375	0	0	1	0	0	1	0	0.96875
1	0	1	0	1	0	1	1.33750	0	0	1	0	1	0	1	0.96250
1	0	1	0	1	0	0	1.33125	0	0	1	0	1	0	0	0.95625
1	0	1	0	1	1	1	1.32500	0	0	1	0	1	1	1	0.95000
1	0	1	0	1	1	0	1.31875	0	0	1	0	1	1	0	0.94375
1	0	1	1	0	0	1	1.31250	0	0	1	1	0	0	1	0.93750
1	0	1	1	0	0	0	1.30625	0	0	1	1	0	0	0	0.93125
1	0	1	1	0	1	1	1.30000	0	0	1	1	0	1	1	0.92500
1	0	1	1	0	1	0	1.29375	0	0	1	1	0	1	0	0.91875
1	0	1	1	1	0	1	1.28750	0	0	1	1	1	0	1	0.91250
1	0	1	1	1	0	0	1.28125	0	0	1	1	1	0	0	0.90625
1	0	1	1	1	1	1	1.27500	0	0	1	1	1	1	1	0.90000
1	0	1	1	1	1	0	1.26875	0	0	1	1	1	1	0	0.89375
1	1	0	0	0	0	1	1.26250	0	1	0	0	0	0	1	0.88750
1	1	0	0	0	0	0	1.25625	0	1	0	0	0	0	0	0.88125
1	1	0	0	0	1	1	1.25000	0	1	0	0	0	1	1	0.87500
1	1	0	0	0	1	0	1.24375	0	1	0	0	0	1	0	0.86875
1	1	0	0	1	0	1	1.23750	0	1	0	0	1	0	1	0.86250
1	1	0	0	1	0	0	1.23125	0	1	0	0	1	0	0	0.85625
1	1	0	0	1	1	1	1.22500	0	1	0	0	1	1	1	0.85000
1	1	0	0	1	1	0	1.21875	0	1	0	0	1	1	0	0.84375
1	1	0	1	0	0	1	1.21250	0	1	0	1	0	0	1	0.83750
1	1	0	1	0	0	0	1.20625	0	1	0	1	0	0	0	0.83125

AMD PVI/SVI 6-bit Parallel Interface

If VID1 is high when the internal POR is de-asserted, the PVI interface is selected.

The input code VID[5:0] is as follows:

VID[5:0] Setting	< 20h	>= 20h
Output Voltage	1.550 V - 0.025 V * VID[5:0]	0.7625 V - 0.0125 V x (VID[5:0] - 20h)

Table 8: VID for AMD PVI/SVI 6-bit Mode

VID Input Bits						Output	VID Input Bits						Output
5	4	3	2	1	0	Voltage	5	4	3	2	1	0	Voltage
0	0	0	0	0	0	1.55000	1	0	0	0	0	0	0.76250
0	0	0	0	0	1	1.52500	1	0	0	0	0	1	0.75000
0	0	0	0	1	0	1.50000	1	0	0	0	1	0	0.73750
0	0	0	0	1	1	1.47500	1	0	0	0	1	1	0.72500
0	0	0	1	0	0	1.45000	1	0	0	1	0	0	0.71250
0	0	0	1	0	1	1.42500	1	0	0	1	0	1	0.70000
0	0	0	1	1	0	1.40000	1	0	0	1	1	0	0.68750
0	0	0	1	1	1	1.37500	1	0	0	1	1	1	0.67500
0	0	1	0	0	0	1.35000	1	0	1	0	0	0	0.66250
0	0	1	0	0	1	1.32500	1	0	1	0	0	1	0.65000
0	0	1	0	1	0	1.30000	1	0	1	0	1	0	0.63750
0	0	1	0	1	1	1.27500	1	0	1	0	1	1	0.62500
0	0	1	1	0	0	1.25000	1	0	1	1	0	0	0.61250
0	0	1	1	0	1	1.22500	1	0	1	1	0	1	0.60000
0	0	1	1	1	0	1.20000	1	0	1	1	1	0	0.58750
0	0	1	1	1	1	1.17500	1	0	1	1	1	1	0.57500
0	1	0	0	0	0	1.15000	1	1	0	0	0	0	0.56250
0	1	0	0	0	1	1.12500	1	1	0	0	0	1	0.55000
0	1	0	0	1	0	1.10000	1	1	0	0	1	0	0.53750
0	1	0	0	1	1	1.07500	1	1	0	0	1	1	0.52500
0	1	0	1	0	0	1.05000	1	1	0	1	0	0	0.51250
0	1	0	1	0	1	1.02500	1	1	0	1	0	1	0.50000
0	1	0	1	1	0	1.00000	1	1	0	1	1	0	0.48750
0	1	0	1	1	1	0.97500	1	1	0	1	1	1	0.47500
0	1	1	0	0	0	0.95000	1	1	1	0	0	0	0.46250
0	1	1	0	0	1	0.92500	1	1	1	0	0	1	0.45000
0	1	1	0	1	0	0.90000	1	1	1	0	1	0	0.43750
0	1	1	0	1	1	0.87500	1	1	1	0	1	1	0.42500
0	1	1	1	0	0	0.85000	1	1	1	1	0	0	0.41250
0	1	1	1	0	1	0.82500	1	1	1	1	0	1	0.40000
0	1	1	1	1	0	0.80000	1	1	1	1	1	0	0.38750
0	1	1	1	1	1	0.77500	1	1	1	1	1	1	0.37500

SVI Interface

The AMD PVI/SVI is based on the I²C standard. The maximum frequency of operation is 400 kHz. If VID1 is low when the internal POR is de-asserted, the SVI interface is selected. VID[7:4], VID[1:0] will be pulled low internally. For SVI mode, VID[3] becomes the SVC pin of the SVI and VID[2] becomes the SVD pin.

Table 9: Address and Data Byte Formats

Address Byte Format		Data Byte Format	
[6:4]	Always 110b	7	Ignored
3	Reserved	[6:0]	VID[6:0]
2	Ignored		
1	If set then the following data byte contains the VID		
0	Ignored		

Subsequent data bytes, if any are ignored. The VID[6:0] codes will be interpreted as follows:

Table 10: VID Codes for AMD PVI/SVI SVI Mode

VID[6:0]	Output Voltage
0x7F to 0x7C	OFF
0x7B to 0x5F	0.375 V
0x5E to 0x00	1.55 - 0.0125 * VID[6:0] V (1.55 V to 0.375 V)

If a valid VID code has not been received by the end of the soft start period, the device will regulate V_{CORE} to a predetermined voltage based on the connections of the SVC and SVD pins (VID[3:2]) during power-up per the AMD PVI/SVI specification as follows:

Vid[3:2]	Voltage
00b	1.1 V
01b	1.0 V
10b	0.9 V
11b	0.8 V

If an “OFF” code is received, then LGATE, UGATE, and PGOOD will be immediately brought low until the next valid VID code is received. At that time, the soft start sequence will begin to bring V_{CORE} to the voltage indicated by the new VID code.

Serial Interface (SIF)

The Serial Interface (SIF) is similar to an I²C communication architecture but operates at 666.7 kHz. The SIF provides the ability for the IDTP62000 to communicate information to the PC clock generator. The IDTP62000 is the master and the 9CPS4592 is the slave. The SIF is a two wire interface, serial data (SIFDAT) and serial clock (SIFCLK). The IDTP62000 master will never read from the 9CPS4592, so the SIFDAT traffic is unidirectional. To avoid contention issues between SMBus write operations and SIF read operations on a Command and Status Register (CSR) the SIF interface does not read CSRs during any SMBus is write operations. The typical system block diagram using the SIF is shown in figure 26. Figure 28 and Figure 29 are reference examples showing the relationship and interaction between the IDTP62000 and the 9CPS4592.

Figure 26: SIF Engine

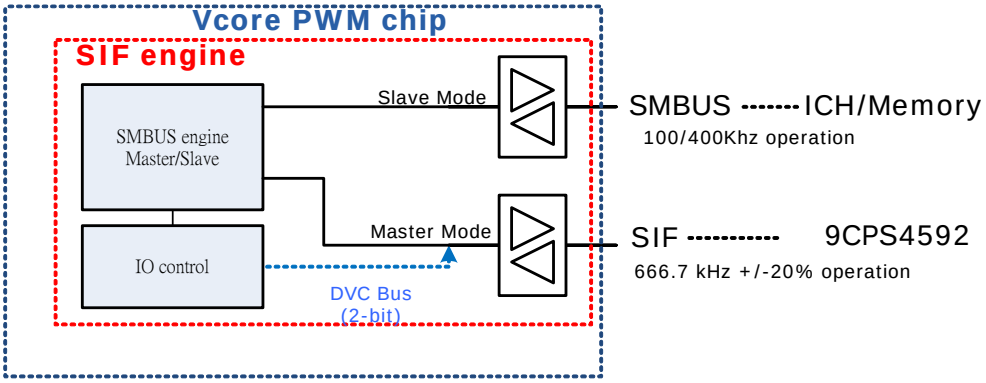


Figure 27: System Block Diagram Showing SIF

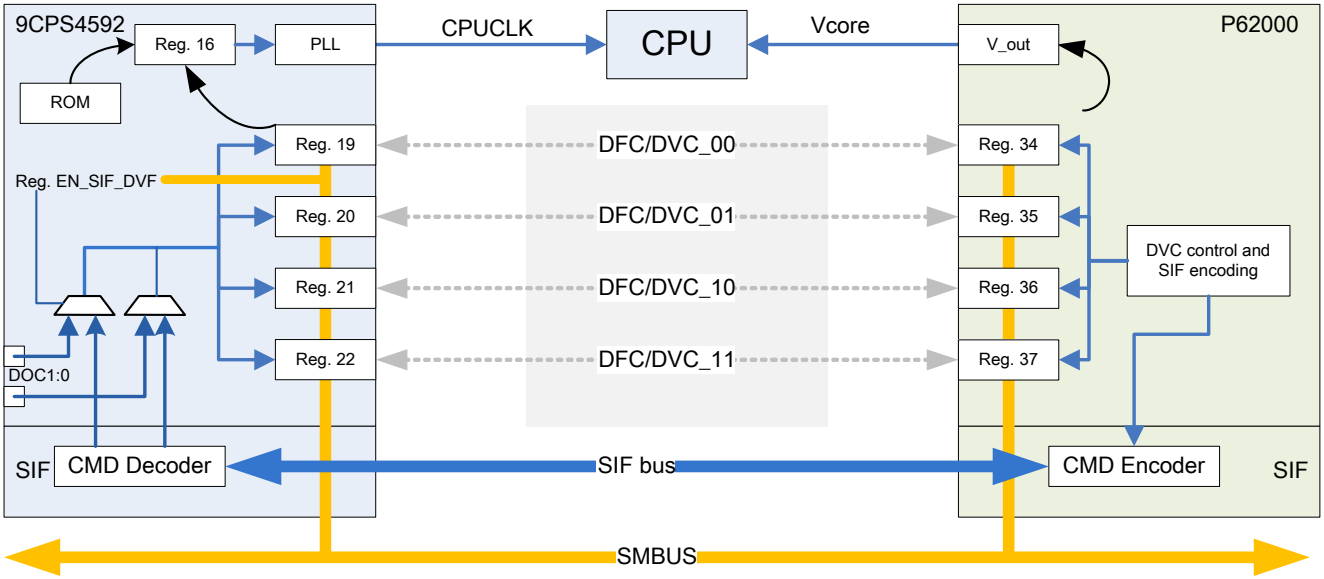


Figure 28: SIF Function Concept Block Diagram Inside the IDTP62000 Chip

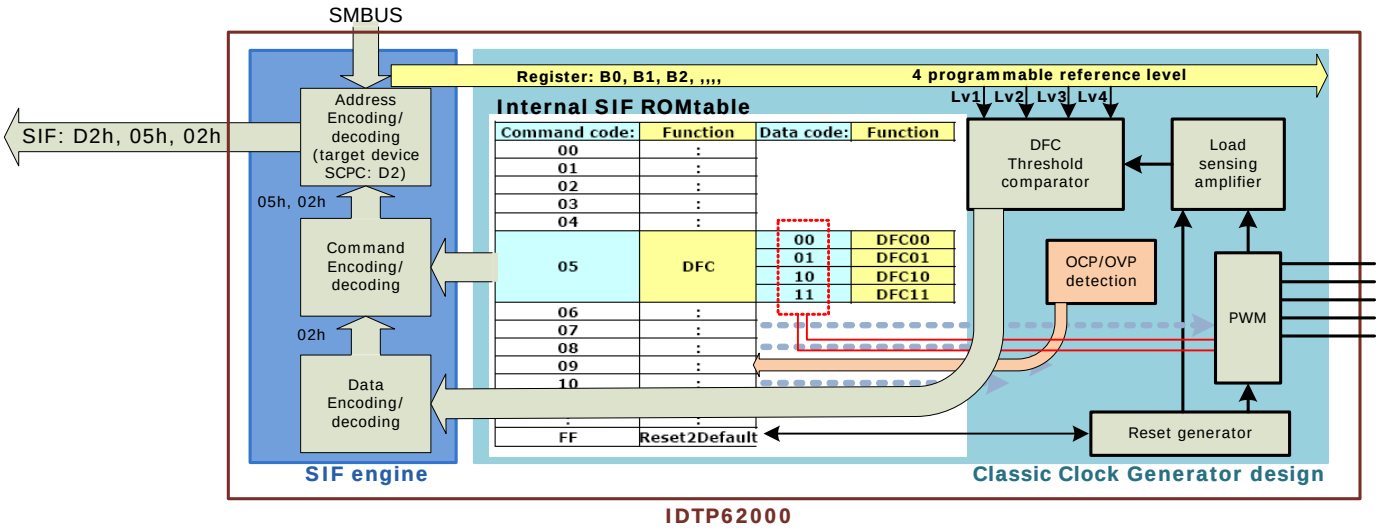
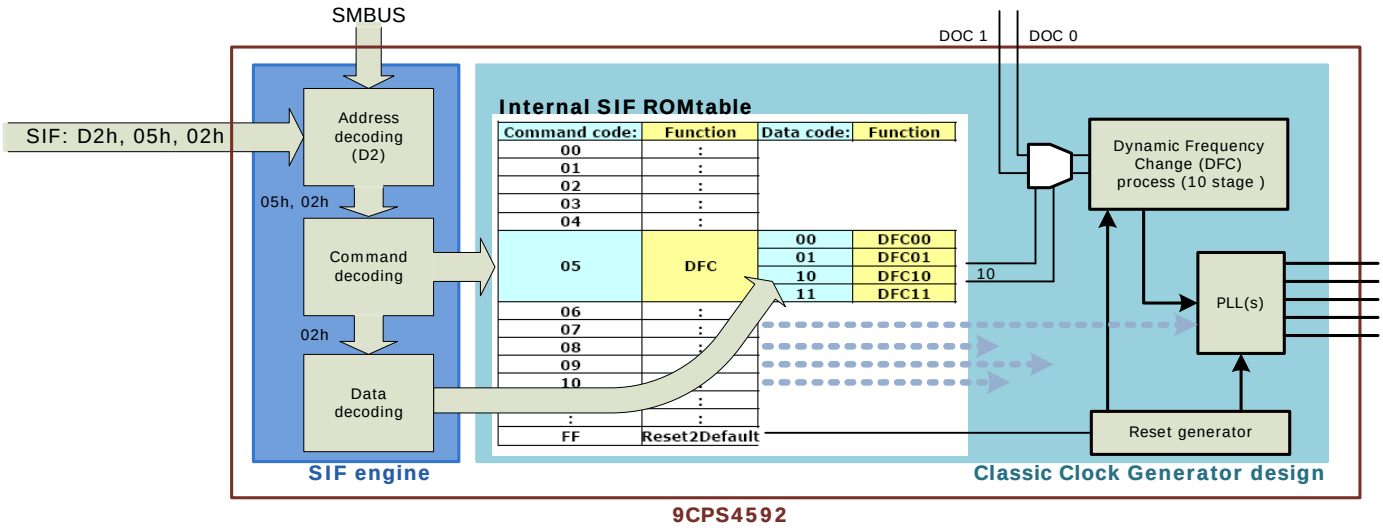


Figure 29: SIF Function Concept Block Diagram Inside the 9CPS4592 Chip



SIF Terminology Definitions

Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device or devices addressed by a master
SCPC	System Clock Power Console - 9CPS4592 with SIF to communicate with the IDTP62000

SIF Specifications

START and STOP Conditions

The START and STOP conditions are generated by the IDTP62000 master. The bus is considered busy after the START condition. The bus is busy if a repeated START is generated.

A start condition is defined by a HIGH to LOW transition on the SIFDAT line while SIFCLK is HIGH. A STOP condition is defined as a LOW to HIGH transition on the SIFDAT line while SIFCLK is HIGH.

Data Transfer

Every byte on the SIFDAT line must be eight bits long. Each byte has to be followed by an acknowledge bit. Data bit transfer is from MSB first to LSB last. If a slave is busy and can't receive or transmit another complete byte of data, it can hold the SIFCLK LOW to force the master to wait. Data transfer continues when SIFCLK is released.

Arbitration

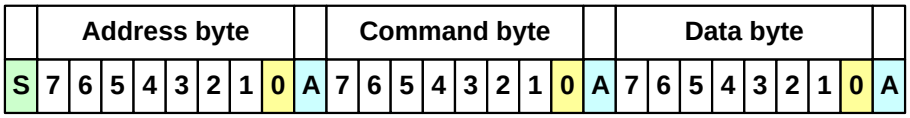
As the IDTP62000 is a master and the 9CPS4592 is a slave no master/master arbitration is required.

7-Bit Addresses

After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit, LSB, for READ/WRITE (R/W). A zero (0) in the eighth bit is a WRITE; a one (1) is a READ. A data transfer may be terminated by a STOP condition generated by the master. If the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

When an address is sent, each device in the system connected to the SIF compares the first seven bits after the START condition with its address. If they match, the device considers itself addressed by the master as a slave/receiver or slave/transmitter, depending on the R/W bit.

Figure 30: SIF Byte Configuration



S	Start Bit
0	Read / Write bit
A	Acknowledge bit

SIF Command Set

9CPS4592 SIF address: D0h (same as its SMBus address)

Table 11: SIF Command Set

From Master Side				From Slave Side	
Command	Function description	Data (hex)	Function description	Ack	Slave Feedback
00	Slave Device Detection		Reserved for future design		
01	PSI status	00~01	PSI status 00: PSI Inactive, 01: PSI Active	A	x
02	Mode	00~FF	Reserved for future design	A	x
03	PWM total phase number	00~0F	Reserved for future design	A	x
04	Dynamic active phase number	00~0F	Reserved for future design	A	x
05	DFC/DVC	00~03 or 10~13	The data byte reflect DVC/DFC registers as DFC00/DVC00 to DFC11/DVC11 *Bit4 is indicator bit for timer usage*	A	x
06	OCP: Over-Current Protection	00~01	PWM Over-Current Protection active 00 = Normal, 01 = OCP active	A	x
07	OVP: Over-Voltage Protection	00~01	PWM Over-Voltage Protection active 00 = Normal, 01 = OVP active	A	x
08	VR_HOT Alert	00~01	00 = Normal, 01 = VR_HOT active	A	x
09	VR_FAN Alert	00~01	00 = Normal, 01 = VR_FAN active	A	x
0A	VID data	00~FF	Reserved for future design	A	x

PSI Status – Command Code: 01h, Data: 00h, 01h

The IDTP62000 has a PSI# input pin which is driven by the CPU to indicate that the CPU has entered its internal power down state. There is no CSR mechanism to disable this command. On assertion of PSI#, the IDTP62000 passes this command to the 9CPS4592 with the data value of 01h. On deassertion of PSI#, the IDTP62000 resends the command with a data payload of 00h. The sending of these SIF commands coincides with the setting and resetting of the CSR bit PSI# (PSI_CTRL[6]).

DFC/DVC – Command Code: 05h, Data: 00~03h, 10~13h

The IDTP62000 sends this command anytime the DVC level changes due to crossing a new DVC threshold. If forced to a new DVC level by some other means (for example, receiving a VR_FAN alert and going to DVC00), then no DFC/DVC command is sent. There is no means for using the SIF interface to tell the 9CPS4592 if DVC mode has been turned on or off, other than passing information about the present DVC level. See Section 3.0 for more details.

OCP: Over-Current Protection – Command Code: 06h, Data: 00h, 01h

The IDTP62000 sends this command to the 9CPS4592 with a data payload of 01h immediately after an over-current shut down event has been detected. This command can be disabled by the IDTP62000 register setting (SIF_CMD_EN[3]). The command is cleared when the OCP event is cleared and PGOOD is high. The sending of these SIF commands will be entirely independent of the setting and resetting of the CSR bit OCP_ALERT.

OVP: Over-Voltage Protection – Command Code: 07h, Data: 00h, 01h

The IDTP62000 sends this command to the 9CPS4592 with a data payload of 01h immediately after an over-voltage event has been detected. This command can be disabled by the IDTP62000 register setting (SIF_CMD_EN[2]). The command is cleared when the OVP event is cleared and PGOOD is high. The sending of these SIF commands will be entirely independent of the setting and resetting of the CSR bit OVP_ALERT.

VR_HOT Alert – Command Code: 08h, Data: 00h, 01h

The IDTP62000 sends this command every time the VR_HOT status changes. The command can be disabled by IDTP62000 register setting (SIF_CMD_EN[1]). When not in DVC mode, this command is sent upon each change in VR_HOT status. The sending of these SIF commands will be entirely independent of the setting and resetting of the CSR bit VRHOT_ALERT.

VR_FAN Alert – Command Code: 09h, Data: 00h, 01h

The IDTP62000 sends this command every time the VR_FAN status changes. The command can be disabled by the SIF_CMD_EN[0] register setting. When not in DVC mode, this command is sent upon each change in VR_FAN status. The sending of these SIF commands will be entirely independent of the setting and resetting of the CSR bit VRFAN_ALERT.

Interaction of SIF commands with DVC mode

When DVC is enabled, the following table describes the impact on DVC status for each of these SIF commands:

Table 12: DVC Action in Conjunction with SIF Commands

Command	Summary of DVC consequence
PSI Status	DVID_EN = 1: disable DVC until PSI status changes to deasserted DVID_EN = 0: continue in DVC mode
OCP alert	Shut down, DVC resumes after reset
OVP alert	Shut down, DVC resumes after reset
VR_HOT alert	Force to DVC00 until VR_NOT is deasserted
VR_FAN alert	Force to DVC00 until VR_FAN is deasserted

DVC GPO Interface

If the DEV_CTRL1 fields are programmed such that GPO_EN = 1b and SIF_EN = 0b, then the SIF interface is disabled and the DVC GPO bus is enabled. The SIF_EN bit always takes priority if enabled.

The purpose of the DVC GPO bus is to provide backward compatibility for legacy ICS clock generator chips. This data bus only delivers the DVC[1:0] information to the clock generator chip via the SIFDAT and SIFCLK pins. When operating in GPO mode, these pins must never drive their output above 3.765V. One means of accomplishing this is to limit the drive for logical high outputs so that an external resistor can be used to pull the voltage on each of these pins down.

SMBus Interface

The IDTP62000 has an SMBus programming interface that is compatible with the System Management Bus (SMBus) Specification Version 2.0, dated August 3, 2000. This interface is used to program the Command and Status registers (CSR).

The designated pins are SMBDAT for data and SMBCLK for the clock. The SMBus interface in the IDTP62000 provides for slave mode operation only. The address of the 7 bit interface is either 0x78 or 0x79 where the LSB of the address is determined by detecting whether the SS/SMBA0 pin is high or low at powerup. The pin value is latched when the internal POR de-asserts so that subsequent changes to the SS/SMBA0 pin do not affect the LSB bit.

Table 13: SMBus Address Determination

SS/SMBA0 at Power On	SMBus Address
L	0x78
H	0x79

Applications Information

PWM Modulation and Regulation

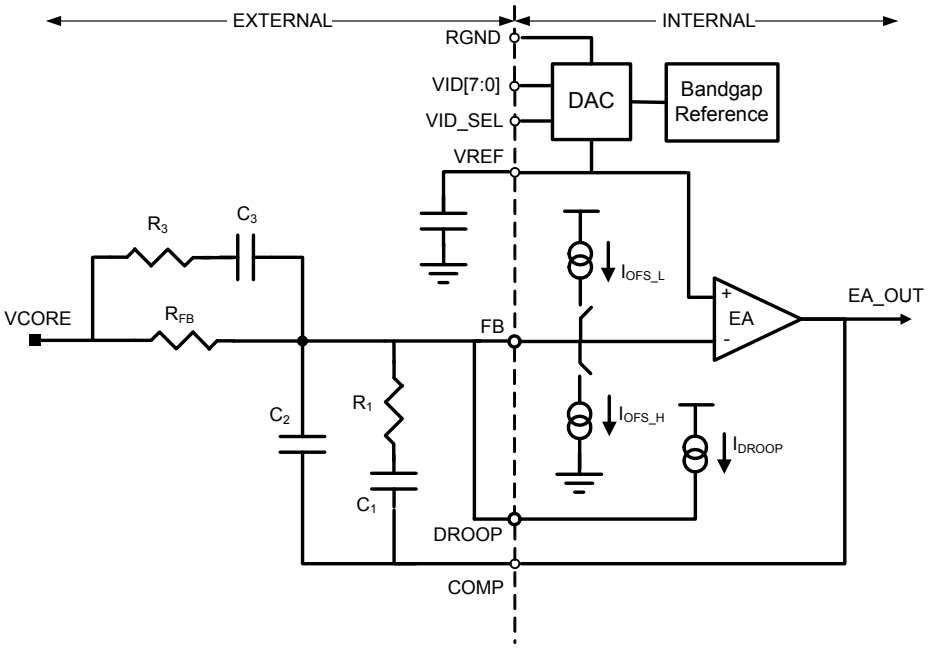
The IDTP62000 implements voltage mode control with trailing edge modulation. Per phase switching frequency is programmed by an external resistor connected from the ROSC pin to GND according to equations (1) and (2).

R_{OSC} = 1 / F_{SW} x 40pF (equation 1)
F_{SW} = 1 / R_{OSC} x 40pF (equation 2)

The voltage mode ramp amplitude is typically 2.4V over the full switching period with duty cycle limited to 93% to ensure proper driver bootstrap operation. The error amp provides high gain, bandwidth, and slew rate using type 3 compensation. A DAC (Digital to Analog Converter) sets the error amp reference voltage and is biased to the converter remote sense ground to eliminate the need for a differential remote sense amplifier and errors factors associated with it. Converter output voltage offset and load line are implemented through bias currents flowing into the feeback resistor. Figure 32 depicts the error amplifier configuration.

Current sharing among active phases is achieved by controlling the duty cycle of each phase through a current mode feedback loop.

Figure 32: Error Amplifier Configuration



Reference Current (IREF) and Load Line Temperature Compensation Enable

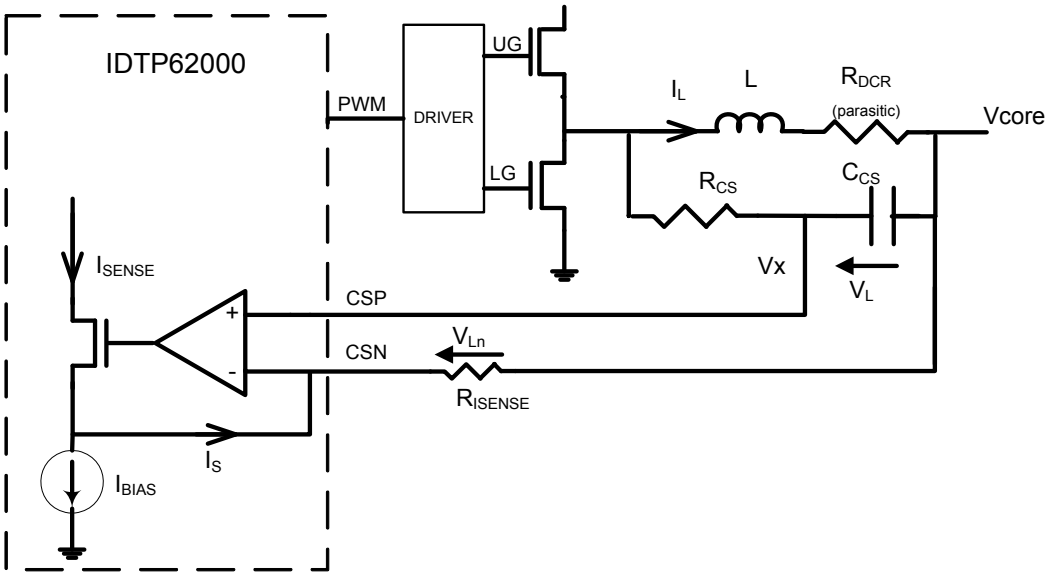
To enable the IDTP62000 to accurately process current information an accurate reference current is created by placing an external 40.2kohm ±1% accurate resistor between IREF and either GND or VDD. Connecting the resistor to GND enables load line temperature compensation while connecting it to VDD disables it. The voltage across the IREF resistor is regulated to 0.8V creating a nominal 19.9µA reference current. Load line temperature compensation is useful for typical inductor current sense applications but should be disabled if a zero TC inductor DCR or precision current sense resistors are used.

Phase Current Sensing

Inductor current is sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor as shown in the following figure. Usually the resistor R_{CS} and capacitor C_{CS} are chosen so that the time constant of R_{CS} x C_{CS} equals the time constant of the inductor, which is the inductance L divided by the inductor RDCR. If the two time constants match, the Voltage across C_{CS} is proportional to the current through L, and the sense circuit can be treated as if it was a sense resistor in series with the inductor. Any mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

The IDTP62000 includes a current sense amplifier that uses feedback to inject a current out of each CSNn input pin such that its voltage is the same as the corresponding CSPn pin. Thus the voltage across the C_{CS} capacitor which represents the inductor current appears across the R_{ISENSE} resistor. The resulting ISENSE current is used to control load balancing, load line, and other functions that require accurate inductor current information. A fixed IBIAS current that is derived from the IREF current reference is added to prevent a "dead zone" when inductor current is zero or negative. This bias current is subtracted prior to subsequent processing by internal circuits. If a noise filter cap is applied from the CSN pin to ground its value should be 45pF or less to ensure stability of the current sense amplifier.

DCR-based Load Current Sensing (per phase)



The TM temperature sense pin is used to compensate for the 0.385% per degree Centigrade temperature coefficient of copper inductor windings. An ADC (analog to digital converter) converts the TIM pin voltage into a 6-bit code representing temperature every 100µs. This code is fed to a DAC (digital to analog converter) that creates an offset in the I_{SENSE} current. The amount of offset is programmable via the SMBus interface. The LSB of the DAC is approximately 2.5°C meaning that the I_{SENSE} signal is adjusted as temperature varies every 2.5°C.

Overcurrent Threshold and R_{ISENSE} Resistor Selection

The hiccup over current threshold is based upon the average I_{SENSE} current generated by all the configured phases and is programmed by the value of the R_{ISENSE} resistors as described by equations 3 and 4.

$IOCP_{AVG}$ = 2.5 x IREF = 49.75 µA if RIREF is the recommended 49.9kohm (equation 3)
$R_{ISENSE} = I_{OCP}$ x DCR / (49.75µA x # of configured phases (equation 4)

For a four phase converter with DCR = 0.8 mohm and a desired overcurrent threshold of 154A;
R_{ISENSE} = 154A x 0.8 mohm / (49.75µA x 4) = 619 ohms

Load Line and R_{FB} Selection

The I_{SENSE} currents from the configured phases are processed and the average value is outputed at the DROOP pin. The droop current is derived from all the configured phases regardless of whether any are disabled due to operation in a power savings mode.Connecting the DROOP and FB pins together enables the current sourced in the DROOP pin to develop a voltage across the FB resistor and implement a load line. Use Equation 5 to select the FB resistor value.

$R_{FB} = R_{DROOP} \times R_{SENSE} \times$ # of configured phases / DCR (equation 5)

For a four phase converter with DCR = 0.8 mohm, RISENSE = 619 ohms, and load line impedance of 1.4 mohms;

R_{FB} = 1.4 mohm x 619 ohm x 4 / 0.8 mohm = 4.33 kohm

IMON Load Current Signal

The I_{SENSE} currents from the configured phases are summed, processed, and sent out to the IMON pin. Use equation 6 to select the RIMON resistor value to program the IMON gain for a particular ICCMAX. Refer to the appropriate Intel VR11.1 specification for information on ICCMAX. An appropriate CIMON capacitor should be placed in parallel with the RIMON resistor to ensure the RC time constant exceeds 300µS.

$R_{IMON} = VIMON_{MAX} \times R_{ISENSE} \times$ # of configured phases / ($ICC_{MAX} \times$ DCR) (equation 6)

For a four phase converter with DCR = 0.8 mohm, ICC_{MAX} of 120A, R_{ISENSE} = 619 ohms, and $VIMON_{MAX}$ = 0.95V;

R_{IMON} = 0.95V * 619 ohms * 4 / (120A x 0.8mohm) = 24.5kohm

VID Programming

The IDTP62000 supports the four VID (voltage identification) tables; Intel VR10.x, Intel VR11.x, AMD 6 bit parallel VID (PVID), and AMD 7 bit serial VID (SVID). The VID_SEL pin must be configured to select the appropriate VID table.

- Connect the VID_SEL pin to ground (GND) to select VR10.x 7 bit VID
- Float the VID_SEL pin or bias it to a voltage between 0.8V and 1.8V to select VR11.x 8 bit VID
- Connect the VID_SEL pin to 5V (VDD) to select an AMD VID
  - If VID1 is low when the IDTP62000 is enabled 7 bit SVID mode is activated
  - If VID1 is high when the IDTP62000 is enabled 6 bit PVID mode is activated

For Intel modes the VID pins are internally biased high to 1.2V logic levels. For AMD modes the pins are internally biased low. In AMD SVI mode VID2 is the SVD input, VID3 is the SVC input, and VID [7:4] and VID [1:0] are biased low internally. In AMD SVI mode the boot voltage is determined by the SVC (VID3) and SVD (VID2) bias upon enable as follows:

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

The VID inputs are monitored and, if stable for 200ns, the IDTP62000 recognizes the new code and changes the internal DAC reference to the new level. In Intel modes the internal reference voltage transitions up at a fixed rate of 12.5mV per microsecond and down at 6.25mV per microsecond. In AMD mode the reference voltage transitions at a fixed rate of 3.125mV per microsecond.

Registers

Memory Map

Command and Status Registers		
Offset	**Register Name**	**Description**
0x00	DEV_CTRL1	Device control register
0x01	DEV_CTRL2	Device control register
0x02	DEV_STAT1	Device status register
0x03	DEV_STAT2	Device status register
0x04	VID_CTRL	VID control register
0x05	VID_DAC_STAT	VID code at input of DAC status register
0x06	VID_INPUT_STAT	Loaded VID from pins status and control register
0x07	OVP_UVP_ADJUST	Over-voltage offset level register
0x08	PSI_CTRL	PSI control register
0x09	TM_STAT	TM value + TC_OFFSET status register
0x0A	TEMP_OFFSET	TM_OFFSET and TC_OFFSET register
Dynamic Efficiency Control Registers		
Offset	**Register Name**	**Description**
0x20	DEC_CTRL	DEC control register
0x21	DEC_SS_DELAY	Soft start to DEC delay register
0x22	DEC_WIN	DEC window filter register
0x23	DEC_LEVEL1_H	DEC one phase load level upper threshold register
0x24	DEC_LEVEL1_L	DEC one phase load level lower threshold register
0x25	DEC_LEVEL2_H	DEC two phase load level upper threshold register
0x26	DEC_LEVEL2_L	DEC two phase load level lower threshold register
0x27	DEC_LEVEL3_H	DEC three phase load level upper threshold register
0x28	DEC_LEVEL3_L	DEC three phase load level lower threshold register
Dynamic Voltage Change Registers		
Offset	**Register Name**	**Description**
0x30	DVC_CTRL	DVC control register
0x31	DVC_WIN	DVC window filter register
0x32	DVC_DFC_DELAY	DVC Vcore delay register
0x33	DVC_SS_DELAY	Soft start to DVC delay register
0x34	DVC00_VID_OFFSET	DVC00 mode DVID is offset register
0x35	DVC01_VID_OFFSET	DVC01 mode DVID is offset register
0x36	DVC10_VID_OFFSET	DVC10 mode DVID is offset register
0x37	DVC11_VID_OFFSET	DVC11 mode DVID is offset register
0x38	DVC_LEVEL1_H	DVC load level1 upper threshold register
0x39	DVC_LEVEL1_L	DVC load level1 lower threshold register
0x3A	DVC_LEVEL2_H	DVC load level2 upper threshold register
0x3B	DVC_LEVEL2_L	DVC load level2 lower threshold register
0x3C	DVC_LEVEL3_H	DVC load level3 upper threshold register
0x3D	DVC_LEVEL3_L	DVC load level3 lower threshold register

Register Bit-Type Descriptions

The following codes are used to describe register bit types:

Type	Description
R/W	Read/Write: Register bit may be written and read by the user
RC	Read Clear: Register bit may not be written by user (writes are ignored), but is set by the IDTP62000 device when appropriate. When read by the user, the bit will be cleared.
RO	Read Only: Register bit may not be written by user (writes are ignored), but is set by the IDTP62000 device. When read by the user, the bit retains its value.
WO	Write Only: Writing the register initiates some sort of one-time action. Reading the register always returns 0, as though the address was undefined. In fact, there may be no physical register present.
R/W or RO	Read/Write or Read Only: Depending on the value of a controlling CSR bit, this register may or may not be written. It may always be read.

Device Control Registers

DEV_CTRL1 (Offset = 00h)

DEV_CTRL1[3:0] shall not directly control the DEC or PSI functions, but rather they indicate which phases may be used. However, if any of these bits are over-written then, DEC and/or PSI shall step up to the maximum allowable number of phases and then resume normal operation.

Bit	Name	Control Function	Type	Default
7	SOFT_RESET	Write 1 to reset all status registers to defaults and begin soft start (identical to resetting via the UVLO_PVCC pin)	WO	
6	Reserved			
5	GPO_EN	GPO Interface Select 0b = Disable 1b = Enable If SIF_EN=1b then this GPO_EN is ignored.	R/W	0b
4	SIF_EN	SIF Interface Select 0b = Disable 1b = Enable	R/W	0b
3	Phase4	Phase #4 enable/disable 0b = Disable 1b = Enable	R/W	Pin control – PWM4
2	Phase3	Phase #3 enable/disable 0b = Disable 1b = Enable	R/W	Pin control – PWM4
1	Phase2	Phase #2 enable/disable 0b = Disable 1b = Enable	R/W	1b
0	Phase1	Phase #1 enable/disable. This phase is always enabled 0b = N/A 1b = Enable	RO	1b

DEV_CTRL2 (Offset = 01h)

Bit	Name	Control Function	Type	Default
7	VID_CSR_WRITE_EN	This bit has two functions: 1) Controls how the VID_INPUT_STAT register is written. 0: VID_INPUT_STAT is modified only by the external VID[7:0] pins, and becomes a read only CSR 1: VID_INPUT_STAT ignores the external VID[7:0] pins and may only be modified by CSR writes. 2) Controls the ability to write to the VID_MODE[1:0] field 0: RO 1: R/W	R/W	0b
6:4	Reserved			
3:0	SIF_CMD_EN[4:0]	If SIF_CMD_EN[n] = 0, then SIF command 'n' is disabled. 3: OCP 2: OVP 1: VR_HOT 0: VR_FAN	R/W	1111b

Device Status Registers

DEV_STAT1 (Offset = 02h)

These bits are cleared when read.

Bit	Name	Control Function	Type	Default
7	OVP_ALERT	Over-Voltage Protection Alert Asserted when an over-voltage shutdown has occurred. 0b = Normal 1b = Warning	RC	0b
6	OCP_ALERT	Over-Current Protection Alert Asserted when an over-current shutdown has occurred. 0b = Normal 1b = Warning	RC	0b
5	UVP_ALERT	Under-Voltage Protection Alert 0b = Normal 1b = Warning	RC	0b
4	VRHOT_ALERT	VR_HOT Alert 0b = Normal 1b = Warning Always 0 if THERM_EN is low.	RC	0b
3	VRFAN_ALERT	VR_FAN Alert 0b = Normal 1b = Warning Always 0 if THERM_EN is low.	RC	0b
2	OCP_WARN	Over-Current Protection Warning Asserted when an over-current condition has been detected and hiccup mode has been entered 0b = Normal 1b = Warning	RC	0b
1	OVP_WARN	Over-Voltage Protection Warning Asserted when an over-voltage condition has been detected, even if that event does not lead to shutdown (as with some Intel soft start situations). 0b = Normal 1b = Warning	RC	0b
0	Reserved			

DEV_STAT2 (Offset = 03h)

RO indicates that the register is read only and RC indicates that the register is cleared when read.

Bit	Name	Control Function	Type	Default
7:6	ACTIVE_PH_NUM[1:0]	Number of phases currently active. This will always be equal to the sum of 1's in DEV_CTRL1[3:0] unless DEC or PSI is active. 00b = 1 phase 01b = 2 phases 10b = 3 phases 11b = 4 phases	RO	
5:4	Reserved			
3:0	Reserved			

VID Code Registers

VID_CTRL (Offset = 04h)

Bit	Name	Control Function	Type	Default
7:6	VID_MODE[1:0]	Voltage regulator mode 00b = VR10 01b = VR11 10b = AMD PVI 11b = AMD SVI This bit may not be written unless VID_CSR_WRITE_EN = 1b	R/W or RO	Defined by VID_SEL and VID[1] pins
5	DVID_EN	Dynamic VID control enable If high, then changes to the VID_INPUT_STAT register are copied to the VID_DAC_STAT register. If low, the VID_DAC_STAT register cannot be changed. When this bit is low and DVC mode is enabled, then the PSI input will be ignored (since the DAC input codes cannot be updated).	R/W	1b
4	VID_OFFSET_EN	VID offset adjustment enable When DVC_EN=1b then regardless of the value contained in this register, the VID_OFFSET will never be enabled.	R/W	0b
3:0	Reserved			

VID_DAC_STAT (Offset = 05h)

This register is always loaded by transferring the value from the VID_INPUT_STAT register (based on the DVID_EN field of the VID_CTRL CSR register), and indicates the VID code currently being used by the DAC. It does not include the effect of any offsets induced by enabling the VID_OFFSET_EN field in the VID_CTRL CSR register.

Bit	Name	Type	Type	Default
7:0	VID_DAC[7:0]	Current VID input setting of DAC	RO	00b

VID_INPUT_STAT (Offset = 06h)

This register is written by either the external VID[7:0] pins or by a CSR write, depending on the value of VID_CSR_WRITE_EN in the DEV_CTRL2 register.

Bit	Name	Type	Type	Default
7:0	VID_INPUT[7:0]	Loaded VID setting This field may not be written unless VID_CSR_WRITE_EN = 1b	R/W or RO	Defined by VID[7:0] pins

UVP and OVP Registers

UVP_OVP_ADJUST (Offset = 07h).

Bit	Name	Type	Type	Default
7:4	Reserved			
3:2	OVP_ OFFSET [1:0]	Over-Voltage protection Level, OVP level will be VREF+OVP_offset 00b = 200mV 01b = 250mV 10b = 300mV 11b = 350mV	R/W	01b
1:0	UVP_ LEVEL [1:0]	Under-Voltage Protection Level. 00 = 80% 01 = 70% 10 = 60% 11 = 50% Hystersis is 10% for all options so that UV is cleared when the voltage rises to UV trip + 10% of the VID setting.	R/W	10b

PSI Registers

PSI_CTRL (Offset = 08h)

This register controls the behavior of the PSI function. The PSI state may be forced by setting the PSI# bit. PSI_PHASE[1:0] determines the minimum number of active phases allowed when PSI mode is active. The active phase status may be read from DEV_CTRL1.

Bit	Name	Type	Type	Default
7	PSI#_EN	PSI# Phase Switching function control bit 0b= Disable 1b= Enable	R/W	1b
6	PSI#	PSI# status 0b= PSI# asserted 1b= PSI# de-asserted	RO	Pin Control
5	PSI_FILTER[5:3]	PSI_FILTER[5] 0b = Disable Filter 1b = Enable Filter PSI_FILTER[4:3] 00b = 128us 01b = 256us 10b = 512us 11b = 1024us	R/W	111b
2	Reserved			
1:0	PSI_PHASE[1:0]	Number of phases that device can downgrade to. If APS is enabled, then this field is ignored and a PSI low event downgrades to APS_PHASE[1:0] 00b/01b=1 phase 10b=2 phases 11b= 3 phases	R/W	01b

Thermal Monitor and Temperature Compensation Registers

TM_STAT (Offset = 09h)

Bit	Name	Control Function	Type	Default
7	TCOMP_EN	Enable Internal Temperature Compensation 0b = Disable 1b = Enable	R/W	Pin Control based on IREF
6	THERM_EN	Enables thermal overstress detection when high. When low, VR_HOT and VR_FAN stay low. 0b = Disable 1b = Enable	R/W	1b
5:0	TEMP[5:0]	Temperature reading on TM pin adjusted by TC_OFFSET and is continuously updated as the part detects new values. Temperature in Centigrade is TEMP[5:0]*2.5 - 15	RO	Pin control

TEMP_OFFSET (Offset = 0Ah)

Bit	Name	Control Function	Type	Default
7:5	TM_OFFSET[2:0]	Offset for VR_HOT and VR_FAN LSB = 5 C. 011b = +20 C 100b = +0 C 010b = +15 C 101b = -5 C 001b = +10 C 110b = -10 C 000b = +5 C 111b = -15 C	R/W	100b
4:0	TC_OFFSET[4:0]	Current scale factor for sensed CSA current. LSB = 2.5 C offset 1xxxxb = Negative offset 0xxxxb = Positive offset 11111b = Disable Temp Comp. Note: 10000b = 00000b= No offset	R/W	1Fx

DEC Registers

DEC_CTRL (Offset = 20h)

Bit	Name	Type	Type	Default
7	DEC_EN	DEC Control. 0b = Disable 1b = Enable If FUSE_DEC_ENABLE = 0, DEC is disabled regardless of DEC_EN.	R/W	0b
6:4	Reserved			
3:2	DEC_PHASE[1:0]	Control for minimum number of phases to be used. This also overrides PSI_PHASE when in DEC mode. 00b/01b = 1 phase 10b = 2 phases 11b = 3 phases	R/W	01b
1:0	Reserved			

DEC_SS_DELAY (Offset = 21h)

Bit	Name	Type	Type	Default
7	Reserved			
6:0	DEC_SS_DELAY[6:0]	Delay after soft start after which DEC operations can occur, 4ms/per LSB.	R/W	0Fx

DEC_WIN (Offset = 22h)

This register defines the window over which the IDTP62000 shall detect whether the load level has crossed a certain user-defined load level. The load level must stay over the threshold for at least 50% of the window period to be considered as a successful level crossing.

Bit	Name	Type	Type	Default
7	Reserved			
6:0	DEC_WIN[6:0]	DEC detection window, 4ms/per LSB.	R/W	0Fx

DEC_LEVEL1_H (Offset = 23h)

This value must be lower than DEC_LEVEL2_x if APS is enabled. It establishes the current level which must be exceeded for a transition from 1 phase to 2 phases to occur.

Bit	Name	Type	Type	Default
4:0	DEC_LEVEL1_H[4:0]	Transition current level is given by I_{OCAVG} * (LEVEL[4:0] + 1)/32	R/W	00x

DEC_LEVEL1_L (Offset = 24h)

This value must be lower than DEC_LEVEL2_x if DEC is enabled. It establishes the current level which must be dropped below for a transition from 2 phases to 1 phase to occur.

Bit	Name	Type	Type	Default
4:0	DEC_LEVEL1_L[4:0]	Transition current level is given by I_{OCAVG} * (LEVEL[4:0] + 1)/32	R/W	00x

DEC_LEVEL2_H (Offset = 25h)

This value must be greater than DEC_LEVEL1_x and less than DEC_LEVEL3_x if DEC is enabled. It establishes the current level which must be exceeded for a transition from 2 phases to 3 phases to occur.

Bit	Name	Type	Type	Default
7:5	Reserved			
4:0	DEC_LEVEL2_H[4:0]	Transition current level is given by I_{OCAVG} * (LEVEL[4:0] + 1)/32	R/W	00x

DEC_LEVEL2_L (Offset = 26h)

This value must be greater than DEC_LEVEL1_x and less than DEC_LEVEL3_x if DEC is enabled. It establishes the current level which must be dropped below for a transition from 3 phases to 2 phases to occur.

Bit	Name	Type	Type	Default
7:5	Reserved			
4:0	DEC_LEVEL2_L[4:0]	Transition current level is given by I_{OCAVG} * (LEVEL[4:0] + 1)/32	R/W	00x

DEC_LEVEL3_H (Offset = 27h)

The value must be greater than DEC_LEVEL2_x if DEC is enabled. It establishes the current level which must be exceeded for a transition from 3 phases to 4 phases to occur.

Bit	Name	Type	Type	Default
7:5	Reserved			
4:0	DEC_LEVEL3_H[4:0]	Transition current level is given by I_{OCAVG} * (LEVEL[4:0] + 1)/32	R/W	00x

DEC_LEVEL3_L (Offset = 28h)

The value must be greater than DEC_LEVEL2_x if DEC is enabled. It establishes the current level which must be dropped below for a transition from 4 phases to 3 phases to occur.

Bit	Name	Type	Type	Default
7:5	Reserved			
4:0	DEC_LEVEL3_L[4:0]	Transition current level is given by I_{OCAVG} * (LEVEL[4:0] + 1)/32	R/W	00x

DVC Registers

DVC_CTRL (Offset = 30h)

DVC operation shall be disabled if the DVC_EN field contains 0.

Bit	Name	Control Function	Type	Default
7	DVC_EN	Enable DVC operation 0b = Disable 1b=Enable If DVC_EN=1 and DVID_EN=0, then PSI# assertions will be ignored.	R/W	0b
6:0	Reserved			

DVC_WIN (Offset = 31h)

This register defines the window over which the IDTP62000 shall detect whether the load level has crossed a certain user-defined load level. The load level must be stay over the level for at least 50% of the window period to be considered a successful level crossing.

Bit	Name	Control Function	Type	Default
7	Reserved			
6:0	DVC_WIN[6:0]	DVC detection window, 1ms/per LSB. This window filter is activated on when a threshold level is crossed.	R/W	0Fx

DVC_DFC_DELAY (Offset = 32h)

Bit	Name	Control Function	Type	Default
7	Reserved			
6:0	DVC_DFC_DELAY [6:0]	DVC/DFC delay time control register. When DVC indicates that Vcore needs to be lowered, the DVC information is sent to the SCPC and the timer is started (4ms/bit). On timer completion, the Vcore voltage is lowered.	R/W	0Fx

DVC_SS_DELAY (Offset = 33h)

Bit	Name	Control Function	Type	Default
7	Reserved			
6:0	DVC_SS_DELAY [6:0]	Delay after soft start after which DVC operations can occur, 4ms/per LSB. This value may not be 0.	R/W	0Fx

DVC00_VID_OFFSET (Offset = 34h)

Indicates the offset voltage to be added to or subtracted from the active VID code while the device is in mode DVC00. This value is also used as an offset when not in DVC mode if VID_OFFSET_EN is high.

Bit	Name	Control Function	Type	Default
7	DVC00_VID_OFFSET [7]	Sign of the offset: 0b = positive 1b = negative	R/W	0b
6:0	DVC00_VID_OFFSET [6:0]	Magnitude of the offset (1 LSB = 6.25 mV)	R/W	00x

DVC01_VID_OFFSET (Offset = 35h)

Indicates the offset voltage to be added to or subtracted from the active VID code while the device is in mode DVC01.

Bit	Name	Control Function	Type	Default
7	DVC01_VID_OFFSET [7]	Sign of the offset: 0b = positive 1b = negative	R/W	0b
6:0	DVC01_VID_OFFSET [6:0]	Magnitude of the offset (1 LSB = 6.25 mV)	R/W	00x

DVC10_VID_OFFSET (Offset = 36h)

Indicates the offset voltage to be added to or subtracted from the active VID code while the device is in mode DVC10.

Bit	Name	Control Function	Type	Default
7	DVC10_VID_OFFSET [7]	Sign of the offset: 0b = positive 1b = negative	R/W	0b
6:0	DVC10_VID_OFFSET [6:0]	Magnitude of the offset (1 LSB = 6.25 mV)	R/W	00x

DVC11_VID_OFFSET (Offset = 37h)

Indicates the offset voltage to be added to or subtracted from the active VID code while the device is in mode DVC11.

Bit	Name	Control Function	Type	Default
7	DVC11_VID_OFFSET [7]	Sign of the offset: 0b = positive 1b = negative	R/W	0b
6:0	DVC11_VID_OFFSET [6:0]	Magnitude of the offset	R/W	00x

DVC_LEVEL1_H (Offset = 38h)

This value must be lower than DVC_LEVEL2_x if DVC is enabled. It establishes the current level which must be exceeded for a transition from DVC00 to DVC01 to occur.

Bit	Name	Control Function	Type	Default
7:5	Reserved			
4:0	DVC_LEVEL1_H [4:0]	Transition current level is given by I_{OCAVG} * (LEVEL[4:0] + 1)/32	R/W	00x

DVC_LEVEL1_L (Offset = 39h)

This value must be lower than DVC_LEVEL2_x if DVC is enabled. It establishes the current level which must be dropped below for a transition from DVC01 to DVC00 to occur.

Bit	Name	Control Function	Type	Default
7:5	Reserved			
4:0	DVC_LEVEL1_L [4:0]	Transition current level is given by I_{OCAVG} * (LEVEL[4:0] + 1)/32	R/W	00x

DVC_LEVEL2_H (Offset = 3Ah)

This value must be greater than DVC_LEVEL1_x and less than DVC_LEVEL3_x if DVC is enabled. It establishes the current level which must be exceeded for a transition from DVC01 to DVC10 to occur.

Bit	Name	Control Function	Type	Default
7:5	Reserved			
4:0	DVC_LEVEL2_H [4:0]	Transition current level is given by I_{OCAVG} * (LEVEL[4:0] + 1)/32	R/W	00x

DVC_LEVEL2_L (Offset = 3Bh)

This value must be greater than DVC_LEVEL1_x and less than DVC_LEVEL3_x if DVC is enabled. It establishes the current level which must be dropped below for a transition from DVC10 to DVC01 to occur.

Bit	Name	Control Function	Type	Default
7:5	Reserved			
4:0	DVC_LEVEL2_L [4:0]	Transition current level is given by I_{OCAVG} * (LEVEL[4:0] + 1)/32	R/W	00x

DVC_LEVEL3_H (Offset = 3Ch)

The value must be greater than DVC_LEVEL2_x if DVC is enabled. It establishes the current level which must be exceeded for a transition from DVC10 to DVC11 to occur.

Bit	Name	Control Function	Type	Default
7:5	Reserved			
4:0	DVC_LEVEL3_H [4:0]	Transition current level is given by I_{OCAVG} * (LEVEL[4:0] + 1)/32	R/W	00x

DVC_LEVEL3_L (Offset = 3Dh)

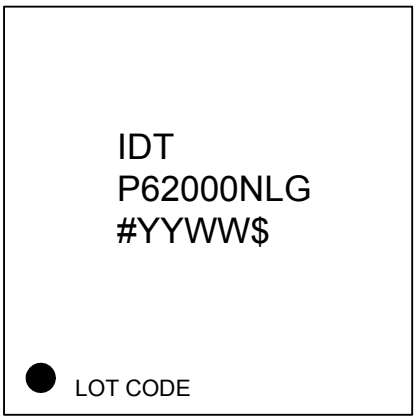
The value must be greater than DVC_LEVEL2_x if DVC is enabled. It establishes the current level which must be dropped below for a transition from DVC11 to DVC10 to occur.

Bit	Name	Control Function	Type	Default
7:5	Reserved			
4:0	DVC_LEVEL3_L [4:0]	Transition current level is given by I_{OCAVG} * (LEVEL[4:0] + 1)/32	R/W	00x

Glossary

Term	Description
AVP	Adaptive Voltage Positioning
CSR	Command and Status Register
DCR	Direct Current Resistance
DEC	Dynamic Efficiency Control
DFC	Dynamic Frequency Change
DVC	Dynamic Voltage Change
D-VID	Dynamic Voltage Identification. A low power mode of operation where the processor instructs the VRD to operate at a lower voltage.
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
Icc	Processor current
Itt	Bus current associated with the Vtt supply
Load Line	A mathematical model that describes voltage current relationship given system impedance (R_{LL}). The load line equations is $V_{cc} = VID - I*R_{LL}$. In this document, the load line is referenced at the socket unless otherwise stated.
NTC	Negative Thermal Coefficient
OCP	Over-current protection
OVP	Over-voltage protection
PROCHOT#	Under thermal monitoring, the VRD asserts this processor input to indicate an over-temperature condition has occurred. Assertion of this signal places the processor in a low power state, thereby cooling the voltage regulator.
PVI	AMD K8 Parallel VID interface
PWM	Pulse Width Modulation
RDS-ON	FET source to drain channel resistance when bias on.
RLL	Load line impedance. Defined as the ratio: Voltage droop/current step. This is the load line slope.
SCPC	System Clock Power Console
SIF	Serial interface to SCPC chip
Static Load Line	DC resistance at the defined regulation node. Defined as the quotient of voltage and current (V/I) under steady state conditions. This value is configured by proper tuning of the PWM controller voltage positioning circuit.
SVI	AMD K8 Serial VID Interface
Thermal Monitor	A feature of the voltage regulator that places the processor in a low power state when critical VRD temperatures are reached, thereby reducing power and VRD temperature.
TOB	Vcc regulation tolerance band. Defines the voltage regulator's 3-σ voltage variation across temperature, manufacturing variation, and aging factors. Must be ensured by design through component selection. Defined at processor maximum current and maximum VID levels.
Transient Load Line	Equal to dV/di or Vdroop/Istep and is controlled by switching frequency, decoupling capacitor selection, motherboard layout parasitics.
V_{CORE}	Processor core voltage identification defined in the processor datasheet.
VID	Voltage Identification: 1. A code supplied by the processor that determines the reference output voltage to be delivered to the processor V_{CORE} lands. 2. VID is the voltage at the processor at zero amperes and the tolerance band at + 3-σ.
VR_TDC	Voltage Regulator Thermal Design Current. The sustained DC current which the voltage regulator must support under the system defined cooling solution.
VRD	Voltage regulator down. A VR circuit resident on the motherboard.
VRDn	The Intel voltage reference specification level n.
VRM	Voltage regulator module that is socketed to a motherboard.
Vtt	Voltage provided to the processor to initiate power up and drive I/O buffer circuits.

Marking Diagram

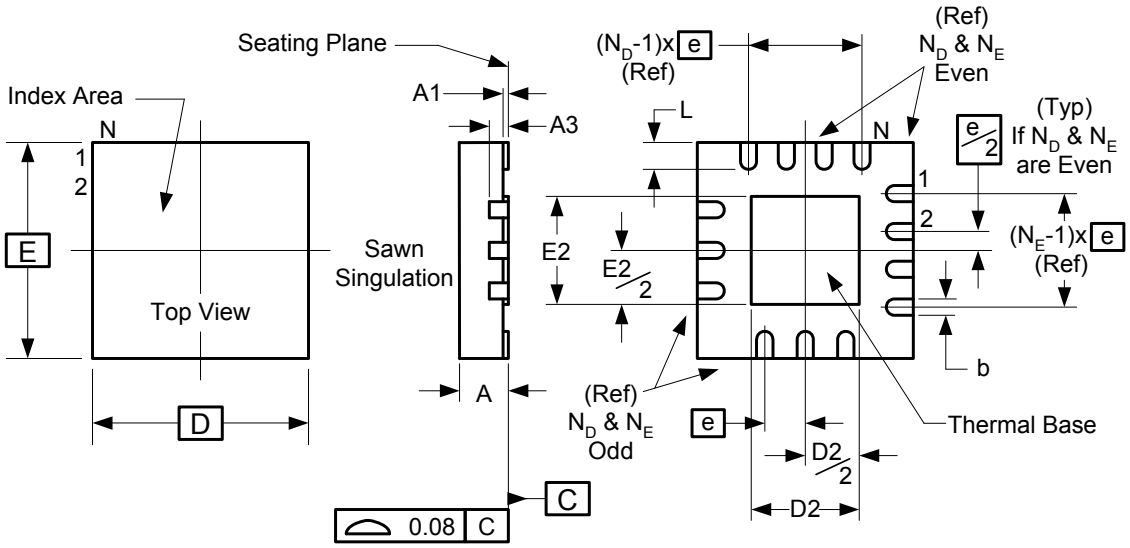


Notes:

1. “LOT CODE” is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “G” denotes Pb (lead) free package, RoHS compliant.
4. Bottom marking: country of origin.

Package Outline and Package Dimensions (64-pin QFN)

Package dimensions are kept current with JEDEC Publication No. 95 (NOTE: For drawing clarity, all pins are not shown)



	Millimeters	
Symbol	**Min**	**Max**
A	0.80	1.00
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N	64	
N_D	16	
N_E	16	
D x E BASIC	9.00 x 9.00	
D2	6.00	6.25
E2	6.00	6.25
L	0.30	0.50

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
P62000NLG	TBD	Tubes	64-pin QFN	0 to +85°C
P62000NLG8		Tape and Reel	64-pin QFN	0 to +85°C

"G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
A		10/28/09	Preliminary Release.
B		12/10/09	Updated pinout/description; added updated block diagram; added Component Values table; corrected formatting issues.
C		12/18/09	Multiple and various changes throughout datasheet per design review.
D		04/20/10	1. Updated part number from IDT9P62000 to IDTP62000. 2. Update Block Diagram 3. Update pin description 4. Update all electrical char tables 5. Update Introduction section 6. Update Output Voltage Offset Programming section 7. Added Input Under Voltage and Enable/Disable section 8. Added Application Information section 9. Updates to register tables 10. Update 4-Phase Component Values table

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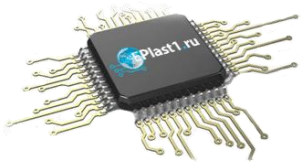
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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