

# 9-Mbit (256K × 36) Flow-Through SRAM

## Features

- Supports 133 MHz bus operations
- 256K × 36 common I/O
- 3.3 V – 5% and +10% core power supply ( $V_{DD}$ )
- 2.5 V or 3.3 V I/O power supply ( $V_{DDQ}$ )
- Fast clock-to-output times
  - 6.5 ns (133-MHz version)
- Provide high performance 2-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- Available in Pb-free 100-pin TQFP package
- “ZZ” sleep mode option

## Functional Description

The CY7C1361KVE33 is a 3.3 V, 256K × 36 synchronous flow-through SRAMs, respectively designed to interface with high speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133 MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ( $CE_1$ ), depth-expansion chip enables ( $CE_2$  and  $CE_3$ ), burst control inputs (ADSC, ADSP, and ADV), write enables ( $BW_x$ , and  $BWE$ ), and global write (GW). Asynchronous inputs include the output enable (OE) and the ZZ pin.

The CY7C1361KVE33 enables either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the processor address strobe (ADSP) or the cache controller address strobe (ADSC) inputs. Address advancement is controlled by the address advancement (ADV) input.

Addresses and chip enables are registered at rising edge of clock when either address strobe processor (ADSP) or address strobe controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin (ADV).

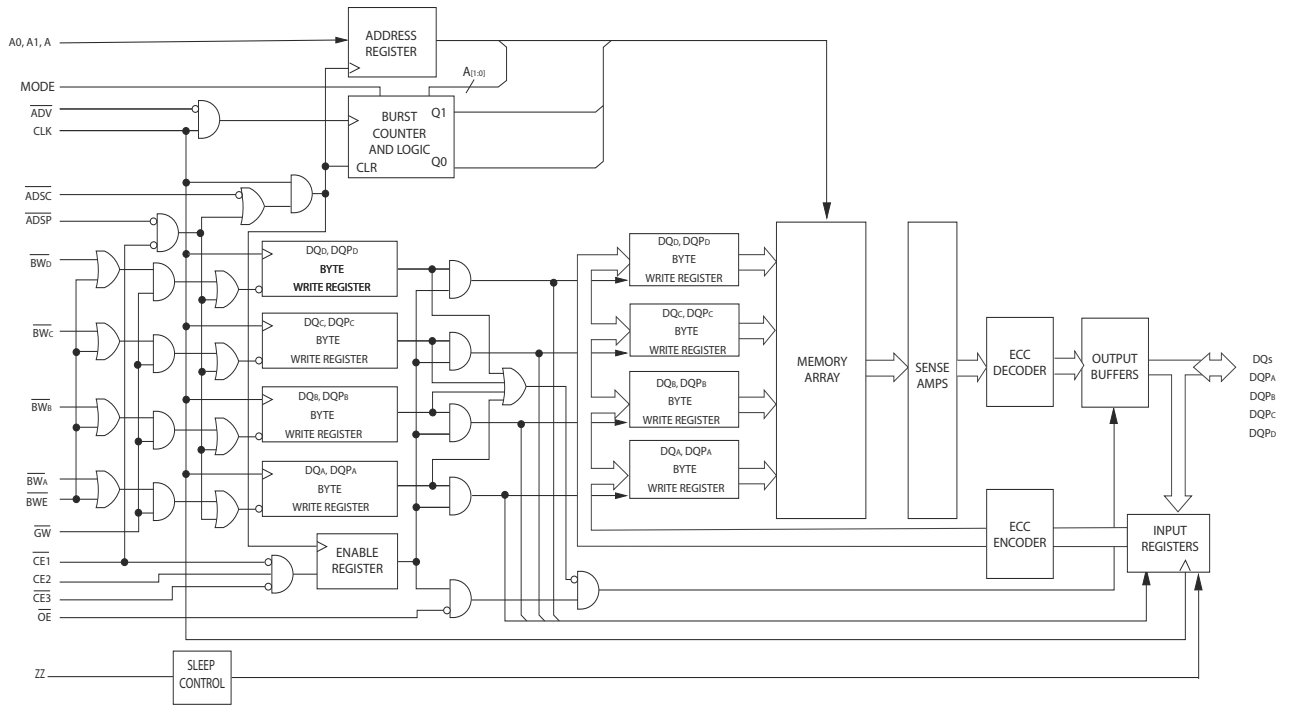
The CY7C1361KVE33 operates from a +3.3 V core power supply while all outputs may operate with either a +2.5 or +3.3 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

For a complete list of related documentation, click [here](#).

## Selection Guide

Description	133 MHz	Unit
Maximum access time	6.5	ns
Maximum operating current	149	mA

Logic Block Diagram – CY7C1361KVE33

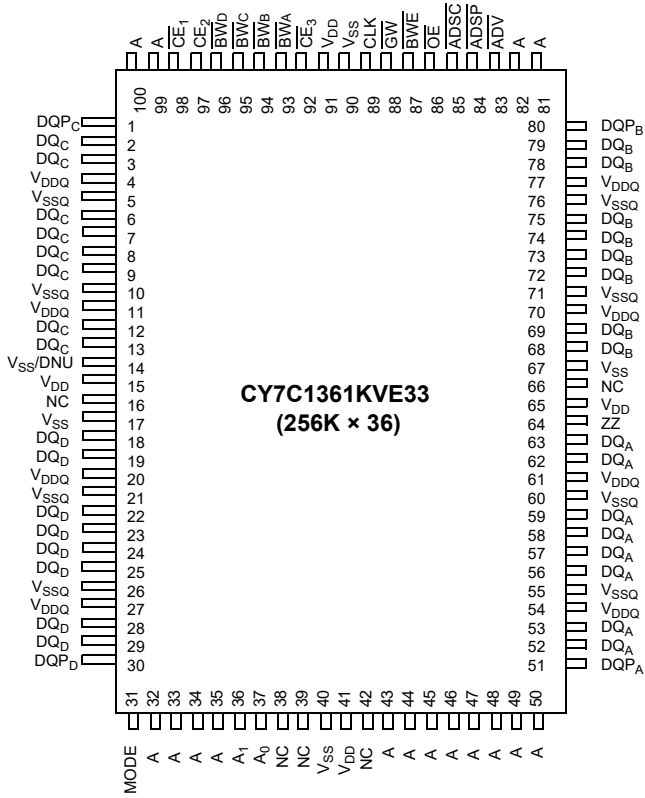


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### Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout



## Pin Definitions

Name	I/O	Description
A <sub>0</sub> , A <sub>1</sub> , A	Input-synchronous	<b>Address inputs used to select one of the address locations.</b> Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE}_1$ , CE <sub>2</sub> , and $\overline{CE}_3$ are sampled active. A <sub>[1:0]</sub> feed the 2-bit counter.
$\overline{BW}_A, \overline{BW}_B, \overline{BW}_C, \overline{BW}_D$	Input-synchronous	<b>Byte write select inputs, active LOW.</b> Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-synchronous	<b>Global write enable input, active LOW.</b> When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{BW}_X$ and $\overline{BWE}$ ).
CLK	Input-clock	<b>Clock input.</b> Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-synchronous	<b>Chip enable 1 input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>2</sub> and $\overline{CE}_3$ to select/deselect the device. ADSP is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE <sub>2</sub>	Input-synchronous	<b>Chip enable 2 input, active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE <sub>3</sub> to select/deselect the device. CE <sub>2</sub> is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-synchronous	<b>Chip enable 3 input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE <sub>2</sub> to select/deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-asynchronous	<b>Output enable, asynchronous input, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
ADV	Input-synchronous	<b>Advance input signal, sampled on the rising edge of CLK.</b> When asserted, it automatically increments the address in a burst cycle.
ADSP	Input-synchronous	<b>Address strobe from processor, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ADSP is ignored when $\overline{CE}_1$ is deasserted HIGH.
ADSC	Input-synchronous	<b>Address strobe from controller, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
$\overline{BWE}$	Input-synchronous	<b>Byte write enable input, active LOW.</b> Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
ZZ	Input-asynchronous	<b>ZZ “sleep” input, active HIGH.</b> When asserted HIGH places the device in a non-time-critical “sleep” condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull down.
DQ <sub>s</sub>	I/O-synchronous	<b>Bidirectional data I/O lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQ <sub>s</sub> and DQP <sub>x</sub> are placed in a tristate condition. The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of OE.
DQP <sub>x</sub>	I/O-synchronous	<b>Bidirectional data parity I/O lines.</b> Functionally, these signals are identical to DQ <sub>s</sub> . During write sequences, DQP <sub>x</sub> is controlled by $\overline{BW}_X$ correspondingly.
MODE	Input-static	<b>Selects burst order.</b> When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
V <sub>DD</sub>	Power supply	<b>Power supply inputs to the core of the device.</b>
V <sub>DDQ</sub>	I/O power supply	<b>Power supply for the I/O circuitry.</b>
V <sub>SS</sub>	Ground	<b>Ground for the core of the device.</b>

**Pin Definitions** (continued)

Name	I/O	Description
V <sub>SSQ</sub>	I/O ground	<b>Ground for the I/O circuitry.</b>
NC	–	<b>No connects.</b> Not internally connected to the die. 18M, 36M, 72M, 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die.
V <sub>SS</sub> /DNU	Ground/DNU	This pin can be connected to ground or should be left floating.

**Functional Overview**

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t<sub>CDV</sub>) is 6.5 ns (133 MHz device).

The CY7C1361KVE33 supports secondary cache in systems using either a linear or interleaved burst sequence. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe (ADSP) or the controller address strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable (BWE) and byte write select (BW<sub>X</sub>) inputs. A global write enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip selects ( $\overline{CE}_1$ , CE<sub>2</sub>,  $\overline{CE}_3$ ) and an asynchronous output enable (OE) provide for easy bank selection and output tristate control. ADSP is ignored if CE<sub>1</sub> is HIGH.

**Single Read Accesses**

A single read access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE}_1$ , CE<sub>2</sub>, and  $\overline{CE}_3$  are all asserted active and (2) ADSP or ADSC is asserted LOW (if the access is initiated by ADSC, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the OE input is asserted LOW, the requested data will be available at the data outputs a maximum to t<sub>CDV</sub> after clock rise. ADSP is ignored if CE<sub>1</sub> is HIGH.

**Single Write Accesses Initiated by ADSP**

This access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE}_1$ , CE<sub>2</sub>,  $\overline{CE}_3$  are all asserted active and (2) ADSP is asserted LOW. The addresses presented are loaded into the address register and the burst inputs (GW, BWE, and BW<sub>X</sub>) are ignored during this first clock cycle. If the write inputs are asserted active (see [Partial Truth Table for Read/Write on page 9](#) for appropriate states that indicate a write) on the next

clock rise, the appropriate data will be latched and written into the device. Byte writes are allowed. All I/Os are tristated during a byte write. Since this is a common I/O device, the asynchronous OE input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to DQs. As a safety precaution, the data lines are tristated once a write cycle is detected, regardless of the state of OE.

**Single Write Accesses Initiated by ADSC**

This write access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE}_1$ , CE<sub>2</sub>, and  $\overline{CE}_3$  are all asserted active, (2) ADSC is asserted LOW, (3) ADSP is deasserted HIGH, and (4) the write input signals (GW, BWE, and BW<sub>X</sub>) indicate a write access. ADSC is ignored if ADSP is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to DQ<sub>[A:D]</sub> is written into the specified address location. Byte writes are allowed. All I/Os are tristated when a write is detected, even a byte write. Since this is a common I/O device, the asynchronous OE input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to DQs. As a safety precaution, the data lines are tristated once a write cycle is detected, regardless of the state of OE.

**Burst Sequences**

The CY7C1361KVE33 provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by A<sub>[1:0]</sub>, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE will select a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to a interleaved burst sequence.

**Interleaved Burst Address Table**

(MODE = Floating or V<sub>DD</sub>)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

**Linear Burst Address Table**

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

**Sleep Mode**

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation 'sleep' mode. Two clock cycles are required to enter into or exit from this 'sleep' mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the 'sleep' mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the 'sleep' mode.  $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{CE}_3$ ,  $\overline{ADSP}$ , and  $\overline{ADSC}$  must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

**ZZ Mode Electrical Characteristics**

Parameter	Description	Test Conditions	Min	Max	Unit
$I_{DDZZ}$	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2 V$	–	65	mA
$t_{ZZS}$	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2 V$	–	$2t_{CYC}$	ns
$t_{ZZREC}$	ZZ recovery time	$ZZ \leq 0.2 V$	$2t_{CYC}$	–	ns
$t_{ZZI}$	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
$t_{RZZI}$	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

## Truth Table

The Truth Table for CY7C1361KVE33 follows. [1, 2, 3, 4, 5]

Cycle Description	Address Used	$\overline{CE}_1$	$CE_2$	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected cycle, power-down	None	H	X	X	L	X	L	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	L	X	L	L	X	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	X	H	L	L	X	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	L	X	L	H	L	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	X	X	H	L	H	L	X	X	X	L-H	Tri-state
Sleep mode, power-down	None	X	X	X	H	X	X	X	X	X	X	Tri-state
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	H	L-H	Tri-state
Write cycle, begin burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	H	L-H	Tri-state
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tri-state
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tri-state
Write cycle, continue burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write cycle, continue burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tri-state
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tri-state
Write cycle, suspend burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write cycle, suspend burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

### Notes

- $\overline{X}$  = "Don't Care." H = Logic HIGH, L = Logic LOW.
- $\overline{WRITE}$  = L when any one or more byte write enable signals and  $\overline{BWE} = L$  or  $\overline{GW} = L$ .  $\overline{WRITE} = H$  when all byte write enable signals,  $\overline{BWE}$ ,  $\overline{GW} = H$ .
- The DQ pins are controlled by the current cycle and the  $\overline{OE}$  signal.  $\overline{OE}$  is asynchronous and is not sampled with the clock.
- The  $\overline{SRAM}$  always initiates a read cycle when  $\overline{ADSP}$  is asserted, regardless of the state of  $\overline{GW}$ ,  $\overline{BWE}$ , or  $\overline{BW}_x$ . Writes may occur only on subsequent clocks after the  $\overline{ADSP}$  or with the assertion of  $\overline{ADSC}$ . As a result,  $\overline{OE}$  must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state.  $\overline{OE}$  is a don't care for the remainder of the write cycle.
- $\overline{OE}$  is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when  $\overline{OE}$  is inactive or when the device is deselected, and all data bits behave as output when  $\overline{OE}$  is active (LOW).



## Partial Truth Table for Read/Write

The Partial Truth Table for Read/Write for CY7C1361KVE33 follows. [6, 7]

Function (CY7C1361KVE33)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write byte (A, DQP <sub>A</sub> )	H	L	H	H	H	L
Write byte (B, DQP <sub>B</sub> )	H	L	H	H	L	H
Write bytes (B, A, DQP <sub>A</sub> , DQP <sub>B</sub> )	H	L	H	H	L	L
Write byte (C, DQP <sub>C</sub> )	H	L	H	L	H	H
Write bytes (C, A, DQP <sub>C</sub> , DQP <sub>A</sub> )	H	L	H	L	H	L
Write bytes (C, B, DQP <sub>C</sub> , DQP <sub>B</sub> )	H	L	H	L	L	H
Write bytes (C, B, A, DQP <sub>C</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	H	L	L	L
Write byte (D, DQP <sub>D</sub> )	H	L	L	H	H	H
Write bytes (D, A, DQP <sub>D</sub> , DQP <sub>A</sub> )	H	L	L	H	H	L
Write bytes (D, B, DQP <sub>D</sub> , DQP <sub>B</sub> )	H	L	L	H	L	H
Write bytes (D, B, A, DQP <sub>D</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	L	H	L	L
Write bytes (D, B, DQP <sub>D</sub> , DQP <sub>B</sub> )	H	L	L	L	H	H
Write bytes (D, B, A, DQP <sub>D</sub> , DQP <sub>C</sub> , DQP <sub>A</sub> )	H	L	L	L	H	L
Write bytes (D, C, A, DQP <sub>D</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	L	L	L	H
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

### Notes

6. X = "Don't Care." H = Logic HIGH, L = Logic LOW.

7. Table only lists a partial listing of the byte write combinations. Any Combination of  $\overline{BW}_X$  is valid Appropriate write will be done based on which byte write is active.

### Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

- Storage temperature ..... -65 °C to + 150 °C
- Ambient temperature with power applied ..... -55 °C to + 125 °C
- Supply voltage on V<sub>DD</sub> relative to GND ..... -0.5 V to + 4.6 V
- Supply voltage on V<sub>DDQ</sub> relative to GND ..... -0.5 V to + V<sub>DD</sub>
- DC voltage applied to outputs in tri-state ..... -0.5 V to V<sub>DDQ</sub> + 0.5 V
- DC input voltage ..... -0.5 V to V<sub>DD</sub> + 0.5 V
- Current into outputs (LOW) ..... 20 mA
- Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2001 V
- Latch-up current ..... > 200 mA

### Operating Range

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Industrial	-40 °C to +85 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V <sub>DD</sub>

### Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single-bit upsets	25 °C	0	0.01	FIT/Mb
LMBU	Logical multi-bit upsets	25 °C	0	0.01	FIT/Mb
SEL	Single event latch up	85 °C	0	0.1	FIT/Dev

\* No LMBU or SEL events occurred during testing; this column represents a statistical  $\chi^2$ , 95% confidence limit calculation. For more details refer to Application Note AN54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

### Electrical Characteristics

Over the Operating Range

Parameter [8, 9]	Description	Test Conditions	Min	Max	Unit
V <sub>DD</sub>	Power supply voltage		3.135	3.6	V
V <sub>DDQ</sub>	I/O supply voltage	for 3.3 V I/O	3.135	V <sub>DD</sub>	V
		for 2.5 V I/O	2.375	2.625	V
V <sub>OH</sub>	Output HIGH voltage	for 3.3 V I/O, I <sub>OH</sub> = -4.0 mA	2.4	-	V
		for 2.5 V I/O, I <sub>OH</sub> = -1.0 mA	2.0	-	V
V <sub>OL</sub>	Output LOW voltage	for 3.3 V I/O, I <sub>OL</sub> = 8.0 mA	-	0.4	V
		for 2.5 V I/O, I <sub>OL</sub> = 1.0 mA	-	0.4	V
V <sub>IH</sub>	Input HIGH voltage <sup>[8]</sup>	for 3.3 V I/O	2.0	V <sub>DD</sub> + 0.3 V	V
		for 2.5 V I/O	1.7	V <sub>DD</sub> + 0.3 V	V
V <sub>IL</sub>	Input LOW voltage <sup>[8]</sup>	for 3.3 V I/O	-0.3	0.8	V
		for 2.5 V I/O	-0.3	0.7	V
I <sub>X</sub>	Input leakage current except ZZ and MODE	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	μA
	Input current of MODE	Input = V <sub>SS</sub>	-30	-	μA
		Input = V <sub>DD</sub>	-	5	μA
	Input current of ZZ	Input = V <sub>SS</sub>	-5	-	μA
Input = V <sub>DD</sub>		-	30	μA	
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub> , output disabled	-5	5	μA

**Notes**

- 8. Overshoot: V<sub>IH(AC)</sub> < V<sub>DD</sub> + 1.5 V (Pulse width less than t<sub>CYC/2</sub>), undershoot: V<sub>IL(AC)</sub> > -2 V (Pulse width less than t<sub>CYC/2</sub>).
- 9. T<sub>Power-up</sub>: Assumes a linear ramp from 0 V to V<sub>DD(min)</sub> within 200 ms. During this time V<sub>IH</sub> < V<sub>DD</sub> and V<sub>DDQ</sub> ≤ V<sub>DD</sub>.

**Electrical Characteristics** (continued)

Over the Operating Range

Parameter [8, 9]	Description	Test Conditions	Min	Max	Unit
$I_{DD}$	$V_{DD}$ operating supply current	$V_{DD} = \text{Max}$ , $I_{OUT} = 0 \text{ mA}$ , $f = f_{MAX} = 1/t_{CYC}$	–	149	mA
$I_{SB1}$	Automatic CE power-down current – TTL inputs	Max $V_{DD}$ , device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$ , inputs switching	–	80	mA
$I_{SB2}$	Automatic CE power-down current – CMOS inputs	Max $V_{DD}$ , device deselected, $V_{IN} \geq V_{DD} - 0.3 \text{ V}$ or $V_{IN} \leq 0.3 \text{ V}$ , $f = 0$ , inputs static	–	70	mA
$I_{SB3}$	Automatic CE power-down current – CMOS inputs	Max $V_{DD}$ , device deselected, $V_{IN} \geq V_{DDQ} - 0.3 \text{ V}$ or $V_{IN} \leq 0.3 \text{ V}$ , $f = f_{MAX}$ , inputs switching	–	80	mA
$I_{SB4}$	Automatic CE power-down current – TTL inputs	Max $V_{DD}$ , device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = 0$ , inputs static	–	70	mA

**Capacitance**

Parameter [10]	Description	Test Conditions	100-pin TQFP Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25 \text{ }^\circ\text{C}$ , $f = 1 \text{ MHz}$ , $V_{DD} = 3.3 \text{ V}$ , $V_{DDQ} = 2.5 \text{ V}$	5	pF
$C_{CLK}$	Clock input capacitance		5	pF
$C_{I/O}$	Input/output capacitance		5	pF

**Thermal Resistance**

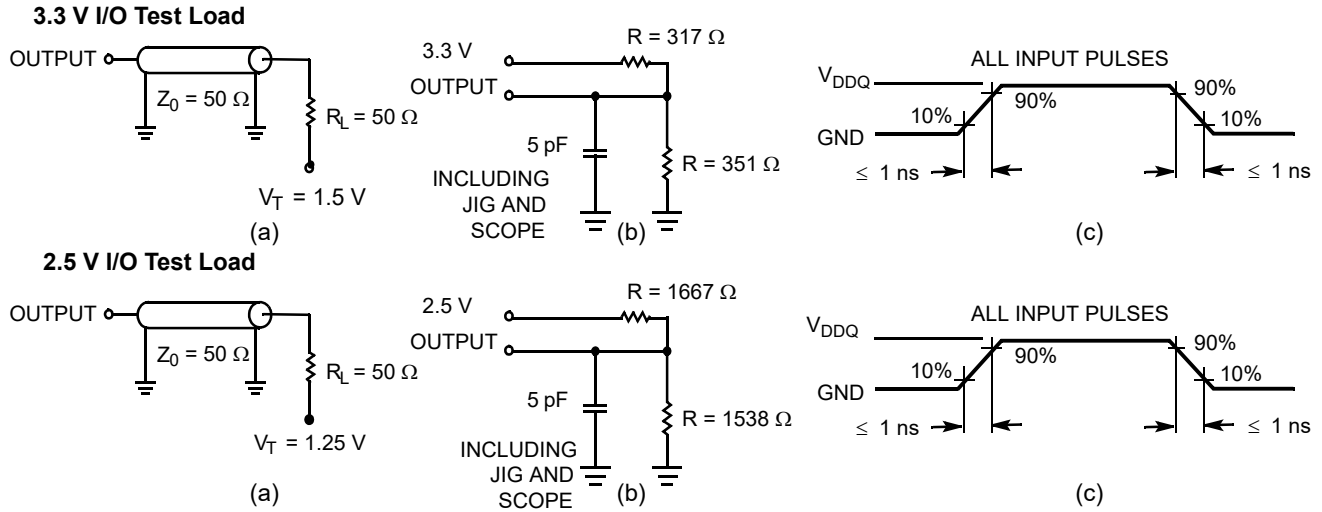
Parameter [10]	Description	Test Conditions	100-pin TQFP Package	Unit	
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51	With Still Air (0 m/s)	37.95	$^\circ\text{C/W}$
			With Still Air (1 m/s)	33.19	$^\circ\text{C/W}$
			With Still Air (3 m/s)	30.44	$^\circ\text{C/W}$
$\Theta_{JB}$	Thermal resistance (junction to board)	–	24.07	$^\circ\text{C/W}$	
$\Theta_{JC}$	Thermal resistance (junction to case)	–	8.36	$^\circ\text{C/W}$	

**Note**

10. Tested initially and after any design or process change that may affect these parameters.

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



## Switching Characteristics

Over the Operating Range

Parameter <sup>[11, 12]</sup>	Description	-133		Unit
		Min	Max	
t <sub>POWER</sub>	V <sub>DD</sub> (typical) to the first access <sup>[13]</sup>	1	–	ms
<b>Clock</b>				
t <sub>CYC</sub>	Clock cycle time	7.5	–	ns
t <sub>CH</sub>	Clock HIGH	2.1	–	ns
t <sub>CL</sub>	Clock LOW	2.1	–	ns
<b>Output Times</b>				
t <sub>CDV</sub>	Data output valid after CLK rise	–	6.5	ns
t <sub>DOH</sub>	Data output hold after CLK rise	2.0	–	ns
t <sub>CLZ</sub>	Clock to low Z <sup>[14, 15, 16]</sup>	2.0	–	ns
t <sub>CHZ</sub>	Clock to high Z <sup>[14, 15, 16]</sup>	–	4.0	ns
t <sub>OEV</sub>	$\overline{\text{OE}}$ LOW to output valid	–	3.2	ns
t <sub>OELZ</sub>	$\overline{\text{OE}}$ LOW to output low Z <sup>[14, 15, 16]</sup>	0	–	ns
t <sub>OEZH</sub>	$\overline{\text{OE}}$ HIGH to output high Z <sup>[14, 15, 16]</sup>	–	4.0	ns
<b>Set-up Times</b>				
t <sub>AS</sub>	Address setup before CLK rise	1.5	–	ns
t <sub>ADS</sub>	ADSP, ADSC setup before CLK rise	1.5	–	ns
t <sub>ADVS</sub>	$\overline{\text{ADV}}$ setup before CLK rise	1.5	–	ns
t <sub>WES</sub>	$\overline{\text{GW}}$ , $\overline{\text{BWE}}$ , $\overline{\text{BW}}_{[\text{A:D}]}$ setup before CLK rise	1.5	–	ns
t <sub>DS</sub>	Data input setup before CLK rise	1.5	–	ns
t <sub>CES</sub>	Chip enable setup	1.5	–	ns
<b>Hold Times</b>				
t <sub>AH</sub>	Address hold after CLK rise	0.5	–	ns
t <sub>ADH</sub>	ADSP, ADSC hold after CLK rise	0.5	–	ns
t <sub>WEH</sub>	$\overline{\text{GW}}$ , $\overline{\text{BWE}}$ , $\overline{\text{BW}}_{[\text{A:D}]}$ hold after CLK rise	0.5	–	ns
t <sub>ADVH</sub>	$\overline{\text{ADV}}$ hold after CLK rise	0.5	–	ns
t <sub>DH</sub>	Data input hold after CLK rise	0.5	–	ns
t <sub>CEH</sub>	Chip enable hold after CLK rise	0.5	–	ns

### Notes

11. Timing reference level is 1.5 V when V<sub>DDQ</sub> = 3.3 V and is 1.25 V when V<sub>DDQ</sub> = 2.5 V.

12. Test conditions shown in (a) of [Figure 2 on page 12](#) unless otherwise noted.

13. This part has a voltage regulator internally; t<sub>POWER</sub> is the time that the power needs to be supplied above V<sub>DD(minimum)</sub> initially, before a read or write operation can be initiated.

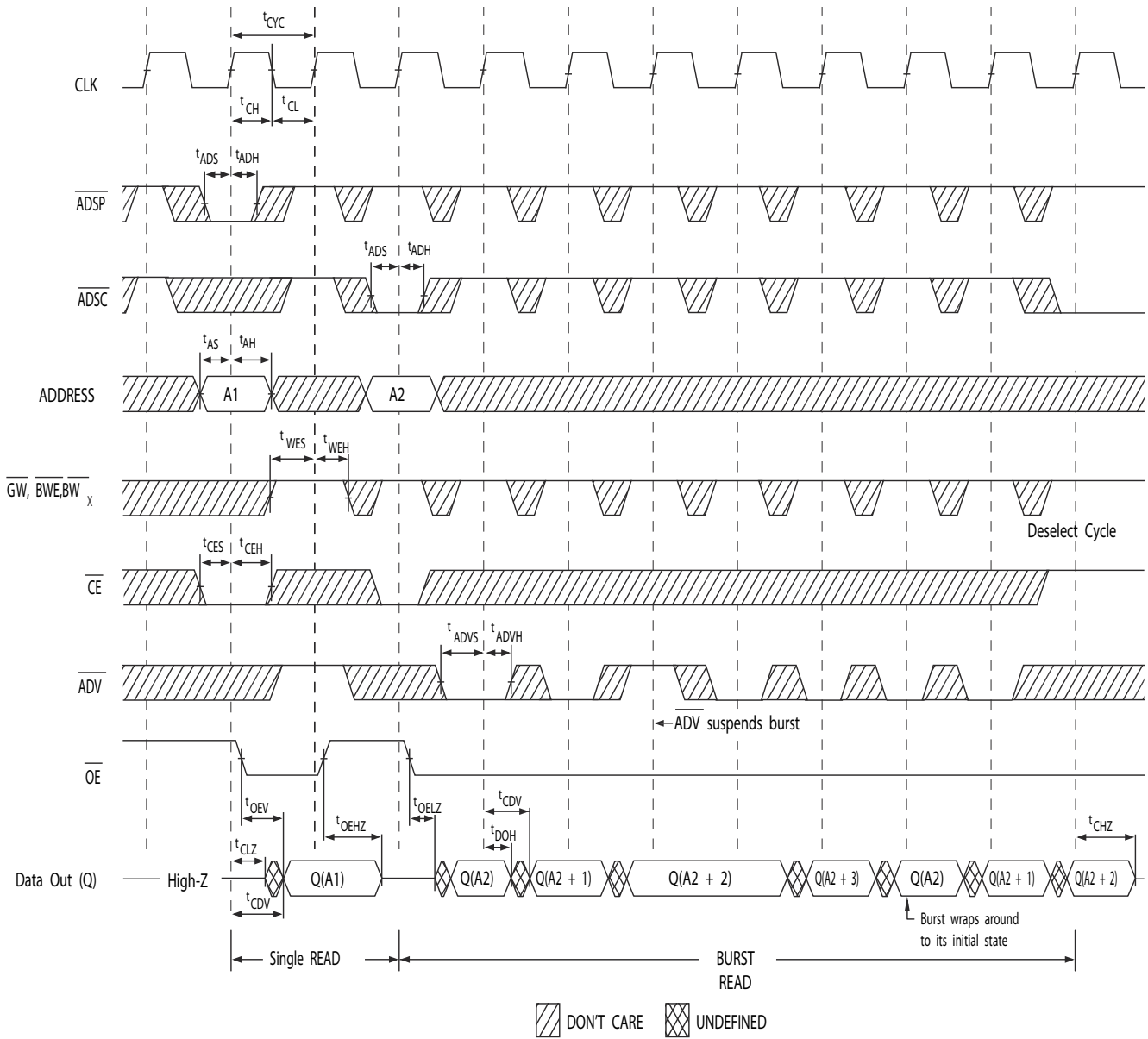
14. t<sub>CHZ</sub>, t<sub>CLZ</sub>, t<sub>OELZ</sub>, and t<sub>OEZH</sub> are specified with AC test conditions shown in part (b) of [Figure 2 on page 12](#). Transition is measured ± 200 mV from steady-state voltage.

15. At any given voltage and temperature, t<sub>OEZH</sub> is less than t<sub>OELZ</sub> and t<sub>CHZ</sub> is less than t<sub>CLZ</sub> to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.

16. This parameter is sampled and not 100% tested.

Timing Diagrams

Figure 3. Read Cycle Timing [17]

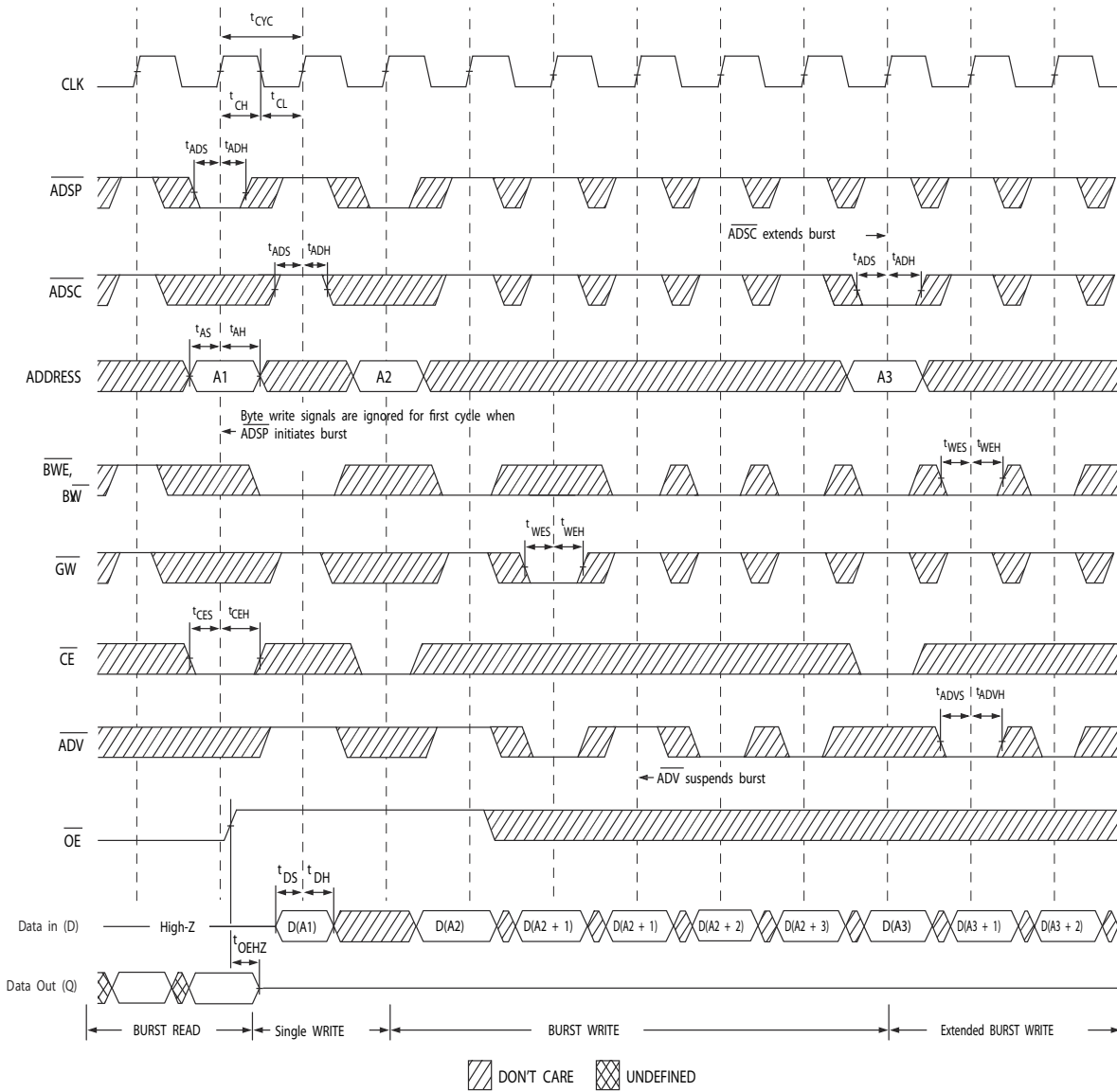


Note

17. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $\overline{CE}_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW or  $\overline{CE}_3$  is HIGH.

Timing Diagrams (continued)

Figure 4. Write Cycle Timing [18, 19]

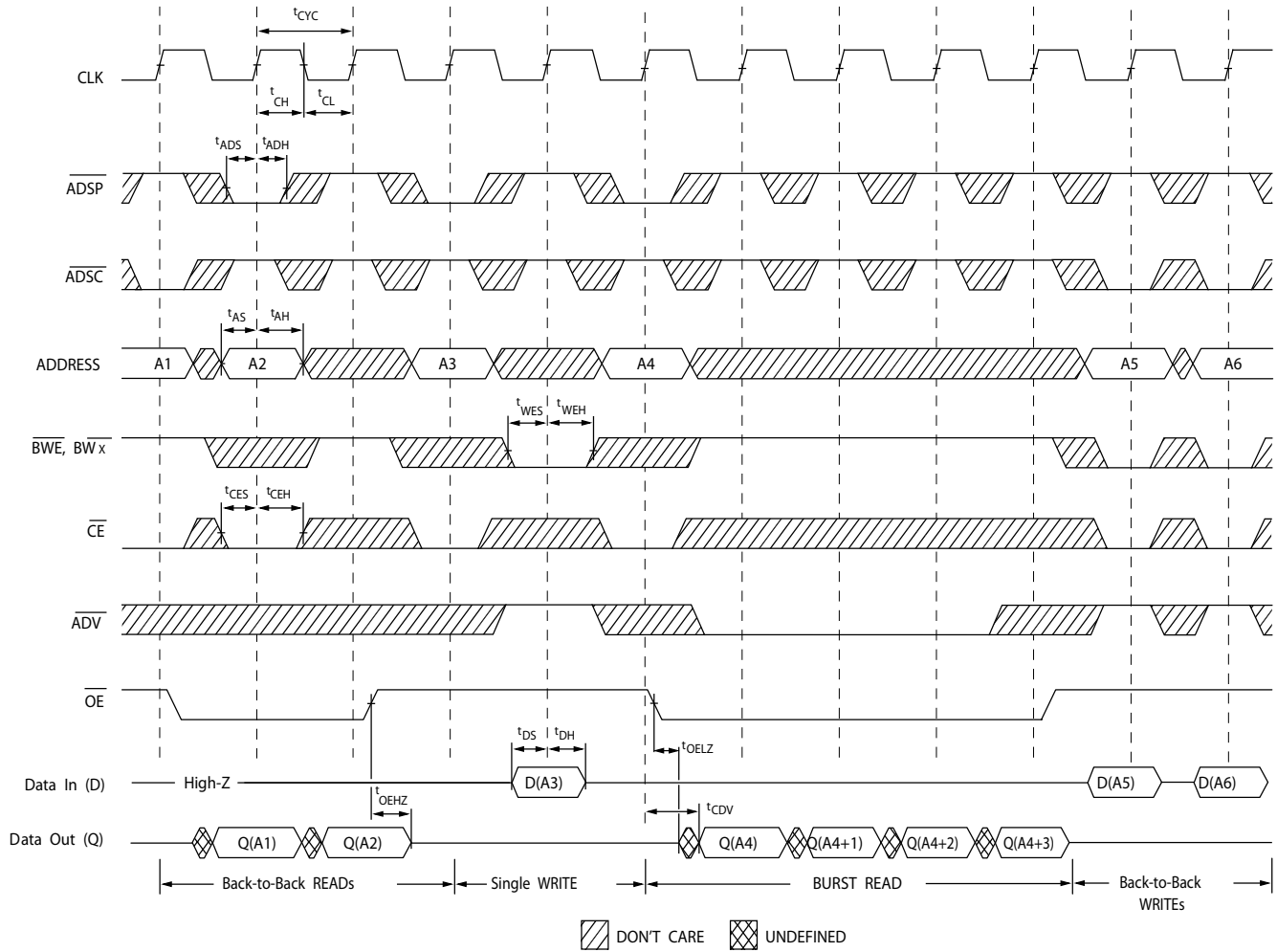


Notes

- 18. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.
- 19. Full width write can be initiated by either GW LOW; or by GW HIGH, BWE LOW and  $BW_x$  LOW.

Timing Diagrams (continued)

Figure 5. Read/Write Cycle Timing [20, 21, 22]



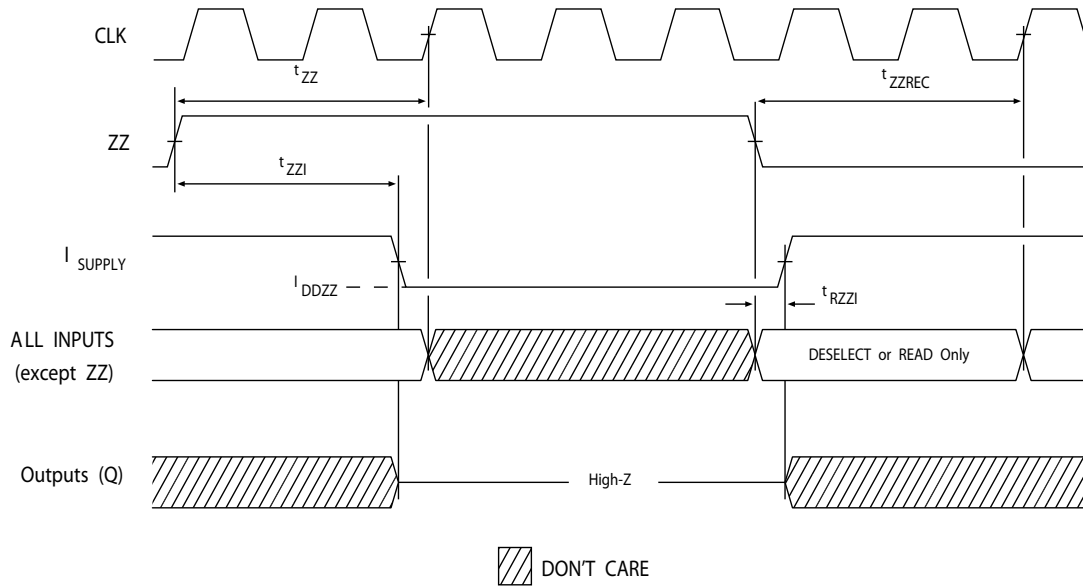
Notes

- 20. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.
- 21. The data bus (Q) remains in high Z following a WRITE cycle, unless a new read access is initiated by ADSP or ADSC.
- 22.  $\overline{W}$  is HIGH.



**Timing Diagrams** (continued)

**Figure 6. ZZ Mode Timing** [23, 24]



**Notes**

- 23. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
- 24. DQs are in high Z when exiting ZZ sleep mode.

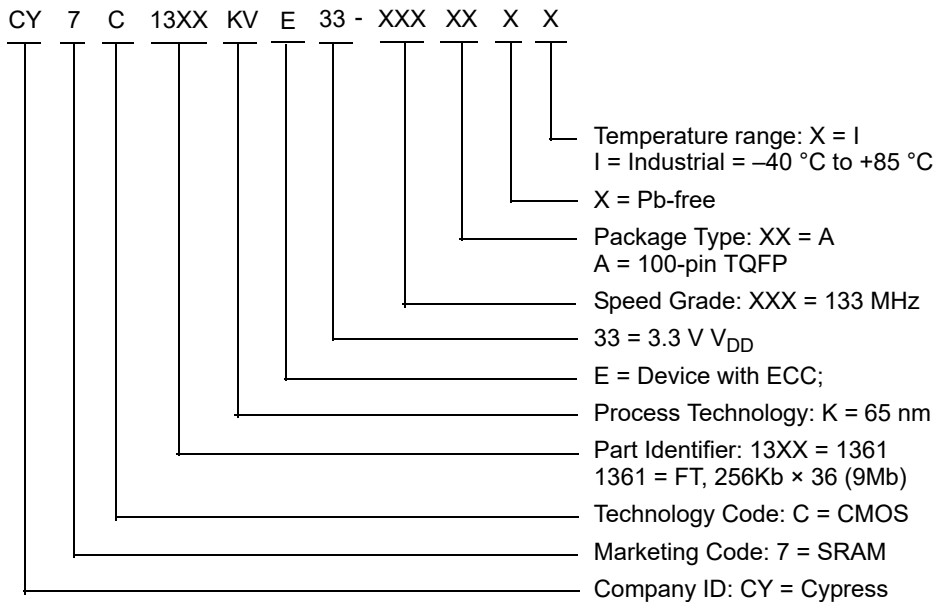
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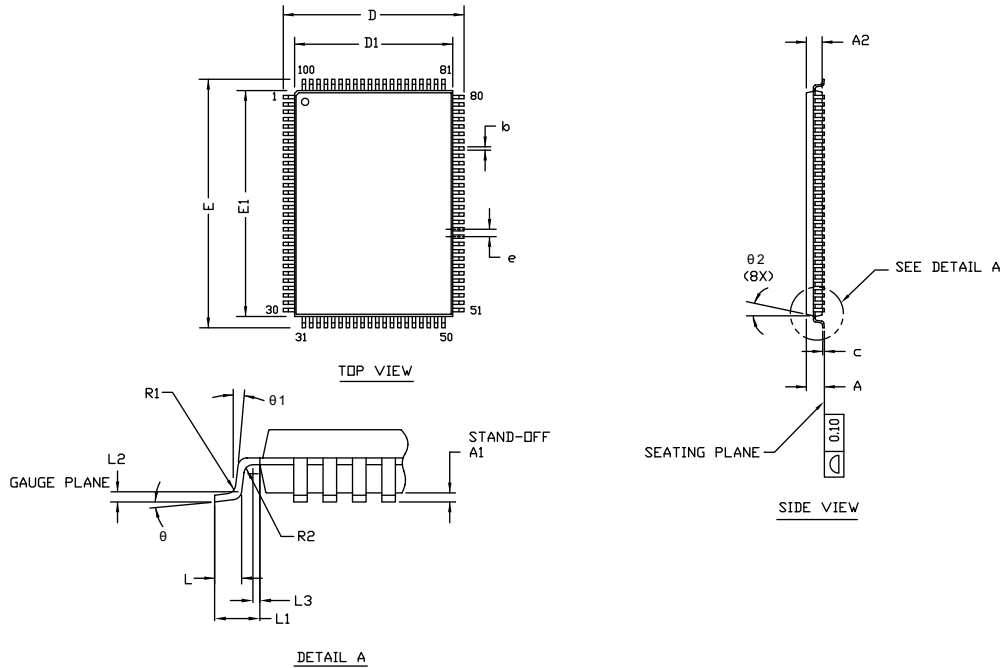
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1361KVE33-133AXI	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Industrial

## Ordering Code Definitions



## Package Diagrams

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
R1	0.08	—	0.20
R2	0.08	—	0.20
θ	0°	—	7°
θ1	0°	—	—
θ2	11°	12°	13°
c	—	—	0.20
b	0.22	0.30	0.38
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
L3	0.20	—	—
e	0.65 TYP		

NOTE:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE. BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
- JEDEC SPECIFICATION NO. REF: MS-026.

51-85050 \*G

## Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
EIA	Electronic Industries Alliance
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
LMBU	Logical Multi-Bit Upsets
LSB	Least Significant Bit
LSBU	Logical Single-Bit Upsets
MSB	Most Significant Bit
$\overline{OE}$	Output Enable
PBGA	Plastic Ball Grid Array
SEL	Single Event Latch up
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1361KVE33, 9-Mbit (256K × 36) Flow-Through SRAM				
Document Number: 002-12709				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	5413843	PRIT	08/24/2016	New data sheet.
*A	6013469	RMES	01/04/2018	Updated <a href="#">Package Diagrams</a> : spec 51-85050 – Changed revision from *E to *G. Updated to new template.

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**Телефон:** 8 (812) 309 58 32 (многоканальный)

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**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.