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RoHS

RF LDMOS Wideband Integrated Power Amplifiers

A2I20H080NR1
A2I20H080GNR1

1800–2200 MHz, 13.5 W AVG., 30 V AIRFAST RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS

The A2I20H080N wideband integrated circuit is an asymmetrical Doherty designed with on–chip matching that makes it usable from 1800 to 2200 MHz. This multi–stage structure is rated for 26 to 32 V operation and covers all typical cellular base station modulation formats.

1800 MHz

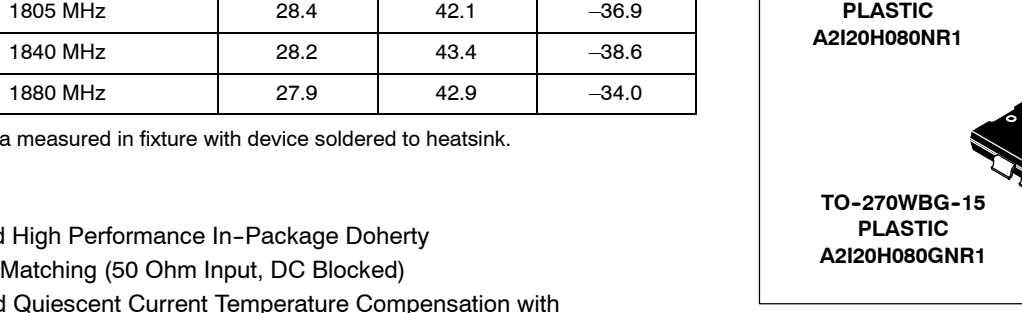
- Typical Doherty Single–Carrier W–CDMA Characterization Performance: V_{DD} = 30 Vdc, I_{DQ1A} = 30 mA, I_{DQ2A} = 195 mA, V_{GS1B} = 1.35 Vdc, V_{GS2B} = 1.25 Vdc, P_{out} = 13.5 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.(1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
1805 MHz	28.4	42.1	–36.9
1840 MHz	28.2	43.4	–38.6
1880 MHz	27.9	42.9	–34.0

1. All data measured in fixture with device soldered to heatsink.

Features

- Advanced High Performance In–Package Doherty
- On–Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (2)
- Designed for Digital Predistortion Error Correction Systems



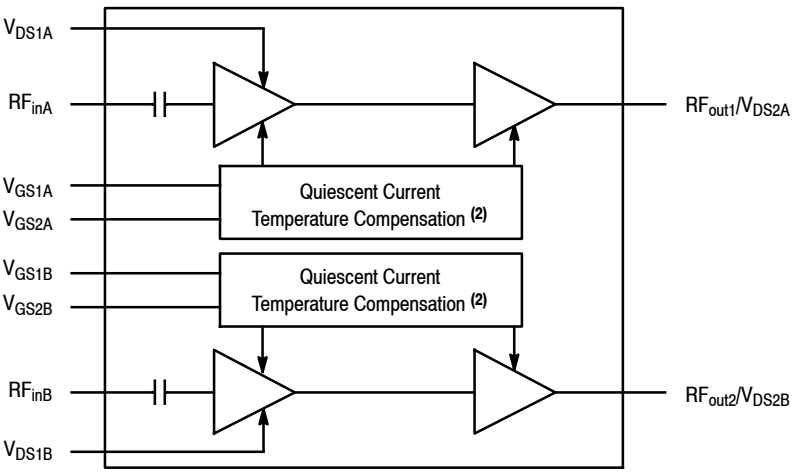
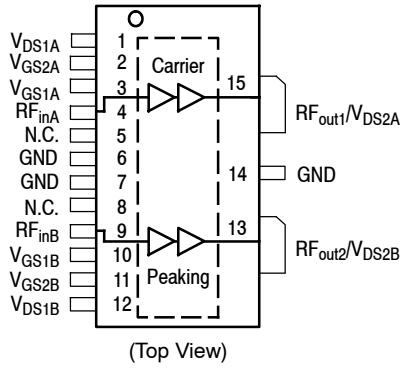


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 2. Pin Connections

2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
Input Power	P_{in}	21	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 76°C, 13.5 W Avg., W-CDMA, 1840 MHz Stage 1, 30 Vdc, I_{DQ1A} = 30 mA, V_{GS1B} = 1.35 Vdc Stage 2, 30 Vdc, I_{DQ2A} = 195 mA, V_{GS2B} = 1.25 Vdc	$R_{\theta JC}$	 6.4 1.9	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Carrier Stage 1 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Carrier Stage 1 – On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 4 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 30 Vdc, I_{DQ1A} = 30 mA)	$V_{GS(Q)}$	—	2.2	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 30 Vdc, I_{DQ1A} = 30 mA, Measured in Functional Test)	$V_{GG(Q)}$	3.2	4.0	4.7	Vdc
Carrier Stage 2 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Carrier Stage 2 – On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 28 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 30 Vdc, I_{DQ2A} = 195 mA)	$V_{GS(Q)}$	—	2.2	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 30 Vdc, I_{DQ2A} = 195 mA, Measured in Functional Test)	$V_{GG(Q)}$	3.0	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 280 mAdc)	$V_{DS(on)}$	0.1	0.2	1.5	Vdc

1. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Peaking Stage 1 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Peaking Stage 1 – On Characteristics (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 9 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Peaking Stage 2 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Peaking Stage 2 – On Characteristics (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 44 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 440 mAdc)	$V_{DS(on)}$	0.1	0.2	1.5	Vdc

1. Each side of device measured separately.

(continued)

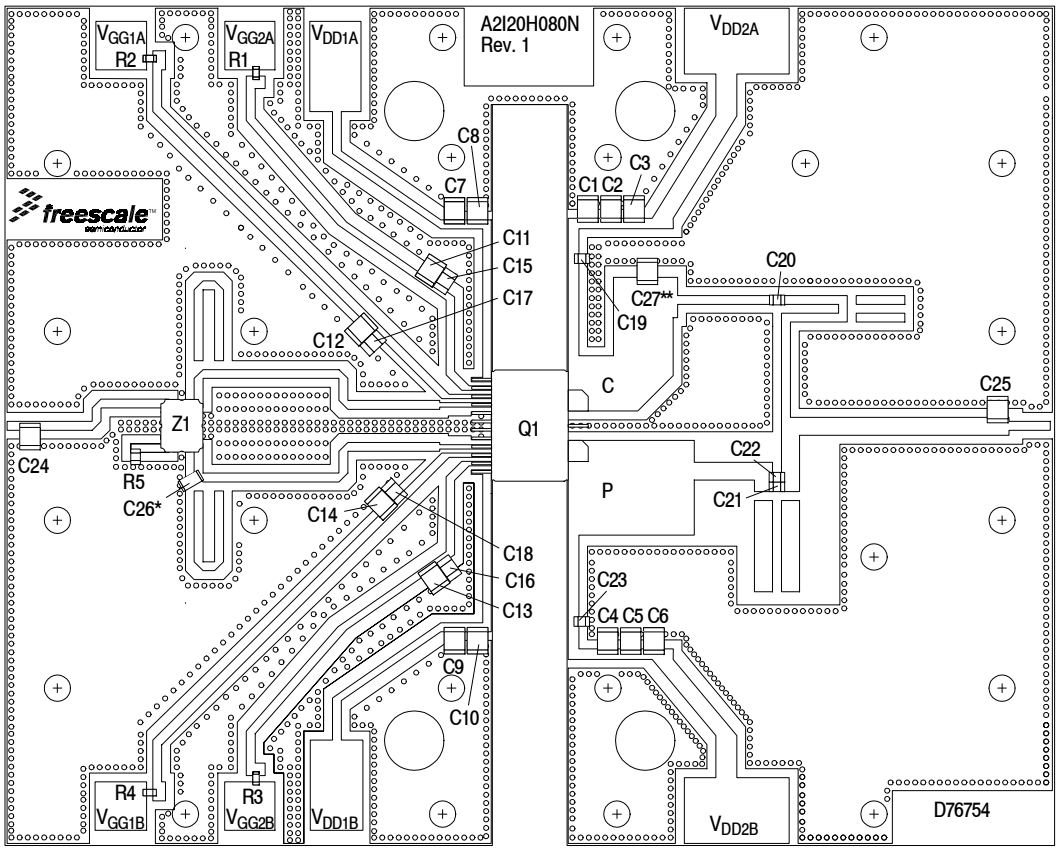
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2,3) (In Freescale Doherty Production Test Fixture, 50 ohm system) V_{DD} = 30 Vdc, I_{DQ1A} = 30 mA, I_{DQ2A} = 195 mA, V_{GS1B} = 1.35 Vdc, V_{GS2B} = 1.25 Vdc, P_{out} = 13.5 W Avg., f = 1880 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	26.5	27.8	30.0	dB
Power Added Efficiency	PAE	38.5	41.6	—	%
Adjacent Channel Power Ratio	ACPR	—	–31.6	–28.0	dBc
P_{out} @ 3 dB Compression Point, CW	P3dB	74.1	82.4	—	W
Load Mismatch (2,4) (In Freescale Doherty Characterization Fixture, 50 ohm system) I_{DQ1A} = 30 mA, I_{DQ2A} = 195 mA, V_{GS1B} = 1.35 Vdc, V_{GS2B} = 1.25 Vdc, f = 1840 MHz					
VSWR 10:1 at 32 Vdc, 89 W CW Output Power (3 dB Input Overdrive from 76 W CW Rated Power)	No Device Degradation				
Typical Performance (2,4) (In Freescale Doherty Characterization Fixture, 50 ohm system) V_{DD} = 30 Vdc, I_{DQ1A} = 30 mA, I_{DQ2A} = 195 mA, V_{GS1B} = 1.35 Vdc, V_{GS2B} = 1.25 Vdc, 1805–1880 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	70	—	W
P_{out} @ 3 dB Compression Point (5)	P3dB	—	90	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz frequency range.)	Φ	—	–22	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	160	—	MHz
Quiescent Current Accuracy over Temperature (6) with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 1 with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 2	ΔI_{QT}	 — —	 1.0 2.0	 — —	%
Gain Flatness in 75 MHz Bandwidth @ P_{out} = 13.5 W Avg.	G_F	—	0.5	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.018	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.01	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2I20H080NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-inch Reel	TO-270WB-15
A2I20H080GNR1		TO-270WBG-15

1. Part internally input matched.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
4. All data measured in fixture with device soldered to heatsink.
5. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
6. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.nxp.com/RF and search for AN1977 or AN1987.



Note: All data measured in fixture with device soldered to heatsink. Production fixture does not include device soldered to heatsink.

*C26 is mounted vertically.

**C27 on characterization board only.

Figure 3. A2I20H080NR1 Test Circuit Component Layout

Table 7. A2I20H080NR1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14	10 μF Chip Capacitors	GRM32ER61H106KA12L	Murata
C15, C16, C17, C18	10 nF Chip Capacitors	C0805C103J5RACTU	Kemet
C19, C20, C21, C22, C23	10 pF Chip Capacitors	ATC600S100JT250XT	ATC
C24, C26	0.4 pF Chip Capacitors	ATC100B0R4BT500XT	ATC
C25, C27*	0.1 pF Chip Capacitors	ATC100B0R1BT500XT	ATC
Q1	RF LDMOS Power Amplifier	A2I20H080NR1	Freescale
R1, R2, R3, R4	2.2 kΩ, 1/8 W Chip Resistors	CRCW08052K20JNEA	Vishay
R5	50 Ω, 8 W Chip Resistor	C8A50Z4A	Anaren
Z1	1700–2000 MHz Band, 5 dB Directional Coupler	X3C19P1-05S	Anaren
PCB	RF35, 0.020″, ε_r = 3.55	D76754	MTL

*C27 on characterization board only.

TYPICAL CHARACTERISTICS — 1805–1880 MHz

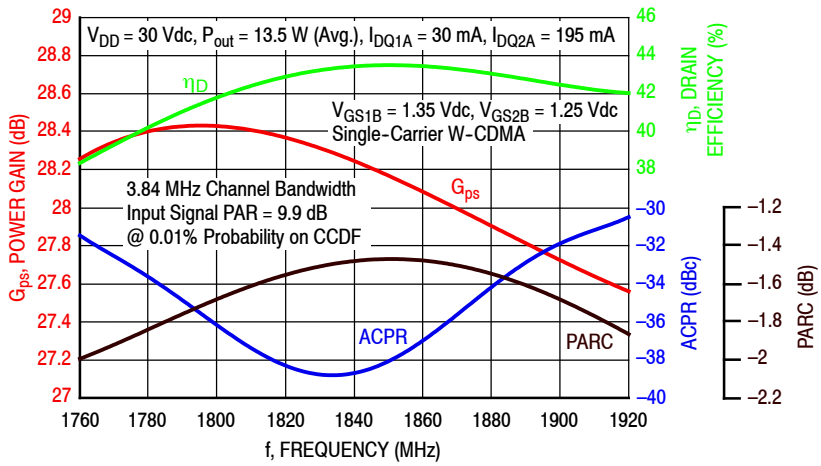


Figure 4. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 13.5 Watts Avg.

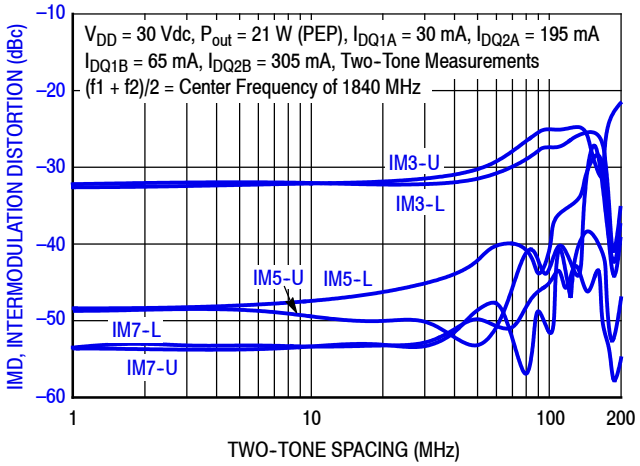


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

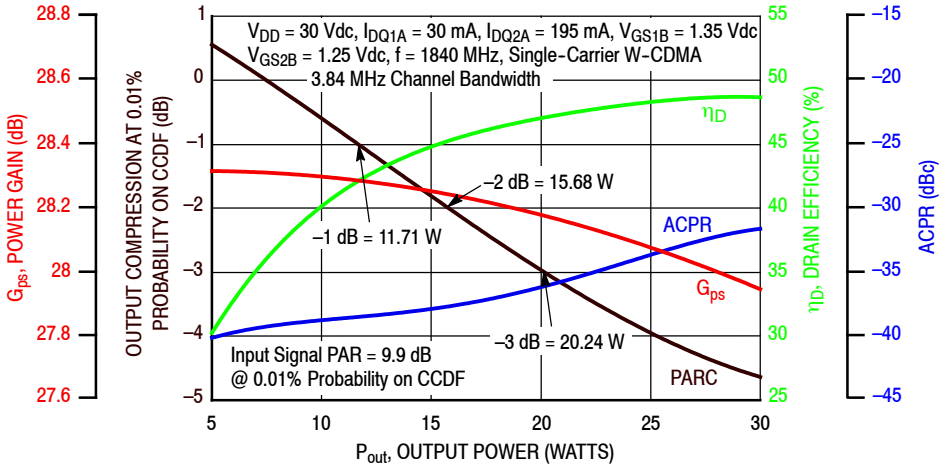


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 1805–1880 MHz

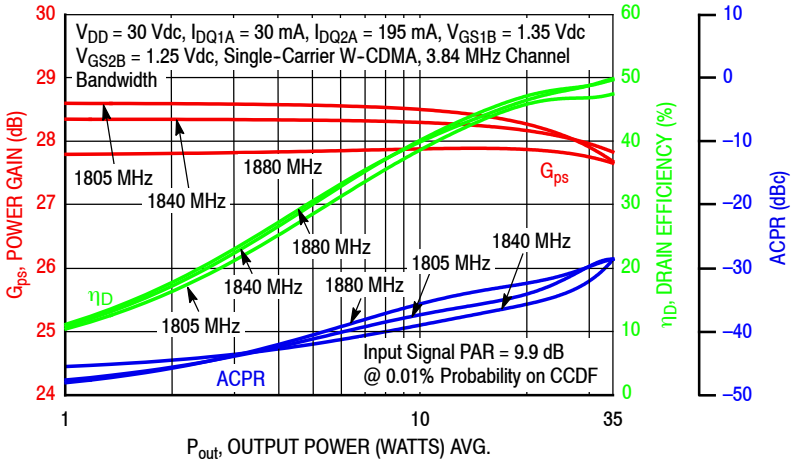


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

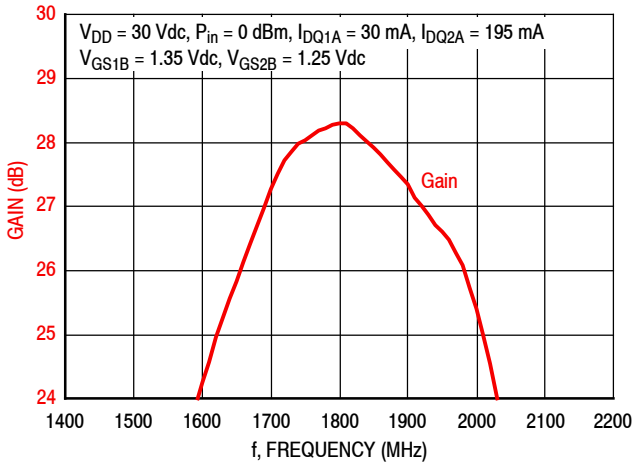


Figure 8. Broadband Frequency Response

Table 8. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 30 Vdc, I_{DQ1A} = 30 mA, I_{DQ2A} = 205 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	33.8 – j12.2	31.2 + j8.75	4.15 + j0.65	32.2	44.5	28	58.1	–8
1840	34.9 – j13.8	34.8 + j13.3	4.00 + j0.80	32.2	44.5	28	57.6	–8
1880	40.8 – j9.23	39.0 + j17.1	3.87 + j0.86	31.9	44.6	29	58.1	–8

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	33.8 – j12.2	34.3 + j8.61	4.49 + j0.38	30.0	45.3	34	59.2	–12
1840	34.9 – j13.8	38.1 + j12.5	4.24 + j0.62	30.1	45.3	34	59.0	–12
1880	40.8 – j9.23	42.6 + j15.0	4.19 + j0.63	29.7	45.3	34	58.8	–11

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 9. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 30 Vdc, I_{DQ1A} = 30 mA, I_{DQ2A} = 205 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	33.8 – j12.2	29.5 + j12.7	3.09 + j3.00	33.7	43.1	20	67.0	–10
1840	34.9 – j13.8	33.3 + j19.2	2.52 + j3.11	33.8	42.7	19	67.4	–11
1880	40.8 – j9.23	38.8 + j22.4	2.68 + j2.78	33.1	43.3	22	67.7	–11

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	33.8 – j12.2	31.1 + j12.8	2.70 + j3.07	31.9	43.5	23	68.6	–16
1840	34.9 – j13.8	35.9 + j18.4	2.47 + j3.21	31.9	43.3	21	68.4	–16
1880	40.8 – j9.23	41.2 + j22.0	2.32 + j3.02	31.3	43.5	22	68.4	–15

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

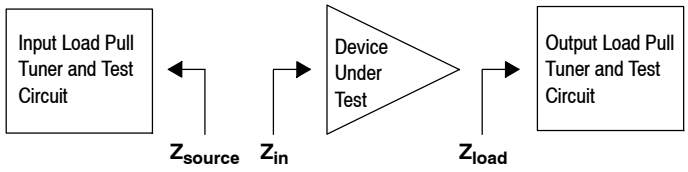


Table 10. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 30 Vdc, I_{DQ1B} = 60 mA, V_{GS2B} = 1.25 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	30.8 – j15.3	27.3 + j12.4	2.44 – j0.54	31.3	46.9	50	60.3	–18
1840	35.4 – j16.8	29.6 + j15.5	2.49 – j0.51	31.3	46.9	49	59.3	–18
1880	38.3 – j17.1	32.5 + j17.8	2.42 – j0.57	31.0	46.9	49	58.7	–17

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	30.8 – j15.3	30.5 + j14.0	2.67 – j0.73	29.1	47.6	58	60.8	–23
1840	35.4 – j16.8	33.3 + j16.6	2.65 – j0.67	29.2	47.5	56	59.8	–23
1880	38.3 – j17.1	36.8 + j18.2	2.67 – j0.72	28.8	47.5	57	59.6	–22

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

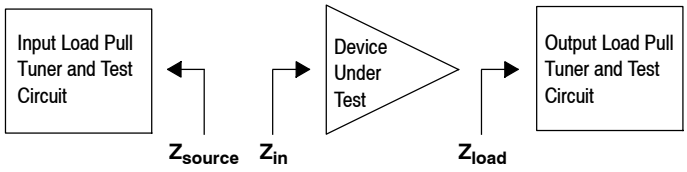
Table 11. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 30 Vdc, I_{DQ1B} = 60 mA, V_{GS2B} = 1.25 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	30.8 – j15.3	22.7 + j17.8	1.34 + j1.73	32.7	43.8	24	73.5	–36
1840	35.4 – j16.8	25.4 + j22.1	1.26 + j1.66	32.5	43.7	23	72.0	–35
1880	38.3 – j17.1	30.5 + j23.6	1.61 + j1.37	32.1	44.8	30	71.2	–28

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	30.8 – j15.3	26.4 + j16.9	1.70 + j1.31	30.8	45.6	36	73.3	–36
1840	35.4 – j16.8	29.7 + j20.8	1.65 + j1.40	30.5	45.3	34	71.5	–36
1880	38.3 – j17.1	33.4 + j23.0	1.61 + j1.20	30.2	45.6	36	71.0	–34

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1840 MHz

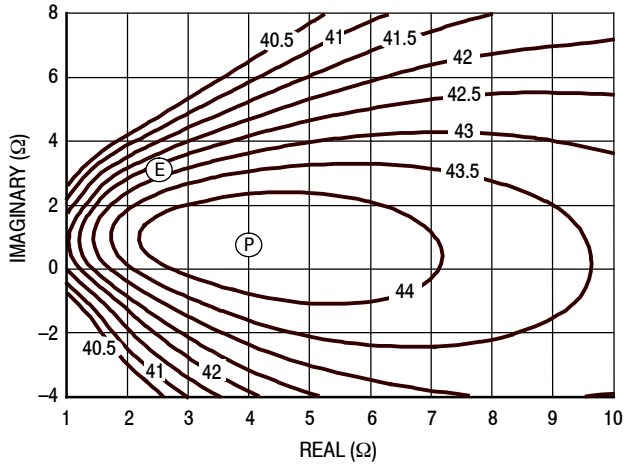


Figure 9. P1dB Load Pull Output Power Contours (dBm)

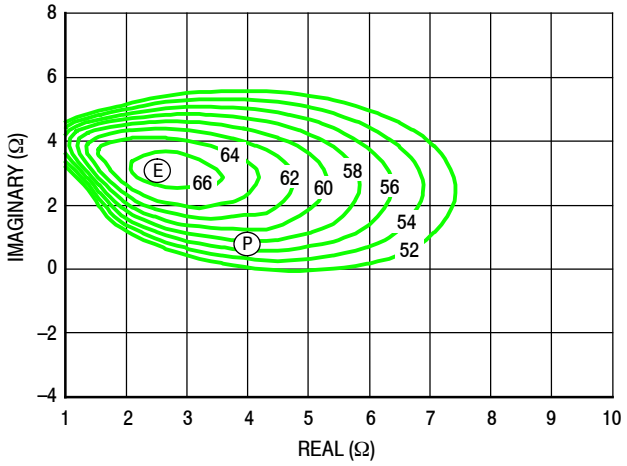


Figure 10. P1dB Load Pull Efficiency Contours (%)

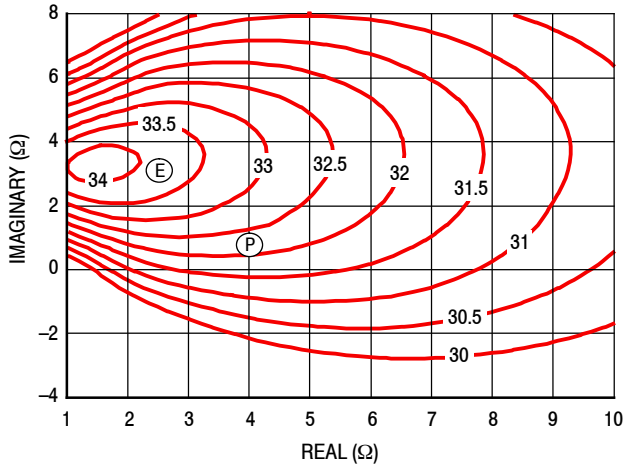


Figure 11. P1dB Load Pull Gain Contours (dB)

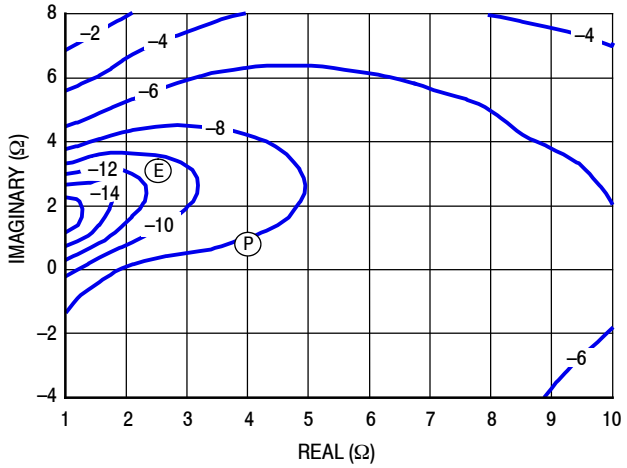


Figure 12. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1840 MHz

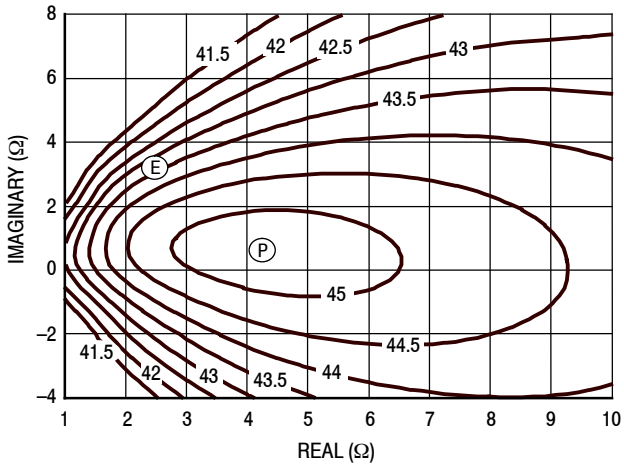


Figure 13. P3dB Load Pull Output Power Contours (dBm)

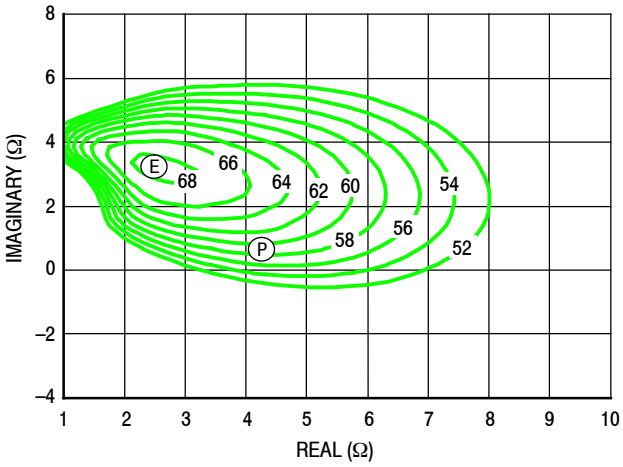


Figure 14. P3dB Load Pull Efficiency Contours (%)

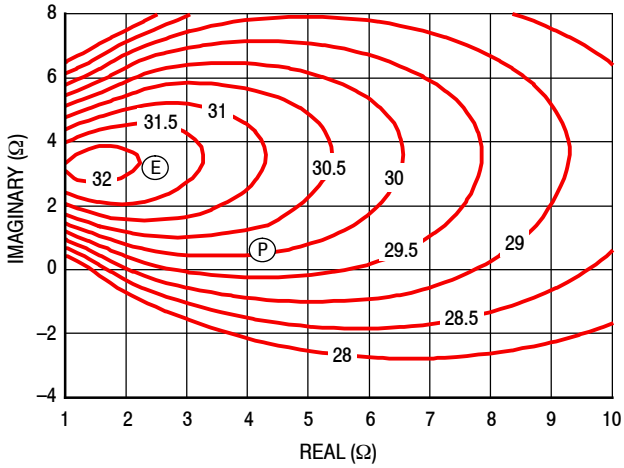


Figure 15. P3dB Load Pull Gain Contours (dB)

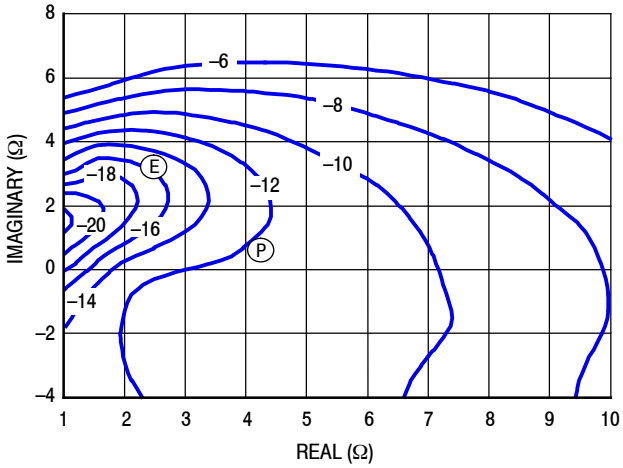


Figure 16. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1840 MHz

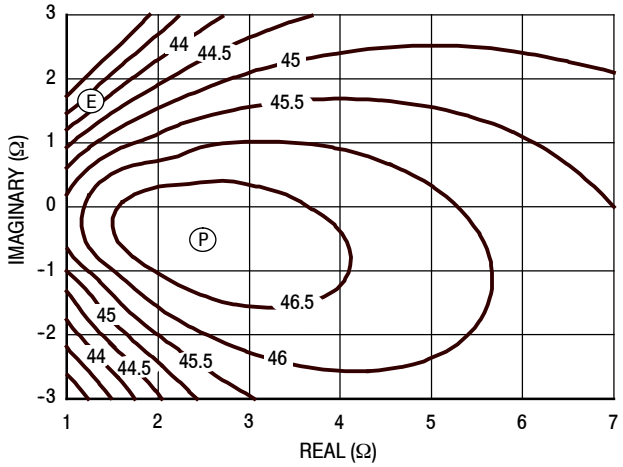


Figure 17. P1dB Load Pull Output Power Contours (dBm)

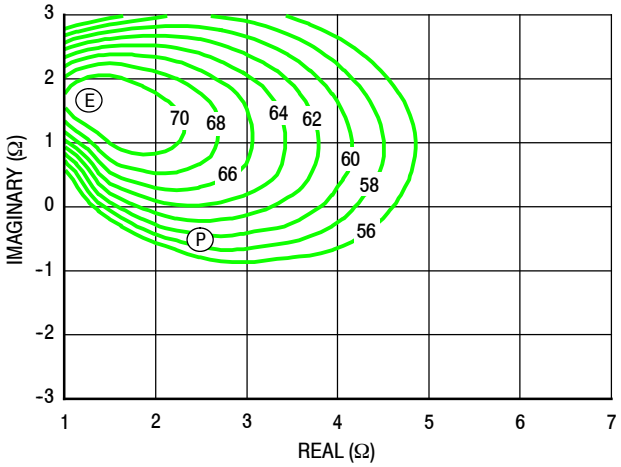


Figure 18. P1dB Load Pull Efficiency Contours (%)

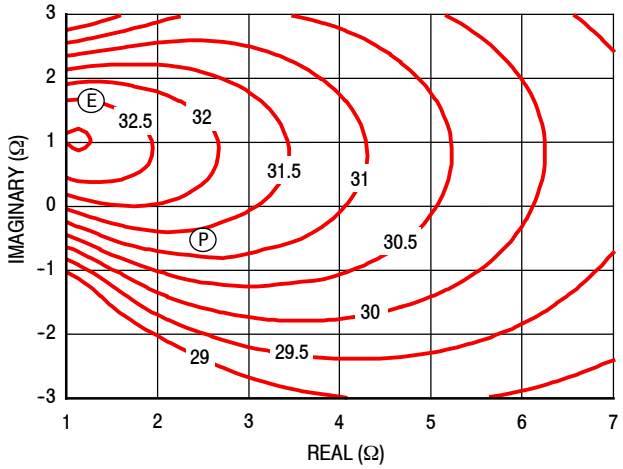


Figure 19. P1dB Load Pull Gain Contours (dB)

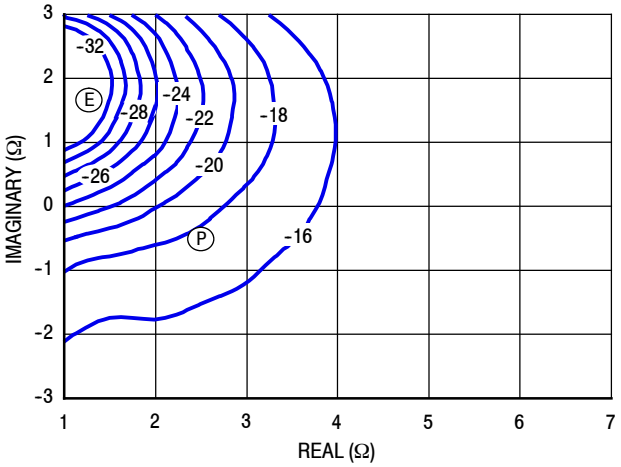


Figure 20. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1840 MHz

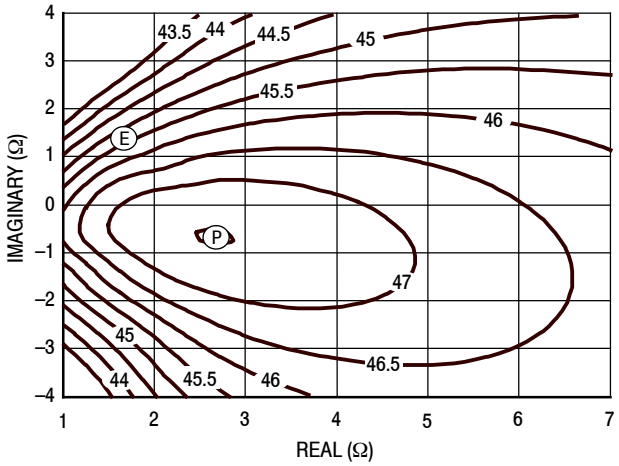


Figure 21. P3dB Load Pull Output Power Contours (dBm)

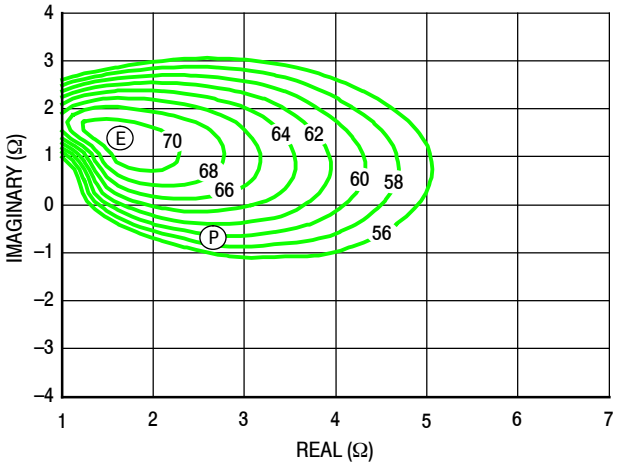


Figure 22. P3dB Load Pull Efficiency Contours (%)

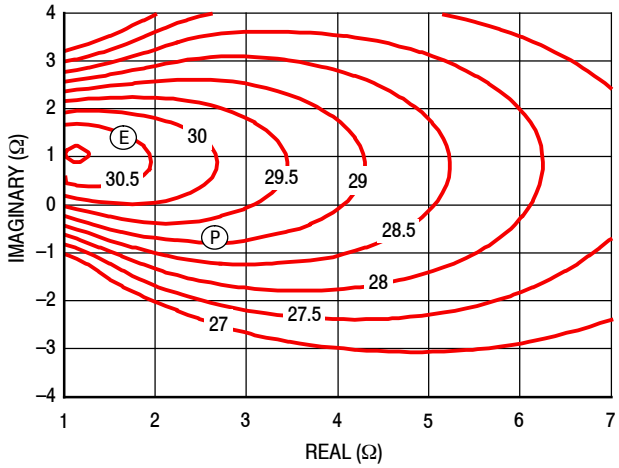


Figure 23. P3dB Load Pull Gain Contours (dB)

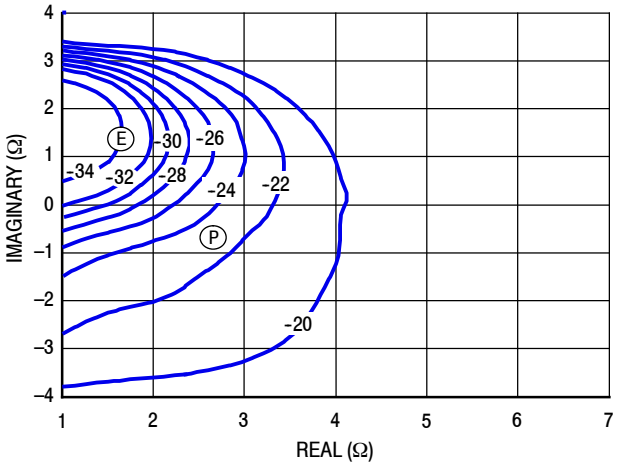


Figure 24. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

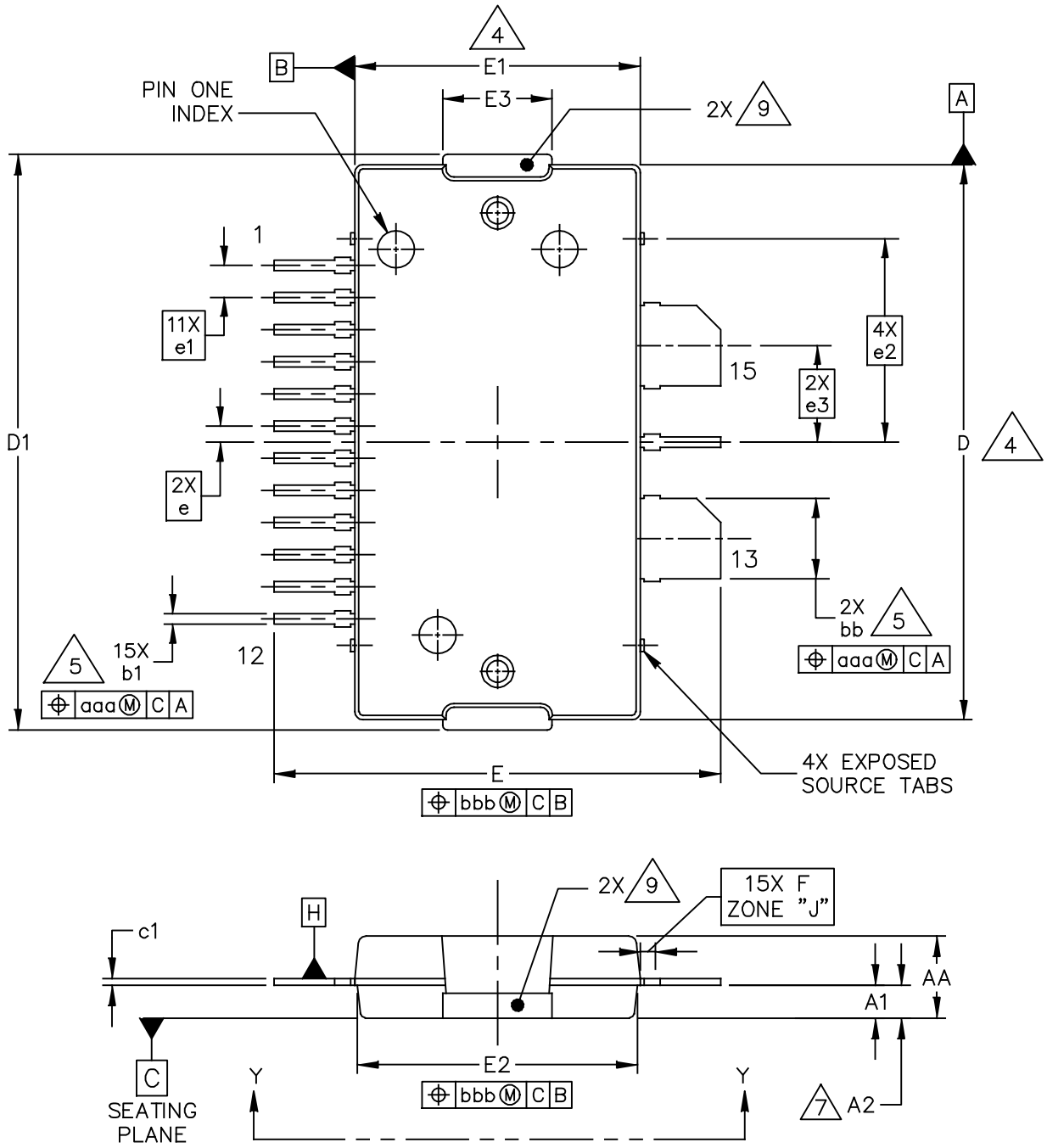
Gain

Drain Efficiency

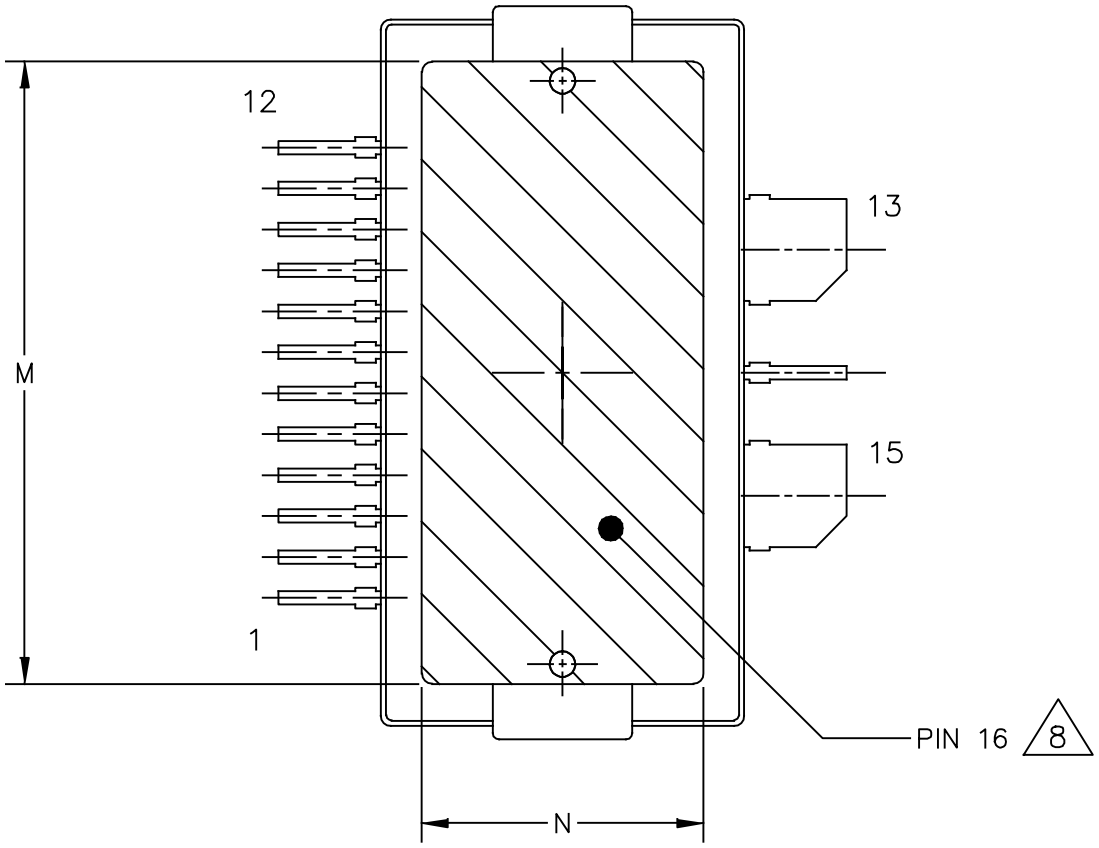
Linearity

Output Power

PACKAGE DIMENSIONS



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VIEW Y–Y

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	STANDARD: NON–JEDEC	
	17 JUN 2014	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	M	.600	----	15.24	----
A1	.039	.043	0.99	1.09	N	.270	----	6.86	----
A2	.040	.042	1.02	1.07	bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	c1	.007	.011	0.18	0.28
E	.551	.559	14.00	14.20	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	e3	.120 BSC		3.05 BSC	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
					bbb	.008		0.20	

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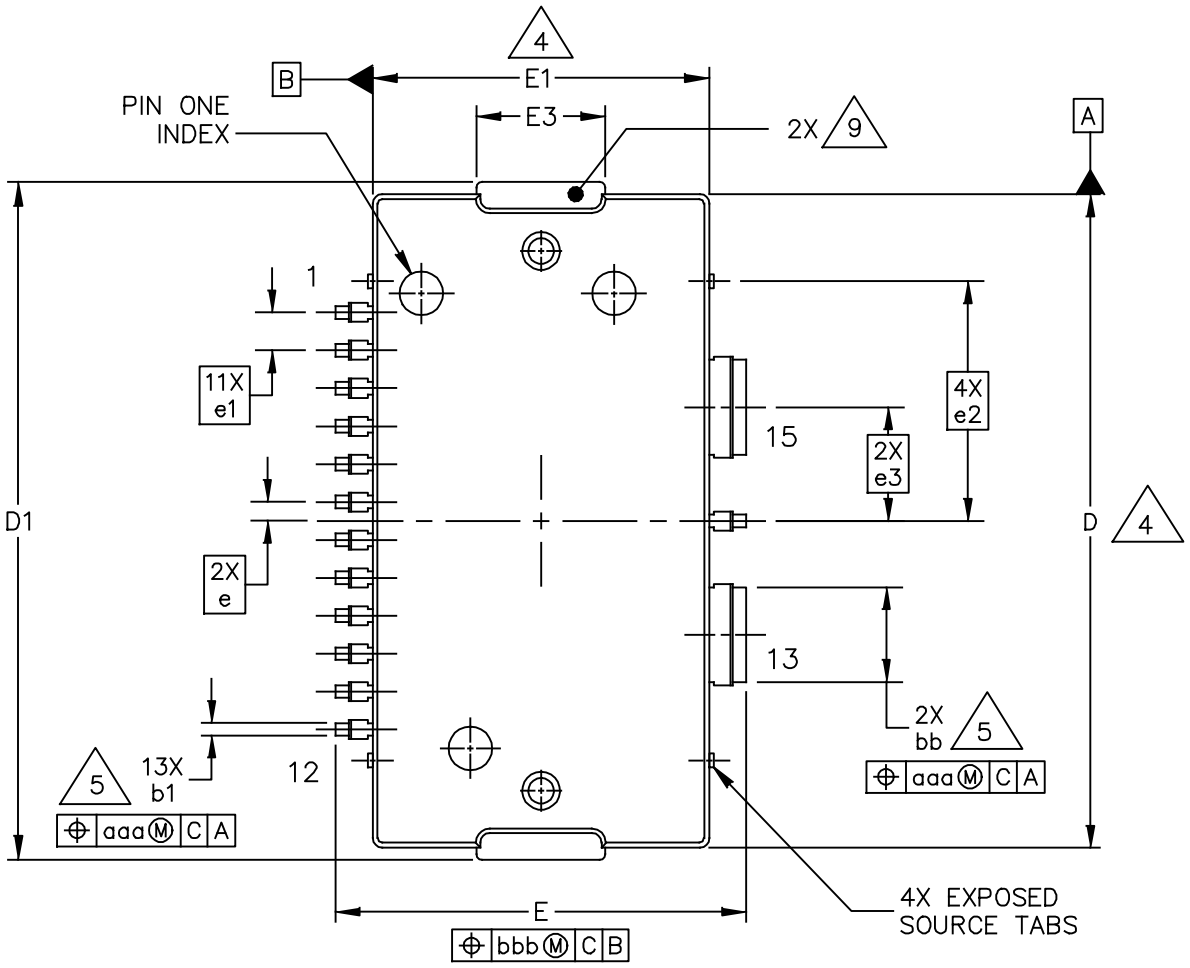
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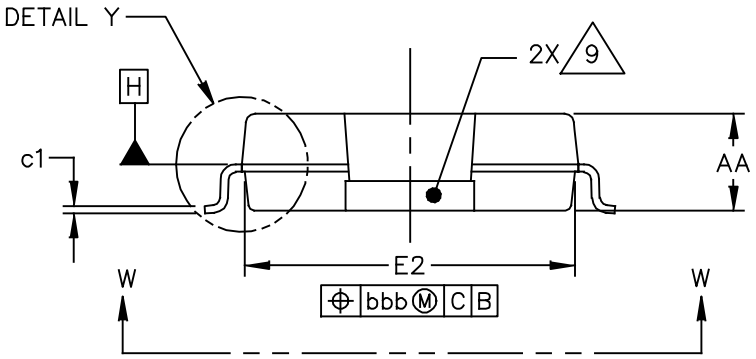
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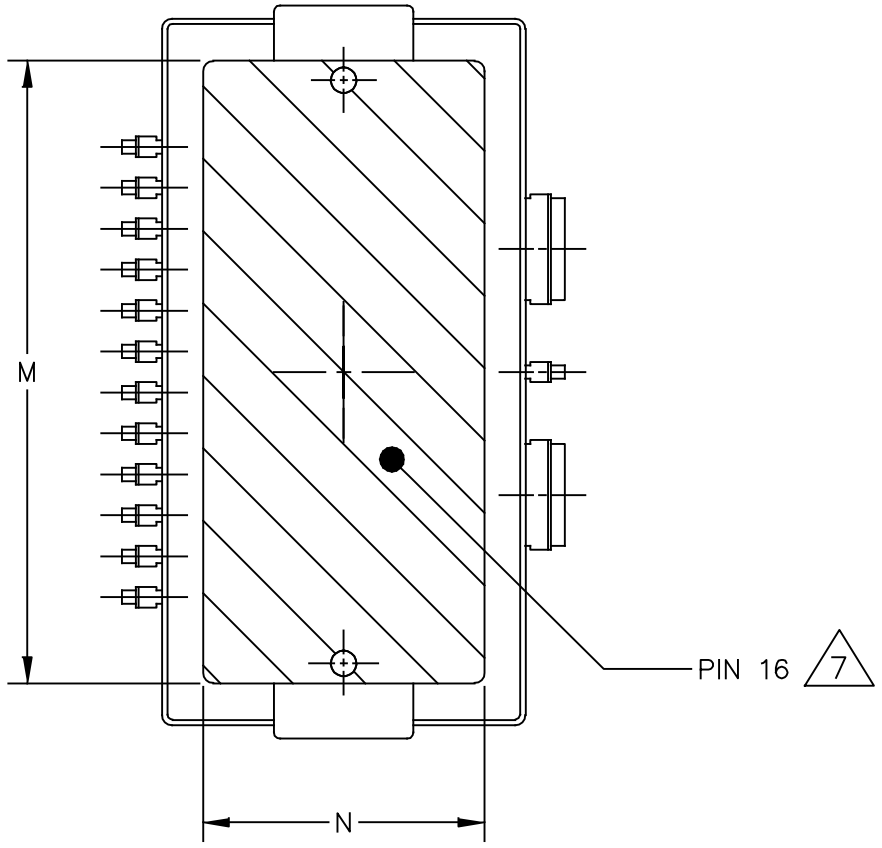
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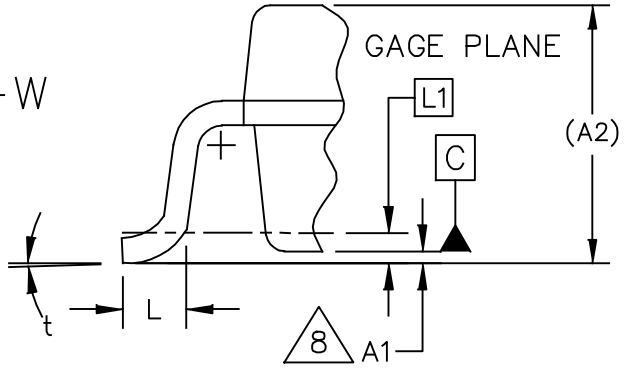




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VIEW W–W



DETAIL "Y"

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NOTES:

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5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	M	.600	----	15.24	----
A1	.001	.004	0.03	0.10	N	.270	----	6.86	----
A2	(.105)		(2.67)		bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	c1	.007	.011	0.18	0.28
E	.429	.437	10.90	11.10	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	e3	.120 BSC		3.05 BSC	
L	.018	.024	0.46	0.61	t	2°	8°	2°	8°
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
					bbb	.008		0.20	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2016	• Initial release of data sheet

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Rev. 0, 3/2016

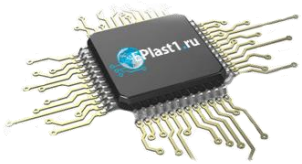
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Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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