

# 1A High Efficiency 2-Cell Supercapacitor Charger with Automatic Cell Balancing

## FEATURES

- High Efficiency Step-Up/Step-Down Charging of Two Series Supercapacitors
- Automatic Cell Balancing Prevents Capacitor Overvoltage During Charging
- Programmable Charging Current Up to 500mA (Single Inductor), 1A (Dual Inductor)
- $V_{IN} = 2.7V$  to  $5.5V$
- Selectable 2.4V/2.65V Regulation per Cell (LTC3625)
- Selectable 2V/2.25V Regulation per Cell (LTC3625-1)
- Low No-Load Quiescent Current:  $23\mu A$
- $I_{VOUT}, I_{VIN} < 1\mu A$  in Shutdown
- Low Profile 12-lead  $3mm \times 4mm$  DFN Package

## APPLICATIONS

- Servers, RAID Systems, Mass Storage, High Current Backup Supplies
- Solid State Hard Drives
- Wireless Power Meters
- High Peak Power Boosted Supplies

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## DESCRIPTION

The LTC<sup>®</sup>3625/LTC3625-1 are programmable supercapacitor chargers designed to charge two supercapacitors in series to a fixed output voltage (4.8V/5.3V or 4V/4.5V selectable) from a 2.7V to 5.5V input supply. Automatic cell balancing prevents overvoltage damage to either supercapacitor while maximizing charge rate. No balancing resistors are required.

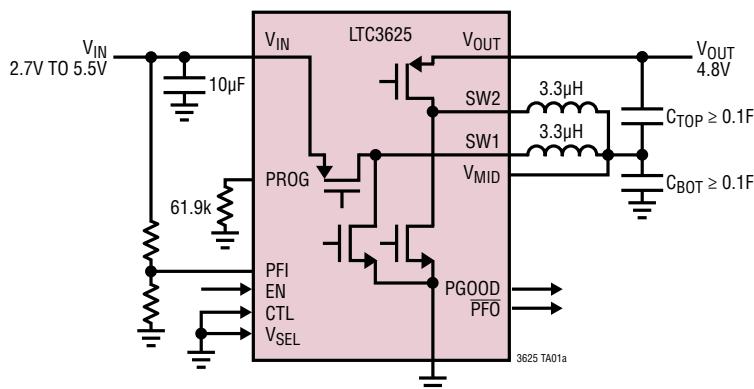
High efficiency, high charging current, low quiescent current and low minimum external parts count (one inductor, one bypass capacitor at  $V_{IN}$  and one programming resistor) make the LTC3625/LTC3625-1 ideally suited for small form factor backup or high peak power systems.

Charging current/maximum input current level is programmed with an external resistor. When the input supply is removed and/or the EN pin is low, the LTC3625/LTC3625-1 automatically enter a low current state, drawing less than  $1\mu A$  from the supercapacitors.

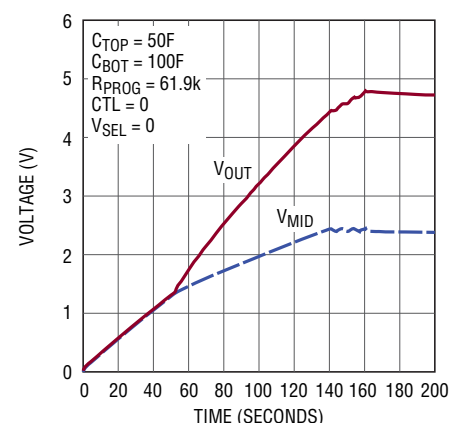
The LTC3625/LTC3625-1 are available in a compact 12-lead  $3mm \times 4mm \times 0.75mm$  DFN package.

## TYPICAL APPLICATION

1A SCAP Charger



Charging Two 2:1 Mismatched Supercapacitors



3625 TA01b

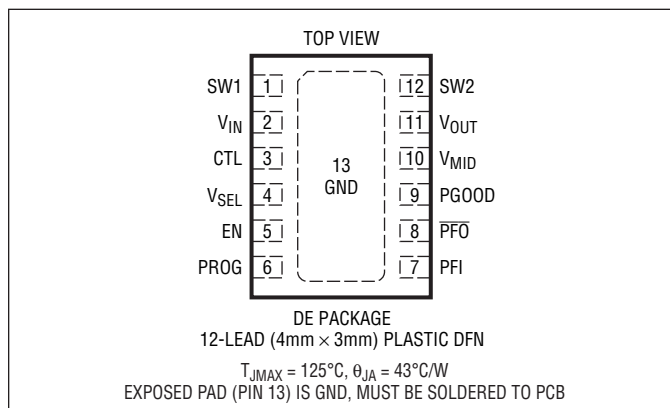
# LTC3625/LTC3625-1

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{IN}$ , $V_{OUT}$ (Transient) $t < 1\text{ms}$ , Duty Cycle $< 1\%$ .....	-0.3V to 7V
$V_{IN}$ , $V_{OUT}$ , $V_{MID}$ , $PGOOD$ , $CTL$ , $PROG$ , $PFI$ , $PFO$ .....	-0.3V to 6V
$EN$ , $V_{SEL}$ .....	-0.3V to $V_{IN} + 0.3V$
$V_{OUT}$ Short-Circuit Duration .....	Indefinite
$I_{PGOOD}$ , $I_{PFO}$ .....	50mA
$I_{PROG}$ .....	1mA
$I_{VIN}$ , $I_{SW1}$ , $I_{SW2}$ , $I_{VOUT}$ (Note 2) .....	3A
Operating Junction Temperature Range (Notes 3, 4) .....	-40°C to 125°C
Storage Temperature Range .....	-65°C to 125°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3625EDE#PBF	LTC3625EDE#TRPBF	3625	12-Lead (4mm × 3mm) Plastic DFN	-40°C to 125°C
LTC3625EDE-1#PBF	LTC3625EDE-1#TRPBF	36251	12-Lead (4mm × 3mm) Plastic DFN	-40°C to 125°C
LTC3625IDE#PBF	LTC3625IDE#TRPBF	3625	12-Lead (4mm × 3mm) Plastic DFN	-40°C to 125°C
LTC3625IDE-1#PBF	LTC3625IDE-1#TRPBF	36251	12-Lead (4mm × 3mm) Plastic DFN	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ .  $V_{IN} = 3.6V$ ,  $R_{PROG} = 143k$ , unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN}$	Input Voltage Range	●	$V_{IN(UVLO)}$		5.5	V
$V_{IN(UVLO)}$	Input Undervoltage Lockout ( $V_{IN}$ Rising)	$V_{SEL} = V_{IN}$ (LTC3625) ● $V_{SEL} = 0V$ (LTC3625) ● $V_{SEL} = 0V$ or $V_{IN}$ (LTC3625-1) ●	2.8 2.53 2.53	2.9 2.63 2.63	3.0 2.73 2.73	V V V
	Input UVLO Hysteresis			100		mV
$V_{OUT(SLEEP)}$	Charger Termination Voltage	$V_{SEL} = V_{IN}$ (LTC3625) ● $V_{SEL} = 0V$ (LTC3625) ● $V_{SEL} = V_{IN}$ (LTC3625-1) ● $V_{SEL} = 0V$ (LTC3625-1) ●	5.2 4.7 4.4 3.9	5.3 4.8 4.5 4.0	5.4 4.9 4.6 4.1	V V V V
	Recharge Hysteresis	Below $V_{OUT(SLEEP)}$		135		mV
$V_{TOP}$ , $V_{BOT}$	Maximum Voltage Across Either of the Supercapacitors After Charging	$V_{SEL} = V_{IN}$ , $V_{OUT} = 5.3V$ (LTC3625) ● $V_{SEL} = 0V$ , $V_{OUT} = 4.8V$ (LTC3625) ● $V_{SEL} = V_{IN}$ , $V_{OUT} = 4.5V$ (LTC3625-1) ● $V_{SEL} = 0V$ , $V_{OUT} = 4V$ (LTC3625-1) ●		2.7 2.45 2.3 2.05	2.75 2.5 2.35 2.1	V V V V
	Maximum Supercapacitor Offset After Charging	$CTL = 0V$ $CTL = V_{IN}$		100 50	180 120	mV mV

# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 3.6\text{V}$ ,  $R_{PROG} = 143\text{k}$ , unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{VIN}$	Input Operating Current, $I_{SW1} = I_{SW2} = 0\mu\text{A}$ , No Switching	CTL = $V_{IN}$ , $V_{MID} = 1.5\text{V}$ , $V_{OUT} = 2.5\text{V}$ (Boost Only) CTL = $V_{IN}$ , $V_{MID} = 1.5\text{V}$ , $V_{OUT} = 3.5\text{V}$ (Buck Only) CTL = 0, $V_{MID} = 1.5\text{V}$ , $V_{OUT} = 2.5\text{V}$ (Buck and Boost)		135 275 365	200 400 530	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$
	Input Sleep Current	$V_{IN} = 5.5\text{V}$ , $V_{OUT} = 5.4\text{V}$ $V_{IN} = 3.6\text{V}$ , $V_{OUT} = 5.4\text{V}$		23 8	35 15	$\mu\text{A}$ $\mu\text{A}$
	Input SD Current	$V_{OUT} = 0\text{V}$		0	1	$\mu\text{A}$
$I_{VOUT}$	$V_{OUT}$ SD Current	$V_{OUT} = 5.4\text{V}$		0	1	$\mu\text{A}$
	$V_{OUT}$ Sleep Current	$V_{OUT} = 5.4\text{V}$ , $V_{IN} = 3.6\text{V}$ , $EN = V_{IN}$ $V_{OUT} = 5.4\text{V}$ , $V_{IN} = 5.5\text{V}$ , $EN = V_{IN}$		17 1	25 2.5	$\mu\text{A}$ $\mu\text{A}$
$V_{PROG}$	PROG Servo Voltage	$V_{OUT} = 3.5\text{V}$ , $V_{MID} = 1.5\text{V}$	● 1.17	1.2	1.23	V
$h_{PROG}$	Ratio of Measured $I_{PROG}$ Current to $I_{BUCK}$ Programmed Current			118,000		
$I_{BUCK}$	Programmed Buck Charge Current	$R_{PROG} = 143\text{k}$ (Note 5) $R_{PROG} = 71.5\text{k}$ (Note 5)	0.88	0.99	1.10	A
			1.76	1.98	2.20	A
$I_{MAX}$	Maximum Programmed Charge Current	$R_{PROG} = 0\Omega$ (Fault Condition) (Note 5)	1.98	2.65	3.31	A
$V_{MID(GOOD)}$	$V_{MID}$ Voltage Where the Boost Regulator is Enabled			1.35		V
	$V_{MID(GOOD)}$ Hysteresis			150		mV
$V_{TRICKLE}$	$V_{OUT}$ Voltage Above Which Boost Regulator Will Exit Trickle Charge Mode and Enter Normal Charge Mode	$V_{OUT}$ Rising		$V_{MID}$		V
	$V_{TRICKLE}$ Falling Hysteresis			50		mV
$I_{PEAK(BUCK)}$	Buck Charge Current Peak			$1.1 \cdot I_{BUCK}$		A
$I_{VALLEY(BUCK)}$	Buck Charge Current Valley			$0.9 \cdot I_{BUCK}$		A
$I_{PEAK(BOOST)}$	Boost Charge Current Peak	$V_{OUT} = 3\text{V}$ , $V_{MID} = 2\text{V}$ (Note 5) $V_{OUT} = 1\text{V}$ , $V_{MID} = 2\text{V}$ (Note 5)	1.59	2.12 200	2.65	A mA
$I_{VALLEY(BOOST)}$	Boost Charge Current Valley	$V_{OUT} = 3\text{V}$ , $V_{MID} = 2\text{V}$ $V_{OUT} = 1\text{V}$ , $V_{MID} = 2\text{V}$	1.41	1.88 0	2.35	A mA
	Maximum Boost Valley Time	$V_{OUT} = 1\text{V}$ , $V_{MID} = 2\text{V}$		6.5		$\mu\text{s}$
$R_{PMOS}$	PMOS On-Resistance			120		$\text{m}\Omega$
$R_{NMOS}$	NMOS On-Resistance			100		$\text{m}\Omega$
$I_{LEAK}$	SW Pin Leakage Current for SW1, SW2	$EN = 0\text{V}$			1	$\mu\text{A}$
$V_{PFI}$	PFI Falling Threshold	●	1.17	1.2	1.23	V
	PFI Hysteresis			15		mV
$I_{PFI}$	Pin Leakage Current for PFI Pin			0	30	nA
<b>Logic (EN, CTL, <math>V_{SEL}</math>, PGOOD, <math>P\overline{F}O</math>)</b>						
$V_{IL}$	Input Low Logic Voltage	EN, CTL, $V_{SEL}$ Pins	●		0.4	V
$V_{IH}$	Input High Logic Voltage	EN, CTL, $V_{SEL}$ Pins	●	1.2		V
$I_{IL}$ , $I_{IH}$	Input Low, High Current for CTL	CTL			1	$\mu\text{A}$
$R_{PD}$	EN Pin Pull-Down Resistance			4.5		$\text{M}\Omega$
	$V_{SEL}$ Pin Pull-Down Resistance	$EN = V_{IN}$		4.5		$\text{M}\Omega$
$V_{OL}$	Output Low Logic Voltage	PGOOD, $P\overline{F}O$ Pins; Sinking 5mA	●	70	200	mV
$I_{OH}$	Logic High Leakage Current	PGOOD, $P\overline{F}O$ Pins; Pin Voltage = 5V			1	$\mu\text{A}$
	PGOOD Rising Threshold	$V_{OUT}$ as a Percentage of Final Target	90	92.5	95	%
	PGOOD Hysteresis	$\Delta V_{OUT}$ as a Percentage of Final Target		3		%

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## ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3625/LTC3625-1 internal switches are guaranteed to survive up to 3A of peak current. Internal current limits will restrict peak current to lower levels.

**Note 3:** The LTC3625/LTC3625-1 are tested under pulsed load conditions such that  $T_J \approx T_A$ . The LTC3625E/LTC3625E-1 are guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the -40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3625/LTC3625-1 are guaranteed over the -40°C to 125°C operating junction temperature range.

The junction temperature ( $T_J$  in °C) is calculated from the ambient temperature ( $T_A$  in °C) and power dissipation ( $P_D$  in Watts) according to the formula:

$$T_J = T_A + (P_D \cdot \theta_{JA})$$

where  $\theta_{JA}$  (in °C/W) is the package thermal impedance.

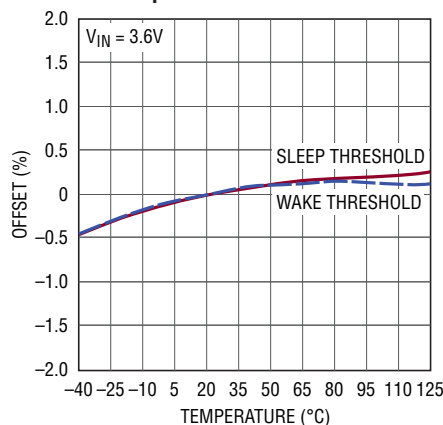
**Note 4:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability or permanently damage the device.

**Note 5:** Measurements are tested with CTL = 0V.

## TYPICAL PERFORMANCE CHARACTERISTICS

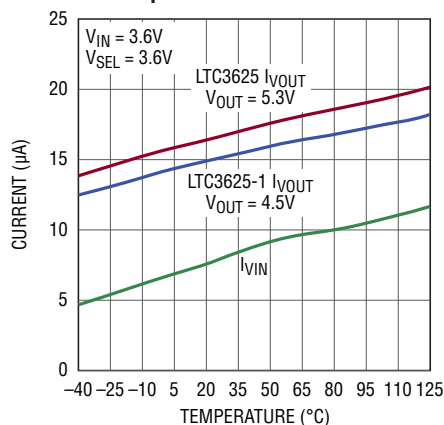
$T_A = 25^\circ\text{C}$ ,  $L_1 = 3.3\mu\text{H}$ ,  $L_2 = 3.3\mu\text{H}$ ,  $C_{IN} = 10\mu\text{F}$ ,  $C_{TOP} = C_{BOT}$ , LTC3625 unless otherwise specified.

**Charge Termination Error vs Temperature**



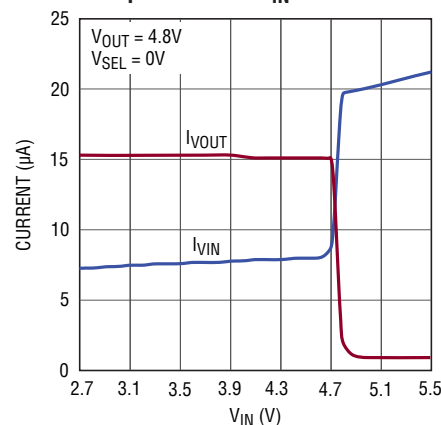
3625 G13

**Input and Output Sleep Currents vs Temperature**



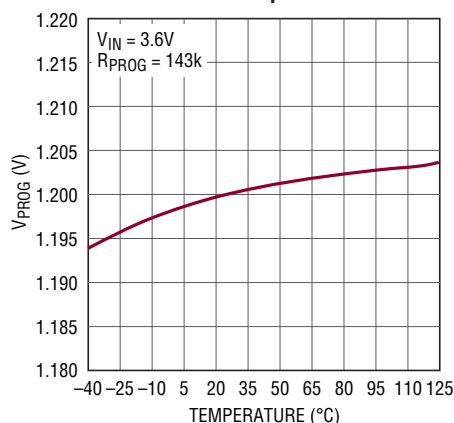
3625 G14

**Sleep Current vs VIN**



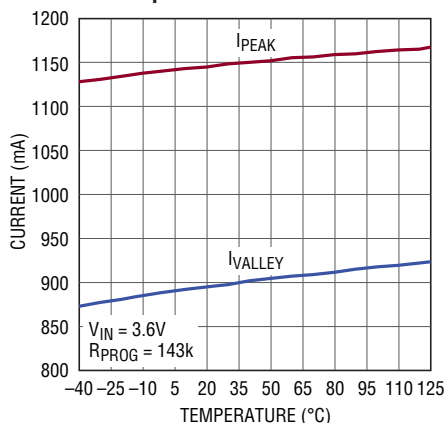
3625 G01

**PROG Voltage and PFI Falling Threshold vs Temperature**



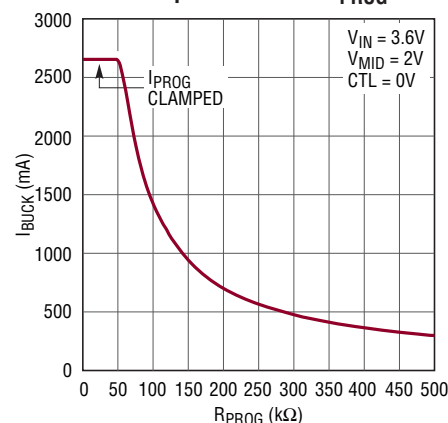
3625 G02

**Buck Current Limits vs Temperature**



3625 G03

**Buck Output Current vs R\_PROG**

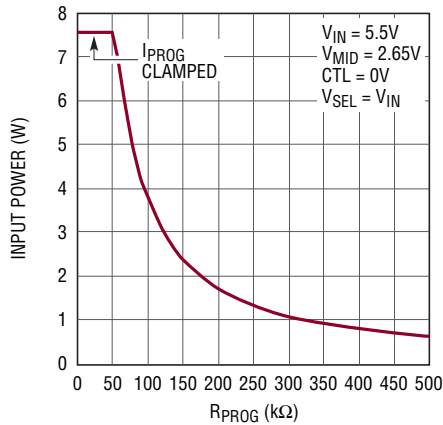


3625 G04  
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# TYPICAL PERFORMANCE CHARACTERISTICS

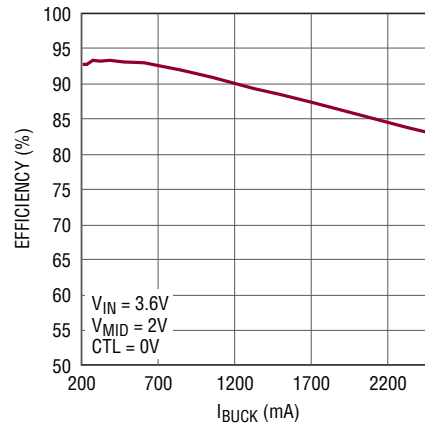
$T_A = 25^\circ\text{C}$ ,  $L_1 = 3.3\mu\text{H}$ ,  $L_2 = 3.3\mu\text{H}$ ,  $C_{IN} = 10\mu\text{F}$ ,  $C_{TOP} = C_{BOT}$ , LTC3625 unless otherwise specified.

### Buck Input Power vs $R_{PROG}$



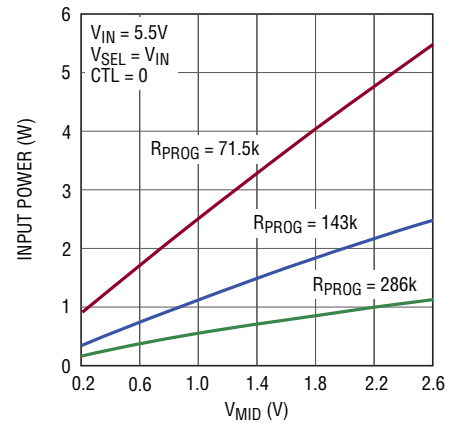
3625 G05

### Buck Efficiency vs $I_{BUCK}$



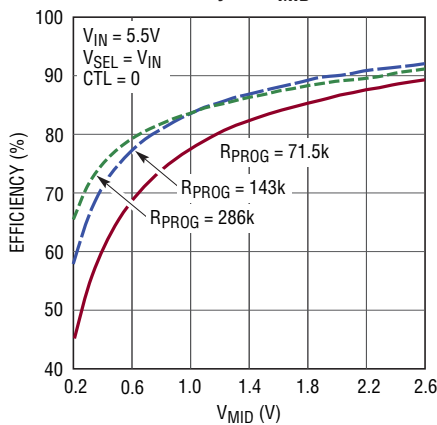
3625 G06

### Buck Input Power vs $V_{MID}$



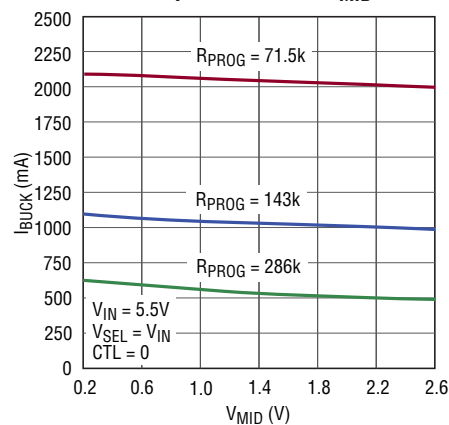
3625 G07

### Buck Efficiency vs $V_{MID}$



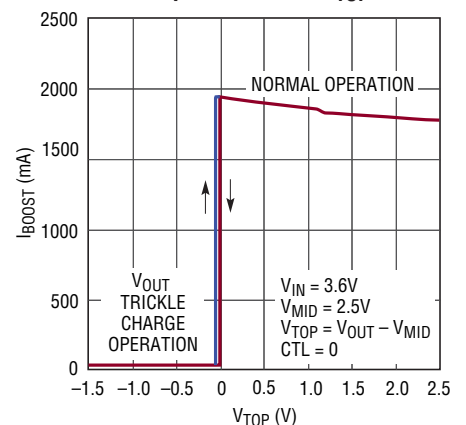
3625 G08

### Buck Output Current vs $V_{MID}$



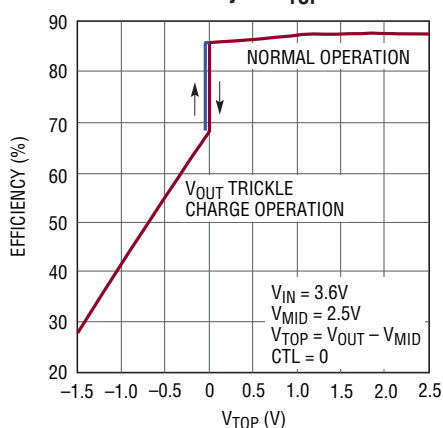
3625 G09

### Boost Input Current vs $V_{TOP}$



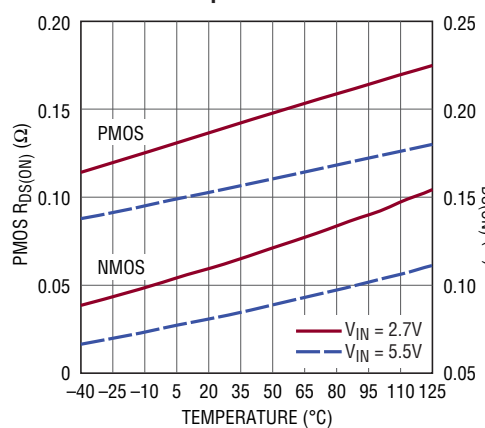
3625 G10

### Boost Efficiency vs $V_{TOP}$



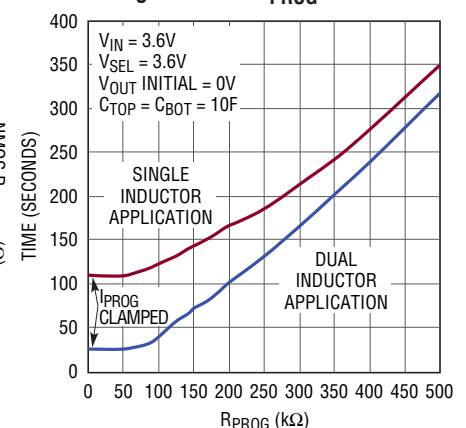
3625 G11

### RFET vs Temperature



3625 G12

### Charge Time vs $R_{PROG}$

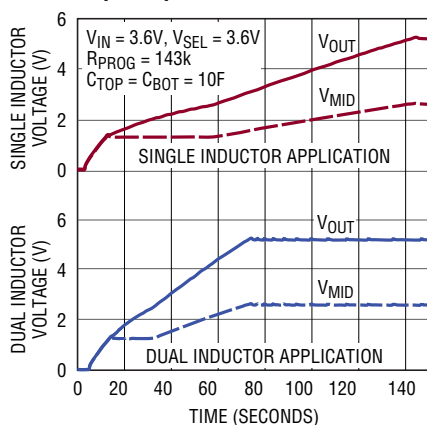


3625 G15

## TYPICAL PERFORMANCE CHARACTERISTICS

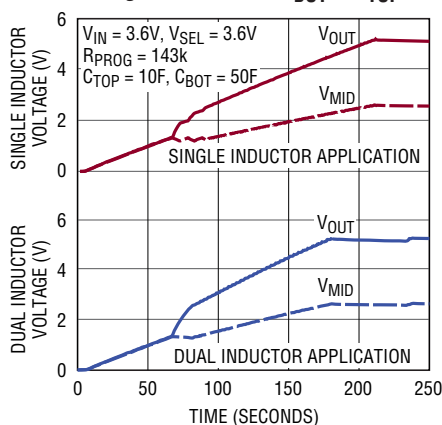
$T_A = 25^\circ\text{C}$ ,  $L_1 = 3.3\mu\text{H}$ ,  $L_2 = 3.3\mu\text{H}$ ,  $C_{IN} = 10\mu\text{F}$ ,  $C_{TOP} = C_{BOT}$ , LTC3625 unless otherwise specified.

Charge Profile Into Matched SuperCaps



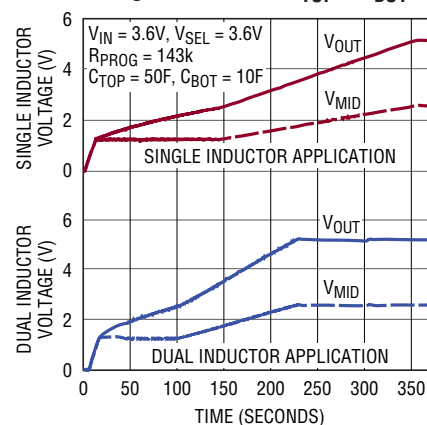
3625 G16

Charge Profile with  $C_{BOT} > C_{TOP}$



3625 G17

Charge Profile with  $C_{TOP} > C_{BOT}$



3625 G18

## PIN FUNCTIONS

**SW1 (Pin 1):** Switch Pin for the Buck Regulator. External inductor connects between SW1 pin and  $V_{MID}$ .

**$V_{IN}$  (Pin 2):** Input Voltage Pin. Bypass to GND with a  $10\mu\text{F}$  or larger ceramic capacitor.

**CTL (Pin 3):** Logic Input. CTL sets the charge mode of the LTC3625/LTC3625-1. A logic high at CTL programs the part to operate with a single inductor; a logic low programs the part to operate with two inductors. In the 2-inductor application the capacitor stack will charge approximately twice as quickly. CTL is a high impedance input and must be tied to either  $V_{IN}$  or GND. Do not float.

**$V_{SEL}$  (Pin 4):** Logic Input.  $V_{SEL}$  selects the output voltage of the LTC3625/LTC3625-1. A logic low at  $V_{SEL}$  sets the per-cell maximum voltage to 2.45V/2.05V ( $V_{OUT} = 4.8\text{V}/4.0\text{V}$ ); a logic high sets the per-cell maximum voltage to 2.70V/2.30V ( $V_{OUT} = 5.3\text{V}/4.5\text{V}$ ). When the part is enabled,  $V_{SEL}$  has a  $4.5\text{M}\Omega$  internal pull-down resistor; if EN is low, then  $V_{SEL}$  is a high impedance input pin.

**EN (Pin 5):** Logic Input. Enables the LTC3625/LTC3625-1. Active high. Has a  $4.5\text{M}\Omega$  internal pull-down resistor.

**PROG (Pin 6):** Charge Current Program Pin. Connecting a resistor from PROG to ground programs the buck output current. This pin serves to 1.2V.

**PFI (Pin 7):** Input to the Power Fail Comparator. This pin connects to an external resistor divider between  $V_{IN}$  and GND. If this functionality is not desired, PFI should be tied to  $V_{IN}$ .

**$\overline{\text{PFO}}$  (Pin 8):** Open-Drain Output of the Power-Fail Comparator. The part pulls this pin low if  $V_{IN}$  is less than a value programmed by an external divider. This pin is active low in shutdown mode. If this functionality is not desired  $\overline{\text{PFO}}$  should be left unconnected.

**PGOOD (Pin 9):** Logic Output. This is an open-drain output which indicates that  $V_{OUT}$  has settled to its final value. Upon start-up, this pin remains low until the output voltage,  $V_{OUT}$ , is within 92.5% (typical) of its final value. Once  $V_{OUT}$  is valid, PGOOD becomes high impedance. If  $V_{OUT}$  falls to 89.5% (typical) of its correct regulation level, PGOOD is pulled low. PGOOD may be pulled up through an external resistor to an appropriate reference level. This pin is active low in shutdown mode.

## PIN FUNCTIONS

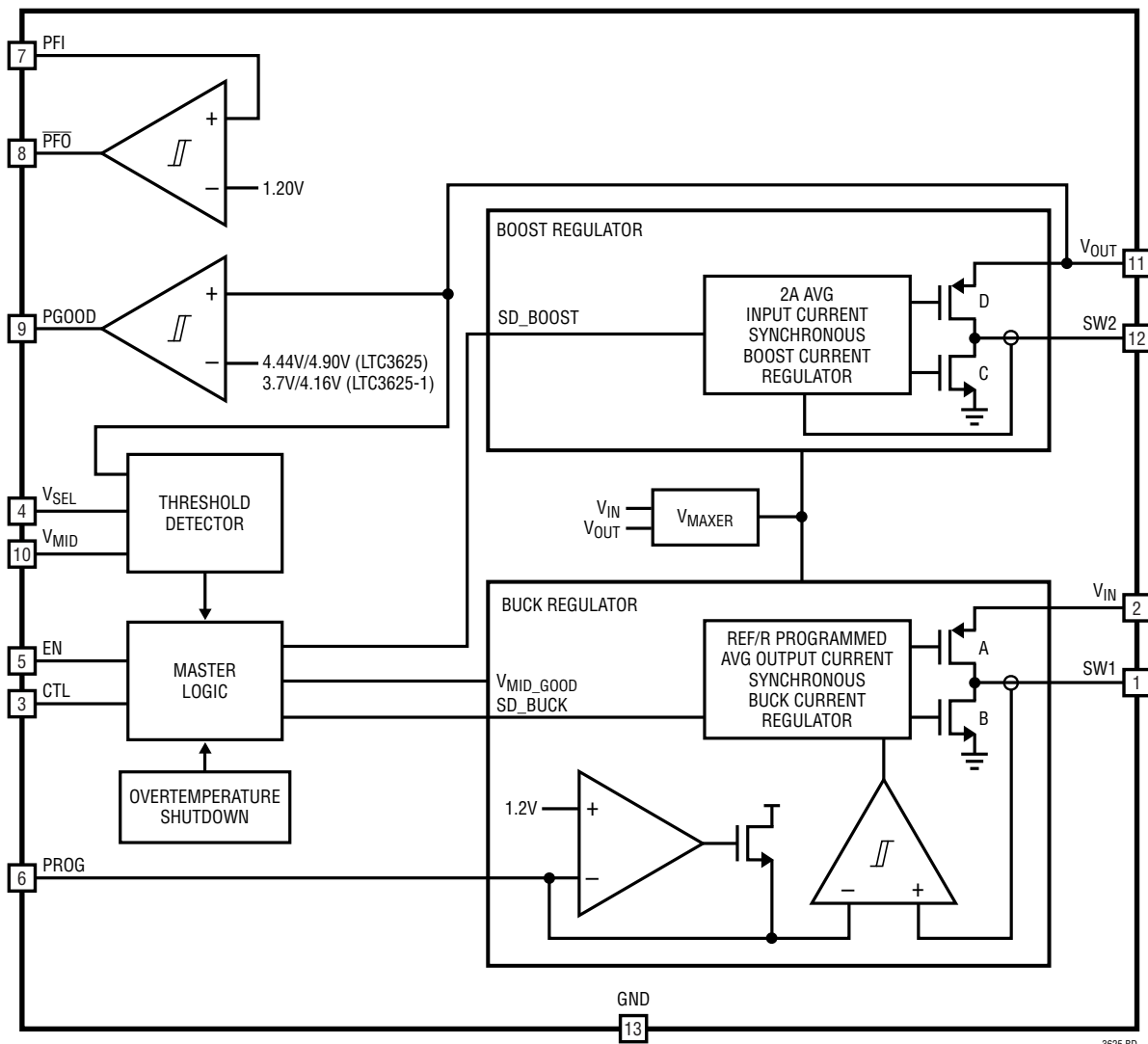
**V<sub>MID</sub> (Pin 10):** Midpoint of Two Series Supercapacitors. The pin voltage is monitored and used, along with V<sub>OUT</sub>, to enable or shut down the buck and boost converters during charging to achieve voltage balancing of the top and bottom supercapacitors.

**V<sub>OUT</sub> (Pin 11):** Output Voltage Pin. Connect V<sub>OUT</sub> to the positive terminal of the top supercapacitor. The pin voltage is monitored and used, along with V<sub>MID</sub>, to enable or shut down the buck and boost converters during charging to achieve voltage balancing of the top and bottom supercapacitors.

**SW2 (Pin 12):** Switch Pin for the Boost Regulator. External inductor connects between the SW2 pin and V<sub>MID</sub>. If CTL is logic high, then SW2 must be connected to SW1.

**GND (Exposed Pad Pin 13):** Ground. The exposed pad must be connected to a continuous ground plane on the printed circuit board directly under the LTC3625/LTC3625-1 for electrical contact and to achieve rated thermal performance.

## BLOCK DIAGRAM



3625 BD

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## OPERATION

The LTC3625/LTC3625-1 are dual cell supercapacitor chargers. Their unique topology charges two series connected capacitors to a fixed output voltage with programmable charging current without overvoltageing either of the cells—even if they are severely mismatched. No balancing resistors are required. The LTC3625/LTC3625-1 include an internal buck converter between  $V_{IN}$  and  $V_{MID}$  to regulate the voltage on  $C_{BOT}$  (across the bottom capacitor) as well as an internal boost converter between  $V_{MID}$  and  $V_{OUT}$  to regulate the voltage on  $C_{TOP}$  (across the top capacitor). The output current of the buck converter is user-programmed via the PROG pin and the input current of the boost converter is set at 2A (typical).

Table 1 indicates the various functions of the LTC3625/LTC3625-1 that can be digitally controlled.

**Table 1. Digital Input Functions**

PIN	VALUE	FUNCTION
CTL*	0	Part runs in 2-inductor application
	1	Part runs in 1-inductor application
VSEL	0	4.8V/4.0V sleep threshold
	1	5.3V/4.5V sleep threshold
EN	0	Part shuts down, $V_{OUT}$ becomes high impedance
	1	Part enables and regulates the output

\*CTL pin must be hard tied to either  $V_{IN}$  or GND.

### $V_{IN}$ Undervoltage Lockout (UVLO)

An internal undervoltage lockout circuit monitors  $V_{IN}$  and keeps the LTC3625/LTC3625-1 disabled until  $V_{IN}$  rises above 2.90V/2.63V (typical) if  $V_{SEL}$  is high or 2.63V/2.63V (typical) if  $V_{SEL}$  is low. Hysteresis on the UVLO turns off the LTC3625/LTC3625-1 if  $V_{IN}$  drops by approximately 100mV below the UVLO rising threshold. When in UVLO, only current needed to detect a valid input will be drawn from  $V_{IN}$  and  $V_{OUT}$ .

### Buck Converter

The buck converter regulates a user-programmed average output current given by:

$$I_{BUCK} = h_{PROG} \cdot \frac{1.2V}{R_{PROG}}$$

where  $h_{PROG} = 118,000$  (typical).

The buck converter regulates the current hysteretically by switching on the buck PMOS until a peak current limit is reached and then turning on the buck NMOS until a valley current limit is reached. In the single inductor application the boost NMOS is used in conjunction with the buck NMOS to increase efficiency at high currents. The forward current limit is set to  $1.1 \cdot I_{BUCK}$  (typical) and the valley current limit is set to  $0.9 \cdot I_{BUCK}$  (typical). Because of this method of regulation, overcurrent limit and reverse-current limit protection is automatically provided. The LTC3625/LTC3625-1 will continue to regulate its programmed current even into a grounded output.

In fault conditions where the PROG pin is shorted to ground, or  $R_{PROG}$  is conductive enough to program  $I_{BUCK}$  to operate outside of specification, the current out of the PROG pin will be clamped to 22.5 $\mu$ A (typical) and  $I_{BUCK}$  will be set to 2.65A (typical). If input current limit is not a concern, the PROG pin may be grounded to minimize charge times.

### Boost Converter

The boost converter regulates a fixed average input current of 2A (typical). The current is regulated hysteretically by switching on the boost NMOS until the peak current limit of 2.12A (typical) is reached, and turning on the boost PMOS until the valley current limit of 1.88A (typical) is reached. In the single inductor application the buck NMOS is used in conjunction with the boost NMOS to increase efficiency. Because of this method of regulation, overcurrent limit and reverse-current limit protection is automatically provided.

In normal operation  $V_{OUT}$  will increase with  $V_{MID}$  so  $V_{OUT}$  should never be below  $V_{MID}$ . In the case where there is a reverse voltage on  $C_{TOP}$  due to a faulty precondition or a large load on the output, the boost converter will operate in trickle charge mode. In this mode the boost PMOS gate will remain high and instead allow the SW2 node to increase until  $SW2 \approx V_{MAX} + 1V$  to allow a higher reverse voltage across the inductor, and the current is ramped down to 0mA. This will result in a less efficient charge delivery through the PMOS. To keep dissipation low,  $I_{PEAK}$  is limited to 200mA (typical). In this mode the discharge phase is terminated if it lasts longer than 6.5 $\mu$ s (typical).

The boost converter is disabled if  $V_{MID}$  falls below the  $V_{MID(GOOD)}$  hysteresis threshold of 1.2V (typical).



## OPERATION

### Single Inductor Operation

With the CTL pin tied to  $V_{IN}$  the LTC3625/LTC3625-1 will operate in single inductor mode. In this mode the same inductor serves in the power path for both the buck and the boost converters. Thus, the buck converter and boost converter will never run simultaneously.

Under certain conditions with a single inductor, a small amount of current can flow from the supercapacitors to  $V_{IN}$  when the boost charger is active. A 25mA load is required on  $V_{IN}$  to prevent the  $V_{IN}$  supply from being pumped to a higher voltage while the boost is active. This minimum load is not needed in the two inductor application and it is also not needed when the charger is disabled.

A typical charge cycle for a fully discharged capacitor stack will proceed as follows:

1. The buck converter will turn on and regulate its output current ramping hysteretically between  $1.1 \cdot I_{BUCK}$  and  $0.9 \cdot I_{BUCK}$  until the  $V_{MID(GOOD)}$  threshold is met (1.35V typical).
2. Once the  $V_{MID(GOOD)}$  threshold is reached, the boost converter will turn on and regulate its input current ramping hysteretically between 2.12A and 1.88A until  $V_{MID}$  falls below the  $V_{MID(GOOD)}$  hysteresis threshold (1.2V typical).
3. Phases 1 and 2 will alternate until  $V_{OUT}$  is approximately 2.4V. When  $V_{TOP}$  (equal to  $V_{OUT} - V_{MID}$ ) is approximately 50mV  $> V_{MID}$ , the boost regulator will turn off and the buck regulator will turn on. Likewise, when  $V_{MID}$  is approximately 50mV  $> V_{TOP}$ , the boost regulator will turn on and the buck regulator will turn off.
4. Phase 3 will continue until  $V_{OUT}$  has reached its programmed output voltage. Once this happens, the part will enter sleep mode and only minimal power will be consumed (see the Electrical Characteristics table).
5. If the supercapacitors' self discharge or an external load cause the output to drop by more than 135mV (typical), then the LTC3625/LTC3625-1 will exit sleep mode and begin charging the appropriate supercapacitor.

In all cases whenever either of the converters is shut down, it will switch to its appropriate discharge phase (NMOS on for the buck and PMOS on for the boost) until

the inductor current reaches 0mA. This optimizes charge delivery to the output capacitors.

Charge time is dependant on the programmed buck output current as well as the value of the supercapacitors being charged. For estimating charge profiles in the single inductor application, see the Typical Performance Characteristics graph Charge Time vs  $R_{PROG}$ .

The effective average  $V_{OUT}$  referred charge current can be approximated as:

$$I_{CHARGE} \cong 0.5 \cdot I_{BUCK} \cdot \epsilon_{BOOST} \cdot \frac{2A}{I_{BUCK} + 2A}$$

where  $\epsilon_{BOOST}$  is the boost converter efficiency, which is typically about 85% (see the Typical Performance Characteristics graph Boost Efficiency vs  $V_{TOP}$ ).

Seen another way, this is the maximum steady-state load the part can support without losing  $V_{OUT}$  regulation.

### Dual Inductor Operation

With the CTL pin tied to GND, the LTC3625/LTC3625-1 will operate in dual inductor mode. In this mode two inductors will serve as the power path for the buck and the boost converters. This will allow both the buck and the boost converter to run simultaneously. As a result, the total charge time will be greatly reduced at the cost of an additional board component.

A typical charge cycle for a fully discharged capacitor stack will proceed as follows:

1. The buck converter will turn on and regulate its output current ramping hysteretically between  $1.1 \cdot I_{BUCK}$  and  $0.9 \cdot I_{BUCK}$  until the  $V_{MID(GOOD)}$  threshold is met (1.35V typical).
2. Once the  $V_{MID(GOOD)}$  threshold is reached, the boost converter will turn on and regulate its input current ramping hysteretically between 2.12A and 1.88A. The buck converter will continue to run at the same time. In some cases ( $I_{BUCK} \sim <1A$ ) the boost converter's input current will exceed the current delivered to  $C_{BOT}$ ; even though the buck converter is running, charge will be removed and  $V_{MID}$  may decrease. Thus, if  $V_{MID}$  falls below the  $V_{MID(GOOD)}$  hysteresis threshold, the boost

## OPERATION

converter will turn off. Once  $V_{MID}$  has again risen above the  $V_{MID(GOOD)}$  threshold, the boost converter will be re-enabled. In the case where  $V_{OUT} < V_{MID}$ , the boost converter will operate in trickle charge mode until  $V_{OUT}$  exceeds  $V_{MID}$  (see Boost Converter).

3. During phase 2, if  $C_{BOT}$  exceeds its individual maximum threshold voltage (2.45V/2.05V typical if  $V_{SEL}$  is low or 2.7V/2.3V typical if  $V_{SEL}$  is high) or if  $V_{TOP}$  exceeds  $V_{BOT}$  by more than 50mV (typical), then the appropriate converter will turn off until the capacitor has fallen below its hysteresis threshold (2.40V/2V typical if  $V_{SEL}$  is low and 2.65V/2.25V typical if  $V_{SEL}$  is high for the buck converter or  $V_{TOP} < V_{MID} - 50mV$  typical for the boost converter).
4. Once  $V_{OUT}$  has reached its programmed output voltage, the part will enter sleep mode, and only minimal power will be consumed (see the Electrical Characteristics table).
5. If the supercapacitors' self discharge or an external load cause the output to drop by more than 135mV (typical), then the LTC3625/LTC3625-1 will exit sleep mode and begin recharging the supercapacitor stack.

In all cases, whenever either of the converters is shut down, it will switch to its appropriate discharge phase (NMOS on for the buck and PMOS on for the boost) until the inductor current reaches 0mA. This optimizes charge delivery to the output capacitors.

Charge time is dependent on the programmed buck output current as well as the value of supercapacitors being charged. For estimating charge profiles in the dual inductor application, see the Typical Performance Characteristics graph Charge Time vs  $R_{PROG}$ .

The effective average  $V_{OUT}$  referred charge current, while both converters are continuously active, can be approximated as:

$$I_{CHARGE} \cong 0.5 \cdot I_{BUCK} - 1A \cdot \left( 1 - 2 \cdot \epsilon_{BOOST} \cdot \frac{V_{MID}}{V_{OUT}} \right)$$

And, while both supercapacitors are in balance and  $V_{MID}$  is above the  $V_{MID(GOOD)}$  threshold as:

$$I_{CHARGE} \cong 0.5 \cdot I_{BUCK} \cdot \epsilon_{BOOST}$$

where  $\epsilon_{BOOST}$  is the boost converter efficiency which is typically around 85% (see the Typical Performance Characteristics graph Boost Efficiency vs  $V_{TOP}$ ).

Seen another way this is the maximum steady-state load the part can support without losing  $V_{OUT}$  regulation.

### PGOOD PIN

The PGOOD pin is an open-drain output used to indicate that  $V_{OUT}$  has approached its final regulation value. PGOOD remains active low until  $V_{OUT}$  reaches 92.5% of its regulation value at which point it will become high impedance. If  $V_{OUT}$  falls below 89.5% of its regulation voltage after PGOOD has been asserted, PGOOD will once again pull active low. PGOOD is an open-drain output and requires a pull-up resistor to the input voltage of the monitoring microprocessor or another appropriate power source. PGOOD is pulled active low in shutdown or input UVLO.

### Power-Fail Input Comparator

The PFI/ $\overline{PFO}$  pins provide an input failure notification to the user. The PFI pin is a high impedance input pin that should be tied to a resistive divider from  $V_{IN}$ .  $\overline{PFO}$  is an open-drain output and requires a pull-up resistor to the input voltage of the monitoring microprocessor or another appropriate power source. When PFI is above 1.2V,  $\overline{PFO}$  is high impedance and will be pulled up through the external resistor. If PFI drops below 1.2V,  $\overline{PFO}$  will be pulled low indicating a power failure. This allows the user to program any desired input power failure indication threshold. There is 15mV of hysteresis on the PFI pin. If this functionality is not desired the PFI pin should be tied to  $V_{IN}$ .  $\overline{PFO}$  is pulled active low in shutdown or input UVLO.

### Shutdown Operation

When the EN pin is pulled low the LTC3625/LTC3625-1 are put into shutdown. In this case, all of the active circuitry is powered down and there will be less than 1 $\mu$ A of leakage current from both  $V_{IN}$  and  $V_{OUT}$ . This allows the input to be present or absent as well as the capacitor stacks to be fully charged or discharged in shutdown without leakage between  $V_{IN}$ ,  $V_{OUT}$  and GND.

## APPLICATIONS INFORMATION

### Programming Charge Current/Maximum Input Current

The  $C_{BOT}$  charge current is programmed with a single resistor connecting the PROG pin to ground. The program resistor and buck output current are calculated using the following equation:

$$R_{PROG} = h_{PROG} \cdot \frac{1.2V}{I_{BUCK}}$$

where  $h_{PROG} = 118,000$  (typical). Excluding quiescent current,  $I_{BUCK}$  is always greater than the average buck input current. An  $R_{PROG}$  resistor value of less than 53.6k will cause the LTC3625/LTC3625-1 to enter overcurrent protection mode and proceed to charge at 2.65A (typical).

The effective buck input current can be calculated as:

$$I_{VIN} = \frac{I_{BUCK}}{\epsilon_{BUCK}} \cdot \frac{V_{MID}}{V_{IN}}$$

where  $\epsilon_{BUCK}$  is the buck converter efficiency (see the Typical Performance Characteristics graph Buck Efficiency vs  $V_{MID}$ ).

### Output Voltage Programming

The LTC3625/LTC3625-1 have a  $V_{SEL}$  input pin that allows the user to set the output threshold voltage to either 4.8V/4.0V or 5.3V/4.5V by forcing a low or high at the  $V_{SEL}$  pin respectively. In the single inductor application the chip will balance the supercapacitors to within 50mV (typical) of each other, resulting in a possible 25mV of over/undercharge per cell. In the dual inductor application the chip will balance the supercapacitors to within 100mV (typical) of each other, resulting in a possible 50mV of over/undercharge per cell.

### Thermal Management

If the junction temperature increases above approximately 150°C, the thermal shutdown circuitry automatically deactivates the output. To reduce the maximum junction temperature, a good thermal connection to the PC board is recommended. Connecting the exposed pad (Pin 13) of the DFN package to a ground plane under the device on two layers of the PC board, will reduce the thermal resistance of the package and PC board considerably.

### $V_{IN}$ Capacitor Selection

The style and value of capacitors used with the LTC3625/LTC3625-1 determine input voltage ripple. Because the LTC3625/LTC3625-1 use a step-down switching power supply from  $V_{IN}$  to  $V_{MID}$ , its input current waveform contains high frequency components. It is strongly recommended that a low equivalent series resistance (ESR) multilayer ceramic capacitor be used to bypass  $V_{IN}$ .

Tantalum and aluminum capacitors are not recommended because of their high ESR. The value of the capacitor on  $V_{IN}$  directly controls the amount of input ripple for a given  $I_{BUCK}$ . Increasing the size of this capacitor will reduce the input ripple.

Multilayer ceramic chip capacitors typically have exceptional ESR performance. MLCCs combined with a tight board layout and an unbroken ground plane will yield very good performance and low EMI emissions. There are several types of ceramic capacitors available, each having considerably different characteristics. For example, X7R ceramic capacitors have the best voltage and temperature stability. X5R ceramic capacitors have higher packing density but poorer performance over their rated voltage and temperature ranges. Y5V ceramic capacitors have the highest packing density, but must be used with caution because of their extreme non-linear characteristic of capacitance versus voltage.

The actual in-circuit capacitance of a ceramic capacitor should be measured with a small AC signal as is expected in-circuit. Many vendors specify the capacitance versus voltage with a 1V<sub>RMS</sub> AC test signal and as a result, overstate the capacitance that the capacitor will present in the application. Using similar operating conditions as the application, the user must measure or request from the vendor the actual capacitance to determine if the selected capacitor meets the minimum capacitance that the application requires.

### Inductor Selection

Many different sizes and shapes of inductors are available from numerous manufacturers. Choosing the right inductor from such a large selection of devices can be overwhelming, but following a few basic guidelines will make the selection process much simpler.

## APPLICATIONS INFORMATION

The buck and boost converters are designed to work with inductors over a wide range of inductances. Choosing a higher valued inductor will decrease operating frequencies, while a lower valued inductor will increase frequency but also increase peak current overshoot/undershoot. For most applications a 3.3μH inductor is recommended. To maximize efficiency, choose an inductor with a low DC resistance. Choose an inductor with a DC current rating at least as large as the maximum  $I_{PEAK}$  the application will see according to the specifications table to ensure that the inductor does not saturate during normal operation. If the single inductor application is used, make sure to size the inductor for the higher of buck or boost peak currents.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or Permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. Inductors that are very thin or have a very small volume typically have much higher core and DCR losses, and will not give the best efficiency. The choice of which style inductor to use often depends more on the price versus size, performance and any radiated EMI requirements than on what the LTC3625/LTC3625-1 family requires to operate.

Table 2 shows several inductors that work well with the LTC3625/LTC3625-1 regulators. These inductors offer a

good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

### Supercapacitor Selection

The LTC3625/LTC3625-1 are designed to charge supercapacitors of values greater than 0.1F per cell. In general, lower capacitance cells have higher ESRs, therefore lower charge currents should be used to help reduce sleep modulation towards the end of a charge cycle. In general, the ESR of a supercapacitor cell should not exceed:

$$ESR \leq \frac{100\text{mV}}{I_{BUCK}}$$

where 100mV is the sleep threshold hysteresis. Higher capacitance cells typically have lower ESRs and can therefore be charged with higher currents. Typically, the LTC3625/LTC3625-1 are designed to charge supercapacitors with values up to 100F, but higher capacitance cells could be used at the expense of greater charge time. Table 3 shows several supercapacitors that work well with the LTC3625/LTC3625-1.

### Printed Circuit Board Layout Considerations

In order to be able to deliver maximum current under all conditions, it is critical that the exposed pad on the backside of the LTC3625/LTC3625-1 package be soldered to the PC

**Table 2. Inductor Manufacturers**

MANUFACTURER	PART NUMBER	INDUCTANCE (μH)	CURRENT (A)	DCR (mΩ)	SIZE (mm)
Coiltronics	DR73-3R3-R	3.3	3.0	20	7 × 7
Coilcraft	MSS7341-332NL	3.3	3.2	20	7 × 7
Vishay	IHLM2525CZER3R3M11	3.3	6.5	26	6.5 × 6.9
Sumida	CDRH6D28P-3RON	3.0	3.0	24	7 × 7
TOKO	B1077AS-3RON	3.0	3.3	30	7.6 × 7.6

**Table 3. Supercapacitor Manufacturers**

MANUFACTURER	PART NUMBER	VALUE (F)	OPERATING VOLTAGE (V)	MAXIMUM ESR (mΩ)	SIZE (mm)
Cooper Bussmann	B1860-2R5107-R	100	2.5	20	18 × 60
Illinois Capacitor	107DCN2R7M	100	2.7	10	22 × 45
NESS Capacitor	ESHSR-0100C0002R7	100	2.7	9	22 × 45
Tecate	TPLS-100//22 X 45F	100	2.7	9	22 × 45
Maxwell	BCAP120P250	120	2.5	2.5	26 × 51

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## APPLICATIONS INFORMATION

board ground. Failure to make thermal contact between the exposed pad on the backside of the package and the copper board will result in higher thermal resistances.

Furthermore, due to its potentially high frequency switching circuitry, it is imperative that the input capacitor, inductors, and output bypass capacitors be as close to the LTC3625/LTC3625-1 as possible, and that there be an unbroken ground plane under the IC and all of its external high frequency components. High frequency currents, such as the  $V_{IN}$  and  $V_{OUT}$  currents on the LTC3625/LTC3625-1, tend to find their way along the ground plane in a myriad of paths ranging from directly back to a mirror path beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur. There should be a group of vias under the grounded backside of the package leading directly down to an internal ground plane. To minimize parasitic inductance, the ground plane should be on the highest possible layer of the PC board.

Any board resistance between inductor(s) and the positive terminal of  $C_{BOT}$  will add to the capacitors internal ESR. Likewise, any resistance between the  $V_{OUT}$  pin and the positive terminal of  $C_{TOP}$  will add to its internal ESR. Any added resistance to the capacitors will reduce the effective charging efficiency. In the case of  $C_{BOT}$  this

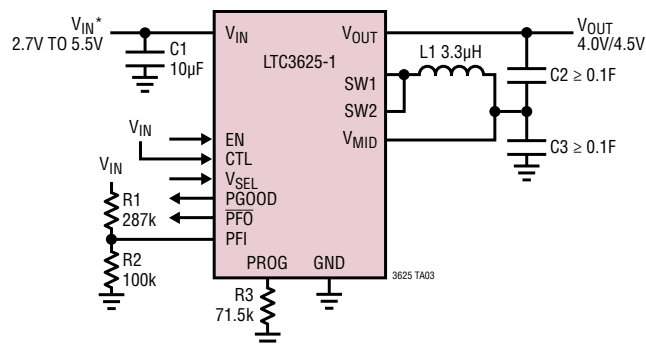
resistance can be kelvined out by a dedicated voltage sense trace from the  $V_{MID}$  pin to a point halfway between the bottom plate of  $C_{TOP}$  and the top plate of  $C_{BOT}$ . In the case of  $C_{TOP}$ , however, it is even more critical to keep any resistance in the connection to a minimum. Excessive series resistance may cause the part to duty cycle in and out of sleep or prematurely shut down the boost, due to the voltage seen at the part being equal to  $V_{OUT} + I_{OUT} \cdot ESR$ . Likewise the  $C_{BOT}$  supercapacitor should be provided with a low impedance contact to the ground plane with an unbroken, low impedance, path back to the backside of the LTC3625/LTC3625-1 package.

When laying out the printed circuit, the following checklist should be used to ensure proper operation of the LTC3625/LTC3625-1.

1. Are the bypass capacitors at  $V_{IN}$  and  $V_{OUT}$  as close as possible to the LTC3625/LTC3625-1? These capacitors provide the AC current to the internal power MOSFETs and their drivers. Minimizing inductance from these capacitors to the LTC3625/LTC3625-1 is a top priority.
2. Are the  $C_{BOT}$  bypass capacitor and the power inductor(s) closely connected? The (–) terminal of the  $C_{BOT}$  bypass capacitor returns current to the GND plane, and then back to  $C_{IN}$ .
3. Keep sensitive components away from the SW pins.
4. Keep the current carrying traces from  $V_{OUT}$  to  $C_{TOP}$  and the inductors to  $C_{BOT}$  to a minimum.

## TYPICAL APPLICATIONS

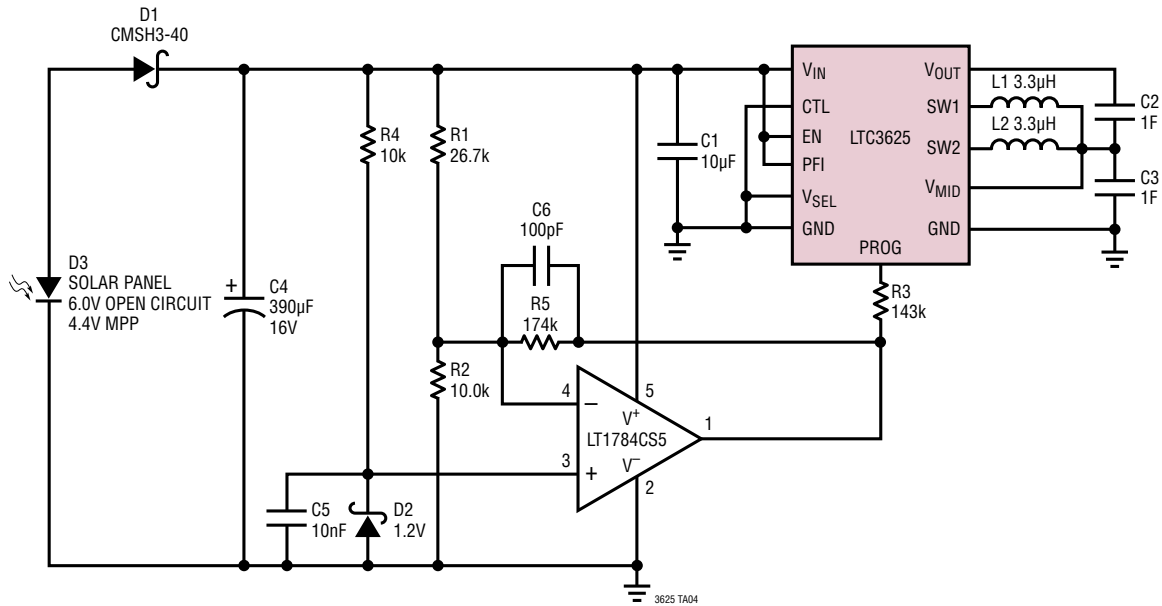
### 450mA Charge Current 1-Inductor Application



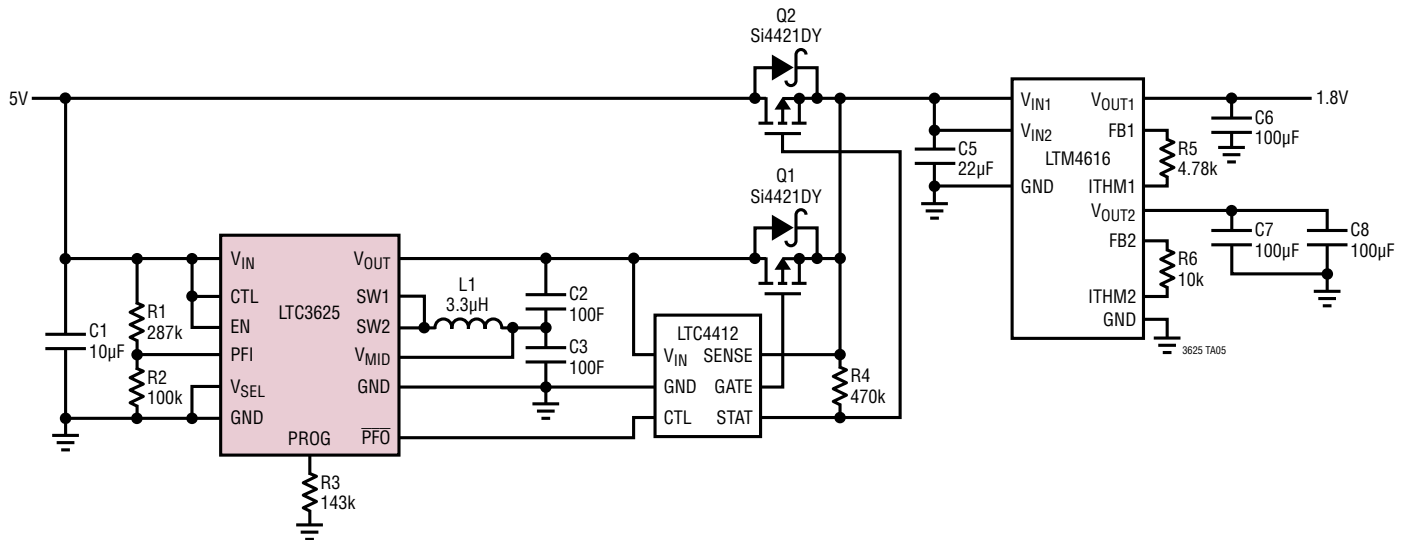
\*25mA MINIMUM LOAD REQUIRED ON  $V_{IN}$

## TYPICAL APPLICATIONS

### Solar Powered SCAP Charger with MPPT



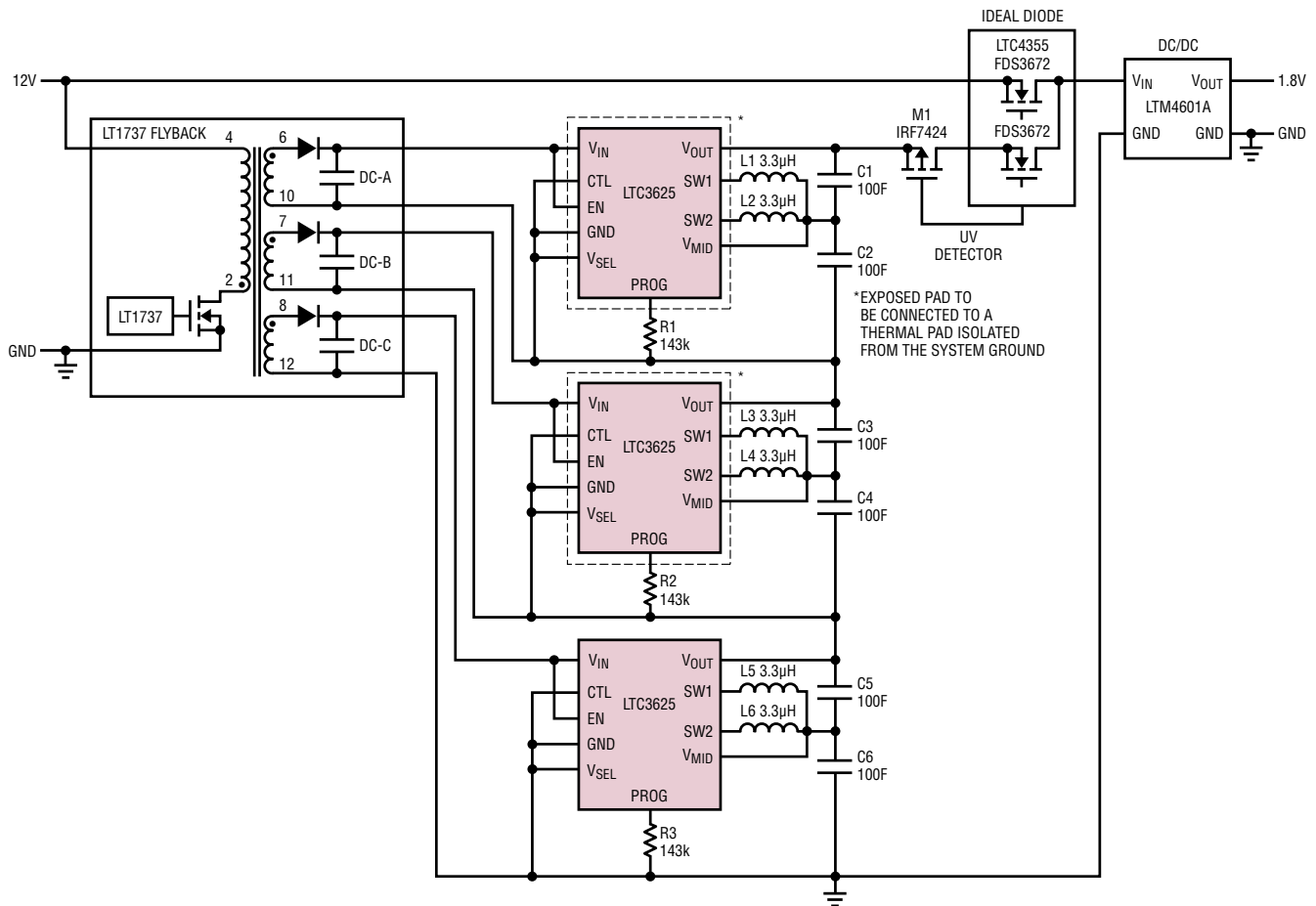
### 5V Power Ride-Through





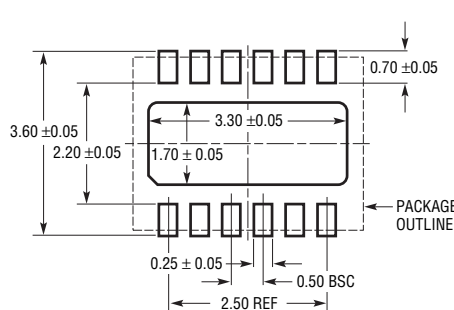
## TYPICAL APPLICATIONS

## 12V Power Ride-Through

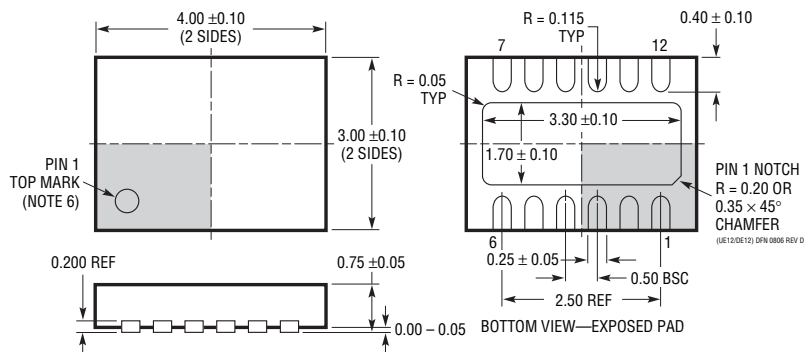


## PACKAGE DESCRIPTION

**DE Package**  
**12-Lead Plastic DFN (4mm × 3mm)**  
 (Reference LTC DWG # 05-08-1695)



NOTE:  
 1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE MO-229  
 2. DRAWING NOT TO SCALE  
 3. ALL DIMENSIONS ARE IN MILLIMETERS



3. ALL DIMENSIONS ARE IN MILLIMETERS  
 4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE  
 5. EXPOSED PAD SHALL BE SOLDER PLATED  
 6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## TYPICAL APPLICATION

## RELATED PARTS

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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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