Single Supply, High Speed, Rail-to-Rail Output, Triple Op Amp

Data Sheet

ADA4855-3

FEATURES

- Voltage feedback architecture
- Rail-to-rail output swing: 0.1 V to 4.9 V
- High speed amplifiers
  - 410 MHz, −3 dB bandwidth, G = 1
  - 210 MHz, −3 dB bandwidth, G = 2
  - Slew rate: 870 V/µs
  - 53 MHz, 0.1 dB large signal flatness
  - 5.3 ns settling time to 0.1% with 2 V step
- High input common-mode voltage range
  - $-V_S - 0.2$ V to $+V_S - 1$ V
- Supply range: 3 V to 5.5 V
- Differential gain error: 0.01%
- Differential phase error: 0.01°
- Low power
  - 7.8 mA/amplifier typical supply current
  - Power-down feature
- Available in 16-lead LFCSP

APPLICATIONS

- Professional video
- Consumer video
- Imaging
- Instrumentation
- Base stations
- Active filters

CONNECTION DIAGRAM

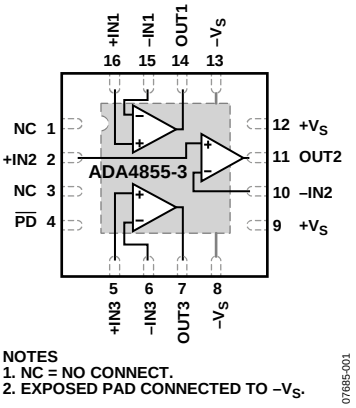

Figure 1.

GENERAL DESCRIPTION

The ADA4855-3 (triple) is a single-supply, rail-to-rail output operational amplifier. It provides excellent high speed performance with 410 MHz, −3 dB bandwidth and a slew rate of 870 V/µs. It has a wide input common-mode voltage range that extends from 0.2 V below ground to 1 V below the positive rail.In addition, the output voltage swings within 100 mV of either supply rail, making this rail-to-rail operational amplifier easy to use on single-supply voltages as low as 3.3 V.

The ADA4855-3 offers a typical low power of 7.8 mA per amplifier and is capable of delivering up to 57 mA of load current. It also features a power-down function for power sensitive applications that reduces the supply current down to 1 mA.

The ADA4855-3 is available in a 16-lead LFCSP and is designed to work over the extended industrial temperature range of −40°C to +105°C.

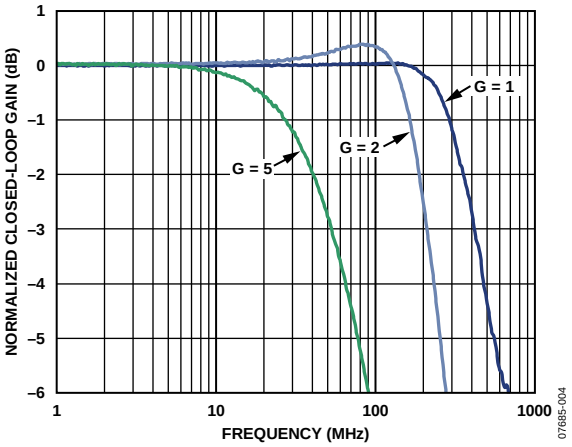

Figure 2. Frequency Response

Rev. A
Document Feedback

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11/08—Revision 0: Initial Version

SPECIFICATIONS

5 V OPERATION

T_A = 25°C, V_S = 5 V, G = 1, R_L = 150 Ω, unless otherwise noted.

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.1 V p-p		410		MHz
	V_O = 2 V p-p		200		MHz
	V_O = 0.1 V p-p, G = 2		210		MHz
	V_O = 2 V p-p, G = 2		120		MHz
Bandwidth for 0.1 dB Flatness	V_O = 2 V p-p		53		MHz
	V_O = 2 V p-p, G = 2		50		MHz
Slew Rate	V_O = 2 V step		870		V/µs
Settling Time to 0.1%	V_O = 2 V step (rise/fall)		5.3/9.5		ns
	V_O = 2 V step (rise/fall), G = 2		7.4/7		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion (HD2/HD3)	f_C = 5 MHz, V_O = 2 V p-p, R_L = 1 kΩ		−84/−105		dBc
	f_C = 20 MHz, V_O = 2 V p-p, R_L = 1 kΩ		−60/−66		dBc
Crosstalk, Output to Output	f = 5 MHz, G = 2		−90		dBc
Input Voltage Noise	f = 100 kHz		6.8		nV/√Hz
Input Current Noise	f = 100 kHz		2		pA/√Hz
Differential Gain Error	G = 2		0.01		%
Differential Phase Error	G = 2		0.01		Degrees
DC PERFORMANCE					
Input Offset Voltage			1.3	3	mV
Input Offset Voltage Drift			5.5		µV/°C
Input Bias Current			−3.8		µA
Input Offset Current			±0.05		µA
Open-Loop Gain	V_O = 0.5 V to 4.5 V		92		dB
INPUT CHARACTERISTICS					
Input Resistance			6.4		MΩ
Input Capacitance			0.5		pF
Input Common-Mode Voltage Range		$-V_S$ − 0.2		$+V_S$ − 1	V
Common-Mode Rejection Ratio	V_{CM} = −0.2 V to +4 V		94		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing			0.1 to 4.9		V
Linear Output Current per Amplifier	HD2 ≤ −60 dBc, R_L = 10 Ω		57		mA
POWER-DOWN					
Turn-On Time			78		ns
Turn-Off Time			1.2		µs
Bias Current	On		0.3		µA
	Off		−125		µA
Turn-On Voltage			$+V_S$ − 1.25		V
POWER SUPPLY					
Operating Range		3		5.5	V
Quiescent Current per Amplifier			7.8		mA
Supply Current When Powered Down			1.1		mA
Power Supply Rejection Ratio	ΔV_S = 4.5 V to 5.5 V		96		dB

3.3 V OPERATION

T_A = 25°C, V_S = 3.3 V, G = 1, R_L = 150 Ω, unless otherwise noted.

Table 2.

Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.1 V p-p		430		MHz
	V_O = 1.4 V p-p		210		MHz
	V_O = 0.1 V p-p, G = 2		210		MHz
	V_O = 2 V p-p, G = 2		125		MHz
Bandwidth for 0.1 dB Flatness	V_O = 1.4 V p-p, G = 2		55		MHz
Slew Rate	V_O = 2 V step, G = 2		870		V/µs
Settling Time to 0.1%	V_O = 2 V step (rise/fall), G = 2		7.4/7.1		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion (HD2/HD3)	f_C = 5 MHz, V_O = 2 V p-p, R_L = 1 kΩ		−76/−76		dBc
	f_C = 20 MHz, V_O = 2 V p-p, R_L = 1 kΩ		−68/−75		dBc
Crosstalk, Output to Output	f = 5 MHz, G = 2		−88		dBc
Input Voltage Noise	f = 100 kHz		6.8		nV/√Hz
Input Current Noise	f = 100 kHz		2		pA/√Hz
Differential Gain Error	G = 2		0.01		%
Differential Phase Error	G = 2		0.01		Degrees
DC PERFORMANCE					
Input Offset Voltage			1.3		mV
Input Offset Voltage Drift			5.5		µV/°C
Input Bias Current			−3.8		µA
Input Offset Current			0.05		µA
Open-Loop Gain	V_O = 0.5 V to 4.5 V		92		dB
INPUT CHARACTERISTICS					
Input Resistance			6.4		MΩ
Input Capacitance			0.5		pF
Input Common-Mode Voltage Range		$-V_S$ − 0.2		$+V_S$ − 1	V
Common-Mode Rejection Ratio	V_{CM} = −0.2 V to +3.2 V		94		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing			0.1 to 3.22		V
Linear Output Current per Amplifier	HD2 ≤ −60 dBc, R_L = 10 Ω		40		mA
POWER-DOWN					
Turn-On Time			78		ns
Turn-Off Time			1.2		µs
Turn-On Voltage			$+V_S$ − 1.25		V
POWER SUPPLY					
Operating Range		3		5.5	V
Quiescent Current per Amplifier			7.5		mA
Supply Current When Powered Down			0.95		mA
Power Supply Rejection Ratio	ΔV_S = 2.97 V to 3.63 V		94		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Internal Power Dissipation[1]	See Figure 3
Common-Mode Input Voltage	($-V_S$ – 0.2 V) to ($+V_S$ – 1 V)
Differential Input Voltage	$\pm V_S$
Output Short-Circuit Duration	Observe power curves
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Specification is for device in free air.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead LFCSP	67	17.5	°C/W

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the ADA4855-3 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

To ensure proper operation, it is necessary to observe the maximum power derating curves.

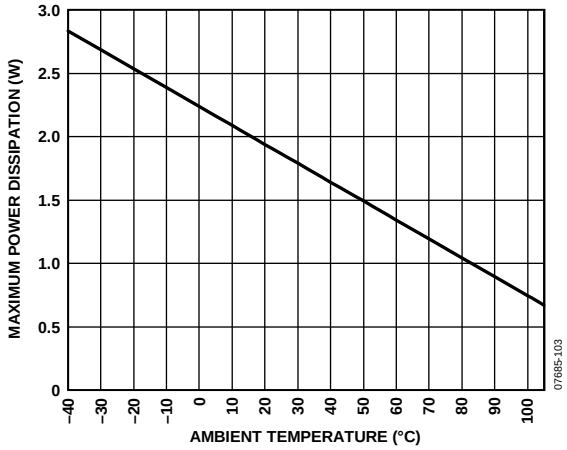

Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

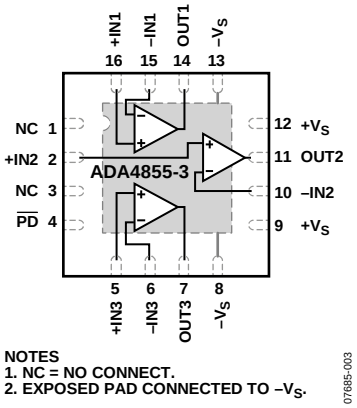

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect.
2	+IN2	Noninverting Input 2.
3	NC	No Connect.
4	$\overline{PD}$	Power Down.
5	+IN3	Noninverting Input 3.
6	−IN3	Inverting Input 3.
7	OUT3	Output 3.
8	$-V_S$	Negative Supply.
9	$+V_S$	Positive Supply.
10	−IN2	Inverting Input 2.
11	OUT2	Output 2.
12	$+V_S$	Positive Supply.
13	$-V_S$	Negative Supply.
14	OUT1	Output 1.
15	−IN1	Inverting Input 1.
16	+IN1	Noninverting Input 1.
17 (EPAD)	Exposed Pad (EPAD)	The exposed pad must be connected to $-V_S$.

TYPICAL PERFORMANCE CHARACTERISTICS

T = 25°C, V_S = 5V, G = 1, R_F = 1 kΩ for G > 1, R_L = 150 Ω, small signal V_{OUT} = 100 mV p-p, and large signal V_{OUT} = 2 V p-p, unless otherwise noted.

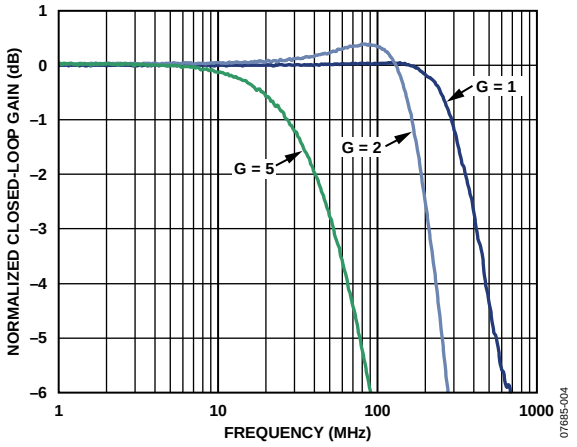

Figure 5. Small Signal Frequency Response vs. Gain

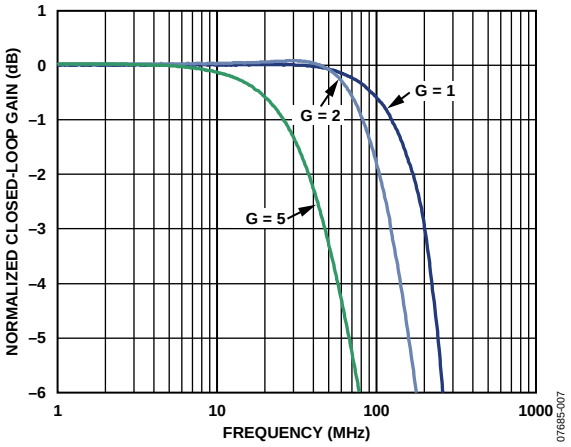

Figure 8. Large Signal Frequency Response vs. Gain

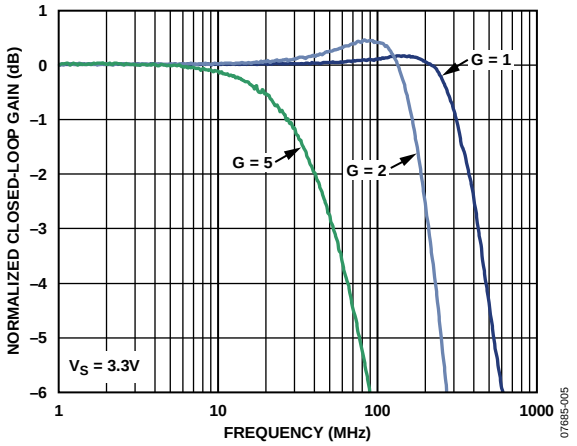

Figure 6. Small Signal Frequency Response vs. Gain

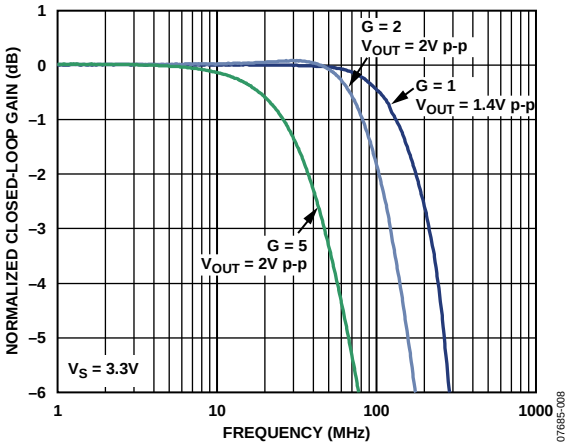

Figure 9. Large Signal Frequency Response vs. Gain

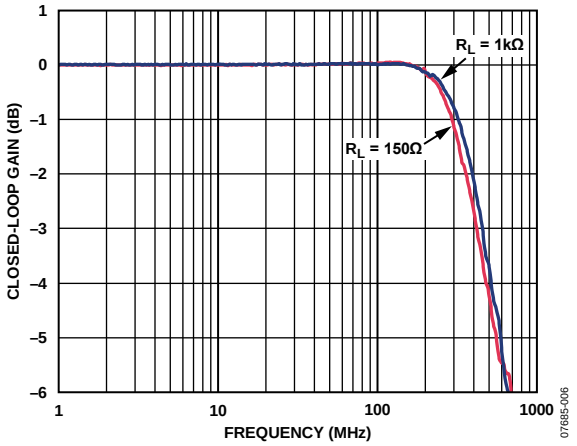

Figure 7. Small Signal Frequency Response vs. Load

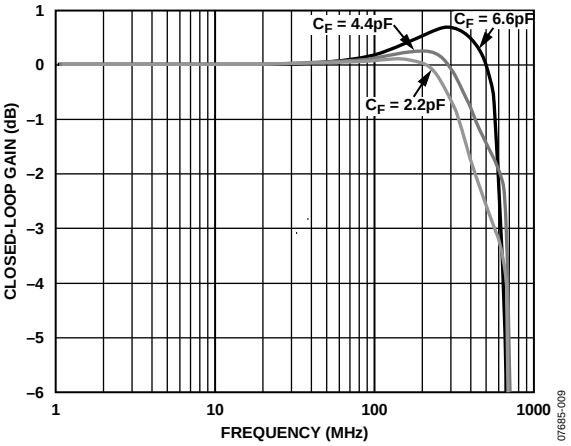

Figure 10. Small Signal Frequency Response vs. Capacitive Load

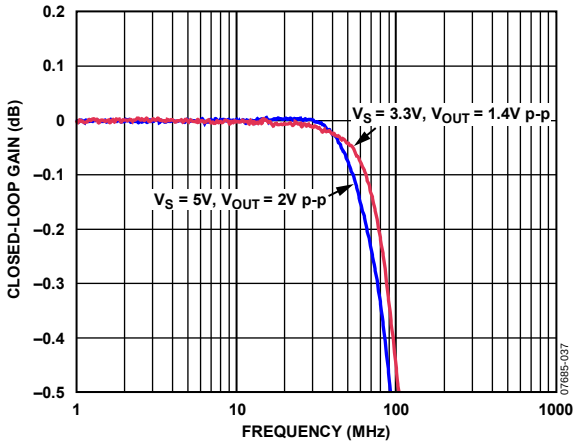

Figure 11. 0.1 dB Flatness vs. Supply Voltage

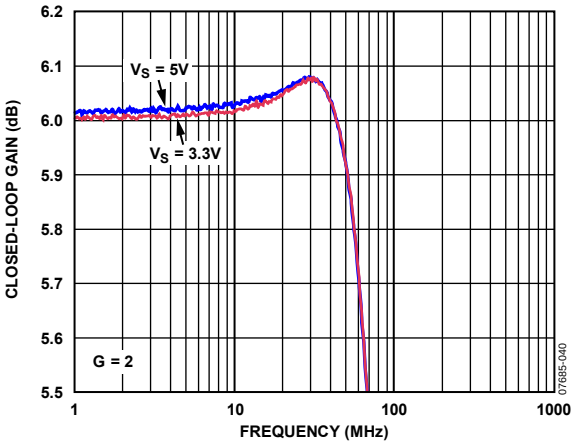

Figure 14. 0.1 dB Flatness vs. Supply Voltage

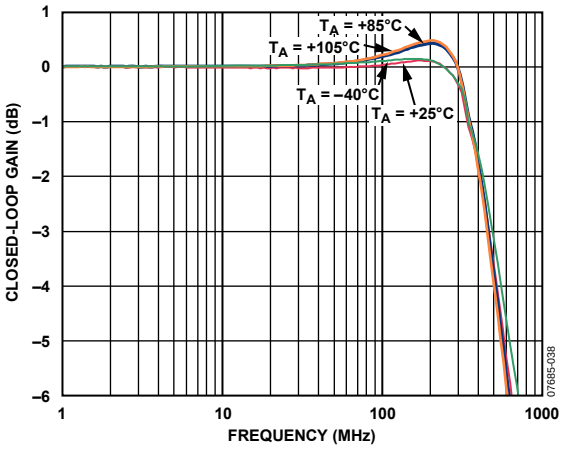

Figure 12. Small Signal Frequency Response vs. Temperature

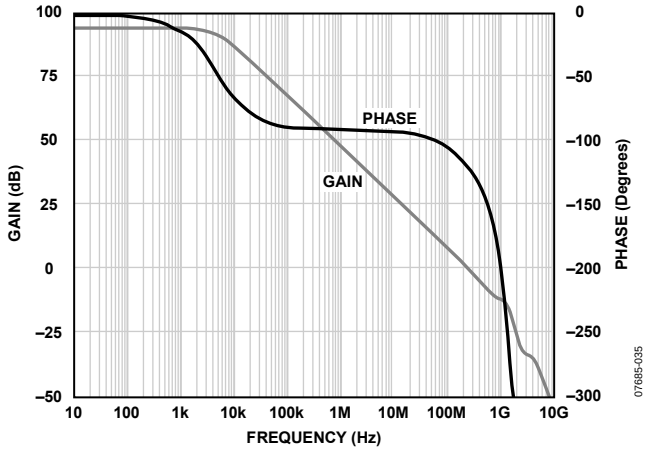

Figure 15. Open-Loop Gain and Phase vs. Frequency

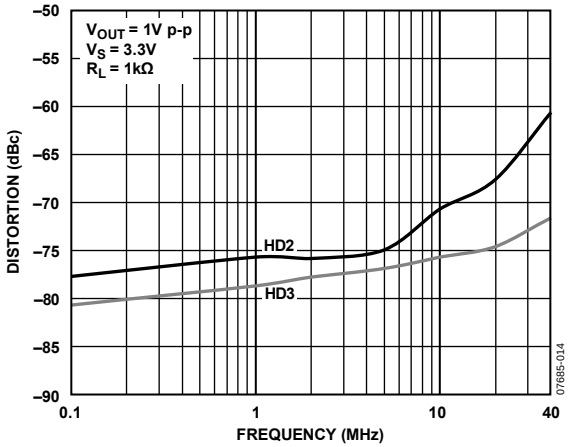

Figure 13. Harmonic Distortion vs. Frequency

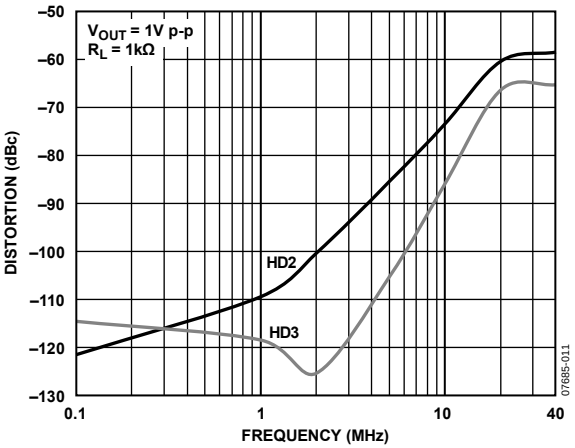

Figure 16. Harmonic Distortion vs. Frequency

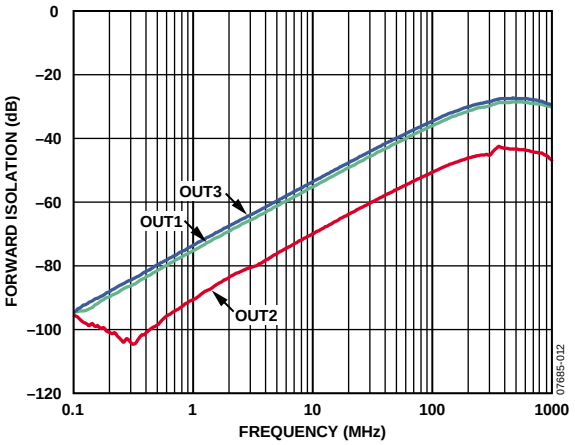

Figure 17. Forward Isolation vs. Frequency

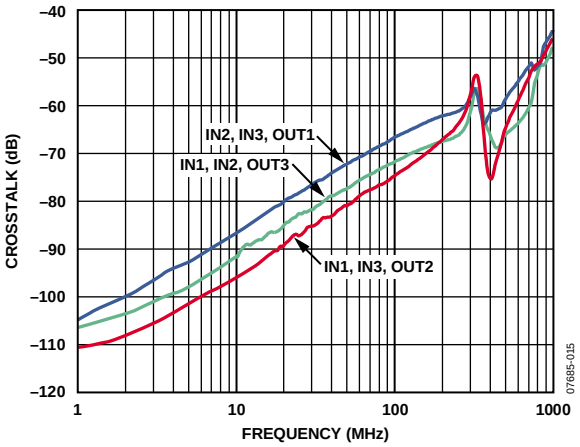

Figure 20. Crosstalk vs. Frequency

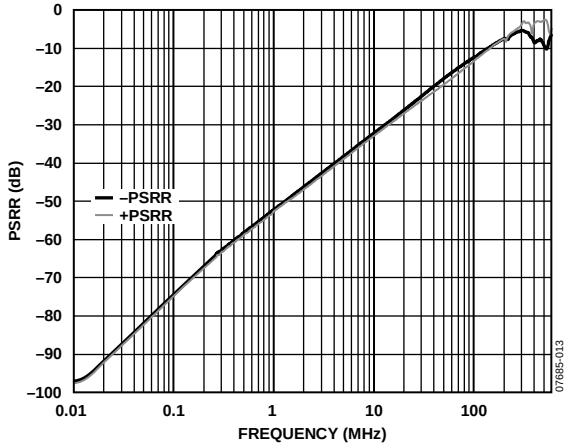

Figure 18. Power Supply Rejection Ratio (PSRR) vs. Frequency

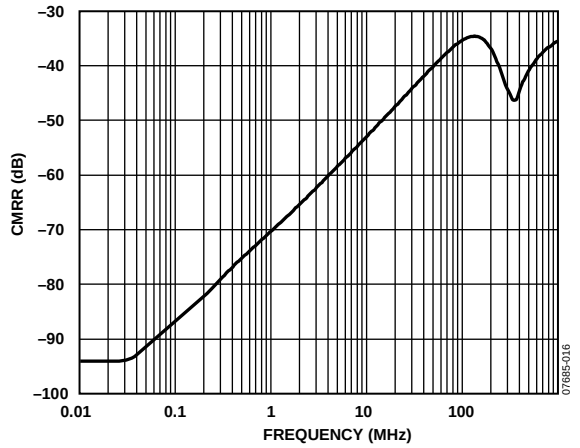

Figure 21. Common-Mode Rejection Ratio (CMRR) vs. Frequency

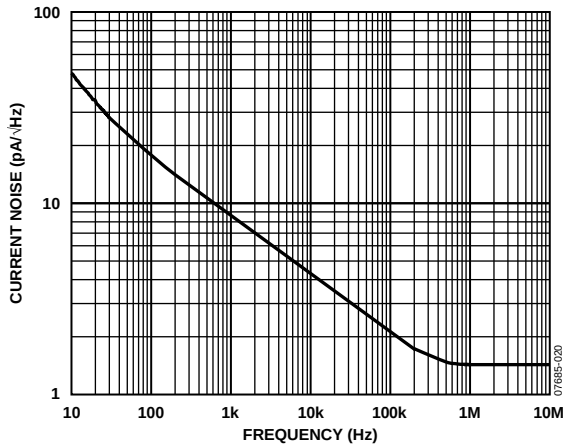

Figure 19. Input Current Noise vs. Frequency

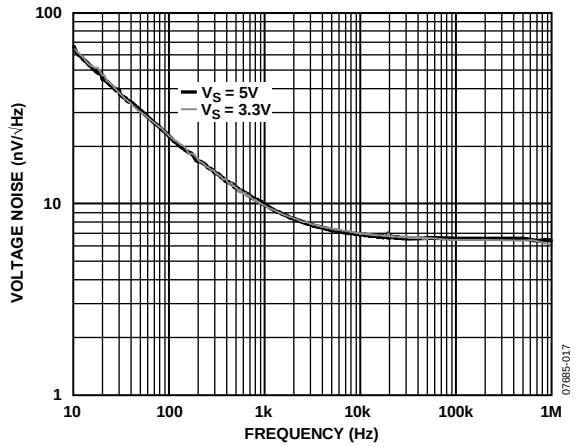

Figure 22. Input Voltage Noise vs. Frequency

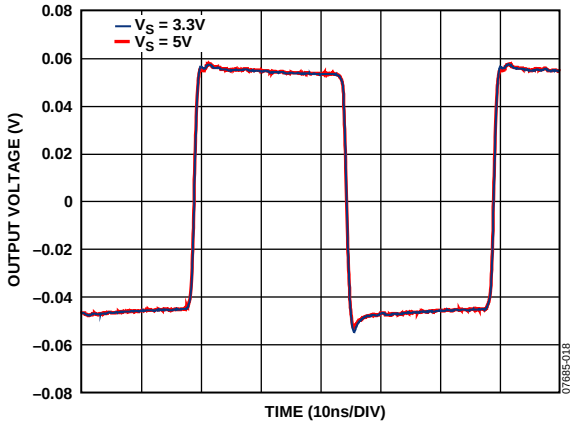

Figure 23. Small Signal Transient Response vs. Supply Voltage

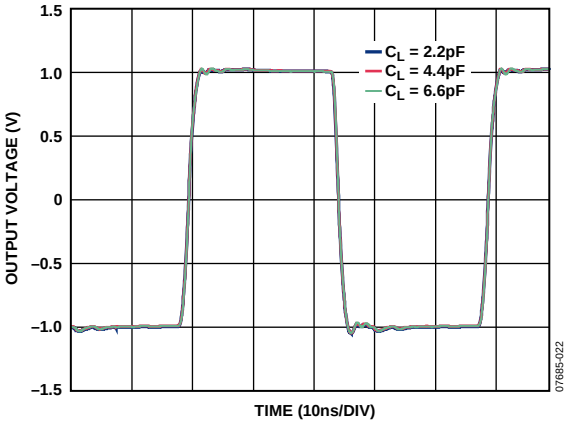

Figure 26. Large Signal Transient Response vs. Capacitive Load

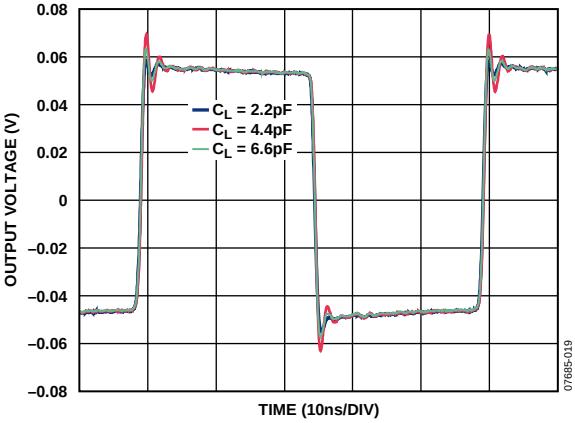

Figure 24. Small Signal Transient Response vs. Capacitive Load

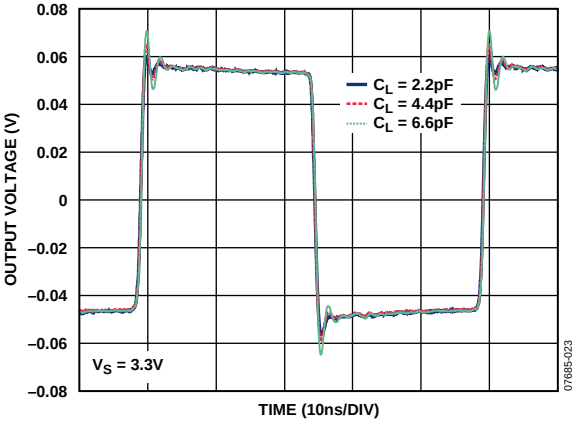

Figure 27. Small Signal Transient Response vs. Capacitive Load

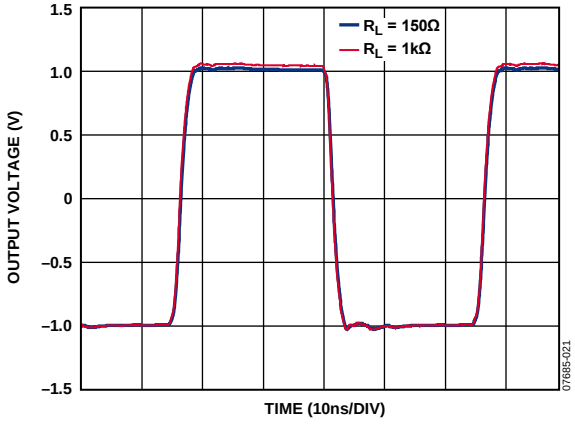

Figure 25. Large Signal Transient Response vs. Load Resistance

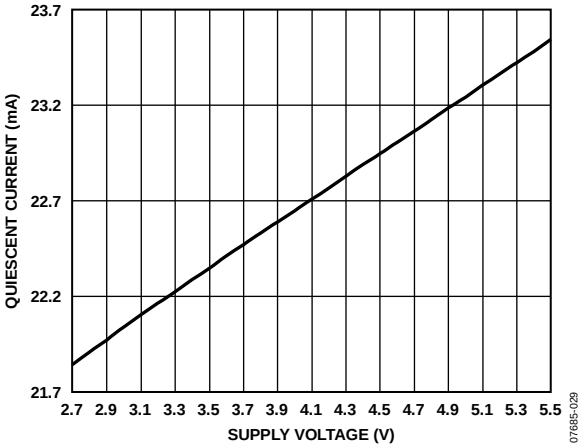

Figure 28. Quiescent Current vs. Supply Voltage

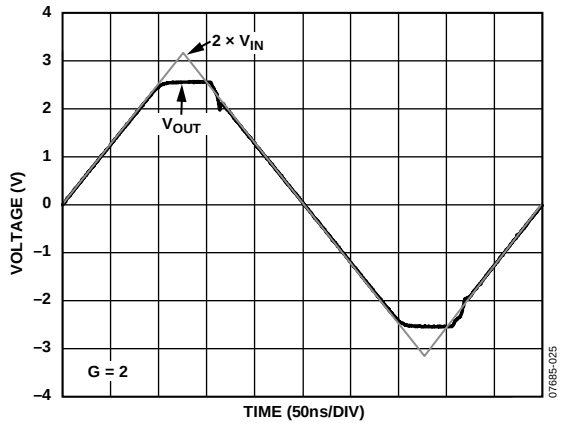

Figure 29. Output Overdrive Recovery

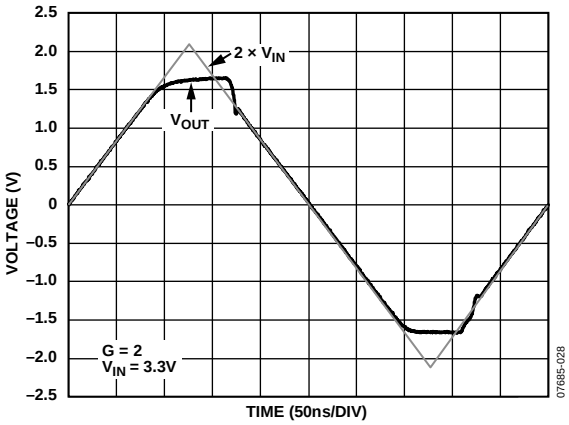

Figure 32. Output Overdrive Recovery

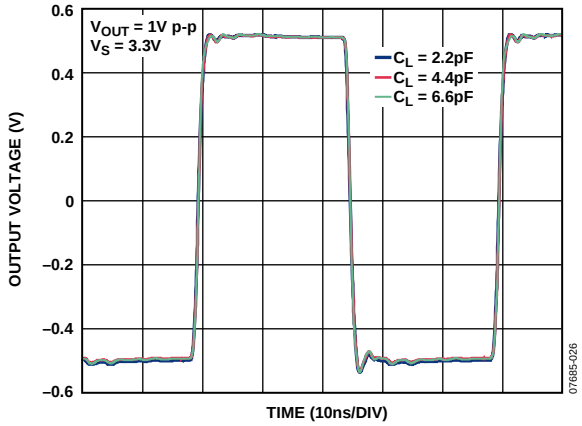

Figure 30. Large Signal Transient Response vs. Capacitive Load

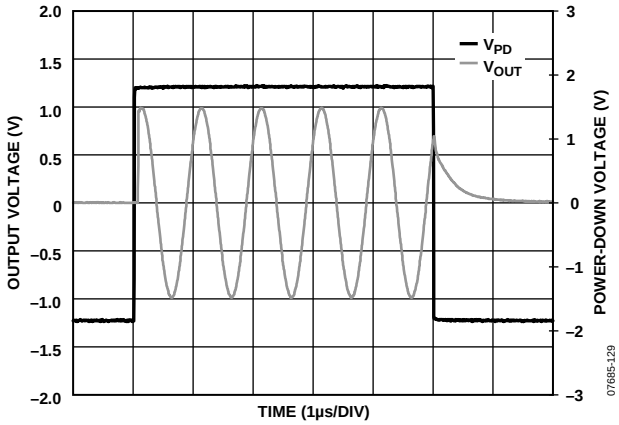

Figure 33. Turn-On/Turn-Off Time

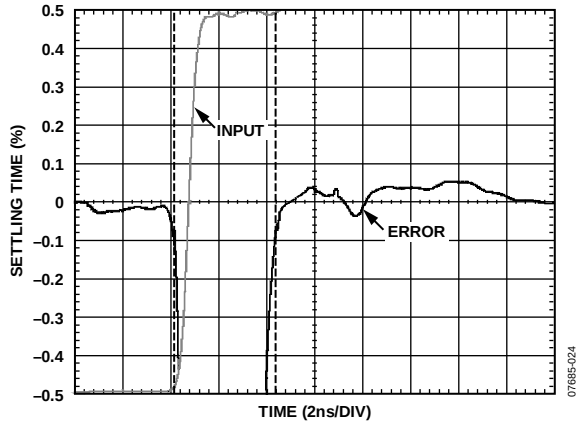

Figure 31. Settling Time

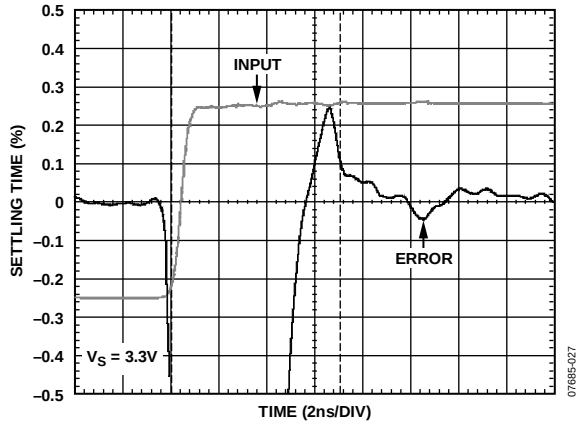

Figure 34. Settling Time

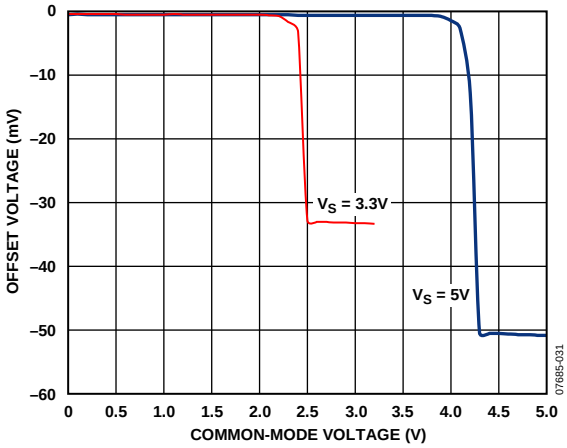

Figure 35. Input Offset Voltage vs. Common-Mode Voltage

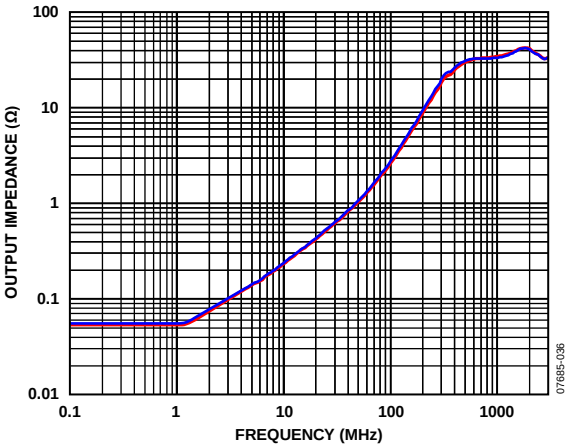

Figure 38. Output Impedance vs. Frequency

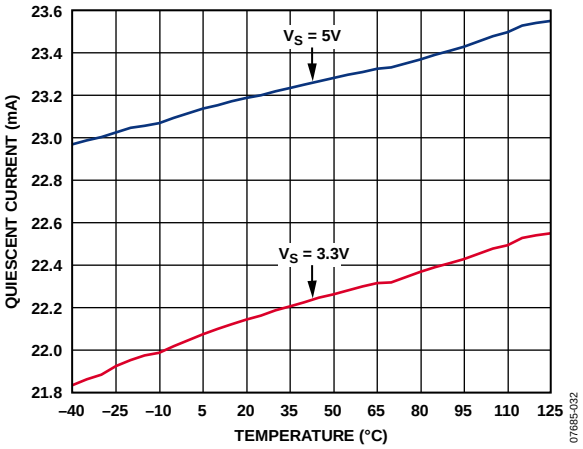

Figure 36. Quiescent Current vs. Temperature

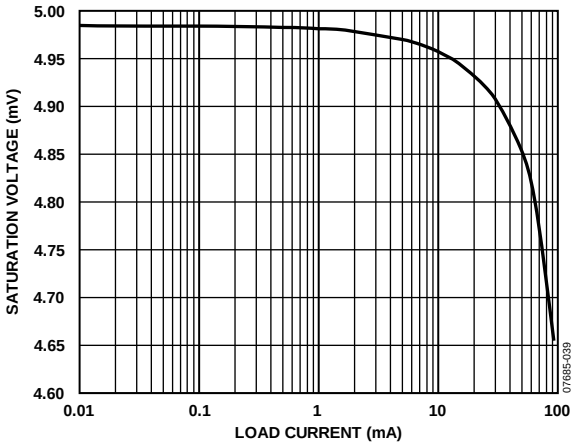

Figure 39. Output Saturation Voltage vs. Load Current

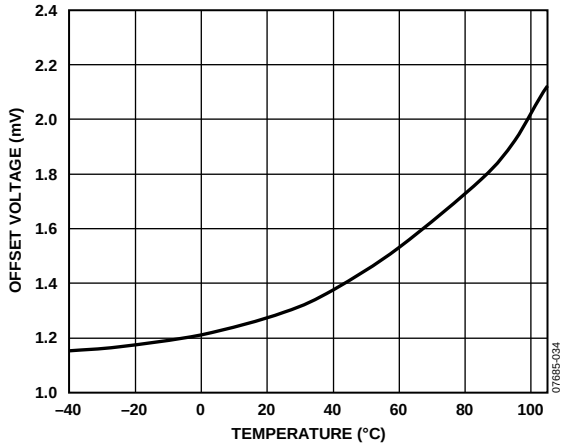

Figure 37. Offset Drift vs. Temperature

TEST CIRCUITS

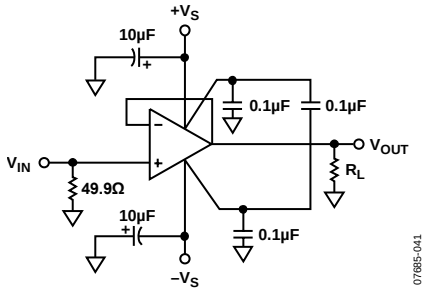

Figure 40. Noninverting Load Configuration

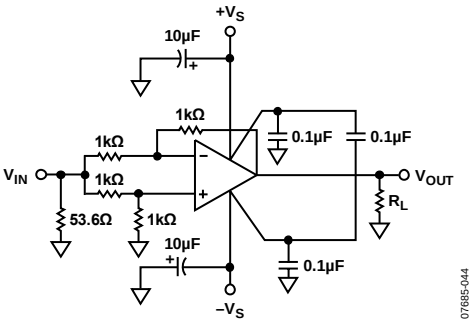

Figure 43. Common-Mode Rejection

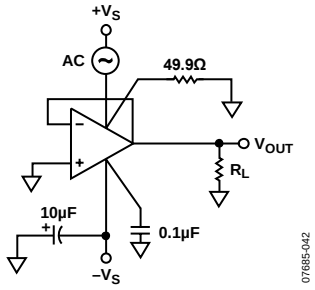

Figure 41. Positive Power Supply Rejection

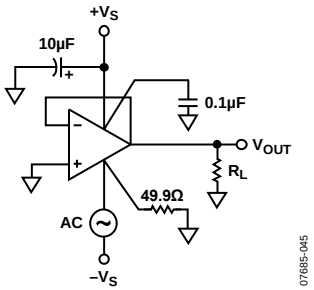

Figure 44. Negative Power Supply Rejection

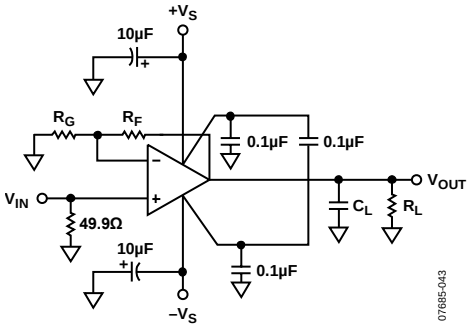

Figure 42. Typical Capacitive Load Configuration

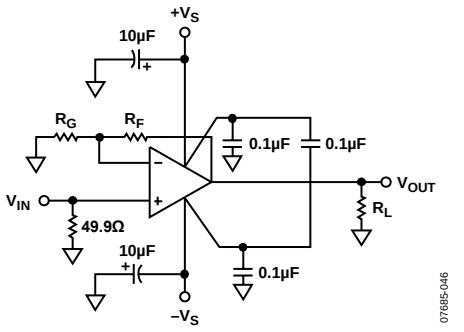

Figure 45. Typical Noninverting Gain Configuration

THEORY OF OPERATION

The ADA4855-3 is a voltage feedback op amp that employs a new input stage that achieves a high slew rate while maintaining a wide common-mode input range. The input common-mode range of the ADA4855-3 extends from 200 mV below the negative rail to 1 V below the positive rail. This feature makes the ADA4855-3 ideal for single-supply applications. In addition, this new input stage does not sacrifice noise performance for slew rate. At 6.8 nV/√Hz, the ADA4855-3 is one of the lowest noise rail-to-rail output video amplifiers in the market.

Besides a novel input stage, the ADA4855-3 employs the Analog Devices, Inc., patented rail-to-rail output stage. This output stage makes efficient use of the power supplies, allowing the op amp to drive up to three video loads to within 350 mV of the positive power rail. In addition, this output stage provides the amplifier with very fast overdrive characteristics, which is an important property in video applications.

The ADA4855-3 comes in a 16-lead LFCSP that has an exposed thermal pad for lower operating temperature. This pad is internally connected to the negative rail. To avoid printed circuit board (PCB) layout problems, the ADA4855-3 features a new pinout flow that is optimized for video applications. As shown in Figure 4, the noninverting input and output pins of each amplifier are adjacent to each other for ease of layout.

The ADA4855-3 is fabricated in Analog Devices dielectrically isolated eXtra Fast Complementary Bipolar 3 (XFCB3) process, which results in the outstanding speed and dynamic range displayed by the amplifier.

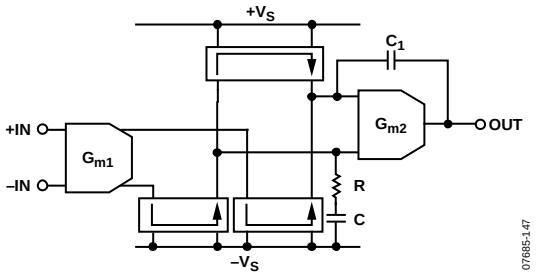

Figure 46. High Level Design Schematic

APPLICATIONS INFORMATION

GAIN CONFIGURATIONS

The ADA4855-3 is a single-supply, high speed, voltage feedback amplifier. Table 6 provides a convenient reference for quickly determining the feedback and gain set resistor values and bandwidth for common gain configurations.

Table 6. Recommended Values and Frequency Performance[1]

Gain	R_F	R_G	−3 dB SS BW (MHz)	Large Signal 0.1 dB Flatness (MHz)
1	0 Ω	N/A	200	53
2	1 kΩ	1 kΩ	120	50
5	1 kΩ	200 Ω	45	6

[1] Conditions: V_S = 5 V, T_A = 25°C, R_L = 150 Ω.

Figure 47 and Figure 48 show the typical noninverting and inverting configurations and recommended bypass capacitor values.

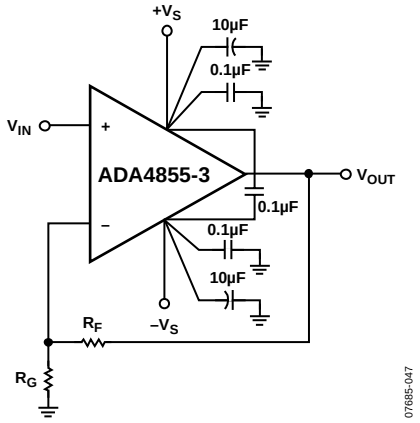

Figure 47. Noninverting Gain Configuration

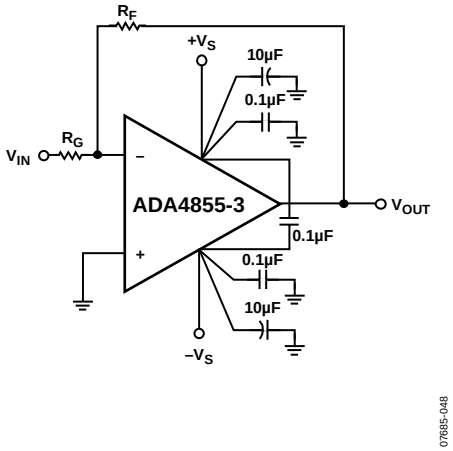

Figure 48. Inverting Gain Configuration

20 MHz ACTIVE LOW-PASS FILTER

The ADA4855-3 triple amplifier lends itself to higher order active filters. Figure 49 shows a 20 MHz, 6-pole, Sallen-Key low-pass filter.

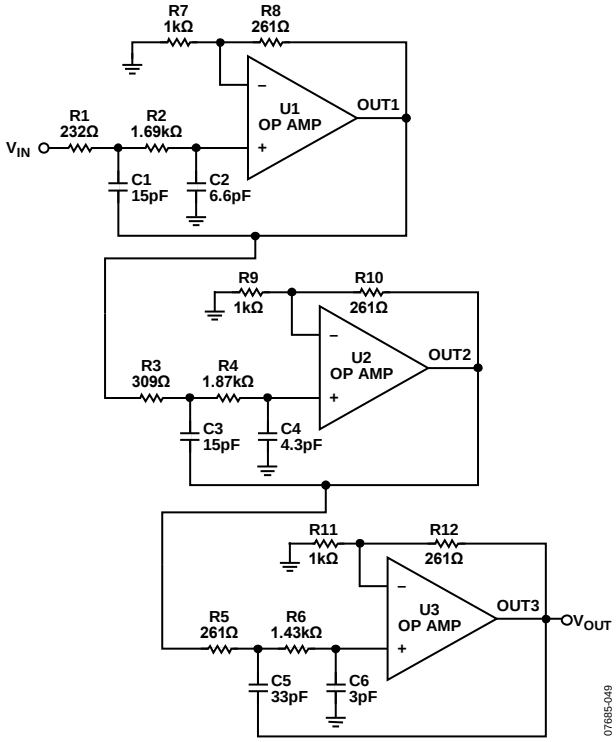

Figure 49. 20 MHz, 6-Pole Low-Pass Filter

The filter has a gain of approximately 6 dB and flat frequency response out to 14 MHz. This type of filter is commonly used at the output of a video DAC as a reconstruction filter. The frequency response of the filter is shown in Figure 50.

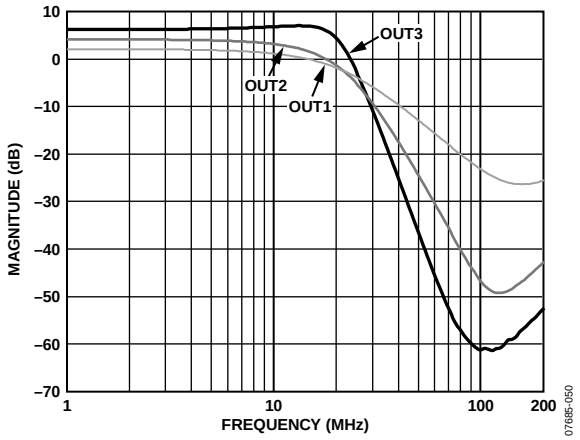

Figure 50. 20 MHz, Low-Pass Filter Frequency Response

RGB VIDEO DRIVER

Figure 51 shows a typical RGB driver application using dual supplies. The gain of the amplifier is set at +2, where $R_F = R_G = 1$ kΩ. The amplifier inputs are terminated with shunt 75 Ω resistors, and the outputs have series 75 Ω resistors for proper video matching. In Figure 51, the $\overline{PD}$ pin is not shown connected to any signal source for simplicity. If the power-down function is not used, it is recommended that the $\overline{PD}$ pin be tied to the positive supply or be left floating (not connected).

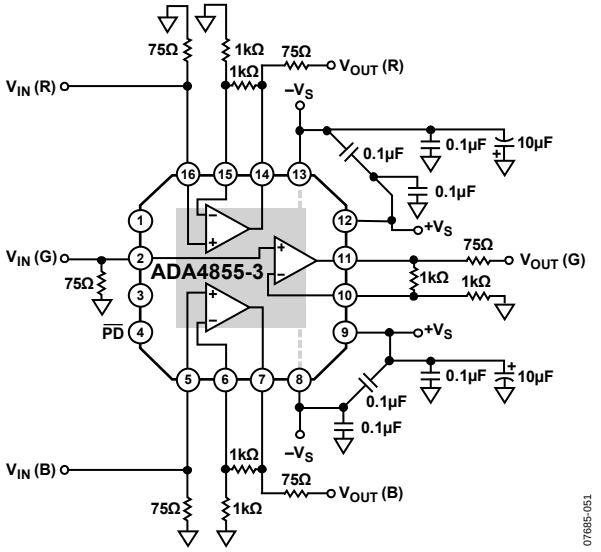

Figure 51. RGB Video Driver

DRIVING MULTIPLE VIDEO LOADS

Each amplifier in the ADA4855-3 can drive up to three video loads simultaneously, as shown in Figure 52. When driving three video loads, the ADA4855-3 maintains its excellent performance for 0.1 dB flatness and 3 dB bandwidth. Figure 53 shows the large signal frequency response of the ADA4855-3 with three different load configurations: 150 Ω, 75 Ω and 50 Ω.

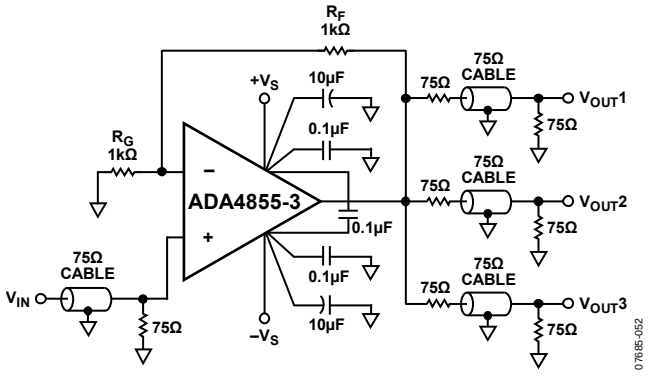

Figure 52. Video Driver Schematic for Triple Video Loads

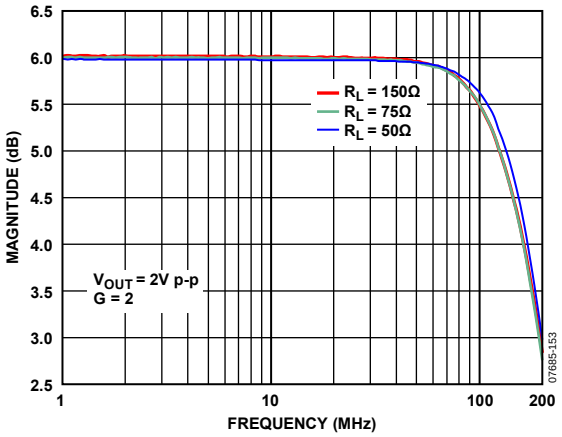

Figure 53. Large Signal Frequency Response vs. Loads

$\overline{PD}$ (POWER-DOWN) PIN

The ADA4855-3 is equipped with a $\overline{PD}$ (power-down) pin for all three amplifiers. This allows the user to reduce the quiescent supply current when an amplifier is inactive. The power-down threshold levels are derived from the voltage applied to the $+V_S$ pin. When used in single-supply applications, this is especially useful with conventional logic levels. The amplifier is enabled when the voltage applied to the $\overline{PD}$ pin is greater than $+V_S - 1.25$ V. In a single-supply application, the voltage threshold is typically +3.75 V, and in a ±2.5 V dual-supply application, the voltage threshold is typically +1.25 V. The amplifier is also enabled when the $\overline{PD}$ pin is left floating (not connected). However, the amplifier is powered down when the voltage on the $\overline{PD}$ pin is lower than 2.5 V from $+V_S$. If the $\overline{PD}$ pin is not used, it is best to connect it to the positive supply.

Table 7. Power-Down Voltage Control

$\overline{PD}$ Pin	5 V	±2.5 V	3 V
Not Active	>3.75 V	>1.25 V	>1.75 V
Active	<2 V	<0 V	<1 V

SINGLE-SUPPLY OPERATION

The ADA4855-3 is designed for a single power supply. Figure 54 shows the schematic for a single 5 V supply video driver. The input signal is ac-coupled into the amplifier via C1. Resistor R2 and Resistor R4 establish the input midsupply reference for the amplifier. C5 prevents constant current from being drawn through the gain set resistor. C6 is the output coupling capacitor. For more information on ac-coupled single-supply operation of op amps, see *Avoiding Op-Amp Instability Problems in Single-Supply Applications*, Analog Dialogue, Volume 35, Number 2, March-May, 2001, at www.analog.com.

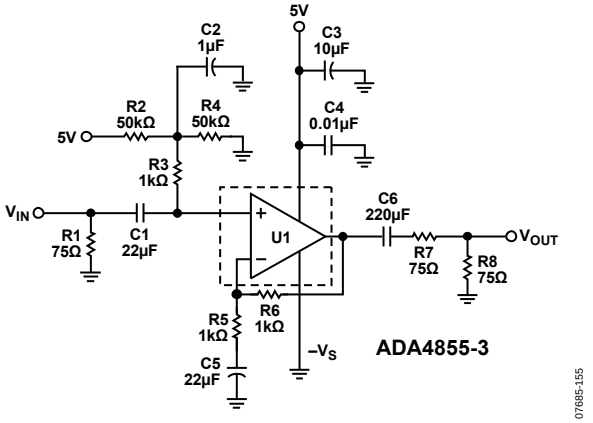

Figure 54. AC-Coupled, Single-Supply Video Driver Schematic

Another way to configure the ADA4855-3 in single-supply operation is dc-coupled. The common-mode input voltage can go ~200 mV below ground, which makes it a true single-supply amplifier. However, in video applications, the black level is set at 0 V, which means that the output of the amplifier must go to ground level as well. The ADA4855-3 has a rail-to-rail output that can swing to within 100 mV from either rail. Figure 55 shows the schematic for adding 50 mV dc offset to the input signal so that the output is not clipped while still properly terminating the input with 75 Ω.

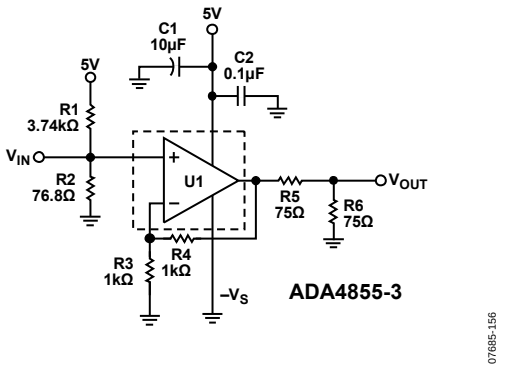

Figure 55. DC-Coupled, Single-Supply Video Driver Schematic

POWER SUPPLY BYPASSING

Careful attention must be paid to bypassing the power supply pins of the ADA4855-3. High quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), should be used to minimize supply voltage ripple and power dissipation. A large, usually tantalum, 2.2 µF to 47 µF capacitor located in close proximity to the ADA4855-3 is required to provide good decoupling for lower frequency signals. The actual value is determined by the circuit transient and frequency requirements. In addition, 0.1 µF MLCC decoupling capacitors should be located as close to each of the power supply pins and across both supplies as is physically possible, no more than 1/8-inch away. The ground returns should terminate immediately into the ground plane. Locating the bypass capacitor return close to the load return minimizes ground loops and improves performance.

LAYOUT

As is the case with all high speed applications, careful attention to printed circuit board (PCB) layout details prevents associated board parasitics from becoming problematic. The ADA4855-3 can operate at up to 410 MHz; therefore, proper RF design techniques must be employed. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance return path. Removing the ground plane on all layers from the area near and under the input and output pins reduces stray capacitance. Signal lines connecting the feedback and gain resistors should be kept as short as possible to minimize the inductance and stray capacitance associated with these traces. Termination resistors and loads should be located as close as possible to their respective inputs and outputs. Input and output traces should be kept as far apart as possible to minimize coupling (crosstalk) through the board. Adherence to microstrip or stripline design techniques for long signal traces (greater than 1 inch) is recommended. For more information on high speed board layout, see *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, Analog Dialogue, Volume 39, September 2005, at www.analog.com.

OUTLINE DIMENSIONS

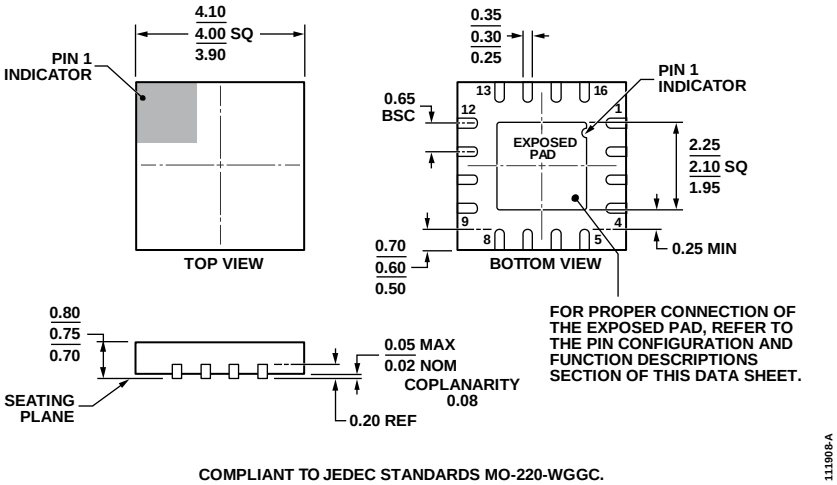

Figure 56.16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADA4855-3YCPZ-R2	−40°C to +105°C	16-Lead LFCSP_WQ	CP-16-23	250
ADA4855-3YCPZ-R7	−40°C to +105°C	16-Lead LFCSP_WQ	CP-16-23	1,500
ADA4855-3YCPZ-RL	−40°C to +105°C	16-Lead LFCSP_WQ	CP-16-23	5,000
ADA4855-3YCP-EBZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D07685-0-2/13(A)

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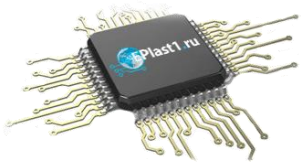
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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