MIC2125/6

28V Synchronous Buck Controllers Featuring Adaptive ON-Time Control

Features

- Hyper Speed Control Architecture Enables:
  - High delta V operation (V_{IN} = 28V and V_{OUT} = 0.6V)
  - Any Capacitor™ stable
- 4.5V to 28V Input Voltage
- Adjustable Output Voltage from 0.6V to 24V
- 200 kHz to 750 kHz Programmable Switching Frequency
- HyperLight Load® (MIC2125)
- Hyper Speed Control® (MIC2126)
- Enable Input and Power Good Output
- Built-in 5V Regulator for Single-Supply Operation
- Programmable current limit and "hiccup" mode short-circuit protection
- 7 ms internal soft-start, internal compensation, and thermal shutdown
- Supports Safe Start-Up into a Prebiased Output
- –40°C to +125°C Junction Temperature Range
- Available in 16-pin, 3 mm × 3 mm QFN Package

Applications

- Networking/Telecom Equipment
- Base Stations, Servers
- Distributed Power Systems
- Industrial Power Supplies

General Description

The MIC2125 and MIC2126 are constant-frequency synchronous buck controllers featuring a unique adaptive ON-time control architecture. The MIC2125/6 operate over an input voltage range from 4.5V to 28V and can be used to supply load current up to 25A. The output voltage is adjustable down to 0.6V with a guaranteed accuracy of ±1%. The device operates with programmable switching frequency from 200 kHz to 750 kHz.

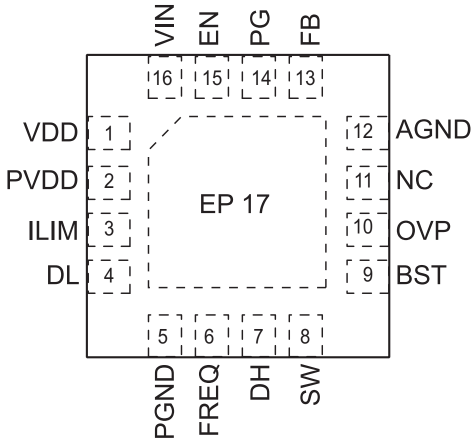
HyperLight Load® architecture provides the same high efficiency and ultra-fast transient response as the Hyper Speed Control® architecture under medium to heavy loads. It also maintains high efficiency under light load conditions by transitioning to variable frequency, discontinuous conduction mode operation.

The MIC2125/6 offer a full suite of features to ensure protection of the IC during fault conditions. These include undervoltage lockout to ensure proper operation under power-sag conditions, internal soft-start to reduce inrush current, "hiccup" mode short-circuit protection, and thermal shutdown.

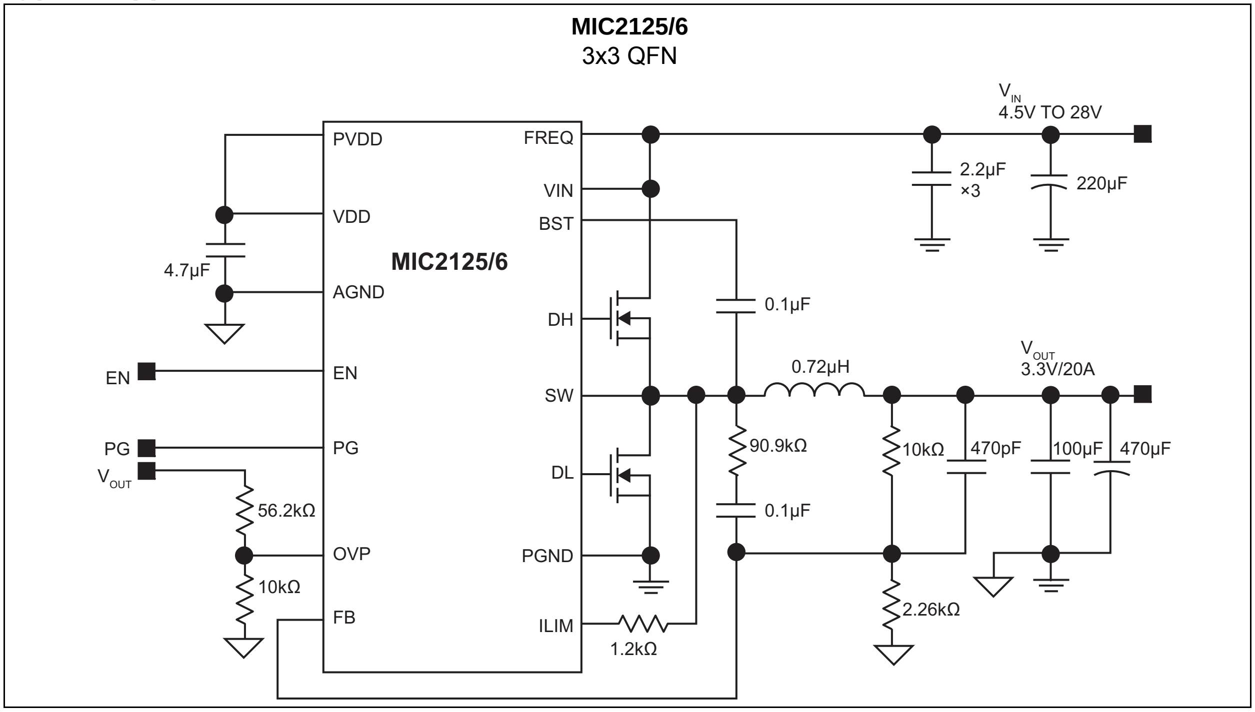
Package Type

MIC2125/6

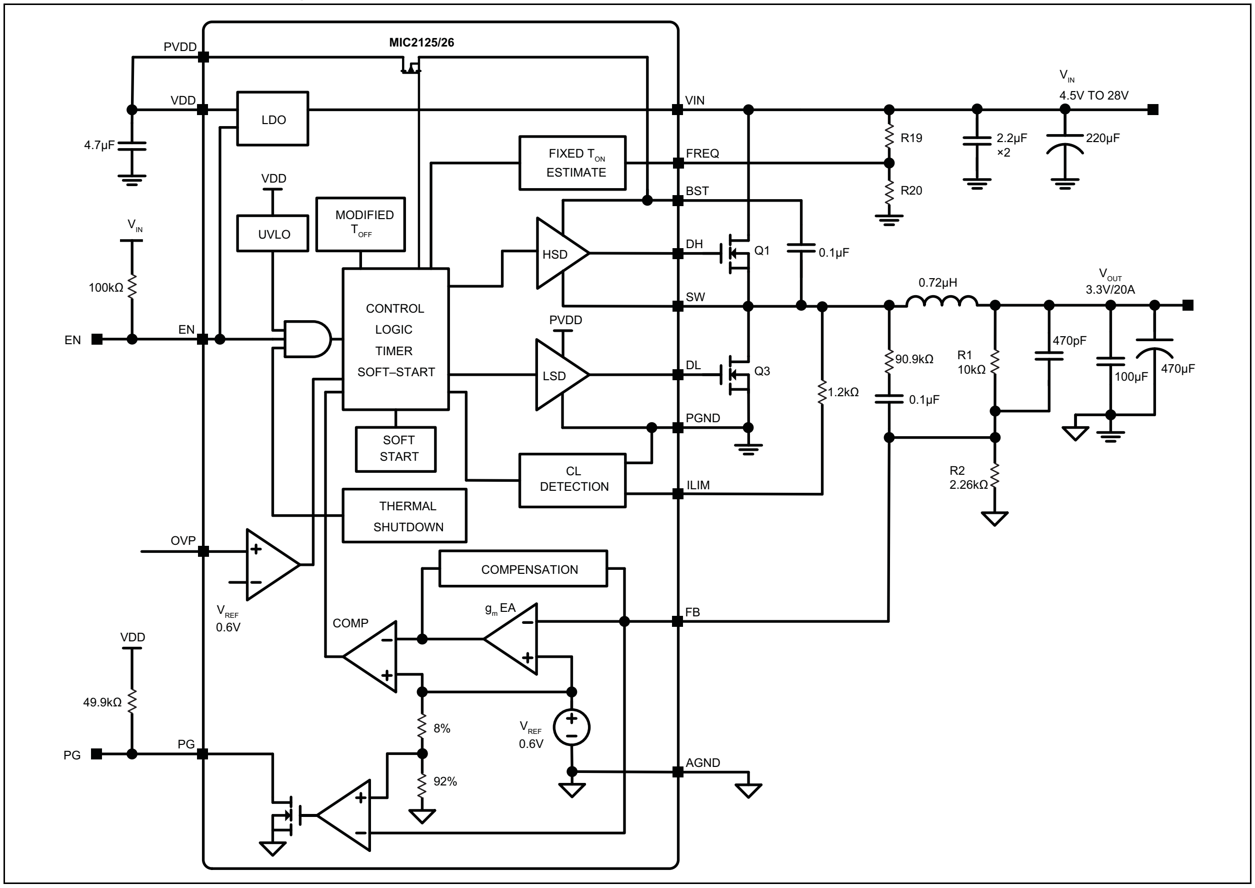
16-Pin 3 mm x 3 mm QFN (ML)



Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN}	–0.3V to +30V
V_{DD}, P_{VDD}	–0.3V to +6V
V_{SW}, V_{FREQ}, V_{ILIM}, V_{EN}	–0.3V to (V_{IN} +0.3V)
V_{BST} to V_{SW}	–0.3V to 6V
V_{BST}	–0.3V to 36V
V_{PG}	–0.3V to (V_{DD} + 0.3V)
V_{FB}	–0.3V to (V_{DD} + 0.3V)
P_{GND} to A_{GND}	–0.3V to +0.3V
ESD Rating(1)	2 kV

Operating Ratings ‡

Supply Voltage (V_{IN})	4.5V to 28V
V_{SW}, V_{FREQ}, V_{ILIM}, V_{EN}	0V to V_{IN}

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{IN} = 12V, V_{OUT} = 1.2V, $V_{BST} - V_{SW}$ = 5V; T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C. (**Note 1**).

Parameters	Min.	Typ.	Max.	Units	Conditions
Power Supply Input					
Input Voltage Range (V_{IN}) (**Note 2**)	**4.5**	—	**5.5**	V	$V_{DD} = V_{IN}$
	4.5	—	**28**		—
Quiescent Supply Current (MIC2125)	—	340	**750**	µA	V_{FB} = 1.5V
Quiescent Supply Current (MIC2126)	—	1.1	**3**	mA	V_{FB} = 1.5V
Shutdown Supply Current	—	0.1	**5**	µA	SW unconnected, V_{EN} = 0V
V_{DD} Supply					
V_{DD} Output Voltage	**4.8**	5.2	**5.4**	V	V_{IN} = 7V to 28V, I_{DD} = 10 mA
V_{DD} UVLO Threshold	**3.7**	4.2	**4.5**		V_{DD} rising
V_{DD} UVLO Hysteresis	—	400	—	mV	—
Load Regulation	0.6	2	3.6	%	I_{DD} = 0 to 40 mA
Reference					
Feedback Reference Voltage	0.597	0.6	0.603	V	T_J = 25°C (±0.5%)
	0.594	0.6	**0.606**		–40°C ≤ T_J ≤ +125°C (±1%)
FB Bias Current	—	0.01	**0.5**	µA	V_{FB} = 0.6V
Enable Control					
EN Logic Level High	**1.6**	—	—	V	—
EN Logic Level Low	—	—	**0.6**		—
EN Hysteresis	—	120	—	mV	—
EN Bias Current	—	6	**30**	µA	V_{EN} = 12V
Oscillator					
Switching Frequency	—	750	—	kHz	$V_{FREQ} = V_{IN}$
	—	375	—		V_{FREQ} = 50% x V_{IN}
Maximum Duty Cycle	—	85	—	%	—
Minimum Duty Cycle	—	0	—		V_{FB} > 0.6V
Minimum On-Time	—	100	—	ns	—
Minimum Off-Time	150	220	300		—
Soft-Start					
Soft-Start Time	—	7	—	ms	—
Short-Circuit Protection and OVP					
Current-Limit Comparator Offset	–15	–4	7	mV	V_{FB} = 0.6V
Current-Limit Source Current	32	36	40	µA	V_{FB} = 0.6V

Note 1: Specification for packaged product only.

2: The application is fully functional at low V_{DD} (supply of the control section) if the external MOSFETs have low voltage V_{TH}.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = 12V, V_{OUT} = 1.2V, $V_{BST} – V_{SW}$ = 5V; T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C. (**Note 1**).

Parameters	Min.	Typ.	Max.	Units	Conditions
Overvoltage Protection Threshold	——	0.62	—	V	—
FET Drivers					
DH, DL Output Low Voltage	—	—	**0.1**	V	I_{SINK} = 10 mA
DH, DL Output High Voltage	V_{PVDD}-0.1 or V_{BST}-0.1	—	—		I_{SOURCE} = 10 mA
DH On-Resistance, High State	—	2.5	—	Ω	—
DH On-Resistance, Low State	—	1.6	—		—
DL On-Resistance, High State	—	1.9	—		—
DL On-Resistance, Low State	—	0.55	—		—
SW, BST Leakage Current	—	—	50	µA	—
Power Good (PG)					
PG Threshold Voltage	**85**	89	**95**	%V_{OUT}	Sweep V_{FB} from low to high
PG Hysteresis	—	6	—		Sweep V_{FB} from high to low
PG Delay Time	—	80	—	µs	Sweep V_{FB} from low to high
PG Low Voltage	—	60	**200**	mV	V_{FB} < 90% x V_{NOM}, I_{PG} = 1 mA
Thermal Protection					
Overtemperature Shutdown	—	150	—	°C	T_J Rising
Overtemperature Shutdown Hysteresis	—	15	—	°C	—

Note 1: Specification for packaged product only.

2: The application is fully functional at low V_{DD} (supply of the control section) if the external MOSFETs have low voltage V_{TH}.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Operating Temperature	T_J	–40	—	+125	°C	Note 1
Storage Temperature Range	T_S	–65	—	+150	°C	—
Junction Temperature	T_J	—	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10s
Package Thermal Resistances						
Thermal Resistance 3 mm x 3 mm QFN-16LD	θ_{JA}	—	50.8	—	°C/W	—
	θ_{JC}	—	25.3	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise noted, V_{IN} = 12V, FREQ = 350 kHz.

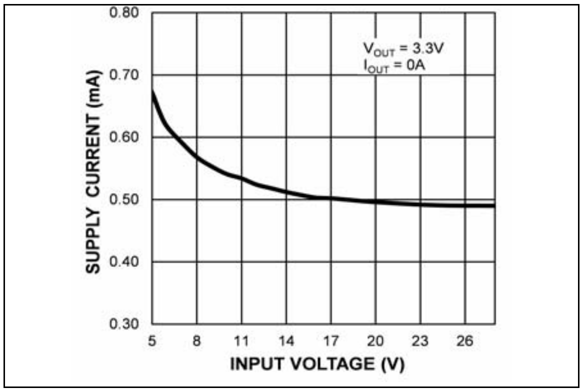


FIGURE 2-1: *V_{IN} Operating Supply Current vs. Input Voltage (MIC2125).*

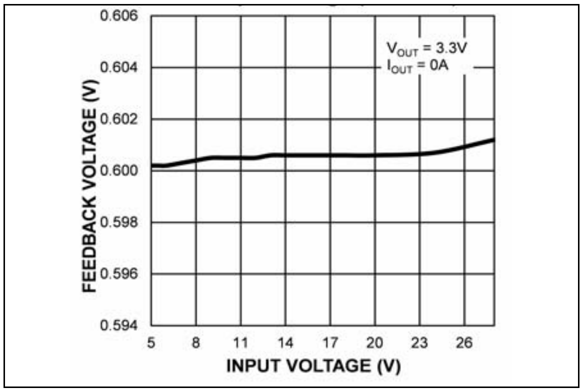


FIGURE 2-2: *Feedback Voltage vs. Input Voltage (MIC2125).*

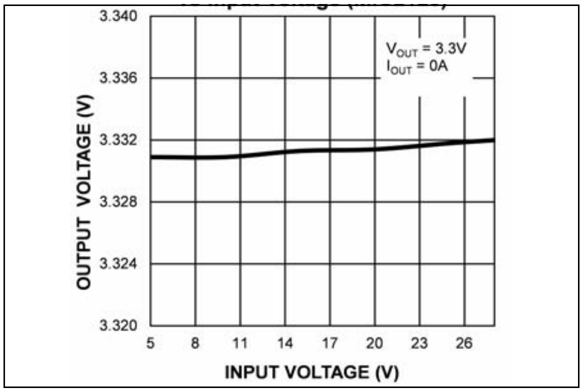


FIGURE 2-3: *Output Voltage vs. Input Voltage (MIC2125).*

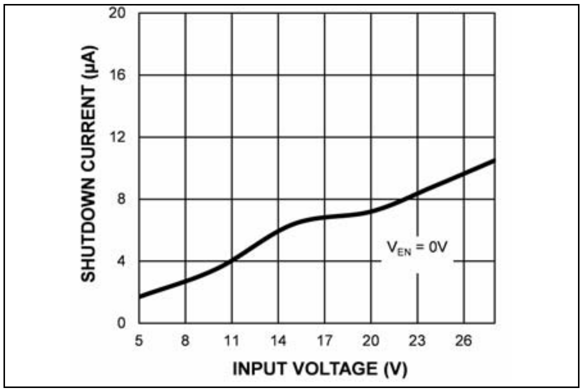


FIGURE 2-4: *V_{IN} Shutdown Current vs. Input Voltage (MIC2125).*

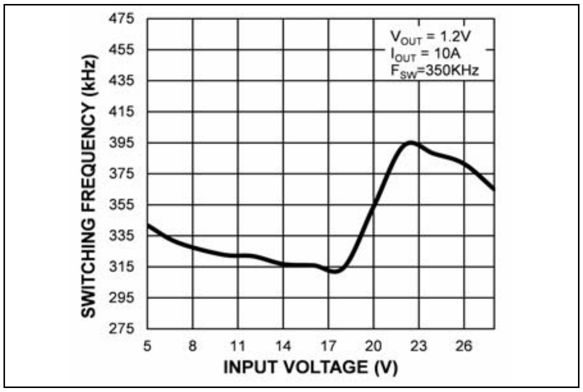


FIGURE 2-5: *Switching Frequency vs. Input Voltage.*

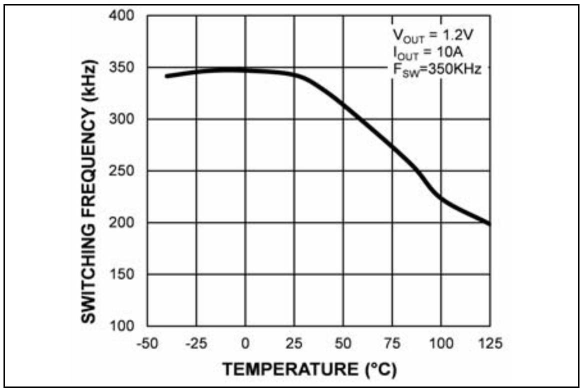


FIGURE 2-6: *Switching Frequency vs. Temperature (MIC2126).*

Note: Unless otherwise noted, V_{IN} = 12V, FREQ = 350 kHz.

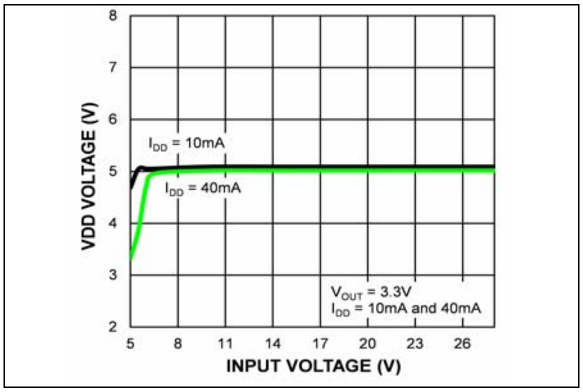


FIGURE 2-7: *V_{DD} Voltage vs. Input Voltage (MIC2125).*

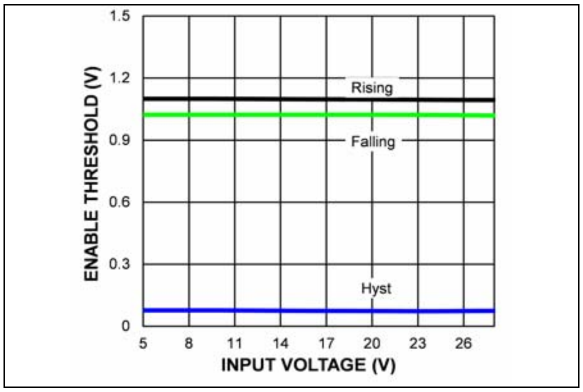


FIGURE 2-8: *Enable Threshold vs. Input Voltage (MIC2125).*

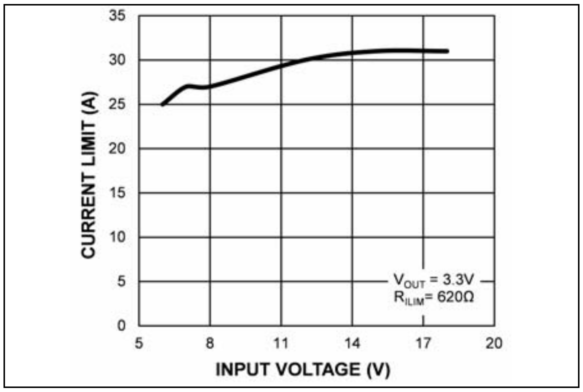


FIGURE 2-9: *Output Peak Current Limit vs. Input Voltage (MIC2125).*

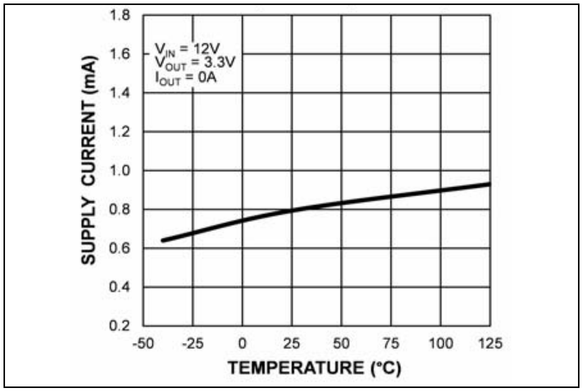


FIGURE 2-10: *V_{IN} Operating Supply Current vs. Temperature (MIC2125).*

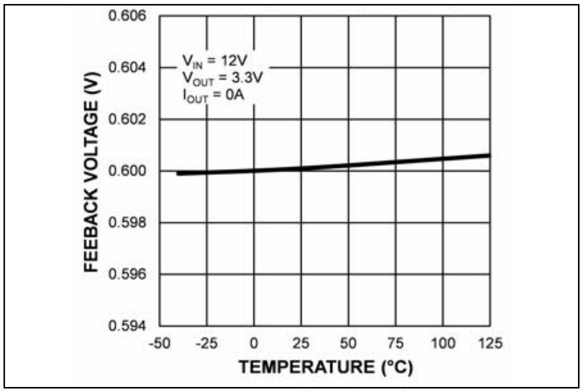


FIGURE 2-11: *Feedback Voltage vs. Temperature (MIC2125).*

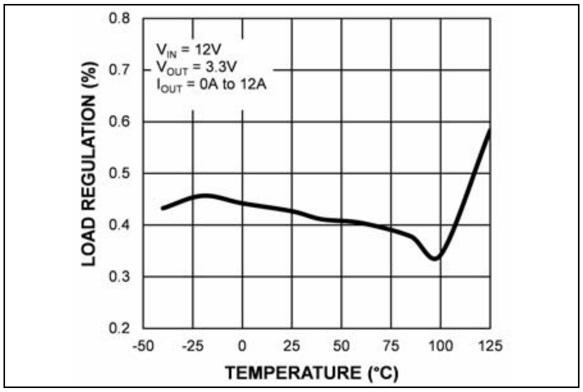


FIGURE 2-12: *Load Regulation vs. Temperature (MIC2125).*

Note: Unless otherwise noted, V_{IN} = 12V, FREQ = 350 kHz.

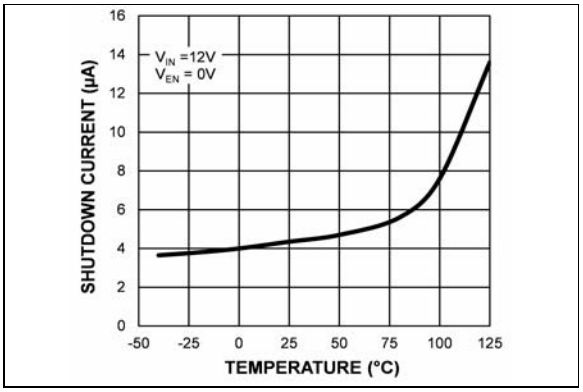


FIGURE 2-13: *V_{IN} Shutdown Current vs. Temperature (MIC2125).*

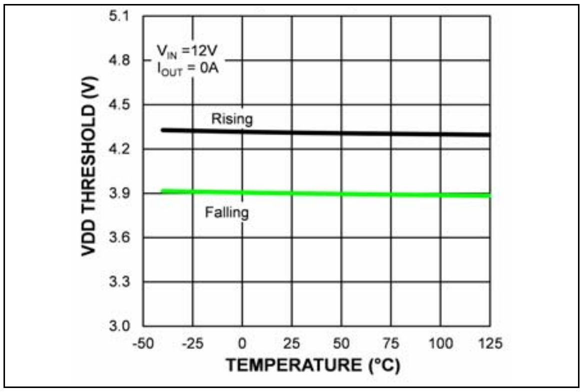


FIGURE 2-14: *V_{DD} UVLO Threshold vs. Temperature (MIC2125).*

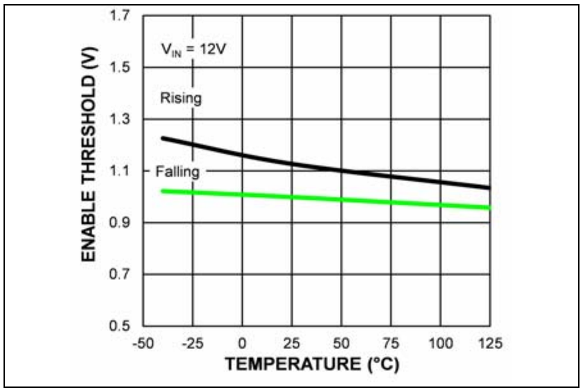


FIGURE 2-15: *Enable Threshold vs. Temperature (MIC2125).*

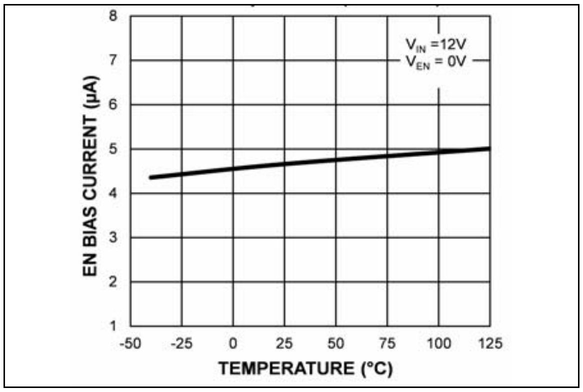


FIGURE 2-16: *EN Bias Current vs. Temperature (MIC2125).*

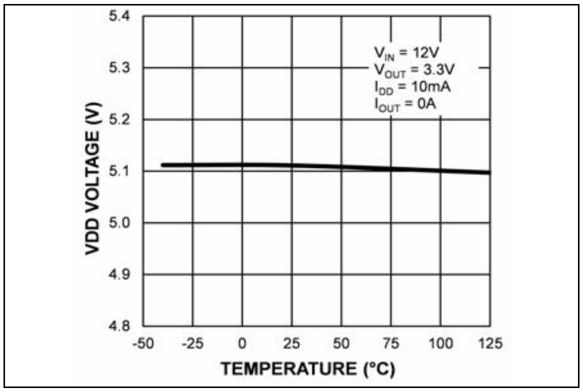


FIGURE 2-17: *V_{DD} Voltage vs. Temperature (MIC2125).*

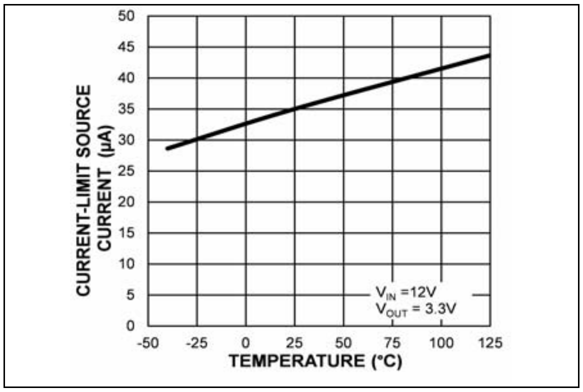


FIGURE 2-18: *Current-Limit Source Current vs. Temperature (MIC2125).*

Note: Unless otherwise noted, V_{IN} = 12V, FREQ = 350 kHz.

***Note:** For Case Temperature graphs: The temperature measurement was taken at the hottest point on the MIC2125/6 case mounted on a 5 square inch PCBn. Actual results will depend upon the size of the PCB, ambient temperature and proximity to other heat emitting components.

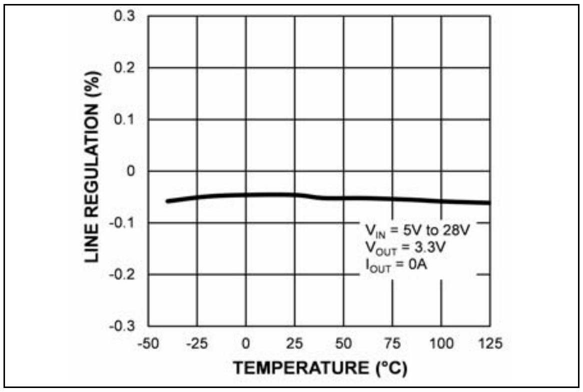


FIGURE 2-19: *Line Regulation vs. Temperature (MIC2125).*

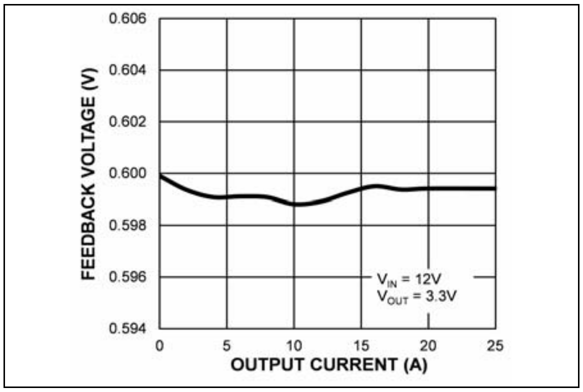


FIGURE 2-20: *Feedback Voltage vs. Output Current (MIC2125).*

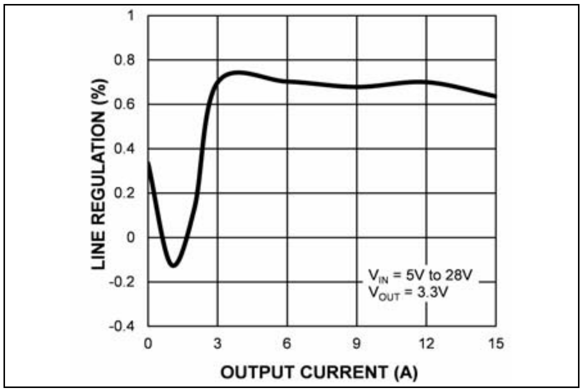


FIGURE 2-21: *Line Regulation vs. Output Current (MIC2125).*

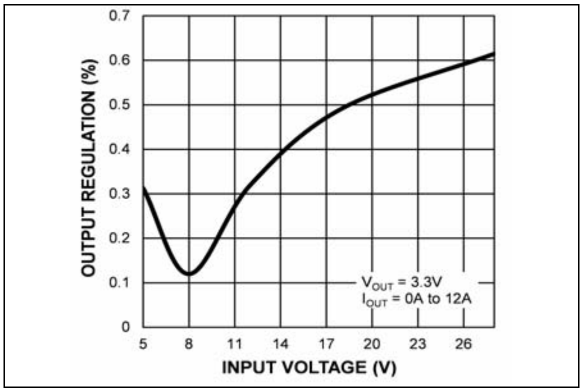


FIGURE 2-22: *Output Regulation vs. Input Voltage (MIC2125).*

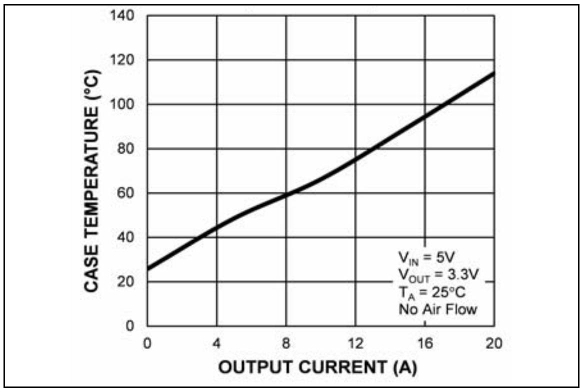


FIGURE 2-23: *Case Temperature* vs. Output Current (MIC2125).*

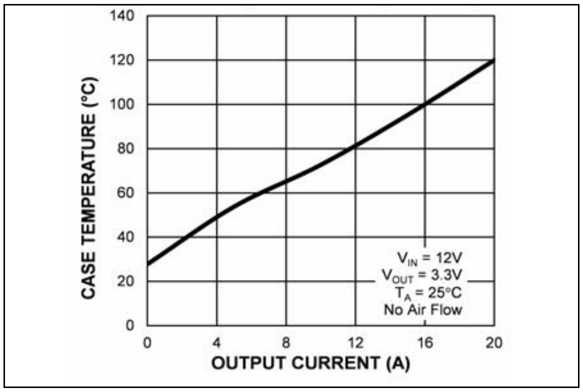


FIGURE 2-24: *Case Temperature* vs. Output Current (MIC2125).*

Note: Unless otherwise noted, V_{IN} = 12V, FREQ = 350 kHz.

***Note:** For Case Temperature graphs: The temperature measurement was taken at the hottest point on the MIC2125/6 case mounted on a 5 square inch PCBn. Actual results will depend upon the size of the PCB, ambient temperature and proximity to other heat emitting components.

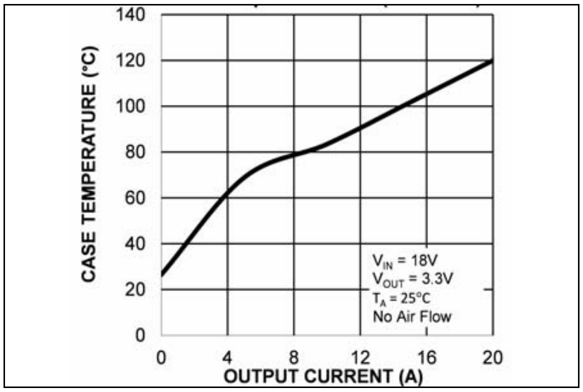


FIGURE 2-25: *Case Temperature* vs. Output Current (MIC2125).*

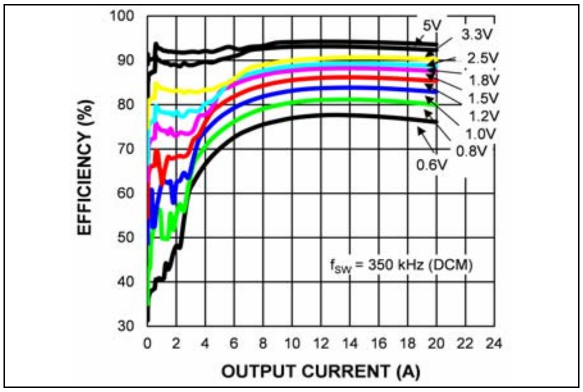


FIGURE 2-28: *Efficiency (V_{IN} = 18V) vs. Output Current (MIC2125).*

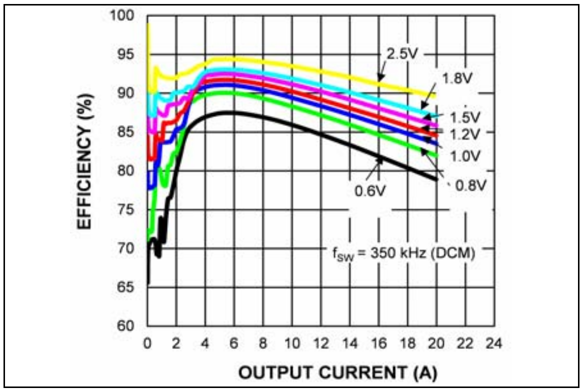


FIGURE 2-26: *Efficiency (V_{IN} = 5V) vs. Output Current (MIC2125).*

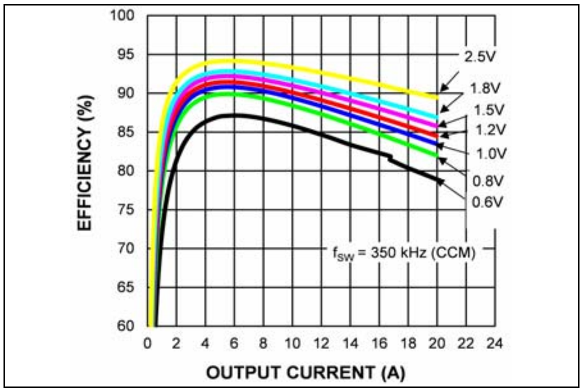


FIGURE 2-29: *Efficiency (V_{IN} = 5V) vs. Output Current (MIC2126).*

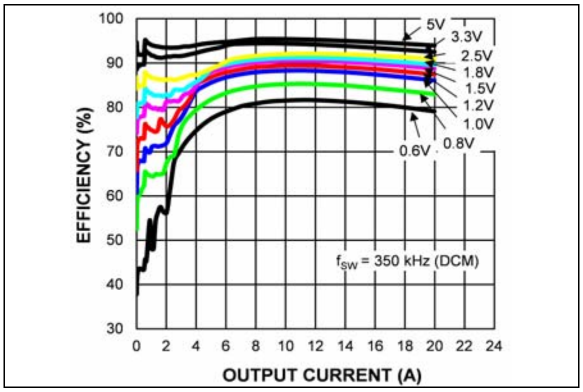


FIGURE 2-27: *Efficiency (V_{IN} = 12V) vs. Output Current (MIC2125).*

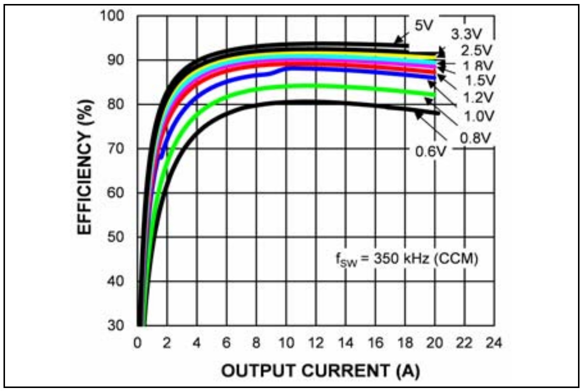


FIGURE 2-30: *Efficiency (V_{IN} = 12V) vs. Output Current (MIC2126).*

Note: Unless otherwise noted, V_{IN} = 12V, FREQ = 350 kHz.

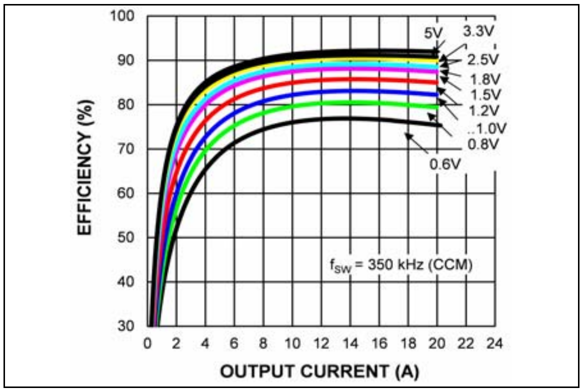


FIGURE 2-31: *Efficiency (V_{IN} = 18V) vs. Output Current (MIC2126).*

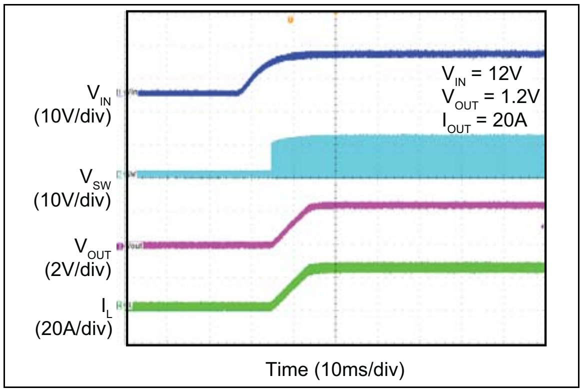


FIGURE 2-32: *V_{IN} Soft Turn-On.*

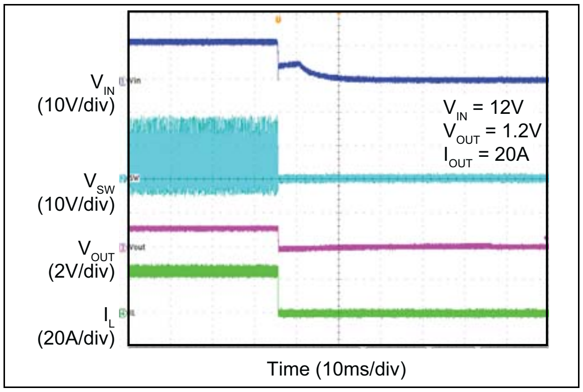


FIGURE 2-33: *V_{IN} Soft Turn-Off.*

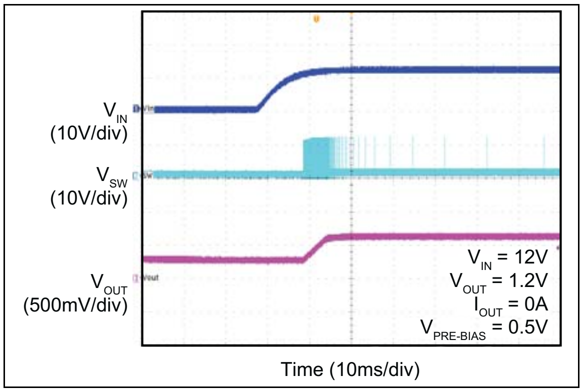


FIGURE 2-34: *MIC2125 V_{IN} Start-Up with Prebiased Output.*

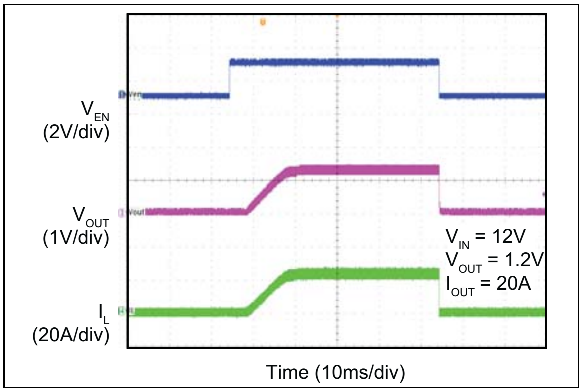


FIGURE 2-35: *Enable Turn-On/Turn-Off.*

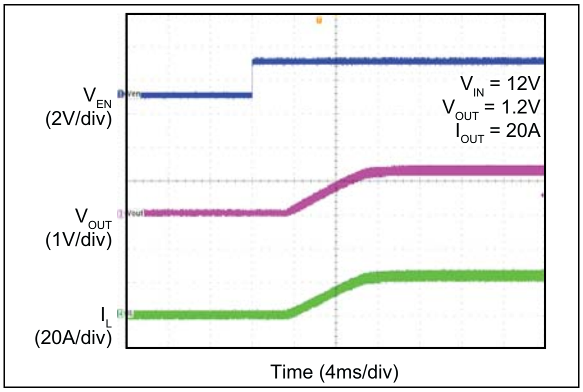


FIGURE 2-36: *Enable Turn-On Delay and Rise Time.*

Note: Unless otherwise noted, V_{IN} = 12V, FREQ = 350 kHz.

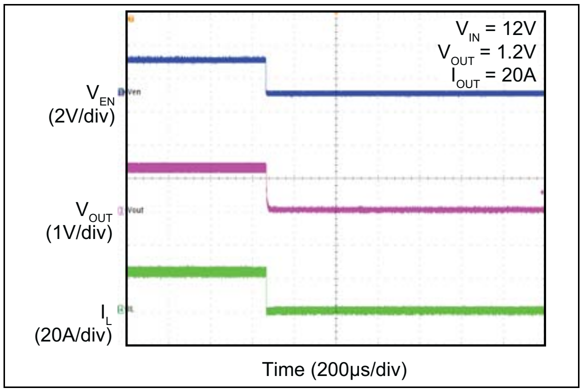


FIGURE 2-37: *Enable Turn-Off Delay and Fall Time.*

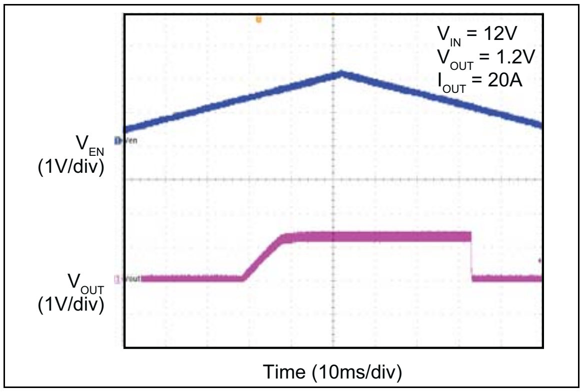


FIGURE 2-38: *Enable Thresholds.*

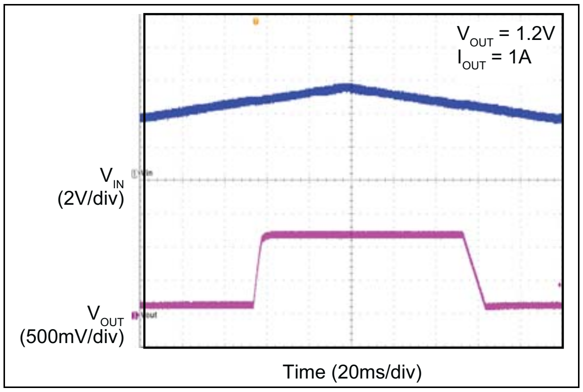


FIGURE 2-39: *Enable Turn-On Delay and Rise Time.*

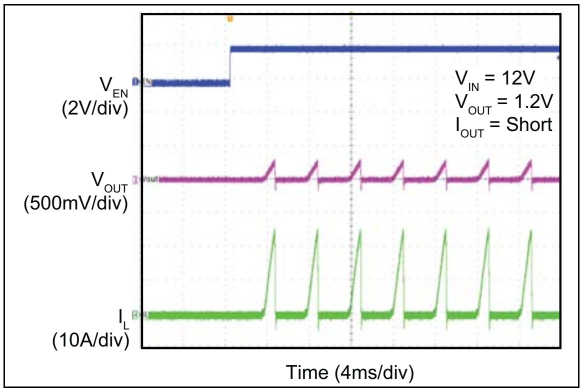


FIGURE 2-40: *Enabled into Short.*

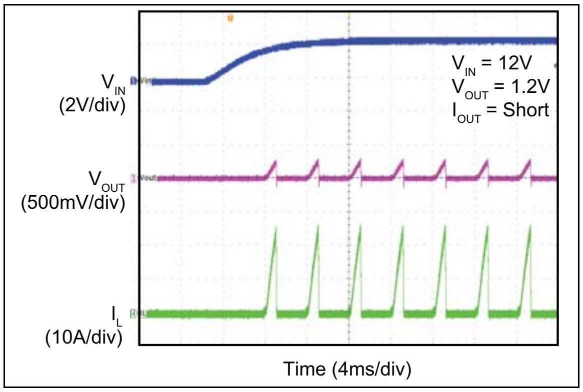


FIGURE 2-41: *Power-Up into Short-Circuit.*

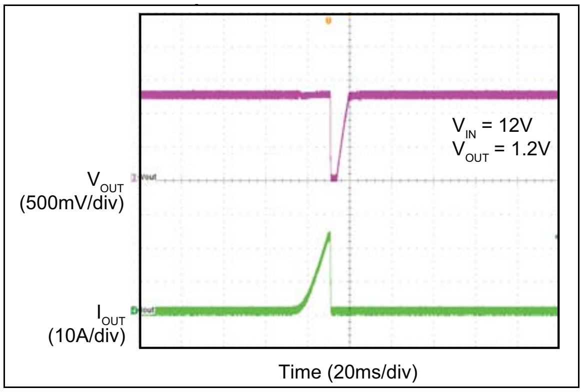


FIGURE 2-42: *Output Peak Current-Limit Threshold.*

Note: Unless otherwise noted, V_{IN} = 12V, FREQ = 350 kHz.

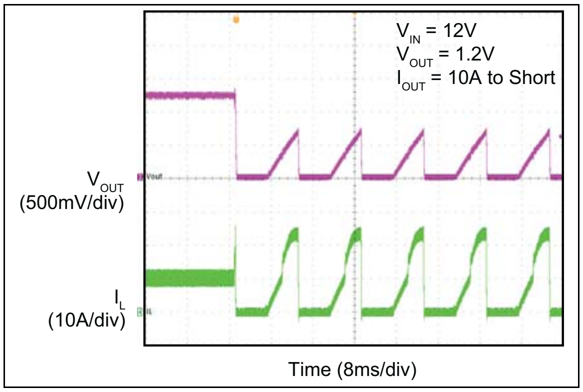


FIGURE 2-43: *Short-Circuit.*

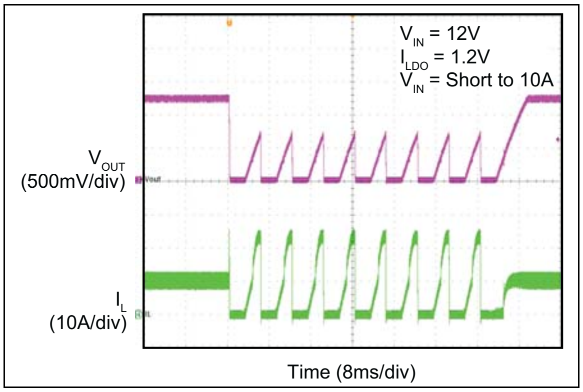


FIGURE 2-44: *Output Recovery from Short-Circuit.*

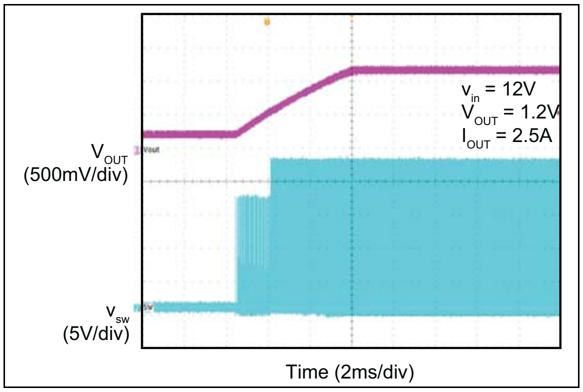


FIGURE 2-45: *Output Recovery from Thermal Shutdown.*

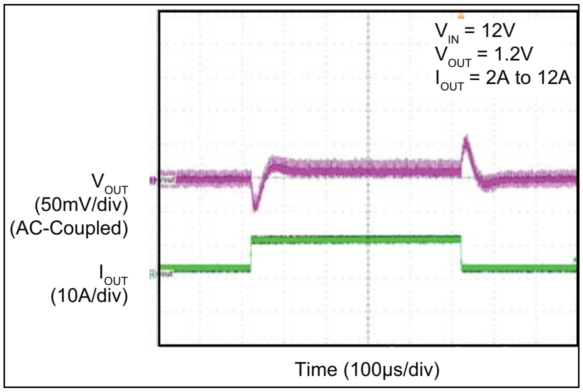


FIGURE 2-46: *Transient Response.*

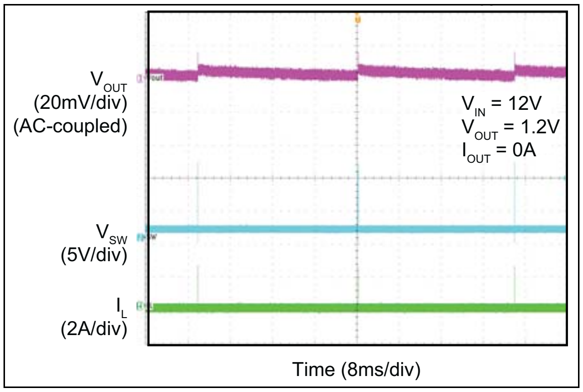


FIGURE 2-47: *MIC2125 Switching Waveform, I_{OUT} = 0A.*

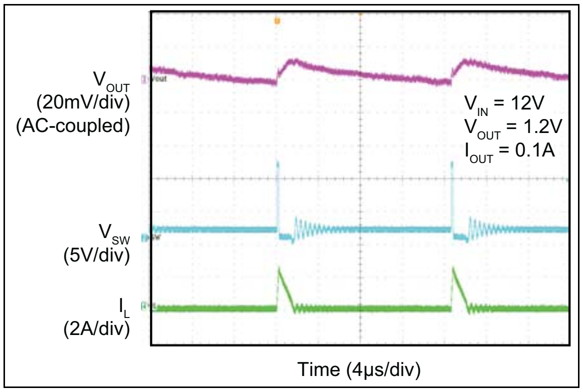


FIGURE 2-48: *MIC2125 Switching Waveform, I_{OUT} = 0.1A.*

Note: Unless otherwise noted, V_{IN} = 12V, FREQ = 350 kHz.

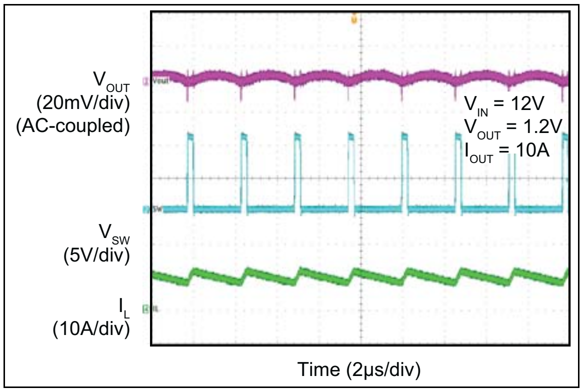


FIGURE 2-49: *Switching Waveform, I_{OUT} = 10A.*

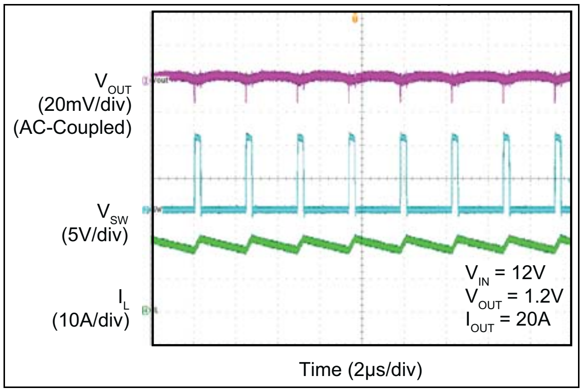


FIGURE 2-50: *Switching Waveform, I_{OUT} = 20A.*

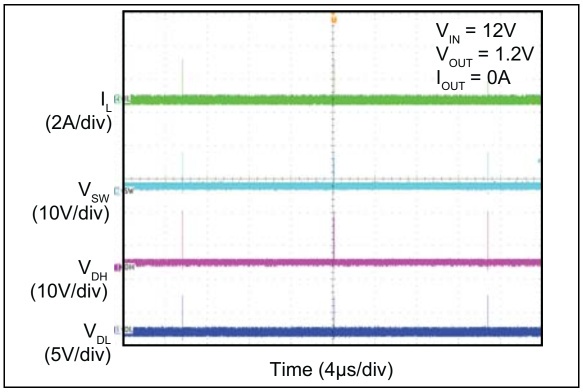


FIGURE 2-51: *MIC2125 Switching Waveform, I_{OUT} = 0A.*

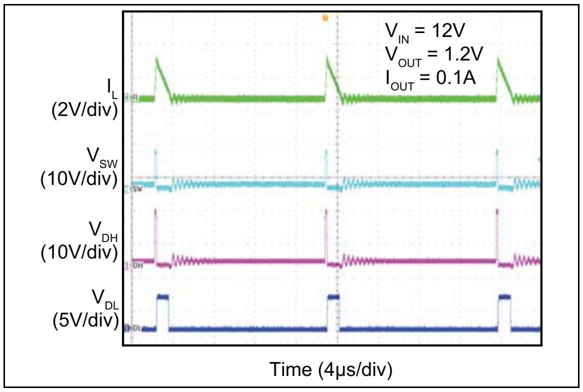


FIGURE 2-52: *MIC2125 Switching Waveform, I_{OUT} = 0.1A.*

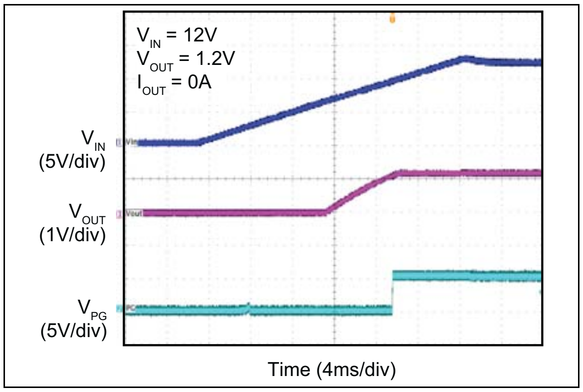


FIGURE 2-53: *Power Good at V_{IN} Soft Turn-On.*

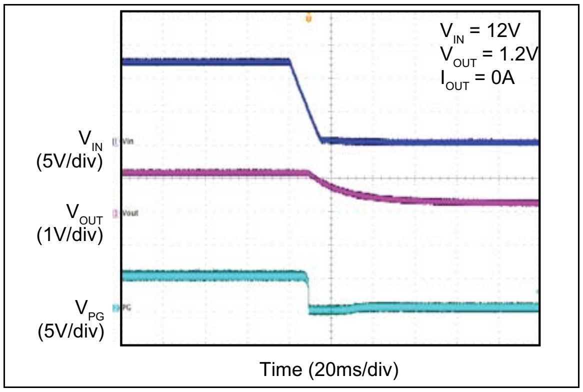


FIGURE 2-54: *Power Good at V_{IN} Soft Turn-Off.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1	V_{DD}	Internal Linear regulator output. Connect a 4.7 µF ceramic capacitor from V_{DD} to A_{GND} for decoupling. In the applications where V_{IN} < +5.5V, V_{DD} should be tied to V_{IN} to by-pass the linear regulator.
2	P_{VDD}	5V supply input for the low-side N-channel MOSFET driver, which can be tied to V_{DD} externally. A 4.7 µF ceramic capacitor from P_{VDD} to P_{GND} is recommended for decoupling.
3	I_{LIM}	Current limit setting input. Connect a resistor from SW to I_{LIM} to set the overcurrent threshold for the converter.
4	DL	Low-side gate driver output. The DL driving voltage swings from ground to V_{DD}.
5	P_{GND}	Power ground. P_{GND} is the return path for the low side gate driver. Connect P_{GND} pin to the source of low-side N-Channel external MOSFET.
6	FREQ	Switching frequency adjust input. Connect FREQ to the mid-point of an external resistor divider from V_{IN} to GND to program the switching frequency. Tie to V_{IN} to operate at 750 kHz frequency.
7	DH	High-side gate driver output. The DH driving voltage is floating on the switch node voltage (V_{SW}).
8	SW	Switch node and current-sense input. Connect the SW pin to the switch node of the buck converter. The SW pin also senses the current by monitoring the voltage across the low-side MOSFET during OFF time. In order to sense the current accurately, connect the low-side MOSFET drain to the SW pin using a Kelvin connection.
9	BST	Bootstrap Capacitor Input. Connect a ceramic capacitor with a minimum value of 0.1 µF from BST to SW.
10	OVP	Output Overvoltage Protection Input. Connect to the mid-point of an external resistive divider from the V_{OUT} to GND to program overvoltage limit. Connect to A_{GND} if the output overvoltage protection is not required.
11	NC	No connect.
12	A_{GND}	Analog Ground. Connect A_{GND} to the exposed pad.
13	FB	Feedback input. Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.6V. A resistor divider connecting the feedback to the output is used to set the desired output voltage.
14	PG	Open-drain Power good output. Pull-up with an external pull-up resistor to V_{DD} or to an external power rail.
15	EN	Enable input. A logic signal to enable or disable the buck converter operation. Logic-high enables the device; logic-low shuts down the regulator. In disable mode, the V_{DD} supply current for the device is minimized to 0.1 µA typically. Do not pull-up EN pin to V_{DD}/P_{VDD}.
16	V_{IN}	Supply voltage input. The V_{IN} operating voltage range is from 4.5V to 28V. A 1 µF ceramic capacitor from V_{IN} to A_{GND} is required for decoupling.
17	EP	Exposed Pad. Connect the exposed pad to the A_{GND} copper plane to improve the thermal performance.

4.0 FUNCTIONAL DESCRIPTION

The MIC2125 and MIC2126 are adaptive on-time synchronous buck controllers built for high input voltage to low output voltage applications. They are designed to operate over a wide input voltage range from 4.5V to 28V and their output is adjustable with an external resistive divider. An adaptive ON-time control scheme is employed to obtain a constant switching frequency and to simplify the control compensation. Overcurrent protection is implemented when sensing low-side MOSFET's $R_{DS(ON)}$. The device features internal soft-start, enable, UVLO, and thermal shutdown.

4.1 Theory of Operation

The MIC2125/6 Functional Block Diagram appears on page two. The output voltage is sensed by the MIC2125/6 feedback pin (FB), and is compared to a 0.6V reference voltage (V_{REF}) at the low gain transconductance error amplifier (g_m). Figure 4-1 shows the MIC2125/6 control loop timing during steady-state operation. When the feedback voltage decreases and the amplifier output is below 0.6V, the comparator triggers and generates an ON-time period. The ON-time period is predetermined by the fixed t_{ON} estimator circuitry value from Equation 4-1:

EQUATION 4-1:

$$t_{ON(ESTIMATED)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Where:

V_{OUT}	Output Voltage
V_{IN}	Power Stage Input Voltage
f_{SW}	Switching Frequency

At the end of the ON-time, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time depends upon the feedback voltage. When the feedback voltage decreases and the output of the g_m amplifier is below 0.6V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(min)}$, which is about 220 ns, the MIC2125/6 control logic applies the $t_{OFF(min)}$ instead. $t_{OFF(min)}$ is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 220 ns $t_{OFF(MIN)}$:

EQUATION 4-2:

$$D_{MAX} = \frac{t_S - t_{OFF(MIN)}}{t_S} = 1 - \frac{220ns}{t_S}$$

Where:

t_S	$1/f_{SW}$

It is not recommended to use MIC2125/6 with an OFF-time close to $t_{OFF(MIN)}$ during steady-state operation.

The adaptive ON-time control scheme results in a constant switching frequency in the MIC2125/6. The actual ON-time and resulting switching frequency varies with the different rising and falling times of the external MOSFETs. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications.

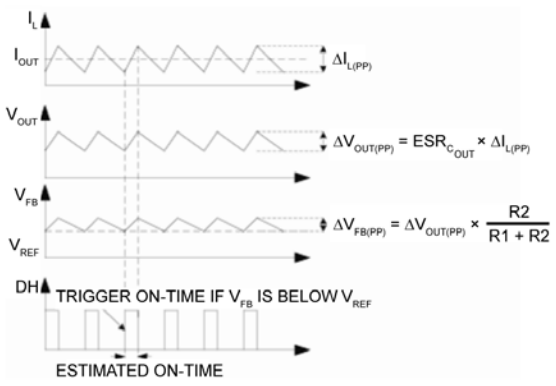


FIGURE 4-1: *MIC2125/6 Control Loop Timing*

Figure 4-2 shows the operation of the MIC2125/6 during load transient. The output voltage drops due to a sudden increase in load, which results in the V_{FB} falling below V_{REF}. This causes the comparator to trigger an ON-time period. At the end of the ON-time, a minimum OFF-time $t_{OFF(min)}$ is generated to charge C_{BST} if the feedback voltage is still below V_{REF}. The next ON-time is triggered immediately after the $t_{OFF(min)}$ due to the low feedback voltage. This operation results in higher switching frequency during load transients. The switching frequency returns to the nominal set frequency once the output stabilizes at new load current level. The output recovery time is fast and the output voltage deviation is small in MIC2125/6 converter due to the varying duty cycle and switching frequency.

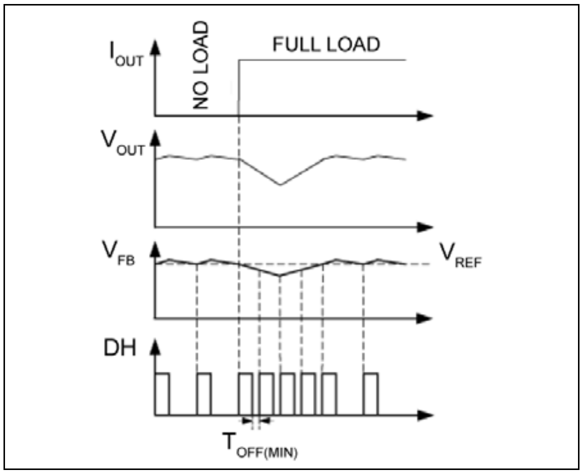


FIGURE 4-2: *MIC2125/6 Load Transient Response*

Unlike true current-mode control, the MIC2125/6 uses the output voltage ripple to trigger an ON-time period. In order to meet the stability requirements, the MIC2125/6 feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the g_m amplifier. The recommended feedback voltage ripple is 20 mV ~ 100 mV over the full input voltage range. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. For these applications, ripple injection is required to ensure proper operation. Refer to the Ripple Injection section under Application Information for details about the ripple injection technique.

4.2 Discontinuous Conduction Mode (MIC2125 Only)

The MIC2125 operates in discontinuous conduction mode at light load. The MIC2125 has a zero crossing comparator (ZC detection) that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If the V_{FB} > 0.6V and the inductor current goes slightly negative, the MIC2125 turns off both the high-side and low-side MOSFETs. During this period, the efficiency is optimized by shutting down all the non-essential circuits and the load current is supplied by the output capacitor. The control circuitry wakes up when the feedback voltage falls below V_{REF} and triggers a t_{ON} pulse. Figure 4-3 shows the control loop timing in discontinuous conduction mode.

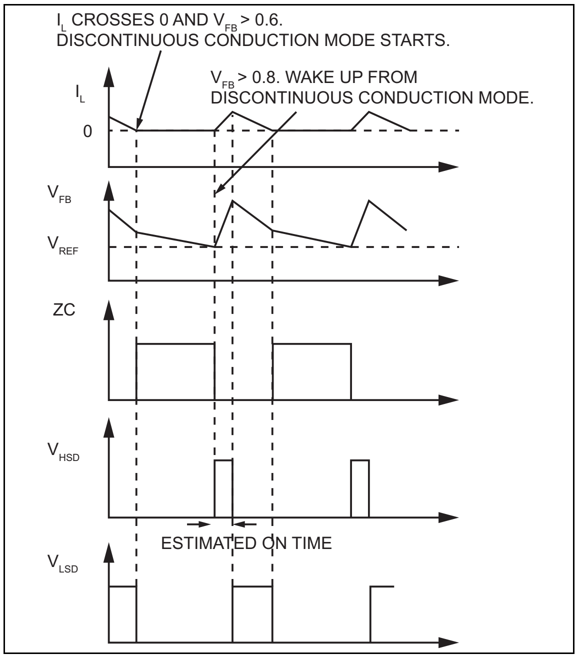


FIGURE 4-3: *MIC2125 Control Loop Timing (Discontinuous Conduction Mode)*

The typical no load supply current during discontinuous conduction mode is only about 340 µA, allowing the MIC2125 to achieve high efficiency at light load operation.

4.3 Soft-Start

Soft-start reduces the power supply inrush current at startup by controlling the output voltage rise time. The MIC2125/6 implements an internal digital soft-start by ramping up the reference voltage V_{REF} from 0 to 100% in about 7 ms. Once the soft-start is completed, the related circuitry is disabled to reduce the current consumption.

4.4 Current Limit

The MIC2125/6 uses the low-side MOSFET $R_{DS(ON)}$ to sense the inductor current.

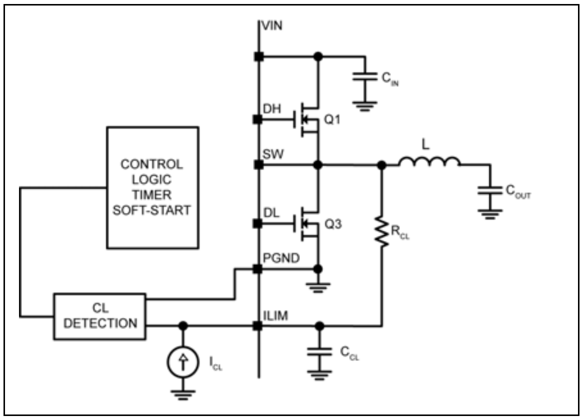


FIGURE 4-4: MIC2125/6 Current-Limiting Circuit

In each switching cycle of the MIC2125/6 converter, the inductor current is sensed by monitoring the voltage across the low-side MOSFET during the OFF period. An internal current source of 36 µA generates a voltage across the external resistor R_{CL}. The I_{LIM} pin voltage $V_{(ILIM)}$ is the sum of the voltage across the low side MOSFET and the voltage across the resistor (V_{CL}). The sensed voltage $V_{(ILIM)}$ is compared with the power ground (P_{GND}) after a blanking time of 150 ns.

If the absolute value of the voltage drop across the low side MOSFET is greater than V_{CL}, the current limit event is triggered. Eight consecutive current limit events triggers hiccup mode. The hiccup sequence, including the soft-start, reduces the stress on the switching FETs and protects the load and supply from severe short conditions.

The current limit can be programmed by using Equation 4-3.

EQUATION 4-3:

$$R_{CL} = \frac{(I_{CLIM} + \Delta_{PP} \times 0.5) \times R_{DS(ON)} - V_{OFFSET}}{I_{CL}}$$

Where:

I_{CLIM}	Desired Current Limit
Δ_{PP}	Inductor Current Peak-to-Peak
$R_{DS(ON)}$	On-Resistance of Low-Side Power MOSFET
V_{OFFSET}	Current-Limit Comparator Offset (Typical Value is –4 mV per Table 1-1)
I_{CL}	Current-Limit Source Current (Typical Value is 36 µA, per Table 1-1)

Because MOSFET $R_{DS(ON)}$ varies from 30% to 40% with temperature, it is recommended to add a 50% margin to I_{CL} in the previous equation to avoid false current limiting due to increased MOSFET junction temperature rise. It is also recommended to connect the SW pin directly to the drain of the low-side MOSFET to accurately sense the MOSFET's $R_{DS(ON)}$.

4.5 Negative Current Limit (MIC2126 Only)

The MIC2126 implements negative current limit by sensing the SW voltage when the low-side FET is off. If the SW node voltage exceeds 12 mV typical, the device turns off the low-side FET until the next ON-time event is triggered. The negative current limit value is given by Equation 4-4.

EQUATION 4-4:

$$I_{NLIM} = \frac{12mV}{R_{DS(ON)}}$$

Where:

I_{NLIM}	Negative Current Limit
$R_{DS(ON)}$	On-Resistance of Low-Side Power MOSFET

4.6 MOSFET Gate Drive

The MIC2125/6 high-side drive circuit is designed to switch an N-Channel MOSFET. Figure 4-1 shows a bootstrap circuit, consisting of a PMOS switch and C_{BST}. This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged while the low-side MOSFET is on and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. If the bias current of the high-side driver is less than 10 mA, a 0.1 µF capacitor is sufficient to hold the gate voltage within minimal droop, (i.e., Δ_{BST} = 10 mA × 3.33 µs/0.1 µF = 333 mV). A small resistor, RG in series with C_{BST}, can be used to slow down the turn-on time of the high-side N-channel MOSFET.

4.7 Overvoltage Protection

The MIC2125/6 includes the OVP feature to protect the load from overshoots due to input transients and output short to a high voltage. When the overvoltage condition is triggered, the converter turns off immediately to allow the output voltage to discharge. The MIC2125/6 power should be recycled to enable it again.

5.0 APPLICATION INFORMATION

5.1 Setting the Switching Frequency

The MIC2125/6 are adjustable-frequency, synchronous buck controllers featuring a unique adaptive ON–time control architecture. The switching frequency can be adjusted between 200 kHz and 750 kHz by changing the resistor divider network consisting of R19 and R20.

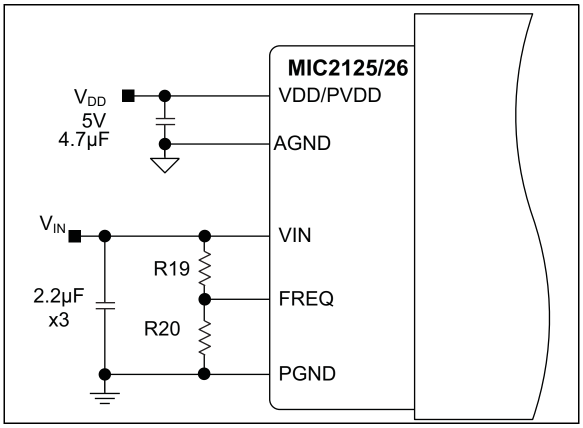


FIGURE 5-1: *Switching Frequency Adjustment.*

Equation 5-1 gives the estimated switching frequency.

EQUATION 5-1:

$$f_{SW(ADJ)} = f_O \times \frac{R20}{R19 + R20}$$

Where:

f_O	Switching Frequency when R19 is 100 kΩ and R20 is open. f_O is typically 750 kHz.

For more precise setting, it is recommended to use Figure 5-2.

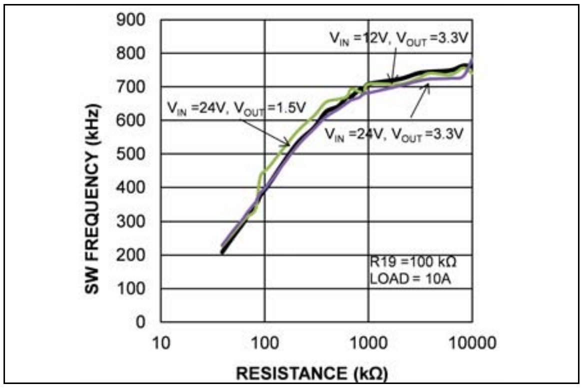


FIGURE 5-2: *Switching Frequency vs. R20*

5.2 MOSFET Selection

Voltage rating, on-resistance, and total gate charge are important parameters for MOSFET selection.

The voltage rating for the high-side and low-side MOSFETs are essentially equal to the power stage input voltage V_{IN}. A safety factor of 30% should be added to the $V_{IN(MAX)}$ while selecting the voltage rating of the MOSFETs to account for voltage spikes due to circuit parasitic elements.

The power dissipated in the MOSFETs is the sum of conduction losses ($P_{CONDUCTION}$) and switching losses (P_{AC}).

EQUATION 5-2:

$$P_{SW} = P_{CONDUCTION} + P_{AC}$$

EQUATION 5-3:

$$P_{CONDUCTION} = I_{SW(RMS)}^{2} \times R_{DS(ON)}$$

Where:

$R_{DS(ON)}$	On-Resistance of the MOSFET
$I_{SW(RMS)}$	RMS current of the MOSFET

The total high-side MOSFET switching loss is:

EQUATION 5-4:

$$P_{AC} = 0.5 \times V_{IN} \times I_{LOAD} \times (t_R + t_F) \times f_{SW}$$

Where:

t_R/t_F	Switching Transition Times
I_{LOAD}	Load Current
f_{SW}	Switching Frequency

Turn-on and turn-off transition times can be approximated by:

EQUATION 5-5:

$$t_R = \frac{Q_{SW(HS)} \times (R_{HSD(PULL-UP)} + R_{HS(GATE)})}{V_{DD} - V_{TH}}$$

EQUATION 5-6:

$$t_F = \frac{Q_{SW(HS)} \times (R_{HSD(PULL-UP)} + R_{HS(GATE)})}{V_{TH}}$$

Where:

$R_{HSD(PULL-UP)}$	High-Side Gate Driver Pull-Up Resistance
$R_{HSD(PULL-DOWN)}$	High-Side Gate Driver Pull-Down Resistance
$R_{HS(GATE)}$	High-Side MOSFET Gate Resistance
$Q_{SW(HS)}$	Switching Gate Charge of the High-Side MOSFET
V_{TH}	Gate Threshold Voltage

The high-side MOSFET switching losses increase with the switching frequency and the input voltage. The low-side MOSFET switching losses are negligible and can be ignored for these calculations.

5.3 Inductor Selection

Inductance value, saturation, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Larger peak-to-peak ripple current increases the power dissipation in the inductor and MOSFETs. Larger output ripple current also requires more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple current requires a larger inductance value and therefore a larger and more expensive inductor.

A good compromise between size, loss, and cost is to set the inductor ripple current to be equal to 40% of the maximum output current.

The inductance value is calculated by Equation 5-7.

EQUATION 5-7:

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times 0.4 \times I_{OUT(MAX)}}$$

Where:

f_{SW}	Switching Frequency
0.4	Ratio of AC Ripple Current to DC Output Current
$V_{IN(MAX)}$	Maximum Power Stage Input Voltage

The peak-to-peak inductor current ripple is:

EQUATION 5-8:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

EQUATION 5-9:

$$I_{L(PK)} = I_{OUT(MAX)} + 0.5 \times \Delta I_{L(PP)}$$

The saturation current rating is given by:

EQUATION 5-10:

$$I_{L(SAT)} = \frac{(R_{CL} \times I_{CL}) - V_{OFFSET}}{R_{DS(ON)}}$$

Where:

R_{CL}	Current-Limit Resistor
I_{CL}	Current-Limit Source Current
V_{OFFSET}	Current-Limit Comparator Offset
$R_{DS(ON)}$	On-Resistance of Low-Side Power MOSFET

The RMS inductor current is used to calculate the I^2R losses in the inductor.

EQUATION 5-11:

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^{2} + \frac{\Delta I_{L(PP)}^{2}}{12}}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high-frequency operation of the MIC2125/6 requires the use of ferrite materials. Lower cost iron powder cores may be used, but the increase in core loss reduces the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized, although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be significant. Core loss information is usually available from the magnetics vendor.

The amount of copper loss in the inductor is calculated by Equation 5-12:

EQUATION 5-12:

$$P_{INDUCTOR(CU)} = I_{L(RMS)}^{2} \times R_{WINDING}$$

5.4 Output Capacitor Selection

The type of the output capacitor is usually determined by its equivalent series resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are ceramic, tantalum, low-ESR aluminum electrolytic, OS-CON, and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR is calculated by Equation 5-13.

EQUATION 5-13:

$$ESR_{C_{OUT}} \le \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}}$$

Where:

$\Delta V_{OUT(PP)}$	Peak-to-Peak Output Voltage Ripple
$\Delta I_{L(PP)}$	Peak-to-Peak Inductor Current Ripple

The required output capacitance is calculated in Equation 5-14.

EQUATION 5-14:

$$C_{OUT} = \frac{\Delta I_{L(PP)}}{\Delta V_{OUT(PP)} \times f_{SW} \times 8}$$

Where:

C_{OUT}	Output Capacitance Value
f_{SW}	Switching Frequency

As described in the Theory of Operation subsection of the Functional Description, the MIC2125/26 requires at least 20 mV peak-to-peak ripple at the FB pin to ensure that the g_m amplifier and the comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide the enough feedback voltage ripple. Refer to the Ripple Injection subsection for details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated in Equation 5-15.

EQUATION 5-15:

$$I_{C_{OUT(RMS)}} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

EQUATION 5-16:

$$P_{DISS(COUT)} = I_{COUT(RMS)}{}^2 \times ESR_{COUT}$$

5.5 Input Capacitor Selection

The input capacitor reduces peak current drawn from the power supply and reduces noise and voltage ripple on the input. The input voltage ripple depends on the input capacitance and ESR. The input capacitance and ESR values are calculated by using Equation 5-17 and Equation 5-18.

EQUATION 5-17:

$$C_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{\eta \times \Delta V_{IN(C)} \times f_{SW}}$$

Where:

I_{OUT}	Load Current
η	Power Conversion Efficiency
$\Delta V_{IN(C)}$	Input Ripple Due to Capacitance Value

EQUATION 5-18:

$$ESR_{CIN} = \frac{\Delta V_{IN(ESR)}}{I_{L(PK)}}$$

Where:

$\Delta V_{IN(ESR)}$	Input Ripple Due to Capacitor ESR Value
$I_{L(PK)}$	Peak Inductor Current

The input capacitor should be qualified for ripple current rating and voltage rating. The RMS value of the input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

EQUATION 5-19:

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

The power dissipated in the input capacitor is:

EQUATION 5-20:

$$P_{DISS(CIN)} = I_{CIN(RMS)}{}^2 \times ESR_{CIN}$$

5.6 Output Voltage Setting

The MIC2125/26 requires two resistors to set the output voltage, as shown in Figure 5-3.

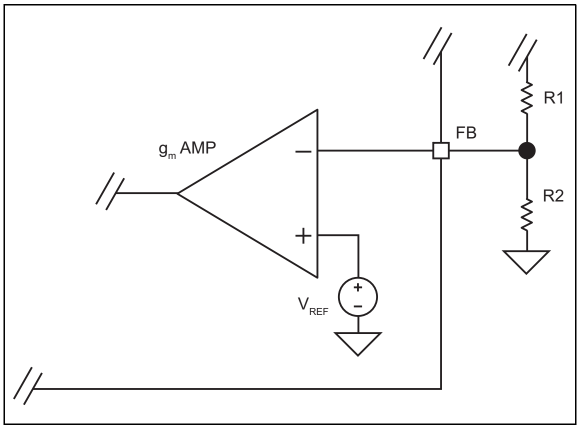


FIGURE 5-3: Voltage-Divider Configuration.

The output voltage is determined by Equation 5-21:

EQUATION 5-21:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

Where:

V_{FB} 0.6V

A typical value of R1 can be in the range of 3 kΩ and 15 kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using Equation 5-22.

EQUATION 5-22:

$$R2 = \frac{V_{FB} \times R1}{V_{OUT} - V_{FB}}$$

5.7 Output Overvoltage Limit Setting

The output overvoltage limit should be typically 20% higher than the nominal output voltage. Set the OVP limit by connecting a resistor divider from the output to ground as shown in Figure 5-4.

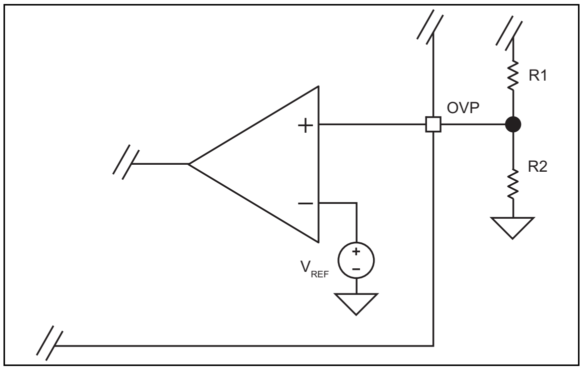


FIGURE 5-4: OVP Voltage-Divider Configuration.

Choose R2 in the range of 10 kΩ to 49.9 kΩ and calculate R1 using Equation 5-23.

EQUATION 5-23:

$$R1 = R2\left[\frac{V_{OVP}}{0.6} - 1\right]$$

5.8 Ripple Injection

The V_{FB} ripple required for proper operation of the MIC2125/6 g_m amplifier and comparator is 20 mV to 100 mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For low output voltages, such as a 1V, the output voltage ripple is only 10 mV to 20 mV, and the feedback voltage ripple is less than 20 mV. If the feedback voltage ripple is so small that the g_m amplifier and comparator cannot sense it, then the MIC2125/6 loses control and the output voltage is not regulated. In order to have sufficient V_{FB} ripple, a ripple injection method should be applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

- Enough ripple at the feedback voltage due to the large ESR of the output capacitors (Figure 5-5). The converter is stable without any ripple injection.

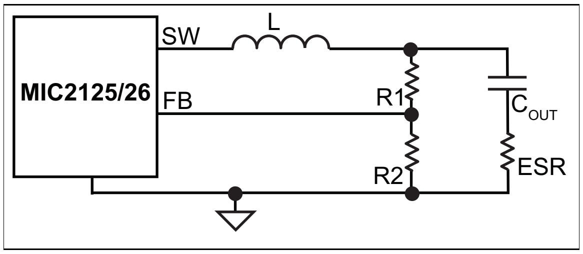


FIGURE 5-5: *Enough Ripple at FB.*

The feedback voltage ripple is:

EQUATION 5-24:

$$\Delta V_{FB(PP)} = \frac{R2}{R1 + R2} \times ESR_{C_{OUT}} \times \Delta I_{L(PP)}$$

Where:

$\Delta I_{L(PP)}$	Peak-to-Peak Value of the Inductor Current Ripple

- Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors.

  The output voltage ripple is fed into the FB pin through a feed-forward capacitor, C_{ff} in this situation, as shown in Figure 5-7. The typical C_{ff} value is between 1 nF and 100 nF.

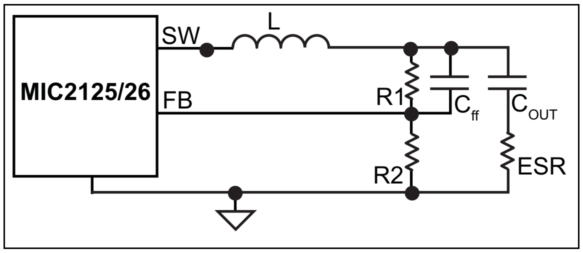


FIGURE 5-6: *Inadequate Ripple at FB.*

With the feed-forward capacitor, the feedback voltage ripple is very close to the output voltage ripple.

EQUATION 5-25:

$$\Delta V_{FB(PP)} \approx ESR \times \Delta I_{L(PP)}$$

- Virtually no ripple at the FB pin voltage due to the very low ESR of the output capacitors.

  Therefore, additional ripple is injected into the FB pin from the switching node SW via a resistor R_{INJ} and a capacitor C_{INJ}, as shown in Figure 5-7.

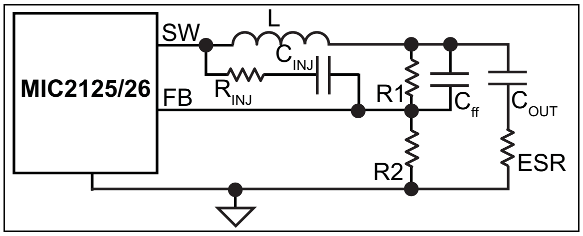


FIGURE 5-7: *Invisible Ripple at FB.*

The process of sizing the ripple injection resistor and capacitors is as follows.

- Select C_{INJ} as 100 nF, which can be considered as short for a wide range of the frequencies.
- Select C_{ff} to feed all output ripples into the feedback pin. Typical choice of C_{ff} is 0.47 nF to 47 nF, if R1 and R2 are in the kΩ range. The C_{ff} value can be calculated using Equation 5-26:

EQUATION 5-26:

$$C_{ff} \approx \frac{1}{R_P} \times \left(\frac{t_S \times V_{IN} \times D \times (1 - D)}{(V_{IN} \times D \times (1 - D)) - \Delta V_{FB(PP)}} \right)$$

Where:

V_{IN}	Power Stage Input Voltage
D	Duty Cycle
t_S	$1/f_{SW}$
R_P	$(R1//R2//R_{INJ})$
$\Delta V_{FB(PP)}$	Feedback Ripple

- Select R_{INJ} according to Equation 5-27.

EQUATION 5-27:

$$R_{INJ} = \frac{1}{C_{ff}} \times \left(\frac{V_{IN} \times D \times (1 - D)}{\Delta V_{FB(PP)} \times f_{SW}} \right)$$

6.0 PCB LAYOUT GUIDELINES

PCB layout is critical to achieve reliable, stable and efficient performance. The following guidelines should be followed to ensure proper operation of the MIC2125/26 converter.

6.1 IC

- The ceramic bypass capacitors which are connected to the V_{DD} and P_{VDD} pins must be located right at the IC. Use wide traces to connect to the V_{DD}, P_{VDD} and A_{GND}, P_{GND} pins respectively.
- The signal ground pin (A_{GND}) must be connected directly to the ground planes.
- Place the IC close to the point-of-load (POL).
- Signal and power grounds should be kept separate and connected at only one location.

6.2 Input Capacitor

- Place the input ceramic capacitors as close as possible to the MOSFETs.
- Place several vias to the ground plane close to the input capacitor ground terminal.

6.3 Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- The SW pin should be connected directly to the drain of the low-side MOSFET to accurately sense the voltage across the low-side MOSFET.

6.4 Output Capacitor

- Use a copper plane to connect the output capacitor ground terminal to the input capacitor ground terminal.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

6.5 MOSFETs

- MOSFET gate drive traces must be short. The ground plane should be the connection between the MOSFET source and P_{GND}.
- Choose a low-side MOSFET with a high C_{GS}/C_{GD} ratio and a low internal gate resistance to minimize the effect of d_V/d_t inducted turn-on.
- Use a 4.5V V_{GS} rated MOSFET. Its higher gate threshold voltage is more immune to glitches than a 2.5V or 3.3V rated MOSFET.

For more information about the Evaluation board layout, please contact Microchip sales.

7.0 PACKAGING INFORMATION

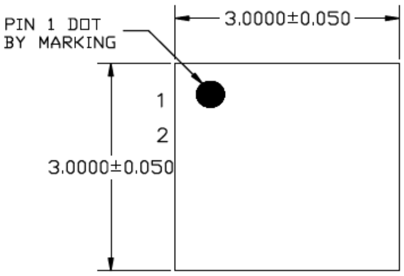
16-Lead QFN 3 mm x 3 mm Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

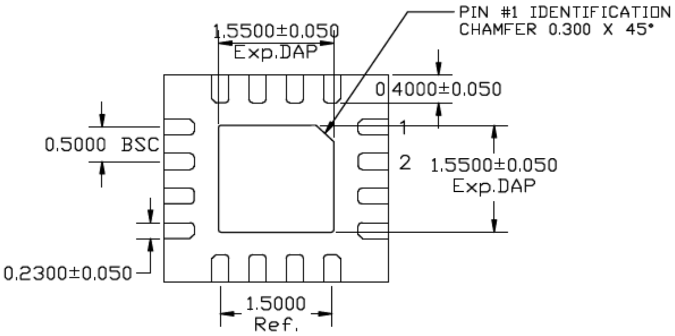
TITLE

16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

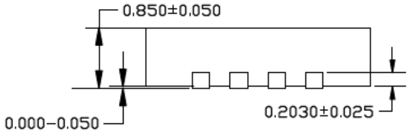
DRAWING #	QFN33-16LD-PL-1	**UNIT**	MM



TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3

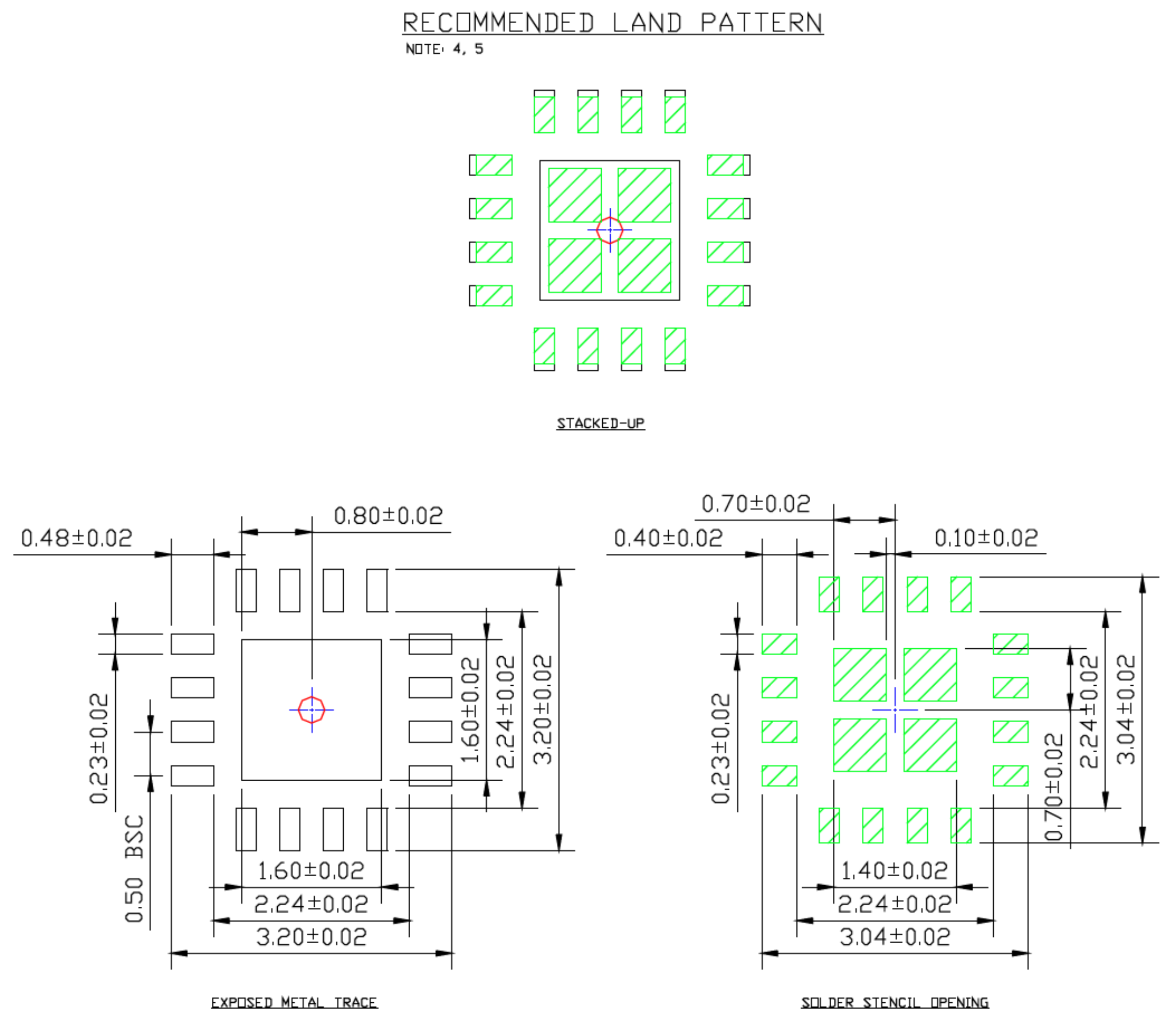


SIDE VIEW
NOTE: 1, 2, 3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

POD-Land Pattern drawing # QFN33-16LD-PL-1



APPENDIX A: REVISION HISTORY

Revision A (November 2015)

- Original Conversion of this Document.

Revision B (December 2015)

- Corrected the erroneous listing of the MIC2126 example with a 64LD package. Replaced with correct 16LD package information.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO. **X** **XX**

Device **Temperature** **Package**

Device:	MIC2125:	28V, Synchronous Buck Controller featuring Adaptive On-Time Control with HyperLight Load
	MIC2126:	28V, Synchronous Buck Controller featuring Adaptive On-Time Control with Hyper Speed Control
Temperature:	Y =	–40°C to +125°C
Package:	ML =	16-Pin 3 mm x 3 mm QFN

Examples:

a)	MIC2125YML:	28V, Synchronous Buck Controller featuring Adaptive On-Time Control with HyperLight Load, –40°C to +125°C junction temperature range, 16LD QFN
b)	MIC2126YML:	28V, Synchronous Buck Controller featuring Adaptive On-Time Control with Hyper Speed Control, –40°C to +125°C junction temperature range, 16LD QFN

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