Data Sheet, Feb. 2003

C515C

8-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

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Page	Subjects (major changes since last revision)

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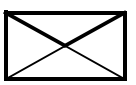


Features

- Full upward compatibility with SAB 80C515A
- On-chip program memory (with optional memory protection)
  - C515C-8R 64 Kbytes on-chip ROM
  - C515C-8E 64 Kbytes on-chip OTP
  - alternatively up to 64 Kbytes external program memory
- 256 bytes on-chip RAM
- 2 Kbytes of on-chip XRAM
- Up to 64 Kbytes external data memory
- Superset of the 8051 architecture with 8 datapointers
- Up to 10 MHz external operating frequency (1 µs instruction cycle time at 6 MHz external clock)
- On-chip emulation support logic (Enhanced Hooks Technology)
- Current optimized oscillator circuit and EMI optimized design

(further features are on next page)

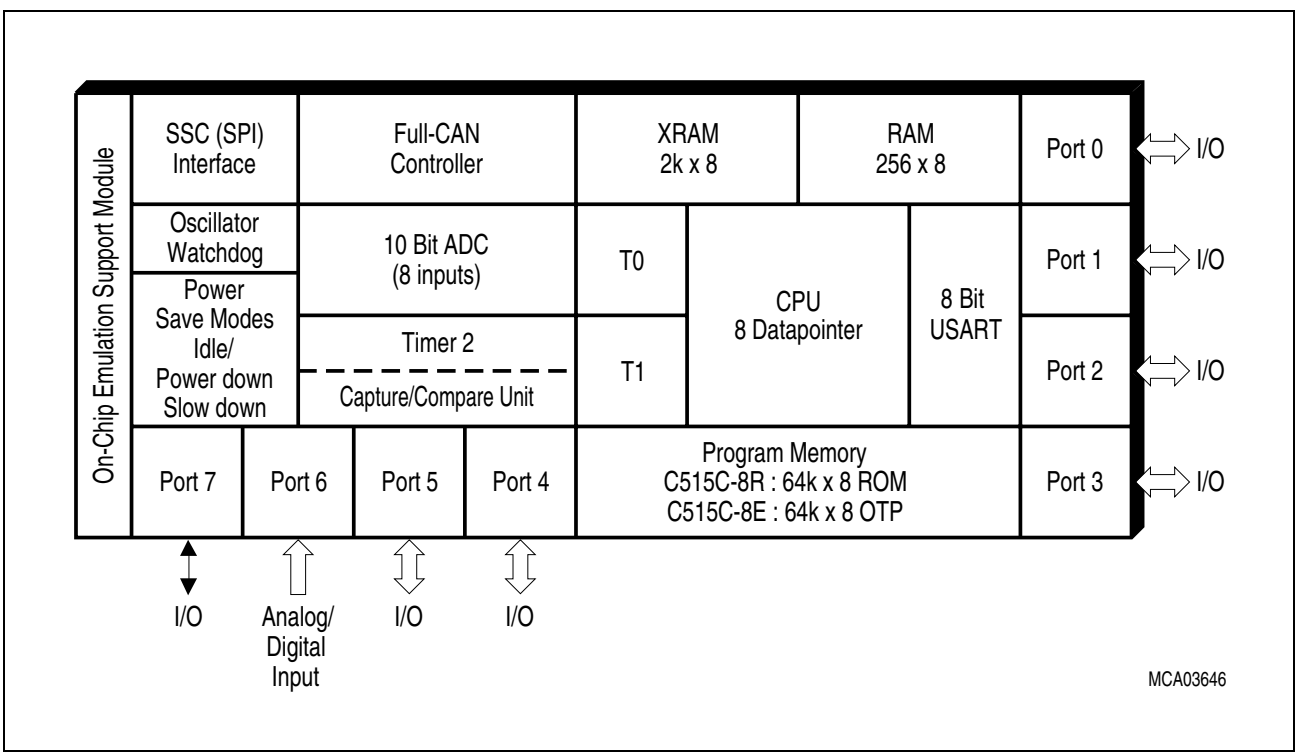


Figure 1 C515C Functional Units

- Eight ports: 48 + 1 digital I/O lines, 8 analog inputs
  - Quasi-bidirectional port structure (8051 compatible)
  - Port 5 selectable for bidirectional port structure (CMOS voltage levels)
- Full-CAN controller on-chip
  - 256 register/data bytes are located in external data memory area
  - max. 1 MBaud at 8 - 10 MHz operating frequency
- Three 16-bit timer/counters
  - Timer 2 can be used for compare/capture functions
- 10-bit A/D converter with multiplexed inputs and built-in self calibration
- Full duplex serial interface with programmable baudrate generator (USART)
- SSC synchronous serial interface (SPI compatible)
  - Master and slave capable
  - Programmable clock polarity/clock-edge to data phase relation
  - LSB/MSB first selectable
  - 2.5 MHz transfer rate at 10 MHz operating frequency
- Seventeen interrupt vectors, at four priority levels selectable
- Extended watchdog facilities
  - 15-bit programmable watchdog timer
  - Oscillator watchdog
- Power saving modes
  - Slow-down mode
  - Idle mode (can be combined with slow-down mode)
  - Software power-down mode with wake-up capability through $\overline{\text{INT0}}$ or RXDC pin
  - Hardware power-down mode
- CPU running condition output pin
- ALE can be switched off
- Multiple separate V_{DD}/V_{SS} pin pairs
- P-MQFP-80-1 package
- Temperature Ranges:
  SAB-C515C versions: T_A = 0 to 70 °C
  SAF-C515C versions: T_A = -40 to 85 °C
  SAH-C515C versions: T_A = -40 to 110 °C

Note: Versions for extended temperature range -40 °C to 110 °C (SAH-C515C) are available on request.

The C515C is an enhanced, upgraded version of the SAB 80C515A 8-bit microcontroller which additionally provides a full CAN interface, a SPI compatible synchronous serial interface, extended power save provisions, additional on-chip RAM, 64K of on-chip program memory, two new external interrupts and RFI related improvements. With a maximum external clock rate of 10 MHz it achieves a 600 ns instruction cycle time (1 µs at 6 MHz).

The C515C-8R contains a non-volatile 64 Kbytes read-only program memory. The C515C-L is identical to the C515C-8R, except that it lacks the on-chip program memory. The C515C-8E is the OTP version in the C515C microcontroller with an on-chip 64 Kbytes one-time programmable (OTP) program memory. The C515C is mounted in a P-MQFP-80-1 package.

If compared to the C515C-8R and C515C-L, the C515C-8E OTP version additionally provides two features:

- The wake-up from software power down mode can, additionally to the external pin P3.2/$\overline{\text{INT0}}$ wake-up capability, also be triggered alternatively by a second pin P4.7/RXDC.
- For power consumption reasons the on-chip CAN controller can be switched off.

Table 1 Differences in Internal Program Memory of the C505 MCUs

Device	Internal Program Memory	
	ROM	**OTP**
C515C-LM	–	–
C515C-8RM	64 Kbytes	–
C515C-8EM	–	64 Kbytes

Note: The term C515C refers to all versions described within this document unless otherwise noted.

Ordering Information

The ordering code for Infineon Technologies' microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set
- The specified temperature rage
- The package and the type of delivery

For the available ordering codes for the C515C please refer to the "**Product information Microcontrollers**", which summarizes all available microcontroller variants.

Note: The ordering codes for the Mask-ROM versions are defined for each product after verification of the respective ROM code.

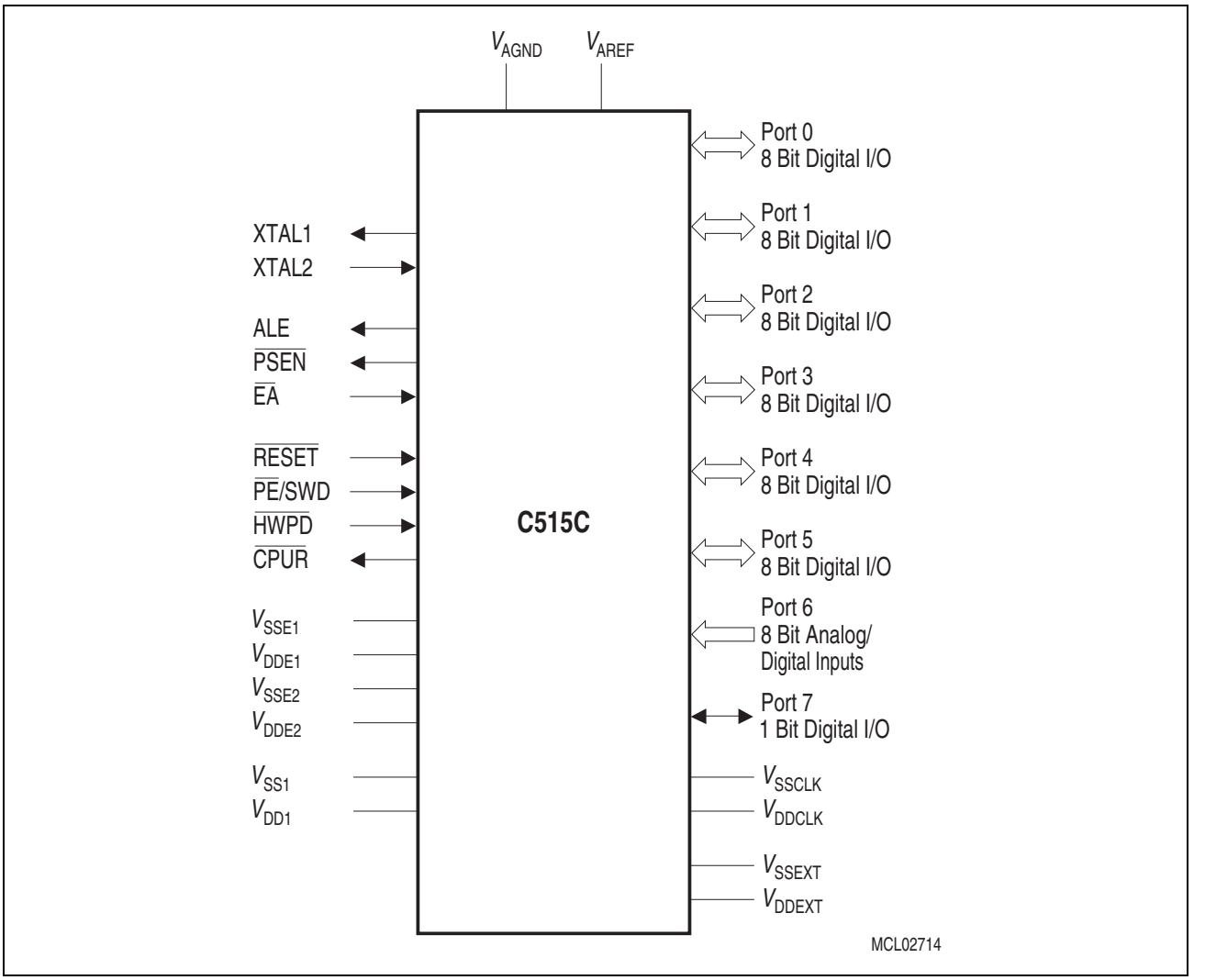


Figure 2 Logic Symbol

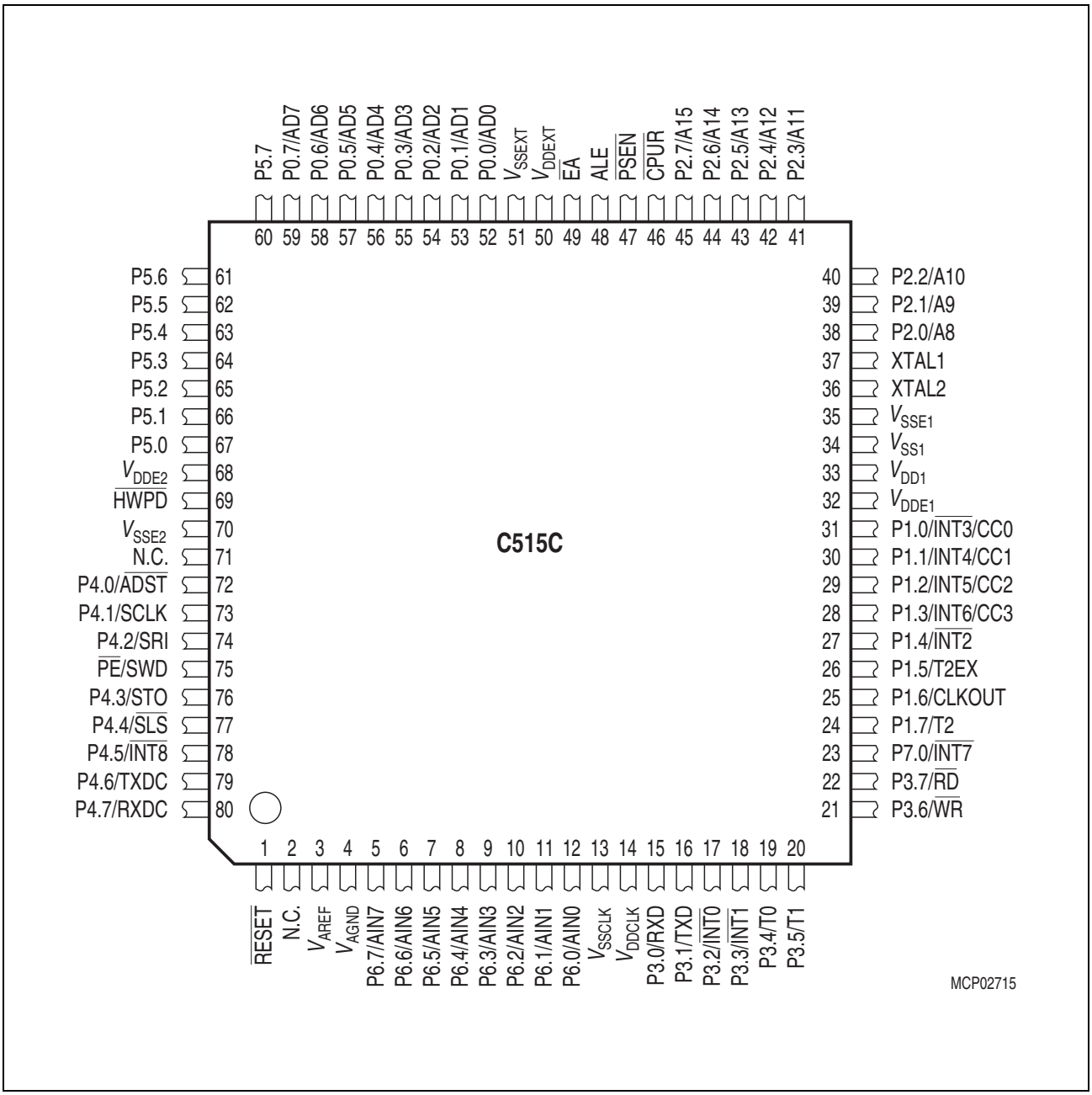


Figure 3 C515C Pin Configuration P-MQFP-80-1 (top view)

Table 2 Pin Definitions and Functions

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
$\overline{\text{RESET}}$	1	I	**$\overline{\text{RESET}}$** A low level on this pin for the duration of two machine cycles while the oscillator is running resets the C515C. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	3	–	**Reference voltage** for the A/D converter
V_{AGND}	4	–	**Reference ground** for the A/D converter
P6.0-P6.7	12-5	I	**Port 6** is an 8-bit unidirectional input port to the A/D converter. Port pins can be used for digital input, if voltage levels simultaneously meet the specifications high/low input voltages and for the eight multiplexed analog inputs.
P7.0 / $\overline{\text{INT7}}$	23	I/O	**Port 7** is an 1-bit quasi-bidirectional I/O port with internal pull-up resistor. When a 1 is written to P7.0 it is pulled high by an internal pull-up resistor, and in that state can be used as input. As input, P7.0 being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistor. If P7.0 is used as interrupt input, its output latch must be programmed to a one (1). The secondary function is assigned to the port 7 pin as follows: P7.0 $\overline{\text{INT7}}$, Interrupt 7 input

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
P3.0-P3.7	15-22	I/O	**Port 3** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:
	15		P3.0 RXD — Receiver data input (asynch.) or data input/output (synch.) of serial interface
	16		P3.1 TXD — Transmitter data output (asynch.) or clock output (synch.) of serial interface
	17		P3.2 $\overline{INT0}$ — External interrupt 0 input / timer 0 gate control input
	18		P3.3 $\overline{INT1}$ — External interrupt 1 input / timer 1 gate control input
	19		P3.4 T0 — Timer 0 counter input
	20		P3.5 T1 — Timer 1 counter input
	21		P3.6 $\overline{WR}$ — $\overline{WR}$ control output; latches the data byte from port 0 into the external data memory
	22		P3.7 $\overline{RD}$ — $\overline{RD}$ control output; enables the external data memory

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
P1.0 - P1.7	31-24	I/O	**Port 1** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. The port is used for the low-order address byte during program verification. Port 1 also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: 31 P1.0 $\overline{\text{INT3}}$ CC0 Interrupt 3 input / compare 0 output / capture 0 input 30 P1.1 INT4 CC1 Interrupt 4 input / compare 1 output / capture 1 input 29 P1.2 INT5 CC2 Interrupt 5 input / compare 2 output / capture 2 input 28 P1.3 INT6 CC3 Interrupt 6 input / compare 3 output / capture 3 input 27 P1.4 $\overline{\text{INT2}}$ Interrupt 2 input 26 P1.5 T2EX Timer 2 external reload / trigger input 25 P1.6 CLKOUT System clock output 24 P1.7 T2 Counter 2 input
XTAL2	36	I	**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
XTAL1	37	O	**XTAL1** Output of the inverting oscillator amplifier.
P2.0-P2.7	38-45	I/O	**Port 2** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing 1's. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{CPUR}}$	46	O	**CPU Running Condition** This output pin is at low level when the CPU is running and program fetches or data accesses in the external data memory area are executed. In idle mode, hardware and software power down mode, and with an active $\overline{\text{RESET}}$ signal $\overline{\text{CPUR}}$ is set to high level. $\overline{\text{CPUR}}$ can be typically used for switching external memory devices into power saving modes.
$\overline{\text{PSEN}}$	47	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. The signal remains high during internal program execution.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
ALE	48	O	The **Address Latch Enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods, except during an external data memory access. ALE can be switched off when the program is executed internally.
$\overline{EA}$	49	I	**$\overline{\text{External Access Enable}}$** When held high, the C515C executes instructions always from the internal ROM. When held low, the C515C fetches all instructions from external program memory. *Note: For the ROM protection version $\overline{EA}$ pin is latched during reset.*
P0.0-P0.7	52-59	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the C515C. External pullup resistors are required during program verification.
P5.0-P5.7	67-60	I/O	**Port 5** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 5 can also be switched into a bidirectional mode, in which CMOS levels are provided. In this bidirectional mode, each port 5 pin can be programmed individually as input or output.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
$\overline{\text{HWPD}}$	69	I	**$\overline{\text{Hardware Power Down}}$** A low level on this pin for the duration of one machine cycle while the oscillator is running resets the C515C. A low level for a longer period will force the part to power down mode with the pins floating.
P4.0-P4.7	72-74, 76-80	I/O	**Port 4** is an 8-bit quasi-bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1's written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. P4 also contains the external A/D converter control pin, the SSC pins, the CAN controller input/output lines, and the external interrupt 8 input. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The alternate functions are assigned to port 4 as follows: 72 P4.0 $\overline{\text{ADST}}$ External A/D converter start pin 73 P4.1 SCLK SSC Master Clock Output / SSC Slave Clock Input 74 P4.2 SRI SSC Receive Input 76 P4.3 STO SSC Transmit Output 77 P4.4 $\overline{\text{SLS}}$ Slave Select Input 78 P4.5 $\overline{\text{INT8}}$ External interrupt 8 input 79 P4.6 TXDC Transmitter output of the CAN controller 80 P4.7 RXDC Receiver input of the CAN controller

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
$\overline{PE}$/SWD	75	I	**$\overline{Power\ saving\ mode\ enable}$ / Start watchdog timer** A low level on this pin allows the software to enter the power down, idle and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default. Use of the software controlled power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor.
V_{SSCLK}	13	–	**Ground (0 V) for on-chip oscillator** This pin is used for ground connection of the on-chip oscillator circuit.
V_{DDCLK}	14	–	**Supply voltage for on-chip oscillator** This pin is used for power supply of the on-chip oscillator circuit.
V_{DDE1} V_{DDE2}	32 68	–	**Supply voltage for I/O ports** These pins are used for power supply of the I/O ports during normal, idle, and power down mode.
V_{SSE1} V_{SSE2}	35 70	–	**Ground (0 V) for I/O ports** These pins are used for ground connections of the I/O ports during normal, idle, and power down mode.
V_{DD1}	33	–	**Supply voltage for internal logic** This pins is used for the power supply of the internal logic circuits during normal, idle, and power down mode.
V_{SS1}	34	–	**Ground (0 V) for internal logic** This pin is used for the ground connection of the internal logic circuits during normal, idle, and power down mode.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
V_{DDEXT}	50	–	**Supply voltage for external access pins** This pin is used for power supply of the I/O ports and control signals which are used during external accesses (for Port 0, Port 2, ALE, $\overline{PSEN}$, P3.6/$\overline{WR}$, and P3.7/$\overline{RD}$).
V_{SSEXT}	51	–	**Ground (0 V) for external access pins** This pin is used for the ground connection of the I/O ports and control signals which are used during external accesses (for Port 0, Port 2, ALE, $\overline{PSEN}$, P3.6/$\overline{WR}$, and P3.7/$\overline{RD}$).
N.C.	2, 71	–	**Not connected** These pins should not be connected.

1) I = Input; O = Output

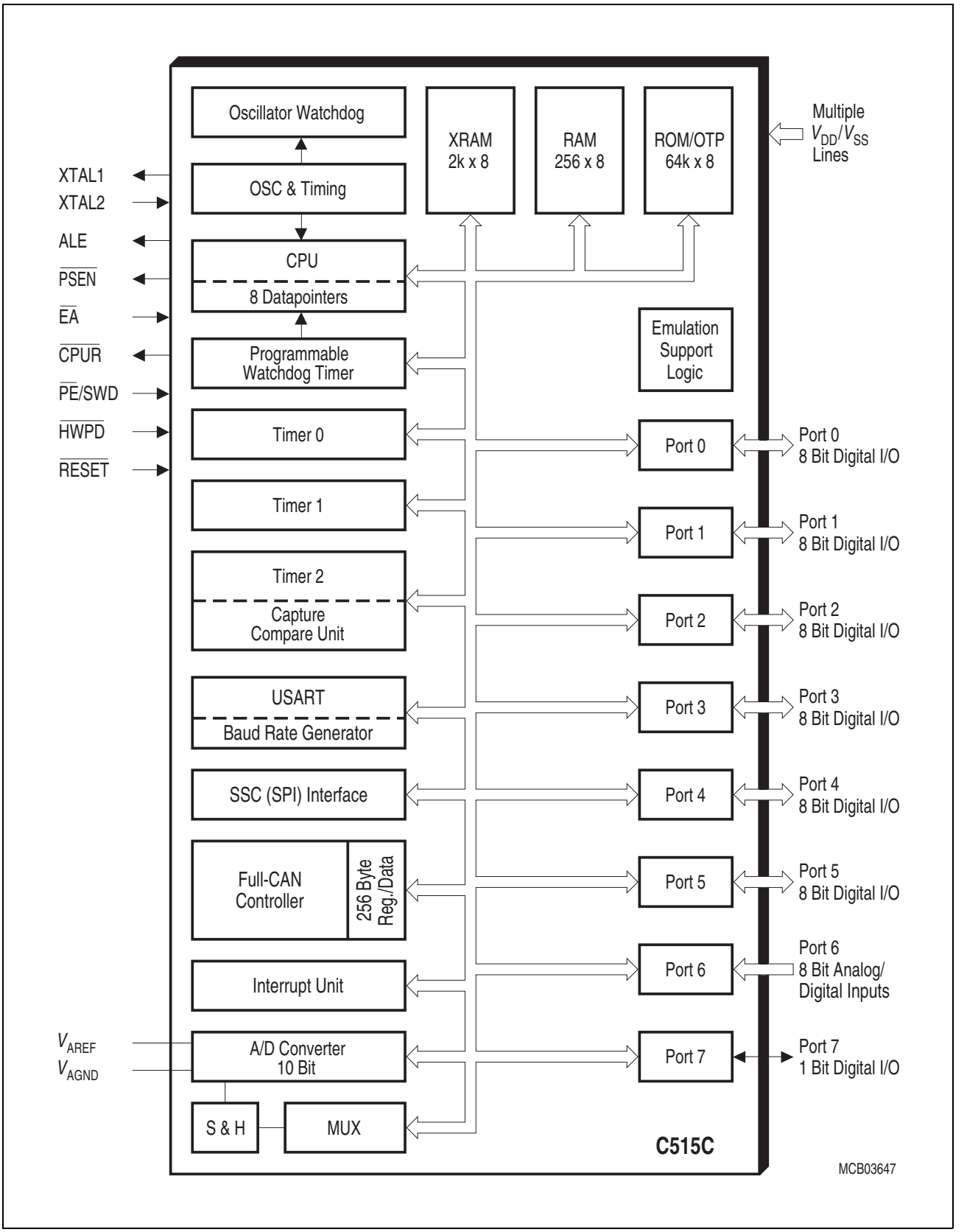


Figure 4 Block Diagram of the C515C

CPU

The C515C is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 6 MHz crystal, 58% of the instructions are executed in 1 µs (10 MHz: 600 ns).

PSW

Special Function Register (D0$_H$) Reset Value: 00$_H$

Bit No.	MSB							LSB	
	D7$_H$	D6$_H$	D5$_H$	D4$_H$	D3$_H$	D2$_H$	D1$_H$	D0$_H$	
D0$_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	Carry Flag Used by arithmetic instruction.
AC	Auxiliary Carry Flag Used by instructions which execute BCD operations.
F0	General Purpose Flag
RS1 RS0	Register Bank select control bits These bits are used to select one of the four register banks.
OV	Overflow Flag Used by arithmetic instruction.
F1	General Purpose Flag
P	Parity Flag Set/cleared by hardware after each instruction to indicate an odd/even number of “one” bits in the accumulator, i.e. even parity.

RS1	RS0	Function
0	0	Bank 0 selected, data address 00$_H$-07$_H$
0	1	Bank 1 selected, data address 08$_H$-0F$_H$
1	0	Bank 2 selected, data address 10$_H$-17$_H$
1	1	Bank 3 selected, data address 18$_H$-1F$_H$

Memory Organization

The C515C CPU manipulates data and operands in the following five address spaces:

- up to 64 Kbytes of internal/external program memory
- up to 64 Kbytes of external data memory
- 256 bytes of internal data memory
- 256 bytes CAN controller registers / data memory
- 2 Kbytes of internal XRAM data memory
- a 128 byte special function register area

Figure 5 illustrates the memory address spaces of the C515C.

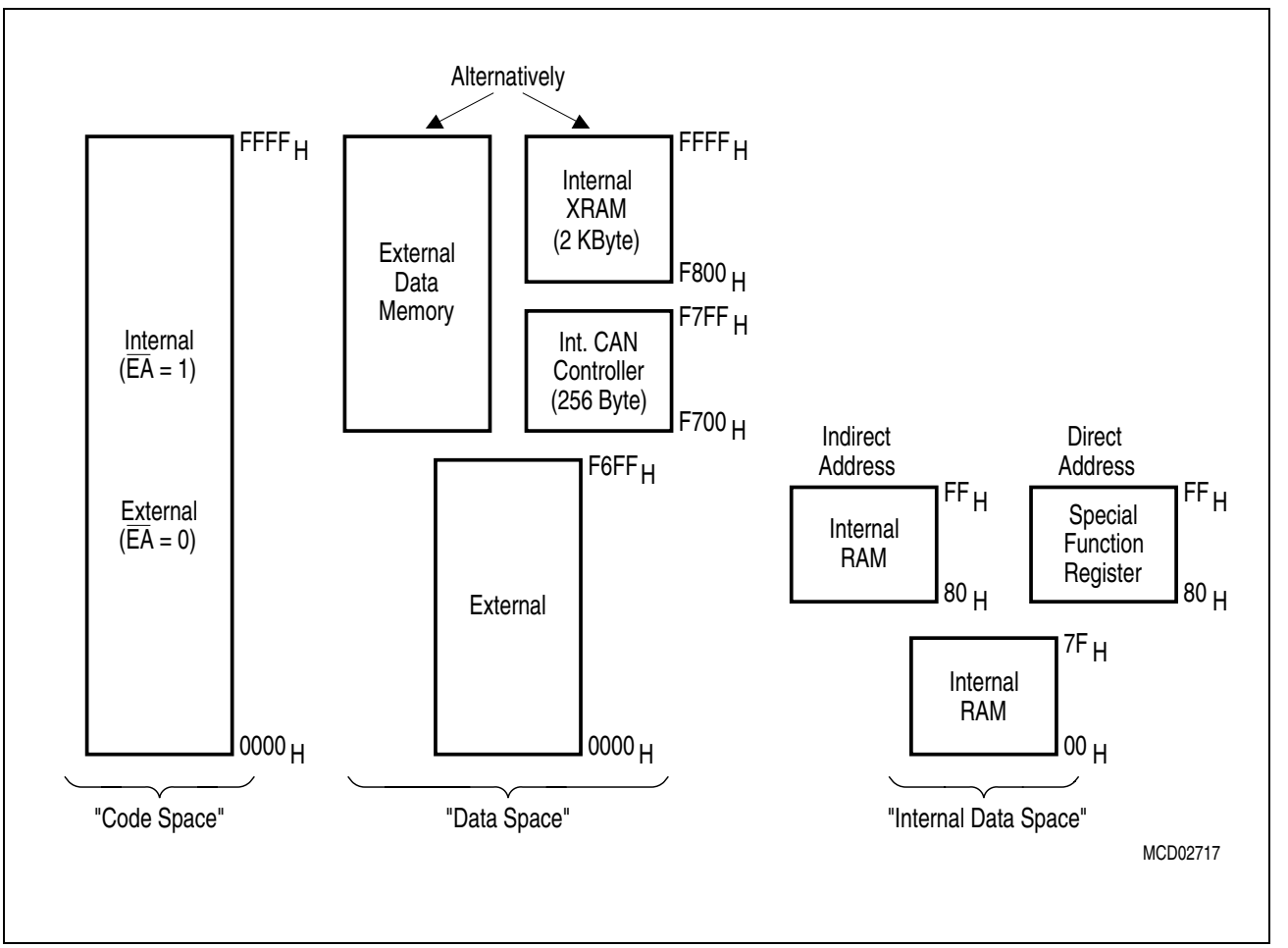


Figure 5 C515C Memory Map

Control of XRAM/CAN Controller Access

The XRAM in the C515C is a memory area that is logically located at the upper end of the external memory space, but is integrated on the chip. Because the XRAM and the CAN controller is used in the same way as external data memory the same instruction types (MOVX) must be used for accessing the XRAM. Two bits in SFR SYSCON, XMAP0 and XMAP1, control the accesses to the XRAM and the CAN controller.

SYSCON
Special Function Register **($B1_H$)** **C515C-8R Reset Value: $X010XX01_B$**
C515C-8E Reset Value: $X010X001_B$

Bit No.	MSB							LSB	
	7	6	5	4	3	2	1	0	
$B1_H$	–	PMOD	EALE	RMAP	–	CSWO	XMAP1	XMAP0	SYSCON

The function of the shaded bits is not described in this section.

Bit	Function
XMAP1	XRAM/CAN controller visible access control Control bit for $\overline{RD}$/$\overline{WR}$ signals during XRAM/CAN Controller accesses. If addresses are outside the XRAM/CAN controller address range or if XRAM is disabled, this bit has no effect. XMAP1 = 0: The signals $\overline{RD}$ and $\overline{WR}$ are not activated during accesses to the XRAM/CAN Controller XMAP1 = 1: Ports 0, 2 and the signals $\overline{RD}$ and $\overline{WR}$ are activated during accesses to XRAM/CAN Controller. In this mode, address and data information during XRAM/CAN Controller accesses are visible externally.
XMAP0	Global XRAM/CAN controller access enable/disable control XMAP0 = 0: The access to XRAM and CAN controller is enabled. XMAP0 = 1: The access to XRAM and CAN controller is disabled (default after reset). All MOVX accesses are performed via the external bus. Further, this bit is hardware protected.

Bit XMAP0 is hardware protected. If it is reset once (XRAM/CAN controller access enabled) it cannot be set by software. Only a reset operation will set the XMAP0 bit again.

The XRAM/CAN controller can be accessed by read/write instructions (MOVX A,DPTR, MOVX @DPTR,A), which use the 16-bit DPTR for indirect addressing. For accessing the XRAM or CAN controller, the effective address stored in DPTR must be in the range of $F700_H$ to $FFFF_H$.

The XRAM can be also accessed by read/write instructions (MOVX A,@Ri, MOVX @Ri,A), which use only an 8-bit address (indirect addressing with registers R0 or R1). Therefore, a special page register XPAGE which provides the upper address information (A8-A15) during 8-bit XRAM accesses. The behaviour of Port 0 and P2 during a MOVX access depends on the control bits XMAP0 and XMAP1 in register SYSCON and on the state of pin $\overline{EA}$. **Table 3** lists the various operating conditions.

Table 3 Behaviour of P0/P2 and $\overline{RD}/\overline{WR}$ During MOVX Accesses

			XMAP1, XMAP0		
			00	**10**	**X1**
$\overline{EA}$ = 0	MOVX @DPTR	DPTR < XRAM/CAN address range	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		DPTR ≥ XRAMCAN address range	a) P0/P2→Bus ($\overline{RD}/\overline{WR}$-Data) b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→Bus ($\overline{RD}/\overline{WR}$-Data) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
	MOVX @ Ri	XPAGE < XRAMCAN addr. page range	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		XPAGE ≥ XRAMCAN addr. page range	a) P0→Bus ($\overline{RD}/\overline{WR}$-Data) P2→I/O b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0→Bus ($\overline{RD}/\overline{WR}$-Data only) P2→I/O b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
$\overline{EA}$ = 1	MOVX @DPTR	DPTR < XRAM/CAN address range	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		DPTR ≥ XRAMCAN address range	a) P0/P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→Bus ($\overline{RD}/\overline{WR}$-Data) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
	MOVX @ Ri	XPAGE < XRAMCAN addr. page range	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		XPAGE ≥ XRAMCAN addr. page range	a) P2→I/O P0/P2→I/O b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0→Bus ($\overline{RD}/\overline{WR}$-Data) P2→I/O b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used

modes compatible to 8051/C501 family

Reset and System Clock

The reset input is an active low input at pin $\overline{\text{RESET}}$. Since the reset is synchronized internally, the $\overline{\text{RESET}}$ pin must be held low for at least two machine cycles (12 oscillator periods) while the oscillator is running. A pullup resistor is internally connected to V_{DD} to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when V_{DD} is applied by connecting the $\overline{\text{RESET}}$ pin to V_{SS} via a capacitor. **Figure 6** shows the possible reset circuitries.

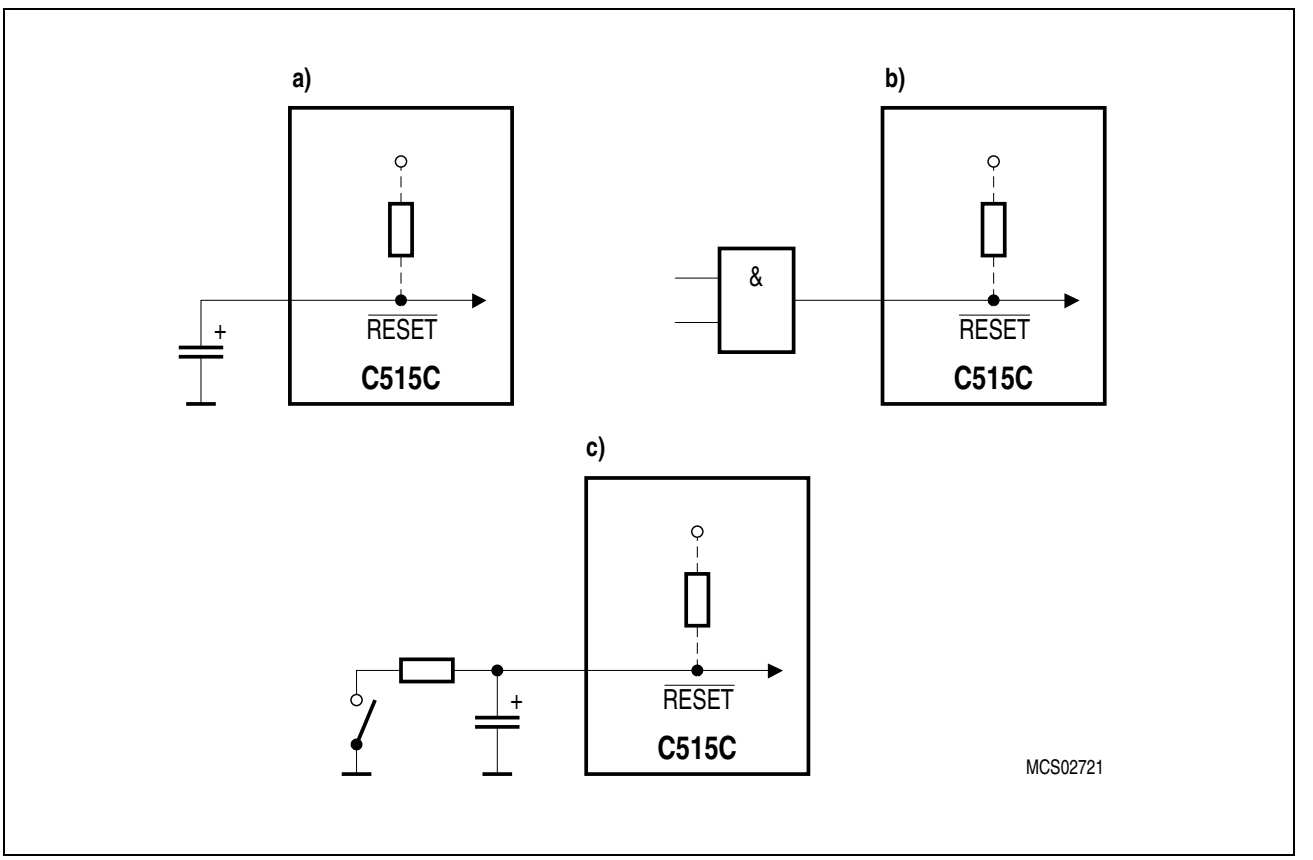


Figure 6 Reset Circuitries

Figure 7 shows the recommended oscillator circiutries for crystal and external clock operation.

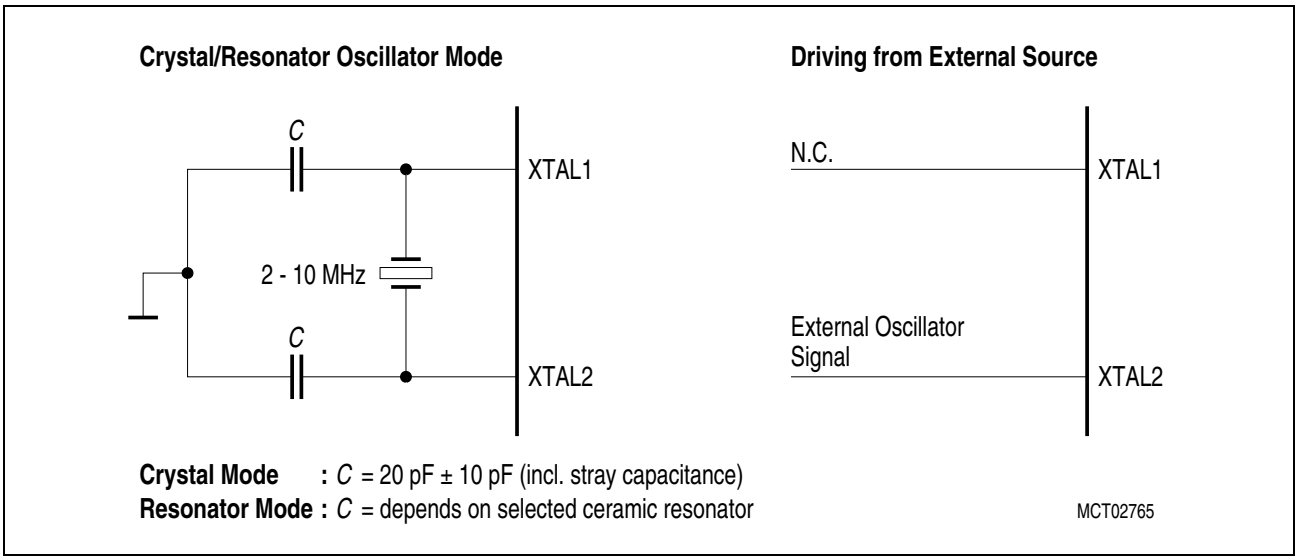


Figure 7 Recommended Oscillator Circuitries

Multiple Datapointers

As a functional enhancement to the standard 8051 architecture, the C515C contains eight 16-bit datapointers instead of only one datapointer. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointer is done in the special function register DPSEL. **Figure 8** illustrates the datapointer addressing mechanism.

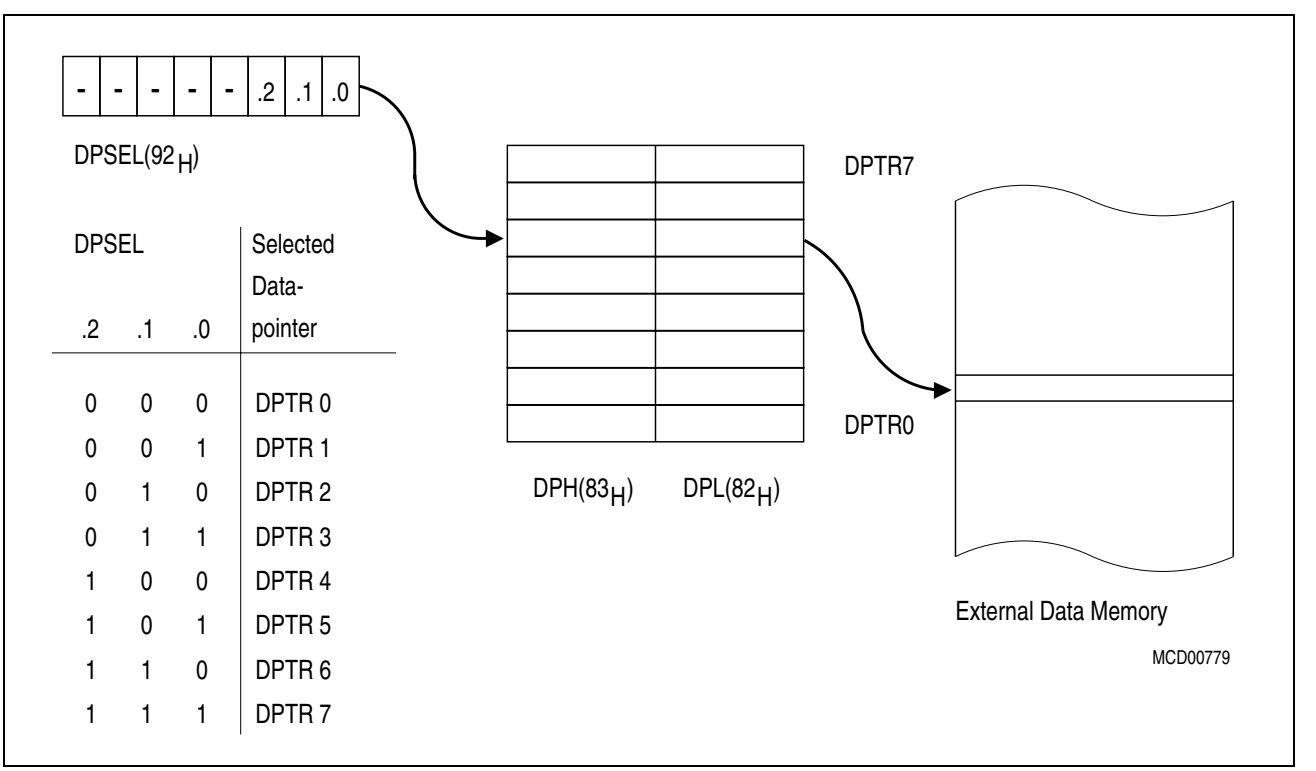


Figure 8 External Data Memory Addressing using Multiple Datapointers

Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the support of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology, which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

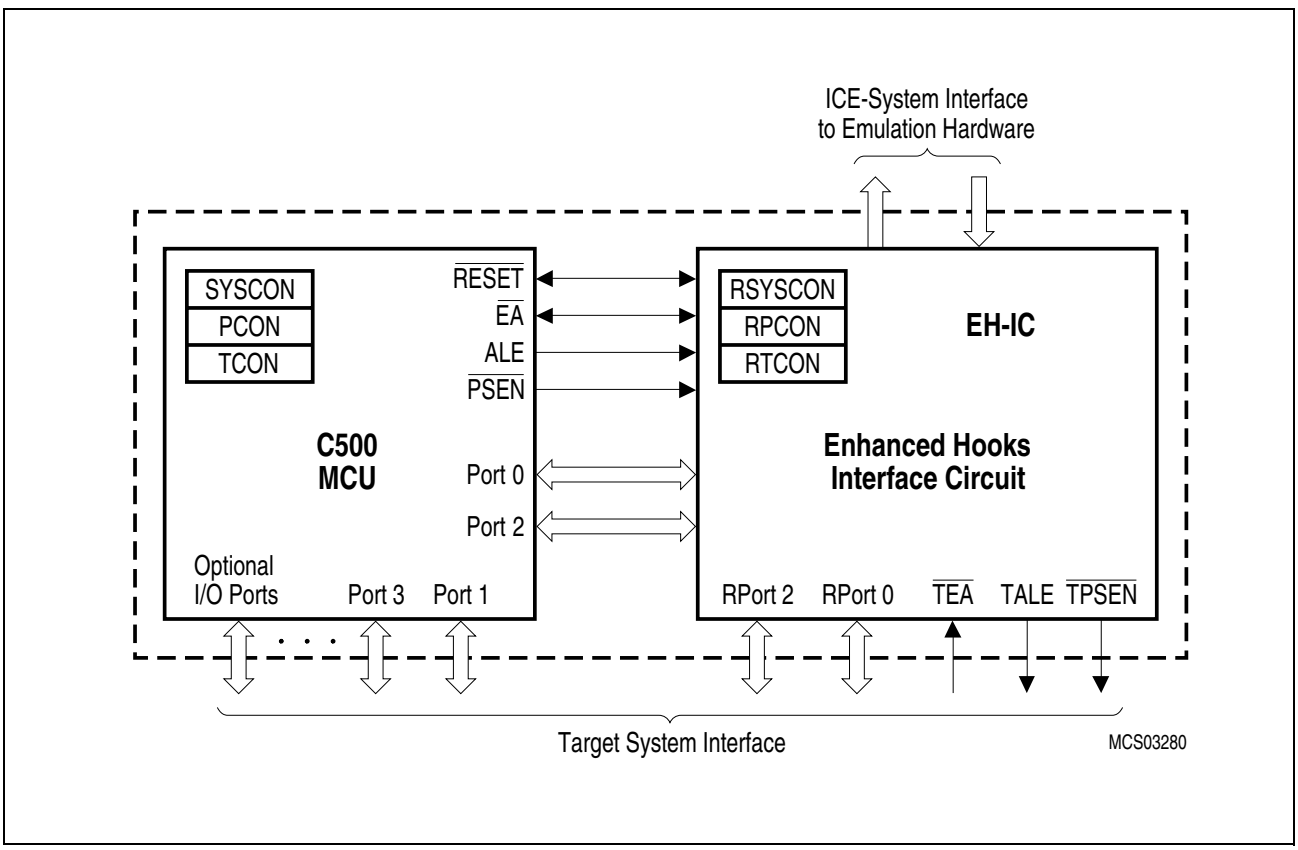


Figure 9 Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the program execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

Special Function Registers

The registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function register area consists of two portions: the standard special function register area and the mapped special function register area. Two special function registers of the C515C (PCON1 and DIR5) are located in the mapped special function register area. For accessing the mapped special function register area, bit RMAP in special function register SYSCON must be set. All other special function registers are located in the standard special function register area which is accessed when RMAP is cleared (“0”). As long as bit RMAP is set, mapped special function register area can be accessed. This bit is not cleared by hardware automatically. Thus, when non-mapped/mapped registers are to be accessed, the bit RMAP must be cleared/set by software, respectively each.

SYSCON
Special Function Register **($B1_H$)** **C515C-8R Reset Value: $X010XX01_B$**
C515C-8E Reset Value: $X010X001_B$

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B1_H$	–	PMOD	EALE	RMAP	–	CSWO	XMAP1	XMAP0	SYSCON

The function of the shaded bits is not described in this section.

Bit	Function
RMAP	Special function register map bit RMAP = 0: The access to the non-mapped (standard) special function register area is enabled (reset value). RMAP = 1: The access to the mapped special function register area is enabled.

The 59 special function registers (SFRs) in the standard and mapped SFR area include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. The SFRs of the C515C are listed in **Table 4** and **Table 5**. In **Table 4** they are organized in groups which refer to the functional blocks of the C515C. The CAN-SFRs are also included in **Table 4**. **Table 5** illustrates the contents of the SFRs in numeric order of their addresses. **Table 6** list the CAN-SFRs in numeric order of their addresses.

Table 4 Special Function Registers - Functional Block

Block	Symbol	Name	Addr	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$**[2]	00_H
	B	B-Register	**$F0_H$**[2]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	92_H	$XXXXX000_B$[3]
	PSW	Program Status Word Register	**$D0_H$**[2]	00_H
	SP	Stack Pointer	81_H	07_H
	SYSCON[1]	System Control Register C515C-8R	$B1_H$	$X010XX01_B$[3]
		C515C-8E	$B1_H$	$X010X001_B$[3]
A/D-Converter	ADCON0[1]	A/D Converter Control Register 0	**$D8_H$**[2]	00_H
	ADCON1	A/D Converter Control Register 1	DC_H	$0XXXX000_B$[3]
	ADDATH	A/D Converter Data Register High Byte	$D9_H$	00_H
	ADDATL	A/D Converter Data Register Low Byte	DA_H	$00XXXXXX_B$[3]
Interrupt System	IEN0[1]	Interrupt Enable Register 0	**$A8_H$**[2]	00_H
	IEN1[1]	Interrupt Enable Register 1	**$B8_H$**[2]	00_H
	IEN2	Interrupt Enable Register 2	$9A_H$	$XX00X00X_B$[3]
	IP0[1]	Interrupt Priority Register 0	$A9_H$	00_H
	IP1	Interrupt Priority Register 1	$B9_H$	$0X000000_B$[3]
	TCON[1]	Timer Control Register	**88_H**[2]	00_H
	T2CON[1]	Timer 2 Control Register	**$C8_H$**[2]	00_H
	SCON[1]	Serial Channel Control Register	**98_H**[2]	00_H
	IRCON	Interrupt Request Control Register	**$C0_H$**[2]	00_H
XRAM	XPAGE	Page Address Register for Extended on-chip XRAM and CAN Controller	91_H	00_H
	SYSCON[1]	System Control Register C515C-8R	$B1_H$	$X010XX01_B$[3]
		C515C-8E	$B1_H$	$X010X001_B$[3]
Ports	P0	Port 0	**80_H**[2]	FF_H
	P1	Port 1	**90_H**[2]	FF_H
	P2	Port 2	**$A0_H$**[2]	FF_H
	P3	Port 3	**$B0_H$**[2]	FF_H
	P4	Port 4	**$E8_H$**[2]	FF_H
	P5	Port 5	**$F8_H$**[2]	FF_H
	DIR5	Port 5 Direction Register	**$F8_H$**[2][4]	FF_H
	P6	Port 6, Analog/Digital Input	DB_H	–
	P7	Port 7	FA_H	$XXXXXXX1_B$[3]
	SYSCON[1]	System Control Register C515C-8R	$B1_H$	$X010XX01_B$[3]
		C515C-8E		$X010X001_B$[3]
Watchdog	WDTREL	Watchdog Timer Reload Register	86_H	00_H
	IEN0[1]	Interrupt Enable Register 0	**$A8_H$**[2]	00_H
	IEN1[1]	Interrupt Enable Register 1	**$B8_H$**[2]	00_H
	IP0[1]	Interrupt Priority Register 0	$A9_H$	00_H

Table 4 Special Function Registers - Functional Block (cont'd)

Block	Symbol	Name	Addr	Contents after Reset
Serial Channel	ADCON0[1]	A/D Converter Control Register 0	**$D8_H$**[2]	00_H
	PCON[1]	Power Control Register	87_H	00_H
	SBUF	Serial Channel Buffer Register	99_H	XX_H[3]
	SCON	Serial Channel Control Register	**98_H**[2]	00_H
	SRELL	Serial Channel Reload Register, low byte	AA_H	$D9_H$
	SRELH	Serial Channel Reload Register, high byte	BA_H	$XXXXXX11_B$[3]
CAN Controller	CR	Control Register	$F700_H$	101_H
	SR	Status Register	$F701_H$	XX_H[6]
	IR	Interrupt Register	$F702_H$	XX_H[6]
	BTR0	Bit Timing Register Low	$F704_H$	UU_H[6]
	BTR1	Bit Timing Register High	$F705_H$	$0UUUUUUU_B$[6]
	GMS0	Global Mask Short Register Low	$F706_H$	UU_H[6]
	GMS1	Global Mask Short Register High	$F707_H$	$UUU11111_B$[6]
	UGML0	Upper Global Mask Long Register Low	$F708_H$	UU_H[6]
	UGML1	Upper Global Mask Long Register High	$F709_H$	UU_H[6]
	LGML0	Lower Global Mask Long Register Low	$F70A_H$	UU_H[6]
	LGML1	Lower Global Mask Long Register High	$F70B_H$	$UUUUU000_B$[6]
	UMLM0	Upper Mask of Last Message Register Low	$F70C_H$	UU_H[6]
	UMLM1	Upper Mask of Last Message Register High	$F70D_H$	UU_H[6]
	LMLM0	Lower Mask of Last Message Register Low	$F70E_H$	UU_H[6]
	LMLM1	Lower Mask of Last Message Register High	$F70F_H$	$UUUUU000_B$[6]
		Message Object Registers:		
	MCR0	Message Control Register Low	$F7n0_H$[5]	UU_H[6]
	MCR1	Message Control Register High	$F7n1_H$[5]	UU_H[6]
	UAR0	Upper Arbitration Register Low	$F7n2_H$[5]	UU_H[6]
	UAR1	Upper Arbitration Register High	$F7n3_H$[5]	UU_H[6]
	LAR0	Lower Arbitration Register Low	$F7n4_H$[5]	UU_H[6]
	LAR1	Lower Arbitration Register High	$F7n5_H$[5]	$UUUUU000_B$[6]
	MCFG	Message Configuration Register	$F7n6_H$[5]	$UUUUUU00_B$[6]
	DB0n	Message Data Byte 0	$F7n7_H$[5]	XX_H[6]
	DB1n	Message Data Byte 1	$F7n8_H$[5]	XX_H[6]
	DB2n	Message Data Byte 2	$F7n9_H$[5]	XX_H[6]
	DB3n	Message Data Byte 3	$F7nA_H$[5]	XX_H[6]
	DB4n	Message Data Byte 4	$F7nB_H$[5]	XX_H[6]
	DB5n	Message Data Byte 5	$F7nC_H$[5]	XX_H[6]
	DB6n	Message Data Byte 6	$F7nD_H$[5]	XX_H[6]
	DB7n	Message Data Byte 7	$F7nE_H$[5]	XX_H[6]

Table 4 Special Function Registers - Functional Block (cont'd)

Block	Symbol	Name	Addr	Contents after Reset
SSC Interface	SSCCON	SSC Control Register	93_H [2]	07_H
	STB	SSC Transmit Buffer	94_H	XX_H [3]
	SRB	SSC Receive Register	95_H	XX_H [3]
	SCF	SSC Flag Register	AB_H [2]	$XXXXXX00_B$ [3]
	SCIEN	SSC Interrupt Enable Register	AC_H	$XXXXXX00_B$ [3]
	SSCMOD	SSC Mode Test Register	96_H	00_H
Timer 0/ Timer 1	TCON	Timer 0/1 Control Register	**88_H** [2]	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Compare/ Capture Unit/ Timer 2	CCEN	Comp./Capture Enable Reg.	$C1_H$	00_H
	CCH1	Comp./Capture Reg. 1, High Byte	$C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$C7_H$	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$C2_H$	00_H
	CCL2	Comp./Capture Reg. 2, Low Byte	$C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$C6_H$	00_H
	CRCH	Com./Rel./Capt. Reg. High Byte	CB_H	00_H
	CRCL	Com./Rel./Capt. Reg. Low Byte	CA_H	00_H
	TH2	Timer 2, High Byte	CD_H	00_H
	TL2	Timer 2, Low Byte	CC_H	00_H
	T2CON	Timer 2 Control Register	**$C8_H$** [2]	00_H
Power Save Modes	PCON [1]	Power Control Register	87_H	00_H
	PCON1	Power Control Register 1 C515C-8R	88_H [7]	$0XXXXXXX_B$ [3]
		C515C-8E	88_H [7]	$0XX0XXXX_B$ [3]

1) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

2) Bit-addressable special function registers

3) "X" means that the value is undefined and the location is reserved.

4) This SFR is a mapped SFR. For accessing this SFR, bit PDIR in SFR IP1 must be set.

5) The notation "n" in the message object address definition defines the number of the related message object.

6) "X" means that the value is undefined and the location is reserved. "U" means that the value is unchanged by a reset operation. "U" values are undefined (as "X") after a power-on reset operation.

7) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 5 Contents of the SFRs, SFRs in Numeric Order of their Addresses

Addr.	Register	Content after Reset[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80_H[2]	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
86_H	WDTREL	00_H	WDT PSEL	.6	.5	.4	.3	.2	.1	.0
87_H	PCON	00_H	SMOD	PDS	IDLS	SD	GF1	GF0	PDE	IDLE
88_H[2]	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
88_H[3]	PCON1[4]	$0XXX\text{-}XXXX_B$	EWPD	–	–	–	–	–	–	–
88_H[3]	PCON1[5]	$0XX0\text{-}XXXX_B$	EWPD	–	–	WS	–	–	–	–
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H[2]	P1	FF_H	T2	CLK-OUT	T2EX	$\overline{INT2}$	INT6	INT5	INT4	$\overline{INT3}$
91_H	XPAGE	00_H	.7	.6	.5	.4	.3	.2	.1	.0
92_H	DPSEL	$XXXX\text{-}X000_B$	–	–	–	–	–	.2	.1	.0
93_H	SSCCON	07_H	SCEN	TEN	MSTR	CPOL	CPHA	BRS2	BRS1	BRS0
94_H	STB	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
95_H	SRB	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
96_H	SSCMOD	00_H	LOOPB	TRIO	0	0	0	0	0	LSBSM
98_H[2]	SCON	00_H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$9A_H$	IEN2	$X00X\text{-}X00X_B$	–	–	EX8	EX7	–	ESSC	ECAN	–
$A0_H$[2]	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$A8_H$[2]	IEN0	00_H	EAL	WDT	ET2	ES	ET1	EX1	ET0	EX0
$A9_H$	IP0	00_H	OWDS	WDTS	.5	.4	.3	.2	.1	.0

Table 5 Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)

Addr.	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AA_H	SRELL	$D9_H$	.7	.6	.5	.4	.3	.2	.1	.0
AB_H	SCF	XXXX-XX00$_B$	–	–	–	–	–	–	WCOL	TC
AC_H	SCIEN	XXXX-XX00$_B$	–	–	–	–	–	–	WCEN	TCEN
$B0_H$[2)]	P3	FF_H	RD	WR	T1	T0	INT1	INT0	TxD	RxD
$B1_H$	SYSCON[4)]	X010-XX01$_B$	–	PMOD	EALE	RMAP	–	–	XMAP1	XMAP0
$B1_H$	SYSCON[5)]	X010-X001$_B$	–	PMOD	EALE	RMAP	–	CSWO	XMAP1	XMAP0
$B8_H$[2)]	IEN1	00_H	EXEN2	SWDT	EX6	EX5	EX4	EX3	EX2	EADC
$B9_H$	IP1	0X00-0000$_B$	PDIR	–	.5	.4	.3	.2	.1	.0
BA_H	SRELH	XXXX-XX11$_B$	–	–	–	–	–	–	.1	.0
$C0_H$[2)]	IRCON	00_H	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	IEX2	IADC
$C1_H$	CCEN	00_H	COCAH3	COCAL3	COCAH2	COCAL2	COCAH1	COCAL1	COCAH0	COCAL0
$C2_H$	CCL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C3_H$	CCH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C4_H$	CCL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C5_H$	CCH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C6_H$	CCL3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C7_H$	CCH3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C8_H$[2)]	T2CON	00_H	T2PS	I3FR	I2FR	T2R1	T2R0	T2CM	T2I1	T2I0
CA_H	CRCL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	CRCH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0

Table 5 Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)

Addr.	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$D0_H$[2)]	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$D8_H$[2)]	ADCON0	00_H	BD	CLK	ADEX	BSY	ADM	MX2	MX1	MX0
$D9_H$	ADDATH	00_H	.9	.8	.7	.6	.5	.4	.3	.2
DA_H	ADDATL	$00XX\text{-}XXXX_B$	.1	.0	–	–	–	–	–	–
DB_H	P6	–	.7	.6	.5	.4	.3	.2	.1	.0
DC_H	ADCON1	$0XXX\text{-}X000_B$	ADCL	–	–	–	0	MX2	MX1	MX0
$E0_H$[2)]	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E8_H$[2)]	P4	FF_H	RXDC	TXDC	$\overline{INT8}$	$\overline{SLS}$	STO	SRI	SCLK	$\overline{ADST}$
$F0_H$[2)]	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F8_H$[2)]	P5	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$F8_H$[2)]	DIR5[6)]	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
FA_H	P7	$XXXX\text{-}XXX1_B$	–	–	–	–	–	–	–	$\overline{INT7}$
FC_H	VR0[7)8)]	$C5_H$	1	1	0	0	0	1	0	1
FD_H	VR1[7)8)]	95_H	1	0	0	1	0	1	0	1
FE_H	VR2[7)8)]	02_H[9)]	0	0	0	0	0	0	1	0

1) "X" means that the value is undefined and the location is reserved.

2) Bit-addressable special function registers

3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

4) This SFR is available in the C515C-8R and C515C-L.

5) This SFR is available in the C515C-8E.

6) This SFR is a mapped SFR. For accessing this SFR, bit PDIR in SFR IP1 must be set.

7) This SFR is a mapped SFR. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

8) These SFRs are read-only registers (C515C-8E only).

9) The content of this SFR varies with the actual step of the C515C-8E (e.g. 01_H for the first step).

Table 6 Contents of the CAN Registers in Numeric Order of their Addresses

Addr. n = 1 to F_H[1)]	Register	Content after Reset[2)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$F700_H$	CR	01_H	TEST	CCE	0	0	EIE	SIE	IE	INIT
$F701_H$	SR	XX_H	BOFF	EWRN	–	RXOK	TXOK	LEC2	LEC1	LEC0
$F702_H$	IR	XX_H	INTID							
$F704_H$	BTR0	UU_H	SJW		BRP					
$F705_H$	BTR1	$0UUU.UUUU_B$	0	TSEG2			TSEG1			
$F706_H$	GMS0	UU_H	ID28-21							
$F707_H$	GMS1	$UUU1.1111_B$	ID20-18			1	1	1	1	1
$F708_H$	UGML0	UU_H	ID28-21							
$F709_H$	UGML1	UU_H	ID20-13							
$F70A_H$	LGML0	UU_H	ID12-5							
$F70B_H$	LGML1	$UUUU.U000_B$	ID4-0					0	0	0
$F70C_H$	UMLM0	UU_H	ID28-21							
$F70D_H$	UMLM1	UU_H	ID20-18			ID17-13				
$F70E_H$	LMLM0	UU_H	ID12-5							
$F70F_H$	LMLM1	$UUUU.U000_B$	ID4-0					0	0	0
$F7n0_H$	MCR0	UU_H	MSGVAL		TXIE		RXIE		INTPND	
$F7n1_H$	MCR1	UU_H	RMTPND		TXRQ		MSGLST CPUUPD		NEWDAT	
$F7n2_H$	UAR0	UU_H	ID28-21							
$F7n3_H$	UAR1	UU_H	ID20-18			ID17-13				
$F7n4_H$	LAR0	UU_H	ID12-5							
$F7n5_H$	LAR1	$UUUU.U000_B$	ID4-0					0	0	0
$F7n6_H$	MCFG	$UUUU.UU00_B$	DLC				DIR	XTD	0	0
$F7n7_H$	DB0n	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$F7n8_H$	DB1n	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$F7n9_H$	DB2n	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$F7nA_H$	DB3n	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$F7nB_H$	DB4n	XX_H	.7	.6	.5	.4	.3	.2	.1	.0

Table 6 Contents of the CAN Registers in Numeric Order of their Addresses (cont'd)

Addr. n = 1 to F_H [1]	Register	Content after Reset [2]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$F7nC_H$	DB5n	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$F7nD_H$	DB6n	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$F7nE_H$	DB7n	XX_H	.7	.6	.5	.4	.3	.2	.1	.0

1) The notation "n" in the address definition defines the number of the related message object.

2) "X" means that the value is undefined and the location is reserved. "U" means that the value is unchanged by a reset operation. "U" values are undefined (as "X") after a power-on reset operation.

Digital I/O Ports

The C515C allows for digital I/O on 49 lines grouped into 6 bidirectional 8-bit ports and one 1-bit port. Each port bit consists of a latch, an output driver and an input buffer. Read and write accesses to the I/O ports P0 through P7 are performed via their corresponding special function registers P0 to P7. The port structure of port 5 of the C515C is especially designed to operate either as a quasi-bidirectional port structure, compatible to the standard 8051-Family, or as a genuine bidirectional port structure. This port operating mode can be selected by software (setting or clearing the bit PMOD in the SFR SYSCON).

The output drivers of port 0 and 2 and the input buffers of port 0 are also used for accessing external memory. In this application, port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the port 2 pins continue emitting the P2 SFR contents.

Analog Input Ports

Ports 6 is available as input port only and provides two functions. When used as digital inputs, the corresponding SFR P6 contains the digital value applied to the port 6 lines. When used for analog inputs the desired analog channel is selected by a three-bit field in SFR ADCON0 or SFR ADCON1. Of course, it makes no sense to output a value to these input-only ports by writing to the SFR P6. This will have no effect.

If a digital value is to be read, the voltage levels are to be held within the input voltage specifications (V_{IL}/V_{IH}). Since P6 is not bit-addressable, all input lines of P6 are read at the same time by byte instructions.

Nevertheless, it is possible to use port 6 simultaneously for analog and digital input. However, care must be taken that all bits of P6 that have an undetermined value caused by their analog function are masked.

Port Structure Selection of Port 5

After a reset operation of the C515C, the quasi-bidirectional 8051-compatible port structure is selected. For selection of the bidirectional (CMOS) port 5 structure the bit PMOD of SFR SYSCON must be set. Because each port 5 pin can be programmed as an input or an output, additionally, after the selection of the bidirectional mode the direction register DIR5 of port 5 must be written. This direction register is mapped to the port 5 register. This means, the port register address is equal to its direction register address. **Figure 10** illustrates the port and direction register configuration.

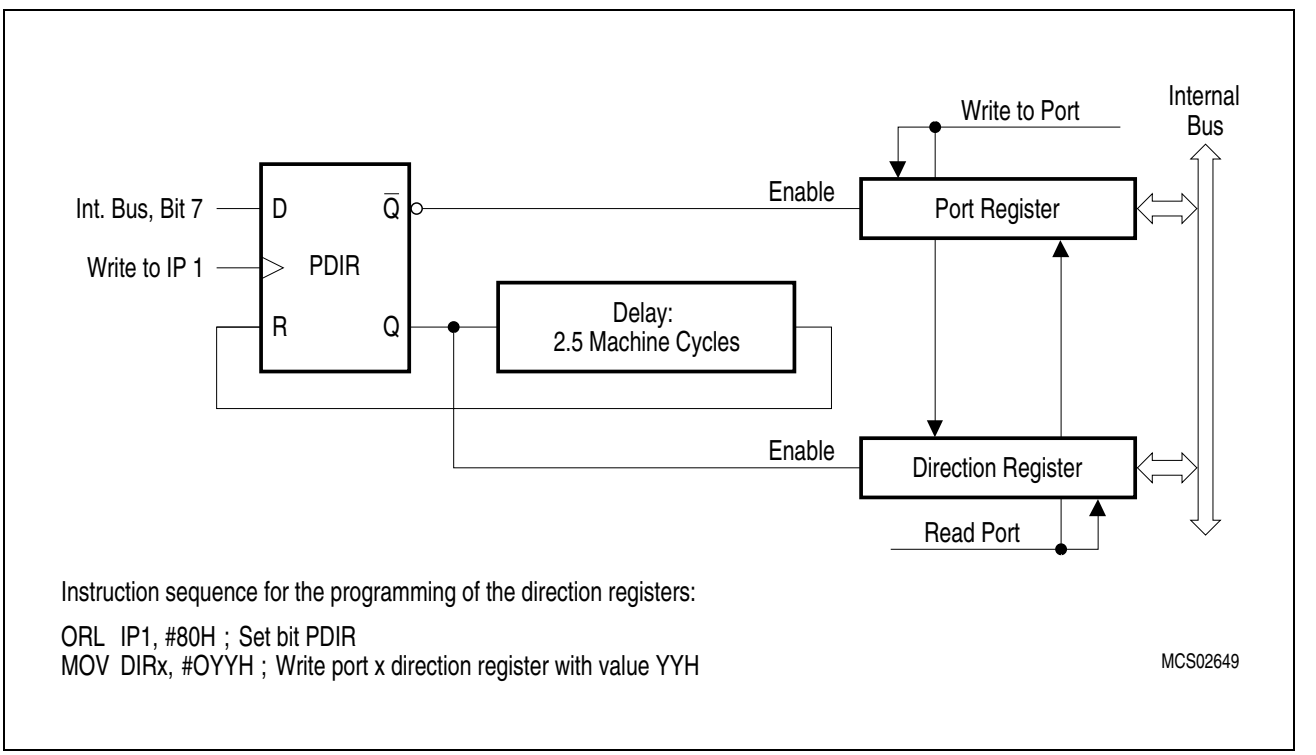


Figure 10 Port Register, Direction Register

Timer / Counter 0 and 1

Timer / Counter 0 and 1 can be used in four operating modes as listed in **Table 7**:

Table 7 Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD		Timer/Counter Input Clock	
		M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	0	0	$f_{OSC}/6 \times 32$	$f_{OSC}/12 \times 32$
1	16-bit timer/counter	0	1	$f_{OSC}/6$	$f_{OSC}/12$
2	8-bit timer/counter with 8-bit autoreload	1	0		
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer / Timer 1 stops	1	1		

In the “timer” function (C/$\overline{T}$ = ‘0’) the register is incremented every machine cycle. Therefore the count rate is $f_{OSC}/6$.

In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{OSC}/12$. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 11** illustrates the input clock logic.

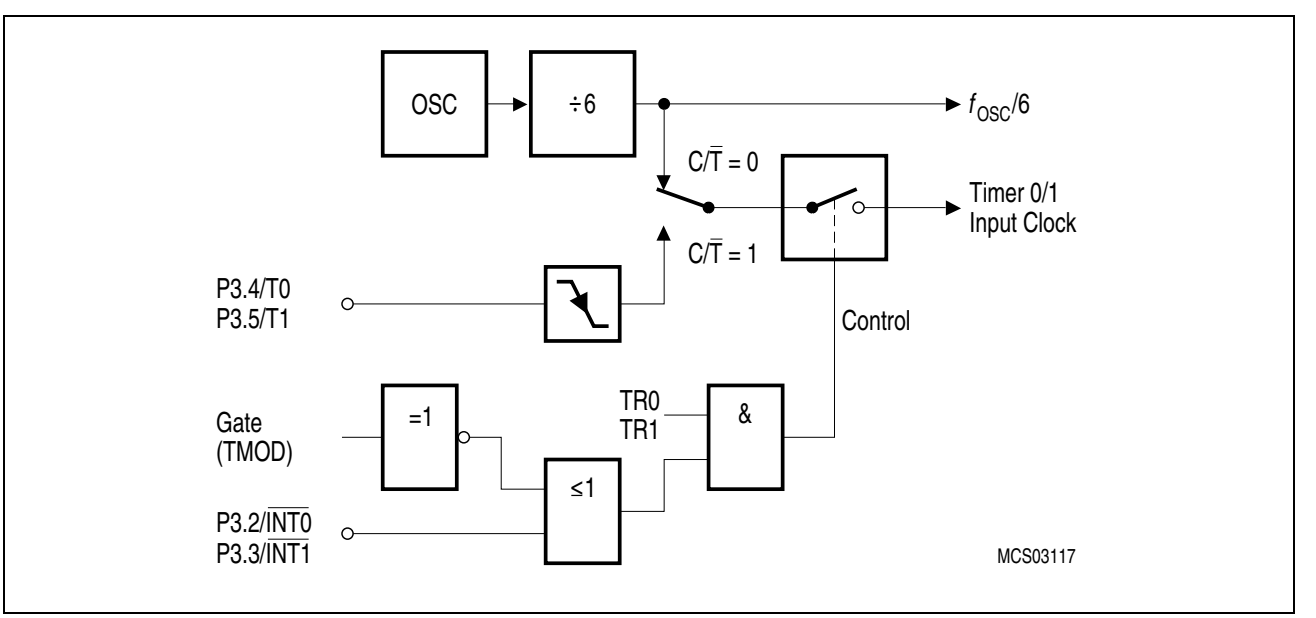


Figure 11 Timer/Counter 0 and 1 Input Clock Logic

Timer / Counter 2 with Compare/Capture/Reload

The timer 2 of the C515C provides additional compare/capture/reload features, which allow the selection of the following operating modes:

- Compare: up to 4 PWM signals with 16-bit/600 ns resolution
- Capture: up to 4 high speed capture inputs with 600 ns resolution
- Reload: modulation of timer 2 cycle time

The block diagram in **Figure 12** shows the general configuration of timer 2 with the additional compare/capture/reload registers. The I/O pins which can used for timer 2 control are located as multifunctional port functions at port 1.

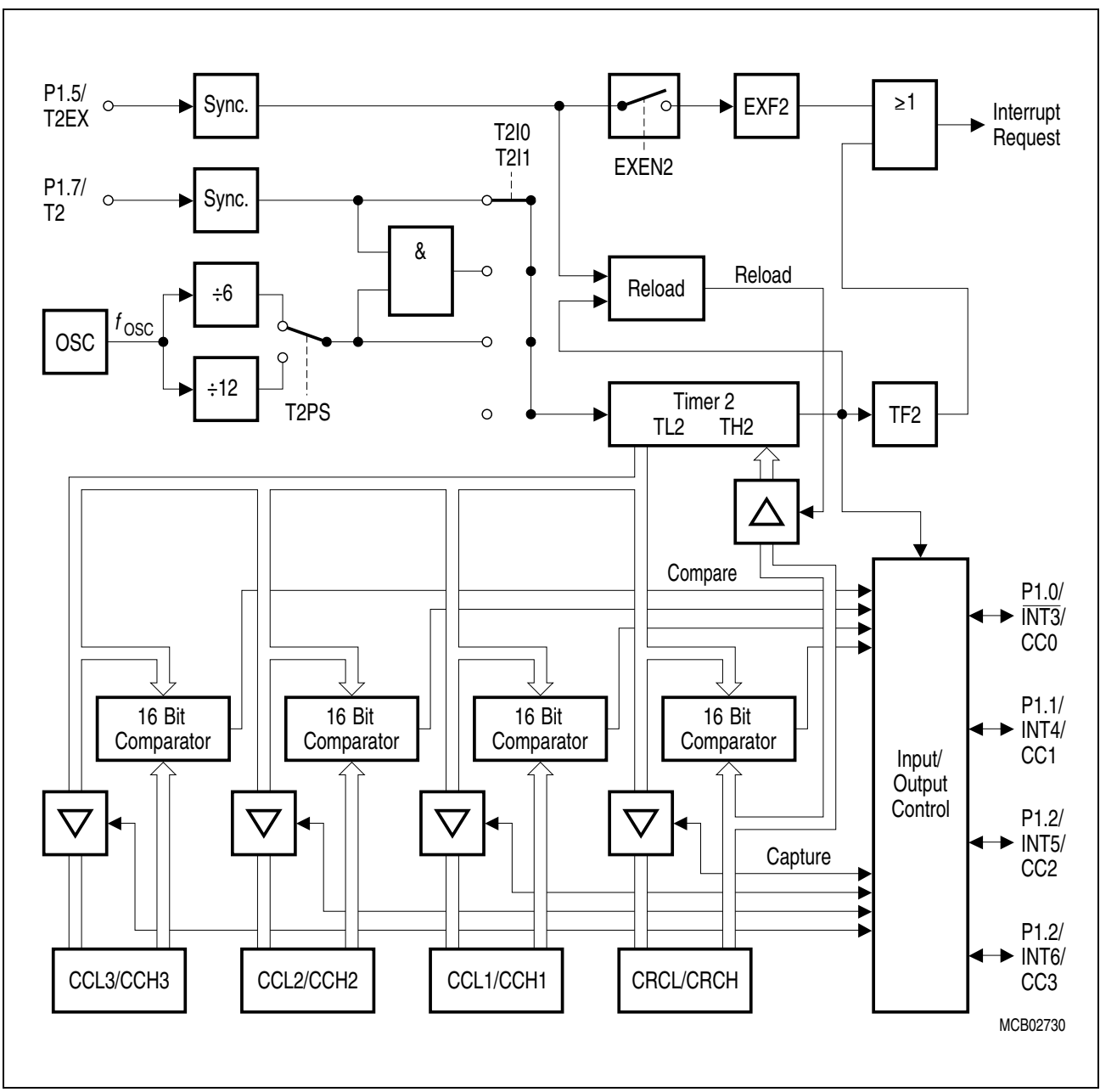


Figure 12 Timer 2 Block Diagram

Timer 2 Operating Modes

The timer 2, which is a 16-bit-wide register, can operate as timer, event counter, or gated timer. A roll-over of the count value in TL2/TH2 from all 1's to all 0's sets the timer overflow flag TF2 in SFR IRCON, which can generate an interrupt. The bits in register T2CON are used to control the timer 2 operation.

Timer Mode: In timer function, the count rate is derived from the oscillator frequency. A prescaler offers the possibility of selecting a count rate of 1/6 or 1/12 of the oscillator frequency.

Gated Timer Mode: In gated timer function, the external input pin T2 (P1.7) functions as a gate to the input of timer 2. If T2 is high, the internal clock input is gated to the timer. T2 = 0 stops the counting procedure. This facilitates pulse width measurements. The external gate signal is sampled once every machine cycle.

Event Counter Mode: In the event counter function. the timer 2 is incremented in response to a 1-to-0 transition at its corresponding external input pin T2 (P1.7). In this function, the external input is sampled every machine cycle. Since it takes two machine cycles (12 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/12 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for at least one full machine cycle.

Reload of Timer 2: Two reload modes are selectable:
In mode 0, when timer 2 rolls over from all 1's to all 0's, it not only sets TF2 but also causes the timer 2 registers to be loaded with the 16-bit value in the CRC register, which is preset by software.

In mode 1, a 16-bit reload from the CRC register is caused by a negative transition at the corresponding input pin P1.5/T2EX. This transition will also set flag EXF2 if bit EXEN2 in SFR IEN1 has been set.

Timer 2 Compare Modes

The compare function of a timer/register combination operates as follows: the 16-bit value stored in a compare or compare/capture register is compared with the contents of the timer register; if the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin and an interrupt can be generated.

Compare Mode 0

In compare mode 0, upon matching the timer and compare register contents, the output signal changes from low to high. It goes back to a low level on timer overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit only and writing to the port will have no effect. **Figure 13** shows a functional diagram of a port circuit when used in compare mode 0. The port latch is directly controlled by the timer overflow and compare match signals. The input line from the internal bus and the write-to-latch line of the port latch are disconnected when compare mode 0 is enabled.

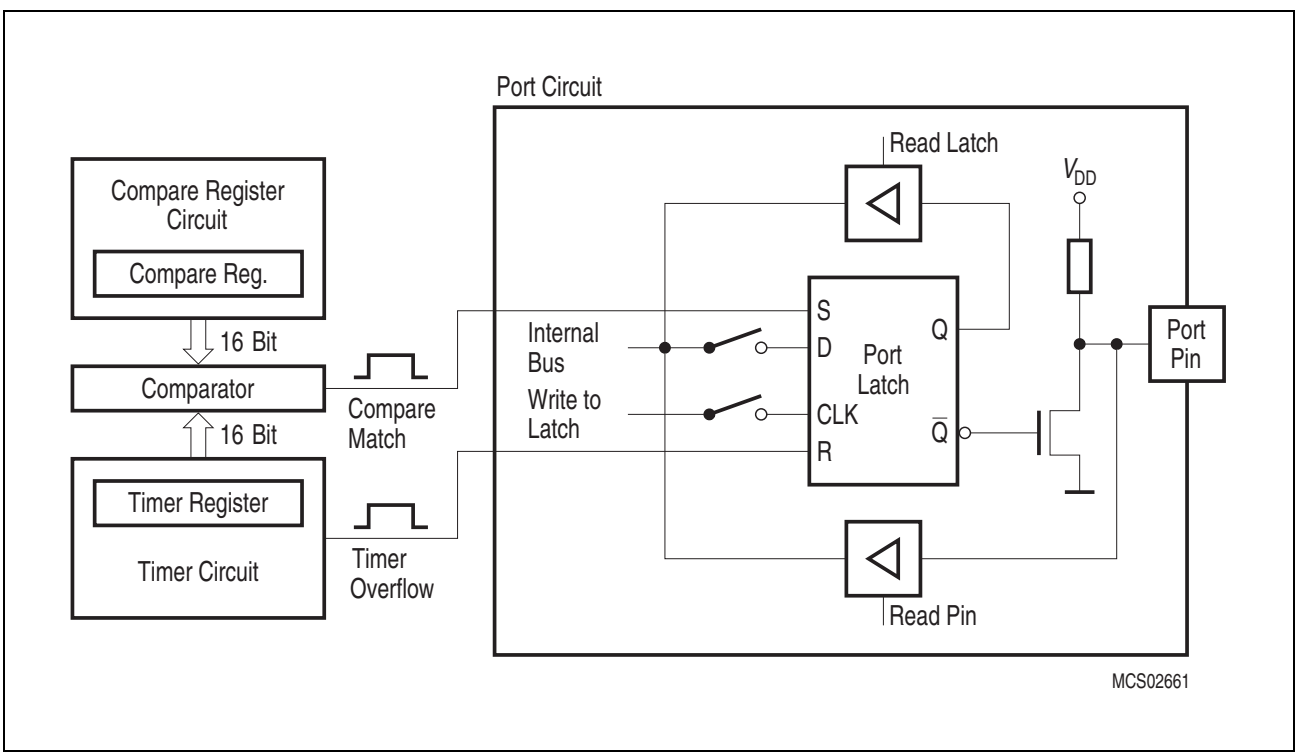


Figure 13 Port Latch in Compare Mode 0

Compare Mode 1

If compare mode 1 is enabled and the software writes to the appropriate output latch at the port, the new value will not appear at the output pin until the next compare match occurs. Thus, it can be choosen whether the output signal has to make a new transition (1-to-0 or 0-to-1, depending on the actual pin-level) or should keep its old value at the time when the timer value matches the stored compare value.

In compare mode 1 (see **Figure 14**) the port circuit consists of two separate latches. One latch (which acts as a “shadow latch”) can be written under software control, but its value will only be transferred to the port latch (and thus to the port pin) when a compare match occurs.

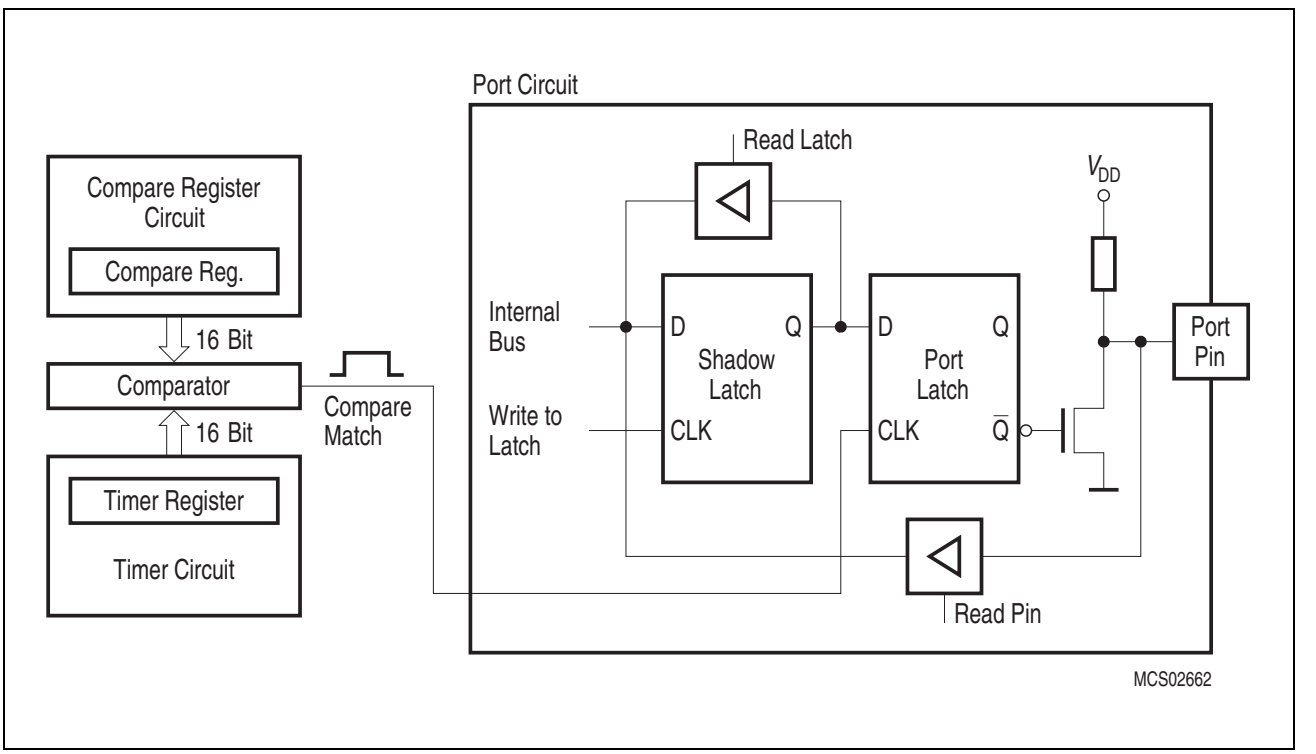


Figure 14 Compare Function in Compare Mode 1

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **Table 8**.

Table 8 USART Operating Modes

Mode	SCON		Description
	SM0	SM1	
0	0	0	**Shift register mode, fixed baud rate** Serial data enters and exits through R×D; T×D outputs the shift clock; 8-bit are transmitted/received (LSB first)
1	0	1	**8-bit UART, variable baud rate** 10 bits are transmitted (through T×D) or received (at R×D)
2	1	0	**9-bit UART, fixed baud rate** 11 bits are transmitted (through T×D) or received (at R×D)
3	1	1	**9-bit UART, variable baud rate** Like mode 2

For clarification some terms regarding the difference between “baud rate clock” and “baud rate” should be mentioned. In the **asynchronous modes** the serial interfaces require a clock rate which is 16 times the baud rate for internal synchronization. Therefore, the baud rate generators/timers have to provide a “baud rate clock” (output signal in **Figure 15** to the serial interface which - there divided by 16 - results in the actual “baud rate”. Further, the abbreviation f_{OSC} refers to the oscillator frequency (crystal or external clock operation).

The variable baud rates for modes 1 and 3 of the serial interface can be derived either from timer 1 or from a dedicated baud rate generator (see **Figure 15**).

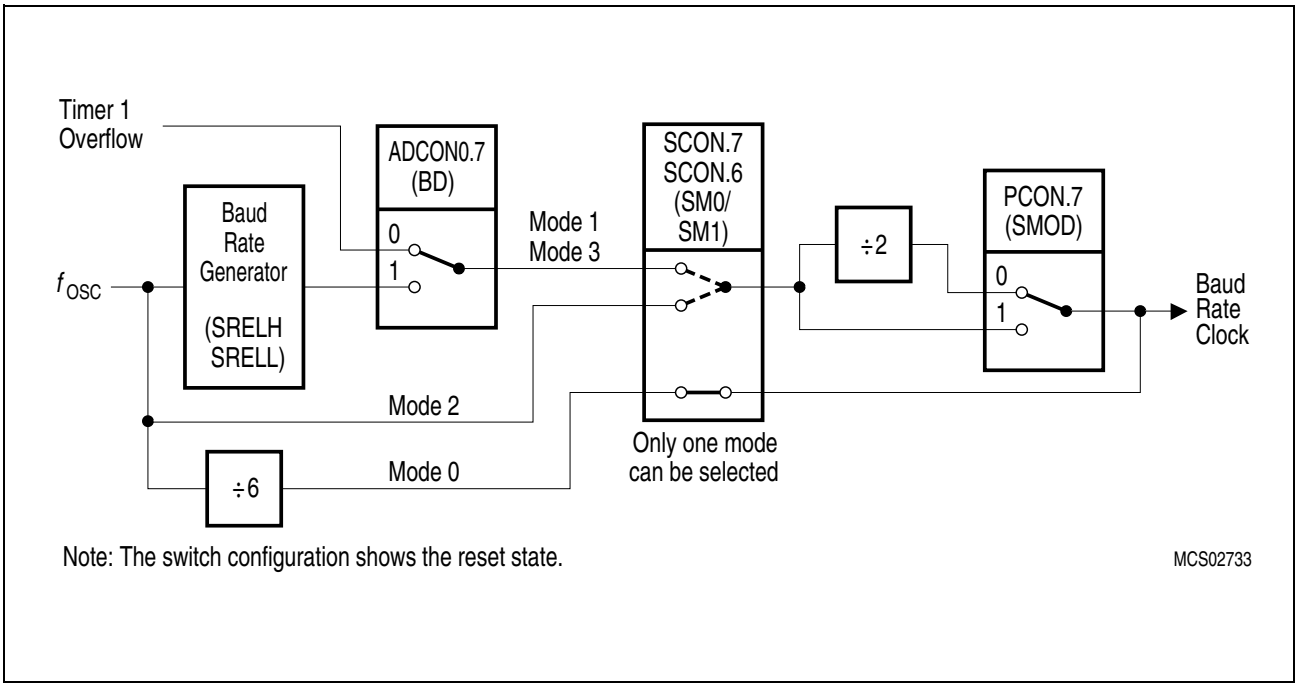


Figure 15 Block Diagram of Baud Rate Generation for the Serial Interface

Table 9 below lists the values/formulas for the baud rate calculation of the serial interface with its dependencies of the control bits BD and SMOD.

Table 9 Serial Interface - Baud Rate Dependencies

Serial Interface Operating Modes	Active Control Bits		Baud Rate Calculation
	BD	SMOD	
Mode 0 (Shift Register)	–	–	f_{OSC} / 6
Mode 1 (8-bit UART) Mode 3 (9-bit UART)	0	X	Controlled by timer 1 overflow: (2^{SMOD} × timer 1 overflow rate) / 32
	1	X	Controlled by baud rate generator ($2^{SMOD} \times f_{OSC}$) / (32 × baud rate generator overflow rate)
Mode 2 (9-bit UART)	–	0 1	f_{OSC} / 32 f_{OSC} / 16

SSC Interface

The C515C microcontroller provides a Synchronous Serial Channel unit, the SSC. This interface is compatible to the popular SPI serial bus interface. **Figure 16** shows the block diagram of the SSC. The central element of the SSC is an 8-bit shift register. The input and the output of this shift register are each connected via a control logic to the pin P4.2 / SRI (SSC Receiver In) and P4.3 / STO (SSC Transmitter Out). This shift register can be written to (SFR STB) and can be read through the Receive Buffer Register SRB.

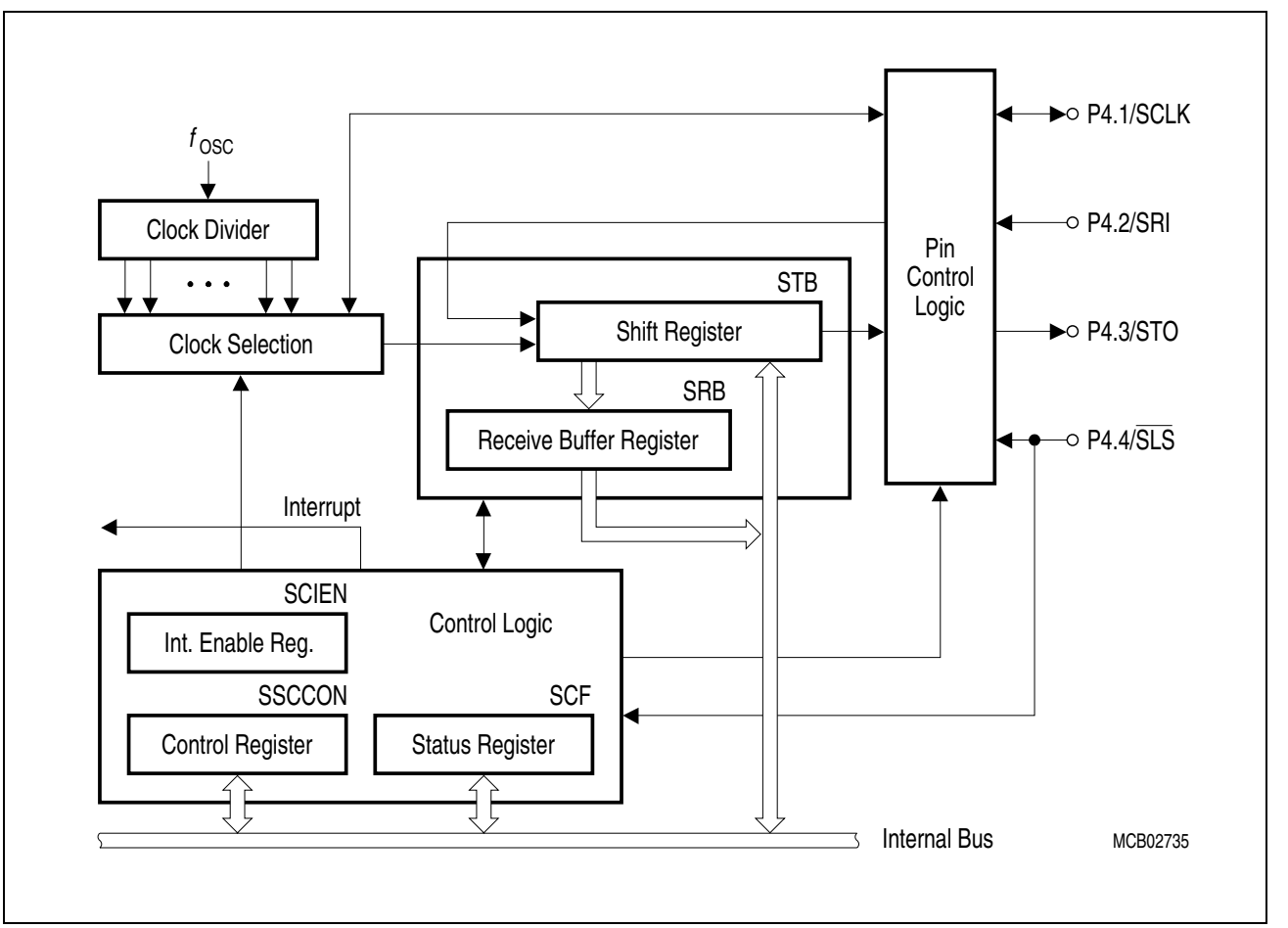


Figure 16 SSC Block Diagram

The SSC has implemented a clock control circuit, which can generate the clock via a baud rate generator in the master mode, or receive the transfer clock in the slave mode. The clock signal is fully programmable for clock polarity and phase. The pin used for the clock signal is P4.1 / SCLK. When operating in slave mode, a slave select input is provided which enables the SSC interface and also will control the transmitter output. The pin used for this is P4.4 / $\overline{\text{SLS}}$.

The SSC control block is responsible for controlling the different modes and operation of the SSC, checking the status, and generating the respective status and interrupt signals.

CAN Controller

The on-chip CAN controller is the functional heart which provides all resources that are required to run the standard CAN protocol (11-bit identifiers) as well as the extended CAN protocol (29-bit identifiers). It provides a sophisticated object layer to relieve the CPU of as much overhead as possible when controlling many different message objects (up to 15). This includes bus arbitration, resending of garbled messages, error handling, interrupt generation, etc. In order to implement the physical layer, external components have to be connected to the C515C.

The internal bus interface connects the on-chip CAN controller to the internal bus of the microcontroller. The registers and data locations of the CAN interface are mapped to a specific 256 bytes wide address range of the external data memory area ($F700_H$ to $F7FF_H$) and can be accessed using MOVX instructions. **Figure 17** shows a block diagram of the on-chip CAN controller.

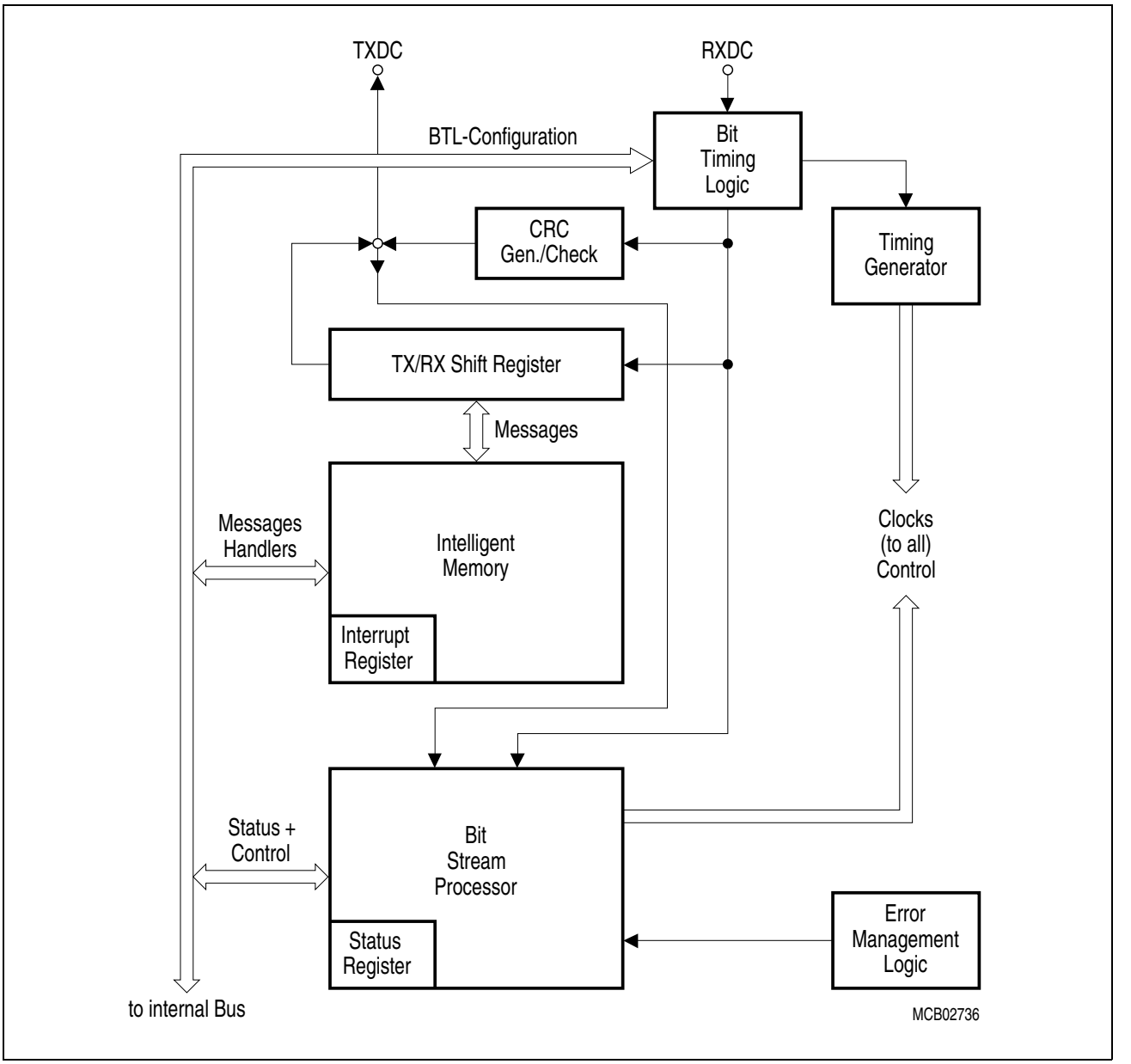


Figure 17 CAN Controller Block Diagram

The **TX/RX Shift Register** holds the destuffed bit stream from the bus line to allow the parallel access to the whole data or remote frame for the acceptance match test and the parallel transfer of the frame to and from the Intelligent Memory.

The **Bit Stream Processor (BSP)** is a sequencer controlling the sequential data stream between the TX/RX Shift Register, the CRC Register, and the bus line. The BSP also controls the EML and the parallel data stream between the TX/RX Shift Register and the Intelligent Memory such that the processes of reception, arbitration, transmission, and error signalling are performed according to the CAN protocol. Note that the automatic retransmission of messages which have been corrupted by noise or other external error conditions on the bus line is handled by the BSP.

The **Cyclic Redundancy Check Register (CRC)** generates the Cyclic Redundancy Check code to be transmitted after the data bytes and checks the CRC code of incoming messages. This is done by dividing the data stream by the code generator polynomial.

The **Error Management Logic (EML)** is responsible for the fault confinement of the CAN device. Its counters, the Receive Error Counter and the Transmit Error Counter, are incremented and decremented by commands from the Bit Stream Processor. According to the values of the error counters, the CAN controller is set into the states error *active*, error *passive* and busoff.

The **Bit Timing Logic (BTL)** monitors the busline input RXDC and handles the busline related bit timing according to the CAN protocol. The BTL synchronizes on a *recessive* to *dominant* busline transition at *Start of Frame* (hard synchronization) and on any further *recessive* to *dominant* busline transition, if the CAN controller itself does not transmit a *dominant* bit (resynchronization). The BTL also provides programmable time segments to compensate for the propagation delay time and for phase shifts and to define the position of the Sample Point in the bit time. The programming of the BTL depends on the baudrate and on external physical delay times.

The **Intelligent Memory** (CAM/RAM array) provides storage for up to 15 message objects of maximum 8 data bytes length. Each of these objects has a unique identifier and its own set of control and status bits. After the initial configuration, the Intelligent Memory can handle the reception and transmission of data without further CPU actions.

Switch-off Capability of the CAN Controller (C515C-8E only)

For power consumption reasons, the on-chip CAN controller in the C515C-8E can be switched off by setting bit CSWO (bit 2) in SFR SYSCON. When the CAN controller is switched off its clock signal is turned off and the operation of the CAN controller is stopped. This switch-off state of the CAN controller is equal to its state in software power down mode. After clearing bit CSWO again the CAN controller has to be reconfigured.

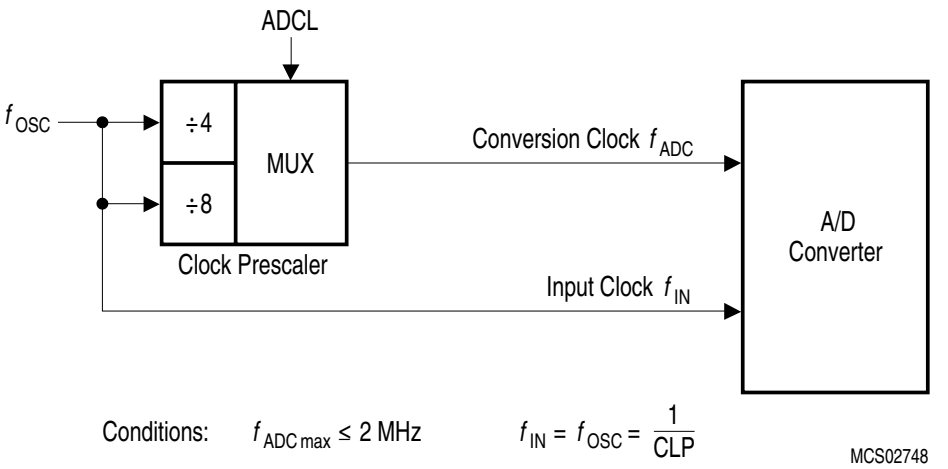
10-Bit A/D Converter

The C515C includes a high performance / high speed 10-bit A/D-Converter (ADC) with 8 analog input channels. It operates with a successive approximation technique and uses self calibration mechanisms for reduction and compensation of offset and linearity errors. The A/D converter provides the following features:

- 8 multiplexed input channels (port 6), which can also be used as digital inputs
- 10-bit resolution
- Single or continuous conversion mode
- Internal or external start-of-conversion trigger capability
- Interrupt request generation after each conversion
- Using successive approximation conversion technique via a capacitor array
- Built-in hidden calibration of offset and linearity errors

The main functional blocks of the A/D converter are shown in **Figure 19**.

The A/D converter uses basically two clock signals for operation: the input clock f_{IN} (= $1/t_{IN}$) and the conversion clock f_{ADC} (= $1/t_{ADC}$). These clock signals are derived from the C515C system clock f_{OSC} which is applied at the XTAL pins. The input clock f_{IN} is equal to f_{OSC}. The conversion clock is limited to a maximum frequency of 2 MHz and therefore must be adapted to f_{OSC} by programming the conversion clock prescaler. The table in **Figure 18** shows the prescaler ratios and the resulting A/D conversion times which must be selected for typical system clock rates.



MCU System Clock Rate (f_{OSC})	ADCL	Conversion Clock f_{ADC} [MHz]
2 MHz	0	.5
4 MHz	0	1
6 MHz	0	1.5
8 MHz	0	2
10 MHz	1	1.25

Figure 18 A/D Converter Clock Selection

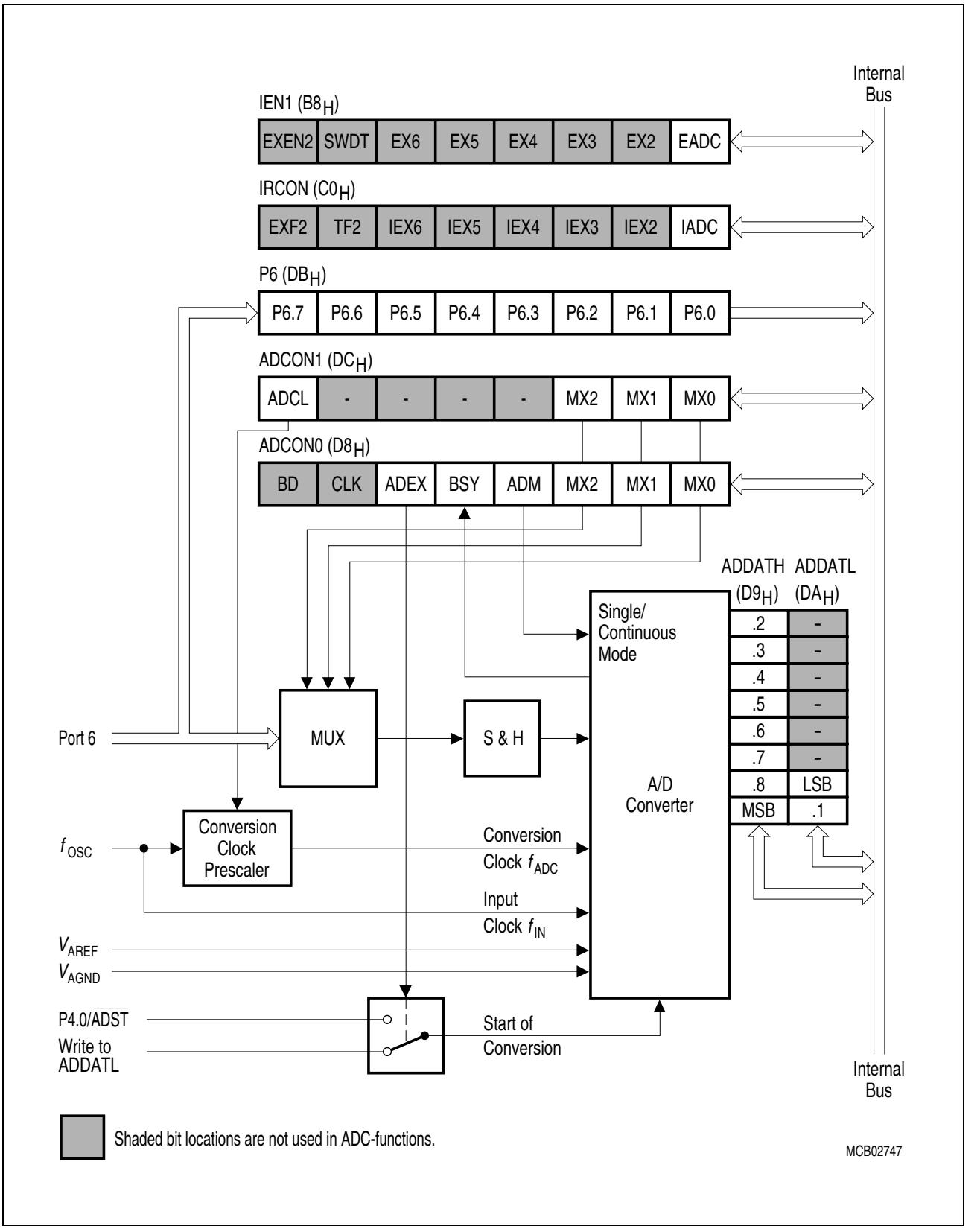
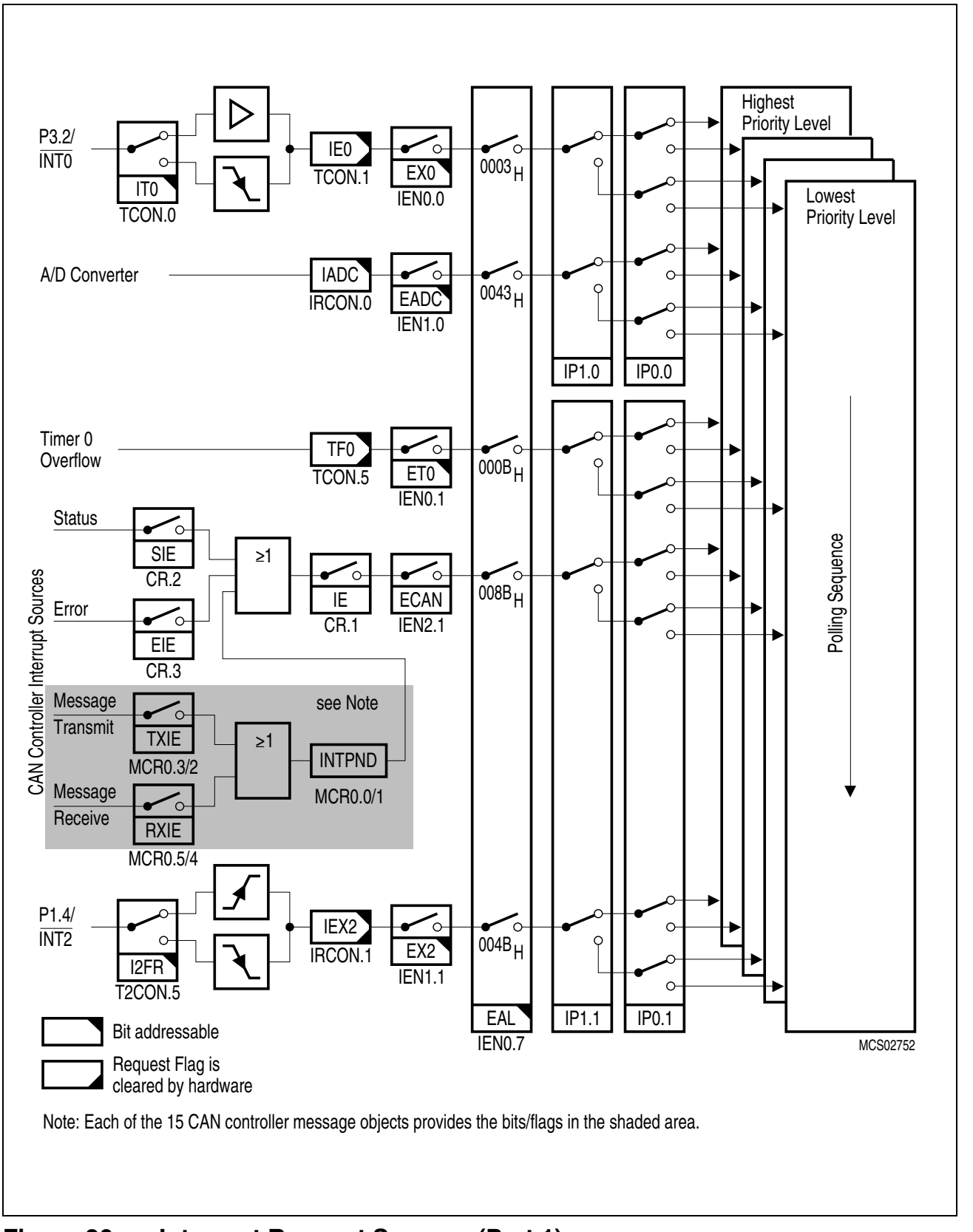


Figure 19 A/D Converter Block Diagram

Interrupt System

The C515C provides 17 interrupt sources with four priority levels. Seven interrupts can be generated by the on-chip peripherals (timer 0, timer 1, timer 2, serial interface, A/D converter, SSC interface, CAN controller), and ten interrupts may be triggered externally (P1.5/T2EX, P3.2/INT0, P3.3/INT1, P1.4/INT2, P1.0/$\overline{\text{INT3}}$, P1.1/INT4, P1.2/INT5, P1.3/INT6, P7.0/$\overline{\text{INT7}}$, P4.5/$\overline{\text{INT8}}$). The wake-up from power-down mode interrupt has a special functionality which allows to exit from the software power-down mode by a short low pulse at pin P3.2/$\overline{\text{INT0}}$.

In the C515C the 17 interrupt sources are combined to six groups of two or three interrupt sources. Each interrupt group can be programmed to one of the four interrupt priority levels. **Figure 20** to **Figure 22** give a general overview of the interrupt sources and illustrate the interrupt request and control flags.



Note: Each of the 15 CAN controller message objects provides the bits/flags in the shaded area.

Figure 20 Interrupt Request Sources (Part 1)

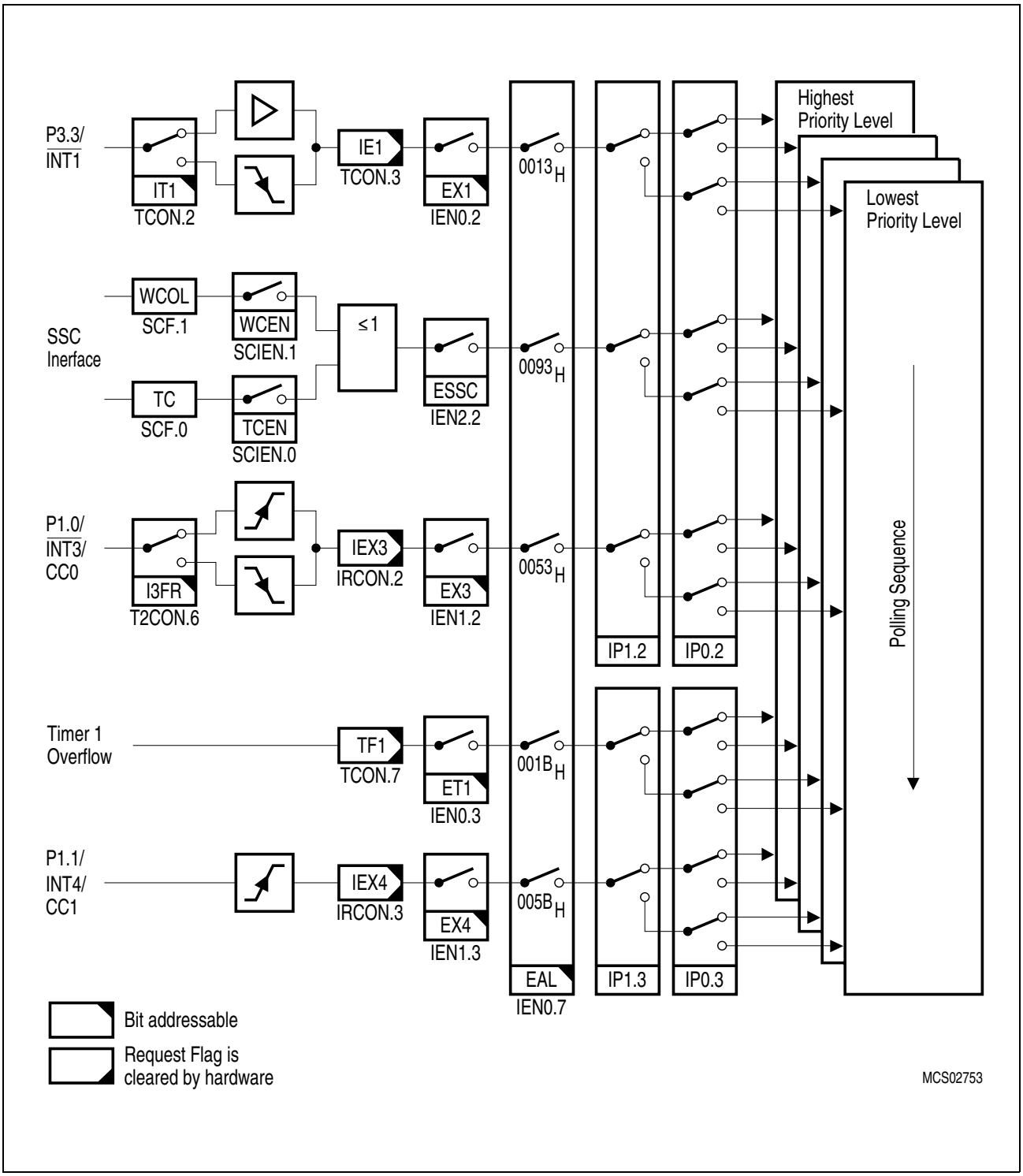


Figure 21 Interrupt Request Sources (Part 2)

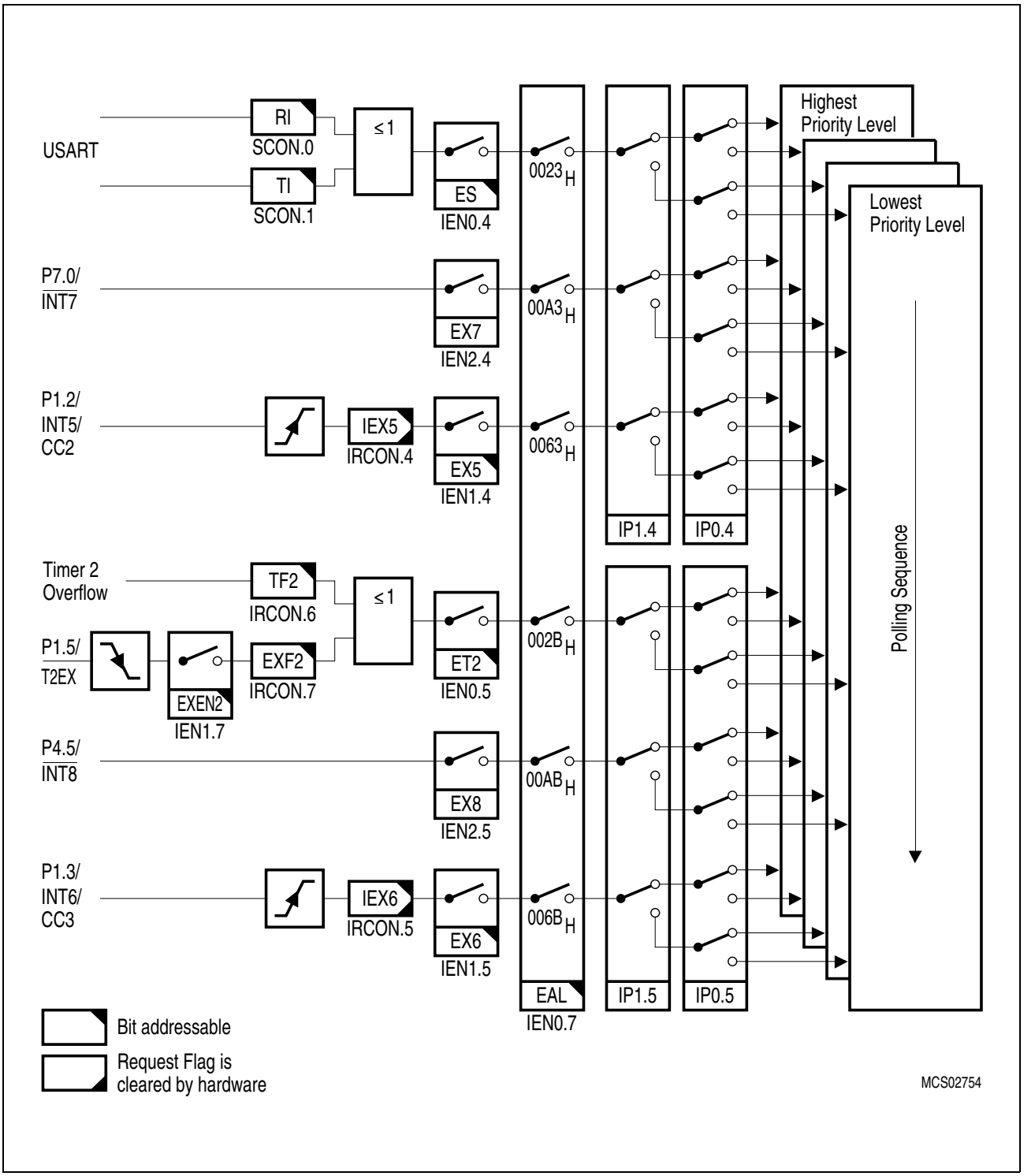


Figure 22 Interrupt Request Sources (Part 3)

Table 10 Interrupt Source and Vectors

Interrupt Source	Interrupt Vector Address	Interrupt Request Flags
External Interrupt 0	0003_H	IE0
Timer 0 Overflow	$000B_H$	TF0
External Interrupt 1	0013_H	IE1
Timer 1 Overflow	$001B_H$	TF1
Serial Channel	0023_H	RI / TI
Timer 2 Overflow / Ext. Reload	$002B_H$	TF2 / EXF2
A/D Converter	0043_H	IADC
External Interrupt 2	$004B_H$	IEX2
External Interrupt 3	0053_H	IEX3
External Interrupt 4	$005B_H$	IEX4
External Interrupt 5	0063_H	IEX5
External Interrupt 6	$006B_H$	IEX6
Wake-up from power-down mode	$007B_H$	–
CAN controller	$008B_H$	–
External Interrupt 7	$00A3_H$	–
External Interrupt 8	$00AB_H$	–
SSC interface	0093_H	TC / WCOL

Fail Save Mechanisms

The C515C offers two on-chip peripherals which monitor the program flow and ensure an automatic “fail-safe” reaction for cases where the controller’s hardware fails or the software hangs up:

- A programmable watchdog timer (WDT) with variable time-out period from 512 microseconds up to approx. 1.1 seconds at 6 MHz.
- An oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state in case the on-chip oscillator fails; it also provides the clock for a fast internal reset after power-on.

Programmable Watchdog Timer

The watchdog timer in the C515C is a 15-bit timer, which is incremented by a count rate of $f_{OSC}/12$ up to $f_{OSC}/192$. For programming of the watchdog timer overflow rate, the upper 7 bit of the watchdog timer can be written. **Figure 23** shows the block diagram of the watchdog timer unit.

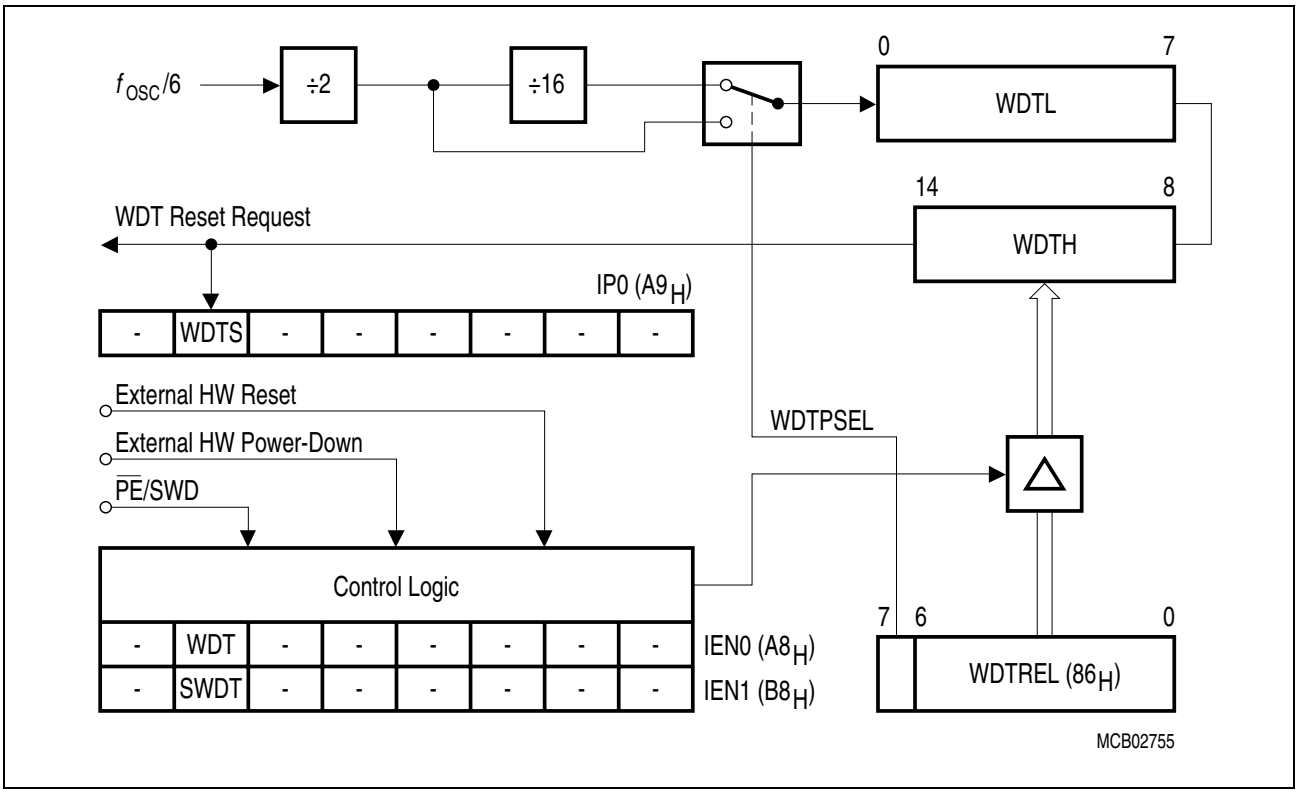


Figure 23 Block Diagram of the Programmable Watchdog Timer

The watchdog timer can be started by software (bit SWDT) or by hardware through pin $\overline{PE}$/SWD, but it cannot be stopped during active mode of the C515C. If the software fails to refresh the running watchdog timer an internal reset will be initiated on watchdog timer overflow. For refreshing of the watchdog timer the content of the SFR WDTREL is transferred to the upper 7-bit of the watchdog timer. The refresh sequence consists of

two consecutive instructions which set the bits WDT and SWDT each. The reset cause (external reset or reset caused by the watchdog) can be examined by software (flag WDTS). It must be noted, however, that the watchdog timer is halted during the idle mode and power down mode of the processor.

Oscillator Watchdog

The oscillator watchdog unit serves for four functions:

- **Monitoring of the on-chip oscillator's function**
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset; if the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part executes a final reset phase of typ. 1 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.
- **Fast internal reset after power-on**
  The oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. The oscillator watchdog unit also works identically to the monitoring function.
- **Restart from the hardware power down mode**
  If the hardware power down mode is terminated the oscillator watchdog has to control the correct start-up of the on-chip oscillator and to restart the program. The oscillator watchdog function is only part of the complete hardware power down sequence; however, the watchdog works identically to the monitoring function.
- **Control of external wake-up from software power-down mode**
  When the software power-down mode is left by a low level at the P3.2/$\overline{\text{INT0}}$ pin, the oscillator watchdog unit assures that the microcontroller resumes operation (execution of the power-down wake-up interrupt) with the nominal clock rate. In the power-down mode the RC oscillator and the on-chip oscillator are stopped. Both oscillators are started again when power-down mode is released. When the on-chip oscillator has a higher frequency than the RC oscillator, the microcontroller starts operation after a final delay of typ. 1 ms in order to allow the on-chip oscillator to stabilize.

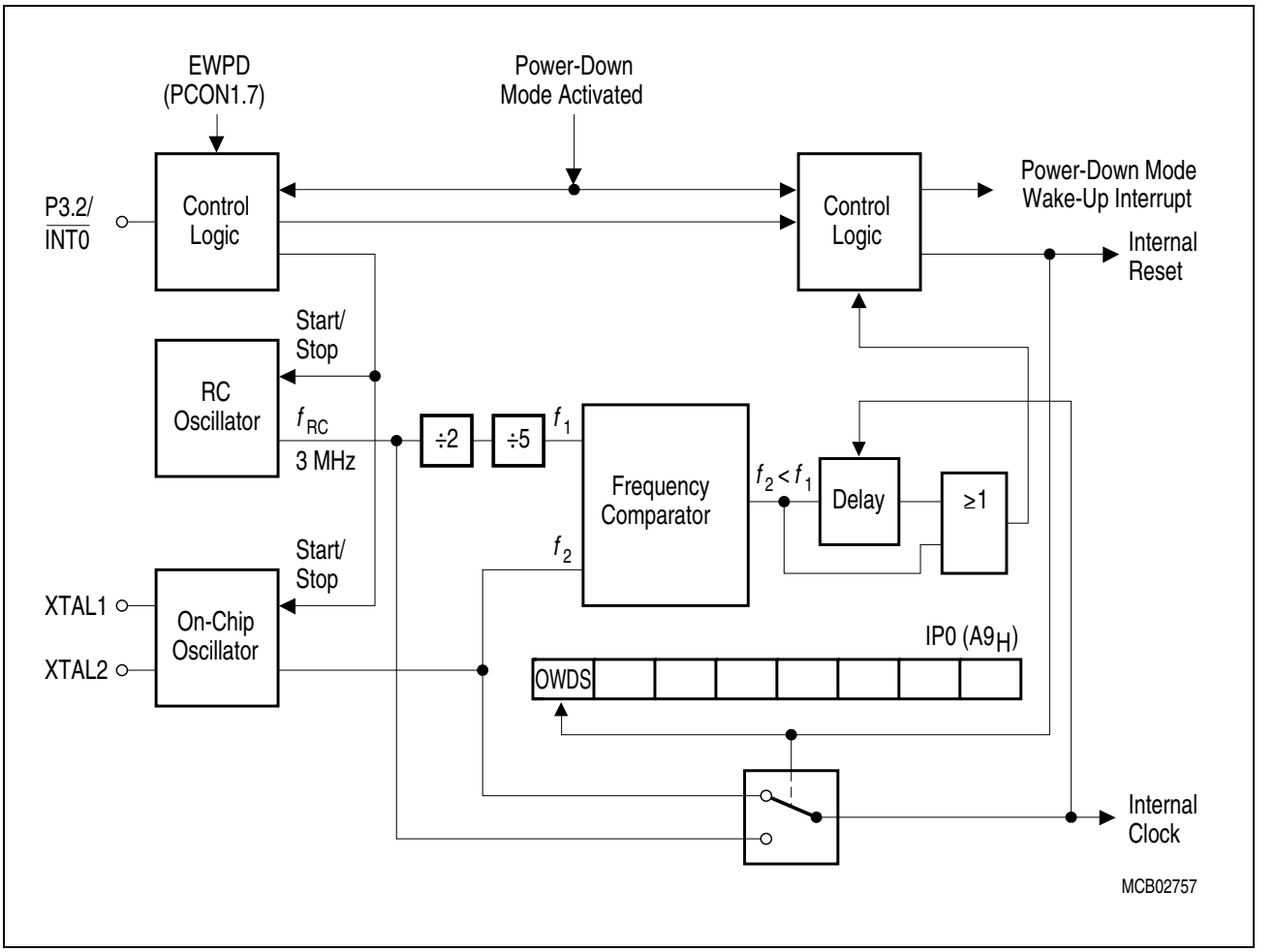


Figure 24 Block Diagram of the Oscillator Watchdog

Power Saving Modes

The C515C provides two basic power saving modes, the idle mode and the power down mode. Additionally, a slow down mode is available. This power saving mode reduces the internal clock rate in normal operating mode and it can be also used for further power reduction in idle mode.

- **Idle mode**
  The CPU is gated off from the oscillator. All peripherals are still provided with the clock and are able to work. Idle mode is entered by software and can be left by an interrupt or reset.
- **Power down mode**
  The operation of the C515C is completely stopped and the oscillator is turned off. This mode is used to save the contents of the internal RAM with a very low standby current.
  Software power down mode: Software power down mode is entered by software and can be left by reset or by a short low pulse at pin P3.2/$\overline{\text{INT0}}$ (or P4.7/$\overline{\text{RXDC}}$, C515C-8E only).
  Hardware power down mode: Hardware power down mode is entered when the pin $\overline{\text{HWPD}}$ is put to low level.
- **Slow-down mode**
  The controller keeps up the full operating functionality, but its normal clock frequency is internally divided by 32. This slows down all parts of the controller, the CPU and all peripherals, to 1/32th of their normal operating frequency. Slowing down the frequency significantly reduces power consumption. The slow down mode can be combined with the idle mode.

Table 11 gives a general overview of the entry and exit conditions of the power saving modes.

In the power down mode of operation, V_{DD} can be reduced to minimize power consumption. It must be ensured, however, that V_{DD} is not reduced before the power down mode is invoked, and that V_{DD} is restored to its normal operating level, before the power down mode is terminated.

If e.g. the idle mode is left through an interrupt, the microcontroller state (CPU, ports, peripherals) remains preserved. If a power saving mode is left by a hardware reset, the microcontroller state is disturbed and replaced by the reset state of the C515C.

If WS (bit 4) is SFR PCON1 is set (C515C-8E only), pin P4.7/$\overline{\text{RXDC}}$ is alternatively selected as wake-up pin for the software power down mode. If WS (bit 4) is SFR PCON1 is cleared (C515C-8E only), pin P3.2/$\overline{\text{INT0}}$ is selected as wake-up pin for the software power down mode.

For the C515C-8R, P3.2/$\overline{\text{INT0}}$ is always selected as wake-up pin.

Table 11 Power Saving Modes Overview

Mode	Entering (2-Instruction Example)	Leaving by	Remarks
Idle mode	ORL PCON, #01_H ORL PCON, #20_H	Occurrence of an interrupt from a peripheral unit	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock
		Hardware Reset	
Software Power-Down Mode	ORL PCON, #02_H ORL PCON, #40_H	Hardware Reset	Oscillator is stopped; contents of on-chip RAM and SFR's are maintained;
		Short low pulse at pin P3.2/$\overline{INT0}$ (or P4.7/$\overline{RXDC}$, C515C-8E only)	
Hardware Power-Down Mode	$\overline{HWPD}$ = low	$\overline{HWPD}$ = high	C515C is put into its reset state and the oscillator is stopped; ports become floating outputs
Slow Down Mode	ORL PCON, #10_H	ANL PCON, #$0EF_H$ or Hardware Reset	Oscillator frequency is reduced to 1/32 of its nominal frequency

OTP Memory Operation (C515C-8E only)

The C515C-8E contains a 64 Kbytes one-time programmable (OTP) program memory. With the C515C-8E fast programming cycles are achieved (1 byte in 100 µs). Also several levels of OTP memory protection can be selected.

For programming of the device, the C515C-8E must be put into the programming mode. This typically is done not in-system but in a special programming hardware. In the programming mode the C515C-8E operates as a slave device similar as an EPROM standalone memory device and must be controlled with address/data information, control lines, and an external 11.5 V programming voltage. **Figure 25** shows the pins of the C515C-8E which are required for controlling of the OTP programming mode.

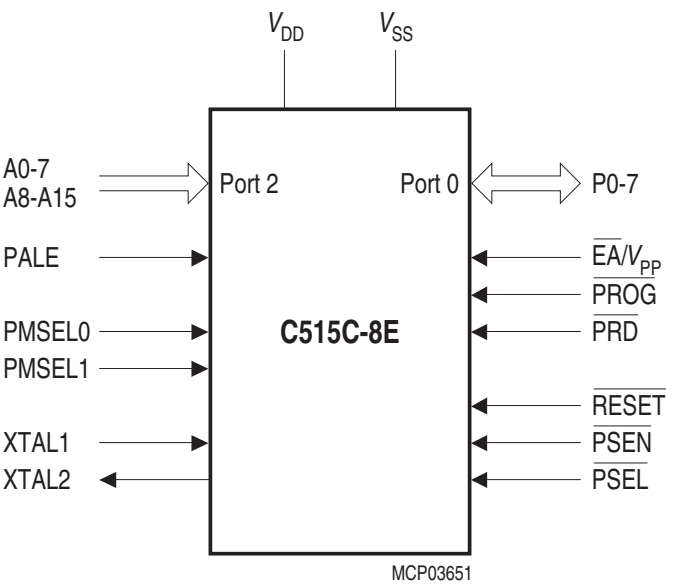


Figure 25 Programming Mode Configuration of the C515C-8E

C515C-8E Pin Configuration in Programming Mode

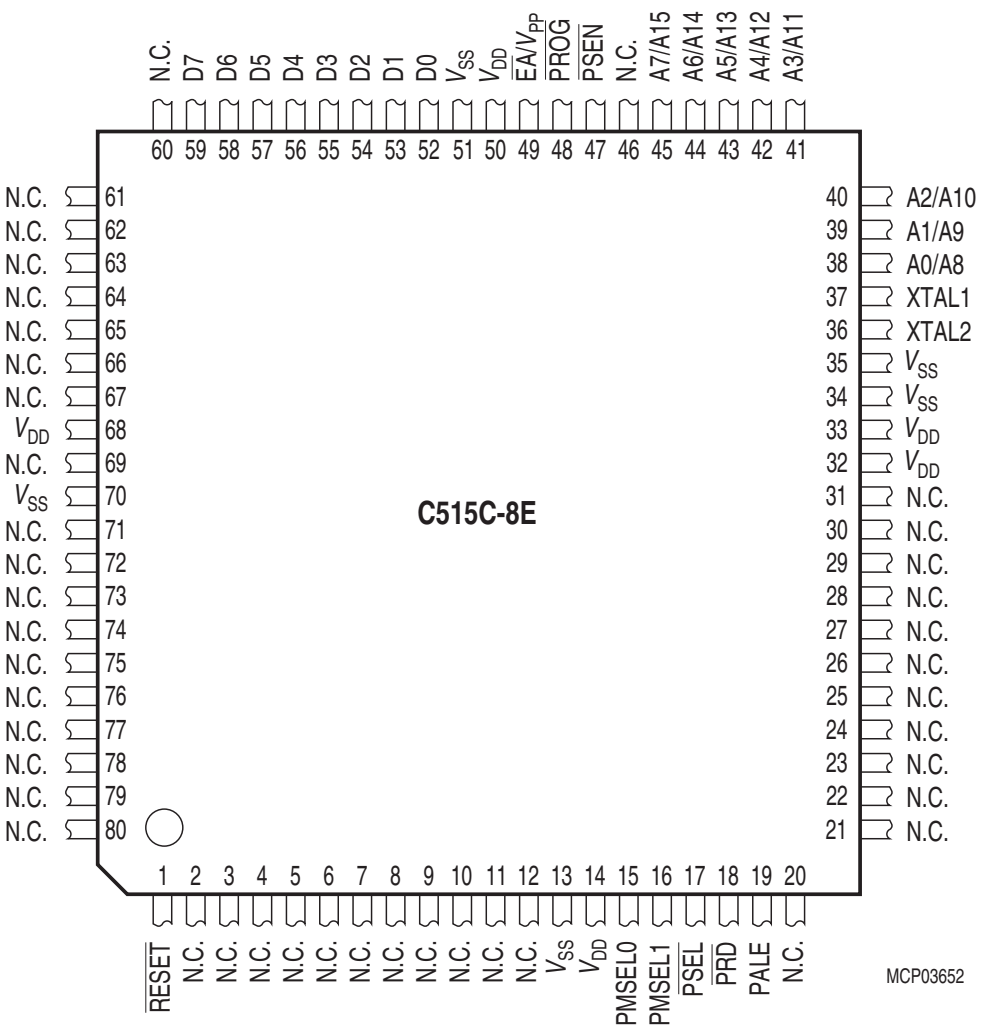


Figure 26 **P-MQFP-80-1 Pin Configuration of the C515C-8E in Programming Mode** (top view)

The following **Table 12** contains the functional description of all C515C-8E pins which are required for OTP memory programming.

Table 12 Pin Definitions and Functions in Programming Mode

Symbol	Pin Number	I/O[1)]	Function
$\overline{\text{RESET}}$	1	I	**Reset** This input must be at static “0” (active) level during the whole programming mode.
PMSEL0 PMSEL1	15 16	I I	**Programming mode selection pins** These pins are used to select the different access modes in programming mode. PMSEL1,0 must satisfy a setup time to the rising edge of PALE. When the logic level of PMSEL1,0 is changed, PALE must be at low level.
$\overline{\text{PSEL}}$	17	I	**Basic programming mode select** This input is used for the basic programming mode selection and must be switched according **Figure 27**.
$\overline{\text{PRD}}$	18	I	**Programming mode read strobe** This input is used for read access control for OTP memory read, version byte read, and lock bit read operations.
PALE	19	I	**Programming address latch enable** PALE is used to latch the high address lines. The high address lines must satisfy a setup and hold time to/from the falling edge of PALE. PALE must be at low level whenever the logic level of PMSEL1,0 is changed.
XTAL2	36	I	**XTAL2** Input to the oscillator amplifier.
XTAL1	37	O	**XTAL1** Output of the inverting oscillator amplifier.

PMSEL1	PMSEL0	Access Mode
0	0	Reserved
0	1	Read version bytes
1	0	Program/read lock bits
1	1	Program/read OTP memory byte

Table 12 Pin Definitions and Functions in Programming Mode (cont'd)

Symbol	Pin Number	I/O[1)]	Function
A0/A8 - A7/A15	38 - 45	I	**Address lines** P2.0-7 are used as multiplexed address input lines A0-A7 and A8-A15. A8-A15 must be latched with PALE.
$\overline{\text{PSEN}}$	47	I	**$\overline{\text{Program store enable}}$** This input must be at static "0" level during the whole programming mode.
$\overline{\text{PROG}}$	48	I	**$\overline{\text{Programming mode write strobe}}$** This input is used in programming mode as a write strobe for OTP memory program and lock bit write operations. During basic programming mode selection a low level must be applied to $\overline{\text{PROG}}$.
$\overline{\text{EA}}/V_{\text{PP}}$	49	I	**$\overline{\text{External Access}}$ / Programming voltage** This pin must be at 11.5 V (V_{PP}) voltage level during programming of an OTP memory byte or lock bit. During an OTP memory read operation this pin must be at high level (V_{IH}). This pin is also used for basic programming mode selection. At basic programming mode selection a low level must be applied to $\overline{\text{EA}}/V_{\text{PP}}$.
D0 - 7	52 - 58	I/O	**Data lines 0-7** During programming mode, data bytes are read or written from or to the C515C-8E via the bidirectional D0-7 which are located at port 0.
V_{SS}	13, 34, 35, 51, 70	–	**Circuit ground potential** must be applied to these pins in programming mode.
V_{DD}	14, 32, 33, 50, 69	–	**Power supply terminal** must be applied to these pins in programming mode.
N.C.	2-12, 20-31, 46, 60-67, 69, 71-80	–	**Not Connected** These pins should not be connected in programming mode.

1) I = Input; O = Output

C515C-8E Basic Programming Mode Selection

The basic programming mode selection scheme is shown in **Figure 27**.

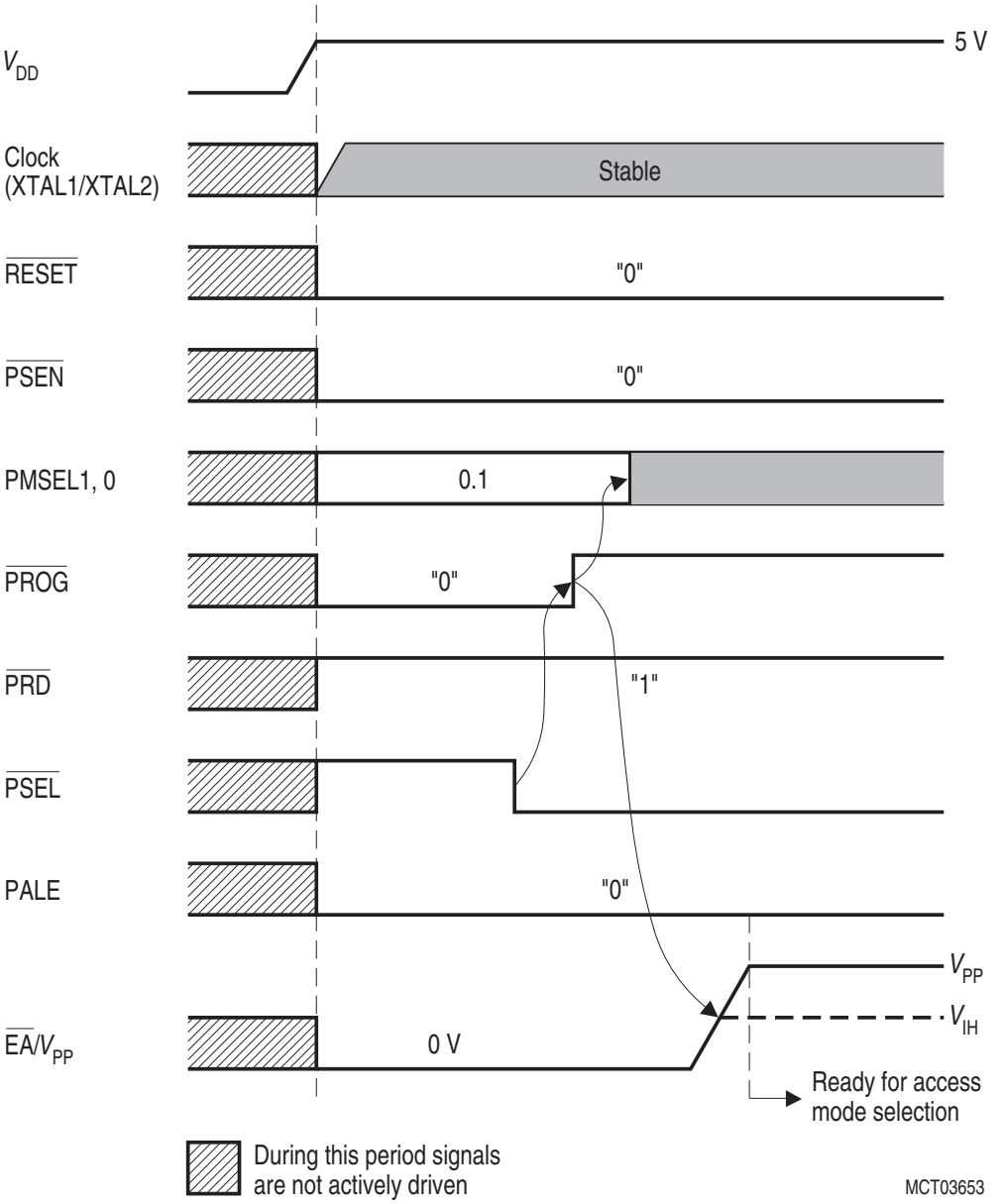


Figure 27 C515C-8E Basic Programming Mode Selection

Table 13 Access Modes Selection

Access Mode	$\overline{EA}$/ V_{PP}	$\overline{PROG}$	$\overline{PRD}$	PMSEL		Address (Port 2)	Data (Port 0)
				1	0		
Program OTP memory byte	V_{PP}	⊓	H	H	H	A0-7 A8-15	D0-7
Read OTP memory byte	V_{IH}	H	⊓				
Program OTP lock bits	V_{PP}	⊓	H	H	L	–	D1, D0 see Table 14
Read OTP lock bits	V_{IH}	H	⊓				
Read OTP version byte	V_{IH}	H	⊓	L	H	Byte addr. of version byte	D0-7

C515C-8E Lock Bits Programming / Read

The C515C-8E has two programmable lock bits which, when programmed according Table 14, provide four levels of protection for the on-chip OTP code memory. The state of the lock bits can also be read.

Table 14 Lock Bit Protection Types

Lock Bits at D1, D0		Protection Level	Protection Type
D1	D0		
1	1	Level 0	The OTP lock feature is disabled. During normal operation of the C515C-8E, the state of the $\overline{EA}$ pin is not latched on reset.
1	0	Level 1	During normal operation of the C515C-8E, MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset. An OTP memory read operation is only possible according to ROM verification mode 2, as it is defined for a protected ROM version of the C515C-8R. Further programming of the OTP memory is disabled (reprogramming security).
0	1	Level 2	Same as level 1, but also OTP memory read operation using ROM verification mode 2 is disabled.
0	0	Level 3	Same as level 2; but additionally external code execution by setting $\overline{EA}$ = low during normal operation of the C515C-8E is no more possible. External code execution, which is initiated by an internal program (e.g. by an internal jump instruction above the ROM boundary), is still possible.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	-65	150	°C	–
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	V_{DD} + 0.5	V	–
Input current on any pin during overload condition	–	-10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	|100 mA|	mA	–
Power dissipation	P_{DISS}	–	1	W	–

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_{DD}	4.25	5.5	V	Active mode, f_{OSCmax} = 10 MHz
		2	5.5	V	Power Down mode
Ground voltage	V_{SS}	0		V	Reference voltage
Ambient temperature:				°C	–
SAB-C515C	T_A	0	70		
SAF-C505	T_A	-40	85		
SAH-C505	T_A	-40	110		
Analog reference voltage	V_{AREF}	4	V_{DD} + 0.1	V	–
Analog ground voltage	V_{AGND}	V_{SS} - 0.1	V_{SS} + 0.2	V	–
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	–
XTAL clock	f_{OSC}	2	10	MHz	–

DC Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltages all except $\overline{EA}$, $\overline{RESET}$, $\overline{HWPD}$ $\overline{EA}$ pin $\overline{RESET}$ and $\overline{HWPD}$ pins Port 5 in CMOS mode	 V_{IL} V_{IL1} V_{IL2} V_{ILC}	 -0.5 -0.5 -0.5 -0.5	 0.2 V_{DD} - 0.1 0.2 V_{DD} - 0.3 0.2 V_{DD} + 0.1 0.3 V_{DD}	V	–
Input high voltages all except XTAL2, $\overline{RESET}$, and $\overline{HWPD}$) XTAL2 pin $\overline{RESET}$ and $\overline{HWPD}$ pins Port 5 in CMOS mode	 V_{IH} V_{IH1} V_{IH2} V_{IHC}	 0.2 V_{DD} + 0.9 0.7 V_{DD} 0.6 V_{DD} 0.7 V_{DD}	 V_{DD} + 0.5 V_{DD} + 0.5 V_{DD} + 0.5 V_{DD} + 0.5	V	–
Output low voltages Ports 1, 2, 3, 4, 5, 7 (incl. CMOS) Port 0, ALE, $\overline{PSEN}$, $\overline{CPUR}$ P4.1, P4.3 in push-pull mode	 V_{OL} V_{OL1} V_{OL3}	 – – –	 0.45 0.45 0.45	V	 I_{OL} = 1.6 mA[1)] I_{OL} = 3.2 mA[1)] I_{OL} = 3.75 mA[1)]
Output high voltages Ports 1, 2, 3, 4, 5, 7 Port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{CPUR}$ Port 5 in CMOS mode P4.1, P4.3 in push-pull mode	 V_{OH} V_{OH2} V_{OHC} V_{OH3}	 2.4 0.9 V_{DD} 2.4 0.9 V_{DD} 0.9 V_{DD} 0.9 V_{DD}	 – – – – – –	V	 I_{OH} = -80 µA I_{OH} = -10 µA I_{OH} = -800 µA I_{OH} = -80 µA[2)] I_{OH} = -800 µA I_{OH} = -833 µA
Logic 0 input current Ports 1, 2, 3, 4, 5, 7	I_{IL}	-10	-70	µA	V_{IN} = 0.45 V
Logical 0-to-1 transition current Ports 1, 2, 3, 4, 5, 7	I_{TL}	-65	-650	µA	V_{IN} = 2 V
Input leakage current Port 0, $\overline{EA}$, P6, $\overline{HWPD}$, AIN0-7	I_{LI}	–	±1	µA	0.45 < V_{IN} < V_{DD}
Input low current To $\overline{RESET}$ for reset XTAL2 $\overline{PE}$/SWD	 I_{LI2} I_{LI3} I_{LI4}	 – – –	 -100 -15 -20	µA	 V_{IN} = 0.45 V V_{IN} = 0.45 V V_{IN} = 0.45 V
Pin capacitance	C_{IO}	–	10	pF	f_c = 1 MHz, T_A = 25 °C
Overload current	I_{OV}	–	±5	mA	[3)4)]
Programming voltage	V_{PP}	10.9	12.1	V	11.5 V ± 5%

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt-trigger, or use an address latch with a Schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{\text{PSEN}}$ to momentarily fall below the 0.9 V_{DD} specification when the address lines are stabilizing.

3) Overload conditions under operating conditions occur if the voltage on the respective pin exceeds the specified operating range (i.e. $V_{OV} > V_{DD} + 0.5$ V or $V_{OV} < V_{SS} - 0.5$ V). The absolute sum of input overload currents on all port pins may not exceed **50 mA**. The supply voltage (V_{DD} and V_{SS}) must remain within the specified limits.

4) Not 100% tested, guaranteed by design characterization.

Power Supply Current

Parameter			Sym-bol	Limit Values		Unit	Test Condition
				typ.[1]	max.[2]		
Active mode	C515C-8R/ C515C-LM	6 MHz 10 MHz	I_{DD}	11.97 18.81	13.74 21.10	mA	[3]
	C515C-8E	6 MHz 10 MHz	I_{DD}	11.3 17.66	12.94 20.10	mA	
Idle mode	C515C-8R/ C515C-LM	6 MHz 10 MHz	I_{DD}	6.9 10.46	7.87 11.87	mA	[4]
	C515C-8E	6 MHz 10 MHz	I_{DD}	3.95 4.71	4.70 5.50	mA	
Active mode with slow-down enabled	C515C-8R/ C515C-LM	6 MHz 10 MHz	I_{DD}	4.06 4.62	5.03 5.75	mA	[5]
	C515C-8E	6 MHz 10 MHz	I_{DD}	4.01 4.65	4.77 5.53	mA	
Idle mode with slow-down enabled	C515C-8R/ C515C-LM	6 MHz 10 MHz	I_{DD}	3.54 3.86	4.46 4.90	mA	[6]
	C515C-8E	6 MHz 10 MHz	I_{DD}	3.62 4.14	4.21 4.77	mA	
Power-down mode	C515C-8R/ C515C-LM		I_{PD}	26	42.9	µA	V_{DD} = 2 … 5.5 V [7]
	C515C-8E		I_{PD}	11.14	30	µA	
At $\overline{EA}/V_{PP}$ in programming mode	C515C-8E		I_{DDP}	–	30	mA	–

[1] The typical I_{DD} values are periodically measured at T_A = +25 °C and V_{DD} = 5 V but not 100% tested.

[2] The maximum I_{DD} values are measured under worst case conditions (T_A = 0 °C or -40 °C and V_{DD} = 5.5 V)

[3] I_{DD} (active mode) is measured with:
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} - 0.5 V; XTAL1 = N.C.;
$\overline{EA}$ = $\overline{PE}$/SWD = Port 0 = Port 6 = V_{DD}; $\overline{HWPD}$ = V_{DD}; $\overline{RESET}$ = V_{SS}; all other pins are disconnected.

[4] I_{DD} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} - 0.5 V; XTAL1 = N.C.;
$\overline{RESET}$ = V_{DD}; $\overline{EA}$ = V_{SS}; Port0 = V_{DD}; all other pins are disconnected;

[5] I_{DD} (active mode with slow-down mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} - 0.5 V; XTAL1 = N.C.;
$\overline{RESET}$ = V_{DD}; all other pins are disconnected; the microcontroller is put into slow-down mode by software.

6) I_{DD} (idle mode with slow-down mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} - 0.5 V; XTAL1 = N.C.;
$\overline{\text{RESET}}$ = V_{DD}; $\overline{\text{EA}}$ = V_{SS}; Port0 = V_{DD}; all other pins are disconnected; the microcontroller is put into idle mode with slow-down enabled by software.

7) I_{PD} (power-down mode) is measured under following conditions:
$\overline{\text{EA}}$ = $\overline{\text{RESET}}$ = Port 0 = Port 6 = V_{DD}; XTAL1 = N.C.; XTAL2 = V_{SS}; $\overline{\text{PE}}$/SWD = V_{SS}; $\overline{\text{HWPD}}$ = V_{DD}; V_{AGND} = V_{SS}; V_{AREF} = V_{DD}; all other pins are disconnected.
I_{PD} (hardware power-down mode) is independent of any particular pin connection.

Power Supply Current Calculation Formulas

Parameter		Symbol	Formula
Active mode	C515C-8R/ C515C-LM	$I_{DD\ typ}$ $I_{DD\ max}$	$1.71 \times f_{OSC} + 1.71$ $1.84 \times f_{OSC} + 2.7$
	C515C-8E	$I_{DD\ typ}$ $I_{DD\ max}$	$1.59 \times f_{OSC} + 1.76$ $1.79 \times f_{OSC} + 2.2$
Idle mode	C515C-8R/ C515C-LM	$I_{DD\ typ}$ $I_{DD\ max}$	$0.89 \times f_{OSC} + 1.56$ $1.00 \times f_{OSC} + 1.87$
	C515C-8E	$I_{DD\ typ}$ $I_{DD\ max}$	$0.19 \times f_{OSC} + 2.81$ $0.20 \times f_{OSC} + 3.5$
Active mode with slow-down enabled	C515C-8R/ C515C-LM	$I_{DD\ typ}$ $I_{DD\ max}$	$0.14 \times f_{OSC} + 3.22$ $0.18 \times f_{OSC} + 3.95$
	C515C-8E	$I_{DD\ typ}$ $I_{DD\ max}$	$0.16 \times f_{OSC} + 3.05$ $0.19 \times f_{OSC} + 3.63$
Idle mode with slow-down enabled	C515C-8R/ C515C-LM	$I_{DD\ typ}$ $I_{DD\ max}$	$0.08 \times f_{OSC} + 3.06$ $0.11 \times f_{OSC} + 3.8$
	C515C-8E	$I_{DD\ typ}$ $I_{DD\ max}$	$0.13 \times f_{OSC} + 2.84$ $0.14 \times f_{OSC} + 3.37$

Note: f_{OSC} is the oscillator frequency in MHz. I_{DD} values are given in mA.

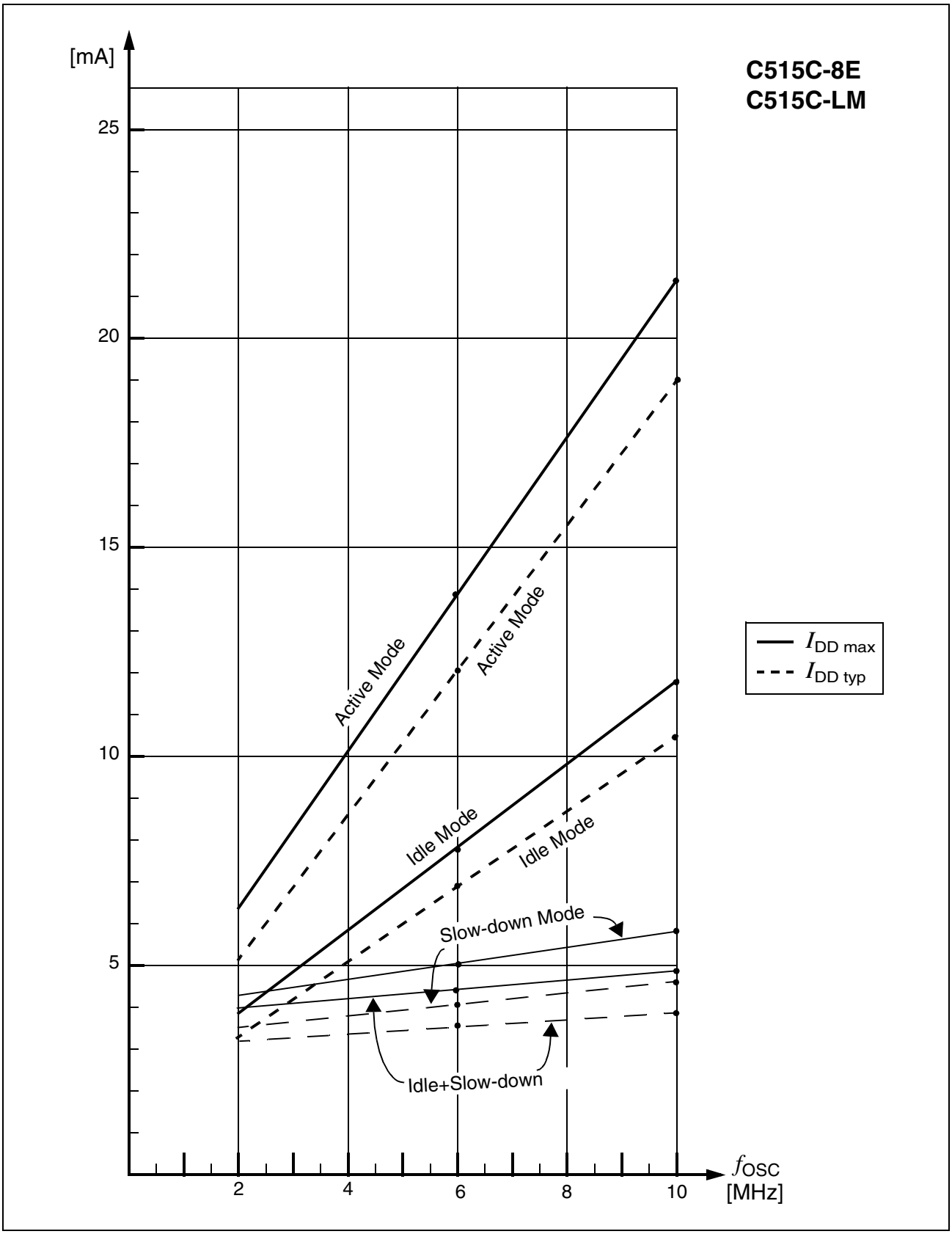


Figure 28 I_{DD} Diagrams of C515C-8R/C515C-LM

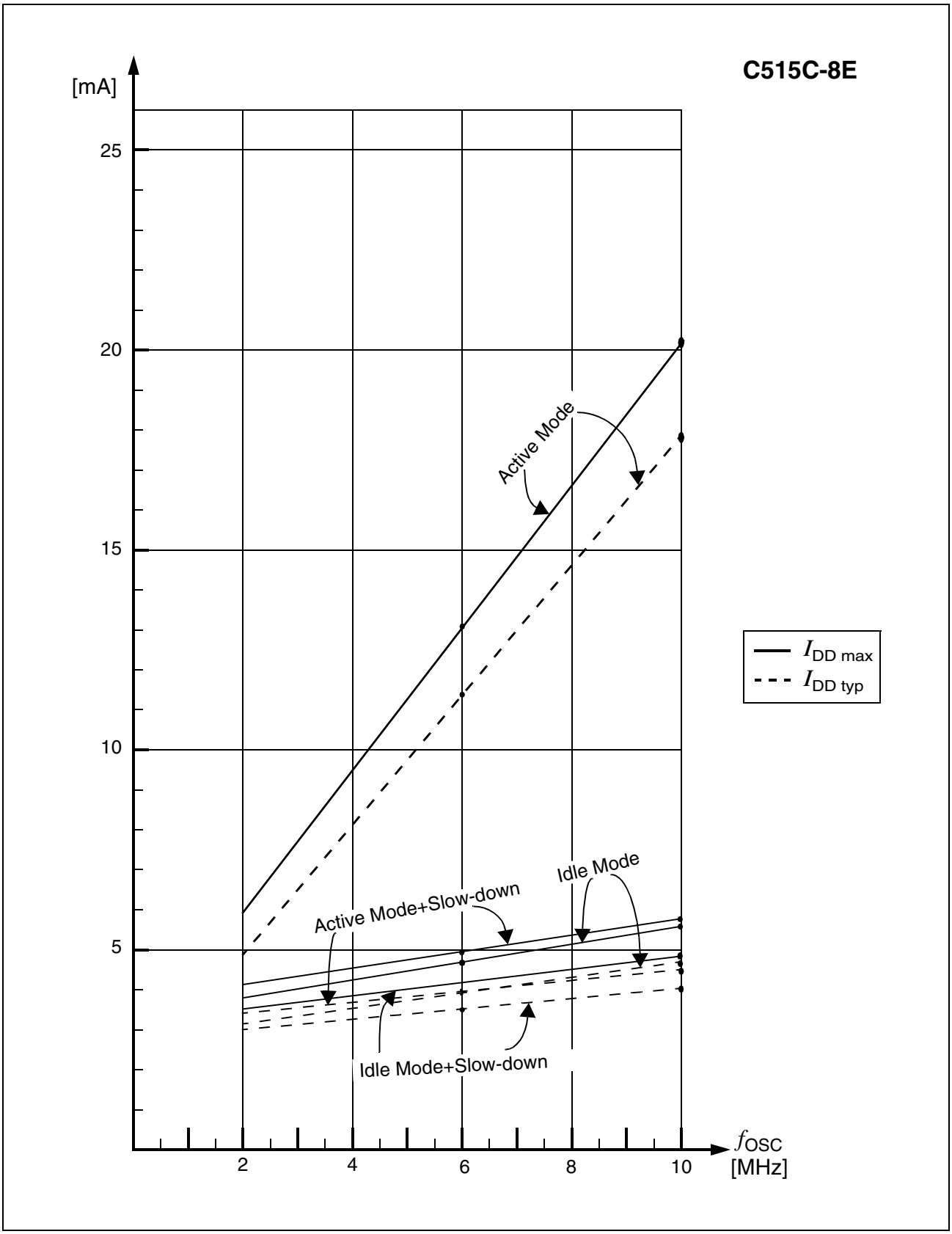


Figure 29 I_{DD} Diagrams of C515C-8E

A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S	–	$16 \times t_{IN}$ $8 \times t_{IN}$	ns	Prescaler ÷ 8 Prescaler ÷ 4 2)
Conversion cycle time	t_{ADCC}	–	$96 \times t_{IN}$ $48 \times t_{IN}$	ns	Prescaler ÷ 8 Prescaler ÷ 4 3)
Total unadjusted error	T_{UE}	–	±2	LSB	4)
Internal resistance of reference voltage source	R_{AREF}	–	t_{ADC} / 250 - 0.25	kΩ	t_{ADC} in [ns] 5)6)
Internal resistance of analog source	R_{ASRC}	–	t_S / 500 - 0.25	kΩ	t_S in [ns] 2)6)
ADC input capacitance	C_{AIN}	–	50	pF	6)

1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

Clock Calculation Table

Clock Prescaler Ratio	ADCL	t_{ADC}	t_S	t_{ADCC}
÷8	1	$8 \times t_{IN}$	$16 \times t_{IN}$	$96 \times t_{IN}$
÷4	0	$4 \times t_{IN}$	$8 \times t_{IN}$	$48 \times t_{IN}$

Further timing conditions: $t_{ADC\ min} = 500$ ns
$t_{IN} = 1 / f_{OSC} = t_{CLP}$

AC Characteristics (Operating Conditions apply)

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		10-MHz Clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP = 2 MHz to 10 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	60	–	CLP - 40	–	ns
Address setup to ALE	t_{AVLL}	15	–	TCL_{Hmin} - 25	–	ns
Address hold after ALE	t_{LLAX}	15	–	TCL_{Hmin} - 25	–	ns
ALE to valid instruction in	t_{LLIV}	–	113	–	2 CLP - 87	ns
ALE to $\overline{PSEN}$	t_{LLPL}	20	–	TCL_{Lmin} - 20	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	115	–	CLP + TCL_{Hmin} - 30	–	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	75	–	CLP + TCL_{Hmin} - 65	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} [1)]	–	30	–	TCL_{Lmin} - 10	ns
Address valid after $\overline{PSEN}$	t_{PXAV} [1)]	35	–	TCL_{Lmin} - 5	–	ns
Address to valid instruction in	t_{AVIV}	–	180	–	2 CLP + TCL_{Hmin} - 60	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0		0	–	ns

1) Interfacing the C515C to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		10-MHz Clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 10 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	230	–	3 CLP - 70	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	230	–	3 CLP - 70	–	ns
Address hold after ALE	t_{LLAX2}	48	–	CLP - 15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	150	–	2 CLP + TCL_{Hmin} - 90	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	80	–	CLP - 20	ns
ALE to valid data in	t_{LLDV}	–	267	–	4 CLP - 133	ns
Address to valid data in	t_{AVDV}	–	285	–	4 CLP + TCL_{Hmin} - 155	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	90	190	CLP + TCL_{Lmin} - 50	CLP + TCL_{Lmin} + 50	ns
Address valid to $\overline{WR}$	t_{AVWL}	103	–	2 CLP - 97	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	15	65	TCL_{Hmin} - 25	TCL_{Hmin} + 25	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	TCL_{Lmin} - 35	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	218	–	3 CLP + TCL_{Lmin} - 122	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	13	–	TCL_{Hmin} - 27	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

SSC Interface Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock Cycle Time: Master Mode Slave Mode	 t_{SCLK} t_{SCLK}	 0.4 1.0	 – –	 µs µs
Clock high time	t_{SCH}	360	–	ns
Clock low time	t_{SCL}	360	–	ns
Data output delay	t_D	–	100	ns
Data output hold	t_{HO}	0	–	ns
Data input setup	t_S	100	–	ns
Data input hold	t_{HI}	100	–	ns
TC bit set delay	t_{DTC}	–	8 CLP	ns

External Clock Drive at XTAL2

Parameter	Symbol	CPU Clock = 10 MHz Duty cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 2 to 10 MHz		Unit
		min.	max.	min.	max.	
Oscillator period	CLP	100	100	100	500	ns
High time	TCL_H	40	–	40	CLP - TCL_L	ns
Low time	TCL_L	40	–	40	CLP - TCL_H	ns
Rise time	t_R	–	12	–	12	ns
Fall time	t_F	–	12	–	12	ns
Oscillator duty cycle	DC	0.4	0.6	40 / CLP	1 - 40 / CLP	–
Clock cycle	TCL	40	60	CLP × DC_{min}	CLP × DC_{max}	ns

Note: The 10 MHz values in the tables are given as an example for a typical duty cycle variation of the oscillator clock from 0.4 to 0.6.

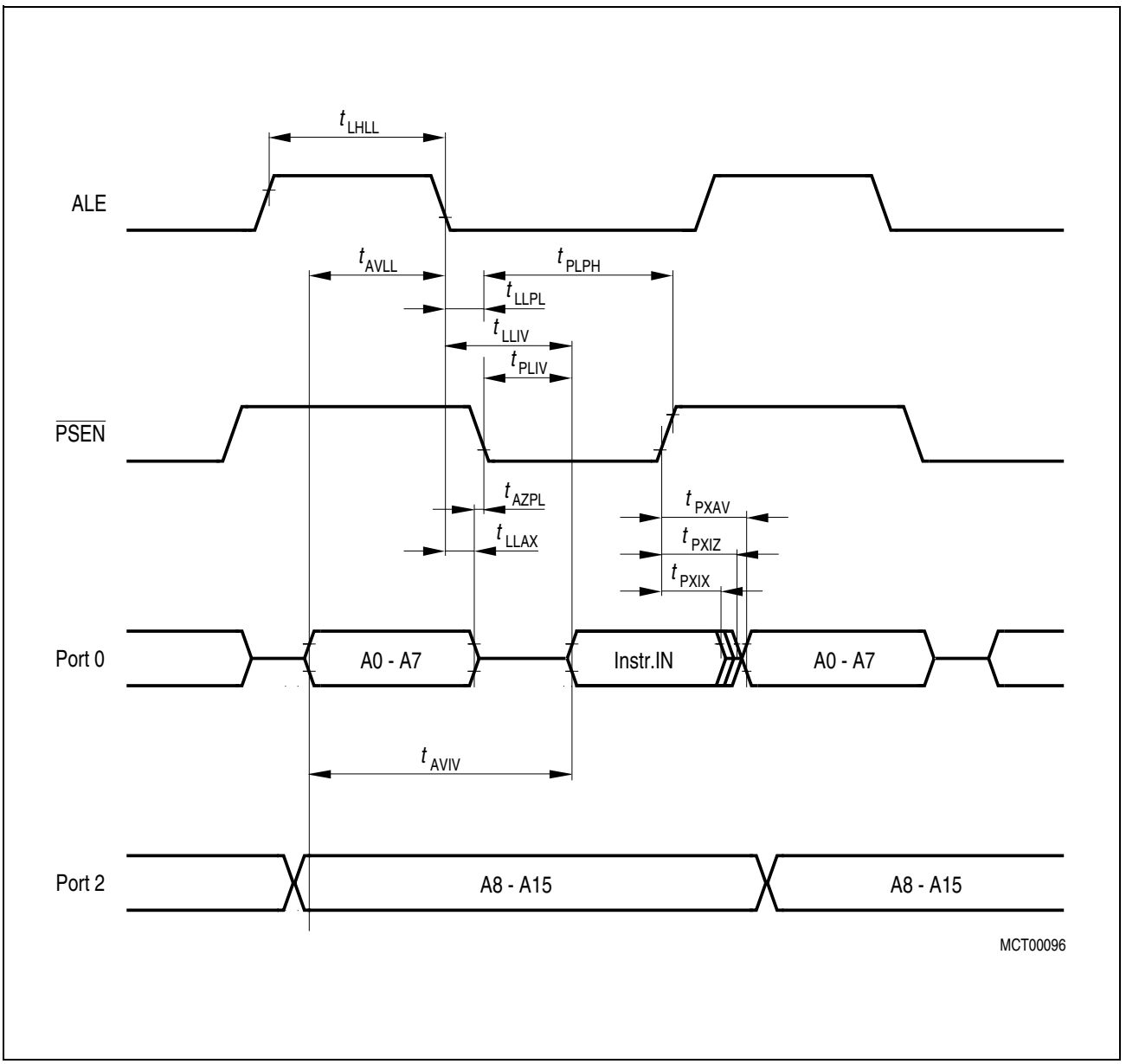


Figure 30 Program Memory Read Cycle

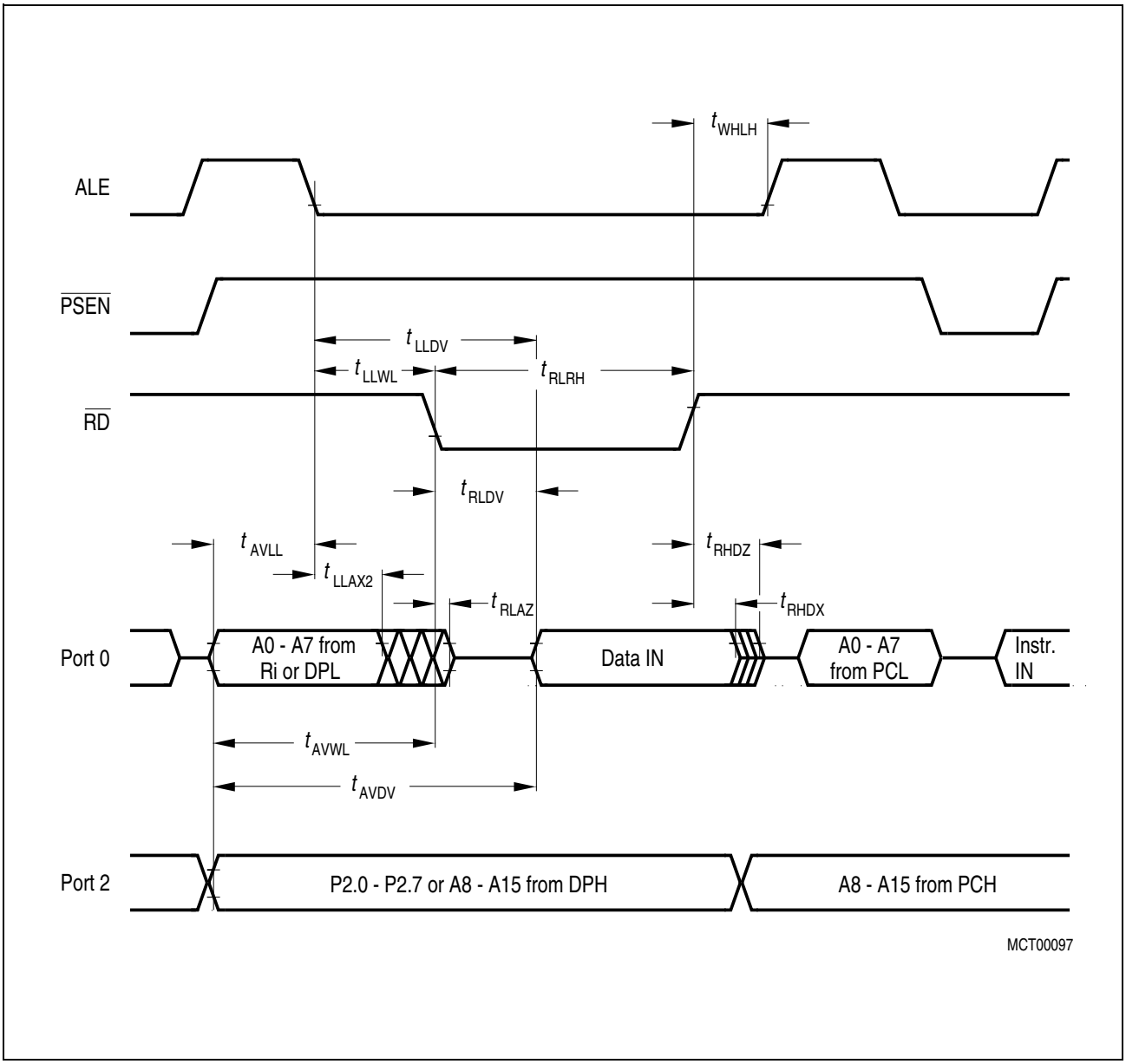


Figure 31 Data Memory Read Cycle

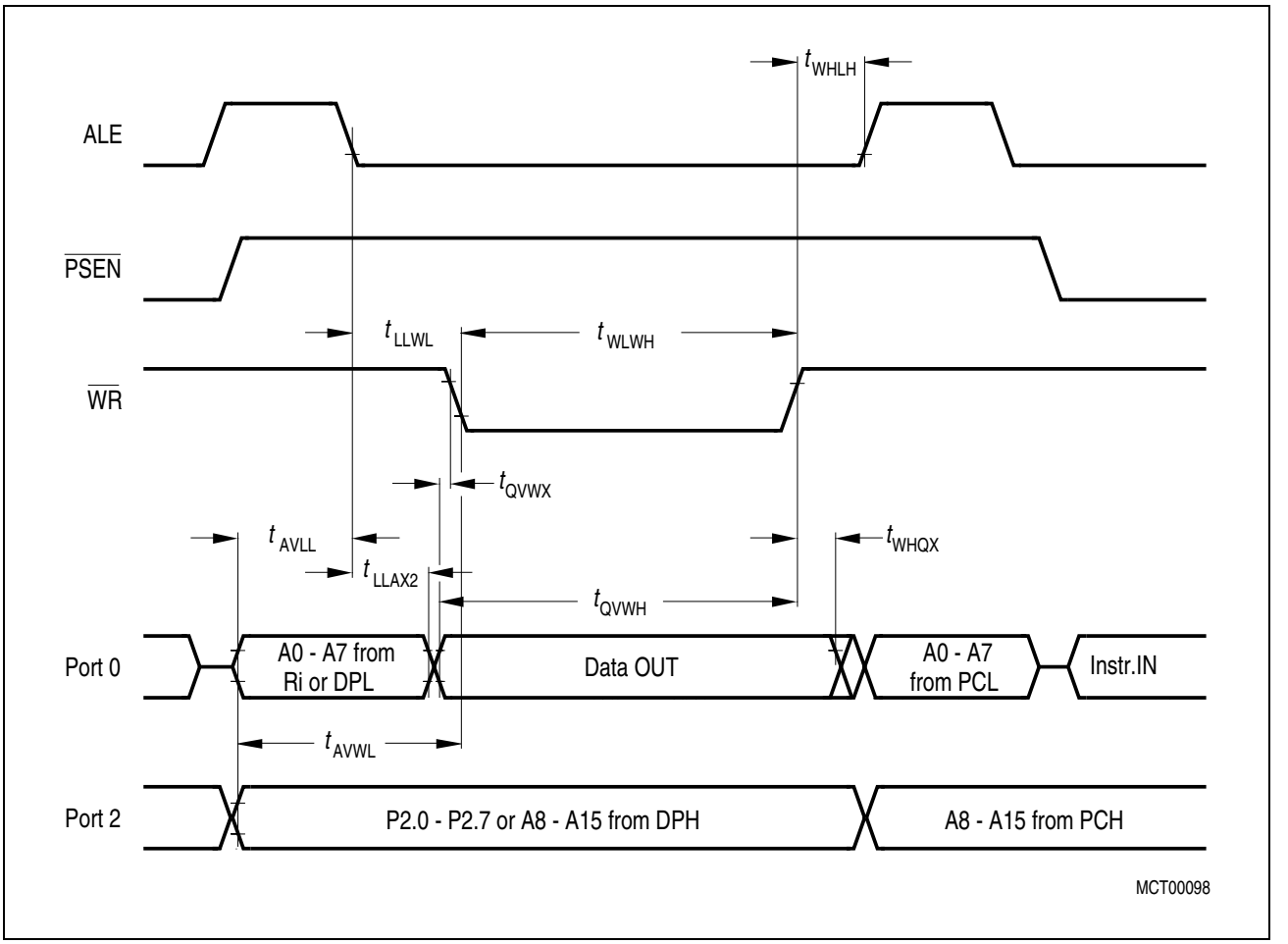


Figure 32 Data Memory Write Cycle

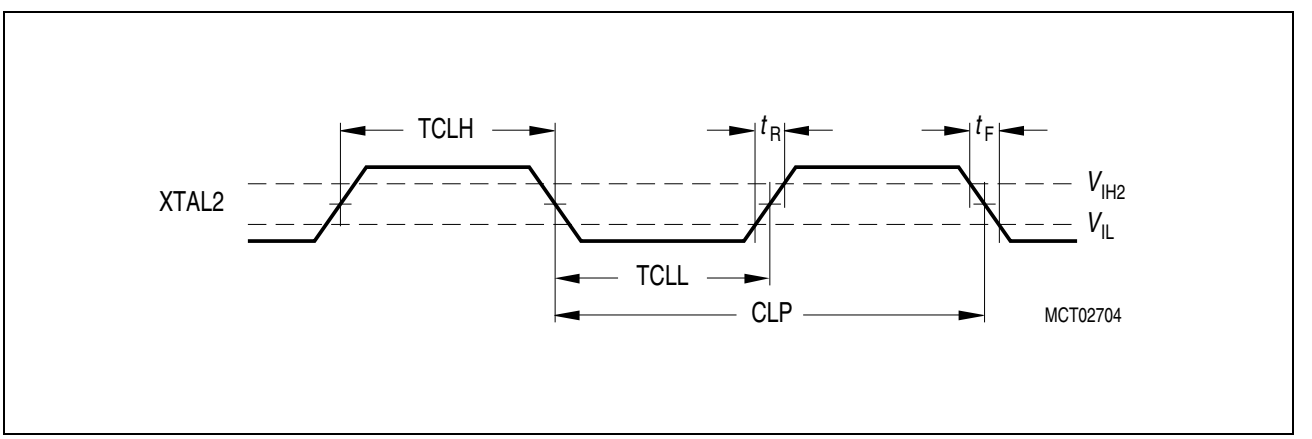


Figure 33 External Clock Drive at XTAL2

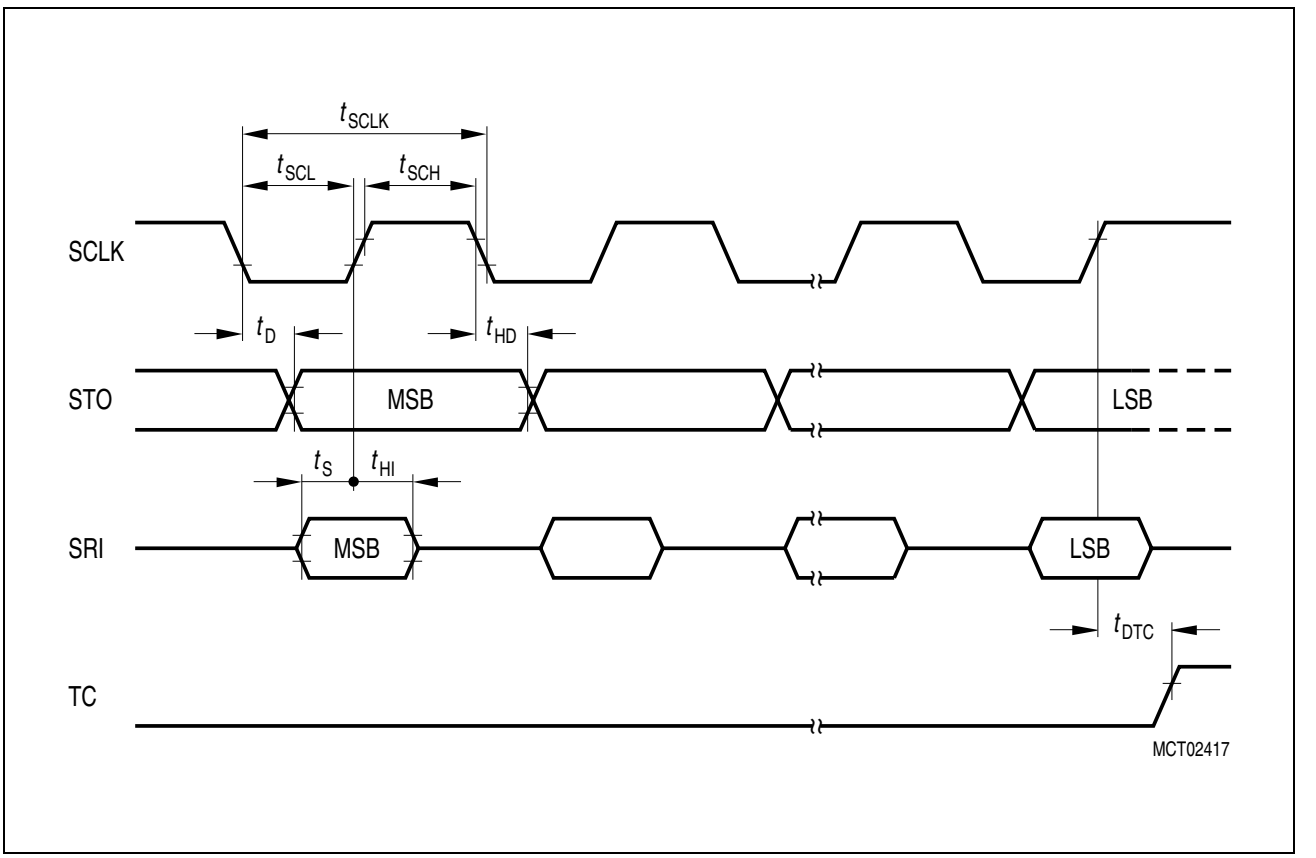


Figure 34 SSC Timing

Notes:

1. *Shown is the data/clock relationship for CPOL = CPHA = 1. The timing diagram is valid for the other cases accordingly.*
2. *In the case of slave mode and CPHA = 0, the output delay for the MSB applies to the falling edge of $\overline{SLS}$ (if transmitter is enabled).*
3. *In the case of master mode and CPHA = 0, the MSB becomes valid after the data has been written into the shift register, i.e. at least one half SCLK clock cycle before the first clock transition.*

OTP Memory Programming Mode Characteristics

V_{DD} = 5 V ± 10%; V_{PP} = 11.5 V ± 5%; T_A = 25 °C ± 10 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{PAW}	35	–	ns
PMSEL setup to ALE rising edge	t_{PMS}	10	–	ns
Address setup to ALE, $\overline{PROG}$, or $\overline{PRD}$ falling edge	t_{PAS}	10	–	ns
Address hold after ALE, $\overline{PROG}$, or $\overline{PRD}$ falling edge	t_{PAH}	10	–	ns
Address, data setup to PROG or $\overline{PRD}$	t_{PCS}	100	–	ns
Address, data hold after $\overline{PROG}$ or $\overline{PRD}$	t_{PCH}	0	–	ns
PMSEL setup to $\overline{PROG}$ or $\overline{PRD}$	t_{PMS}	10	–	ns
PMSEL hold after $\overline{PROG}$ or $\overline{PRD}$	t_{PMH}	10	–	ns
$\overline{PROG}$ pulse width	t_{PWW}	100	–	µs
$\overline{PRD}$ pulse width	t_{PRW}	100	–	ns
Address to valid data out	t_{PAD}	–	75	ns
$\overline{PRD}$ to valid data out	t_{PRD}	–	20	ns
Data hold after $\overline{PRD}$	t_{PDH}	0	–	ns
Data float after $\overline{PRD}$	t_{PDF}	–	20	ns
$\overline{PROG}$ high between two consecutive $\overline{PROG}$ low pulses	t_{PWH1}	1	–	µs
$\overline{PRD}$ high between two consecutive $\overline{PRD}$ low pulses	t_{PWH2}	100	–	ns
XTAL clock period	t_{CLKP}	2	10	MHz

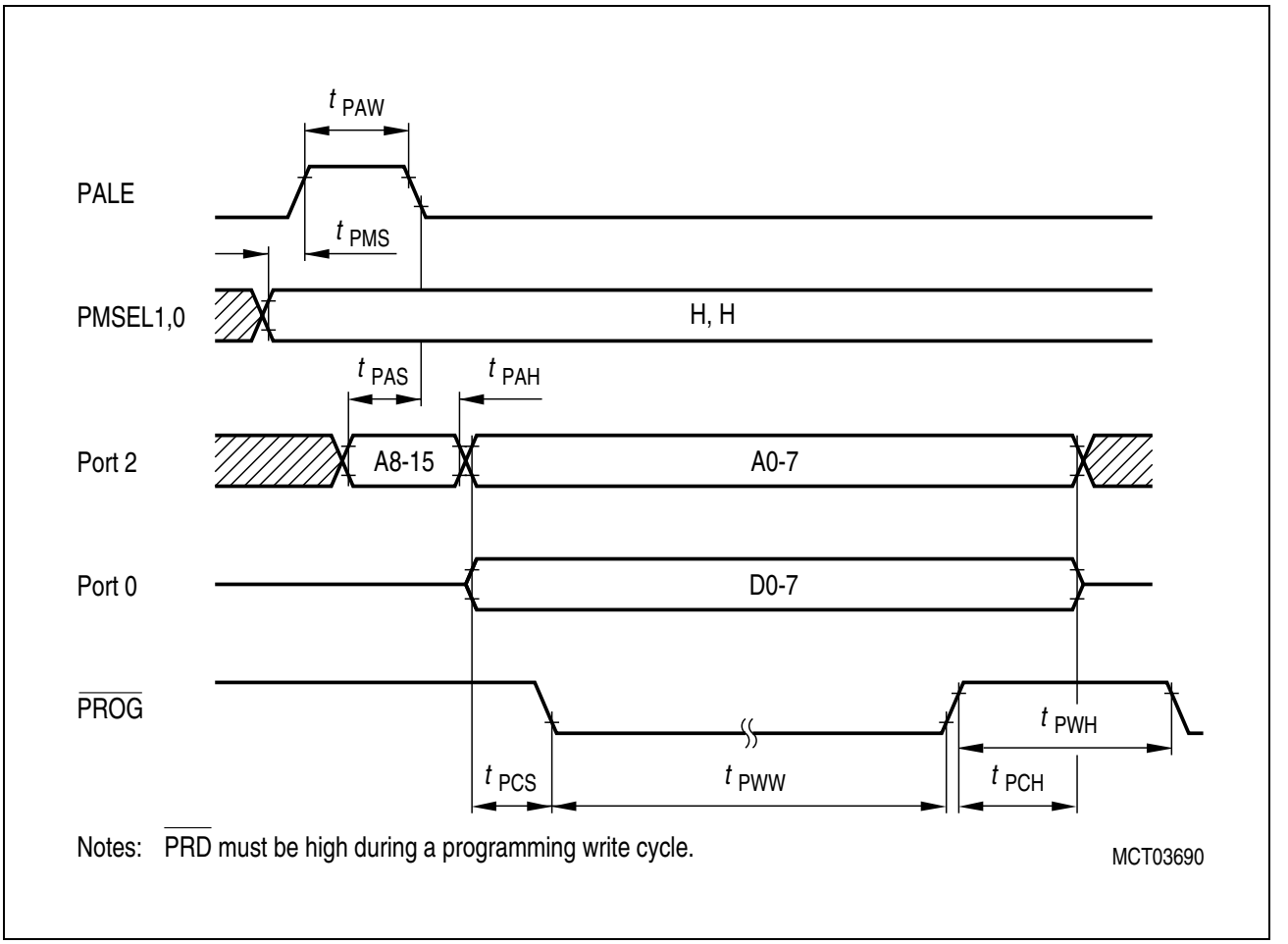


Figure 35 Programming Code Byte - Write Cycle Timing

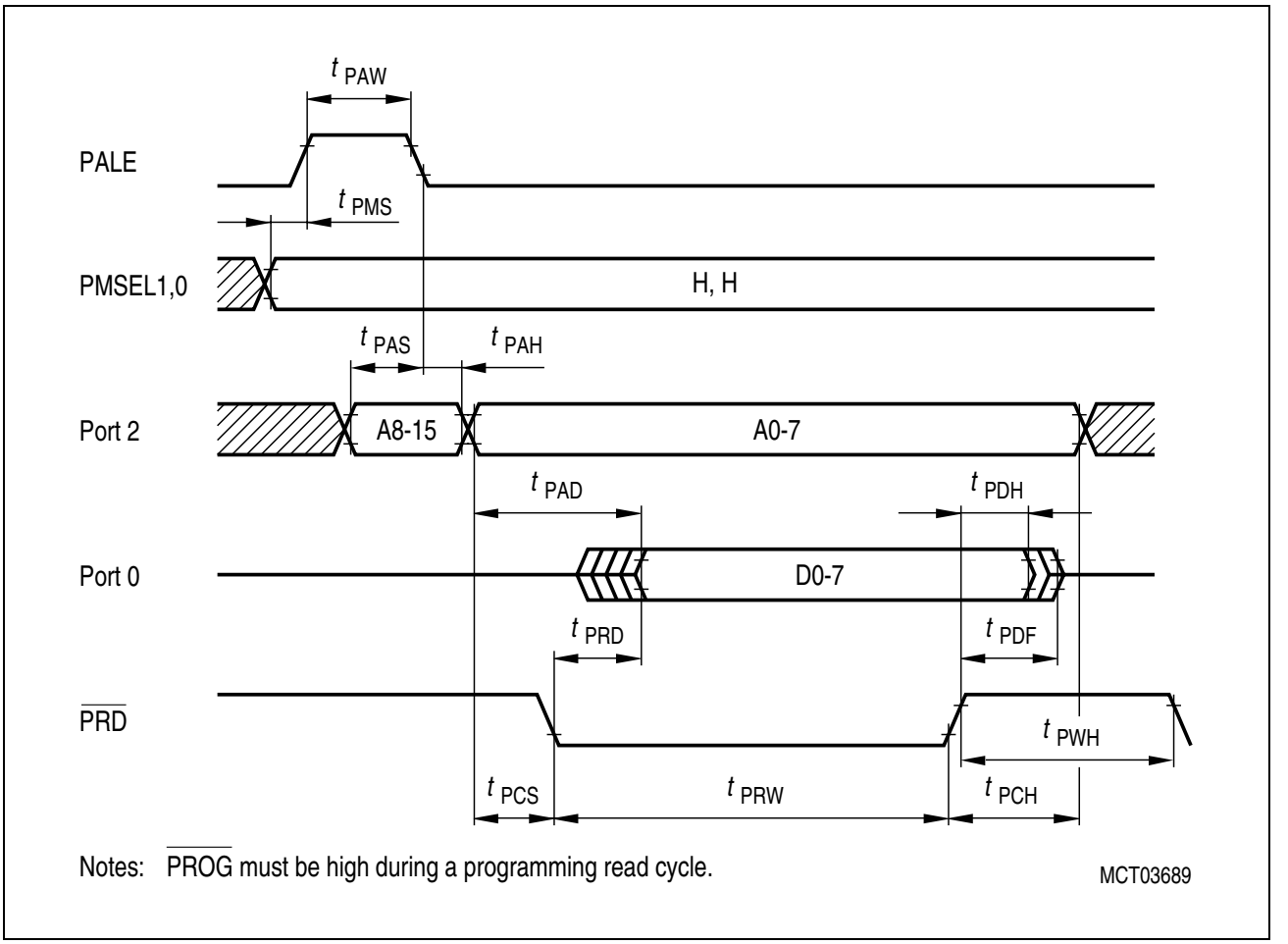


Figure 36 Verify Code Byte - Read Cycle Timing

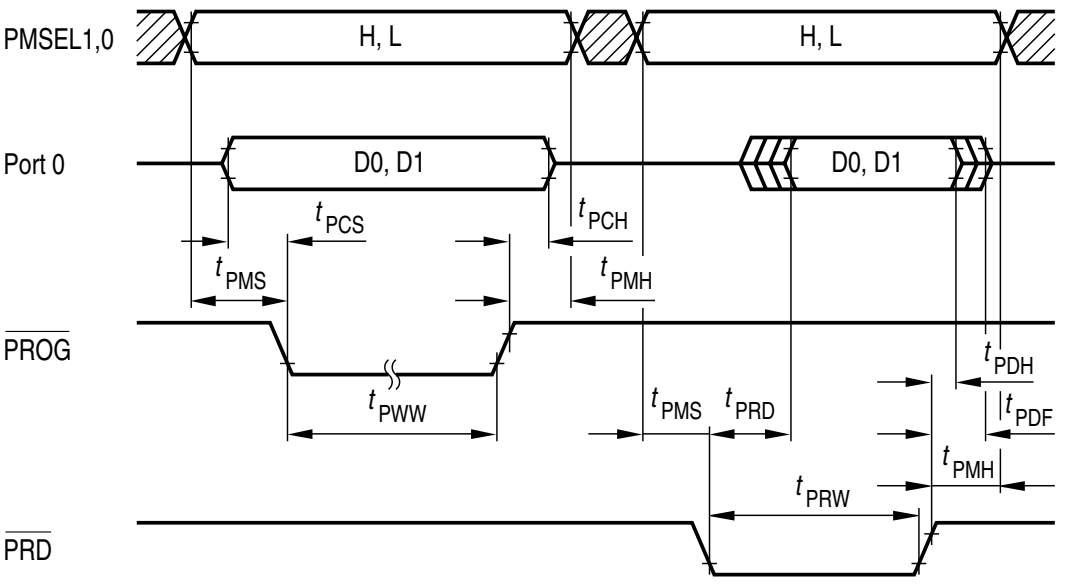
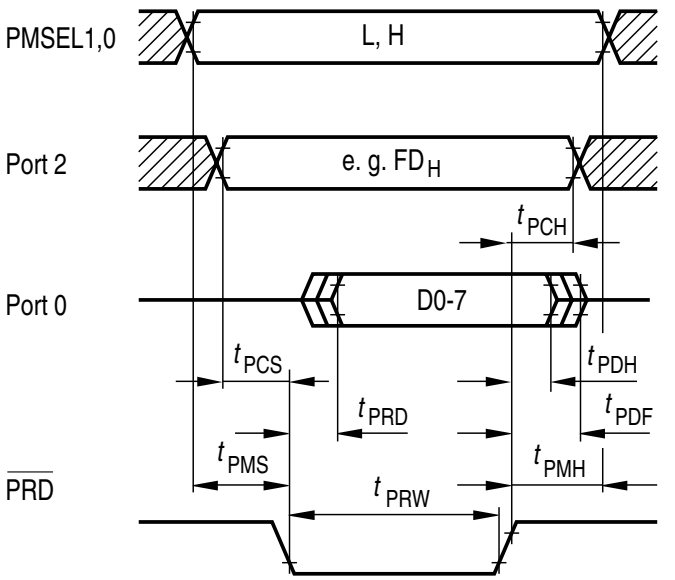


Figure 37 Lock Bit Access Timing



Note: $\overline{\text{PROG}}$ must be high during a programming read cycle.

MCT03394

Figure 38 Version Byte - Read Timing

ROM/OTP Verification Characteristics for C515C-8R / C515C-8E

ROM Verification Mode 1 (C515C-8R)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	5 CLP	ns

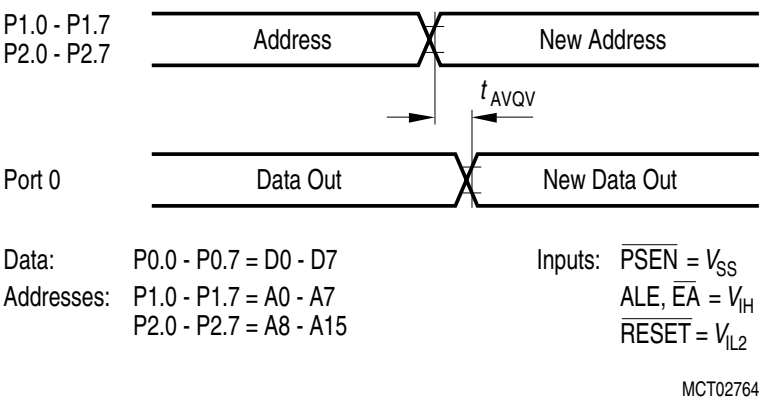


Figure 39 ROM Verification Mode 1

ROM/OTP Verification Mode 2

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
ALE pulse width	t_{AWD}	–	CLP	–	ns
ALE period	t_{ACY}	–	6 CLP	–	ns
Data valid after ALE	t_{DVA}	–	–	2 CLP	ns
Data stable after ALE	t_{DSA}	4 CLP	–	–	ns
P3.5 setup to ALE low	t_{AS}	–	t_{CL}	–	ns
Oscillator frequency	1 / CLP	4	–	6	MHz

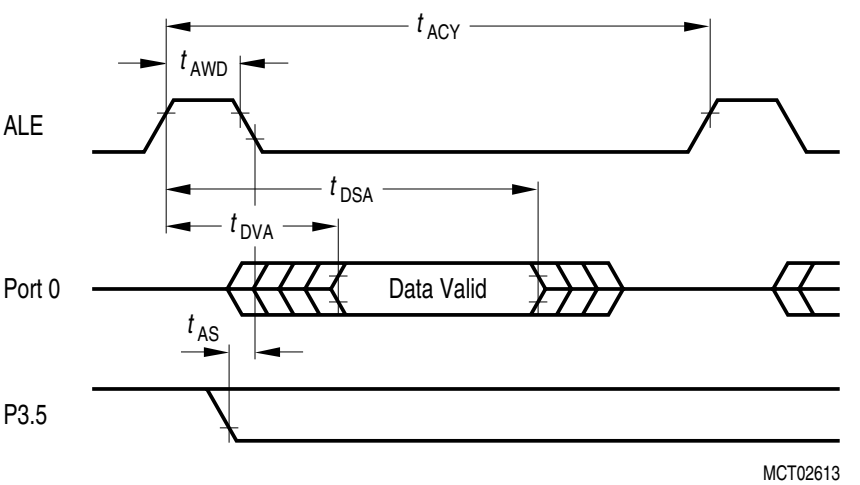
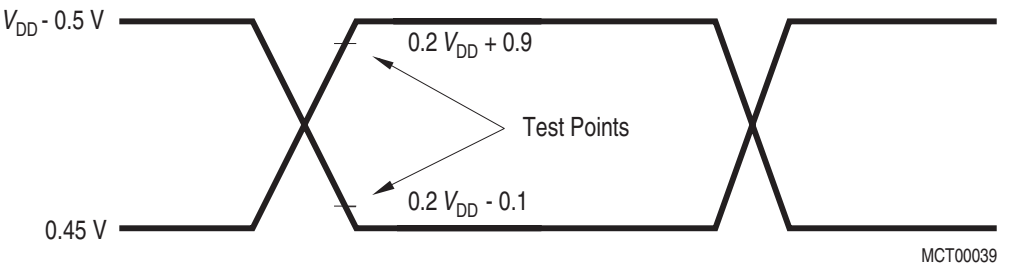
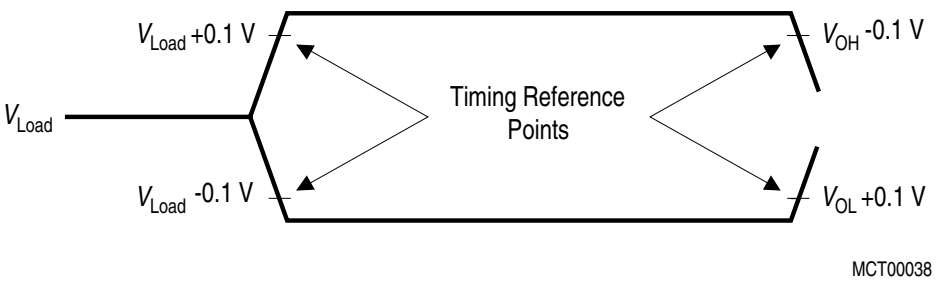


Figure 40 ROM/OTP Verification Mode 2



AC Inputs during testing are driven at V_{DD} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 41 AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20 mA

Figure 42 AC Testing: Float Waveforms

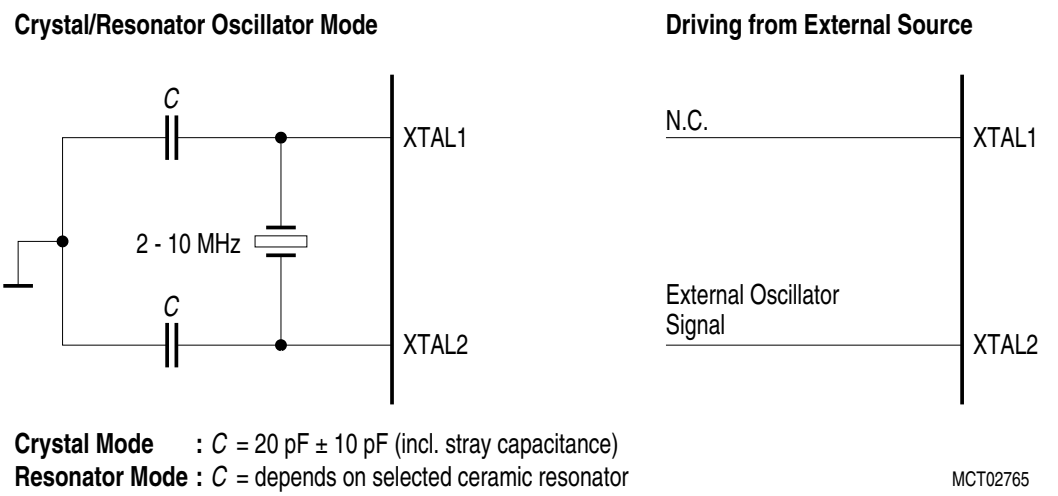
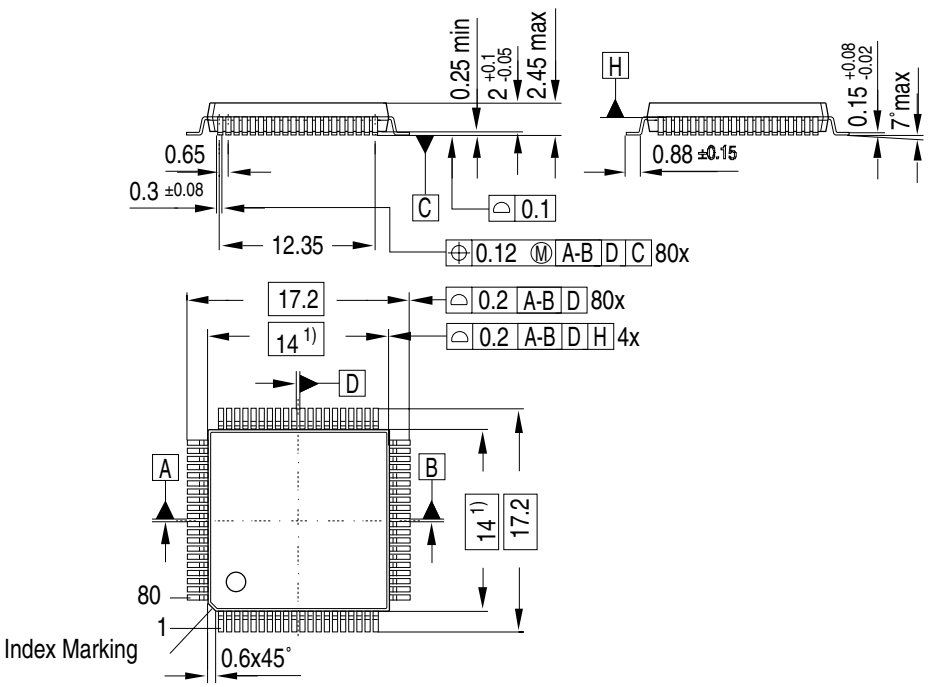


Figure 43 Recommended Oscillator Circuits for Crystal Oscillator

Package Outlines

P-MQFP-80-1
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

GPM05249

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SMD = Surface Mounted Device

Dimensions in mm

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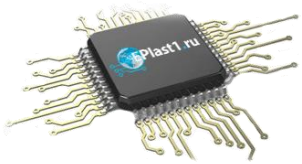

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