# Low Cost, 300 MHz Rail-to-Rail Amplifiers

Data Sheet

# AD8061/AD8062/AD8063

## FEATURES

- Low cost
- Single (AD8061), dual (AD8062)
- Single with disable (AD8063)
- Rail-to-rail output swing
- Low offset voltage: 6 mV
- High speed
  - 300 MHz, −3 dB bandwidth (G = 1)
  - 650 V/µs slew rate
  - 8.5 nV/√Hz at 5 V
  - 35 ns settling time to 0.1% with 1 V step
- Operates on 2.7 V to 8 V supplies
  - Input voltage range = −0.2 V to +3.2 V with $V_S$ = 5 V
- Excellent video specifications ($R_L$ = 150 Ω, G = 2)
  - Gain flatness: 0.1 dB to 30 MHz
  - 0.01% differential gain error
  - 0.04° differential phase error
- 35 ns overload recovery
- Low power
  - 6.8 mA/amplifier typical supply current
  - AD8063 400 µA when disabled

## APPLICATIONS

- Imaging
- Photodiode preamps
- Professional video and cameras
- Handsets
- DVDs/CDs
- Base stations
- Filters
- ADC drivers
- Clock buffers

## CONNECTION DIAGRAMS

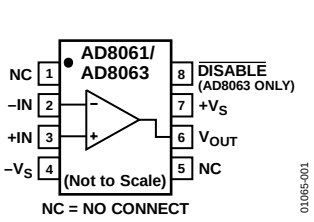


Figure 1. 8-Lead SOIC (R)

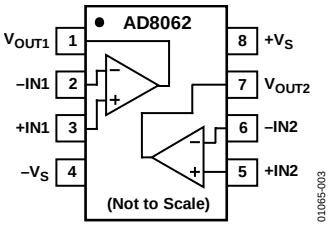


Figure 2. 8-Lead SOIC (R)/MSOP (RM)

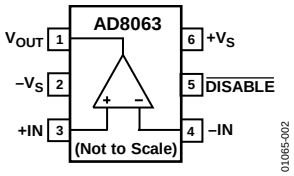


Figure 3. 6-Lead SOIC-23 (RJ)

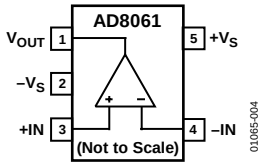


Figure 4. 5-Lead SOIC-23 (RJ)

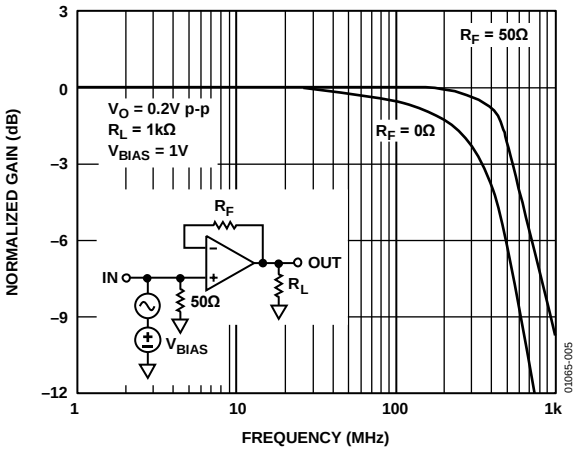


Figure 5. Small Signal Response, $R_F$ = 0 Ω, 50 Ω

## GENERAL DESCRIPTION

The AD8061/AD8062/AD8063 are rail-to-rail output voltage feedback amplifiers offering ease of use and low cost. They have a bandwidth and slew rate typically found in current feedback amplifiers. All have a wide input common-mode voltage range and output voltage swing, making them easy to use on single supplies as low as 2.7 V.

Despite being low cost, the AD8061/AD8062/AD8063 provide excellent overall performance. For video applications, their differential gain and phase errors are 0.01% and 0.04° into a 150 Ω load, along with 0.1 dB flatness out to 30 MHz. Additionally, they offer wide bandwidth to 300 MHz along with 650 V/µs slew rate.

The AD8061/AD8062/AD8063 offer a typical low power of 6.8 mA/amplifier, while being capable of delivering up to 50 mA of load current. The AD8063 has a power-down disable feature that reduces the supply current to 400 µA. These features make the AD8063 ideal for portable and battery-powered applications where size and power are critical.

Rev. J
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## REVISION HISTORY

**5/13—Rev. I to Rev. J**
Added Output Voltage Swing Parameters; Table 1 ... 3
Added Output Voltage Swing Parameters; Table 2 ... 4
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Updated Outline Dimensions ... 19
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Replaced TPC 9 with new graph ... 7

**11/00—Rev. A to Rev. B**

**2/00—Rev. 0 to Rev. A**

**11/99—Revision 0: Initial Version**

# SPECIFICATIONS

$T_A$ = 25°C, $V_S$ = 5 V, $R_L$ = 1 kΩ, $V_O$ = 1 V, unless otherwise noted.

**Table 1.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | G = 1, $V_O$ = 0.2 V p-p | 150 | 320 | | MHz |
| | G = −1, +2, $V_O$ = 0.2 V p-p | 60 | 115 | | MHz |
| −3 dB Large Signal Bandwidth | G = 1, $V_O$ = 1 V p-p | | 280 | | MHz |
| Bandwidth for 0.1 dB Flatness | G = 1, $V_O$ = 0.2 V p-p | | 30 | | MHz |
| Slew Rate | G = 1, $V_O$ = 2 V step, $R_L$ = 2 kΩ | 500 | 650 | | V/µs |
| | G = 2, $V_O$ = 2 V step, $R_L$ = 2 kΩ | 300 | 500 | | V/µs |
| Settling Time to 0.1% | G = 2, $V_O$ = 2 V step | | 35 | | ns |
| NOISE/DISTORTION PERFORMANCE | | | | | |
| Total Harmonic Distortion | $f_C$ = 5 MHz, $V_O$ = 2 V p-p, $R_L$ = 1 kΩ | | −77 | | dBc |
| | $f_C$ = 20 MHz, $V_O$ = 2 V p-p, $R_L$ = 1 kΩ | | −50 | | dBc |
| Crosstalk, Output to Output | f = 5 MHz, G = 2, AD8062 | | −90 | | dBc |
| Input Voltage Noise | f = 100 kHz | | 8.5 | | nV/√Hz |
| Input Current Noise | f = 100 kHz | | 1.2 | | pA/√Hz |
| Differential Gain Error (NTSC) | G = 2, $R_L$ = 150 Ω | | 0.01 | | % |
| Differential Phase Error (NTSC) | G = 2, $R_L$ = 150 Ω | | 0.04 | | Degrees |
| Third-Order Intercept | f = 10 MHz | | 28 | | dBc |
| SFDR | f = 5 MHz | | 62 | | dB |
| DC PERFORMANCE | | | | | |
| Input Offset Voltage | | | 1 | 6 | mV |
| | $T_{MIN}$ to $T_{MAX}$ | | 2 | 6 | mV |
| Input Offset Voltage Drift | | | 3.5 | | µV/°C |
| Input Bias Current | | | 3.5 | 9 | µA |
| | $T_{MIN}$ to $T_{MAX}$ | | 4 | 9 | µA |
| Input Offset Current | | | ±0.3 | ±4.5 | µA |
| Open-Loop Gain | $V_O$ = 0.5 V to 4.5 V, $R_L$ = 150 Ω | 68 | 70 | | dB |
| | $V_O$ = 0.5 V to 4.5 V, $R_L$ = 2 kΩ | 74 | 90 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Resistance | | | 13 | | MΩ |
| Input Capacitance | | | 1 | | pF |
| Input Common-Mode Voltage Range | | | −0.2 to +3.2 | | V |
| Common-Mode Rejection Ratio | $V_{CM}$ = −0.2 V to +3.2 V | 62 | 80 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing Low | $R_L$ = 150 Ω | 0.3 | 0.1 | | V |
| | $R_L$ = 2 kΩ | 0.25 | 0.1 | | V |
| Output Voltage Swing High | $R_L$ = 150 Ω | 4.75 | 4.86 | | V |
| | $R_L$ = 2 kΩ | 4.85 | 4.9 | | V |
| Output Current | $V_O$ = 0.5 V to 4.5 V | 25 | 50 | | mA |
| Capacitive Load Drive, $V_{OUT}$ = 0.8 V | 30% overshoot: G = 1, $R_S$ = 0 Ω | | 25 | | pF |
| | G = 2, $R_S$ = 4.7 Ω | | 300 | | pF |
| POWER-DOWN DISABLE | | | | | |
| Turn-On Time | | | 40 | | ns |
| Turn-Off Time | | | 300 | | ns |
| $\overline{\text{DISABLE}}$ Voltage (Off) | | | 2.8 | | V |
| $\overline{\text{DISABLE}}$ Voltage (On) | | | 3.2 | | V |
| POWER SUPPLY | | | | | |
| Operating Range | | 2.7 | 5 | 8 | V |
| Quiescent Current per Amplifier | | | 6.8 | 9.5 | mA |
| Supply Current when Disabled (AD8063 Only) | | | 0.4 | | mA |
| Power Supply Rejection Ratio | $\Delta V_S$ = 2.7 V to 5 V | 72 | 80 | | dB |

$T_A$ = 25°C, $V_S$ = 3 V, $R_L$ = 1 kΩ, $V_O$ = 1 V, unless otherwise noted.

**Table 2.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | G = 1, $V_O$ = 0.2 V p-p | 150 | 300 | | MHz |
| | G = −1, +2, $V_O$ = 0.2 V p-p | 60 | 115 | | MHz |
| −3 dB Large Signal Bandwidth | G = 1, $V_O$ = 1 V p-p | | 250 | | MHz |
| Bandwidth for 0.1 dB Flatness | G = 1, $V_O$ = 0.2 V p-p | | 30 | | MHz |
| Slew Rate | G = 1, $V_O$ = 1 V step, $R_L$ = 2 kΩ | 190 | 280 | | V/µs |
| | G = 2, $V_O$ = 1.5 V step, $R_L$ = 2 kΩ | 180 | 230 | | V/µs |
| Settling Time to 0.1% | G = 2, $V_O$ = 1 V step | | 40 | | ns |
| NOISE/DISTORTION PERFORMANCE | | | | | |
| Total Harmonic Distortion | $f_C$ = 5 MHz, $V_O$ = 2 V p-p, $R_L$ = 1 kΩ | | −60 | | dBc |
| | $f_C$ = 20 MHz, $V_O$ = 2 V p-p, $R_L$ = 1 kΩ | | −44 | | dBc |
| Crosstalk, Output to Output | f = 5 MHz, G = 2 | | −90 | | dBc |
| Input Voltage Noise | f = 100 kHz | | 8.5 | | nV/√Hz |
| Input Current Noise | f = 100 kHz | | 1.2 | | pA/√Hz |
| DC PERFORMANCE | | | | | |
| Input Offset Voltage | | | 1 | 6 | mV |
| | $T_{MIN}$ to $T_{MAX}$ | | 2 | 6 | mV |
| Input Offset Voltage Drift | | | 3.5 | | µV/°C |
| Input Bias Current | | | 3.5 | 8.5 | µA |
| | $T_{MIN}$ to $T_{MAX}$ | | 4 | 8.5 | µA |
| Input Offset Current | | | ±0.3 | ±4.5 | µA |
| Open-Loop Gain | $V_O$ = 0.5 V to 2.5 V, $R_L$ = 150 Ω | 66 | 70 | | dB |
| | $V_O$ = 0.5 V to 2.5 V, $R_L$ = 2 kΩ | 74 | 90 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Resistance | | | 13 | | MΩ |
| Input Capacitance | | | 1 | | pF |
| Input Common-Mode Voltage Range | | | −0.2 to +1.2 | | V |
| Common-Mode Rejection Ratio | $V_{CM}$ = −0.2 V to +1.2 V | | 80 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing Low | $R_L$ = 150 Ω | 0.3 | 0.1 | | V |
| | $R_L$ = 2 kΩ | 0.3 | 0.1 | | V |
| Output Voltage Swing High | $R_L$ = 150 Ω | 2.85 | 2.87 | | V |
| | $R_L$ = 2 kΩ | 2.9 | 2.9 | | V |
| Output Current | $V_O$ = 0.5 V to 2.5 V | | 25 | | mA |
| Capacitive Load Drive, $V_{OUT}$ = 0.8 V | 30% overshoot, G = 1, $R_S$ = 0 Ω | | 25 | | pF |
| | G = 2, $R_S$ = 4.7 Ω | | 300 | | pF |
| POWER-DOWN DISABLE | | | | | |
| Turn-On Time | | | 40 | | ns |
| Turn-Off Time | | | 300 | | ns |
| $\overline{\text{DISABLE}}$ Voltage—Off | | | 0.8 | | V |
| $\overline{\text{DISABLE}}$ Voltage—On | | | 1.2 | | V |
| POWER SUPPLY | | | | | |
| Operating Range | | 2.7 | | 3 | V |
| Quiescent Current per Amplifier | | | 6.8 | 9 | mA |
| Supply Current when Disabled (AD8063 Only) | | | 0.4 | | mA |
| Power Supply Rejection Ratio | | 72 | 80 | | dB |

$T_A$ = 25°C, $V_S$ = 2.7 V, $R_L$ = 1 kΩ, $V_O$ = 1 V, unless otherwise noted.

**Table 3.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | G = 1, $V_O$ = 0.2 V p-p | 150 | 300 | | MHz |
| | G = −1, +2, $V_O$ = 0.2 V p-p | 60 | 115 | | MHz |
| | G = 1, $V_O$ = 1 V p-p | | 230 | | MHz |
| Bandwidth for 0.1 dB Flatness | G = 1, $V_O$ = 0.2 V p-p, $V_O$ dc = 1 V | | 30 | | MHz |
| Slew Rate | G = 1, $V_O$ = 0.7 V step, $R_L$ = 2 kΩ | 110 | 150 | | V/µs |
| | G = 2, $V_O$ = 1.5 V step, $R_L$ = 2 kΩ | 95 | 130 | | V/µs |
| Settling Time to 0.1% | G = 2, $V_O$ = 1 V step | | 40 | | ns |
| NOISE/DISTORTION PERFORMANCE | | | | | |
| Total Harmonic Distortion | $f_C$ = 5 MHz, $V_O$ = 2 V p-p, $R_L$ = 1 kΩ | | −60 | | dBc |
| | $f_C$ = 20 MHz, $V_O$ = 2 V p-p, $R_L$ = 1 kΩ | | −44 | | dBc |
| Crosstalk, Output to Output | f = 5 MHz, G = 2 | | −90 | | dBc |
| Input Voltage Noise | f = 100 kHz | | 8.5 | | nV/√Hz |
| Input Current Noise | f = 100 kHz | | 1.2 | | pA/√Hz |
| DC PERFORMANCE | | | | | |
| Input Offset Voltage | | | 1 | 6 | mV |
| | $T_{MIN}$ to $T_{MAX}$ | | 2 | 6 | mV |
| Input Offset Voltage Drift | | | 3.5 | | µV/°C |
| Input Bias Current | | | 3.5 | | µA |
| | $T_{MIN}$ to $T_{MAX}$ | | 4 | 8.5 | µA |
| Input Offset Current | | | ±0.3 | ±4.5 | µA |
| Open-Loop Gain | $V_O$ = 0.5 V to 2.2 V, $R_L$ = 150 Ω | 63 | 70 | | dB |
| | $V_O$ = 0.5 V to 2.2 V, $R_L$ = 2 kΩ | 74 | 90 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Resistance | | | 13 | | MΩ |
| Input Capacitance | | | 1 | | pF |
| Input Common-Mode Voltage Range | | | −0.2 to +0.9 | | V |
| Common-Mode Rejection Ratio | $V_{CM}$ = −0.2 V to +0.9 V | | 0.8 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing Low | $R_L$ = 150 Ω | 0.3 | 0.1 | | V |
| | $R_L$ = 2 kΩ | 0.25 | 0.1 | | V |
| Output Voltage Swing High | $R_L$ = 150 Ω | 2.55 | 2.55 | | V |
| | $R_L$ = 2 kΩ | 2.6 | 2.6 | | V |
| Output Current | $V_O$ = 0.5 V to 2.2 V | | 25 | | mA |
| Capacitive Load Drive, $V_{OUT}$ = 0.8 V | 30% overshoot: G = 1, $R_S$ = 0 Ω | | 25 | | pF |
| | G = 2, $R_S$ = 4.7 Ω | 300 | | | pF |
| POWER-DOWN DISABLE | | | | | |
| Turn-On Time | | | 40 | | ns |
| Turn-Off Time | | | 300 | | ns |
| $\overline{\text{DISABLE}}$ Voltage (Off) | | | 0.5 | | V |
| $\overline{\text{DISABLE}}$ Voltage (On) | | | 0.9 | | V |
| POWER SUPPLY | | | | | |
| Operating Range | | 2.7 | | 8 | V |
| Quiescent Current per Amplifier | | | 6.8 | 8.5 | mA |
| Supply Current when Disabled (AD8063 Only) | | | 0.4 | | mA |
| Power Supply Rejection Ratio | | | 80 | | dB |

# ABSOLUTE MAXIMUM RATINGS

**Table 4.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 8 V |
| Internal Power Dissipation[1] | |
| 8-lead SOIC (R) | 0.8 W |
| 5-lead SOT-23 (RJ) | 0.5 W |
| 6-lead SOT-23 (RJ) | 0.5 W |
| 8-lead MSOP (RM) | 0.6 W |
| Input Voltage (Common-Mode) | ($-V_S$ – 0.2 V) to ($+V_S$ + 0.2 V) |
| Differential Input Voltage | $\pm V_S$ |
| Output Short-Circuit Duration | Observe power derating curves |
| Storage Temperature Range R-8, RM-8, SOT-23-5, SOT-23-6 | −65°C to +125°C |
| Operating Temperature Range | −40°C to +85°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |

[1] Specification is for device in free air.
8-Lead SOIC_N: $\theta_{JA}$ = 160°C/W; $\theta_{JC}$ = 56°C/W.
5-Lead SOT-23: $\theta_{JA}$ = 240°C/W; $\theta_{JC}$ = 92°C/W.
6-Lead SOT-23: $\theta_{JA}$ = 230°C/W; $\theta_{JC}$ = 92°C/W.
8-Lead MSOP: $\theta_{JA}$ = 200°C/W; $\theta_{JC}$ = 44°C/W.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8061/AD8062/AD8063 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. While the AD8061/AD8062/AD8063 is internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions.

To ensure proper operation, it is necessary to observe the maximum power derating curves.

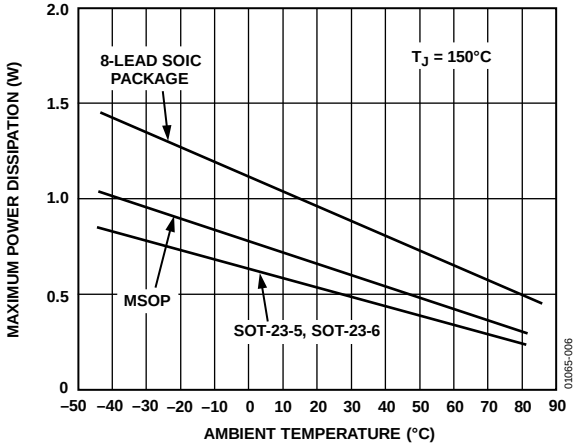



*Figure 6. Maximum Power Dissipation vs. Temperature for AD8061/AD8062/AD8063*

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

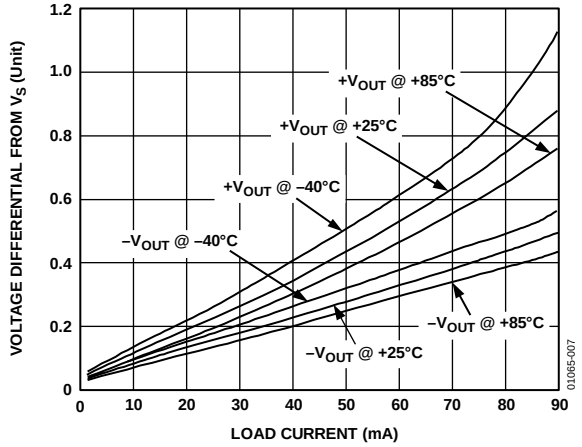



Figure 7. Output Saturation Voltage vs. Load Current

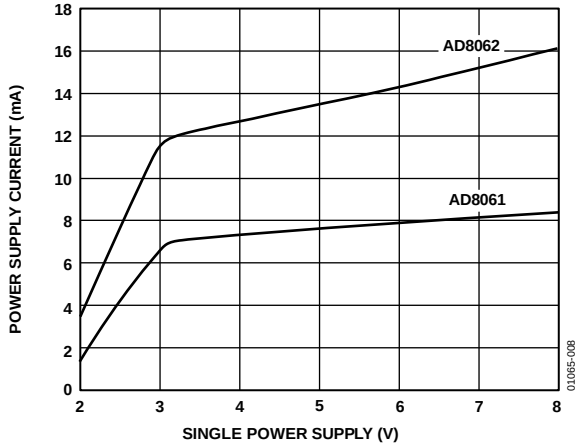



Figure 8. $I_{SUPPLY}$ vs. $V_{SUPPLY}$

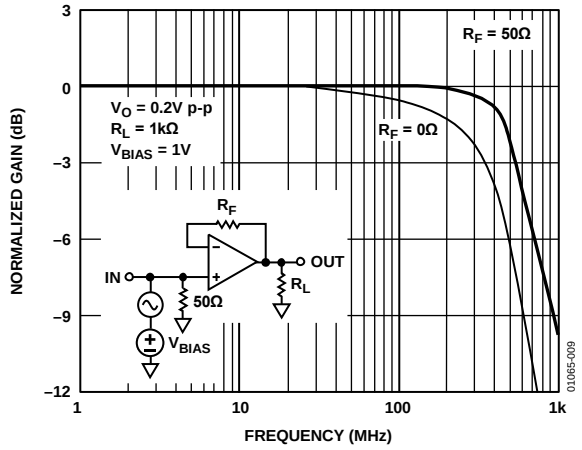



Figure 9. Small Signal Response, $R_F$ = 0 Ω, 50 Ω

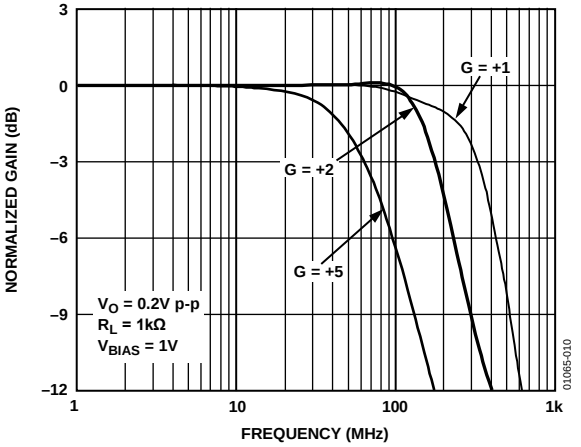



Figure 10. Small Signal Frequency Response

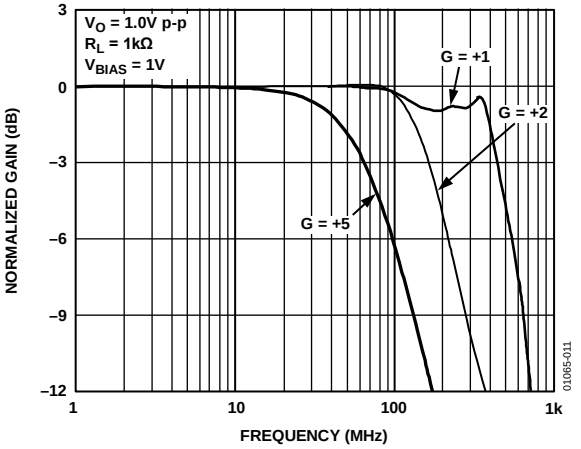



Figure 11. Large Signal Frequency Response

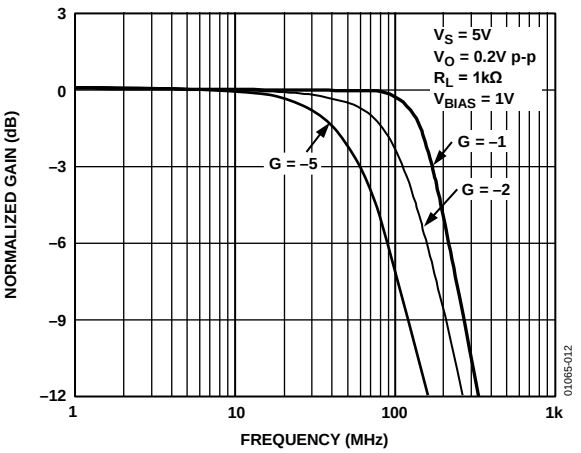



Figure 12. Small Signal Frequency Response

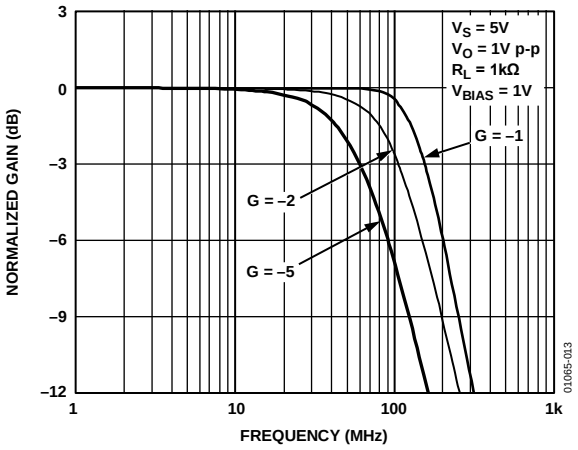



Figure 13. Large Signal Frequency Response

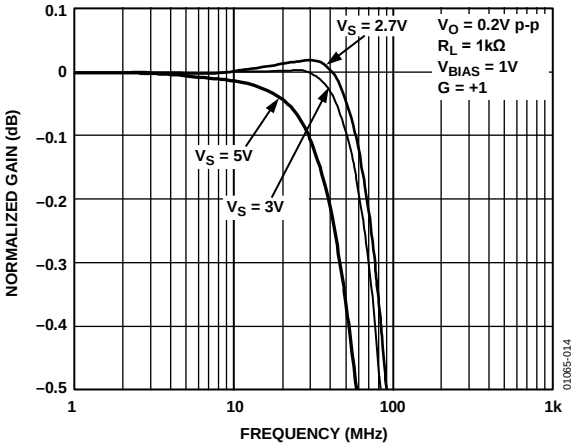



Figure 14. 0.1 dB Flatness

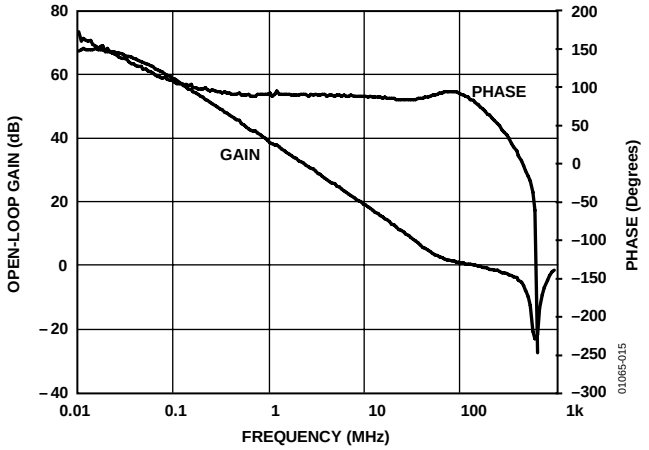



Figure 15. AD8062 Open-Loop Gain and Phase vs. Frequency, $V_S$ = 5 V, $R_L$ = 1 kΩ

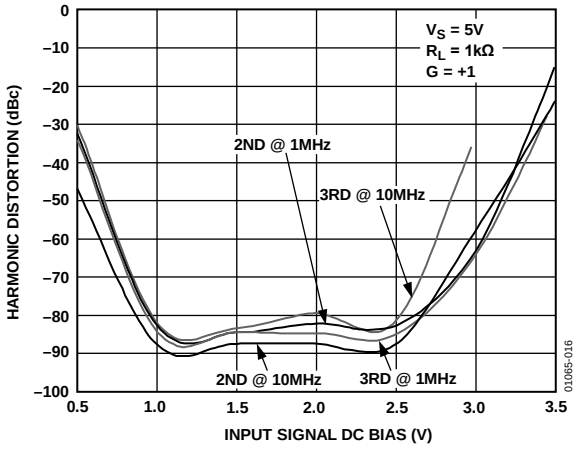



Figure 16. Harmonic Distortion for a 1 V p-p Signal vs. Input Signal DC Bias

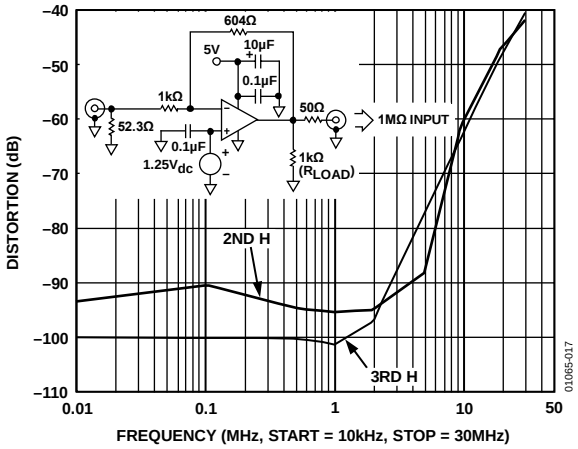



Figure 17. Harmonic Distortion for a 1 V p-p Output Signal vs. Input Signal DC Bias

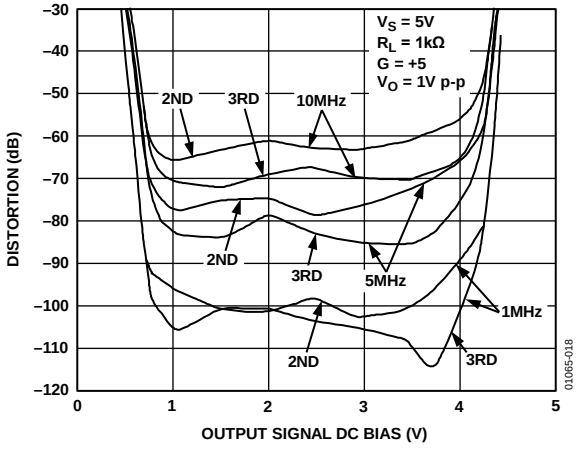



Figure 18. Harmonic Distortion vs. Output Signal DC Bias

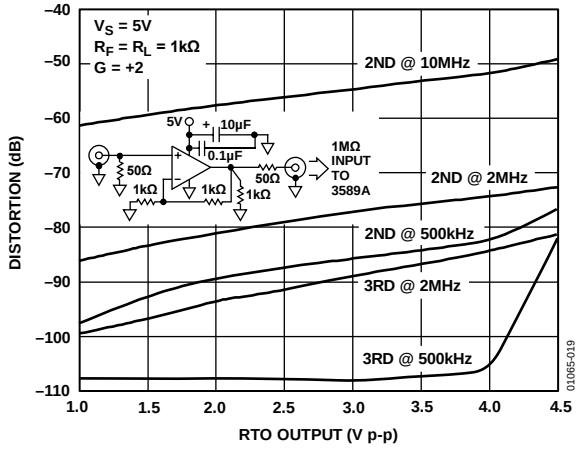



Figure 19. Harmonic Distortion vs. Output Signal Amplitude

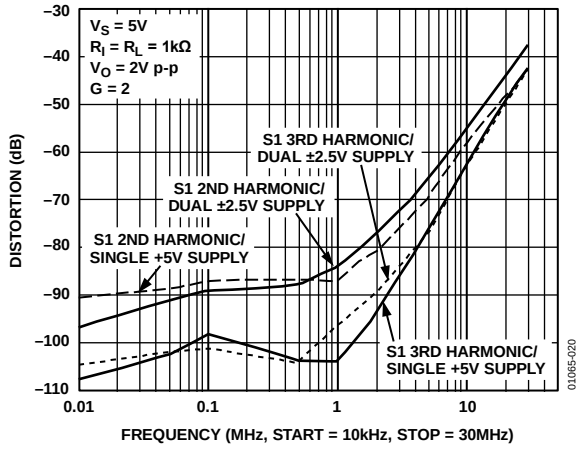



Figure 20. Harmonic Distortion vs. Frequency

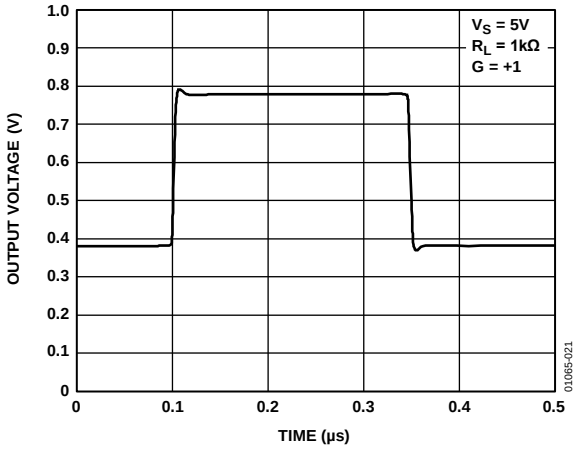



Figure 21. 400 mV Pulse Response

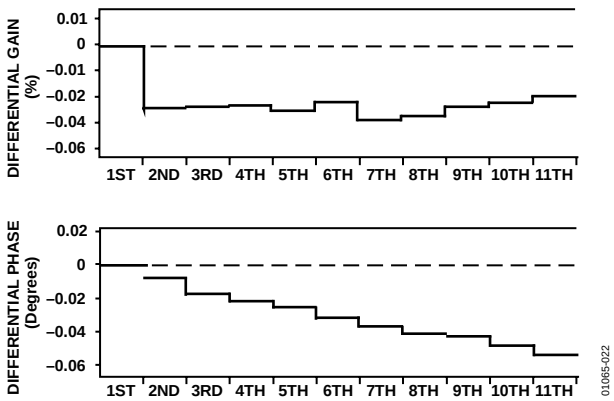



Figure 22. Differential Gain and Phase Error, G = 2, NTSC Input Signal, $R_L$ = 1 kΩ, $V_S$ = 5 V

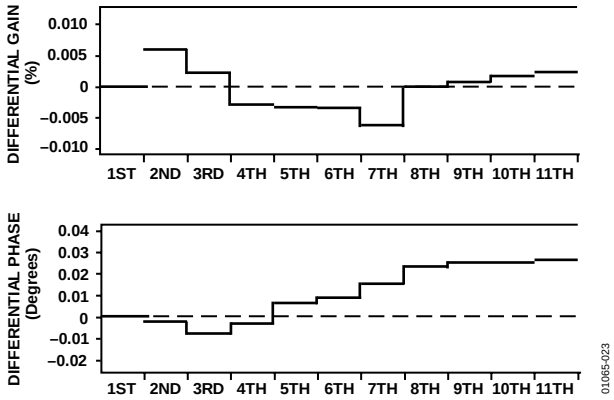



Figure 23. Differential Gain and Phase Error, G = 2, NTSC Input Signal, $R_L$ = 150 Ω, $V_S$ = 5 V

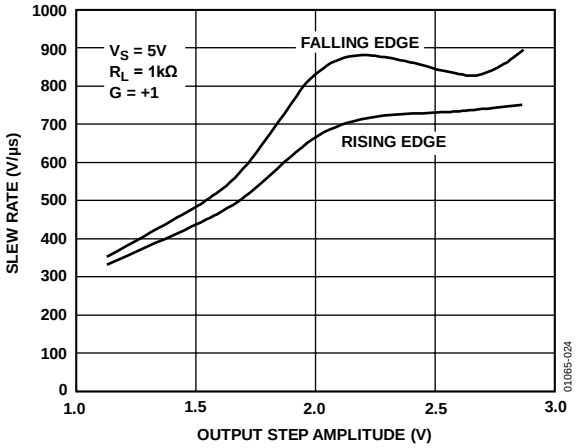



Figure 24. Slew Rate vs. Output Step Amplitude

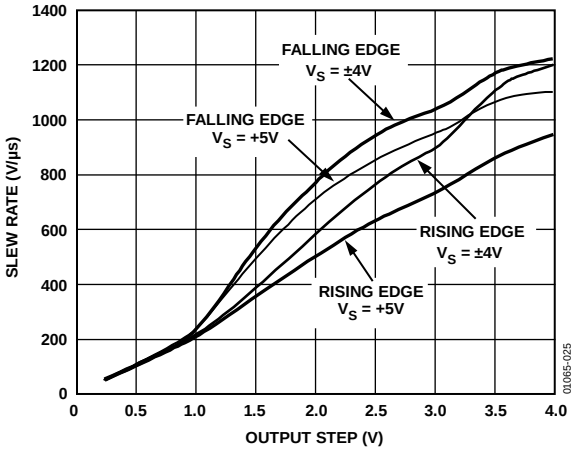



Figure 25. Slew Rate vs. Output Step Amplitude, G = 2, $R_L$ = 1 kΩ, $V_S$ = 5 V

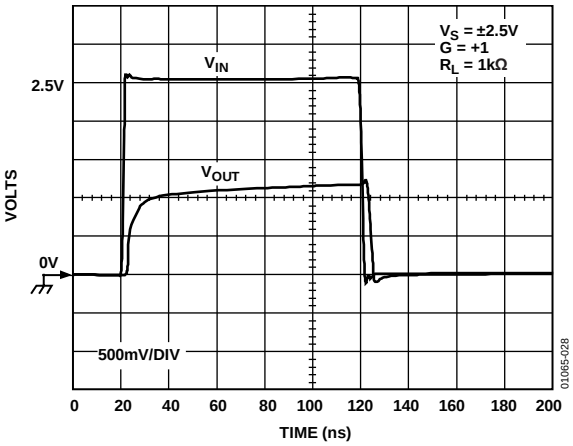



Figure 28. Input Overload Recovery, Input Step = 0 V to 2 V

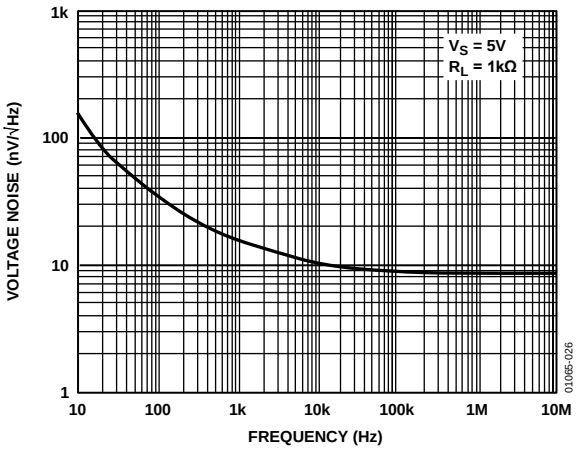



Figure 26. Voltage Noise vs. Frequency

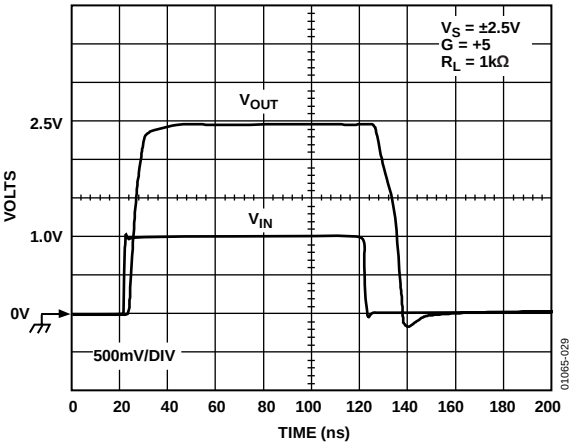



Figure 29. Output Overload Recovery, Input Step = 0 V to 1 V

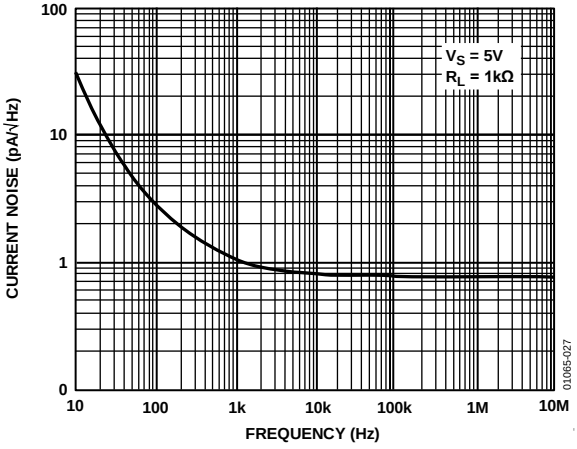



Figure 27. Current Noise vs. Frequency

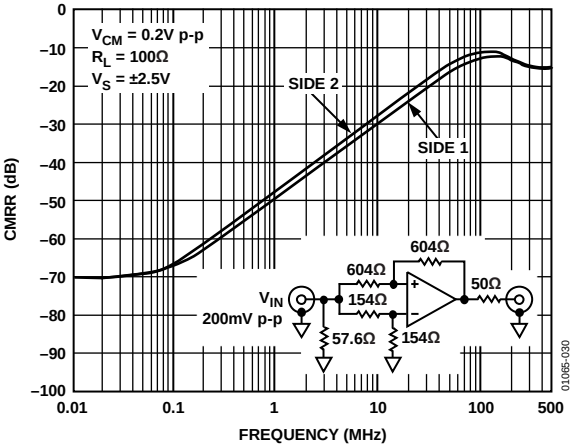



Figure 30. CMRR vs. Frequency

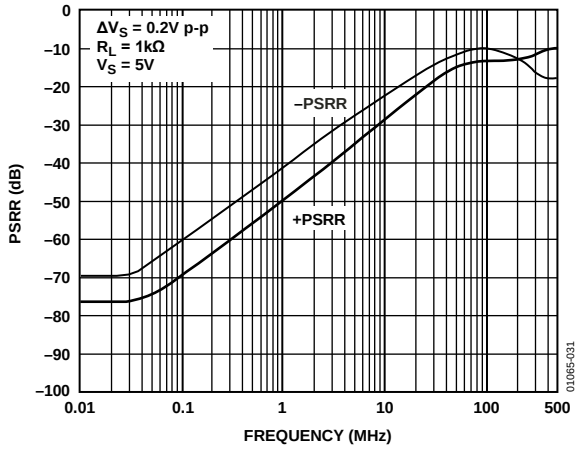



Figure 31. ±PSRR vs. Frequency Delta

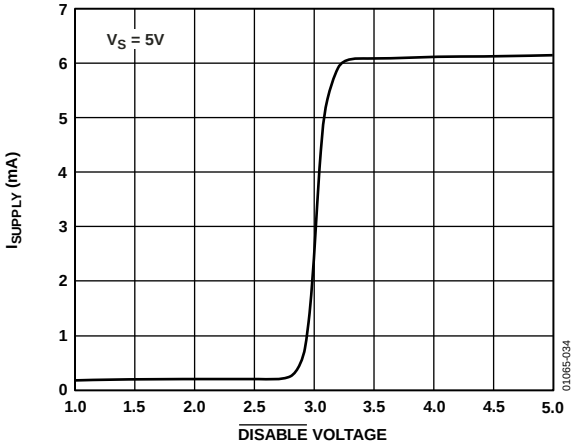



Figure 34. AD8063 $\overline{DISABLE}$ Voltage vs. Supply Current

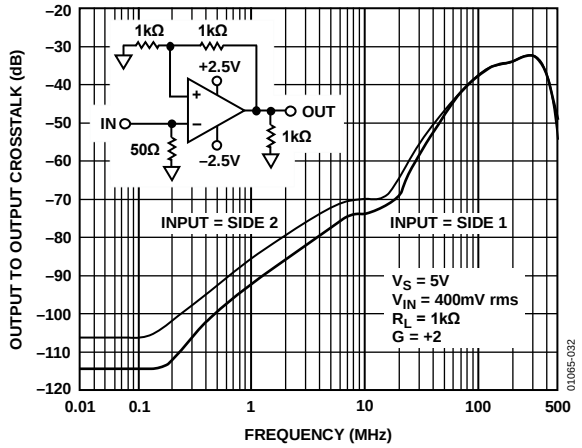



Figure 32. AD8062 Crosstalk, $V_{OUT}$ = 2.0 V p-p, $R_L$ = 1 kΩ, G = 2, $V_S$ = 5 V

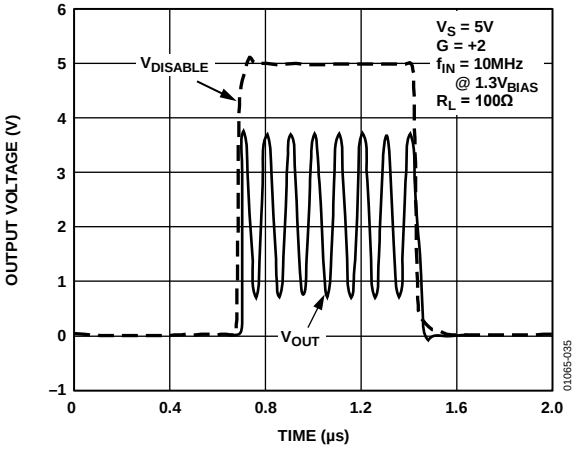



Figure 35. AD8063 $\overline{DISABLE}$ Function, Voltage = 0 V to 5 V

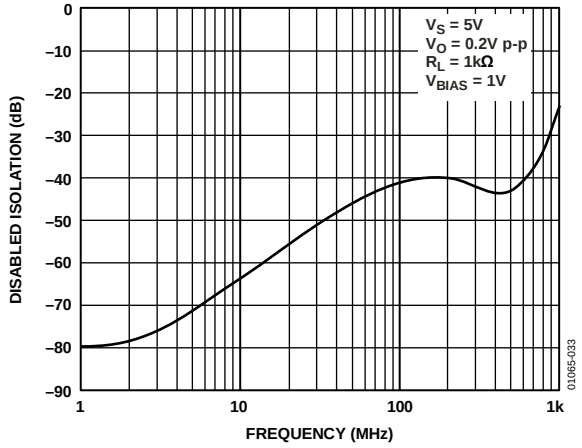



Figure 33. AD8063 Disabled Output Isolation Frequency Response

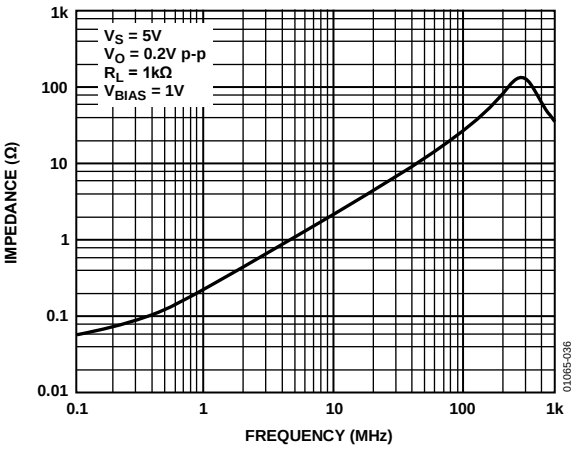



Figure 36. Output Impedance vs. Frequency, $V_{OUT}$ = 0.2 V p-p, $R_L$ = 1 kΩ, $V_S$ = 5 V

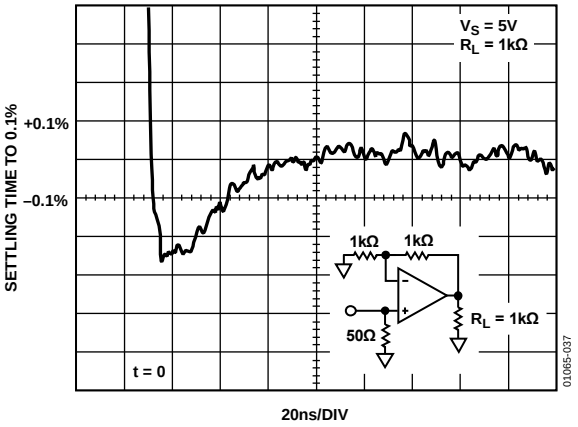



Figure 37. Output Settling Time to 0.1%

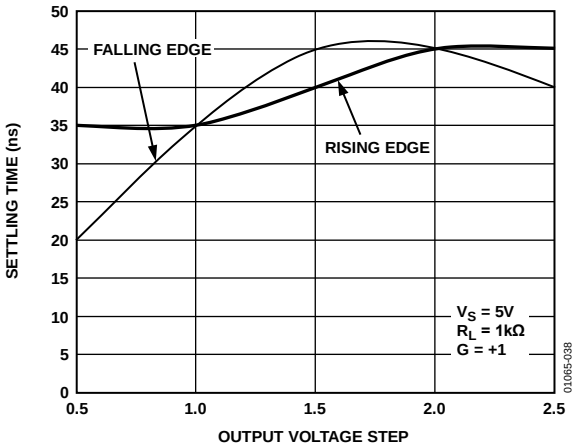



Figure 38. Settling Time vs. $V_{OUT}$

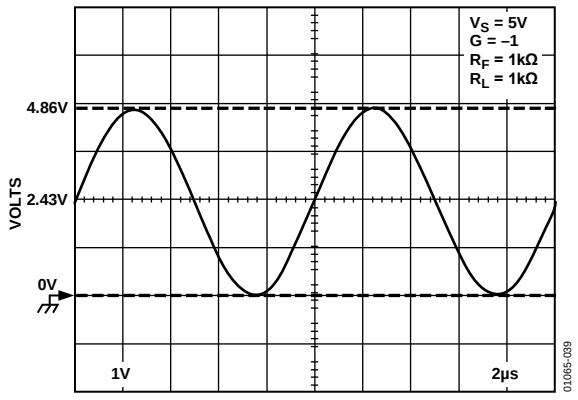



Figure 39. Output Swing

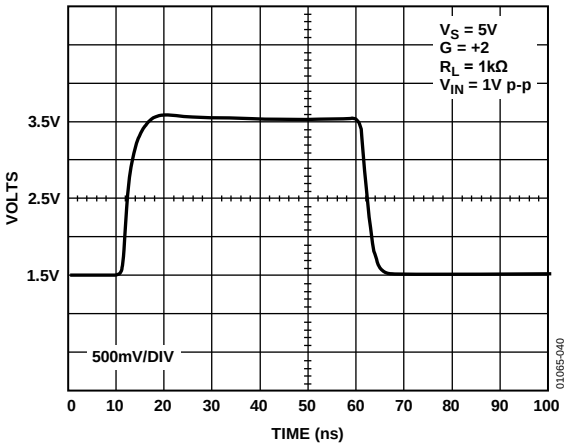



Figure 40. 1 V Step Response

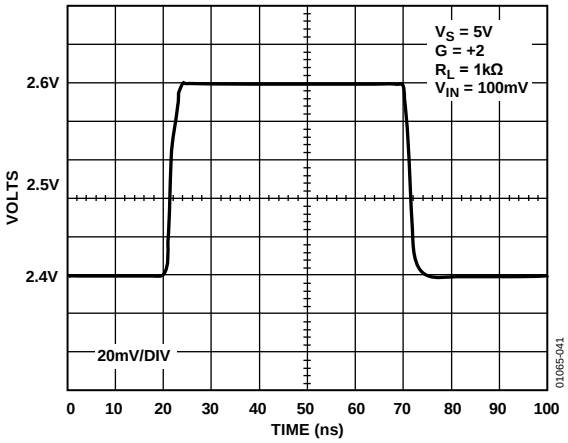



Figure 41. 100 mV Step Response

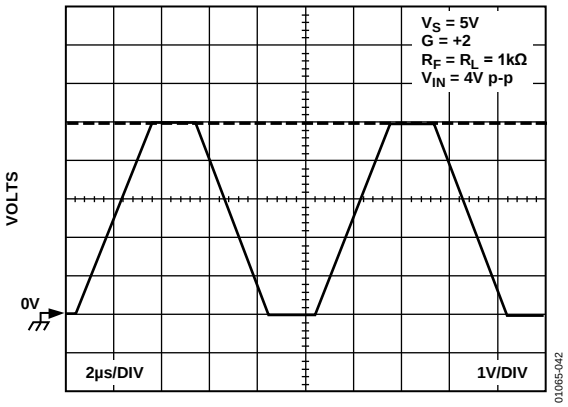



Figure 42. Output Rail-to-Rail Swing

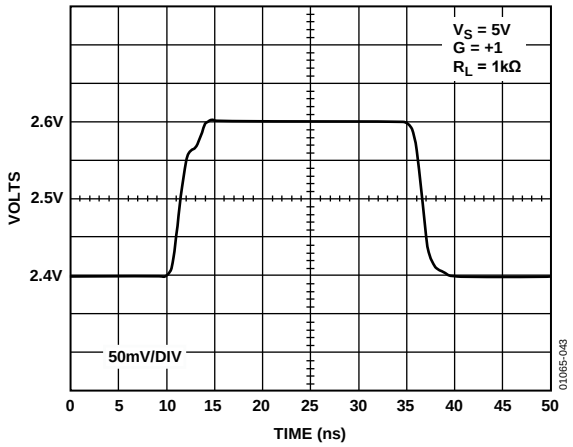



*Figure 43. 200 mV Step Response*

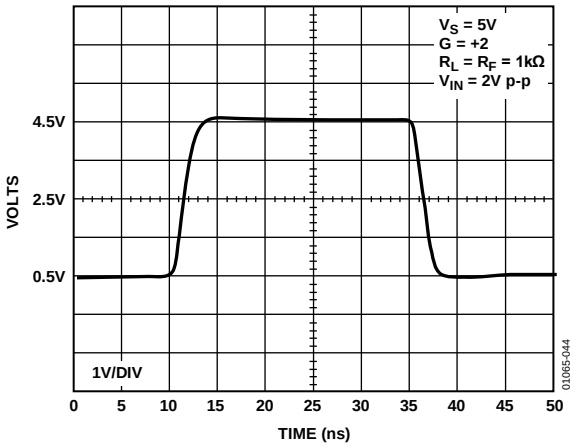



*Figure 44. 2 V Step Response*

# CIRCUIT DESCRIPTION

The AD8061/AD8062/AD8063 family is comprised of high speed voltage feedback op amps. The high slew rate input stage is a true, single-supply topology, capable of sensing signals at or below the minus supply rail. The rail-to-rail output stage can pull within 30 mV of either supply rail when driving light loads and within 0.3 V when driving 150 Ω. High speed performance is maintained at supply voltages as low as 2.7 V.

## HEADROOM CONSIDERATIONS

These amplifiers are designed for use in low voltage systems. To obtain optimum performance, it is useful to understand the behavior of the amplifier as input and output signals approach the amplifier's headroom limits.

The AD8061/AD8062/AD8063 input common-mode voltage range extends from the negative supply voltage (actually 200 mV below this), or ground for single-supply operation, to within 1.8 V of the positive supply voltage. Thus, at a gain of 2, the AD8061/AD8062/AD8063 can provide full rail-to-rail output swing for supply voltage as low as 3.6 V, assuming the input signal swings from $-V_S$ (or ground) to $+V_S/2$. At a gain of 3, the AD8061/AD8062/AD8063 can provide a rail-to-rail output range down to 2.7 V total supply voltage.

Exceeding the headroom limit is not a concern for any inverting gain on any supply voltage, as long as the reference voltage at the amplifier's positive input lies within the amplifier's input common-mode range.

The input stage is the headroom limit for signals when the amplifier is used in a gain of 1 for signals approaching the positive rail. Figure 45 shows a typical offset voltage vs. input common-mode voltage for the AD8061/AD8062/AD8063 amplifier on a 5 V supply. Accurate dc performance is maintained from approximately 200 mV below the minus supply to within 1.8 V of the positive supply. For high speed signals, however, there are other considerations. Figure 46 shows −3 dB bandwidth vs. dc input voltage for a unity-gain follower. As the common-mode voltage approaches the positive supply, the amplifier holds together well, but the bandwidth begins to drop at 1.9 V within $+V_S$.

This manifests itself in increased distortion or settling time. Figure 16 plots the distortion of a 1 V p-p signal with the AD8061/AD8062/AD8063 amplifier used as a follower on a 5 V supply vs. signal common-mode voltage. Distortion performance is maintained until the input signal center voltage gets beyond 2.5 V, as the peak of the input sine wave begins to run into the upper common-mode voltage limit.

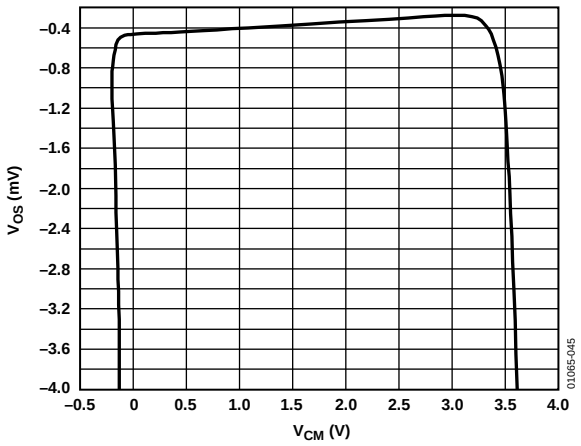



*Figure 45. $V_{OS}$ vs. Common-Mode Voltage, $V_S$ = 5 V*

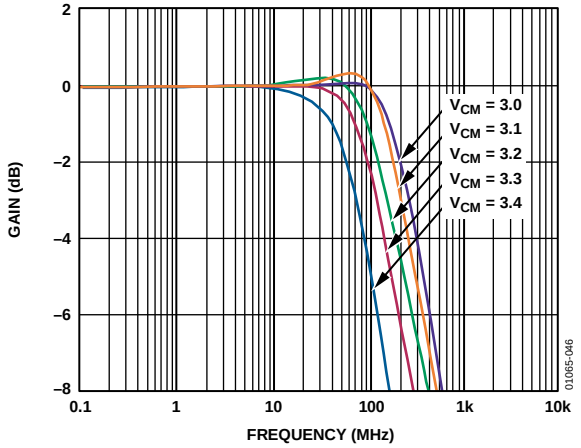



*Figure 46. Unity-Gain Follower Bandwidth vs. Input Common Mode, $V_S$ = 5 V*

Higher frequency signals require more headroom than lower frequencies to maintain distortion performance. Figure 47 illustrates how the rising edge settling time for the amplifier configured as a unity-gain follower stretches out as the top of a 1 V step input approaches and exceeds the specified input common-mode voltage limit.

For signals approaching the minus supply and inverting gain and high positive gain configurations, the headroom limit is the output stage. The AD8061/AD8062/AD8063 amplifiers use a common emitter style output stage. This output stage maximizes the available output range, limited by the saturation voltage of the output transistors. The saturation voltage increases with the drive current the output transistor is required to supply, due to the output transistors' collector resistance. The saturation voltage is estimated using the equation

$$V_{SAT} = 25 \text{ mV} + I_O \times 8\ \Omega$$

where:
$I_O$ is the output current.
8 Ω is a typical value for the output transistors' collector resistance.

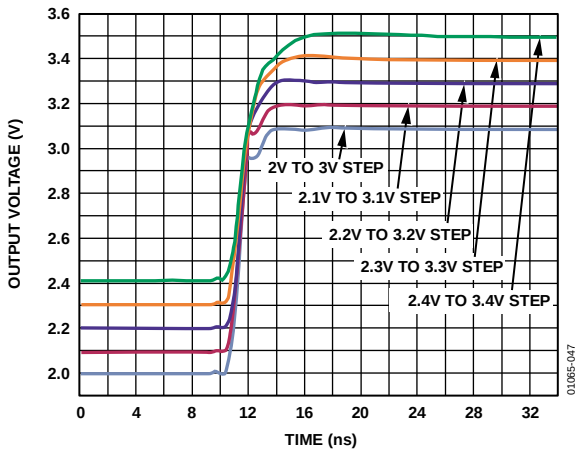



*Figure 47. Output Rising Edge for 1 V Step at Input Headroom Limits, G = 1, $V_S$ = 5 V, 0 V*

As the saturation point of the output stage is approached, the output signal shows increasing amounts of compression and clipping. As in the input headroom case, the higher frequency signals require a bit more headroom than lower frequency signals. Figure 16, Figure 17, and Figure 18 illustrate this point, plotting typical distortion vs. output amplitude and bias for gains of 2 and 5.

## OVERLOAD BEHAVIOR AND RECOVERY

### *Input*

The specified input common-mode voltage of the AD8061/AD8062/AD8063 is −200 mV below the negative supply to within 1.8 V of the positive supply. Exceeding the top limit results in lower bandwidth and increased settling time as seen in Figure 46 and Figure 47. Pushing the input voltage of a unity-gain follower beyond 1.6 V within the positive supply leads to the behavior shown in Figure 48—an increasing amount of output error and much increased settling time. Recovery time from input voltages 1.6 V or closer to the positive supply is approximately 35 ns, which is limited by the settling artifacts caused by transistors in the input stage coming out of saturation.

The AD8061/AD8062/AD8063 family does not exhibit phase reversal, even for input voltages beyond the voltage supply rails. Going more than 0.6 V beyond the power supplies turns on protection diodes at the input stage, which greatly increases the current draw of the device.

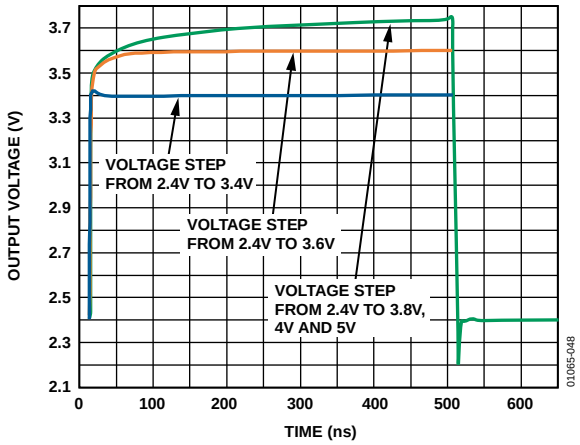



*Figure 48. Pulse Response for G = 1 Follower, Input Step Overloading the Input Stage*

### *Output*

Output overload recovery is typically within 40 ns after the amplifier's input is brought to a nonoverloading value. Figure 49 shows output recovery transients for the amplifier recovering from a saturated output from the top and bottom supplies to a point at midsupply.

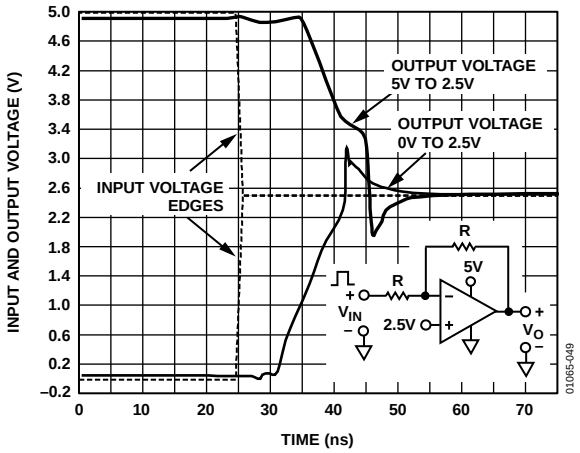



*Figure 49. Overload Recovery, G = −1, $V_S$ = 5 V*

## CAPACITIVE LOAD DRIVE

The AD8061/AD8062/AD8063 family is optimized for bandwidth and speed, not for driving capacitive loads. Output capacitance creates a pole in the amplifier's feedback path, leading to excessive peaking and potential oscillation. If dealing with load capacitance is a requirement of the application, the two strategies to consider are as follows:

Use a small resistor in series with the amplifier's output and the load capacitance.
Reduce the bandwidth of the amplifier's feedback loop by increasing the overall noise gain.

Figure 50 shows a unity-gain follower using the series resistor strategy. The resistor isolates the output from the capacitance and, more importantly, creates a zero in the feedback path that compensates for the pole created by the output capacitance.

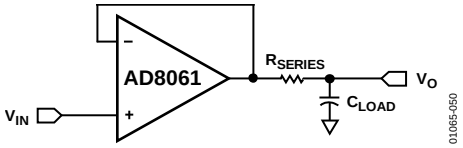



*Figure 50. Series Resistor Isolating Capacitive Load*

Voltage feedback amplifiers like those in the AD8061/AD8062/AD8063 family are able to drive more capacitive load without excessive peaking when used in higher gain configurations because the increased noise gain reduces the bandwidth of the overall feedback loop. Figure 51 plots the capacitance that produces 30% overshoot vs. noise gain for a typical amplifier.

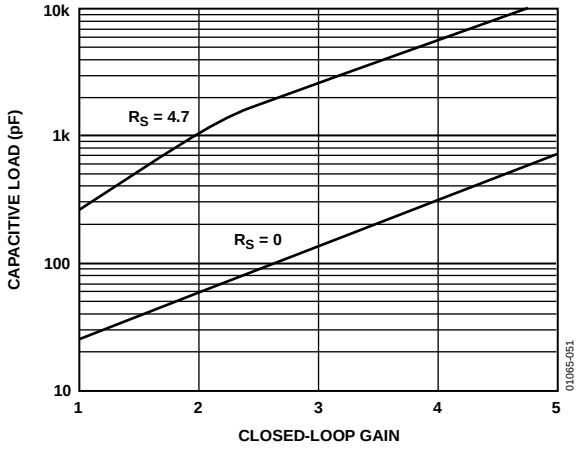



*Figure 51. Capacitive Load vs. Closed-Loop Gain*

## DISABLE OPERATION

The internal circuit for the AD8063 disable function is shown in Figure 52. When the $\overline{\text{DISABLE}}$ node is pulled below 2 V from the positive supply, the supply current decreases from typically 6.5 mA to under 400 µA, and the AD8063 output enters a high impedance state. If the $\overline{\text{DISABLE}}$ node is not connected and allowed to float, the AD8063 stays biased at full power.

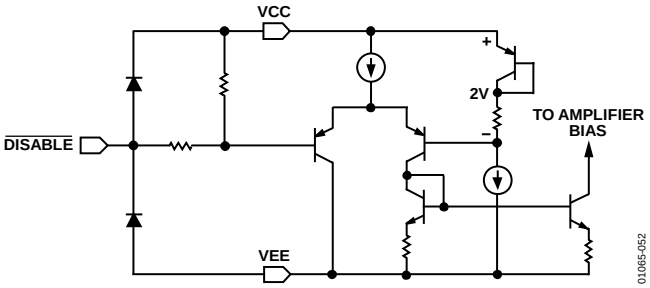



*Figure 52. Disable Circuit of the AD8063*

Figure 34 shows the AD8063 supply current vs. $\overline{\text{DISABLE}}$ voltage. Figure 35 plots the output seen when the AD8063 input is driven with a 10 MHz sine wave, and $\overline{\text{DISABLE}}$ is toggled from 0 V to 5 V, illustrating the part's turn-on and turn-off time. Figure 33 shows the input/output isolation response with the AD8063 shut off.

## BOARD LAYOUT CONSIDERATIONS

Maintaining the high speed performance of the AD8061/AD8062/AD8063 family requires the use of high speed board layout techniques and low parasitic components.

The PCB should have a ground plane covering unused portions of the component side of the board to provide a low impedance path. Remove the ground plane near the package to reduce parasitic capacitance.

Proper bypassing is critical. Use a ceramic 0.1 µF chip capacitor to bypass both supplies. Locate the chip capacitor within 3 mm of each power pin. Additionally, connect in parallel a 4.7 µF to 10 µF tantalum electrolytic capacitor to provide charge for fast, large signal changes at the output.

Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. Locate the feedback resistor close to the inverting input pin. The value of the feedback resistor may come into play—for instance, 1 kΩ interacting with 1 pF of parasitic capacitance creates a pole at 159 MHz. Use stripline design techniques for signal traces longer than 25 mm. Design them with either 50 Ω or 75 Ω characteristic impedance and proper termination at each end.

# APPLICATIONS INFORMATION

## SINGLE-SUPPLY SYNC STRIPPER

When a video signal contains synchronization pulses, it is sometimes desirable to remove them prior to performing certain operations. In the case of analog-to-digital conversion, the sync pulses consume some of the dynamic range, so removing them increases the converter's available dynamic range for the video information.

Figure 53 shows a basic circuit for creating a sync stripper using the AD8061 powered by a single supply. When the negative supply is at ground potential, the lowest potential to which the output can go is ground. This feature is exploited to create a waveform whose lowest amplitude is the black level of the video and does not include the sync level.

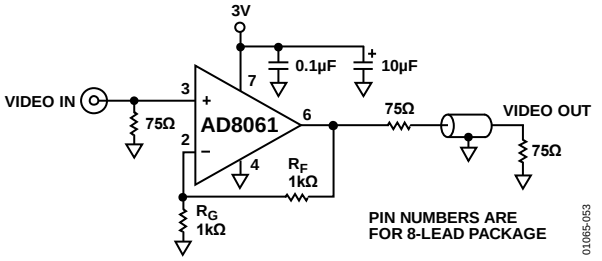



*Figure 53. Single 3 V Sync Stripper Using AD8061*

In this case, the input video signal has its black level at ground, so it comes out at ground at the input. Because the sync level is below the black level, it does not show up at the output. However, all of the active video portion of the waveform is amplified by a gain of 2 and then normalized to unity gain by the back-terminated transmission line. Figure 54 is an oscilloscope plot of the input and output waveforms.

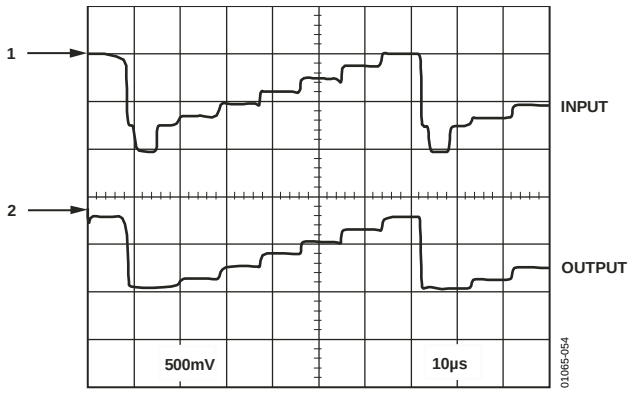



*Figure 54. Input and Output Waveforms for a Single-Supply Video Sync Stripper Using an AD8061*

Some video signals with sync are derived from single-supply devices, such as video DACs. These signals can contain sync, but the whole waveform is positive, and the black level is not at ground but at a positive voltage.

The circuit can be modified to provide the sync stripping function for such a waveform. Instead of connecting $R_G$ to ground, connect it to a dc voltage that is two times the black level of the input signal. The gain from the noninverting input to the output is 2, which means the black level is amplified by 2 to the output. However, the gain through $R_G$ is −1 to the output. It takes a dc level of twice the input black level to shift the black level to ground at the output. When this occurs, the sync is stripped, and the active video is passed as in the ground-referenced case.

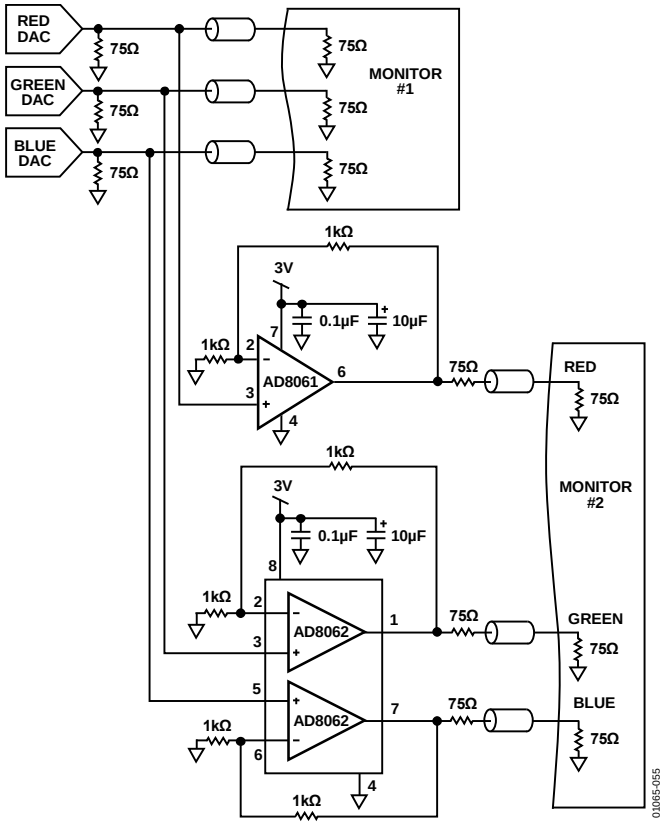



*Figure 55. RGB Cable Driver Using AD8061 and AD8062*

## RGB AMPLIFIER

Most RGB graphics signals are created by video DAC outputs that drive a current through a resistor to ground. At the video black level, the current goes to zero, and the voltage of the video is also zero. Before the availability of high speed rail-to-rail op amps, it was essential that an amplifier have a negative supply to amplify such a signal. Such an amplifier is necessary if one wants to drive a second monitor from the same DAC outputs.

However, high speed, rail-to-rail output amplifiers like the AD8061 and AD8062 accept ground-level input signals and output ground-level signals. They are used as RGB signal amplifiers. A combination of the AD8061 (single) and the AD8062 (dual) amplifies the three video channels of an RGB system. Figure 55 shows a circuit that performs this function.

## MULTIPLEXER

The AD8063 has a disable pin used to power down the amplifier to save power or to create a mux circuit. If two (or more) AD8063 outputs are connected together, and only one is enabled, then only the signal of the enabled amplifier will appear at the output. This configuration is used to select from various input signal sources. Additionally, the same input signal is applied to different gain stages, or differently tuned filters, to make a gain-step amplifier or a selectable frequency amplifier.

Figure 56 shows a schematic of two AD8063 devices used to create a mux that selects between two inputs. One of these is a 1 V p-p, 3 MHz sine wave; the other is a 2 V p-p, 1 MHz sine wave.

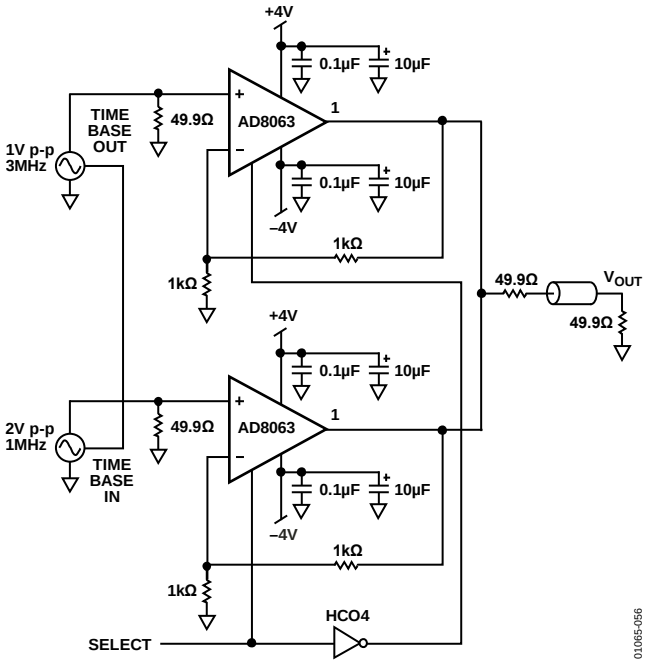



*Figure 56. Two-to-One Multiplexer Using Two AD8063s*

The select signal and the output waveforms for this circuit are shown in Figure 57. For synchronization clarity, two different frequency synthesizers, whose time bases are locked to each other, generate the signals.

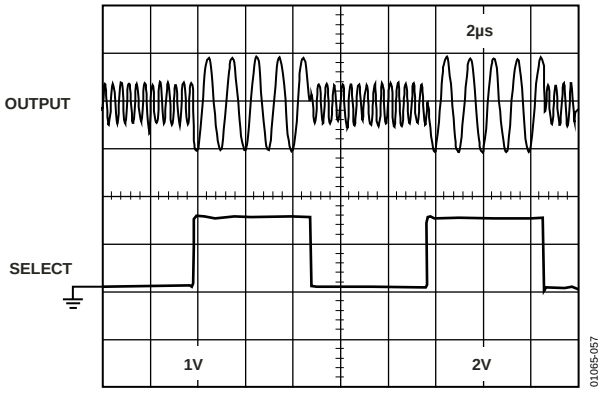
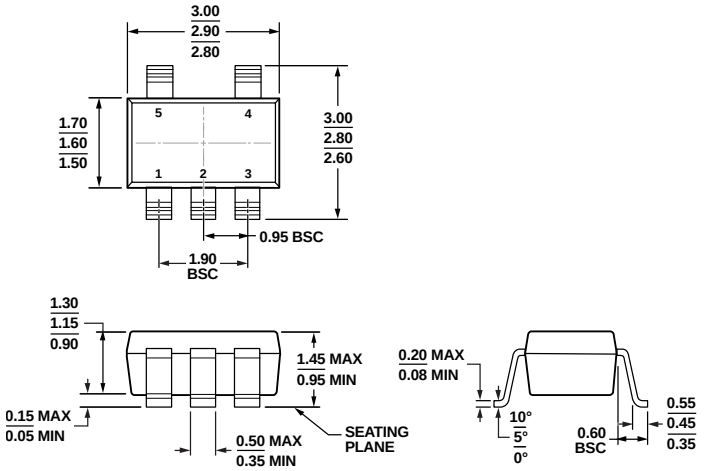


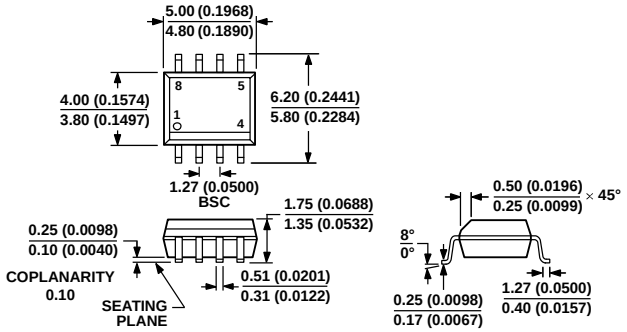

*Figure 57. AD8063 Mux Output*

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-178-AA

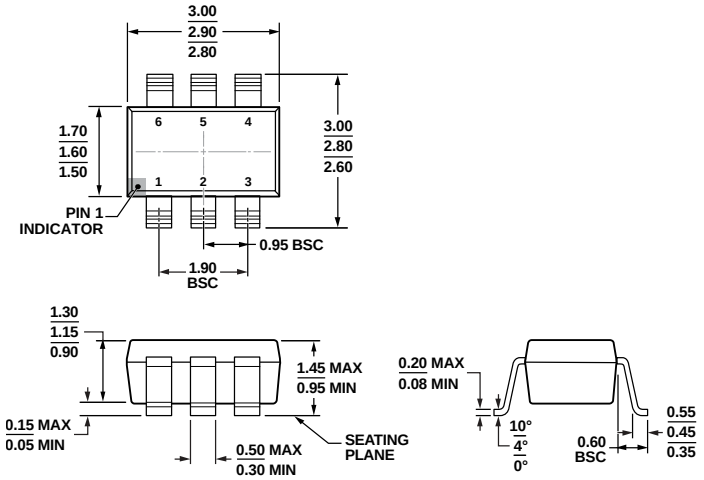
*Figure 58. 5-Lead Small Outline Transistor Package [SOT-23]*
*(RJ-5)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

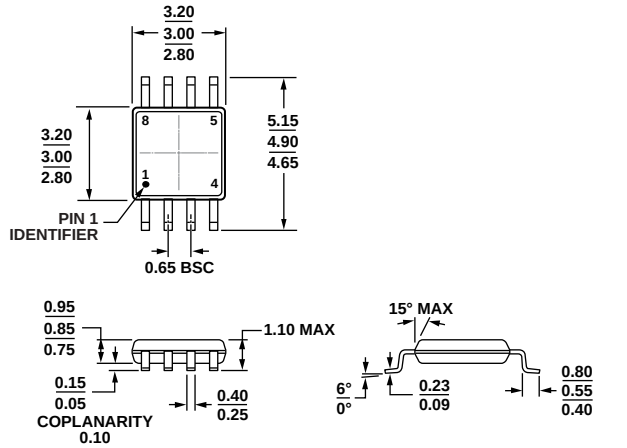
11-01-2010-A
012407-A

*Figure 59. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body (R-8)*
*Dimensions shown in millimeters and (inches)*




COMPLIANT TO JEDEC STANDARDS MO-178-AB

*Figure 60. 6-Lead Small Outline Transistor Package [SOT-23]*
*(RJ-6)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MO-187-AA

12-16-2008-A
10-07-2009-B

*Figure 61. 8-Lead Mini Small Outline Package [MSOP]*
*(RM-8)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|
| AD8061AR | −40°C to +85°C | 8-Lead SOIC_N | R-8 | |
| AD8061ARZ | −40°C to +85°C | 8-Lead SOIC_N | R-8 | |
| AD8061ARZ-REEL | −40°C to +85°C | 8-Lead SOIC_N, 13-Inch Tape and Reel | R-8 | |
| AD8061ARZ-REEL7 | −40°C to +85°C | 8-Lead SOIC_N, 7-Inch Tape and Reel | R-8 | |
| AD8061ART-R2 | −40°C to +85°C | 5-Lead SOT-23, 250 Piece Tape and Reel | RJ-5 | HGA |
| AD8061ART-REEL7 | −40°C to +85°C | 5-Lead SOT-23, 7-Inch Tape and Reel | RJ-5 | HGA |
| AD8061ARTZ-R2 | −40°C to +85°C | 5-Lead SOT-23, 250 Piece Tape and Reel | RJ-5 | H0D[2] |
| AD8061ARTZ-REEL | −40°C to +85°C | 5-Lead SOT-23, 13-Inch Tape and Reel | RJ-5 | H0D[2] |
| AD8061ARTZ-REEL7 | −40°C to +85°C | 5-Lead SOT-23, 7-Inch Tape and Reel | RJ-5 | H0D[2] |
| AD8061AR-EBZ | | Evaluation Board for 8-Lead SOIC_N | | |
| AD8061ART-EBZ | | Evaluation Board for 5-Lead SOT-23 | | |
| AD8062AR | −40°C to +85°C | 8-Lead SOIC_N | R-8 | |
| AD8062ARZ | −40°C to +85°C | 8-Lead SOIC_N | R-8 | |
| AD8062ARZ-RL | −40°C to +85°C | 8-Lead SOIC_N, 13-Inch Tape and Reel | R-8 | |
| AD8062ARZ-R7 | −40°C to +85°C | 8-Lead SOIC_N, 7-Inch Tape and Reel | R-8 | |
| AD8062ARM | −40°C to +85°C | 8-Lead MSOP | RM-8 | HCA |
| AD8062ARMZ | −40°C to +85°C | 8-Lead MSOP | RM-8 | #HCA |
| AD8062ARMZ-RL | −40°C to +85°C | 8-Lead MSOP, 13-Inch Tape and Reel | RM-8 | #HCA |
| AD8062ARMZ-R7 | −40°C to +85°C | 8-Lead MSOP, 7-Inch Tape and Reel | RM-8 | #HCA |
| AD8062AR-EBZ | | Evaluation Board for 8-Lead SOIC_N | | |
| AD8062ARM-EBZ | | Evaluation Board for 8-Lead MSOP | | |
| AD8063ARZ | −40°C to +85°C | 8-Lead SOIC_N | R-8 | |
| AD8063ARZ-REEL | −40°C to +85°C | 8-Lead SOIC_N, 13-Inch Tape and Reel | R-8 | |
| AD8063ARZ-REEL7 | −40°C to +85°C | 8-Lead SOIC_N, 7-Inch Tape and Reel | R-8 | |
| AD8063ART-R2 | −40°C to +85°C | 6-Lead SOT-23, 250 Piece Tape and Reel | RJ-6 | HHA |
| AD8063ART-REEL7 | −40°C to +85°C | 6-Lead SOT-23, 7-Inch Tape and Reel | RJ-6 | HHA |
| AD8063ARTZ-R2 | −40°C to +85°C | 6-Lead SOT-23, 250 Piece Tape and Reel | RJ-6 | H0E[3] |
| AD8063ARTZ-REEL | −40°C to +85°C | 6-Lead SOT-23, 13-Inch Tape and Reel | RJ-6 | H0E[3] |
| AD8063ARTZ-REEL7 | −40°C to +85°C | 6-Lead SOT-23, 7-Inch Tape and Reel | RJ-6 | H0E[3] |
| AD8063AR-EBZ | | Evaluation Board for 8-Lead SOIC_N | | |
| AD8063ART-EBZ | | Evaluation Board for 6-Lead SOT-23 | | |

[1] Z = RoHS Compliant Part, # denotes RoHS product may be top or bottom marked.
[2] New branding after data code 0542, previously branded HGA.
[3] New branding after data code 0542, previously branded HHA.

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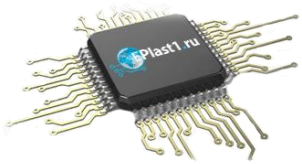


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