



256K X 36, 512K X 18
3.3V Synchronous SRAMs
3.3V I/O, Burst Counter
Pipelined Outputs, Single Cycle Deselect

IDT71V67603/Z
IDT71V67803/Z

Features

- ◆ 256K x 36, 512K x 18 memory configurations
- ◆ Supports high system speed:
 - 166MHz 3.5ns clock access time
 - 150MHz 3.8ns clock access time
 - 133MHz 4.2ns clock access time
- ◆ LBO input selects interleaved or linear burst mode
- ◆ Self-timed write cycle with global write control (\overline{GW}), byte write enable (\overline{BWE}), and byte writes (\overline{BWx})
- ◆ 3.3V core power supply
- ◆ Power down controlled by ZZ input
- ◆ 3.3V I/O supply (V_{DDQ})
- ◆ Packaged in a JEDEC Standard 100-pin thin plastic quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array (fBGA).

256K x 36/512K x 18. The IDT71V67603/7803 SRAMs contain write, data, address and control registers. Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V67603/7803 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected (\overline{ADV} =LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses are defined by the internal burst counter and the \overline{LBO} input pin.

The IDT71V67603/7803 SRAMs utilize IDT's latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP), a 119 ball grid array (BGA) and a 165 fine pitch ball grid array (fBGA).

Description

The IDT71V67603/7803 are high-speed SRAMs organized as

Pin Description Summary

| | | | |
|---|-----------------------------------|--------|--------------|
| A ₀ -A ₁₈ | Address Inputs | Input | Synchronous |
| \overline{CE} | Chip Enable | Input | Synchronous |
| CS ₀ , \overline{CS}_1 | Chip Selects | Input | Synchronous |
| \overline{OE} | Output Enable | Input | Asynchronous |
| \overline{GW} | Global Write Enable | Input | Synchronous |
| \overline{BWE} | Byte Write Enable | Input | Synchronous |
| \overline{BW}_1 , \overline{BW}_2 , \overline{BW}_3 , $\overline{BW}_4^{(1)}$ | Individual Byte Write Selects | Input | Synchronous |
| CLK | Clock | Input | N/A |
| \overline{ADV} | Burst Address Advance | Input | Synchronous |
| \overline{ADSC} | Address Status (Cache Controller) | Input | Synchronous |
| \overline{ADSP} | Address Status (Processor) | Input | Synchronous |
| \overline{LBO} | Linear / Interleaved Burst Order | Input | DC |
| ZZ | Sleep Mode | Input | Asynchronous |
| I/O ₀ -I/O ₃₁ , I/OP ₁ -I/OP ₄ | Data Input / Output | I/O | Synchronous |
| V _{DD} , V _{DDQ} | Core Power, I/O Power | Supply | N/A |
| V _{SS} | Ground | Supply | N/A |

NOTE:

5310 tbl 01

1. \overline{BW}_3 and \overline{BW}_4 are not applicable for the IDT71V67802.

FEBRUARY 2009

Pin Definitions⁽¹⁾

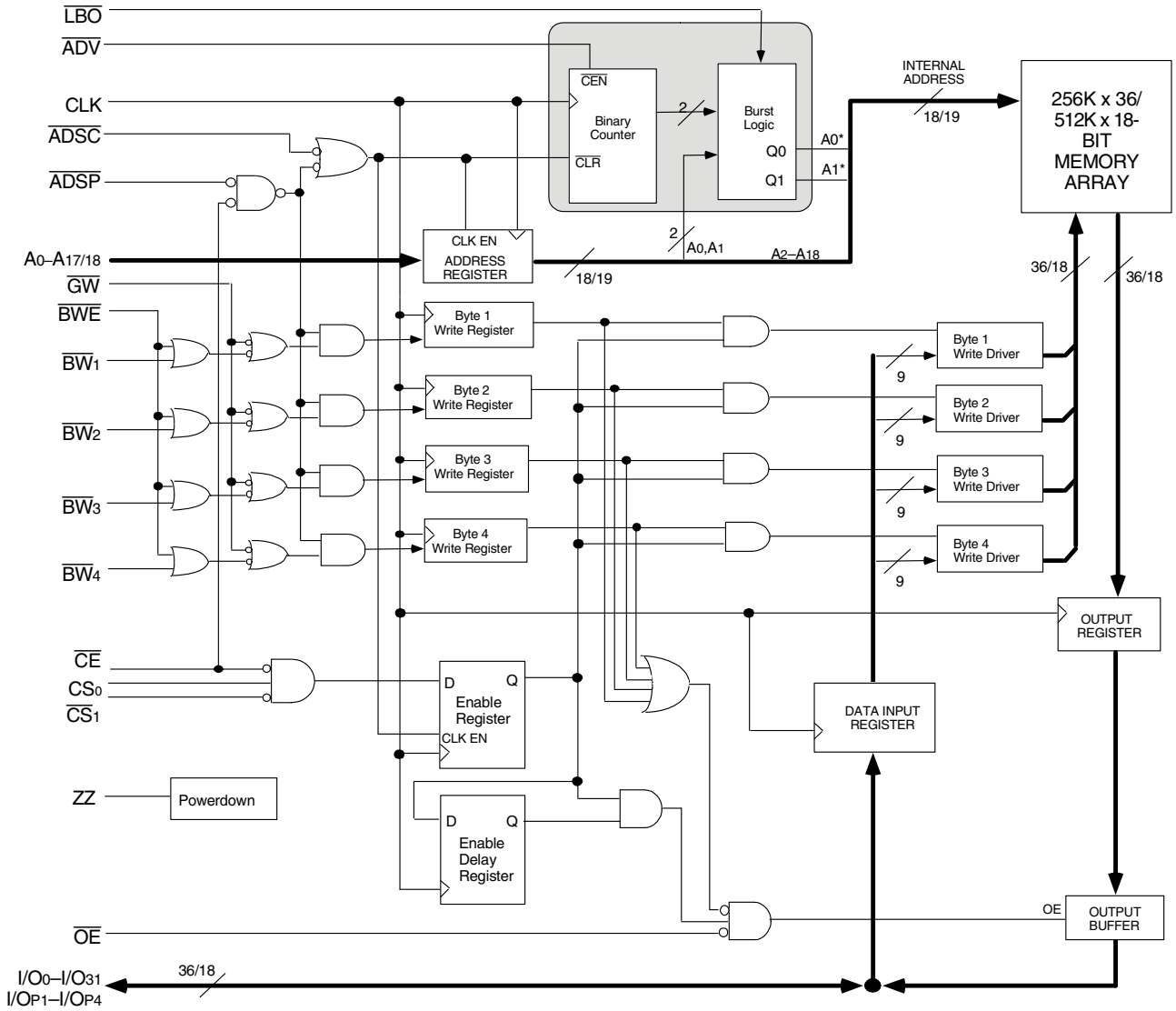
| Symbol | Pin Function | I/O | Active | Description |
|-----------------------------|-----------------------------------|-----|--------|--|
| A0-A18 | Address Inputs | I | N/A | Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and $\overline{\text{ADSC}}$ Low or $\overline{\text{ADSP}}$ Low and $\overline{\text{CE}}$ Low. |
| $\overline{\text{ADSC}}$ | Address Status (Cache Controller) | I | LOW | Synchronous Address Status from Cache Controller. $\overline{\text{ADSC}}$ is an active LOW input that is used to load the address registers with new addresses. |
| $\overline{\text{ADSP}}$ | Address Status (Processor) | I | LOW | Synchronous Address Status from Processor. $\overline{\text{ADSP}}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{\text{ADSP}}$ is gated by $\overline{\text{CE}}$. |
| $\overline{\text{ADV}}$ | Burst Address Advance | I | LOW | Synchronous Address Advance. $\overline{\text{ADV}}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When the input is HIGH the burst counter is not incremented; that is, there is no address advance. |
| $\overline{\text{BWE}}$ | Byte Write Enable | I | LOW | Synchronous byte write enable gates the byte write inputs $\overline{\text{BW1-BW4}}$. If $\overline{\text{BWE}}$ is LOW at the rising edge of CLK then $\overline{\text{BWx}}$ inputs are passed to the next stage in the circuit. If $\overline{\text{BWE}}$ is HIGH then the byte write inputs are blocked and only $\overline{\text{GW}}$ can initiate a write cycle. |
| $\overline{\text{BW1-BW4}}$ | Individual Byte Write Enables | I | LOW | Synchronous byte write enables. $\overline{\text{BW1}}$ controls I/O0-7, I/OP1, $\overline{\text{BW2}}$ controls I/O8-15, I/OP2, etc. Any active byte write causes all outputs to be disabled. |
| $\overline{\text{CE}}$ | Chip Enable | I | LOW | Synchronous chip enable. $\overline{\text{CE}}$ is used with CS0 and $\overline{\text{CS1}}$ to enable the IDT71V67603/7803. $\overline{\text{CE}}$ also gates $\overline{\text{ADSP}}$. |
| CLK | Clock | I | N/A | This is the clock input. All timing references for the device are made with respect to this input. |
| CS0 | Chip Select 0 | I | HIGH | Synchronous active HIGH chip select. CS0 is used with $\overline{\text{CE}}$ and $\overline{\text{CS1}}$ to enable the chip. |
| $\overline{\text{CS1}}$ | Chip Select 1 | I | LOW | Synchronous active LOW chip select. $\overline{\text{CS1}}$ is used with $\overline{\text{CE}}$ and CS0 to enable the chip. |
| $\overline{\text{GW}}$ | Global Write Enable | I | LOW | Synchronous global write enable. This input will write all four 9-bit data bytes when LOW on the rising edge of CLK. $\overline{\text{GW}}$ supersedes individual byte write enables. |
| I/O0-I/O31 I/OP1-I/OP4 | Data Input/Output | I/O | N/A | Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK. |
| $\overline{\text{LBO}}$ | Linear Burst Order | I | LOW | Asynchronous burst order selection input. When $\overline{\text{LBO}}$ is HIGH, the interleaved burst sequence is selected. When $\overline{\text{LBO}}$ is LOW the Linear burst sequence is selected. $\overline{\text{LBO}}$ is a static input and must not change state while the device is operating. |
| $\overline{\text{OE}}$ | Output Enable | I | LOW | Asynchronous output enable. When $\overline{\text{OE}}$ is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When $\overline{\text{OE}}$ is HIGH the I/O pins are in a high-impedance state. |
| VDD | Power Supply | N/A | N/A | 3.3V core power supply. |
| VDDO | Power Supply | N/A | N/A | 3.3V I/O Supply. |
| VSS | Ground | N/A | N/A | Ground. |
| NC | No Connect | N/A | N/A | NC pins are not electrically connected to the device. |
| ZZ | Sleep Mode | I | HIGH | Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V67603/7803 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. |

NOTE:

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

5310 tbl 02

Functional Block Diagram



5301 drw 01

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Commercial | Unit |
|------------------------------------|--------------------------------------|-------------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| V _{TERM} ^(3,6) | Terminal Voltage with Respect to GND | -0.5 to V _{DD} | V |
| V _{TERM} ^(4,6) | Terminal Voltage with Respect to GND | -0.5 to V _{DD} +0.5 | V |
| V _{TERM} ^(5,6) | Terminal Voltage with Respect to GND | -0.5 to V _{DDQ} +0.5 | V |
| T _A ⁽⁷⁾ | Operating Temperature | -0 to +70 | °C |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -55 to +125 | °C |
| P _T | Power Dissipation | 2.0 | W |
| I _{OUT} | DC Output Current | 50 | mA |

NOTES:

5310 tbl 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{DD} terminals only.
- V_{DDQ} terminals only.
- Input terminals only.
- I/O terminals only.
- This is a steady-state DC parameter that applies after the power supplies have ramped up. Power supply sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
- T_A is the "instant on" case temperature.

Recommended Operating Temperature and Supply Voltage

| Grade | Temperature ⁽¹⁾ | V _{SS} | V _{DD} | V _{DDQ} |
|------------|----------------------------|-----------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 0V | 3.3V±5% | 3.3V±5% |
| Industrial | -40°C to +85°C | 0V | 3.3V±5% | 3.3V±5% |

NOTE:

5310 tbl 04

- T_A is the "instant on" case temperature.

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|-----------------------------|---------------------|------|-----------------------|------|
| V _{DD} | Core Supply Voltage | 3.135 | 3.3 | 3.465 | V |
| V _{DDQ} | I/O Supply Voltage | 3.135 | 3.3 | 3.465 | V |
| V _{SS} | Supply Voltage | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage - Inputs | 2.0 | — | V _{DD} +0.3 | V |
| V _{IH} | Input High Voltage - I/O | 2.0 | — | V _{DDQ} +0.3 | V |
| V _{IL} | Input Low Voltage | -0.3 ⁽¹⁾ | — | 0.8 | V |

5310 tbl 05

NOTE:

- V_{IL} (min) = -1.0V for pulse width less than t_{CVI2}, once per cycle.

100 Pin TQFP Capacitance

(T_A = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|------------------|--------------------------|------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 5 | pF |
| C _{I/O} | I/O Capacitance | V _{OUT} = 3dV | 7 | pF |

5310 tbl 07

165 fBGA Capacitance

(T_A = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|------------------|--------------------------|------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 7 | pF |
| C _{I/O} | I/O Capacitance | V _{OUT} = 3dV | 7 | pF |

5310 tbl 07b

119 BGA Capacitance

(T_A = +25°C, f = 1.0MHz)

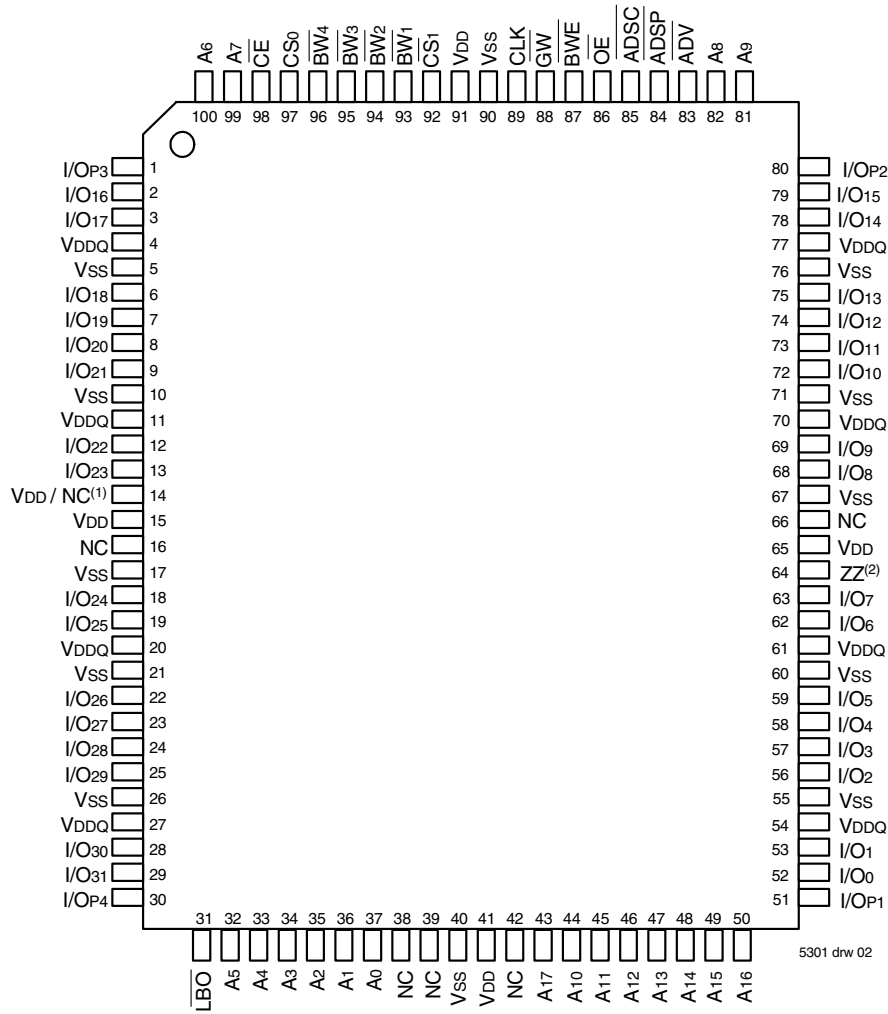
| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|------------------|--------------------------|------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 7 | pF |
| C _{I/O} | I/O Capacitance | V _{OUT} = 3dV | 7 | pF |

5310 tbl 07a

NOTE:

- This parameter is guaranteed by device characterization, but not production tested.

Pin Configuration – 256K x 36, 100-Pin TQFP

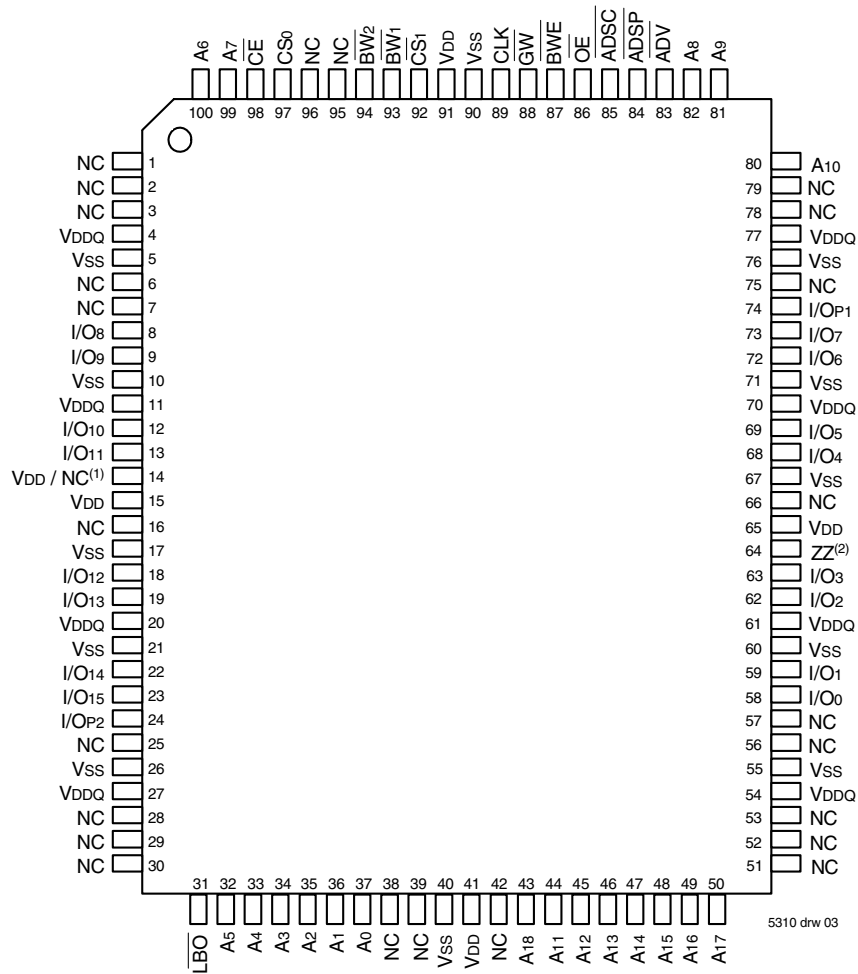


Top View

NOTES:

1. Pin 14 can either be directly connected to V_{DD}, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

Pin Configuration – 512K x 18, 100-Pin TQFP

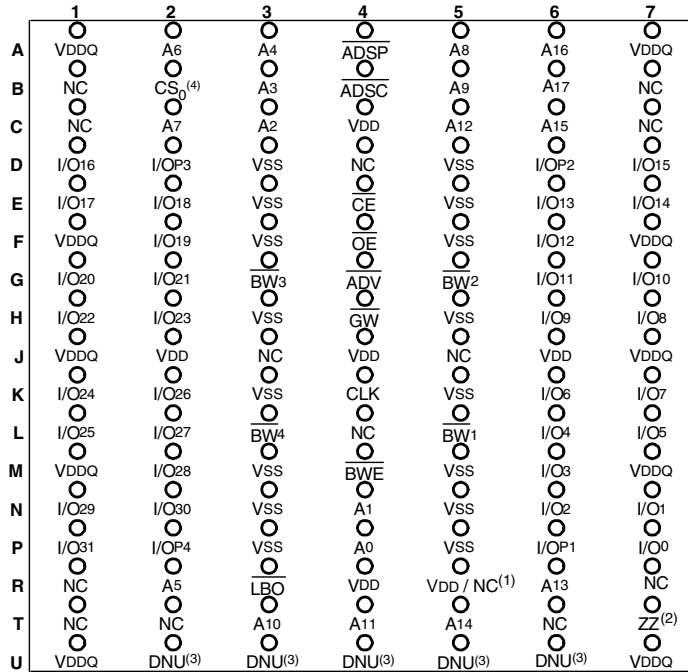


Top View

NOTES:

1. Pin 14 can either be directly connected to VDD, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

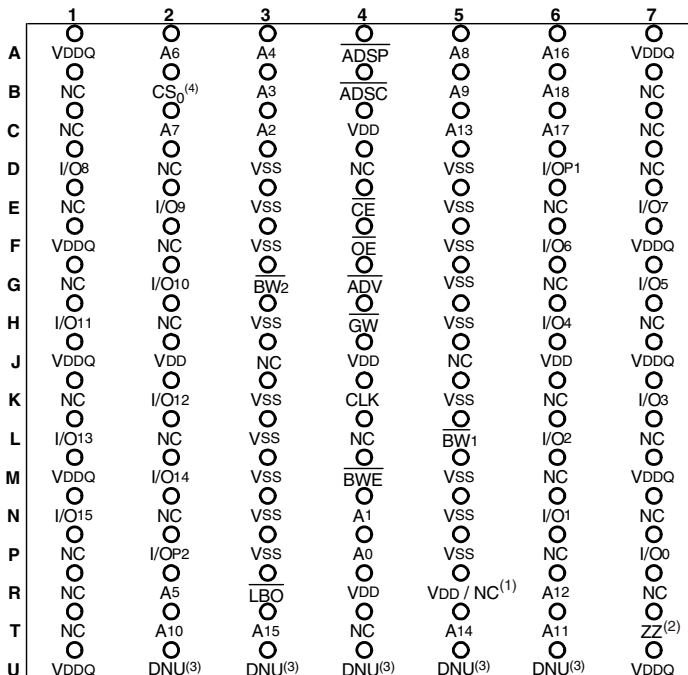
Pin Configuration – 256K x 36, 119 BGA



5310 drw 04

Top View

Pin Configuration – 512K x 18, 119 BGA



5310 drw 05

Top View

NOTES:

1. R5 can either be directly connected to VDD, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
2. T7 can be left unconnected and the device will always remain in active mode.
3. DNU= Do not use; these signals can either be left unconnected or tied to Vss.
4. On future 18M device CS₀ will be removed, B2 will be used for address expansion.

Pin Configuration – 256K x 36, 165 fBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|--------------------|-------------------|-----------------|-------------------|--------------------|-------------------|--------------------|-------------------|-------------------|-------------------|-------------------|
| A | NC ⁽³⁾ | A7 | \overline{CE} | \overline{BW}_3 | \overline{BW}_2 | \overline{CS}_1 | \overline{BWE} | \overline{ADSC} | \overline{ADV} | A8 | NC |
| B | NC | A6 | CS0 | \overline{BW}_4 | \overline{BW}_1 | CLK | \overline{GW} | \overline{OE} | \overline{ADSP} | A9 | NC ⁽³⁾ |
| C | I/O _{P3} | NC | VDDQ | VSS | VSS | VSS | VSS | VSS | VDDQ | NC | I/O _{P2} |
| D | I/O ₁₇ | I/O ₁₆ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₁₅ | I/O ₁₄ |
| E | I/O ₁₉ | I/O ₁₈ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₁₃ | I/O ₁₂ |
| F | I/O ₂₁ | I/O ₂₀ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₁₁ | I/O ₁₀ |
| G | I/O ₂₃ | I/O ₂₂ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₉ | I/O ₈ |
| H | VDD ⁽¹⁾ | NC | NC | VDD | VSS | VSS | VSS | VDD | NC | NC | ZZ ⁽²⁾ |
| J | I/O ₂₅ | I/O ₂₄ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₇ | I/O ₆ |
| K | I/O ₂₇ | I/O ₂₆ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₅ | I/O ₄ |
| L | I/O ₂₉ | I/O ₂₈ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₃ | I/O ₂ |
| M | I/O ₃₁ | I/O ₃₀ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₁ | I/O ₀ |
| N | I/O _{P4} | NC | VDDQ | VSS | NC | NC ⁽³⁾ | NC | VSS | VDDQ | NC | I/O _{P1} |
| P | NC | NC ⁽³⁾ | A5 | A2 | DNU ⁽⁴⁾ | A1 | DNU ⁽⁴⁾ | A10 | A13 | A14 | A17 |
| R | \overline{LBO} | NC ⁽³⁾ | A4 | A3 | DNU ⁽⁴⁾ | A0 | DNU ⁽⁴⁾ | A11 | A12 | A15 | A16 |

5310 tbl 17a

Pin Configuration – 512K x 18, 165 fBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|--------------------|-------------------|-----------------|-------------------|--------------------|-------------------|--------------------|-------------------|-------------------|------------------|-------------------|
| A | NC ⁽³⁾ | A7 | \overline{CE} | \overline{BW}_2 | NC | \overline{CS}_1 | \overline{BWE} | \overline{ADSC} | \overline{ADV} | A8 | A10 |
| B | NC | A6 | CS0 | NC | \overline{BW}_1 | CLK | \overline{GW} | \overline{OE} | \overline{ADSP} | A9 | NC ⁽³⁾ |
| C | NC | NC | VDDQ | VSS | VSS | VSS | VSS | VSS | VDDQ | NC | I/O _{P1} |
| D | NC | I/O ₈ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O ₇ |
| E | NC | I/O ₉ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O ₆ |
| F | NC | I/O ₁₀ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O ₅ |
| G | NC | I/O ₁₁ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O ₄ |
| H | VDD ⁽¹⁾ | NC | NC | VDD | VSS | VSS | VSS | VDD | NC | NC | ZZ ⁽²⁾ |
| J | I/O ₁₂ | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₃ | NC |
| K | I/O ₁₃ | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₂ | NC |
| L | I/O ₁₄ | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₁ | NC |
| M | I/O ₁₅ | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₀ | NC |
| N | I/O _{P2} | NC | VDDQ | VSS | NC | NC ⁽³⁾ | NC | VSS | VDDQ | NC | NC |
| P | NC | NC ⁽³⁾ | A5 | A2 | DNU ⁽⁴⁾ | A1 | DNU ⁽⁴⁾ | A11 | A14 | A15 | A18 |
| R | \overline{LBO} | NC ⁽³⁾ | A4 | A3 | DNU ⁽⁴⁾ | A0 | DNU ⁽⁴⁾ | A12 | A13 | A16 | A17 |

5310 tbl 17b

NOTES:

1. H1 can either be directly connected to VDD, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
2. H11 can be left unconnected and the device will always remain in active mode.
3. Pin N6, B11, A1, R2 and P2 are reserved for 18M, 36M, 72M, and 144M and 288M respectively.
4. DNU= Do not use; these signals can either be left unconnected or tied to VSS.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD} = 3.3V \pm 5\%$)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-------------|--|---|------|------|---------|
| $ I_{L} $ | Input Leakage Current | $V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$ | — | 5 | μA |
| $ I_{LZZ} $ | ZZ and \overline{LBO} Input Leakage Current ⁽¹⁾ | $V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$ | — | 30 | μA |
| $ I_{LO} $ | Output Leakage Current | $V_{OUT} = 0V \text{ to } V_{DDQ}, \text{ Device Deselected}$ | — | 5 | μA |
| V_{OL} | Output Low Voltage | $I_{OL} = +8mA, V_{DD} = \text{Min.}$ | — | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -8mA, V_{DD} = \text{Min.}$ | 2.4 | — | V |

5310 tbl 08

NOTE:

1. The \overline{LBO} pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ pin will be internally pulled to V_{SS} if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽¹⁾

| Symbol | Parameter | Test Conditions | 166MHz | 150MHz | | 133MHz | | Unit |
|-----------|------------------------------------|---|------------|--------|-----|--------|-----|------|
| | | | Com'l only | Com'l | Ind | Com'l | Ind | |
| I_{DD} | Operating Power Supply Current | Device Selected, Outputs Open, $V_{DD} = \text{Max.}, V_{DDQ} = \text{Max.}, V_{IN} \geq V_{IH} \text{ or } \leq V_{IL}, f = f_{MAX}^{(2)}$ | 340 | 305 | 325 | 260 | 280 | mA |
| I_{SB1} | CMOS Standby Power Supply Current | Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{DDQ} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = 0^{(2,3)}$ | 50 | 50 | 70 | 50 | 70 | mA |
| I_{SB2} | Clock Running Power Supply Current | Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{DDQ} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = f_{MAX}^{(2,3)}$ | 160 | 155 | 175 | 150 | 170 | mA |
| I_{ZZ} | Full Sleep Mode Supply Current | $ZZ \geq V_{HD}, V_{DD} = \text{Max.}$ | 50 | 50 | 70 | 50 | 70 | mA |

5310 tbl 09

NOTES:

- All values are maximum guaranteed values.
- At $f = f_{MAX}$, inputs are cycling at the maximum frequency of read cycles of $1/t_{cvc}$ while $\overline{ADSC} = \text{LOW}$; $f=0$ means no input lines are changing.
- For I/Os $V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V$. For other inputs $V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V$.

AC Test Conditions ($V_{DDQ} = 3.3V$)

| | |
|--------------------------------|--------------|
| Input Pulse Levels | 0 to 3V |
| Input Rise/Fall Times | 2ns |
| Input Timing Reference Levels | 1.5V |
| Output Timing Reference Levels | 1.5V |
| AC Test Load | See Figure 1 |

5310 tbl 10

AC Test Load

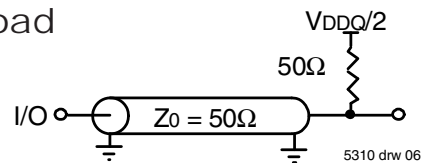


Figure 1. AC Test Load

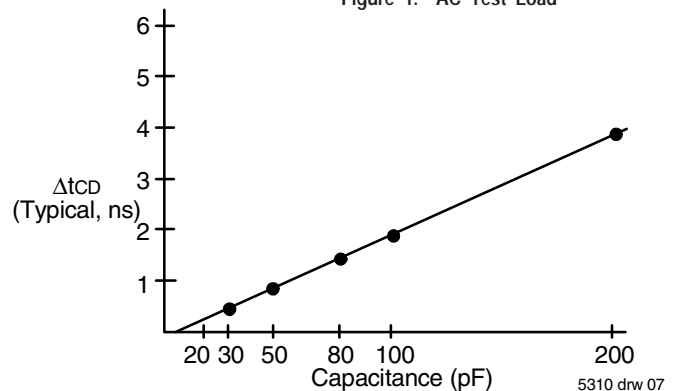


Figure 2. Lumped Capacitive Load, Typical Derating

Synchronous Truth Table^(1,3)

| Operation | Address Used | \overline{CE} | CS ₀ | \overline{CS}_1 | \overline{ADSP} | \overline{ADSC} | \overline{ADV} | \overline{GW} | \overline{BWE} | \overline{BW}_x | \overline{OE} (2) | CLK | I/O |
|------------------------------|--------------|-----------------|-----------------|-------------------|-------------------|-------------------|------------------|-----------------|------------------|-------------------|---------------------|-----|------|
| Deselected Cycle, Power Down | None | H | X | X | X | L | X | X | X | X | X | - | HI-Z |
| Deselected Cycle, Power Down | None | L | X | H | L | X | X | X | X | X | X | - | HI-Z |
| Deselected Cycle, Power Down | None | L | L | X | L | X | X | X | X | X | X | - | HI-Z |
| Deselected Cycle, Power Down | None | L | X | H | X | L | X | X | X | X | X | - | HI-Z |
| Deselected Cycle, Power Down | None | L | L | X | X | L | X | X | X | X | X | - | HI-Z |
| Read Cycle, Begin Burst | External | L | H | L | L | X | X | X | X | X | L | - | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | L | X | X | X | X | X | H | - | HI-Z |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | H | X | L | - | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | H | L | - | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | H | H | - | HI-Z |
| Write Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | L | X | - | DIN |
| Write Cycle, Begin Burst | External | L | H | L | H | L | X | L | X | X | X | - | DIN |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | H | X | L | - | DOUT |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | H | X | H | - | HI-Z |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | X | H | L | - | DOUT |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | X | H | H | - | HI-Z |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | H | X | L | - | DOUT |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | H | X | H | - | HI-Z |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | X | H | L | - | DOUT |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | X | H | H | - | HI-Z |
| Write Cycle, Continue Burst | Next | X | X | X | H | H | L | H | L | L | X | - | DIN |
| Write Cycle, Continue Burst | Next | X | X | X | H | H | L | L | X | X | X | - | DIN |
| Write Cycle, Continue Burst | Next | H | X | X | X | H | L | H | L | L | X | - | DIN |
| Write Cycle, Continue Burst | Next | H | X | X | X | H | L | L | X | X | X | - | DIN |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | H | X | L | - | DOUT |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | H | X | H | - | HI-Z |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | X | H | L | - | DOUT |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | X | H | H | - | HI-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | H | X | L | - | DOUT |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | H | X | H | - | HI-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | X | H | L | - | DOUT |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | X | H | H | - | HI-Z |
| Write Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | L | L | X | - | DIN |
| Write Cycle, Suspend Burst | Current | X | X | X | H | H | H | L | X | X | X | - | DIN |
| Write Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | L | L | X | - | DIN |
| Write Cycle, Suspend Burst | Current | H | X | X | X | H | H | L | X | X | X | - | DIN |

NOTES:

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. \overline{OE} is an asynchronous input.
3. ZZ = low for this table.

5310 tbl 11

Synchronous Write Function Truth Table^(1, 2)

| Operation | \overline{GW} | \overline{BWE} | \overline{BW}_1 | \overline{BW}_2 | \overline{BW}_3 | \overline{BW}_4 |
|-----------------------------|-----------------|------------------|-------------------|-------------------|-------------------|-------------------|
| Read | H | H | X | X | X | X |
| Read | H | L | H | H | H | H |
| Write all Bytes | L | X | X | X | X | X |
| Write all Bytes | H | L | L | L | L | L |
| Write Byte 1 ⁽³⁾ | H | L | L | H | H | H |
| Write Byte 2 ⁽³⁾ | H | L | H | L | H | H |
| Write Byte 3 ⁽³⁾ | H | L | H | H | L | H |
| Write Byte 4 ⁽³⁾ | H | L | H | H | H | L |

5310 tbl 12

NOTES:

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
2. \overline{BW}_3 and \overline{BW}_4 are not applicable for the IDT71V67803.
3. Multiple bytes may be selected during the same cycle.

Asynchronous Truth Table⁽¹⁾

| Operation ⁽²⁾ | \overline{OE} | ZZ | I/O Status | Power |
|--------------------------|-----------------|----|------------------|---------|
| Read | L | L | Data Out | Active |
| Read | H | L | High-Z | Active |
| Write | X | L | High-Z - Data In | Active |
| Deselected | X | L | High-Z | Standby |
| Sleep Mode | X | H | High-Z | Sleep |

5310 tbl 13

NOTES:

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

Interleaved Burst Sequence Table ($\overline{LBO}=V_{DD}$)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|-------------------------------|------------|----|------------|----|------------|----|------------|----|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address ⁽¹⁾ | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

5310 tbl 14

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

Linear Burst Sequence Table ($\overline{LBO}=V_{SS}$)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|-------------------------------|------------|----|------------|----|------------|----|------------|----|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address ⁽¹⁾ | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

5310 tbl 15

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

AC Electrical Characteristics

(VDD = 3.3V ±5%, Commercial and Industrial Temperature Ranges)

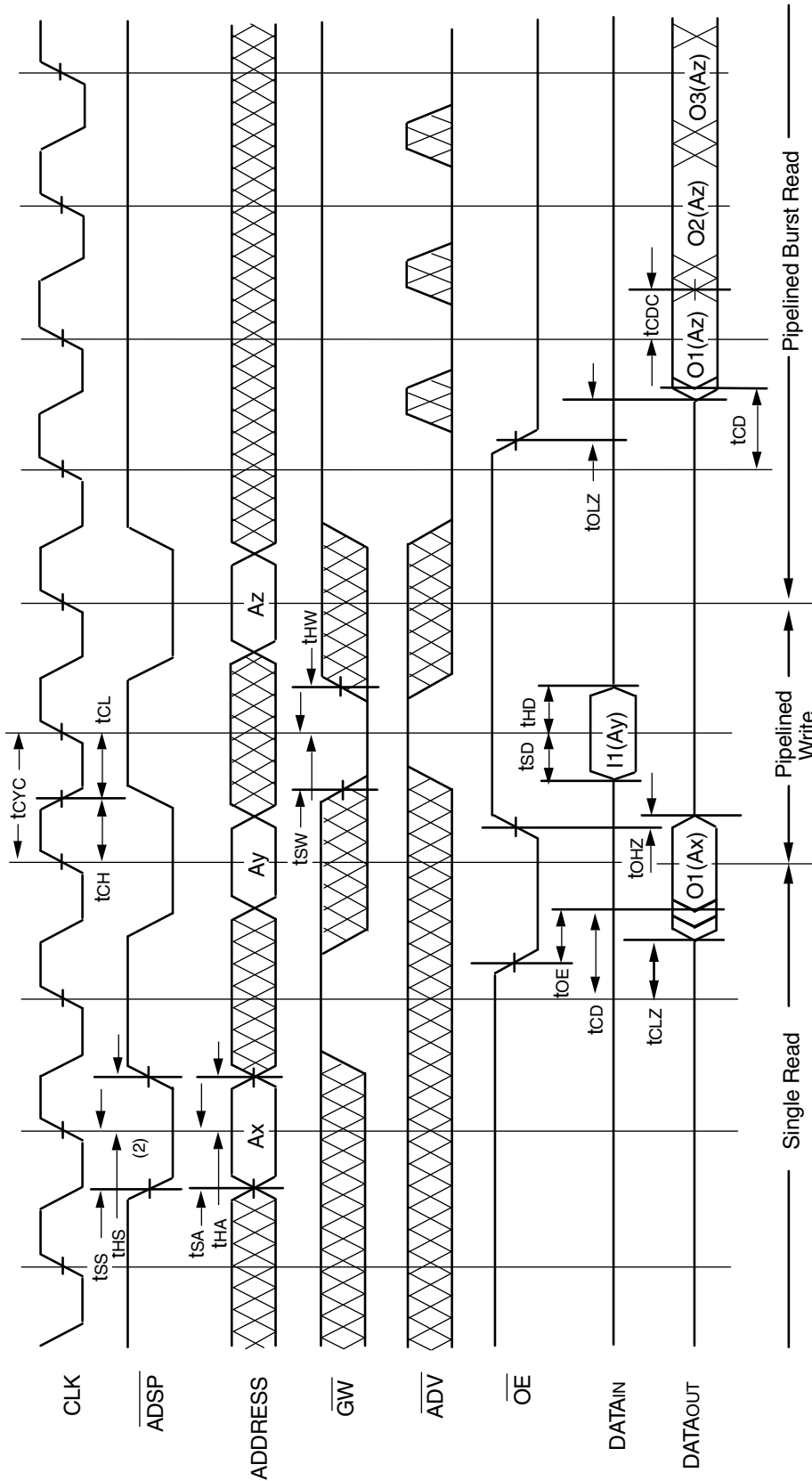
| Symbol | Parameter | 166MHz | | 150MHz | | 133MHz | | Unit |
|--|-------------------------------------|--------|------|--------|------|--------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{CYC} | Clock Cycle Time | 6 | — | 6.7 | — | 7.5 | — | ns |
| t _{CH} ⁽¹⁾ | Clock High Pulse Width | 2.4 | — | 2.6 | — | 3 | — | ns |
| t _{CL} ⁽¹⁾ | Clock Low Pulse Width | 2.4 | — | 2.6 | — | 3 | — | ns |
| Output Parameters | | | | | | | | |
| t _{CD} | Clock High to Valid Data | — | 3.5 | — | 3.8 | — | 4.2 | ns |
| t _{CD} | Clock High to Data Change | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{CLZ} ⁽²⁾ | Clock High to Output Active | 0 | — | 0 | — | 0 | — | ns |
| t _{CHZ} ⁽²⁾ | Clock High to Data High-Z | 1.5 | 3.5 | 1.5 | 3.8 | 1.5 | 4.2 | ns |
| t _{OE} | Output Enable Access Time | — | 3.5 | — | 3.8 | — | 4.2 | ns |
| t _{OLZ} ⁽²⁾ | Output Enable Low to Output Active | 0 | — | 0 | — | 0 | — | ns |
| t _{OHZ} ⁽²⁾ | Output Enable High to Output High-Z | — | 3.5 | — | 3.8 | — | 4.2 | ns |
| Set Up Times | | | | | | | | |
| t _{SA} | Address Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{SS} | Address Status Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{SD} | Data In Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{SW} | Write Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{SAV} | Address Advance Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| t _{SC} | Chip Enable/Select Setup Time | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| Hold Times | | | | | | | | |
| t _{HA} | Address Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HS} | Address Status Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HD} | Data In Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HW} | Write Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HAV} | Address Advance Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HC} | Chip Enable/Select Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| Sleep Mode and Configuration Parameters | | | | | | | | |
| t _{ZZPW} | ZZ Pulse Width | 100 | — | 100 | — | 100 | — | ns |
| t _{ZZR} ⁽³⁾ | ZZ Recovery Time | 100 | — | 100 | — | 100 | — | ns |
| t _{CFG} ⁽⁴⁾ | Configuration Set-up Time | 24 | — | 27 | — | 30 | — | ns |

5310 tbl 16

NOTES:

1. Measured as HIGH above V_{IH} and LOW below V_{IL}.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{\text{LBO}}$ input. $\overline{\text{LBO}}$ is a static input and must not change during normal operation.

Timing Waveform of Combined Pipelined Read and Write Cycles^(1,2,3)



5310 drw 09

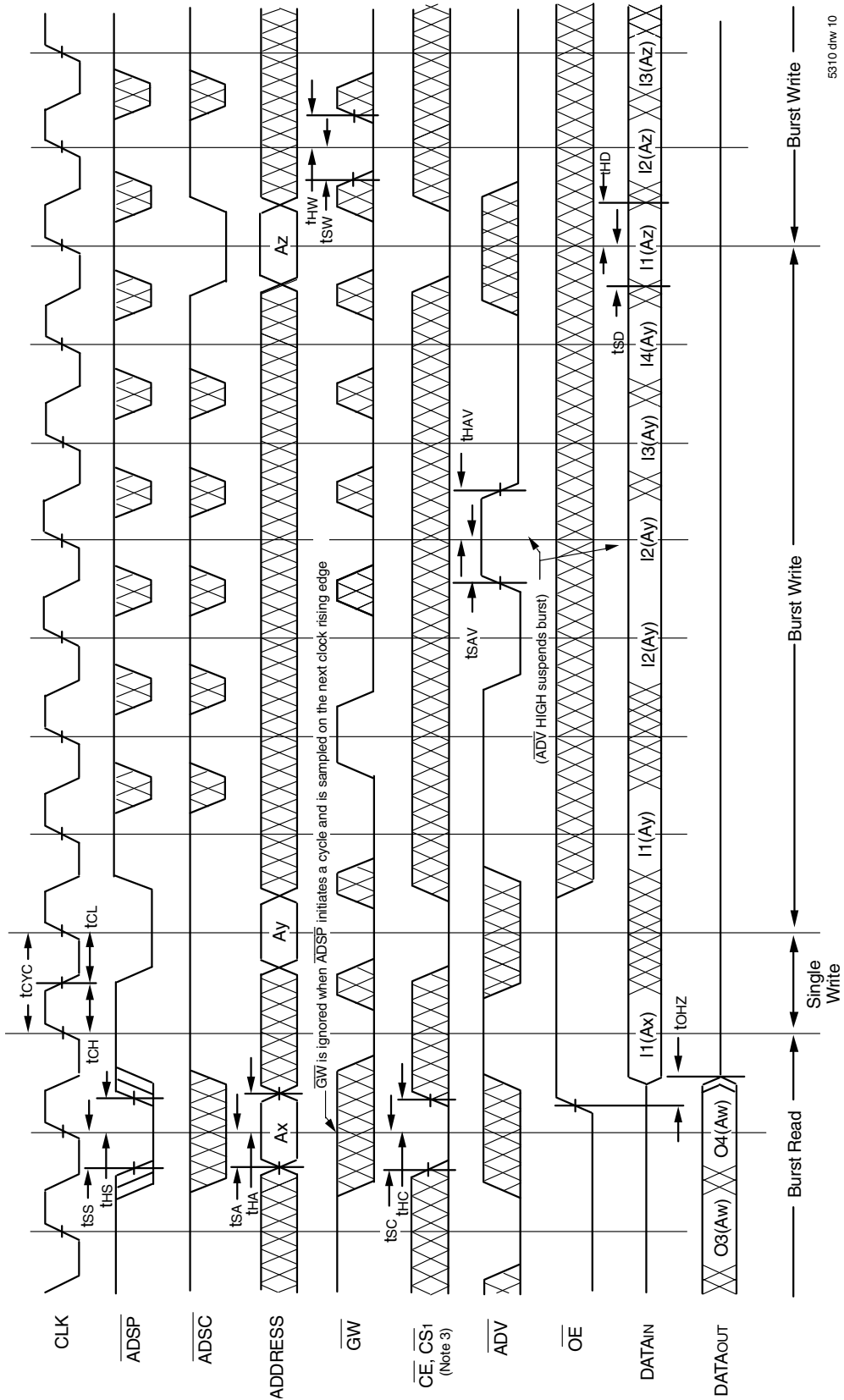
NOTES:

1. Device is selected through entire cycle; \overline{CE} and $\overline{CS1}$ are LOW, $\overline{CS0}$ is HIGH.

2. ZZ input is LOW and \overline{LBO} is Don't Care for this cycle.

3. O1 (Ax) represents the first output from the external address Ax. I1 (Ay) represents the first input from the external address Ay. O1 (Az) represents the first output from the external address Az, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the \overline{LBO} input.

Timing Waveform of Write Cycle No. 1 — **GW** Controlled^(1,2,3)

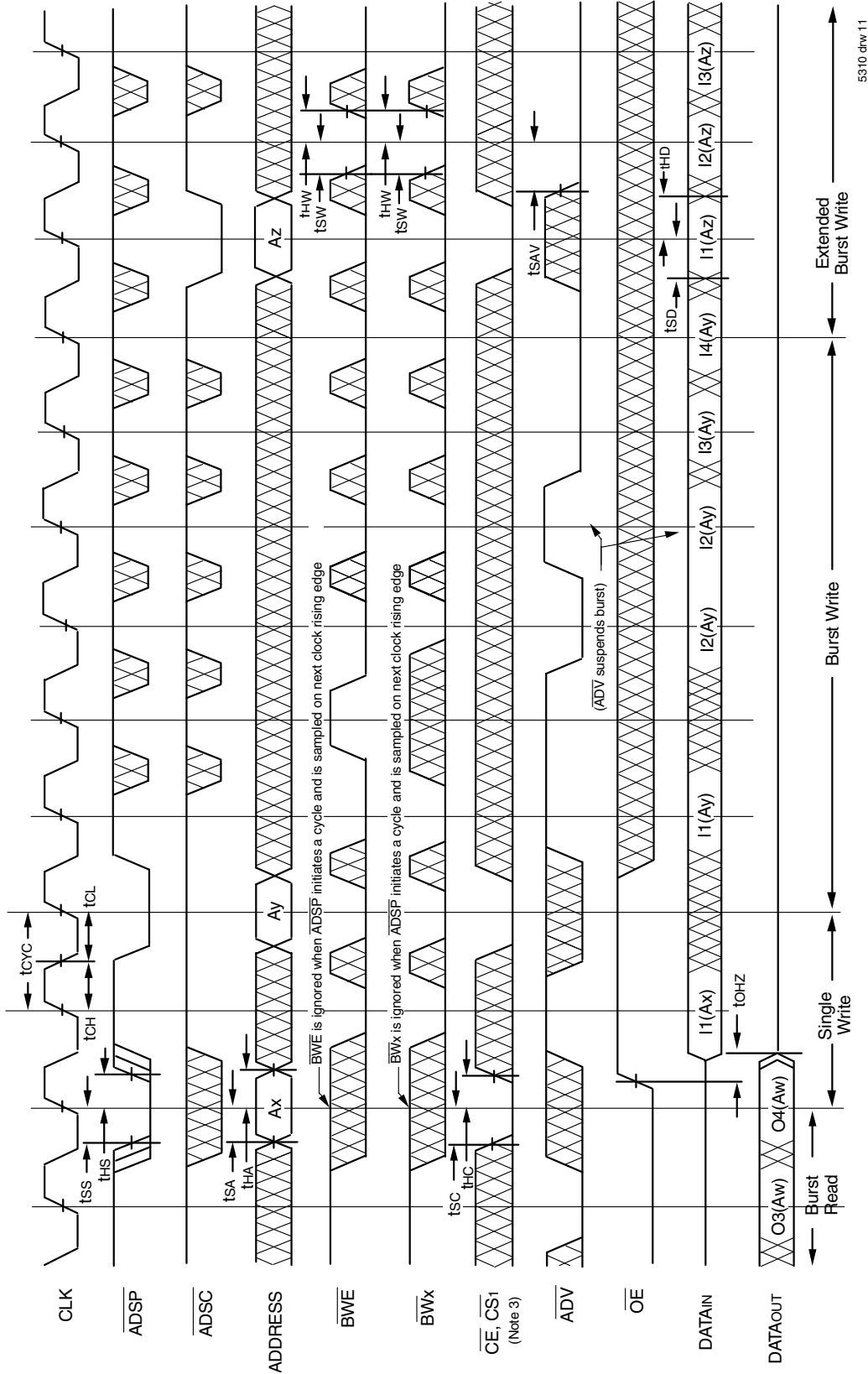


5310 drw 10

NOTES:

1. ZZ input is LOW, BWE is HIGH and LBO is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input. In the case of input I2 (Ay) this data is valid for two cycles because ADV is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the CE and CS1 signals. For example, when CE and CS1 are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Write Cycle No. 2 — Byte Controlled^(1,2,3)

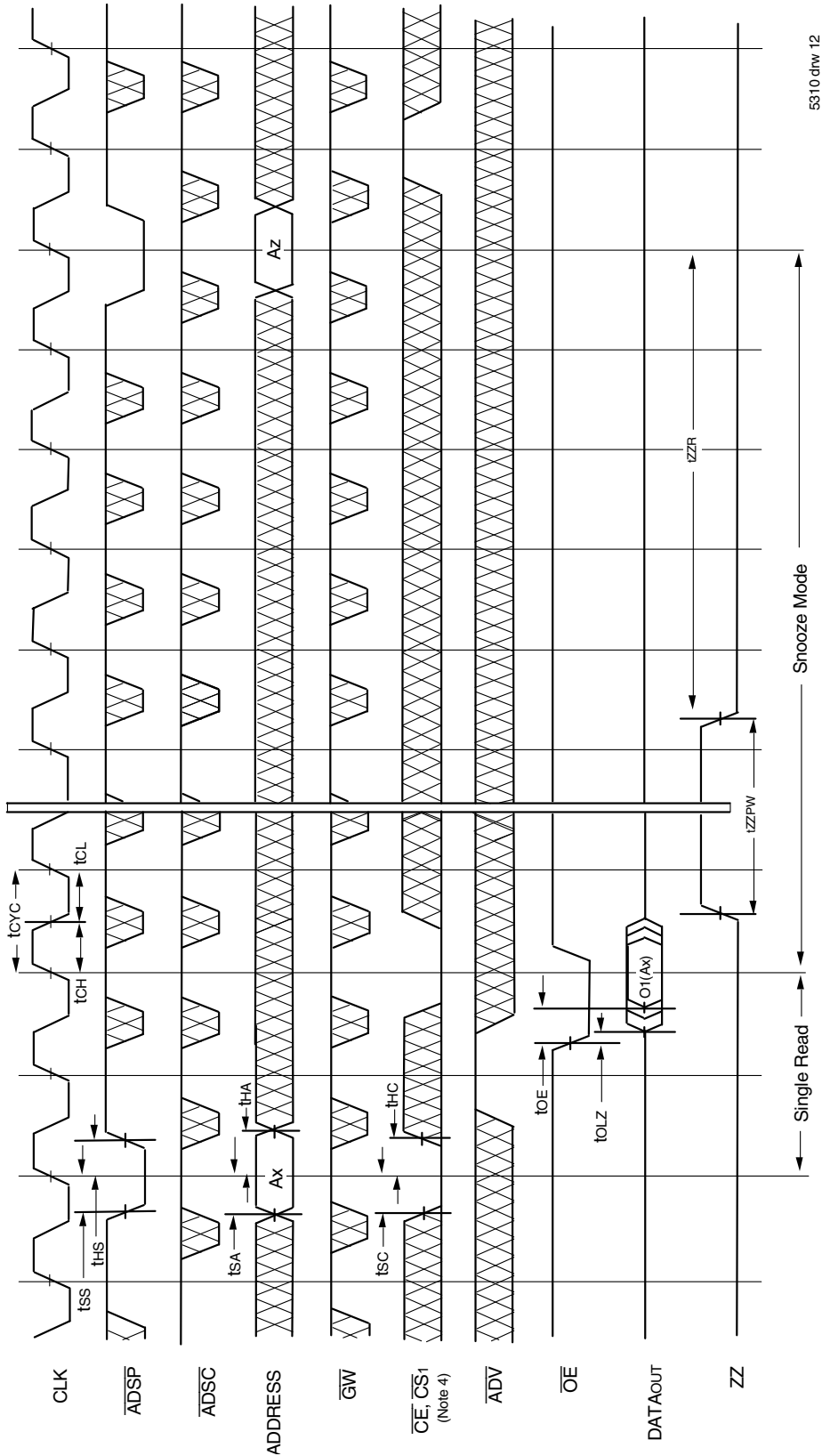


5310 d1w 11

NOTES:

1. Zz input is LOW, \overline{GW} is HIGH and \overline{LBO} is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input. In the case of input I2 (Ay) this data is valid for two cycles because ADV is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the CE and CS1 signals. For example, when \overline{CE} and CS1 are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Sleep (ZZ) and Power-Down Modes^(1,2,3)

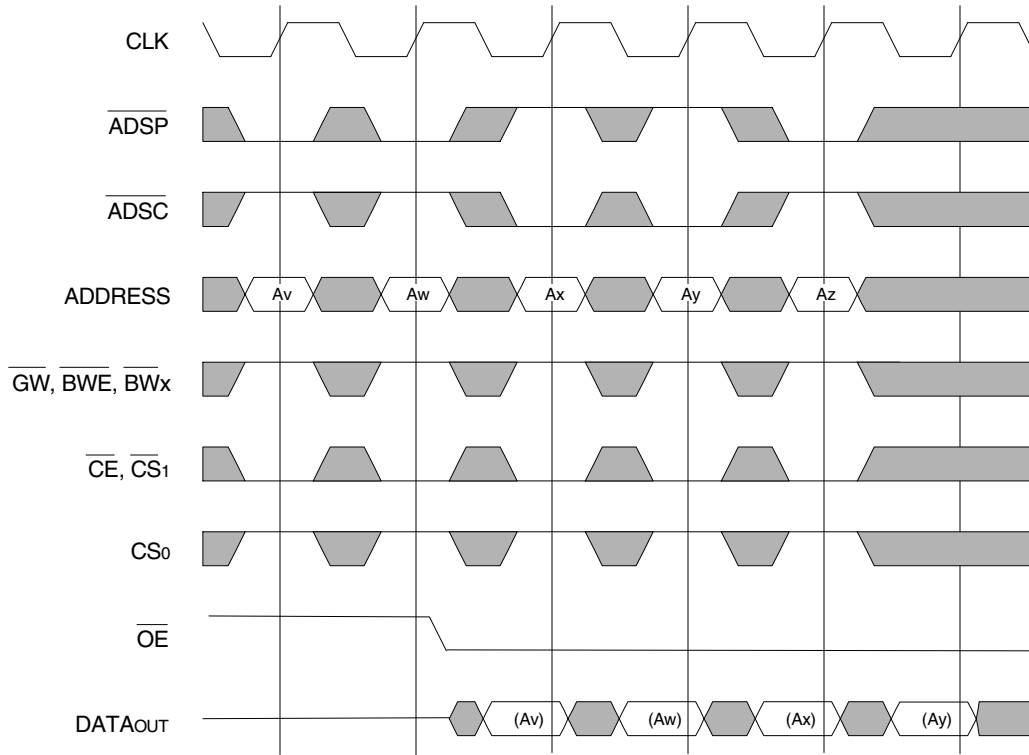


5910.drw.12

NOTES:

1. Device must power up in deselected Mode
2. LBO is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS0 timing transitions are identical but inverted to the CE and CS1 signals. For example, when CE and CS1 are LOW on this waveform, CS0 is HIGH.

Non-Burst Read Cycle Timing Waveform

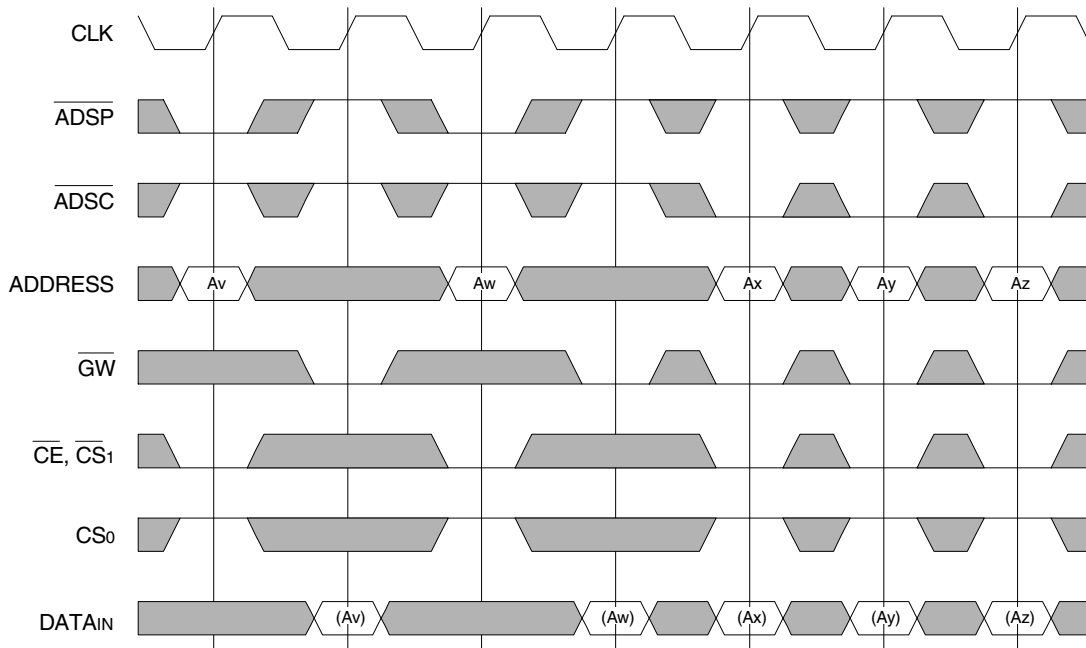


NOTES:

1. ZZ input is LOW, \overline{ADV} is HIGH and \overline{LBO} is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles, \overline{ADSP} and \overline{ADSC} function identically and are therefore interchangeable.

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Non-Burst Write Cycle Timing Waveform

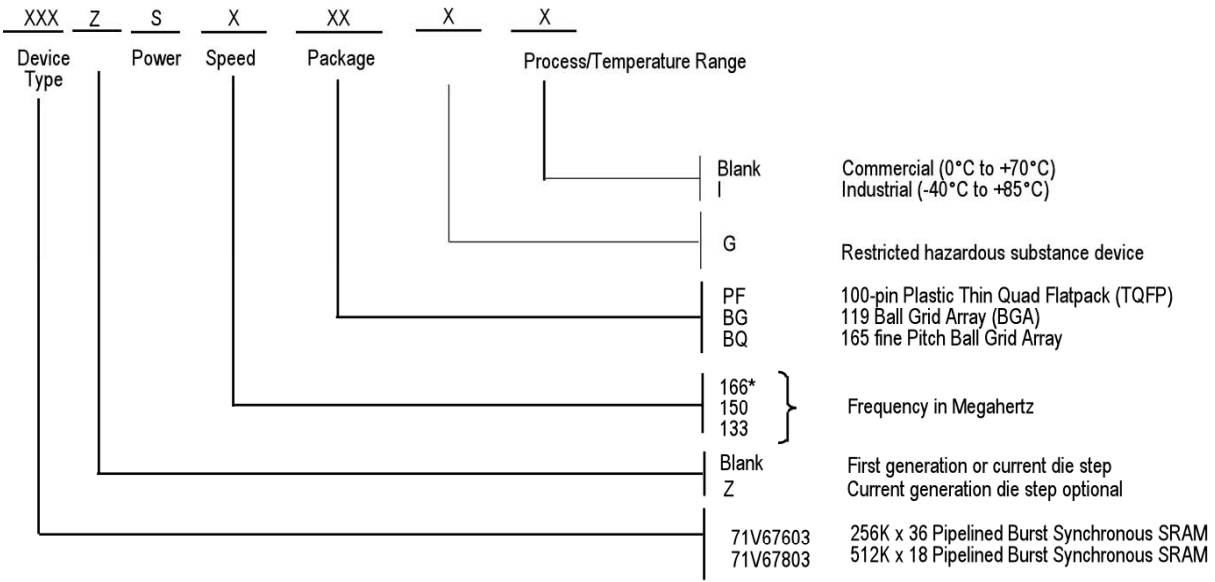


NOTES:

1. ZZ input is LOW, \overline{ADV} and \overline{OE} are HIGH, and \overline{LBO} is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. Although only \overline{GW} writes are shown, the functionality of \overline{BWE} and \overline{BWx} together is the same as \overline{GW} .
4. For write cycles, \overline{ADSP} and \overline{ADSC} have different limitations.

5310 drw 15

Ordering Information



5310 dw 13

* Industrial temperature not available on 166MHz devices

Datasheet Document History

| | | |
|-----------|--------------------|--|
| 12/31/99 | | Created datasheet from 71V676 and 71V678 datasheets. I/O voltage and speed grade offerings have been split into separate part numbers. See the following datasheets for: 3.3V I/O, 133-166MHz 71V67603 2.5V I/O, 133-166MHz 71V67602 3.3V I/O, 183-200MHz 71V67613 2.5V I/O, 183-200MHz 71V67612 |
| 04/26/00 | Pg. 4 | Add capacitance for BGA package; Insert clarification note to Absolute Max Ratings and Recommended Operating Temperature tables. |
| | Pg. 7 | Replace Pin U6 with TRST pin in BGA pin configuration; Add pin description note in pinout |
| | Pg. 18 | Inserted 100 pin TQFP Package Diagram Outline |
| 05/24/00 | Pg. 1,8,4,21 22 | Add new package offering, 13 x 15 fBGA |
| | Pg. 5,6,7,8 | Correct note 2 in BGA and TQFP pinouts |
| | Pg. 20 | Correction in the 119BGA Package Diagram Outline |
| 07/12/00 | Pg. 5,6 | Remove note from TQFP pinout |
| | Pg. 7 | Add/Remove reference note from BG119 pinout |
| | Pg. 9 | Remove note from BQ165 pinout |
| | Pg. 20 | Update BG119 Package Diagram Outline dimensions |
| 12/18/00 | Pg. 9 | Updated ISB2 levels for F=133-166MHz |
| 10/29/01 | Pg. 1,2 | Remove 166MHz and JTAG pins |
| | Pg. 7,8 | Updated pins U2-U6 to DNU and P5,P7,R5 & R7 to DNU |
| | Pg. 9 | Remove 166MHz and raise range by 10mA on 150Mhz and 133MHz |
| | Pg. 12,22 | Remove 166MHz |
| 10/22/02 | Pg.1-22 | Changed datasheet from Advanced to final release. |
| | Pg. 4,9,12, 22 | Added I temp to datasheet. |
| 11/19/02 | Pg.1,9,12,22 | Added 166MHz to datasheet. |
| 04/15 /03 | Pg.4 | Updated 165fBGA table from TBD to 7. |
| 09/30/04 | Pg.7 | Updated 119BGA pin configurations-reordered I/O signals on P6, P7 (128K x 36) and P7, N6, L6, K7, H6, G7, F6, E7, D6 (256K x 18). |
| | Pg.22 | Added "Restricted hazardous substance device" to ordering information. |
| 02/21/07 | Pg.22 | Added Z generation die step to ordering information. |
| 02/20/09 | Pg 22 | Removed IDT from ordering information. |



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- Защита от снятия компонента с производства.



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