

74HC273; 74HCT273

Octal D-type flip-flop with reset; positive-edge trigger

Rev. 5 — 26 February 2016

Product data sheet

1. General description

The 74HC273; 74HCT273 is an octal positive-edge triggered D-type flip-flop. The device features clock (CP) and master reset (MR) inputs. The outputs Q_n will assume the state of their corresponding D_n inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A LOW on $\overline{\text{MR}}$ forces the outputs LOW independently of clock and data inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Input levels:
 - ◆ For 74HC273: CMOS level
 - ◆ For 74HCT273: TTL level
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | Version |
| 74HC273D | –40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74HCT273D | | | | |
| 74HC273DB | –40 °C to +125 °C | SSOP20 | plastic shrink small outline package; 20 leads; body width 5.3 mm | SOT339-1 |
| 74HCT273DB | | | | |
| 74HC273PW | –40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74HCT273PW | | | | |
| 74HC273BQ | –40 °C to +125 °C | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |
| 74HCT273BQ | | | | |

4. Functional diagram



Fig 1. Functional diagram

Fig 2. Logic symbol

Fig 3. IEC logic symbol

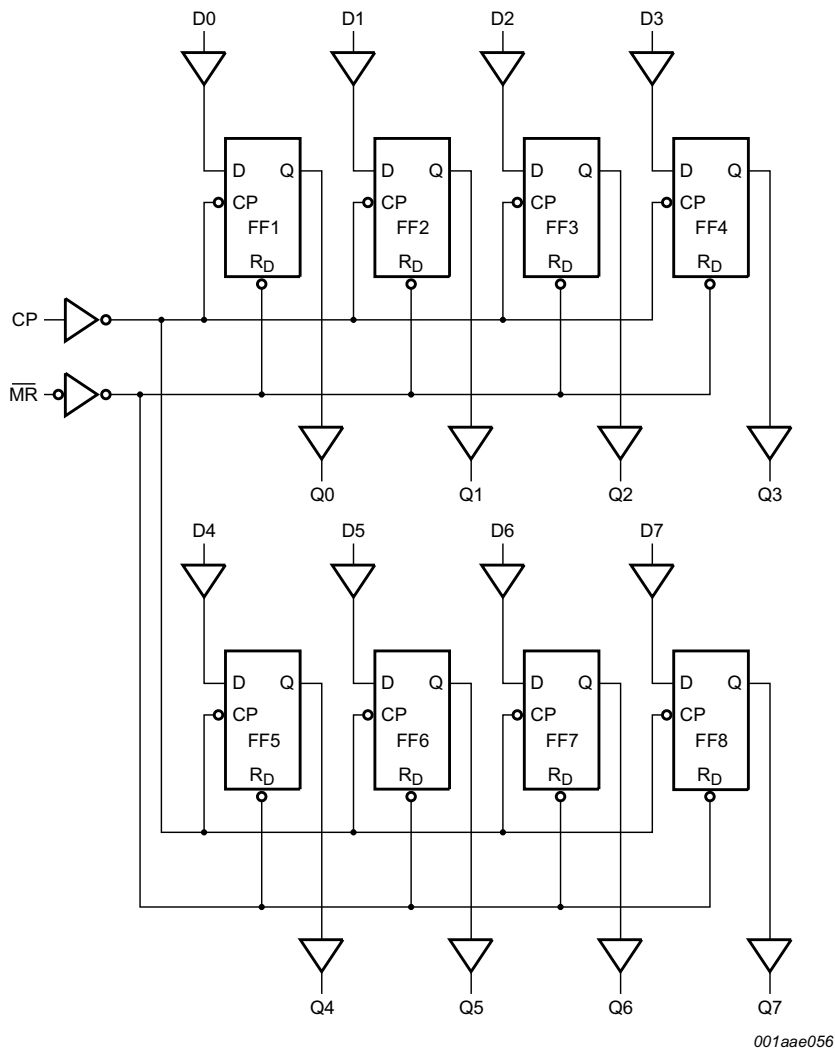
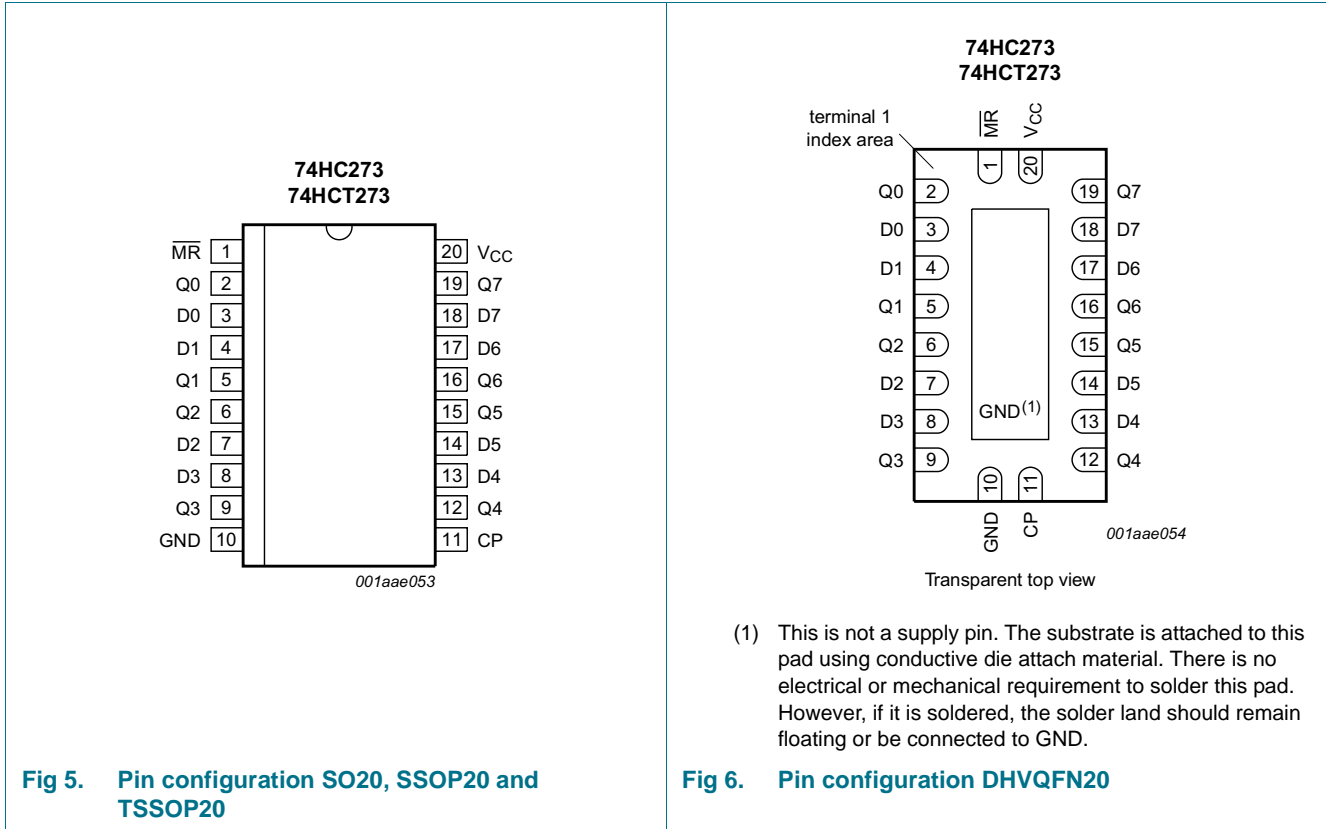


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------------------|----------------------------|---|
| $\overline{\text{MR}}$ | 1 | master reset input (active LOW) |
| Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7 | 2, 5, 6, 9, 12, 15, 16, 19 | flip-flop output |
| D0, D1, D2, D3, D4, D5, D6, D7 | 3, 4, 7, 8, 13, 14, 17, 18 | data input |
| GND | 10 | ground (0 V) |
| CP | 11 | clock input (LOW-to-HIGH, edge-triggered) |
| V _{CC} | 20 | supply voltage |

6. Functional description

Table 3. Function table^[1]

| Operating modes | Inputs | | | Outputs |
|-----------------|------------------------|----|----|---------|
| | $\overline{\text{MR}}$ | CP | Dn | Qn |
| reset (clear) | L | X | X | L |
| load "1" | H | ↑ | h | H |
| load "0" | H | ↑ | l | L |

- [1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 L = LOW voltage level;
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 X = don't care;
 ↑ = LOW-to-HIGH clock transition.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---|------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7 | V |
| I_{IK} | input clamping current | $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$ ^[1] | - | ±20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$ ^[1] | - | ±20 | mA |
| I_O | output current | $-0.5 \text{ V} < V_O < V_{CC} + 0.5 \text{ V}$ | - | ±25 | mA |
| I_{CC} | supply current | | - | 50 | mA |
| I_{GND} | ground current | | -50 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40 \text{ °C}$ to $+125 \text{ °C}$ | | | |
| | | SO20, SSOP20, TSSOP20 and DHVQFN20 package ^[2] | - | 500 | mW |

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] For SO20 package: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For SSOP20 and TSSOP20 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN20 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 74HC273 | | | 74HCT273 | | | Unit |
|------------------|-------------------------------------|-------------------------|---------|------|-----------------|----------|------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | - | +125 | -40 | - | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | V _{CC} = 6.0 V | - | - | 83 | - | - | - | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|--|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC273 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| | | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|--|-------|------|------|------------------|-------|-------------------|-------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |
| 74HCT273 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -20 µA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 20 µA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 5.2 mA; V _{CC} = 5.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 8.0 | - | 80 | - | 160 | µA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | MR input | - | 100 | 360 | - | 450 | - | 490 | µA |
| | | CP input | - | 175 | 630 | - | 787.5 | - | 857.5 | µA |
| | | Dn input | - | 15 | 54 | - | 67.5 | - | 73.5 | µA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristicsGND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see [Figure 10](#)

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|-------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC273 | | | | | | | | | | |
| t _{pd} | propagation delay | CP to Qn; see Figure 7 ^[1] | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 41 | 150 | - | 185 | - | 225 | ns |
| | | V _{CC} = 4.5 V | - | 15 | 30 | - | 37 | - | 45 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 15 | - | - | - | - | - | ns |
| | | V _{CC} = 6.0 V | - | 13 | 26 | - | 31 | - | 38 | ns |

Table 7. Dynamic characteristics ...continuedGND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 10](#)

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|-----------|-------------------------------|---|-------|------|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t_{PHL} | HIGH to LOW propagation delay | \overline{MR} to Qn; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 44 | 150 | - | 185 | - | 225 | ns |
| | | $V_{CC} = 4.5$ V | - | 16 | 30 | - | 37 | - | 45 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 15 | - | - | - | - | - | ns |
| | | $V_{CC} = 6.0$ V | - | 14 | 26 | - | 31 | - | 38 | ns |
| t_t | transition time | Qn output; see Figure 7 ^[2] | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | $V_{CC} = 4.5$ V | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | $V_{CC} = 6.0$ V | - | 6 | 13 | - | 15 | - | 19 | ns |
| t_{w} | pulse width | CP input HIGH or LOW; see Figure 7 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 80 | 14 | - | 100 | - | 120 | - | ns |
| | | $V_{CC} = 4.5$ V | 16 | 5 | - | 20 | - | 24 | - | ns |
| | | $V_{CC} = 6.0$ V | 14 | 4 | - | 17 | - | 20 | - | ns |
| | | \overline{MR} input LOW; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 60 | 17 | - | 75 | - | 90 | - | ns |
| | | $V_{CC} = 4.5$ V | 12 | 6 | - | 15 | - | 18 | - | ns |
| | | $V_{CC} = 6.0$ V | 10 | 5 | - | 13 | - | 15 | ns | |
| t_{rec} | recovery time | \overline{MR} to CP; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 50 | -6 | - | 65 | - | 75 | - | ns |
| | | $V_{CC} = 4.5$ V | 10 | -2 | - | 13 | - | 15 | - | ns |
| | | $V_{CC} = 6.0$ V | 9 | -2 | - | 11 | - | 13 | - | ns |
| t_{su} | set-up time | Dn to CP; see Figure 9 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 60 | 11 | - | 75 | - | 90 | - | ns |
| | | $V_{CC} = 4.5$ V | 12 | 4 | - | 15 | - | 18 | - | ns |
| | | $V_{CC} = 6.0$ V | 10 | 3 | - | 13 | - | 15 | - | ns |
| t_h | hold time | Dn to CP; see Figure 9 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 3 | -6 | - | 3 | - | 3 | - | ns |
| | | $V_{CC} = 4.5$ V | 3 | -2 | - | 3 | - | 3 | - | ns |
| | | $V_{CC} = 6.0$ V | 3 | -2 | - | 3 | - | 3 | - | ns |
| f_{max} | maximum frequency | CP input; see Figure 7 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 6 | 20.6 | - | 4.8 | - | 4 | - | MHz |
| | | $V_{CC} = 4.5$ V | 30 | 103 | - | 24 | - | 20 | - | MHz |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 66 | - | - | - | - | - | MHz |
| | | $V_{CC} = 6.0$ V | 35 | 122 | - | 28 | - | 24 | - | MHz |
| C_{PD} | power dissipation capacitance | per package; $V_I = \text{GND to } V_{CC}$ ^[3] | - | 20 | - | - | - | - | - | pF |

Table 7. Dynamic characteristics ...continuedGND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 10](#)

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|-----------------|-------------------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HCT273 | | | | | | | | | | |
| t_{pd} | propagation delay | CP to Qn; see Figure 7 [1] | | | | | | | | |
| | | $V_{CC} = 4.5$ V | - | 16 | 30 | - | 38 | - | 45 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 15 | - | - | - | - | - | ns |
| t_{PHL} | HIGH to LOW propagation delay | \overline{MR} to Qn; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 4.5$ V | - | 23 | 34 | - | 43 | - | 51 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 20 | - | - | - | - | - | ns |
| t_t | transition time | Qn output; see Figure 7 [2] | | | | | | | | |
| | | $V_{CC} = 4.5$ V | - | 7 | 15 | - | 19 | - | 22 | ns |
| t_{w} | pulse width | CP input; see Figure 7 | | | | | | | | |
| | | $V_{CC} = 4.5$ V | 16 | 9 | - | 20 | - | 24 | - | ns |
| | | \overline{MR} input LOW; see Figure 8 | | | | | | | | |
| t_{rec} | recovery time | \overline{MR} to CP; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 4.5$ V | 10 | -2 | - | 13 | - | 15 | - | ns |
| t_{su} | set-up time | Dn to CP; see Figure 9 | | | | | | | | |
| | | $V_{CC} = 4.5$ V | 12 | 5 | - | 15 | - | 18 | - | ns |
| t_h | hold time | Dn to CP; see Figure 9 | | | | | | | | |
| | | $V_{CC} = 4.5$ V | 3 | -4 | - | 3 | - | 3 | - | ns |
| f_{max} | maximum frequency | CP input; see Figure 7 | | | | | | | | |
| | | $V_{CC} = 4.5$ V | 30 | 56 | - | 24 | - | 20 | - | MHz |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 36 | - | - | - | - | - | MHz |
| C_{PD} | power dissipation capacitance | per package; $V_I = GND$ to $V_{CC} - 1.5$ V [3] | - | 23 | - | - | - | - | - | pF |

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .[2] t_t is the same as t_{THL} and t_{TLH} .[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

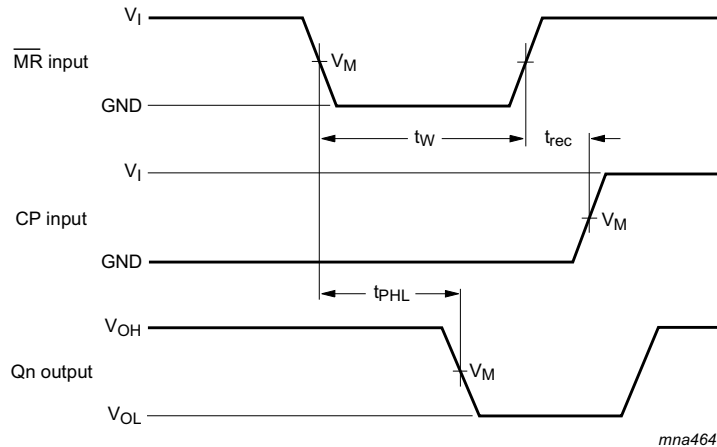
 f_i = input frequency in MHz; f_o = output frequency in MHz; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs; C_L = output load capacitance in pF; V_{CC} = supply voltage in V.

11. Waveforms



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Propagation delay clock input (CP) to output (Qn), clock (CP) pulse width, output transition time and the maximum clock pulse frequency



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Propagation delay master reset (MR) to output (Qn), pulse width master reset (MR) and recovery time master reset (MR) to clock (CP)



Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Data set-up and hold times data input (Dn)

Table 8. Measurement points

| Type | Input | | Output |
|----------|----------|-------------|-------------|
| | V_I | V_M | V_M |
| 74HC273 | V_{CC} | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT273 | 3 V | 1.3 V | 1.3 V |



Table 9. Test data

| Type | Input | | Load | | S1 position |
|----------|----------|------------|--------------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} |
| 74HC273 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | open |
| 74HCT273 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | open |

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Fig 11. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



Fig 12. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig 13. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Fig 14. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------------|---|-----------------------|---------------|---------------------|
| 74HC_HCT273 v.5 | 20160226 | Product data sheet | - | 74HC_HCT273 v.4 |
| Modifications: | <ul style="list-style-type: none"> Type numbers 74HC273N and 74HCT273N (SOT146-1) removed. | | | |
| 74HC_HCT273 v.4 | 20130610 | Product data sheet | - | 74HC_HCT273 v.3 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. | | | |
| 74HC_HCT273 v.3 | 20060124 | Product data sheet | - | 74HC_HCT273_CNV v.2 |
| 74HC_HCT273_CNV v.2 | 19970827 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

15.2 Definitions

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16. Contact information

For more information, please visit: <http://www.nexperia.com>

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