

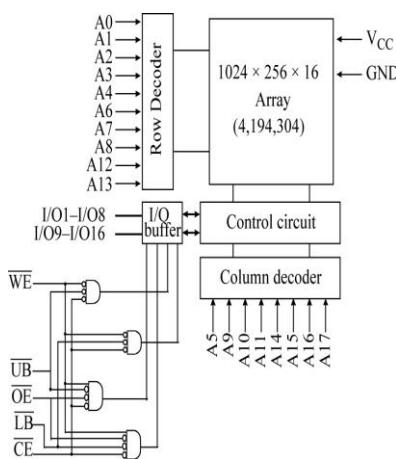


3.3 V 256 K × 16 CMOS SRAM

Features

- Pin compatible with AS7C34098
- Industrial and commercial temperature
- Organization: 262,144 words × 16 bits
- Center power and ground pins
- High speed
 - 10/12/15/20 ns address access time
 - 4/5/6/7 ns output enable access time
- Low power consumption: ACTIVE
 - 650 mW /max @ 10 ns
- Low power consumption: STANDBY
 - 28.8 mW /max CMOS
- Individual byte read/write controls
- Easy memory expansion with \overline{CE} , \overline{OE} inputs
- TTL- and CMOS-compatible, three-state I/O
- JEDEC standard packages
 - 44-pin SOJ -400-mil
 - 44-pin TSOP 2
 - 48-pin Mini BGA
- ESD protection \geq 2000 volts
- Latch-up current \geq 200 mA

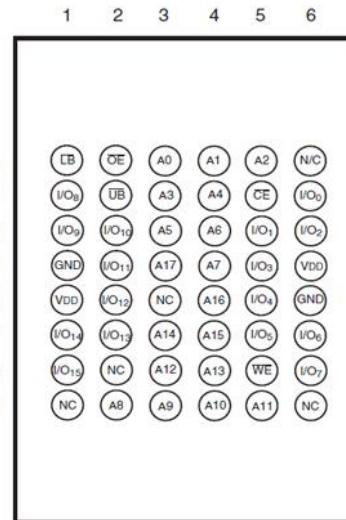
Logic block diagram



Pin arrangement for SOJ and TSOP 2

44-pin (400 mil) SOJ TSOP2							
A0	1	44	A17	A0	A16	A1	N/C
A1	2	43	A16	A1	A15	A2	N/C
A2	3	42	A15	A2	I/O ₁	A3	I/O ₂
A3	4	41	OE	A3	I/O ₃	A4	I/O ₄
A4	5	40	UB	A4	GND	A5	VDD
CE	6	39	LB	CE	V _{CC}	A6	N/C
I/O ₁	7	38	I/O ₁₆	I/O ₁	GND	A7	I/O ₅
I/O ₂	8	37	I/O ₁₅	I/O ₂	VDD	A8	I/O ₆
I/O ₃	9	36	I/O ₁₄	I/O ₃	I/O ₁₂	A9	N/C
I/O ₄	10	35	I/O ₁₃	I/O ₄	NC	A10	A16
V _{CC}	11	34	GND	V _{CC}	A11	A17	GND
GND	12	33	V _{CC}	GND	A12	I/O ₁	I/O ₇
I/O ₅	13	32	I/O ₁₂	I/O ₅	I/O ₁₃	A13	I/O ₈
I/O ₆	14	31	I/O ₁₁	I/O ₆	WE	A14	N/C
I/O ₇	15	30	I/O ₁₀	I/O ₇	NC	A15	A10
I/O ₈	16	29	I/O ₉	I/O ₈	A16	A11	A11
WE	17	28	NC	WE	A17	A12	NC
A5	18	27	A14	A5	A18	A13	A13
A6	19	26	A13	A6	A19	A12	A12
A7	20	25	A12	A7	A20	A11	A11
A8	21	24	A11	A8	A21	A10	A10
A9	22	23	A10	A9	A22	A11	A11

Bottom View 48BGA



Selection guide

		-10	-12	-15	-20	Unit
Maximum address access time		10	12	15	20	ns
Maximum output enable access time		4	5	6	7	ns
Maximum operating current	Industrial	180	160	140	110	mA
	Commercial	170	150	130	100	mA
Maximum CMOS standby current		8	8	8	8	mA



Functional description

The AS7C34098A is a high-performance CMOS 4,194,304-bit Static Random Access Memory (SRAM) device organized as 262,144 words \times 16 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 4/5/6/7 ns are ideal for high-performance applications. The chip enable input \overline{CE} permits easy memory expansion with multiple-bank memory systems.

When \overline{CE} is high the device enters standby mode. The device is guaranteed not to exceed 28.8mW power consumption in CMOS standby mode. A write cycle is accomplished by asserting write enable (\overline{WE}) and chip enable (\overline{CE}). Data on the input pins I/O1–I/O16 is written on the rising edge of \overline{WE} (write cycle 1) or \overline{CE} (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable (\overline{OE}) or write enable (\overline{WE}).

A read cycle is accomplished by asserting output enable (\overline{OE}) and chip enable (\overline{CE}), with write enable (\overline{WE}) high. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

The device provides multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. \overline{LB} controls the lower bits, I/O1–I/O8, and \overline{UB} controls the higher bits, I/O9–I/O16.

All chip inputs and outputs are TTL- and CMOS-compatible, and operation is for 3.3V (AS7C34098A) supply. The device is available in the JEDEC standard 400-mil, 44-pin SOJ, TSOP 2.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	V_{t1}	-0.50	+5.0	V
Voltage on any pin relative to GND	V_{t2}	-0.50	$V_{CC} + 0.50$	V
Power dissipation	P_D	—	1.5	W
Storage temperature (plastic)	T_{stg}	-65	+150	°C
Ambient temperature with V_{CC} applied	T_{bias}	-55	+125	°C
DC current into outputs (low)	I_{OUT}	—	± 20	mA

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

CE	WE	OE	LB	UB	I/O1–I/O8	I/O9–I/O16	Mode
H	X	X	X	X	High Z	High Z	Standby (I_{SB} , I_{SB1})
L	H	H	X	X	High Z	High Z	Output disable (I_{CC})
L	X	X	H	H			
L	H	L	L	H	D_{OUT}	High Z	
			H	L	High Z	D_{OUT}	
			L	L	D_{OUT}	D_{OUT}	
L	L	X	L	H	D_{IN}	High Z	Read (I_{CC})
			H	L	High Z	D_{IN}	
			L	L	D_{IN}	D_{IN}	
Key: X = Don't care, L = Low, H = High.							



Recommended operating conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage	V _{CC} (10/12/15/20)	3.0	3.3	3.6	V
Input voltage	V _{IH} ^{**}	2.0	—	V _{CC} + 0.5	V
	V _{IL} [*]	-0.5	—	0.8	V
Ambient operating temperature	commercial	T _A	0	—	70 °C
	industrial	T _A	-40	—	85 °C

* V_{IL} min = -1.0V for pulse width less than 5ns.

** V_{IH} max = V_{CC} + 2.0V for pulse width less than 5ns.

DC operating characteristics (over the operating range)¹

Parameter	Symbol	Test conditions	-10		-12		-15		-20		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	I _{LI}	V _{CC} = Max V _{IN} = GND to V _{CC}	—	1	—	1	—	1	—	1	μA
Output leakage current	I _{LO}	V _{CC} = Max CE = V _{IH} or OE = V _{IH} or WE = V _{IL} V _{I/O} = GND to V _{CC}	—	1	—	1	—	1	—	1	μA
Operating power supply current	I _{CC}	V _{CC} = Max	Industrial	—	180	—	160	—	140	—	110 mA
		CE ≤ V _{IL} , f = f _{max} I _{OUT} = 0mA	Commercial	-	170	-	150	-	130	-	100 mA
Standby power supply current	I _{SB}	V _{CC} = Max CE ≥ V _{IH} , f = Max	—	60	—	60	—	60	—	60	mA
	I _{SB1}	V _{CC} = Max CE ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0	—	8	—	8	—	8	—	8	mA
Output voltage	V _{OL}	I _{OL} = 8 mA, V _{CC} = Min	—	0.4	—	0.4	—	0.4	—	0.4	V
	V _{OH}	I _{OH} = -4 mA, V _{CC} = Min	2.4	—	2.4	—	2.4	—	2.4	—	V

Capacitance (f = 1MHz, T_a = 25° C, V_{CC} = NOMINAL)²

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C _{IN}	A, CE, WE, OE, UB, LB	V _{IN} = 0V	6	pF
I/O capacitance	C _{I/O}	I/O	V _{IN} = V _{OUT} = 0V	8	pF



Read cycle (over the operating range)^{3,9}

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	10	—	12	—	15	—	20	—	ns	
Address access time	t_{AA}	—	10	—	12	—	15	—	20	ns	
Chip enable (\bar{CE}) access time	t_{ACE}	—	10	—	12	—	15	—	20	ns	
Output enable (\bar{OE}) access time	t_{OE}	—	4	—	5	—	6	—	7	ns	
Output hold from address change	t_{OH}	3	—	3	—	3	—	3	—	ns	5
\bar{CE} Low to output in low Z	t_{CLZ}	3	—	3	—	3	—	3	—	ns	4, 5
\bar{CE} High to output in high Z	t_{CHZ}	—	5	—	6	—	7	—	9	ns	4, 5
\bar{OE} Low to output in low Z	t_{OLZ}	0	—	0	—	0	—	0	—	ns	4, 5
\bar{OE} High to output in high Z	t_{OHZ}	—	5	—	6	—	7	—	9	ns	4, 5
\bar{LB} , \bar{UB} access time	t_{BA}	—	5	—	6	—	7	—	8	ns	
\bar{LB} , \bar{UB} Low to output in low Z	t_{BLZ}	0	—	0	—	0	—	0	—	ns	
\bar{LB} , \bar{UB} High to output in high Z	t_{BHZ}	—	5	—	6	—	7	—	9	ns	
Power up time	t_{PU}	0	—	0	—	0	—	0	—	ns	5
Power down time	t_{PD}	—	10	—	12	—	15	—	20	ns	5

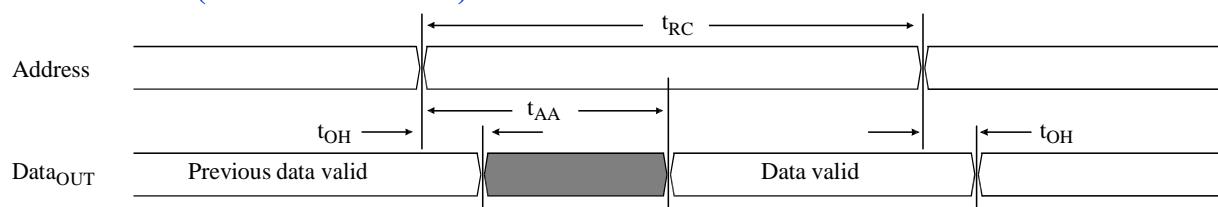
Key to switching waveforms

Rising input

Falling input

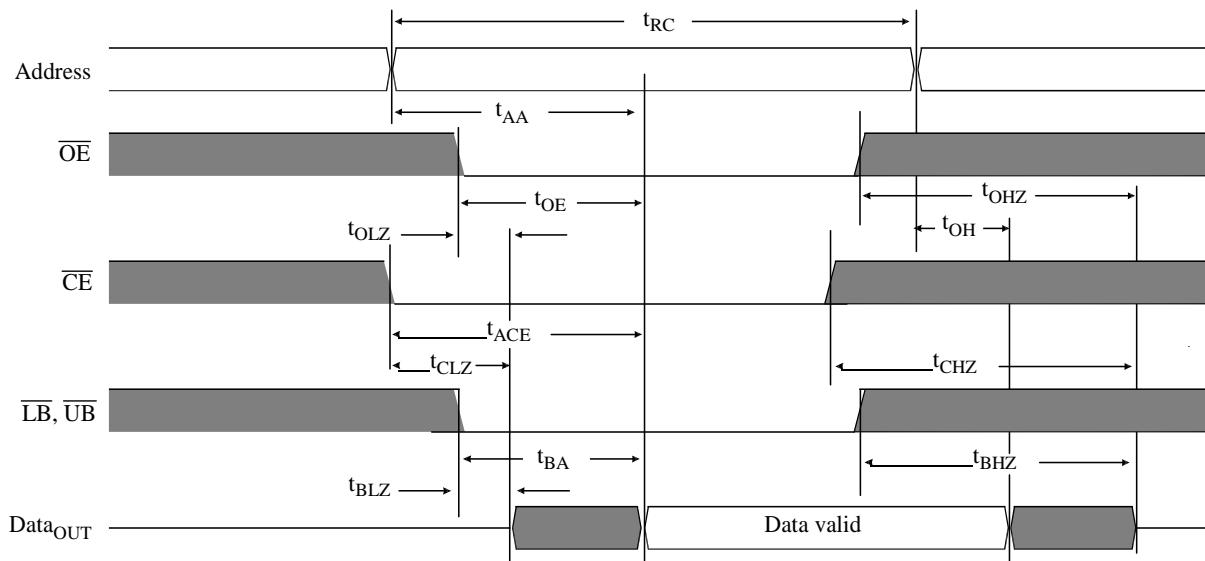
Undefined/don't care

Read waveform 1 (address controlled)^{6,7,9}





Read waveform 2 ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{UB}}$, $\overline{\text{LB}}$ controlled)^{6,8,9}

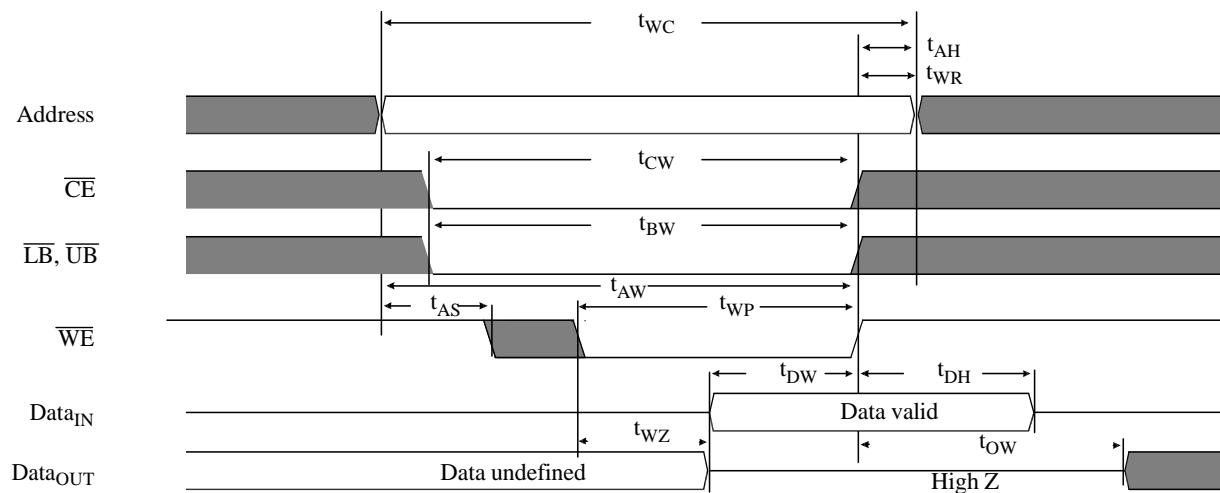


Write cycle (over the operating range)¹⁰

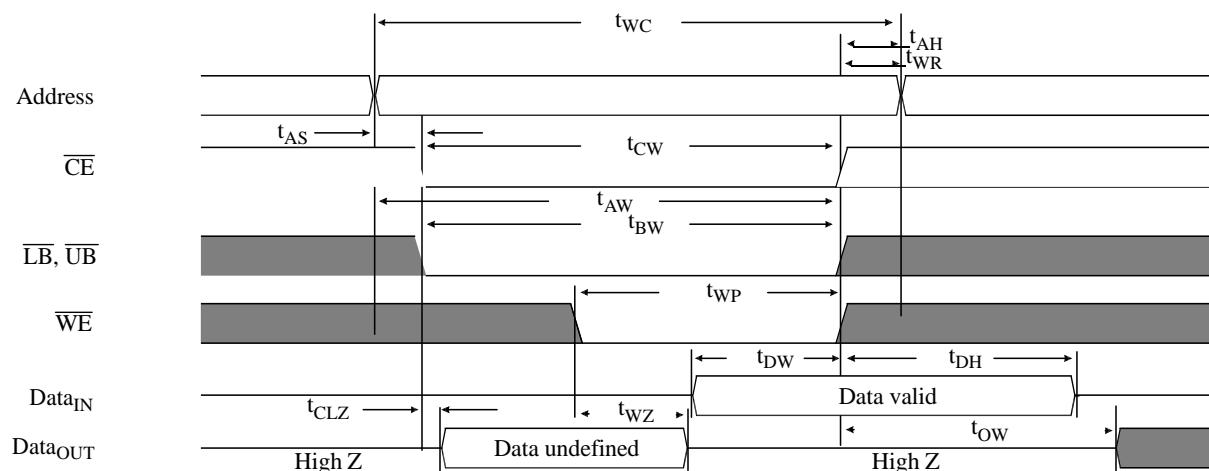
Parameter	Symbol	-10		-12		-15		-20		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	10	–	12	–	15	–	20	–	ns	
Chip enable ($\overline{\text{CE}}$) to write end	t_{CW}	7	–	8	–	10	–	12	–	ns	
Address setup to write end	t_{AW}	7	–	8	–	10	–	12	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	
Write pulse width ($\overline{\text{OE}} = \text{High}$)	t_{WP1}	7	–	8	–	10	–	12	–	ns	
Write pulse width ($\overline{\text{OE}} = \text{Low}$)	t_{WP2}	10	–	12	–	15	–	20	–	ns	
Write recovery time	t_{WR}	0	–	0	–	0	–	0	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	5	–	6	–	7	–	9	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	4, 5
Write enable to output in High-Z	t_{WZ}	0	5	0	6	0	7	0	9	ns	4, 5
Output active from write end	t_{OW}	3	–	3	–	3	–	3	–	ns	4, 5
Byte enable Low to write end	t_{BW}	7	–	8	–	10	–	12	–	ns	4, 5



Write waveform 1(\overline{WE} controlled)¹⁰

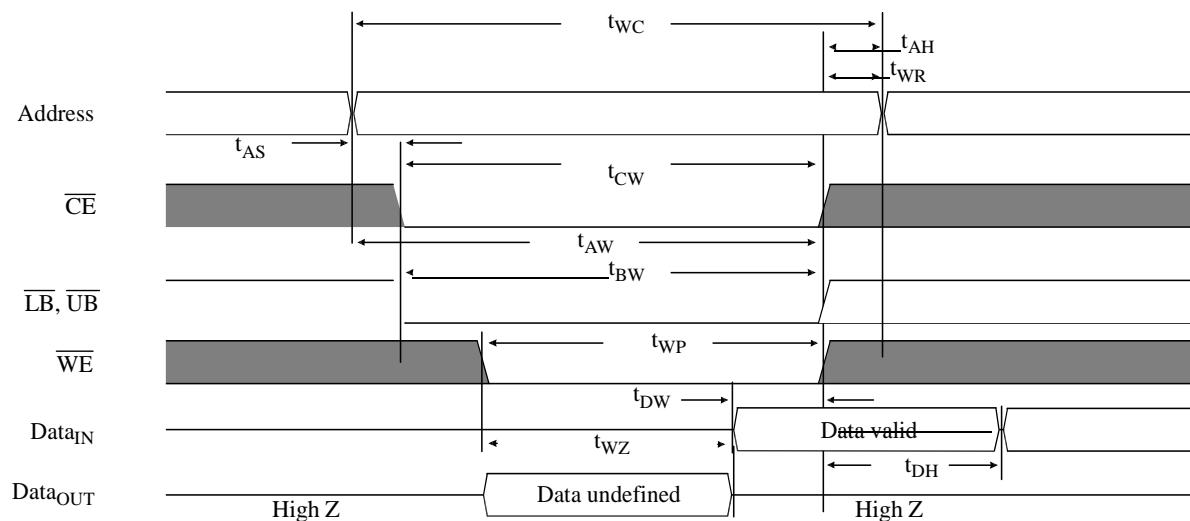


Write waveform 2 (\overline{CE} controlled)¹⁰





Write waveform 3¹⁰



AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

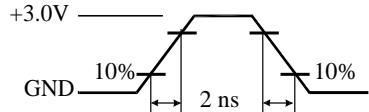


Figure A: Input pulse

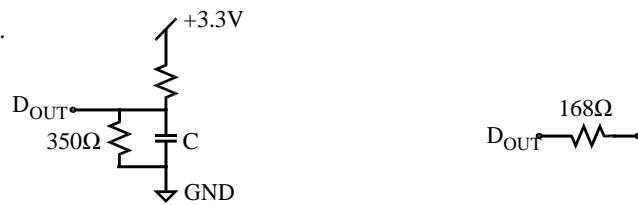


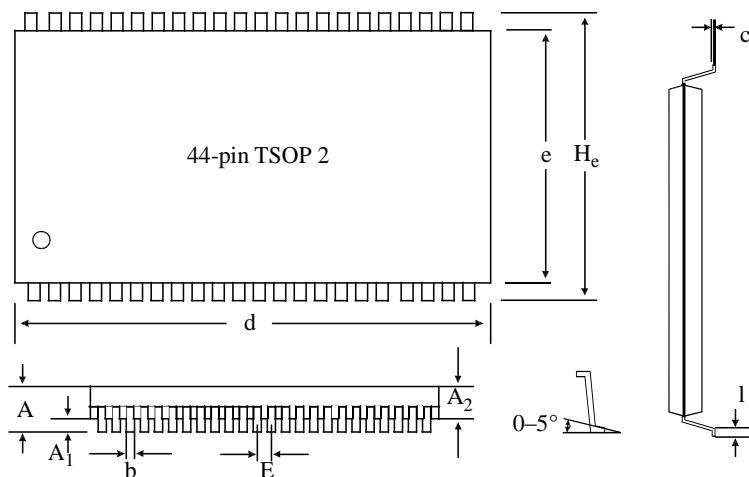
Figure B: 3.3V Output load

Notes

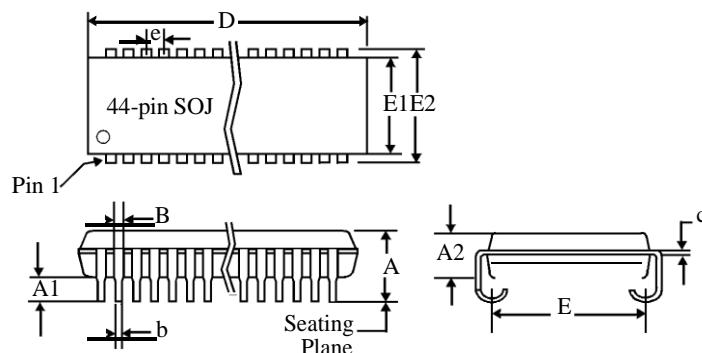
- 1 During V_{CC} power-up, a pull-up resistor to V_{CC} on \overline{CE} is required to meet I_{SB} specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see *AC Test Conditions*, Figures A and B.
- 4 t_{CLZ} and t_{CHZ} are specified with $C_L = 5\text{pF}$ as in Figure B. Transition is measured $\pm 500\text{mV}$ from steady-state voltage.
- 5 This parameter is guaranteed, but not tested.
- 6 WE is High for read cycle.
- 7 CE and OE are Low for read cycle.
- 8 Address valid prior to or coincident with CE transition Low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 11 C=30pF, except on High Z and Low Z parameters, where C=5pF.



Package dimensions



	44-pin TSOP 2	
	Min (mm)	Max (mm)
A		1.2
A₁	0.05	0.15
A₂	0.95	1.05
b	0.3	0.45
c	0.12	0.21
d	18.31	18.52
e	10.06	10.26
H_e	11.68	11.94
E	0.80 (typical)	
l	0.40	0.60

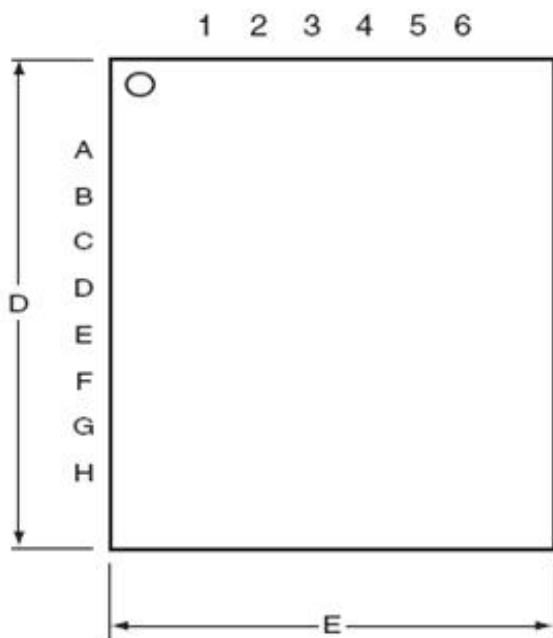


	44-pin SOJ 400 mils	
	Min(mils)	Max(mils)
A	0.128	0.148
A1	0.025	-
A2	0.105	0.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.120	1.130
E	0.370 NOM	
E1	0.395	0.405
E2	0.435	0.445
e	0.050 NOM	

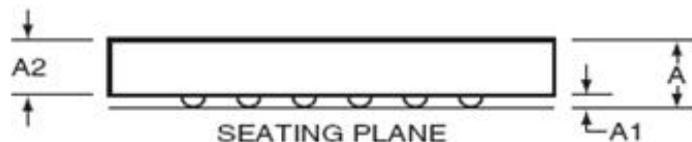
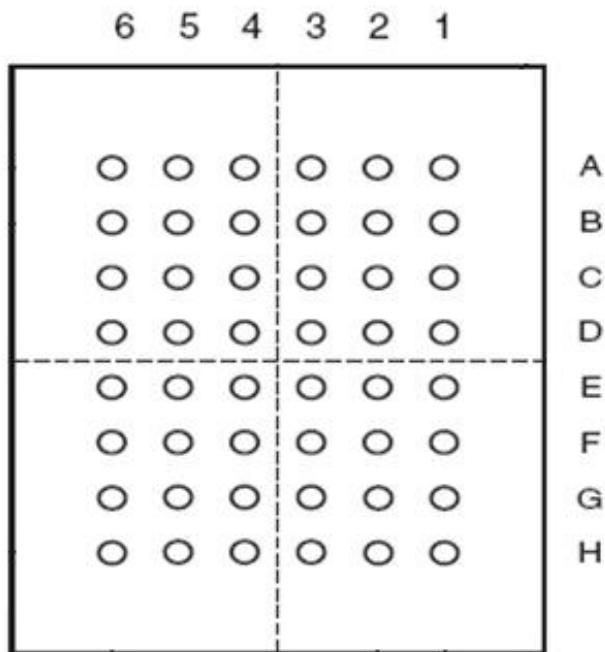


Outline of 48BGA

Top View



Bottom View



Notes:

1. Controlling dimensions are in millimeters.

BGA 8mm x 10mm

MILLIMETERS

Sym.	Min.	Typ.	Max.
A	—	—	1.20
A1	0.24	—	0.30
A2	0.60	—	—
D	9.90	10.00	10.10
D1	5.25 BSC		
E	7.90	8.00	8.10
E1	3.75 BSC		
e	0.75 BSC		
b	0.30	0.35	0.40



Ordering Codes

Package	Temperature	10 ns	12	15 ns	20 ns
SOJ	Commercial	AS7C34098A-10JC	AS7C34098A-12JC	AS7C34098A-15JC	AS7C34098A-20JC
	Industrial	AS7C34098A-10JI	AS7C34098A-12JI	AS7C34098A-15JI	AS7C34098A-20JI
BGA	Industrial	AS7C34098A-10BIN			
TSOP 2	Commercial	AS7C34098A-10TC	AS7C34098A-12TC	AS7C34098A-15TC	AS7C34098A-20TC
	Industrial	AS7C34098A-10TI	AS7C34098A-12TI	AS7C34098A-15TI	AS7C34098A-20TI

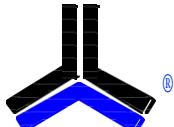
Note: Add suffix 'N' to the above part numbers for Lead Free Parts. (Ex: AS7C34098A - 10TCN)

Part numbering system

AS7C	X	4098A	-XX	J / T or B	X	X
SRAM prefix	Voltage: 3 - 3.3V CMOS	Device number	Access time	Packages: J: SOJ 400 mil T: TSOP 2 B: BGA	Temperature ranges: C: Commercial, 0°C to 70°C I: Industrial, -40°C to 85°C	N = Lead Free Parts



AS7C34098A



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- Поставка более 17-ти миллионов наименований электронных компонентов;
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- Подбор аналогов;
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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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