2200 MHz to 2700 MHz, Dual-Balanced Mixer, LO Buffer, IF Amplifier, and RF Balun

ADL5354

FEATURES

RF frequency range of 2200 MHz to 2700 MHz
IF frequency range of 30 MHz to 450 MHz
Power conversion gain: 8.6 dB
SSB noise figure of 10.6 dB
Input IP3 of 26.1 dBm
Input P1dB of 10.6 dBm
Typical LO power of 0 dBm
Single-ended, 50 Ω RF and LO input ports
High isolation SPDT LO input switch
Single-supply operation: 3.3 V to 5 V
Exposed paddle, 6 mm × 6 mm, 36-lead LFCSP
1500 V HBM/500 V FICDM ESD performance

APPLICATIONS

Cellular base station receivers
Transmit observation receivers
Radio link downconverters

FUNCTIONAL BLOCK DIAGRAM

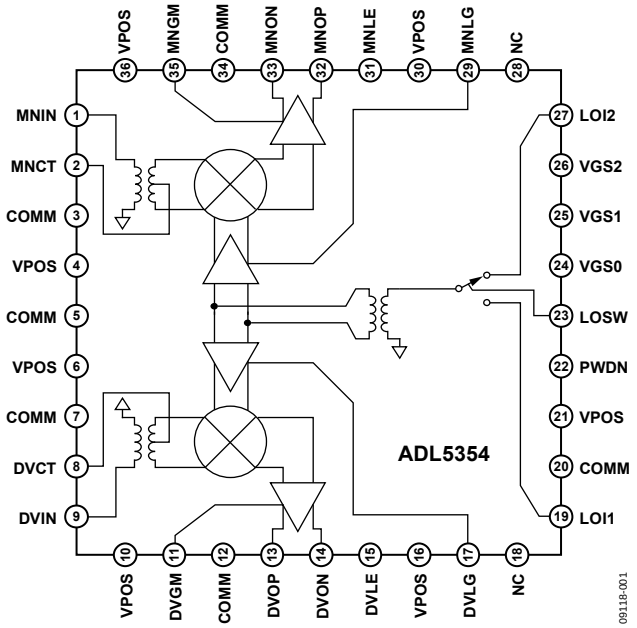


Figure 1.

GENERAL DESCRIPTION

The ADL5354 uses a highly linear, doubly balanced, passive mixer core along with integrated RF and local oscillator (LO) balancing circuitry to allow single-ended operation. The ADL5354 incorporates the RF baluns, allowing for optimal performance over a 2200 MHz to 2700 MHz RF input frequency range. The balanced passive mixer arrangement provides good LO-to-RF leakage, typically better than −37 dBm, and excellent intermodulation performance. The balanced mixer core also provides extremely high input linearity, allowing the device to be used in demanding cellular applications where in-band blocking signals may otherwise result in the degradation of dynamic performance. A high linearity IF buffer amplifier follows the passive mixer core to yield a typical power conversion gain of 8 dB and can be used with a wide range of output impedances.

The ADL5354 provides two switched LO paths that can be used in time division duplex (TDD) applications where it is desirable to ping-pong between two local oscillators. LO current can be externally set using a resistor to minimize dc current commensurate with the desired level of performance. For low voltage applications, the ADL5354 is capable of operation at voltages as low as 3.3 V with substantially reduced current. For low voltage operation, an additional logic pin is provided to power down (~300 µA) the circuit when desired.

The ADL5354 is fabricated using a BiCMOS high performance IC process. The device is available in a 6 mm × 6 mm, 36-lead LFCSP and operates over a −40°C to +85°C temperature range. An evaluation board is also available.

Table 1. Passive Mixers

RF Frequency (MHz)	Single Mixer	Single Mixer and IF Amp	Dual Mixer and IF Amp
500 to 1700	ADL5367	ADL5357	ADL5358
1200 to 2500	ADL5365	ADL5355	ADL5356
2200 to 2700		ADL5353	ADL5354

Rev. 0
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REVISION HISTORY

2/11—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, I_S = 350 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2332 MHz, LO power = 0 dBm, RF power = −10 dBm, R1 = R4 = 1.3 kΩ, R2 = R5 = 1 kΩ, Z_O = 50 Ω, VGS0 = VGS1 = VGS2 = 0 V, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20 dB over a limited bandwidth		20		dB
Input Impedance			50		Ω
RF Frequency Range		2200		2700	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		230||0.75		Ω||pF
IF Frequency Range		30		450	MHz
DC Bias Voltage[1]	Externally generated	3.3	5.0	5.5	V
LO INTERFACE					
LO Power		−6	0	+10	dBm
Return Loss			13		dB
Input Impedance			50		Ω
LO Frequency Range		1750		2670	MHz
POWER-DOWN (PWDN) INTERFACE[2]					
PWDN Threshold			1.0		V
Logic 0 Level				0.4	V
Logic 1 Level		1.4			V
PWDN Response Time	Device enabled, IF output to 90% of its final level		160		ns
	Device disabled, supply current < 5 mA		230		ns
PWDN Input Bias Current	Device enabled		0		µA
	Device disabled		70		µA

[1] Apply supply voltage from external circuit through choke inductors.
[2] PWDN function is intended for use with $V_S \leq 3.6$ V only.

5 V PERFORMANCE

V_S = 5 V, I_S = 350 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2332 MHz, LO power = 0 dBm, RF power = −10 dBm, R1 = R4 = 1.3 kΩ, R2 = R5 = 1 kΩ, VGS0 = VGS1 = VGS2 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Power Conversion Gain	Including 4:1 IF port transformer and PCB loss		8.6		dB
Voltage Conversion Gain	Z_{SOURCE} = 50 Ω, differential Z_{LOAD} = 200 Ω differential		14.6		dB
SSB Noise Figure			10.6		dB
Input Third-Order Intercept (IIP3)	f_{RF1} = 2534.5 MHz, f_{RF2} = 2535.5 MHz, f_{LO} = 2332 MHz, each RF tone at −10 dBm		26.1		dBm
Input Second-Order Intercept (IIP2)	f_{RF1} = 2535 MHz, f_{RF2} = 2585 MHz, f_{LO} = 2332 MHz, each RF tone at −10 dBm		50		dBm
Input 1 dB Compression Point (IP1dB)			10.6		dBm
LO-to-IF Leakage	Unfiltered IF output		−20.7		dBm
LO-to-RF Leakage			−37		dBm
RF-to-IF Isolation			−34		dBc
IF/2 Spurious	−10 dBm input power		−73		dBc
IF/3 Spurious	−10 dBm input power		−71		dBc
IF Channel-to-Channel Isolation			52		dB
POWER SUPPLY					
Positive Supply Voltage		4.75	5	5.25	V
Quiescent Current	LO supply		170		mA
	IF supply		180		mA
Total Quiescent Current	V_S = 5 V		350		mA

3.3 V PERFORMANCE

V_S = 3.3 V, I_S = 200 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2332 MHz, LO power = 0 dBm, R9 = 226 Ω, R14 = 604 Ω, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Power Conversion Gain	Including 4:1 IF port transformer and PCB loss		8		dB
Voltage Conversion Gain	Z_{SOURCE} = 50 Ω, differential Z_{LOAD} = 200 Ω differential		14		dB
SSB Noise Figure			9.9		dB
Input Third-Order Intercept (IIP3)	f_{RF1} = 2534.5 MHz, f_{RF2} = 2535.5 MHz, f_{LO} = 2332 MHz, each RF tone at −10 dBm		17.5		dBm
Input Second-Order Intercept (IIP2)	f_{RF1} = 2535 MHz, f_{RF2} = 2585 MHz, f_{LO} = 2332 MHz, each RF tone at −10 dBm		49		dBm
Input 1 dB Compression Point (IP1dB)			7		dBm
POWER INTERFACE					
Supply Voltage		3.0	3.3	3.6	V
Quiescent Current	Resistor programmable		200		mA
Power-Down Current	Device disabled		300		µA

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage, V_S	5.5 V
RF Input Level	20 dBm
LO Input Level	13 dBm
MNOP, MNON, DVOP, DVON Bias	6.0 V
VGS2,VGS1,VGS0, LOSW, PWDN	5.5 V
Internal Power Dissipation	2.2 W
Thermal Characteristic θ_{JA}	22°C/W
Maximum Junction Temperature	150°C
Temperature Range	
Operating	−40°C to +85°C
Storage	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

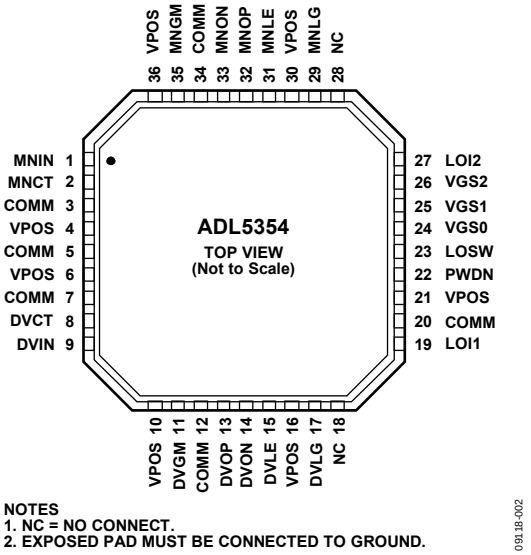


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	MNIN	RF Input for Main Channel. Internally matched to 50 Ω. Must be ac-coupled.
2	MNCT	Center Tap for Main Channel Input Balun. Bypass to ground using low inductance capacitor.
3, 5, 7, 12, 20, 34	COMM	Device Common (DC Ground).
4, 6, 10, 16, 21, 30, 36	VPOS	Positive Supply Voltage.
8	DVCT	Center Tap for Diversity Channel Input Balun. Bypass to ground using low inductance capacitor.
9	DVIN	RF Input for Diversity Channel. Internally matched to 50 Ω. Must be ac-coupled.
11	DVGM	Diversity Amplifier Bias Setting. Connect a 1.3 kΩ resistor to ground for typical operation.
13, 14	DVOP, DVON	Diversity Channel Differential Open-Collector Outputs. DVOP and DVON should be pulled up to VCC using external inductors, see Figure 53 for details.
15	DVLE	Diversity Channel IF Return. This pin must be grounded.
17	DVLG	Diversity Channel LO Buffer Bias Setting. Connect a 1 kΩ resistor to ground for typical operation.
18, 28	NC	No Connect. Do not connect to this pin.
19	LOI1	Local Oscillator Input 1. Internally matched to 50 Ω. Must be ac-coupled.
22	PWDN	Power Down. Connect this pin to ground for normal operation. Connect pin to 3 V for disable mode when using VPOS ≤ 3.6 V. PWDN pin must be grounded when VPOS > 3.6 V.
23	LOSW	Local Oscillator Input Selection Switch. Set LOSW high to select LOI1 or set LOSW low to select LOI2.
24, 25, 26	VGS0, VGS1, VGS2	Gate to Source Control Voltages. For typical operation, set VGS0, VGS1, and VGS2 to a low logic level.
27	LOI2	Local Oscillator Input 2. Internally matched to 50 Ω. Must be ac-coupled.
29	MNLG	Main Channel LO Buffer Bias Setting. Connect a 1 kΩ resistor to ground for typical operation.
31	MNLE	Main Channel IF Return. This pin must be grounded.
32, 33	MNOP, MNON	Main Channel Differential Open-Collector Outputs. Pull up MNOP and MNON to VCC by using external inductors, see Figure 53 for details.
35	MNGM	Main Amplifier Bias Setting. Connect a 1.3 kΩ resistor to ground for typical operation.
	EPAD	Exposed Paddle. Exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

5 V PERFORMANCE

V_S = 5 V, I_S = 350 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2332 MHz, LO power = 0 dBm, RF power = −10 dBm, R1 = R4 = 1.3 kΩ, R2 = R5 = 1 kΩ, Z_O = 50 Ω, VGS0 = VGS1 = VGS2 = 0 V, unless otherwise noted.

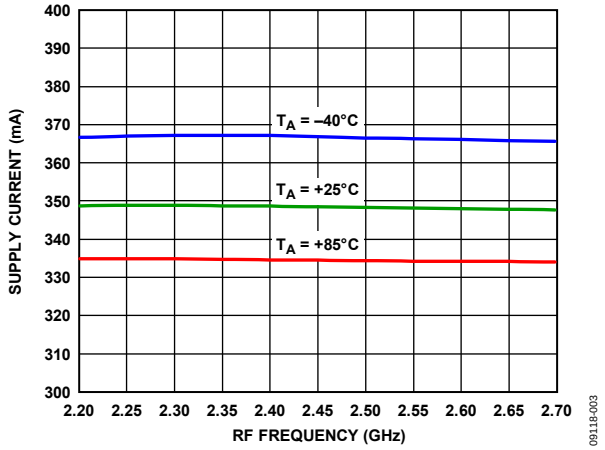


Figure 3. Supply Current vs. RF Frequency

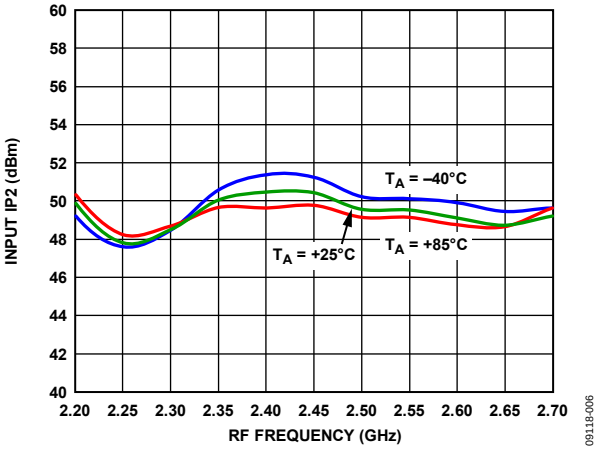


Figure 6. Input IP2 vs. RF Frequency

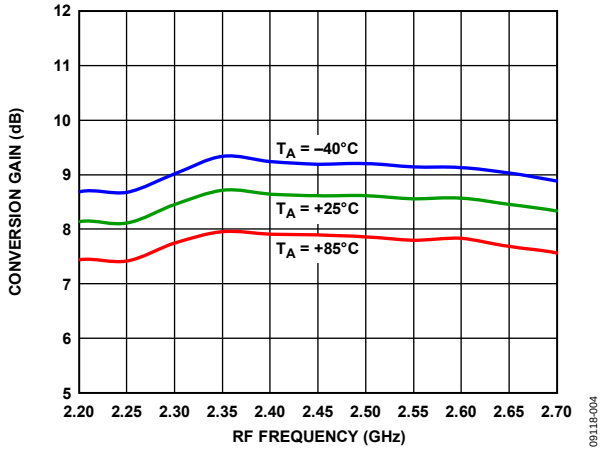


Figure 4. Power Conversion Gain vs. RF Frequency

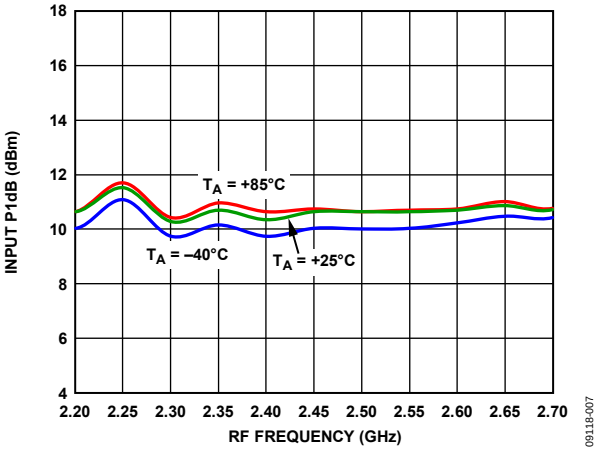


Figure 7. Input P1dB vs. RF Frequency

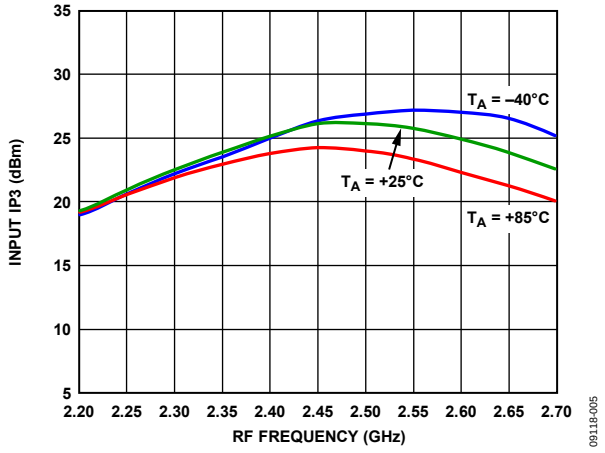


Figure 5. Input IP3 vs. RF Frequency

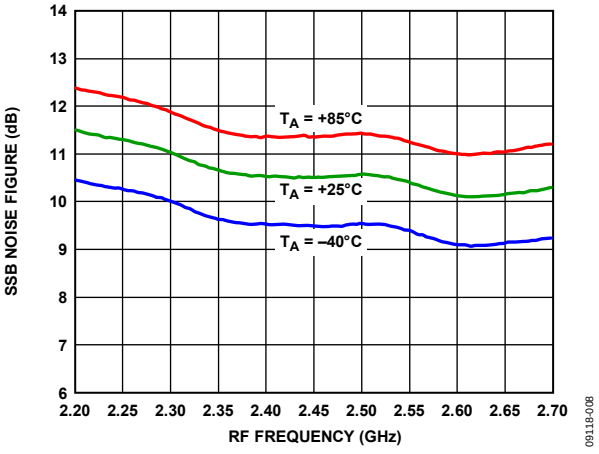


Figure 8. SSB Noise Figure vs. RF Frequency

V_S = 5 V, I_S = 350 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2332 MHz, LO power = 0 dBm, RF power = −10 dBm, R1 = R4 = 1.3 kΩ, R2 = R5 = 1 kΩ, Z_O = 50 Ω, VGS0 = VGS1 = VGS2 = 0 V, unless otherwise noted.

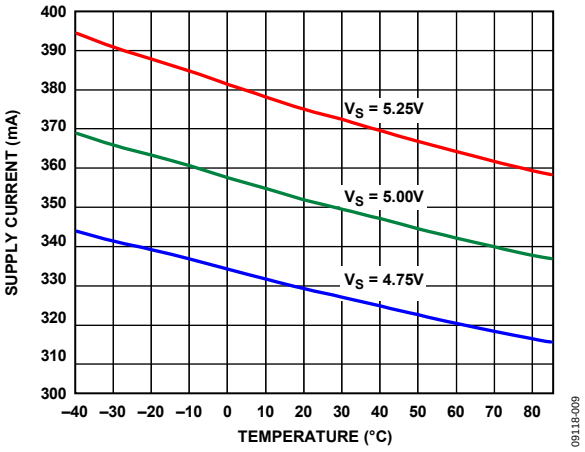


Figure 9. Supply Current vs. Temperature

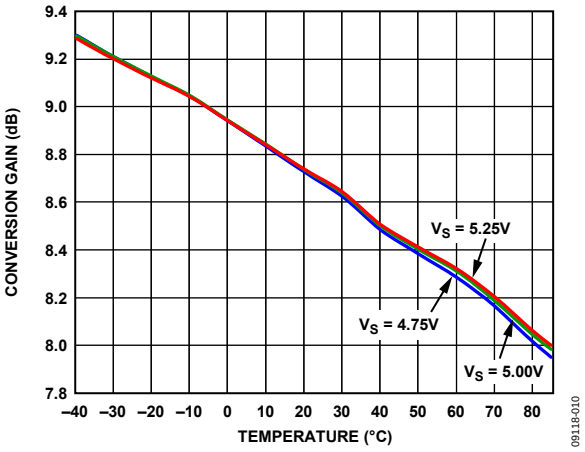


Figure 10. Power Conversion Gain vs. Temperature

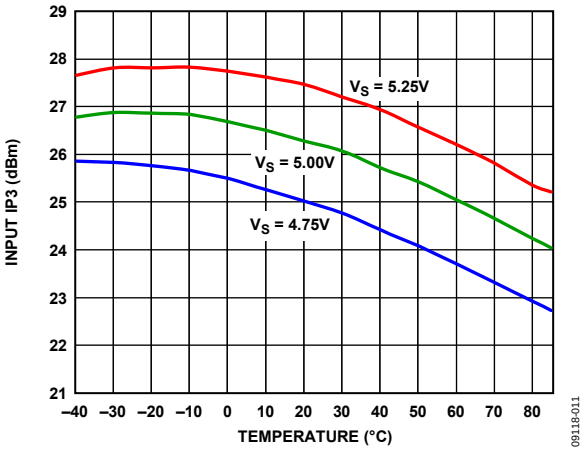


Figure 11. Input IP3 vs. Temperature

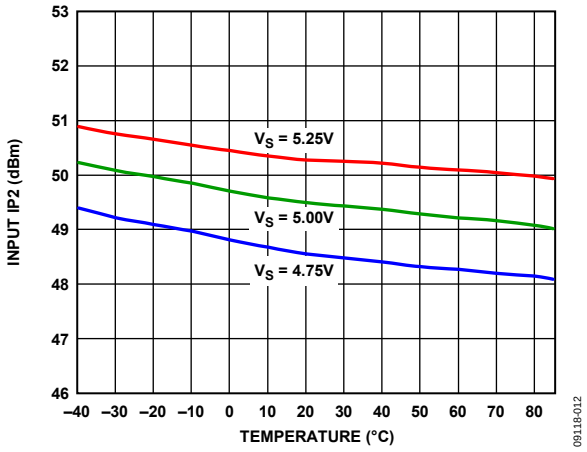


Figure 12. Input IP2 vs. Temperature

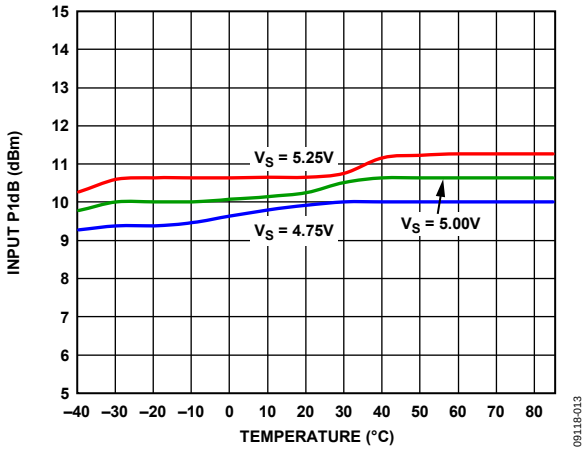


Figure 13. Input P1dB vs. Temperature

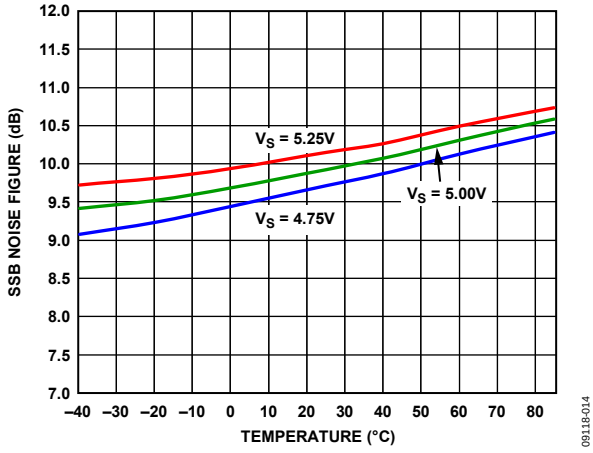


Figure 14. SSB Noise Figure vs. Temperature

V_S = 5 V, I_S = 350 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2332 MHz, LO power = 0 dBm, RF power = −10 dBm, R1 = R4 = 1.3 kΩ, R2 = R5 = 1 kΩ, Z_O = 50 Ω, VGS0 = VGS1 = VGS2 = 0 V, unless otherwise noted.

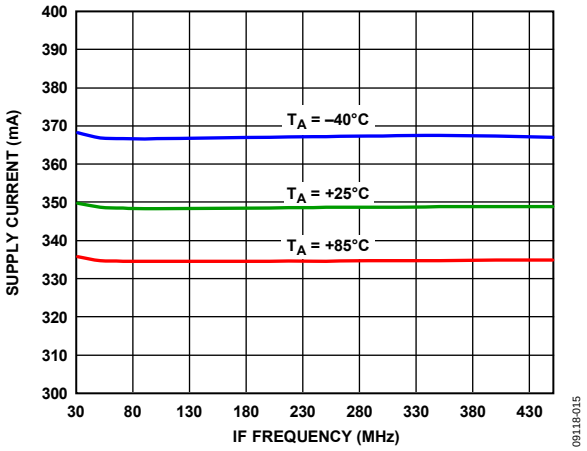


Figure 15. Supply Current vs. IF Frequency

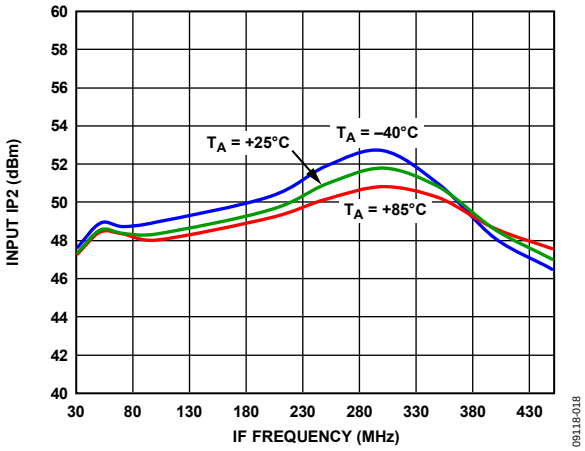


Figure 18. Input IP2 vs. IF Frequency

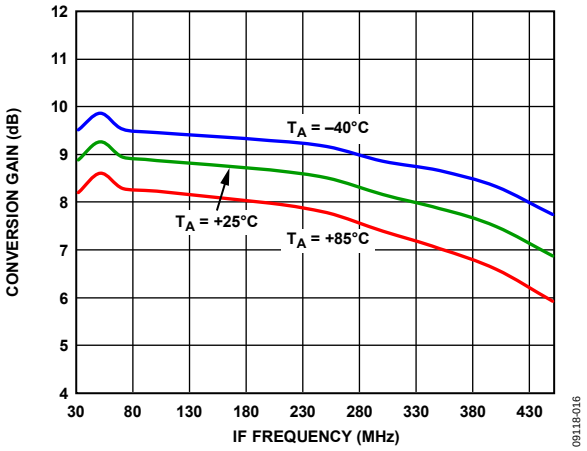


Figure 16. Power Conversion Gain vs. IF Frequency

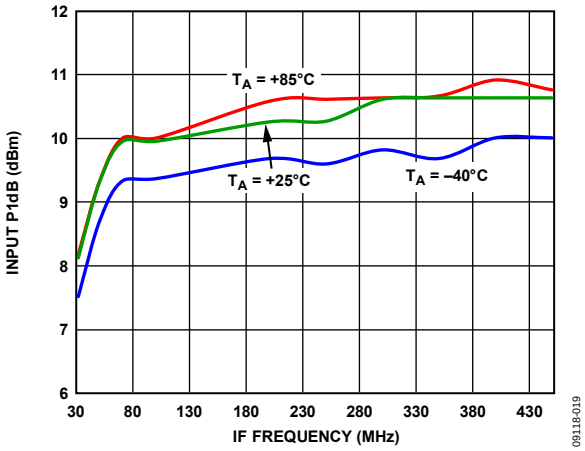


Figure 19. Input P1dB vs. IF Frequency

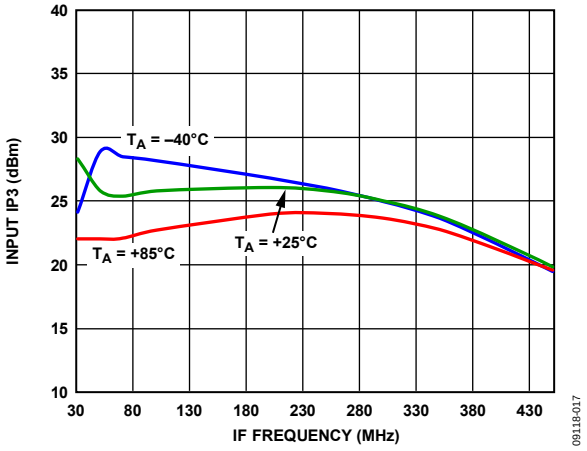


Figure 17. Input IP3 vs. IF Frequency

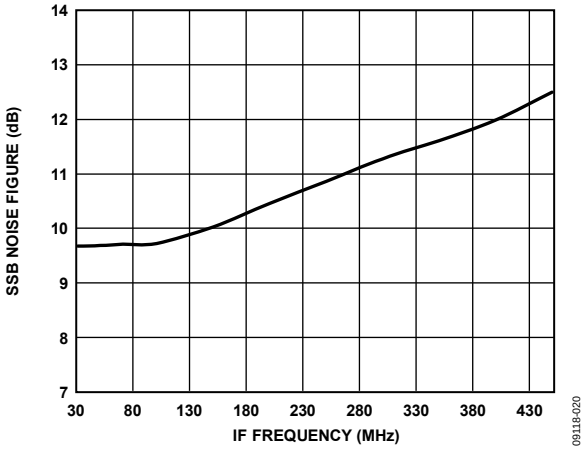


Figure 20. SSB Noise Figure vs. IF Frequency

V_S = 5 V, I_S = 350 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2332 MHz, LO power = 0 dBm, RF power = −10 dBm, R1 = R4 = 1.3 kΩ, R2 = R5 = 1 kΩ, Z_O = 50 Ω, VGS0 = VGS1 = VGS2 = 0 V, unless otherwise noted.

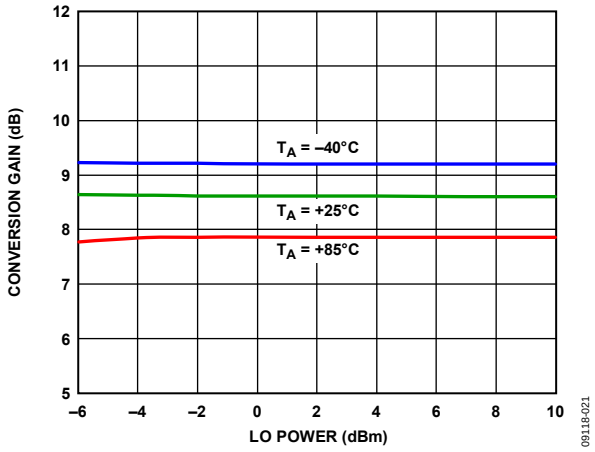


Figure 21. Power Conversion Gain vs. LO Power

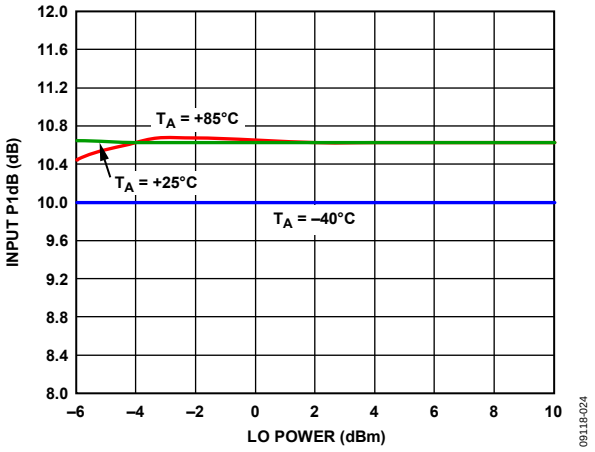


Figure 24. Input P1dB vs. LO Power

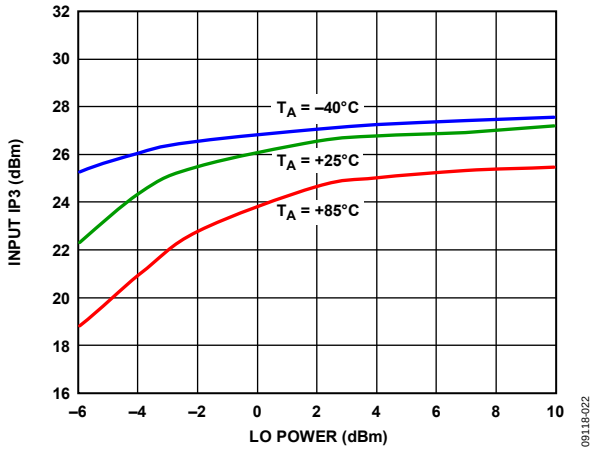


Figure 22. Input IP3 vs. LO Power

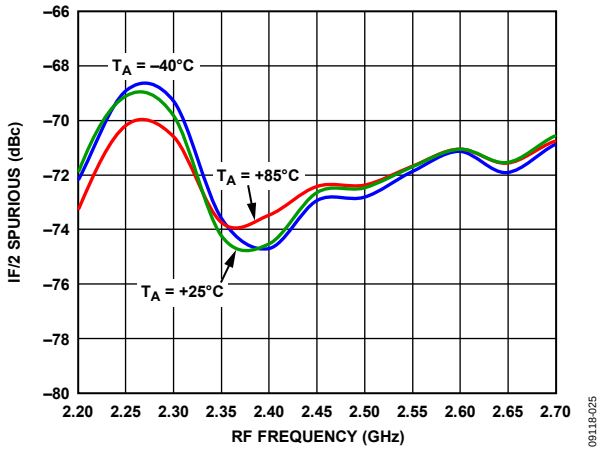


Figure 25. IF/2 Spurious vs. RF Frequency, RF Power = −10 dBm

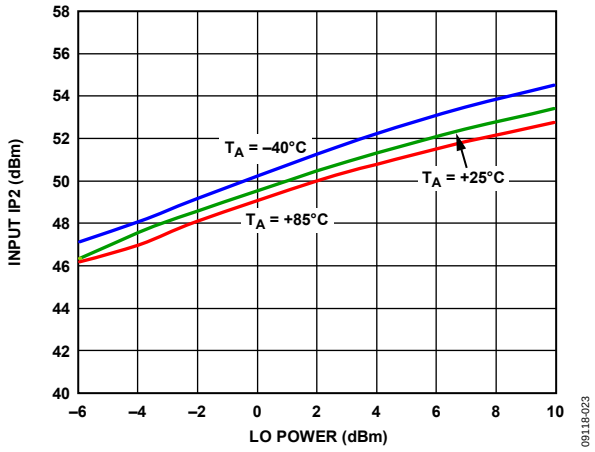


Figure 23. Input IP2 vs. LO Power

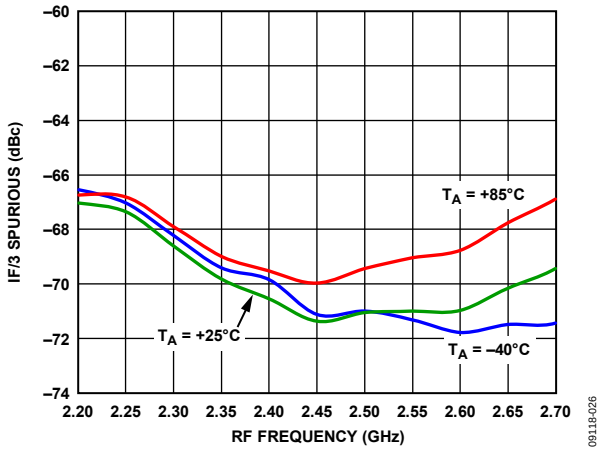


Figure 26. IF/3 Spurious vs. RF Frequency, RF Power = −10 dBm

V_S = 5 V, I_S = 350 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2332 MHz, LO power = 0 dBm, RF power = −10 dBm, R1 = R4 = 1.3 kΩ, R2 = R5 = 1 kΩ, Z_O = 50 Ω, VGS0 = VGS1 = VGS2 = 0 V, unless otherwise noted.

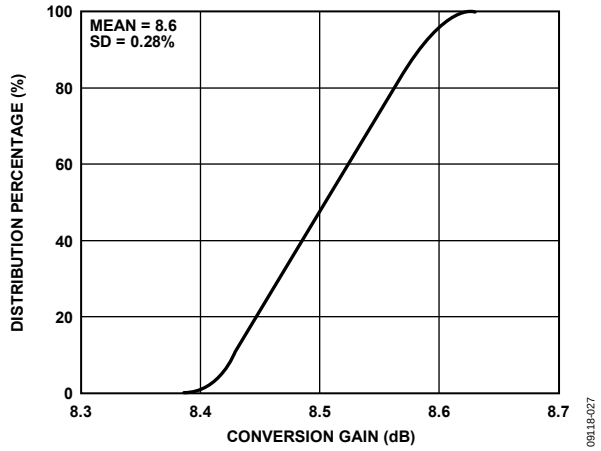


Figure 27. Conversion Gain Distribution

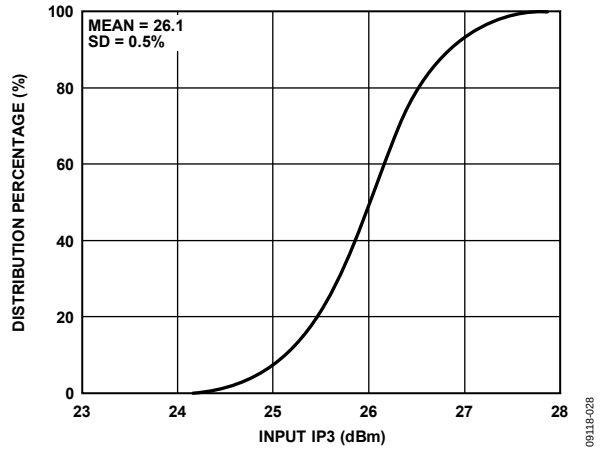


Figure 28. Input IP3 Distribution

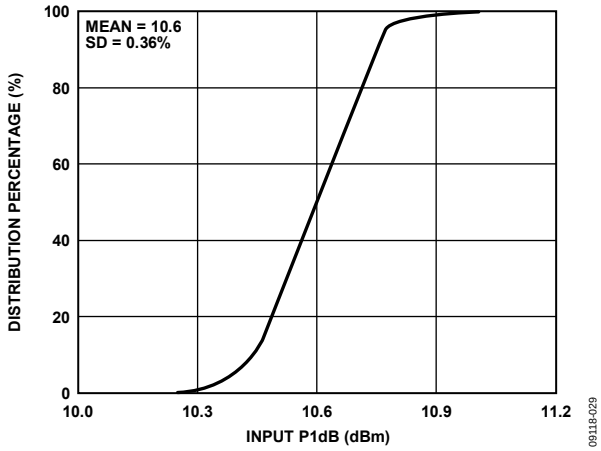


Figure 29. Input P1dB Distribution

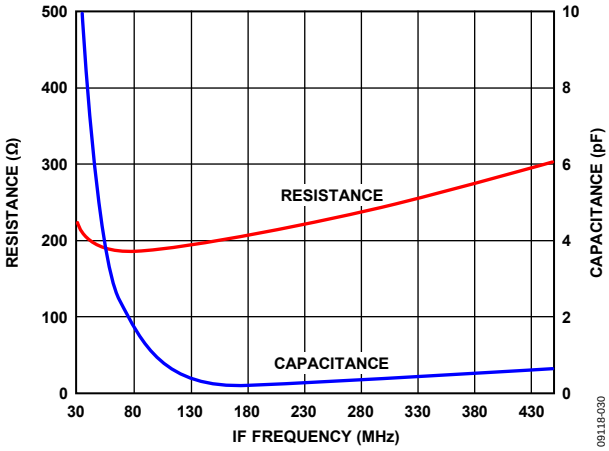


Figure 30. IF Output Impedance (R Parallel, C Equivalent)

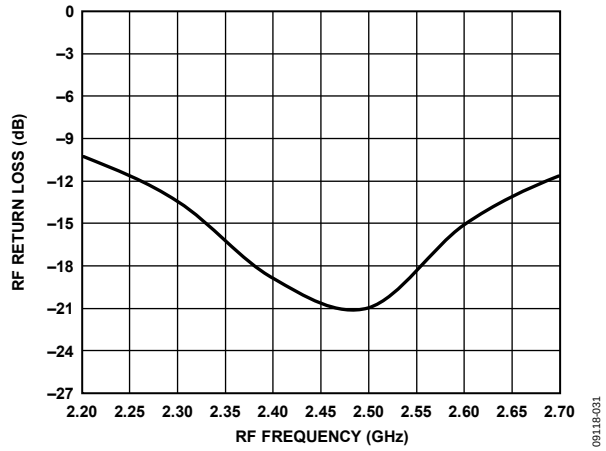


Figure 31. RF Return Loss, Fixed IF

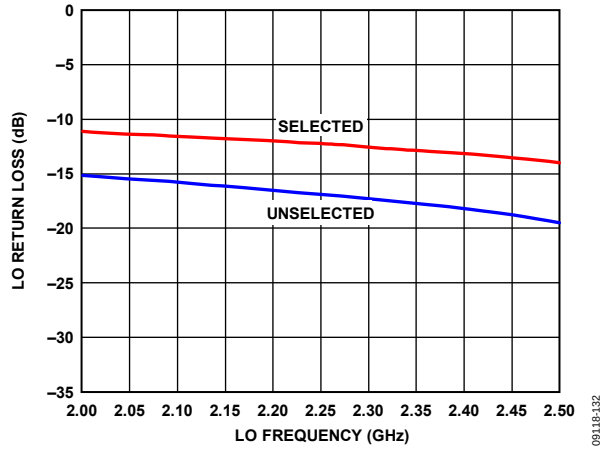


Figure 32. LO Return Loss, Selected and Unselected

V_S = 5 V, I_S = 350 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2332 MHz, LO power = 0 dBm, RF power = −10 dBm, R1 = R4 = 1.3 kΩ, R2 = R5 = 1 kΩ, Z_O = 50 Ω, VGS0 = VGS1 = VGS2 = 0 V, unless otherwise noted.

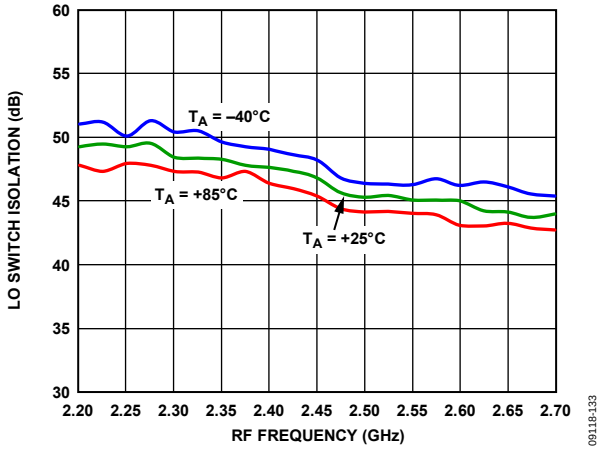


Figure 33. LO Switch Isolation vs. RF Frequency

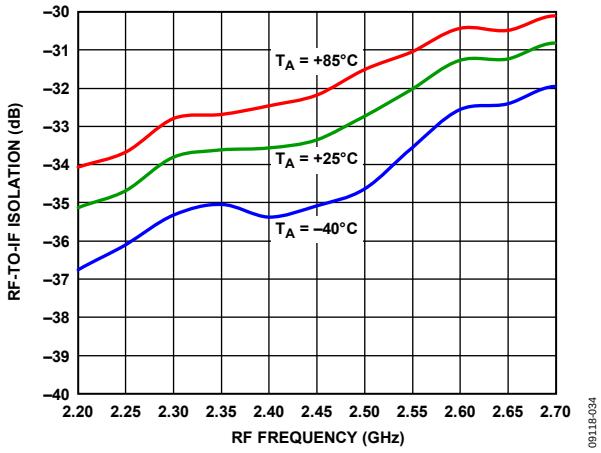


Figure 34 RF-to-IF Isolation vs. RF Frequency

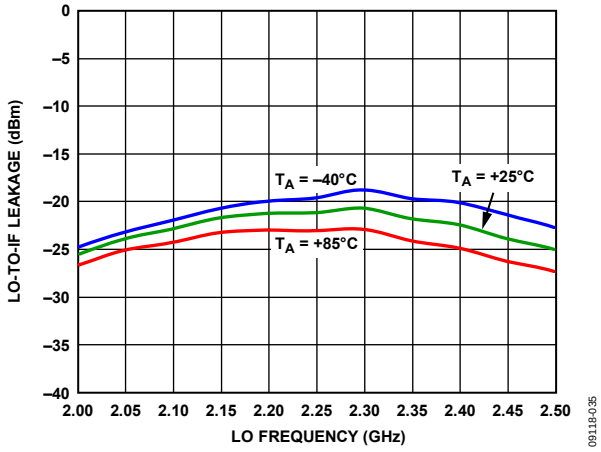


Figure 35. LO-to-IF Leakage vs. LO Frequency

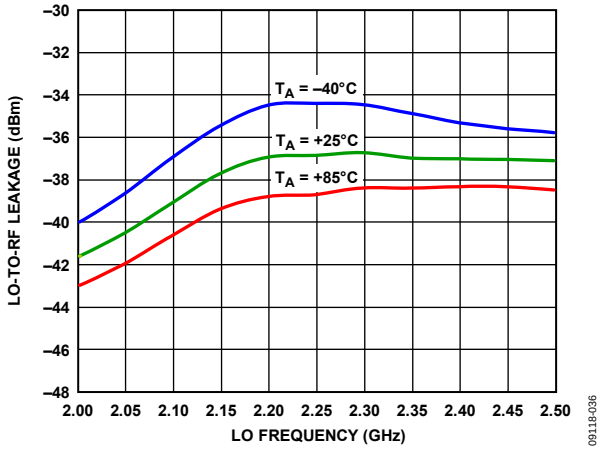


Figure 36. LO-to-RF Leakages vs. LO Frequency

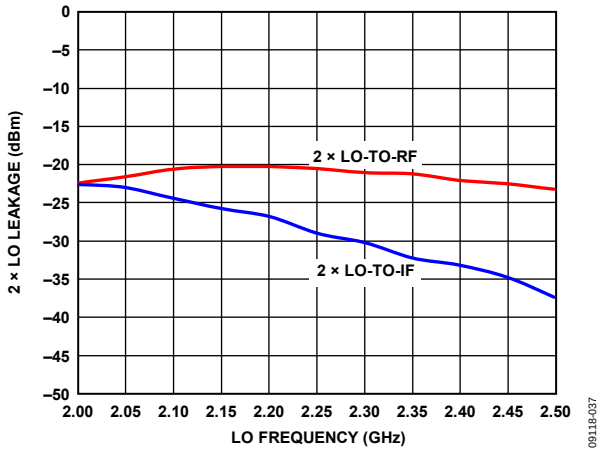


Figure 37. 2 × LO Leakage vs. LO Frequency

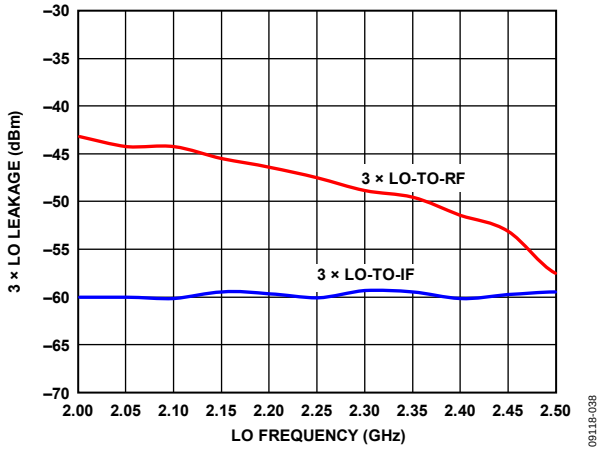


Figure 38. 3 × LO Leakage vs. LO Frequency

V_S = 5 V, I_S = 350 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2332 MHz, LO power = 0 dBm, RF power = −10 dBm, R1 = R4 = 1.3 kΩ, R2 = R5 = 1 kΩ, Z_O = 50 Ω, VGS0 = VGS1 = VGS2 = 0 V, unless otherwise noted.

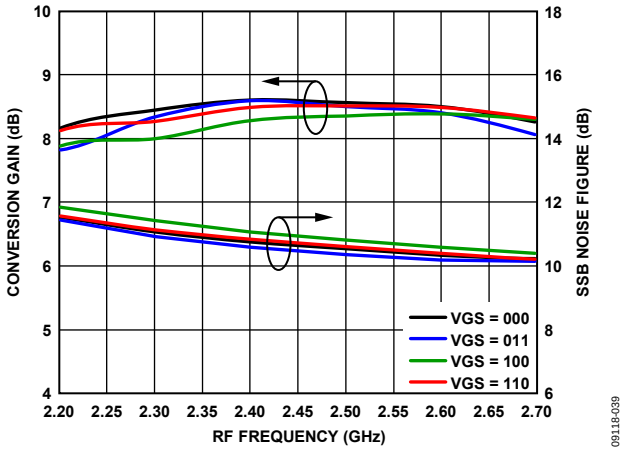


Figure 39. Power Conversion Gain and SSB Noise Figure vs. RF Frequency for Various VGS Settings

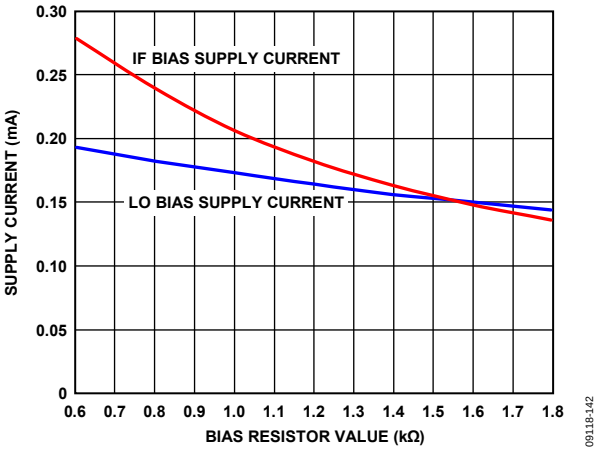


Figure 42. LO and IF Supply Current vs. IF and LO Bias Resistor Value

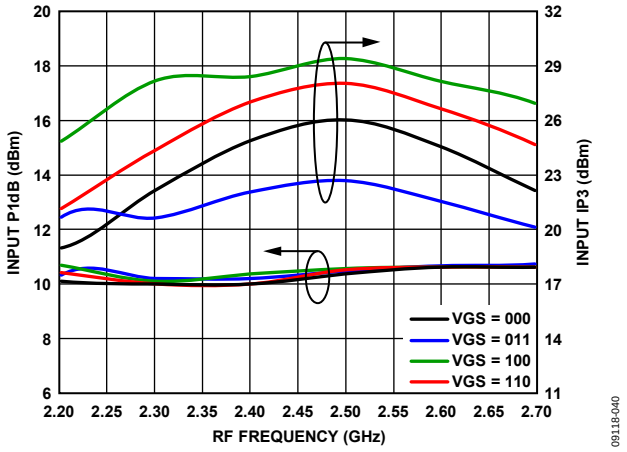


Figure 40. Input P1dB and Input IP3 vs. RF Frequency for Various VGS Settings

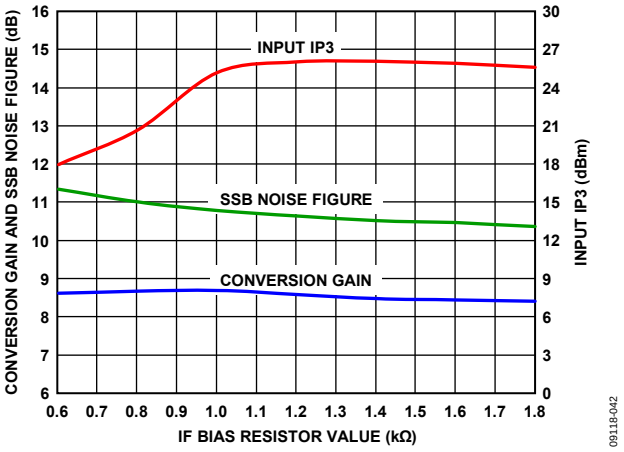


Figure 43. Power Conversion Gain, SSB Noise Figure, and Input IP3 vs. IF Bias Resistor Value

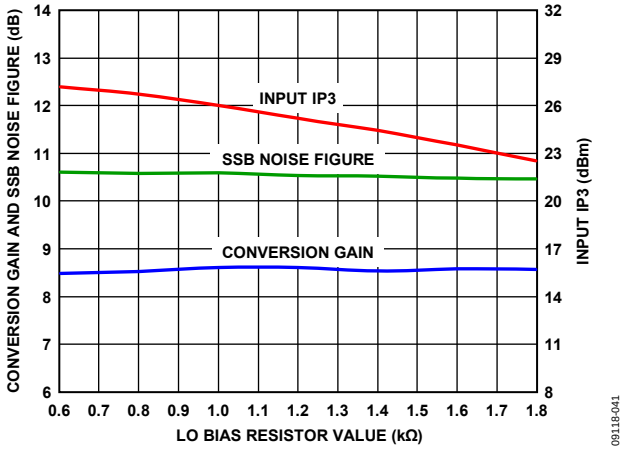


Figure 41. Power Conversion Gain, SSB Noise Figure, and Input IP3 vs. LO Bias Resistor Value

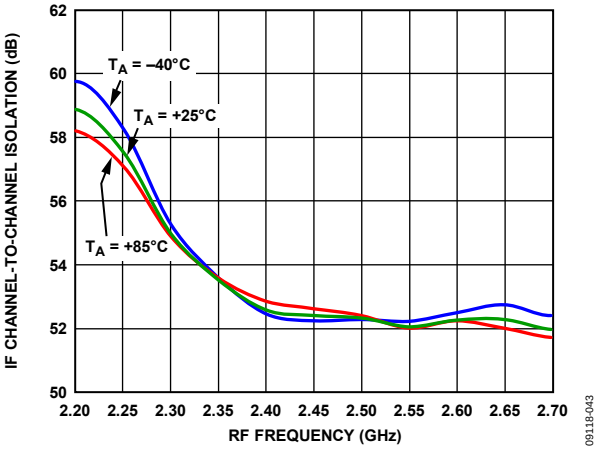


Figure 44. IF Channel-to-Channel Isolation vs. RF Frequency

3.3 V PERFORMANCE

V_S = 3.3 V, I_S = 200 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2332 MHz, LO power = 0 dBm, R9 = 226 Ω, R14 = 604 Ω, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

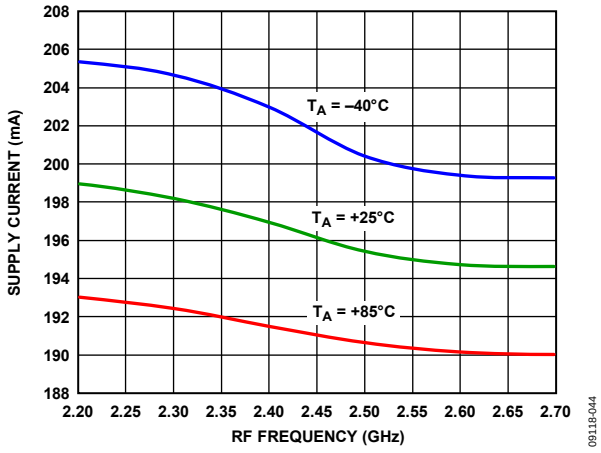


Figure 45. Supply Current vs. RF Frequency at 3.3 V

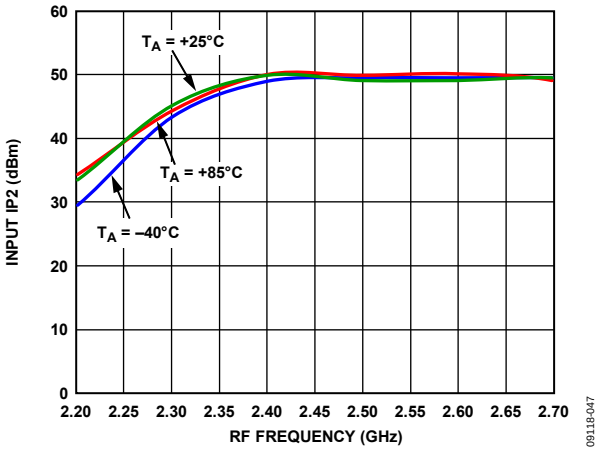


Figure 48. Input IP2 vs. RF Frequency at 3.3 V

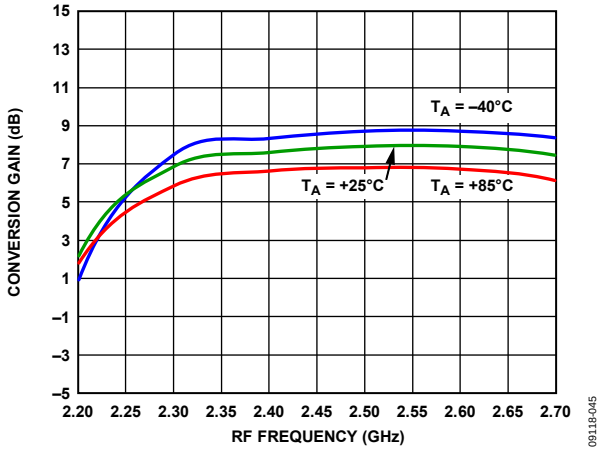


Figure 46. Power Conversion Gain vs. RF Frequency at 3.3 V

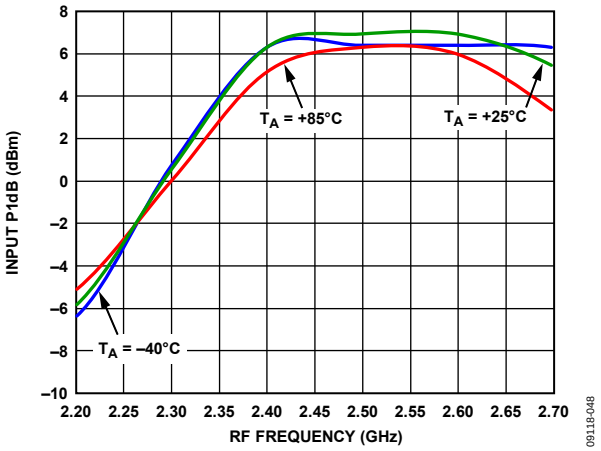


Figure 49. Input P1dB vs. RF Frequency at 3.3 V

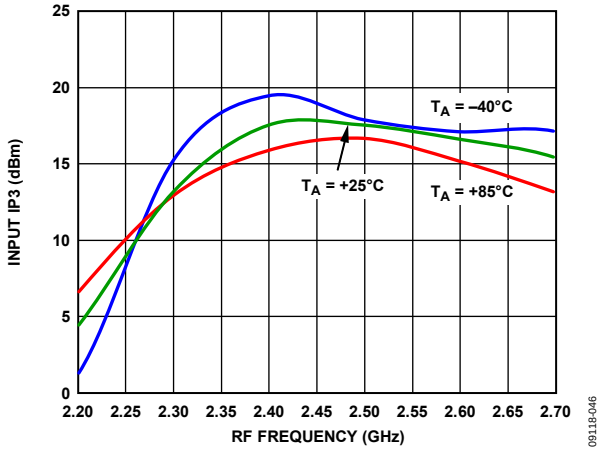


Figure 47. Input IP3 vs. RF Frequency at 3.3 V

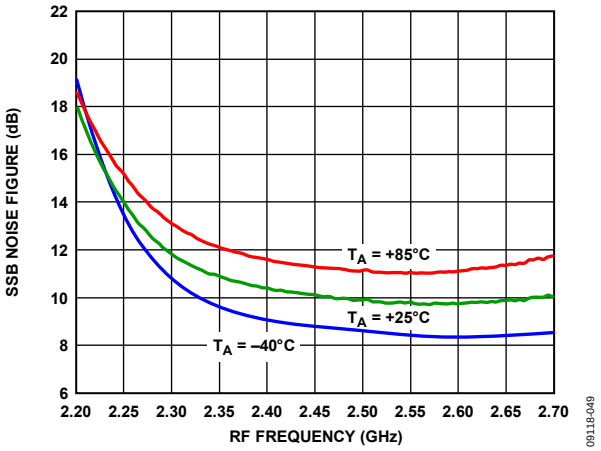


Figure 50. SSB Noise Figure vs. RF Frequency at 3.3 V

SPUR TABLES

All spur tables are (N × f_{RF}) − (M × f_{LO}) and were measured using the standard evaluation board. Mixer spurious products are measured in dBc from the IF output power level. Data was measured only for frequencies less than 6 GHz. Typical noise floor of the measurement system = −100 dBm.

5 V PERFORMANCE

V_S = 5 V, I_S = 350 mA, T_A = 25°C, f_{RF} = 2500 MHz, f_{LO} = 2297 MHz, LO power = 0 dBm, RF power = −10 dBm, VGS0 = VGS1 = VGS2 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

		M														
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
N	0		−19.7	−28.9												
	1	−41.5	0.00	−65.2	−51.9											
	2	−92.6	−95.3	−73.6	−90.2	−84.3										
	3		<−100	<−100	−77.6	<−100	<−100									
	4			<−100	<−100	<−100	<−100	<−100								
	5				<−100	<−100	<−100	<−100	<−100	<−100						
	6					<−100	<−100	<−100	<−100	<−100	<−100					
	7							<−100	<−100	<−100	<−100	<−100				
	8								<−100	<−100	<−100	<−100	<−100			
	9									<−100	<−100	<−100	<−100	<−100		
	10										<−100	<−100	<−100	<−100	<−100	
	11											<−100	<−100	<−100	<−100	<−100
	12												<−100	<−100	<−100	<−100
	13													<−100	<−100	<−100
	14														<−100	<−100
	15															<−100

3.3 V PERFORMANCE

V_S = 3.3 V, I_S = 200 mA, T_A = 25°C, f_{RF} = 2500 MHz, f_{LO} = 2297 MHz, LO power = 0 dBm, RF power = −10 dBm, R1 = R4 = 1.2 kΩ, R2 = R5 = 400 Ω, VGS0 = VGS1 = VG2 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

		M														
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
N	0		−26.5	−36.3												
	1	−40.6	0.00	−58.8	−55.5											
	2	−87.8	−77.7	−64.2	−79.1	−84.3										
	3		<−100	<−100	−70.2	<−100	<−100									
	4			<−100	<−100	<−100	<−100	<−100	<−100							
	5				<−100	<−100	<−100	<−100	<−100	<−100	<−100					
	6					<−100	<−100	<−100	<−100	<−100	<−100	<−100				
	7							<−100	<−100	<−100	<−100	<−100	<−100			
	8								<−100	<−100	<−100	<−100	<−100			
	9									<−100	<−100	<−100	<−100	<−100		
	10										<−100	<−100	<−100	<−100	<−100	
	11											<−100	<−100	<−100	<−100	<−100
	12												<−100	<−100	<−100	<−100
	13													<−100	<−100	<−100
	14														<−100	<−100
	15															<−100

CIRCUIT DESCRIPTION

The ADL5354 consists of two primary components: the radio frequency (RF) subsystem and the local oscillator (LO) subsystem. The combination of design, process, and packaging technology allows the functions of these subsystems to be integrated into a single die using mature packaging and interconnection technologies to provide a high performance, low cost design with excellent electrical, mechanical, and thermal properties. In addition, the need for external components is minimized, optimizing cost and size.

The RF subsystem consists of integrated, low loss RF baluns, passive MOSFET mixers, sum termination networks, and IF amplifiers. The LO subsystem consists of an SPDT-terminated FET switch and two multistage limiting LO amplifiers. The purpose of the LO subsystem is to provide a large, fixed amplitude, balanced signal to drive the mixer independent of the level of the LO input. A block diagram of the device is shown in Figure 51.

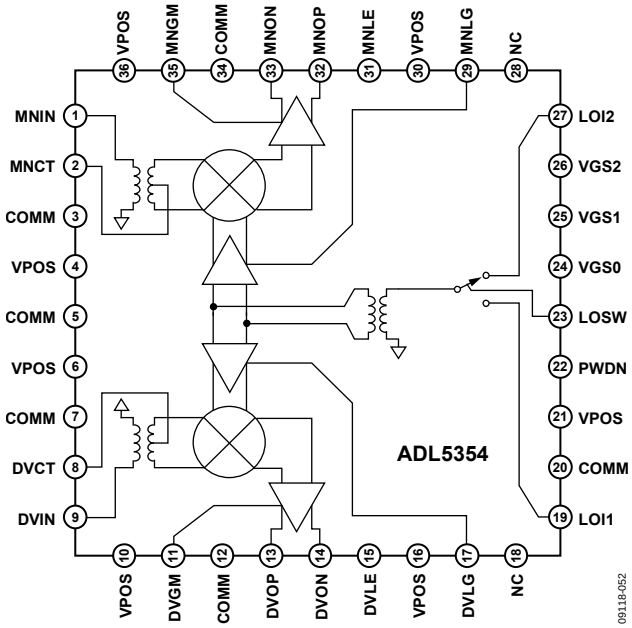


Figure 51. Simplified Schematic

RF SUBSYSTEM

The single-ended, 50 Ω RF input is internally transformed to a balanced signal using a low loss (<1 dB) unbalanced-to-balanced (balun) transformer. This transformer is made possible by an extremely low loss metal stack, which provides both excellent balance and dc isolation for the RF port. Although the port can be dc connected, it is recommended that a blocking capacitor be used to avoid running excessive dc current through the part. The RF balun can easily support an RF input frequency range of 2200 MHz to 2700 MHz.

The resulting balanced RF signal is applied to a passive mixer that commutates the RF input with the output of the LO subsystem. The passive mixer is essentially a balanced, low loss switch that adds minimal noise to the frequency translation. The only noise contribution from the mixer is due to the resistive loss of the switches, which is in the order of a few ohms.

Because the mixer is inherently broadband and bidirectional, it is necessary to properly terminate all the idler (M × N product) frequencies generated by the mixing process. Terminating the mixer avoids the generation of unwanted intermodulation products and reduces the level of unwanted signals at the input of the IF amplifier, where high peak signal levels can compromise the compression and intermodulation performance of the system. This termination is accomplished by the addition of a sum network between the IF amplifier and the mixer and in the feedback elements in the IF amplifier.

The IF amplifier is a balanced feedback design that simultaneously provides the desired gain, noise figure, and input impedance that is required to achieve the overall performance. The balanced open-collector output of the IF amplifier, with impedance modified by the feedback within the amplifier, permits the output to be connected directly to a high impedance filter, differential amplifier, or an analog-to-digital input while providing optimum second-order intermodulation suppression. The differential output impedance of the IF amplifier is approximately 200 Ω. If operation in a 50 Ω system is desired, the output can be transformed to 50 Ω by using a 4:1 transformer.

The intermodulation performance of the design is generally limited by the IF amplifier. The IP3 performance can be optimized by adjusting the IF current with an external resistor. Additionally, dc current can be saved by increasing either or both resistors. It is permissible to reduce the dc supply voltage to as low as 3.3 V, further reducing the dissipated power of the part. (No performance enhancement is obtained by reducing the value of these resistors, and excessive dc power dissipation may result.)

LO SUBSYSTEM

The ADL5354 has two LO inputs permitting multiple synthesizers to be rapidly switched with extremely short switching times (<40 ns) for frequency agile applications. The two inputs are applied to a high isolation SPDT switch that provides a constant input impedance, regardless of whether the port is selected, to avoid pulling the LO sources. This multiple section switch also ensures high isolation to the off input, minimizing any leakage from the unwanted LO input that may result in undesired IF responses.

The single-ended LO input is converted to a fixed amplitude differential signal using a multistage, limiting LO amplifier. This results in consistent performance over a range of LO input power. Optimum performance is achieved from −6 dBm to +10 dBm, but the circuit continues to function at considerably lower levels of LO input power.

The performance of this amplifier is critical in achieving a high intercept passive mixer without degrading the noise floor of the

system. This is a critical requirement in an interferer rich environment, such as cellular infrastructure, where blocking interferers can limit mixer performance. The bandwidth of the intermodulation performance is somewhat influenced by the current in the LO amplifier chain. For dc current sensitive applications, it is permissible to reduce the current in the LO amplifier by raising the value of the external bias control resistor. For dc current critical applications, the LO chain can operate with a supply voltage as low as 3.3 V, resulting in substantial dc power savings.

In addition, when operating with supply voltages below 3.6 V, the ADL5354 has a power-down mode that permits the dc current to drop to ~300 μA.

The logic inputs are designed to work with any logic family that provides a Logic 0 input level of less than 0.4 V and a Logic 1 input level that exceeds 1.4 V. All logic inputs are high impedance up to Logic 1 levels of 3.3 V. At levels exceeding 3.3 V, protection circuitry permits operation up to 5.5 V, although a small bias current is drawn.

All pins, including the RF pins, are ESD protected and have been tested to a level of 1500 V HBM and 500 V FICDM.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The ADL5354 mixer is designed to downconvert radio frequencies (RF) primarily between 2200 MHz and 2700 MHz to lower intermediate frequencies (IF) between 30 MHz and 450 MHz. Figure 52 depicts the basic connections of the mixer. It is recommended to ac couple the RF and LO input ports to prevent nonzero dc voltages from damaging the RF balun or LO input circuit. The RFIN matching network consists of a series 1.5 pF capacitor and a shunt 4.3 nH inductor to provide the optimized RF input return loss for the desired frequency band.

IF PORT

The mixer differential IF interface requires pull-up choke inductors to bias the open-collector outputs and to set the output match. The shunting impedance of the choke inductors used to couple dc current into the IF amplifier should be selected to provide the desired output return loss.

The real part of the output impedance is approximately 200 Ω, which matches many commonly used SAW filters without the need for a transformer. This results in a voltage conversion gain that is approximately 6 dB higher than the power conversion gain, as shown in Table 3. When a 50 Ω output impedance is needed, use a 4:1 impedance transformer, as shown in Figure 52.

BIAS RESISTOR SELECTION

The IF bias resistors (R1 and R4) and LO bias resistors (R2 and R5) are used to adjust the bias current of the integrated amplifiers at the IF and LO terminals. It is necessary to have a sufficient amount of current to bias both the internal IF and LO amplifiers to optimize dc current vs. optimum IIP3 performance.

MIXER VGS CONTROL DAC

The ADL5354 features three logic control pins, VGS0 (Pin 24), VGS1 (Pin 25), and VGS2 (Pin26), that allow programmability for internal gate-to-source voltages for optimizing mixer performance over desired frequency bands. The evaluation board defaults VGS0, VGS1, and VGS2 to ground.

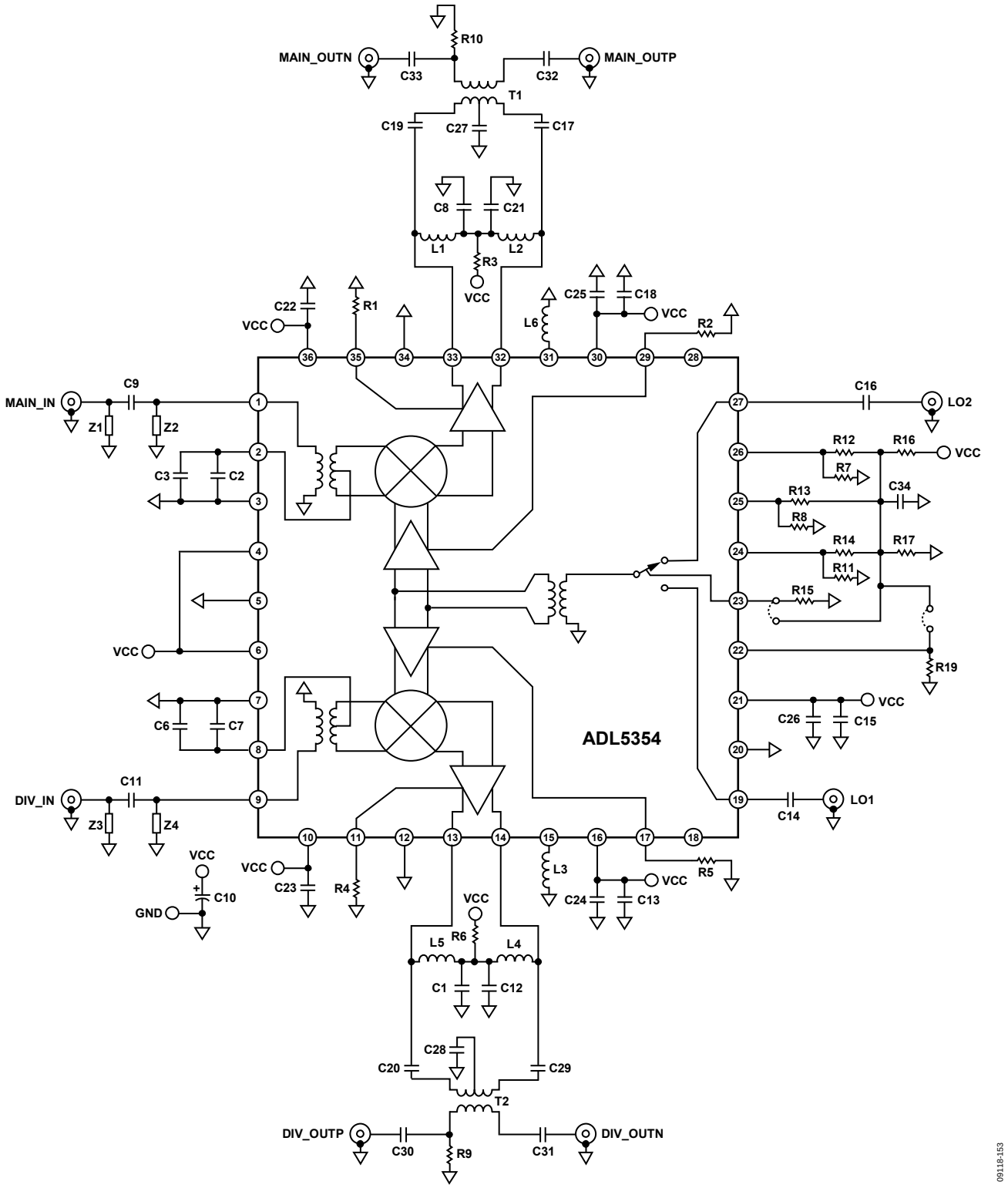


Figure 52. Typical Application Circuit

EVALUATION BOARD

An evaluation board is available for the family of double balanced mixers. The standard evaluation board schematic is shown in Figure 53. The evaluation board is fabricated using Rogers® RO3003 material. Table 7 describes the various configuration options of the evaluation board. Evaluation board layout is shown in Figure 54 and Figure 55.

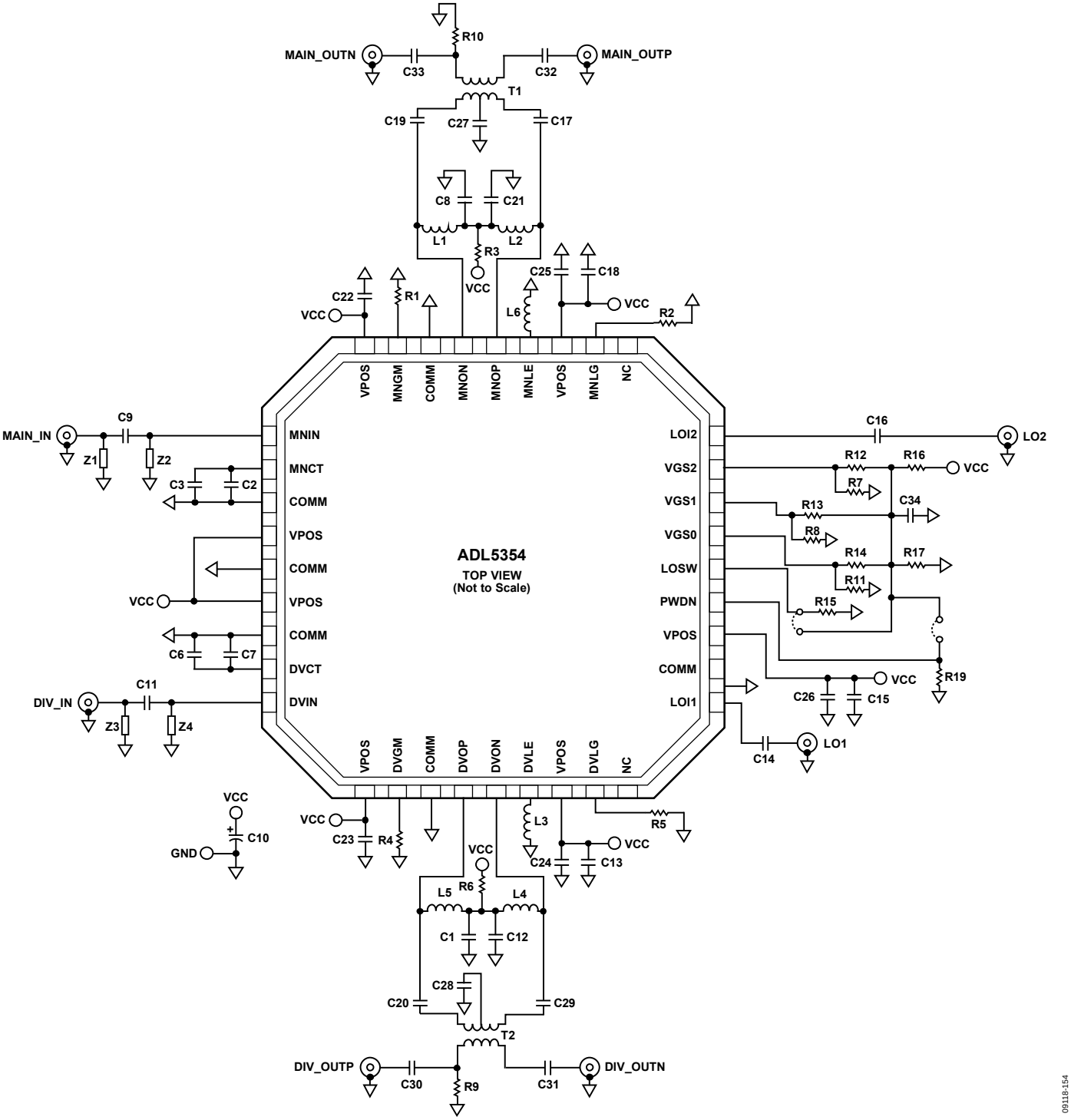


Figure 53. Evaluation Board Schematic

Table 7. Evaluation Board Configuration

Components	Description	Default Conditions
C1, C8, C10, C12, C13, C15, C18, C21, C22, C23, C24, C25, C26	Power supply decoupling. Nominal supply decoupling consists of a 0.01 µF capacitor to ground in parallel with 10 pF capacitors to ground positioned as close to the device as possible.	C10 = 4.7 µF (Size 3216), C1, C8, C12, C21 = 150 pF (Size 0402), C22, C23, C24, C25, C26 = 10 pF (Size 0402), C13, C15, C18 = 0.1 µF (Size 0402)
Z1 to Z4, C2, C3, C6, C7, C9, C11	RF main and diversity input interface. Main and diversity input channels are ac-coupled through C9 and C11. Z1 to Z4 provide additional component placement for external matching/filter networks. C2, C3, C6, and C7 provide bypassing for the center taps of the main and diversity on-chip input baluns.	C2, C7 = 10 pF (Size 0402), C3, C6 = 0.01 µF (Size 0402), C9, C11 = 1.5 pF (Size 0402), Z2, Z4 = 4.3 nH (Size 0402), Z1, Z3 = open (Size 0402)
T1, T2, C17, C19, C20, C27 to C33, L1, L2, L4, L5, R3, R6, R9, R10	IF main and diversity output interface. The open-collector IF output interfaces are biased through the pull-up choke inductors (L1, L2, L4, and L5), leaving R3 and R6 available for additional supply bypassing. T1 and T2 are 4:1 impedance transformers that are used to provide a single-ended IF output interface, and C27 and C28 provide the center tap bypassing. C17, C19, C20, C29, C30, C31, C32, and C33 ensure an ac-coupled output interface. Remove R9 and R10 for balanced output operation.	C17, C19, C20, C29 to C33 = 0.001 µF (Size 0402), C27, C28 = 150 pF (Size 0402), T1, T2 = TC4-1T+ (Mini-Circuits), L1, L2, L4, L5 = 330 nH (Size 0805), R3, R6, R9, R10 = 0 Ω (Size 0402)
C14, C16, R15, LOSEL	LO interface. C14 and C16 provide ac coupling for the LOI1 and LOI2 local oscillator inputs. LOSEL selects the appropriate LO input for both mixer cores. R15 provides a pull-down to ensure LOI2 is enabled when the LOSEL jumper is removed. The jumper can be removed to allow the LOSEL interface to be exercised by using an external logic generator.	C14, C16 = 10 pF (Size 0402), R15 = 10 kΩ (Size 0402), LOSEL = 2-pin shunt
R19, PWDN	PWDN interface. When the PWDN 2-pin shunt is inserted, the ADL5354 is powered down. When R19 is open, it pulls the PWDN logic low and enables the device. The jumper can be removed to allow PWDN interface to be exercised using an external logic generator. Grounding the PWDN pin is allowed during nominal operation but is not permitted when supply voltages exceed 3.3 V.	R19 = 10 kΩ (Size 0402), PWDN = 2-pin shunt
R1, R2, R4, R5, L3, L6, R7, R8, R11 to R14, R16, R17, C34	Bias control. R16 and R17 form a voltage divider to provide a 3 V for logic control, bypassed to ground through C34. Resistors R7, R8, R11, R12, R13, and R14 provide resistor programmability of VGS0, VGS1, and VGS2. Typically, these nodes can be hardwired for nominal operation. Grounding these pins is allowed for nominal operation. R2 and R5 set the bias point for the internal LO buffers. R1 and R4 set the bias point for the internal IF amplifiers. L3 and L6 are external inductors used to improve isolation and common-mode rejection.	R1, R4 = 1.3 kΩ (Size 0402), R2, R5 = 1 kΩ (Size 0402), L3, L6 = 0 Ω (Size 0603), R12, R13, R14 = open (Size 0402), R7, R8, R11 = 0 Ω (Size 0402), R16 = 10 kΩ (Size 0402), R17 = 15 kΩ (Size 0402), C34 = 1 nF (Size 0402)

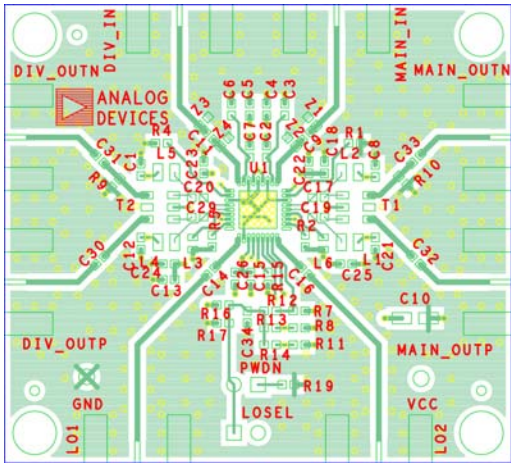


Figure 54. Evaluation Board Top Layer

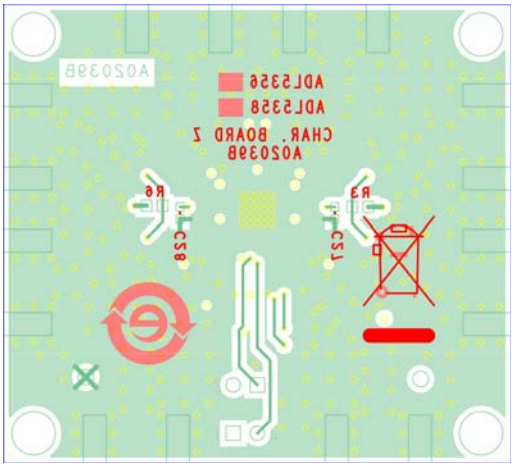


Figure 55. Evaluation Board Bottom Layer

OUTLINE DIMENSIONS

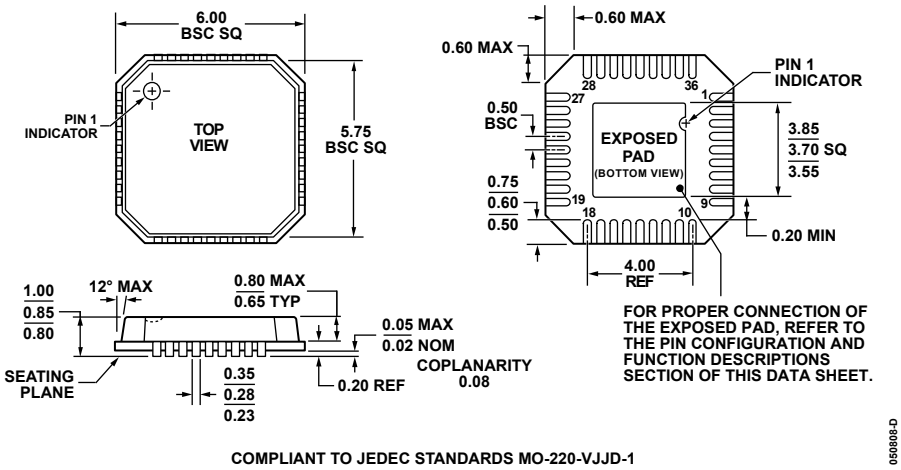


Figure 56. 36-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm Body, Very Thin Quad (CP-36-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADL5354ACPZ-R2	−40°C to +85°C	36-Lead LFCSP_VQ	CP-36-1
ADL5354ACPZ-R7	−40°C to +85°C	36-Lead LFCSP_VQ	CP-36-1
ADL5354-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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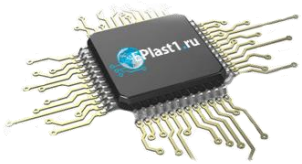
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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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