

### FEATURES

- High accuracy reference output voltage:  $1\text{ V} \pm 0.9\%$**
- Single-supply voltage operation: 2.3 V to 5.5 V**
- Rail-to-rail common-mode input voltage range**
- Low input offset voltage across  $V_{\text{CMR}}$ : 1 mV typical**
- Guarantees comparator output logic low from  $V_{\text{CC}} = 0.9\text{ V}$  to undervoltage lockout (UVLO)**
- Operating temperature range:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$**
- Package types:**
  - 8-lead, narrow body SOIC ([ADCMP394](#))
  - 10-lead MSOP ([ADCMP395](#))
  - 16-lead, narrow body SOIC ([ADCMP396](#))

### APPLICATIONS

- Battery management/monitoring**
- Power supply detection**
- Window comparators**
- Threshold detectors/discriminators**
- Microprocessor systems**

### GENERAL DESCRIPTION

The [ADCMP394/ADCMP395/ADCMP396](#) are single/dual/quad rail-to-rail input, low power comparator ideal for use in general-purpose applications. These comparators operate from a supply voltage of 2.3 V to 5.5 V and draw a minimal amount of current. The single [ADCMP394](#) consumes only 33.9  $\mu\text{A}$  of supply current. The dual [ADCMP395](#) and quad [ADCMP396](#) consumes 37.2  $\mu\text{A}$  and 41.6  $\mu\text{A}$  of supply current respectively. The low voltage and low current operation of these devices makes it ideal for battery-powered systems.

The comparators features a common-mode input voltage range of 200 mV beyond rails, an offset voltage of 1 mV typical across the full common-mode range, and a UVLO monitor. In addition, the design of the comparator allows a defined output state upon power-up. The comparator generates a logic low output if the supply voltage is less than the UVLO threshold.

The [ADCMP394/ADCMP395/ADCMP396](#) incorporates a  $1\text{ V} \pm 0.9\%$  buffered reference voltage. The reference voltage output can directly connect to the comparator input to serve as the trip value for precise monitoring and detection of positive voltage. It can also act as an offset when monitoring the negative voltage.

The [ADCMP394](#) and [ADCMP396](#) are available in 8-pin and 16-lead, narrow body SOIC package, respectively. The [ADCMP395](#) is available in a 10-lead MSOP package. The comparators are specified to operate over the  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$  extended temperature range.

Rev. B

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### FUNCTIONAL BLOCK DIAGRAMS

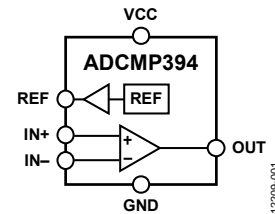


Figure 1.

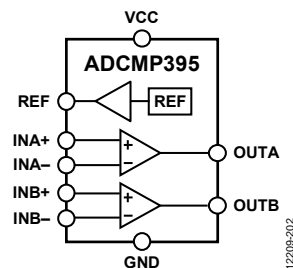


Figure 2.

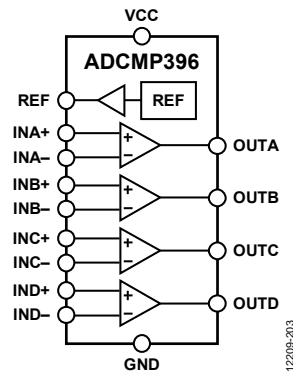


Figure 3.

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**REVISION HISTORY**

**5/16—Rev. A to Rev. B**

Changes to Equation 4 .....	12
Changes to Figure 39.....	14

**3/15—Rev. 0 to Rev. A**

Added ADCMP395/ADCMP396 (Throughout) .....	1
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**11/14—Revision 0: Initial Version**

## SPECIFICATIONS

$V_{CC} = 2.3 \text{ V to } 5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ ,  $V_{CMR} = -200 \text{ mV to } V_{CC} + 200 \text{ mV}$ , unless otherwise noted. Typical values are at  $T_A = 25^\circ\text{C}$ .

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments <sup>1</sup>
<b>POWER SUPPLY</b>						
Supply Voltage Range	$V_{CC}$	2.3 0.9		5.5 UVLO <sub>RISE</sub>	V V	Guarantees comparator output low
$V_{CC}$ Quiescent Current	$I_{CC}$					
ADCMP394			33.9	47.9	$\mu\text{A}$	All outputs in high-Z state, $V_{OD} = 0.1 \text{ V}$
ADCMP395			32.6	45.8	$\mu\text{A}$	All outputs low, $V_{OD} = 0.1 \text{ V}$
ADCMP396			37.2	51.9	$\mu\text{A}$	All outputs in high-Z state, $V_{OD} = 0.1 \text{ V}$
			35.9	49.2	$\mu\text{A}$	All outputs low, $V_{OD} = 0.1 \text{ V}$
			41.6	59.4	$\mu\text{A}$	All outputs in high-Z state, $V_{OD} = 0.1 \text{ V}$
			41.3	56.4	$\mu\text{A}$	All outputs low, $V_{OD} = 0.1 \text{ V}$
<b>UNDERVOLTAGE LOCKOUT</b>						
$V_{CC}$ Rising	UVLO <sub>RISE</sub>	2.062	2.162	2.262	V	
Hysteresis	UVLO <sub>HYS</sub>	5	25	50	mV	
<b>REFERENCE OUTPUT</b>						
Reference Output Voltage	$V_{REF}$	0.991 0.991	1 1	1.008 1.008	V V	$I_{REF} = \pm 1 \text{ mA}$ , $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $I_{REF} = \pm 1 \text{ mA}$
<b>COMPARATOR INPUT</b>						
Common-Mode Input Range	$V_{CMR}$	-200		$V_{CC} + 200$	mV	
Input Offset Voltage	$V_{OS}$		0.5 0.5 1 1	2.5 2.5 5 5	mV mV mV mV	$IN+ = IN- = 1 \text{ V}$ $IN+ = IN- = 1 \text{ V}$ , $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $T_A = -40^\circ\text{C to } +85^\circ\text{C}$
Input Offset Current	$I_{OS}$			10	nA	$V_{CMR} = -50 \text{ mV to } V_{CC} + 50 \text{ mV}$
Input Bias Current	$I_{BIAS}$			$\pm 30$ $\pm 80$ $\pm 10$	nA nA nA	$IN+ = IN- = 1 \text{ V}$ $V_{CMR} = -50 \text{ mV to } V_{CC} + 50 \text{ mV}$ $V_{CMR} = -50 \text{ mV to } V_{CC} + 50 \text{ mV}$ , $T_A = -40^\circ\text{C to } +85^\circ\text{C}$
Input Hysteresis	$V_{HYST}$		3 6	4 8	mV mV	$V_{CM} = 1 \text{ V}$
<b>COMPARATOR OUTPUT</b>						
Output Low Voltage	$V_{OL}$		0.1 0.01	0.3 0.15	V V	$V_{CC} = 2.3 \text{ V}$ , $I_{SINK} = 2.5 \text{ mA}$ $V_{CC} = 0.9 \text{ V}$ , $I_{SINK} = 100 \mu\text{A}$
Output Leakage Current	$I_{LEAK}$			150	nA	$V_{OUT} = 0 \text{ V to } 5.5 \text{ V}$
<b>COMPARATOR CHARACTERISTICS</b>						
Power Supply Rejection Ratio	PSRR	60	80		dB	
Common-Mode Rejection Ratio	CMRR	50	74		dB	
Voltage Gain	$A_V$		132		dB	
Rise Time <sup>2</sup>	$t_R$		1.1		$\mu\text{s}$	$V_{OUT} = 10\% \text{ to } 90\% \text{ of } V_{CC}$
Fall Time <sup>2</sup>	$t_F$		0.15		$\mu\text{s}$	$V_{OUT} = 90\% \text{ to } 10\% \text{ of } V_{CC}$
Propagation Delay						
Input Rising <sup>2</sup>	$t_{PROP\_R}$		4.7 4.9		$\mu\text{s}$ $\mu\text{s}$	$V_{CM} = 1 \text{ V}$ , $V_{CC} = 2.3 \text{ V}$ , $V_{OD} = 10 \text{ mV}$ $V_{CM} = 1 \text{ V}$ , $V_{CC} = 5 \text{ V}$ , $V_{OD} = 10 \text{ mV}$
				2.8 3.2	$\mu\text{s}$ $\mu\text{s}$	$V_{CM} = 1 \text{ V}$ , $V_{CC} = 2.3 \text{ V}$ , 100 mV overdrive $V_{CM} = 1 \text{ V}$ , $V_{CC} = 5 \text{ V}$ , 100 mV overdrive
ADCMP395 Channel B			4.9		$\mu\text{s}$	$V_{CM} = 1 \text{ V}$ , $V_{CC} = 2.3 \text{ V}$ , $V_{OD} = 10 \text{ mV}$
			9.7		$\mu\text{s}$	$V_{CM} = 1 \text{ V}$ , $V_{CC} = 5 \text{ V}$ , $V_{OD} = 10 \text{ mV}$
Input Falling <sup>2</sup>	$t_{PROP\_F}$		4.5 9.5		$\mu\text{s}$ $\mu\text{s}$	$V_{CM} = 1 \text{ V}$ , $V_{CC} = 2.3 \text{ V}$ , $V_{OD} = 10 \text{ mV}$ $V_{CM} = 1 \text{ V}$ , $V_{CC} = 5 \text{ V}$ , $V_{OD} = 10 \text{ mV}$
				2	$\mu\text{s}$	$V_{CM} = 1 \text{ V}$ , $V_{CC} = 2.3 \text{ V}$ , 100 mV overdrive
ADCMP395 Channel B				4.2	$\mu\text{s}$	$V_{CM} = 1 \text{ V}$ , $V_{CC} = 5 \text{ V}$ , 100 mV overdrive
			4.7		$\mu\text{s}$	$V_{CM} = 1 \text{ V}$ , $V_{CC} = 2.3 \text{ V}$ , $V_{OD} = 10 \text{ mV}$
			5		$\mu\text{s}$	$V_{CM} = 1 \text{ V}$ , $V_{CC} = 5 \text{ V}$ , $V_{OD} = 10 \text{ mV}$

<sup>1</sup>  $V_{OD}$  is overdrive voltage.

<sup>2</sup>  $R_{PULL-UP} = 10 \text{ k}\Omega$ , and  $C_L = 50 \text{ pF}$ .

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC Pin	-0.3 V to +6 V
All INx+ and INx- Pins	-0.3 V to +6 V
All OUTx Pins	-0.3 V to +6 V
Reference Load Current, $I_{REF}$	$\pm 1$ mA
OUTx Pins Sink Current, $I_{SINK}$	10 mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Lead Temperature (10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Table 3. Thermal Resistance

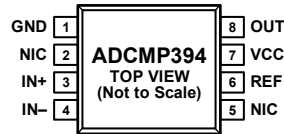
Package Type	$\theta_{JA}$	Unit
8-Lead Narrow-Body SOIC	121	°C/W
10-Lead MSOP	130	°C/W
16-Lead Narrow-Body SOIC	80	°C/W

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

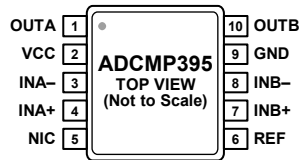


NOTES  
1. NIC = NOT INTERNALLY CONNECTED.

Figure 4. ADCMP394 Pin Configuration

Table 4. ADCMP394 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Device Ground.
2, 5	NIC	Not Internally Connected.
3	IN+	Comparator Noninverting Input.
4	IN-	Comparator Inverting Input.
6	REF	Reference Output. This pin can be used to setup the comparator threshold.
7	VCC	Device Supply Input.
8	OUT	Comparator Output, Open-Drain.



NIC = NOT INTERNALLY CONNECTED.

Figure 5. ADCMP395 Pin Configuration

Table 5. ADCMP395 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUTA	Comparator A Output, Open Drain.
2	VCC	Device Supply Input.
3	INA-	Comparator A Inverting Input.
4	INA+	Comparator A Noninverting Input.
5	NIC	Not Internally Connected.
6	REF	Reference Output. This pin can be used to set up comparator threshold.
7	INB+	Comparator B Noninverting Input.
8	INB-	Comparator B Inverting Input.
9	GND	Device Ground.
10	OUTB	Comparator B Output, Open Drain.



NIC = NOT INTERNALLY CONNECTED.

Figure 6. ADCMP396 Pin Configuration

Table 6. ADCMP396 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUTB	Comparator B Output, Open Drain.
2	OUTA	Comparator A Output, Open Drain.
3	VCC	Device Supply Input.
4	INA-	Comparator A Inverting Input.
5	INA+	Comparator A Noninverting Input.
6	INB-	Comparator B Inverting Input.
7	INB+	Comparator B Noninverting Input.
8	NIC	Not Internally Connected.
9	REF	Reference Output. This pin can be used to set up the comparator threshold.
10	INC-	Comparator C Inverting Input.
11	INC+	Comparator C Noninverting Input.
12	IND-	Comparator D Inverting Input.
13	IND+	Comparator D Noninverting Input.
14	GND	Device Ground.
15	OUTD	Comparator D Output, Open Drain.
16	OUTC	Comparator C Output, Open Drain.

TYPICAL PERFORMANCE CHARACTERISTICS

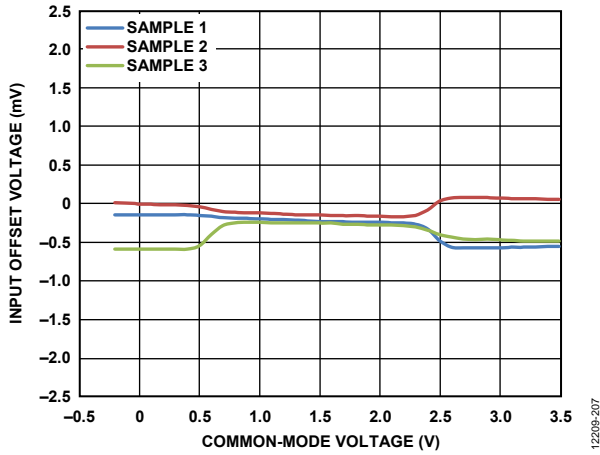


Figure 7. Input Offset Voltage ( $V_{OS}$ ) vs. Common-Mode Voltage ( $V_{CM}$ ),  $V_{CC} = 3.3V$

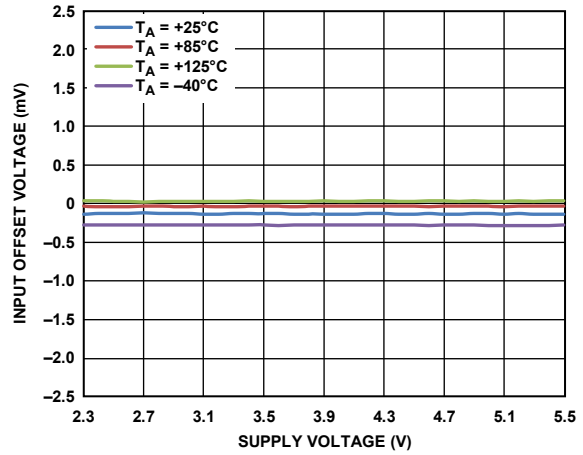


Figure 10. Input Offset Voltage ( $V_{OS}$ ) vs. Supply Voltage ( $V_{CC}$ ),  $V_{CM} = 1V$  for Various Temperatures

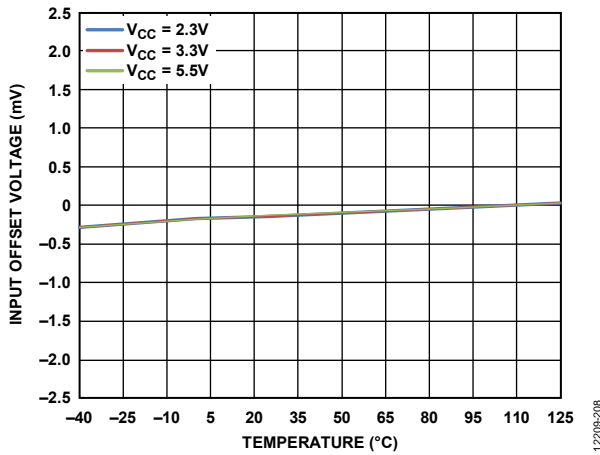


Figure 8. Input Offset Voltage ( $V_{OS}$ ) vs. Temperature for Various Supply Voltages,  $V_{CM} = 1V$

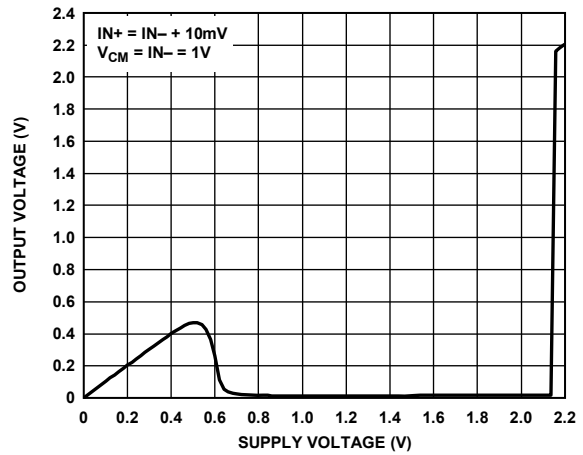


Figure 11. Output Voltage ( $V_{OUT}$ ) vs. Supply Voltage ( $V_{CC}$ ),  $R_{PULLUP} = 10k\Omega$

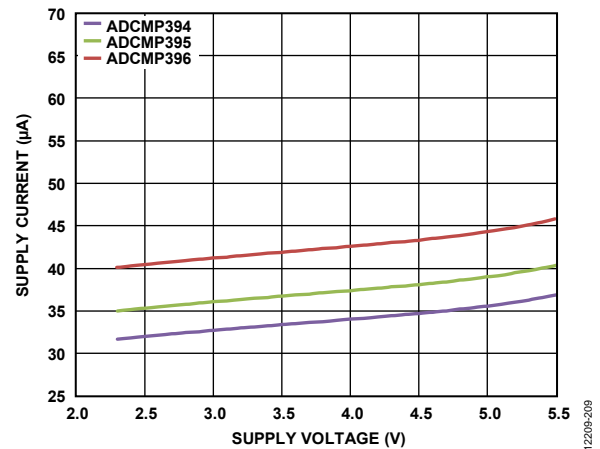


Figure 9. Supply Current ( $I_{CC}$ ) vs. Supply Voltage ( $V_{CC}$ ) at Output Low Voltage

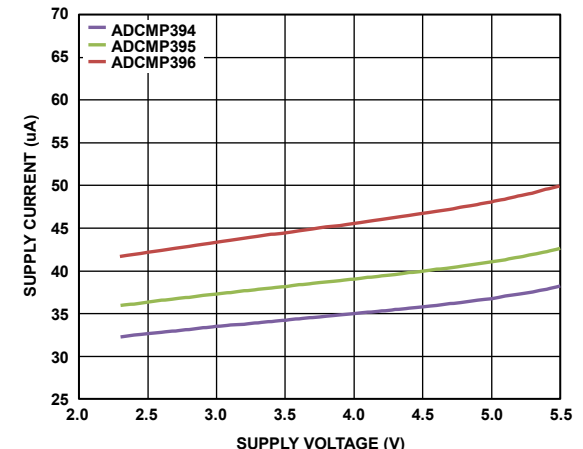


Figure 12. Supply Current ( $I_{CC}$ ) vs. Supply Voltage ( $V_{CC}$ ) at Output High Voltage



Figure 13. Supply Current ( $I_{CC}$ ) vs. Temperature at Output High Voltage ( $V_{OH}$ )



Figure 16. Supply Current ( $I_{CC}$ ) vs. Temperature at Output Low Voltage ( $V_{OL}$ )



Figure 14. Input Hysteresis vs. Supply Voltage ( $V_{CC}$ ),  $V_{CM} = 1\text{ V}$  for Various Temperatures



Figure 17. Input Hysteresis vs. Temperature,  $V_{CM} = 1\text{ V}$  for Various Supply Voltages ( $V_{CC}$ )



Figure 15. Propagation Delay vs. Temperature, Low to High,  $V_{OD} = 10\text{ mV}$



Figure 18. Propagation Delay vs. Temperature, High to Low,  $V_{OD} = 10\text{ mV}$





Figure 19. Propagation Delay vs. Input Overdrive Voltage, Low to High



Figure 22. Propagation Delay vs. Input Overdrive Voltage, High to Low



Figure 20. Propagation Delay vs. Input Overdrive Voltage, Low to High, Channel B



Figure 23. Propagation Delay vs. Input Overdrive Voltage, High to Low, Channel B



Figure 21. Output Voltage Rise Time ( $t_r$ ) vs. Pull-Up Resistance ( $R_{PULLUP}$ )



Figure 24. Output Voltage Fall Time ( $t_f$ ) vs. Pull-Up Resistance ( $R_{PULLUP}$ )



Figure 25. Reference Voltage ( $V_{REF}$ ) vs. Source Current ( $I_{SOURCE}$ ) of the REF Pin,  $V_{CC} = 3.3\text{ V}$



Figure 28. Reference Voltage ( $V_{REF}$ ) vs. Sink Current ( $I_{SINK}$ ) of the REF Pin,  $V_{CC} = 3.3\text{ V}$



Figure 26. Reference Voltage ( $V_{REF}$ ) vs. Temperature,  $V_{CC} = 3.3\text{ V}$



Figure 29. Reference Voltage ( $V_{REF}$ ) vs. Supply Voltage ( $V_{CC}$ )



Figure 27. Output Voltage ( $V_{OUT}$ ) Low vs. Sink Current ( $I_{SINK}$ ) for Various Supply Voltages



Figure 30. Output Voltage ( $V_{OUT}$ ) Low vs. Sink Current ( $I_{SINK}$ ),  $V_{CC} = 0.9\text{ V}$

## THEORY OF OPERATION

### BASIC COMPARATOR

In its most basic configuration, a comparator can be used to convert an analog input signal to a digital output signal (see Figure 31). The analog signal on INx+ is compared to the voltage on INx-, and the voltage at OUTx is either high or low, depending on whether INx+ is at a higher or lower potential than INx-, respectively.

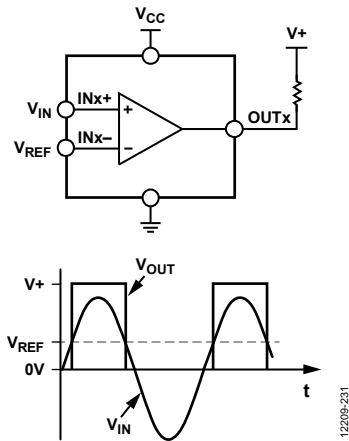


Figure 31. Basic Comparator and Input and Output Signals

### RAIL-TO-RAIL INPUT (RRI)

Using a CMOS nonRRI stage (that is, a single differential pair) limits the input voltage to approximately one gate-to-source voltage ( $V_{GS}$ ) away from one of the supply lines. Because  $V_{GS}$  for normal operation is commonly more than 1 V, a single differential pair input stage comparator greatly restricts the allowable input voltage. This restriction can be quite limiting with low voltage supplies. To resolve this issue, RRI stages allow the input signal range to extend up to the supply voltage range. In the case of the ADCMP394/ADCMP395/ADCMP396, the inputs continue to operate 200 mV beyond the supply rails.

### OPEN-DRAIN OUTPUT

The ADCMP394/ADCMP395/ADCMP396 have an open-drain output stage that requires an external resistor to pull up to the logic high voltage level when the output transistor is switched off. The pull-up resistor must be large enough to avoid excessive power dissipation, but small enough to switch logic levels reasonably quickly when the comparator output is connected to other digital circuitry. The rise time of the open-drain output depends on the pull-up resistor ( $R_{PULLUP}$ ) and load capacitor ( $C_L$ ) used.

The rise time can be calculated by

$$t_R = 2.2 R_{PULLUP} C_L \quad (1)$$

### POWER-UP BEHAVIOR

On power-up, when  $V_{CC}$  reaches 0.9 V, the ADCMP394/ADCMP395/ADCMP396 is guaranteed to assert an output low logic. When the voltage on the  $V_{CC}$  pin exceeds UVLO, the comparator inputs take control.

### CROSSOVER BIAS POINT

Rail-to-rail inputs of this type of architecture in both op amps and comparators, have a dual front-end design. PMOS devices are inactive near the  $V_{CC}$  rail, and NMOS devices are inactive near GND. At some predetermined point in the common-mode range, a crossover occurs. At this point, normally 0.8 V and  $V_{CC} - 0.8$  V, the measured offset voltages change.

### COMPARATOR HYSTERESIS

In noisy environments, or when the differential input amplitudes are relatively small or slow moving, adding hysteresis ( $V_{HYST}$ ) to the comparator is often desirable. The transfer function for a comparator with hysteresis is shown in Figure 32. As the input voltage approaches the threshold (0 V in Figure 32) from below the threshold region in a positive direction, the comparator switches from low to high when the input crosses  $+V_{HYST}/2$ . The new switch threshold becomes  $-V_{HYST}/2$ . The comparator remains in the high state until the  $-V_{HYST}/2$  threshold is crossed from below the threshold region in a negative direction. In this manner, noise or feedback output signals centered on the 0 V input cannot cause the comparator to switch states unless it exceeds the region bounded by  $\pm V_{HYST}/2$ .



Figure 32. Comparator Hysteresis Transfer Function

## TYPICAL APPLICATIONS

### ADDING HYSTERESIS

To add hysteresis, see Figure 33; two resistors are used to create different switching thresholds, depending on whether the input signal is increasing or decreasing in magnitude. When the input voltage increases, the threshold is above  $V_{REF}$ , and when the input voltage decreases, the threshold is below  $V_{REF}$ .



Figure 33. Noninverting Comparator Configuration with Hysteresis

The upper input threshold level is given by

$$V_{IN\_HI} = \frac{V_{REF}(R1 + R2)}{R2} \quad (2)$$

Assuming  $R_{LOAD} \gg R2$ ,  $R_{PULLUP}$ .

The lower input threshold level is given by

$$V_{IN\_LO} = \frac{V_{REF}(R1 + R2 + R_{PULLUP}) - V_{CC}R1}{R2 + R_{PULLUP}} \quad (3)$$

The hysteresis is the difference between these voltage levels.

$$V_{HYS} = \frac{V_{REF} \times (R1 \times R_{PULLUP}) + V_{CC} \times (R1 \times R2)}{R2(R2 + R_{PULLUP})} \quad (4)$$

### WINDOW COMPARATOR FOR POSITIVE VOLTAGE MONITORING

When monitoring a positive supply, the desired nominal operating voltage for monitoring is denoted by  $V_M$ ,  $I_M$  is the nominal current through the resistor divider,  $V_{OV}$  is the overvoltage trip point, and  $V_{UV}$  is the undervoltage trip point.

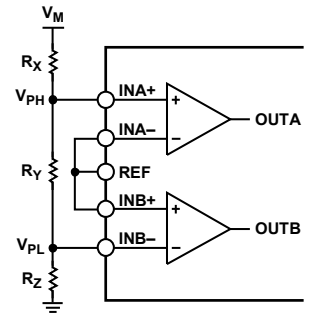


Figure 34. Positive Undervoltage/Overvoltage Monitoring Configuration

Figure 34 illustrates the positive voltage monitoring input connection. Three external resistors,  $R_X$ ,  $R_Y$ , and  $R_Z$  divide the positive voltage for monitoring,  $V_M$ , into the high-side voltage,  $V_{PH}$ , and the low-side voltage,  $V_{PL}$ . The high-side voltage is connected to the  $INA+$  pin and the low-side voltage is connected to the  $INB-$  pin.

To trigger an overvoltage condition, the low-side voltage (in this case,  $V_{PL}$ ) must exceed the  $V_{REF}$  threshold on the  $INB+$  pin. Calculate the low-side voltage,  $V_{PL}$ , by the following:

$$V_{PL} = V_{REF} = V_{OV} \left( \frac{R_Z}{R_X + R_Y + R_Z} \right) \quad (5)$$

In addition,

$$R_X + R_Y + R_Z = V_M / I_M \quad (6)$$

Therefore,  $R_Z$ , which sets the desired trip point for the overvoltage monitor, is calculated as

$$R_Z = \frac{(V_{REF})(V_M)}{(V_{OV})(I_M)} \quad (7)$$

To trigger the undervoltage condition, the high-side voltage,  $V_{PH}$ , must be less than the  $V_{REF}$  threshold on the  $INA-$  pin. The high-side voltage,  $V_{PH}$ , is calculated by

$$V_{PH} = V_{REF} = V_{UV} \left( \frac{R_Y + R_Z}{R_X + R_Y + R_Z} \right) \quad (8)$$

Because  $R_Z$  is already known,  $R_Y$  can be expressed as

$$R_Y = \frac{(V_{REF})(V_M)}{(V_{UV})(I_M)} - R_Z \quad (9)$$

When  $R_Y$  and  $R_Z$  are known,  $R_X$  can be calculated by

$$R_X = (V_M / I_M) - R_Y - R_Z \quad (10)$$

If  $V_M$ ,  $I_M$ ,  $V_{OV}$ , or  $V_{UV}$  changes, each step must be recalculated.

### WINDOW COMPARATOR FOR NEGATIVE VOLTAGE MONITORING

Figure 35 shows the circuit configuration for negative supply voltage monitoring. To monitor a negative voltage, a reference voltage is required to connect to the end node of the voltage divider circuit, in this case, REF.



Figure 35. Negative Undervoltage/Overvoltage Monitoring Configuration

Equation 7, Equation 9, and Equation 10 need some minor modifications. The reference voltage,  $V_{REF}$ , is added to the overall voltage drop; therefore, it must be subtracted from  $V_M$ ,  $V_{UV}$ , and  $V_{OV}$  before using each of them in Equation 7, Equation 9, and Equation 10.

To monitor a negative voltage level, the resistor divider circuit divides the voltage differential level between  $V_{REF}$  and the negative supply voltage into the high-side voltage,  $V_{NH}$ , and the low-side voltage,  $V_{NL}$ . The high-side voltage,  $V_{NH}$ , is connected to  $INA+$ , and the low-side voltage,  $V_{NL}$ , is connected to  $INB-$ .

To trigger an overvoltage condition, the monitored voltage must exceed the nominal voltage in terms of magnitude, and the high-side voltage (in this case,  $V_{NH}$ ) on the  $INA+$  pin must be more negative than ground. Calculate the high-side voltage,  $V_{NH}$ , by using the following formula:

$$V_{NH} = GND = \left[ (V_{REF} - V_{OV}) \left( \frac{R_X + R_Y}{R_X + R_Y + R_Z} \right) \right] + V_{OV} \quad (11)$$

In addition,

$$R_X + R_Y + R_Z = \frac{(V_M - V_{REF})}{I_M} \quad (12)$$

Therefore,  $R_Z$ , which sets the desired trip point for the overvoltage monitor, is calculated by

$$R_Z = \frac{V_{REF}(V_M - V_{REF})}{I_M(V_{REF} - V_{OV})} \quad (13)$$

To trigger an undervoltage condition, the monitored voltage must be less than the nominal voltage in terms of magnitude, and the low-side voltage (in this case,  $V_{NL}$ ) on the  $INB-$  pin must be more positive than ground. Calculate the low-side voltage,  $V_{NL}$ , by the following:

$$V_{NL} = GND = \left[ (V_{REF} - V_{UV}) \left( \frac{R_X}{R_X + R_Y + R_Z} \right) \right] + V_{UV} \quad (14)$$

Because  $R_Z$  is already known,  $R_Y$  can be expressed as follows:

$$R_Y = \frac{V_{REF}(V_M - V_{REF})}{I_M(V_{REF} - V_{UV})} - R_Z \quad (15)$$

When  $R_Y$  and  $R_Z$  are known,  $R_X$  is then calculated by

$$R_X = \frac{(V_M - V_{REF})}{I_M} - R_Y - R_Z \quad (16)$$

### PROGRAMMABLE SEQUENCING CONTROL CIRCUIT

The circuit shown in Figure 36 is used to control power supply sequencing. The delay is set by the combination of the pull-up resistor ( $R_{PULLUP}$ ), the load capacitor ( $C_L$ ), and the resistor divider network.



Figure 36. Programmable Sequencing Control Circuit

Figure 37 shows a simple block diagram for a programmable sequencing control circuit. The application delays the enable signal,  $EN$ , of the external regulators (LDO x) in a linear order when the open-drain signal ( $SEQ$ ) changes from low to high impedance.

The [ADCMP394/ADCMP395/ADCMP396](#) have a defined output state during startup, which prevents any regulator from turning on if  $V_{CC}$  is still below the  $UVLO$  threshold.



Figure 37. Simplified Block Diagram of a Programmable Sequencing Control Circuit



Figure 38. Programmable Sequencing Control Circuit Timing Diagram

When the SEQ signal changes from low to high impedance, the load capacitor,  $C_L$ , starts to charge. The time it takes to charge the load capacitor to the pull-up voltage (in this case,  $V_{REF}$  or  $V_{CC}$ ) is the maximum delay programmable in the circuit. It is recommended to have the threshold within 10% to 90% of the pull-up voltage. Calculate the maximum allowable delay by

$$t_{MAX} = 2.2R_{PULLUP}C_{LOAD} \quad (17)$$

The delay of each output is changed by changing the threshold voltage,  $V1$  to  $V4$ , when the comparator changes its output state.

To calculate the voltage thresholds for the comparator, use the following formulas:

$$V1 = V_{REF} \left( 1 - e^{\frac{-t_1}{R_{PULLUP}C_L}} \right) \quad (18)$$

$$V2 = V_{REF} \left( 1 - e^{\frac{-t_2}{R_{PULLUP}C_L}} \right) \quad (19)$$

$$V3 = V_{REF} \left( 1 - e^{\frac{-t_3}{R_{PULLUP}C_L}} \right) \quad (20)$$

$$V4 = V_{REF} \left( 1 - e^{\frac{-t_4}{R_{PULLUP}C_L}} \right) \quad (21)$$

The threshold voltages can come from a voltage reference or a voltage divider circuit, as shown in Figure 36.

First, determine the allowable current,  $I_{DIV}$ , flowing through the resistor divider. After the value for  $I_{DIV}$  is determined, calculate  $R1$ ,  $R2$ ,  $R3$ ,  $R4$ , and  $R5$  using the following formulas:

$$R_{DIV} = \frac{V_{REF}}{I_{DIV}} = R1 + R2 + R3 + R4 + R5 \quad (22)$$

$$R1 = \frac{V1R_{DIV}}{V_{REF}} \quad (23)$$

$$R2 = \frac{V2R_{DIV}}{V_{REF}} - R1 \quad (24)$$

$$R3 = \frac{V3R_{DIV}}{V_{REF}} - R1 - R2 \quad (25)$$

$$R4 = \frac{V4R_{DIV}}{V_{REF}} - R1 - R2 - R3 \quad (26)$$

$$R5 = R_{DIV} - R1 - R2 - R3 - R4 \quad (27)$$

To create a mirrored voltage sequence, add a resistor ( $R_{MIRROR}$ ) between the pull-up resistor ( $R_{PULLUP}$ ) and the load capacitor ( $C_L$ ) as shown in Figure 39.



Figure 39. Circuit Configuration for a Mirrored Voltage Sequencer

Figure 39 shows the circuit configuration for a mirrored voltage sequencer. When SEQ changes from low to high impedance, the response is similar to Figure 38. When SEQ changes from high to low impedance, the load capacitor ( $C_L$ ) starts to discharge at a rate set by  $R_{MIRROR}$ . The delay of each comparator is dependent on the threshold voltage previously set for  $t_1$  to  $t_4$ . The result is a mirrored power-down sequence.

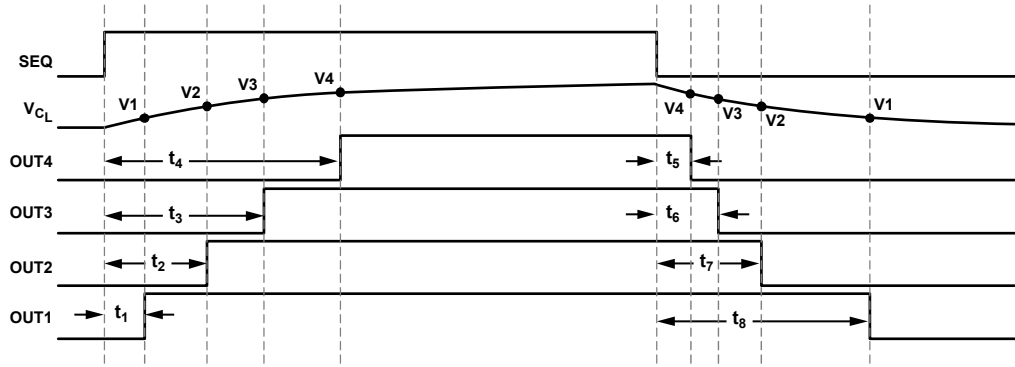


Figure 40. Mirrored Voltage Sequencer Timing Diagram

12209-240

The timing diagram for the mirrored voltage sequencer is shown in Figure 40.

Equation 18 through Equation 21 must account for the additional resistance,  $R_{MIRROR}$ , in the calculations of the voltage thresholds. To calculate these new thresholds, see Equation 28 through Equation 31.

$$V1 = V_{REF} \left( 1 - e^{\frac{-t_1}{(R_{PULLUP} + R_{MIRROR})C_L}} \right) \quad (28)$$

$$V2 = V_{REF} \left( 1 - e^{\frac{-t_2}{(R_{PULLUP} + R_{MIRROR})C_L}} \right) \quad (29)$$

$$V3 = V_{REF} \left( 1 - e^{\frac{-t_3}{(R_{PULLUP} + R_{MIRROR})C_L}} \right) \quad (30)$$

$$V4 = V_{REF} \left( 1 - e^{\frac{-t_4}{(R_{PULLUP} + R_{MIRROR})C_L}} \right) \quad (31)$$

$R_{MIRROR}$  provides the mirrored delay by prolonging the discharge time of the capacitor. The mirrored voltage sequencer uses the same threshold in Equation 28 to Equation 31 in a decreasing order. To calculate the exact value of the mirrored delay time, see Equation 32 through Equation 35.

$$t_5 = -R_{MIRROR}C_L \ln \left( \frac{V4}{V_{REF}} \right) \quad (32)$$

$$t_6 = -R_{MIRROR}C_L \ln \left( \frac{V3}{V_{REF}} \right) \quad (33)$$

$$t_7 = -R_{MIRROR}C_L \ln \left( \frac{V2}{V_{REF}} \right) \quad (34)$$

$$t_8 = -R_{MIRROR}C_L \ln \left( \frac{V1}{V_{REF}} \right) \quad (35)$$

### MIRRORED VOLTAGE SEQUENCER EXAMPLE

To illustrate how the mirrored voltage sequencer works, see Figure 37 and then consider a system that uses a  $V_{REF}$  of 1 V and requires a delay of 50 ms when SEQ changes from low to high impedance, and between each regulator when turning on. These considerations require a rise time of at least 200 ms for the pull-up resistor ( $R_{PULLUP}$ ) and the load capacitor ( $C_L$ ). The sum of the resistance of  $R_{MIRROR}$  and  $R_{PULLUP}$  must be large enough to charge the capacitor longer than the minimum required delay. For a symmetrical mirrored power-down sequence, the value of  $R_{MIRROR}$  must be much larger than  $R_{PULLUP}$ . A 10 k $\Omega$   $R_{PULLUP}$  value limits the pull-down current to 100  $\mu$ A while giving a reasonable value for  $R_{MIRROR}$ . A typical 1  $\mu$ F capacitor together with a 150 k $\Omega$   $R_{MIRROR}$  value gives a value of

$$t_{MAX} = 2.2((160 \times 10^3) \times (1 \times 10^{-6})) = 351 \text{ ms} \quad (36)$$

The threshold voltage required by each comparator is set by Equation 28 to Equation 31. For example,

$$V1 = V_{REF} \left( 1 - e^{\frac{-50 \times 10^{-3}}{160 \times 10^3 \times 1 \times 10^{-6}}} \right)$$

where  $V1 = 268.38 \text{ mV}$ .

Therefore,  $V2 = 464.74 \text{ mV}$ ,  $V3 = 608.39 \text{ mV}$ , and  $V4 = 713.5 \text{ mV}$ .

Next, consider 10  $\mu$ A as the maximum current ( $I_{DIV}$ ) flowing through the resistor divider network. This current gives the total resistance of the divider network ( $R_{DIV}$ ) and the individual resistor values using Equation 22 to Equation 27, resulting in the following:

- $R_{DIV} = 100 \text{ k}\Omega$
- $R1 = 26.84 \text{ k}\Omega \approx 26.7 \text{ k}\Omega$
- $R2 = 19.64 \text{ k}\Omega \approx 19.6 \text{ k}\Omega$
- $R3 = 14.37 \text{ k}\Omega \approx 14.3 \text{ k}\Omega$
- $R4 = 10.51 \text{ k}\Omega \approx 10.5 \text{ k}\Omega$
- $R5 = 28.65 \text{ k}\Omega \approx 28.7 \text{ k}\Omega$

Resistor values from the calculation are nonindustry standard, using industry standard resistor values resulted in a new  $R_{DIV}$  value of 99.8 k $\Omega$ . Due to the discrepancy of the calculated resistor value to the industry standard value, the threshold of each comparator also changed. Calculate the new threshold values by using a simple voltage divider formula:

$$V1 = V_{REF}R1/R_{DIV} \tag{37}$$

where  $V1 = \frac{1V(26.7\text{ k}\Omega)}{99.8\text{ k}\Omega} = 267.54\text{ mV}$ .

Therefore,  $V2 = 463.93\text{ mV}$ ,  $V3 = 607.21\text{ mV}$ , and  $V4 = 712.42\text{ mV}$ .

Because the threshold of each comparator has changed, the time when each comparator changes its output has also changed. Calculate the new delay values for each comparator by using the following equation:

$$t_1 = -C_L(R_{PULLUP} + R_{MIRROR})\ln\left(1 - \frac{V1}{V_{REF}}\right) \tag{38}$$

where  $t_1 = -1\ \mu\text{F}(10\text{ k}\Omega + 150\text{ k}\Omega)\ln\left(1 - \frac{267.54\text{ mV}}{1}\right) = 49.81\text{ ms}$ .

Therefore,  $t_2 = 99.78\text{ ms}$ ,  $t_3 = 149.52\text{ ms}$ , and  $t_4 = 199.4\text{ ms}$ .

To calculate  $t_5$  through  $t_8$ , use Equation 32 to Equation 35:

$$t_5 = -R_{MIRROR}C_L\ln\left(\frac{V4}{V_{REF}}\right)$$

where  $t_5 = -150\text{ k}\Omega \times 1\ \mu\text{F} \times \ln\left(\frac{712.42\text{ mV}}{1}\right) = 50.86\text{ ms}$ .

Therefore,  $t_6 = 74.83\text{ ms}$ ,  $t_7 = 115.2\text{ ms}$ , and  $t_8 = 197.78\text{ ms}$ .

### THRESHOLD AND TIMEOUT PROGRAMMABLE VOLTAGE SUPERVISOR

Figure 41 shows a circuit configuration for a programmable threshold and timeout circuit. The timeout,  $t_{RESET}$ , defines the duration that the input voltage ( $V_{IN}$ ) must be kept above the threshold voltage to toggle the RESET signal, preventing the device from operating when  $V_{IN}$  is not stable. If  $V_{IN}$  falls below the threshold voltage, the  $\overline{\text{RESET}}$  signal toggles quickly.



Figure 41. Programmable Threshold and Timeout Circuit



Figure 42. Threshold and Timeout Programmable Voltage Supervisor Timing Diagram

During startup, the ADCMP394/ADCMP395/ADCMP396 guarantee a low output state when  $V_{CC}$  is still below the UVLO threshold, preventing the voltage supervisor from toggling.

When  $V_{IN}$  reaches the threshold set by the resistor divider ( $R1$  and  $R2$ ) and  $V_{REF}$ ,  $\text{OUT1}$  changes from low to high and starts to charge the timeout capacitor ( $C_T$ ). If  $V_{IN}$  is kept above the threshold voltage and the voltage in  $C_T$  reaches  $V_{REF}$ ,  $\text{OUT2}$  toggles. If  $V_{IN}$  falls below the threshold voltage while  $C_T$  is charging, the timeout capacitor quickly discharges, preventing  $\text{OUT2}$  from toggling while  $V_{IN}$  is not stable.

In the condition that  $V_{IN}$  is tied to  $V_{CC}$ , the circuit operates when  $V_{CC}$  is more than the minimum operating voltage.

The threshold voltage ( $V_{TH}$ ) is configured by changing the resistor divider or  $V_{REF}$ . Calculate the threshold voltage by

$$V_{TH} = V_{REF}\left(1 + \frac{R1}{R2}\right) \tag{39}$$

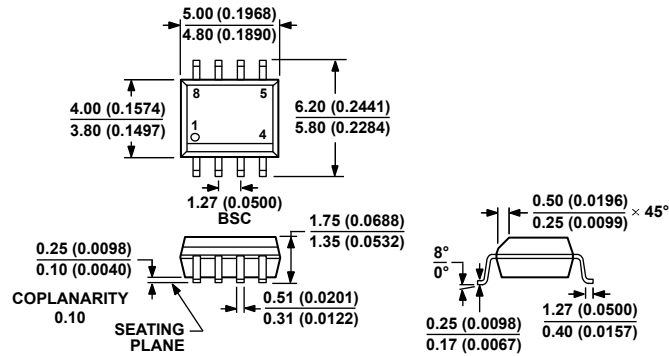
Timeout is adjusted by changing the values of the pull-up resistor or the timeout capacitor. To set the timeout value, determine the allowable current flowing through  $R_{PULLUP}$ ,  $I_{PULLUP}$ . When  $I_{PULLUP}$  is known, calculate  $R_{PULLUP}$  and  $C_T$  by the following formulas:

$$R_{PULLUP} = V_{CC}/I_{PULLUP} \tag{40}$$

$$C_T = \frac{-t_{RESET}}{R_{PULLUP}\ln\left(1 - \frac{V_{REF}}{V_{CC}}\right)} \tag{41}$$



OUTLINE DIMENSIONS

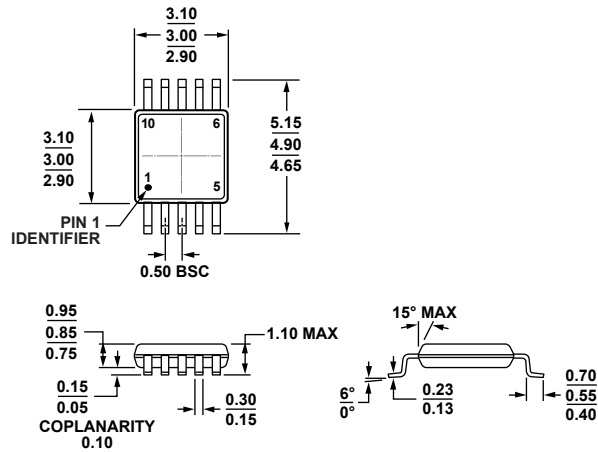


COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 43. 8-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

012407-A



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 44. 10-Lead Mini Small Outline Package [MSOP] (RM-10)

Dimensions shown in millimeters

081708-A



COMPLIANT TO JEDEC STANDARDS MS-012-AC  
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 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 45. 16-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-16)

Dimensions shown in millimeters and (inches)

069006-A

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
ADCMP394ARZ	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADCMP394ARZ-RL7	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADCMP395ARMZ	-40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	LQ4
ADCMP395ARMZ-RL7	-40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	LQ4
ADCMP396ARZ	-40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16	
ADCMP396ARZ-RL7	-40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16	

<sup>1</sup> Z = RoHS Compliant Part.



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#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.