IGLOO2 FPGA and SmartFusion2 SoC FPGA

DS0451 Datasheet

Microsemi

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1. Introduction

Microsemi's mainstream SmartFusion®2 SoC and IGLOO®2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated mathblocks, multiple embedded memory blocks, and high-performance SERDES communications interfaces on a single chip. Both families benefit from low power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to five MB of embedded RAM, up to 16 SERDES lanes, and up to four PCI Express Gen 2 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 devices integrate an entire low power real time Microcontroller Subsystem with a rich set of Industry standard peripherals including Ethernet, USB, and CAN, while IGLOO2 devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

2. Device Status

For more information on device status, refer to the "Datasheet Categories" section on page 135.

Table 1 • **IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status**

Design Security Device Densities	**Status**
005	Production
010, 010T	Production
025, 025T	Production
050, 050T	Production
060, 060T	Preliminary
090, 090T	Production
150, 150T	Production
Data Security Device Densities	**Status**
005S	Production
010TS	Production
025TS	Production
050TS	Production
060TS	Preliminary
090TS	Production
150TS	Production

3. Product Briefs and Pin Descriptions

The product brief and pin descriptions are published separately:

IGLOO2 Product Brief

IGLOO2 Pin Descriptions

SmartFusion2 SoC FPGA Product Brief

SmartFusion2 Pin Descriptions

4. General Specifications

4.1 Operating Conditions

Stresses beyond those listed in Table 2 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in Table 2 is not implied.

Table 2 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits		Units	Notes
		Min	Max		
VDD	DC core supply voltage. Must always power this pin.	–0.3	1.32	V	
VPP	Power supply for charge pumps (for normal operation and programming). Must always power this pin.	–0.3	3.63	V	
MSS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	–0.3	3.63	V	
HPMS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	–0.3	3.63	V	
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	–0.3	3.63	V	
PLL0_PLL1_MSS_MDDR_VDDA	Analog power pad for MDDR PLL	–0.3	3.63	V	
PLL0_PLL1_HPMS_MDDR_VDDA	Analog power pad for MDDR PLL	–0.3	3.63	V	
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0–5	–0.3	3.63	V	
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	–0.3	3.63	V	
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL lane0 to lane3. This is a +2.5 V SERDES internal PLL supply.	–0.3	2.75	V	
SERDES_[01]_L[0123]_VDDAIO	TX/RX analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply.	–0.3	1.32	V	
SERDES_[01]_VDD	PCIe®/PCS power supply	–0.3	1.32	V	
VDDIx	DC FPGA I/O buffer supply voltage for MSIO I/O Bank	–0.3	3.63	V	
	DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O Banks	–0.3	2.75	V	
VI	I/O Input voltage for MSIO I/O Bank	–0.3	3.63	V	
	I/O Input voltage for MSIOD/DDRIO I/O Bank	–0.3	2.75	V	
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	–0.3	3.63	V	
T_{STG}	Storage temperature	–65	150	°C	*

Table 2 • Absolute Maximum Ratings (continued)

Symbol	Parameter	Limits		Units	Notes
		Min	Max		
T_J	Junction temperature	–55	125	°C	

*Note: *For flash programming and retention maximum limits, refer to Table 4 on page 14. For recommended operating conditions, refer to Table 3 on page 13.*

Table 3 • Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
T_J	Operating Junction Temperature	Commercial	0	25	85	°C	
		Industrial	–40	25	100	°C	
	Programming Junction Temperatures	Commercial	0	25	85	°C	
		Industrial	–40	25	100	°C	1
VDD	DC core supply voltage. Must always power this pin.		1.14	1.2	1.26	V	
VPP	Power supply for charge pumps (for normal operation and programming) for the 005, 010, 025, 050 devices	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
VPP	Power supply for charge pumps (for normal operation and programming) for the 090 and 150 devices	3.3 V range	3.15	3.3	3.45	V	
MSS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
HPMS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PLL0_PLL1_MSS_MDDR_VDDA	Analog power pad for MDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PLL0_PLL1_HPMS_MDDR_VDDA	Analog power pad for MDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0 to PLL5	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	2.5 V range	2.375	2.5	2.625	V	2
		3.3 V range	3.15	3.3	3.45	V	2
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL Lane0 to Lane3. This is a +2.5 V SERDES internal PLL supply.		2.375	2.5	2.625	V	
SERDES_[01]_L[0123]_VDDAIO	TX/RX analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply.		1.14	1.2	1.26	V	
SERDES_[01]_VDD	PCIe/PCS power supply		1.14	1.2	1.26	V	

Notes:

1. *Programming at Industrial temperature range is available only with VPP=3.3V.*
2. *Power supply ramps must all be strictly monotonic, without plateaus.*

Table 3 • Recommended Operating Conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
VDDIx	1.2 V DC supply voltage		1.14	1.2	1.26	V	
	1.5 V DC supply voltage		1.425	1.5	1.575	V	
	1.8 V DC supply voltage		1.71	1.8	1.89	V	
	2.5 V DC supply voltage		2.375	2.5	2.625	V	
	3.3 V DC supply voltage		3.15	3.3	3.45	V	
	LVDS differential I/O		2.375	2.5	3.45	V	
	B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O		2.375	2.5	2.625	V	
	LVPECL differential I/O		3.15	3.3	3.45	V	
VREFx	Reference voltage supply for FDDR (Bank0) and MDDR (Bank5)		0.49 × VDDIx	0.5 × VDDIx	0.51 × VDDIx	V	
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	

Notes:

1. *Programming at Industrial temperature range is available only with VPP=3.3V.*
2. *Power supply ramps must all be strictly monotonic, without plateaus.*

Table 4 • FPGA Operating Limits

Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Digest Temperature	Digest Cycles	Retention (Biased/ Unbiased)	Notes
Commercial	FPGA	Min T_J = 0°C Max T_J = 85°C	Min T_J = 0°C Max TJ = 85°C	500	Min T_J = 0°C Max T_J = 85°C	2000	20 years	
Industrial	FPGA	Min T_J = –40°C Max T_J = 100°C	Min T_J = –40°C Max T_J = 100°C	500	Min T_J = –40°C Max T_J = 100°C	2000	20 years	*

*Note: *Programming at Industrial temperature range is available only with VPP = 3.3 V*

Table 5 • Embedded Operating Flash Limits

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Commercial	Embedded flash	Min T_J = 0°C Max T_J = 85°C	Min T_J = 0°C Max T_J = 85°C	< 1000 cycles per page, up to two million cycles per eNVM Array	20 years
			Min T_J = 0°C Max T_J = 85°C	< 10000 cycles per page, up to 20 million cycles per eNVM Array	10 years
Industrial	Embedded flash	Min T_J = –40°C Max T_J = 100°C	Min T_J = –40°C Max T_J = 100°C	< 1000 cycles per page, up to two million cycles per eNVM Array	20 years
			Min T_J = –40°C Max T_J = 100°C	< 10000 cycles per page, up to 20 million cycles per eNVM Array	10 years

Table 6 • **Device Storage Temperature and Retention**

Product Grade	Storage Temperature (Tstg)	Retention
Commercial	Min T_J = 0°C Max T_J = 85°C	20 years
Industrial	Min T_J = –40°C Max T_J = 100°C	20 years

4.2 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to –1.0 V for no longer than 10% or the period. The current during the transition must not exceed 100mA.

For AC signals, the input signal may overshoot during transitions to VCCI + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100mA.

Note: The above specification does not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

4.3 Thermal Characteristics

4.3.1 Introduction

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 7 • **Package Thermal Resistance**

Product M2GL/M2S	θ_{JA} Still Air	θ_{JA} 1.0 m/s	θ_{JA} 2.5 m/s	θ_{JB}	θ_{JC}	Units
005						
FG484	19.36	15.81	14.63	9.74	5.27	°C/W
VF256	41.30	38.16	35.30	28.41	3.94	°C/W
VF400	20.19	16.94	15.41	8.86	4.95	°C/W
TQ144	42.80	36.80	34.50	37.20	10.80	°C/W
010						
FG484	18.22	14.83	13.62	8.83	4.92	°C/W
VF256	37.36	34.26	31.45	24.84	7.89	°C/W
VF400	19.40	15.75	14.22	8.11	4.22	°C/W
TQ144	38.60	32.60	30.30	31.80	8.60	°C/W
025						
FG484	17.03	13.66	12.45	7.66	4.18	°C/W
VF256	33.85	30.59	27.85	21.63	6.13	°C/W
VF400	18.36	14.89	13.36	7.12	3.41	°C/W
FCS325	29.17	24.87	23.12	14.44	2.31	°C/W
050						
FG484	15.29	12.19	10.99	6.27	3.24	°C/W
FG896	14.70	12.50	10.90	7.20	4.90	°C/W
VF400	17.53	14.17	12.63	6.32	2.81	°C/W
FCS325	27.38	23.18	21.41	12.47	1.59	°C/W
060						
FG484	15.40	12.06	10.85	6.14	3.15	°C/W
FG676	15.49	12.21	11.06	7.07	3.87	°C/W
VF400	17.45	14.01	12.47	6.22	2.69	°C/W
FCS325	27.03	22.91	21.25	12.33	1.54	°C/W
090						
FG484	14.64	11.37	10.16	5.43	2.77	°C/W
FG676	14.52	11.19	10.37	6.17	3.24	°C/W
FCS325	26.63	22.26	20.13	14.24	2.50	°C/W
150						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W
FCS536	15.01	12.06	10.76	3.69	1.55	°C/W
FCV484	16.21	13.11	11.84	6.73	0.10	°C/W

4.3.2 Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution, but it is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using EQ 4.

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where

θ_{JA} = 14.7°C/W (taken from Table 7 on page 16).

T_A = 85°C

$$\text{Maximum Power Allowed} = \frac{100°C - 85°C}{14.7°C/W} = 1.088\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

4.3.3 Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

4.3.4 Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

5. Power Consumption

5.1 Quiescent Supply Current

Table 8 • **Quiescent Supply Current Characteristics**

Power Supplies/Blocks	Modes and Configurations		Notes
	Non-Flash*Freeze Mode	Flash*Freeze Mode	
FPGA Core	On	Off	
VDD / SERDES_[01]_VDD	On	On	1
VPP / VPPNVM	On	On	
HPMS_MDDR_PLL_VDDA / FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA / PLL0_PLL1_HPMS_MDDR_VDDA	0 V	0 V	
SERDES_[01]_PLL_VDDA	0 V	0 V	3
SERDES_[01]_L[0123]_VDDAPLL / VDD_2V5	On	On	3
SERDES_[01]_L[0123]_VDDAIIO	On	On	3

Table 8 • Quiescent Supply Current Characteristics (continued)

VDDIx	On	On	2, 4
VREFx	On	On	
MSSDDR CLK	32 kHz	32 kHz	
RAM	On	Sleep state	
System Controller	50 MHz	50 MHz	
50 MHz Oscillator (enable/disable)	Enable	Disabled	
1 MHz Oscillator (enable/disable)	Disabled	Disabled	
Crystal Oscillator (enable/disable)	Disabled	Disabled	

Notes:

1. *SERDES_[01]_VDD Power Supply is shorted to VDD.*
2. *VDDIx has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate VDDI Bank supplies. For details on bank power supplies, refer to the "Recommendation for Unused Bank Supplies" table in the SmartFusion2 Board Design Guidelines and IGLOO2 Board Design Guidelines application notes.*
3. *SERDES and DDR blocks to be unused.*
4. *No Differential (that is to say, LVDS) I/O's or ODT attributes to be used.*

Table 9 • SmartFusion2 and IGLOO2 Quiescent Supply Current – Typical Process

Parameter	Modes	Conditions	005 VDD=1.2 V	010 VDD=1.2 V	025 VDD=1.2 V	050 VDD=1.2 V	090 VDD=1.2 V	150 VDD=1.2 V	Units
IDC1	Non-Flash*Freeze	Typical (T_J = 25°C)	5.4	6.6	8.6	11.4	15.0	21.7	mA
		Commercial (T_J = 85°C)	17.4	25.0	36.4	52.3	72.8	112.2	mA
		Industrial (T_J = 100°C)	25.1	36.6	54.0	78.1	109.4	169.4	mA
IDC2	Flash*Freeze	Typical (T_J = 25°C)	1.6	2.2	2.8	3.2	4.2	5.2	mA
		Commercial (T_J = 85°C)	10.8	15.2	19.6	21.8	29.0	35.6	mA
		Industrial (T_J = 100°C)	16.6	23.4	30.1	33.6	44.7	54.8	mA

Table 10 • SmartFusion2 and IGLOO2 Quiescent Supply Current – Worst-Case Process

Parameter	Modes	Conditions	005 VDD=1.26 V	010 VDD=1.26 V	025 VDD=1.26 V	050 VDD=1.26 V	090 VDD=1.26 V	150 VDD=1.26 V	Units
IDC1	Non-Flash*Freeze	Commercial (T_J= 85°C)	32.2	47.2	69.7	101.0	141.5	219.2	mA
		Industrial (T_J = 100°C)	47.5	70.4	104.9	152.6	214.6	333.6	mA
IDC2	Flash*Freeze	Commercial (T_J = 85°C)	21.5	30.3	39.1	43.6	58.0	71.1	mA
		Industrial (T_J = 100°C)	33.2	46.7	60.2	67.1	89.3	109.6	mA

5.2. Programming Currents

The tables below represent programming, verify and Inrush currents for SmartFusion2 SoC and IGLOO2 FPGA devices.

Table 11 • **Currents During Program Cycle, 0°C < = Tj <= 85°C – Typical Process**

Power Supplies	Voltage (V)	005	010	025	050	090	150	Units	Notes
VDD	1.26	46	53	55	58	42	52	mA	
VPP	3.46	8	11	6	10	12	12	mA	
VPPNVM	3.46	1	2	2	3	3	–	mA	*
VDDI	2.62	31	16	17	1	12	81	mA	
	3.46	62	31	36	1	17	84	mA	
Number of banks	–	7	8	8	10	9	19	–	
*Note: *VPP and VPPNVM are internally shorted.*									

Table 12 • **Currents During Verify Cycle, 0°C <= Tj <= 85°C – Typical Process**

Power Supplies	Voltage (V)	005	010	025	050	090	150	Units	Notes
VDD	1.26	44	53	55	58	41	51	mA	
VPP	3.46	6	5	3	15	11	12	mA	
VPPNVM	3.46	1	0	0	1	1	–	mA	*
VDDI	2.62	31	16	17	1	11	81	mA	
	3.46	61	32	36	1	17	84	mA	
Number of banks	–	7	8	8	10	9	19	–	
*Note: *VPP and VPPNVM are internally shorted.*									

Table 13 • **Inrush Currents at Power up, –40°C <= Tj <= 100°C – Typical Process**

Power Supplies	Voltage (V)	005	010	025	050	090	150	Units
VDD	1.26	25	32	38	48	77	109	mA
VPP	3.46	33	49	36	180	36	51	mA
VDDI	2.62	134	141	161	187	272	388	mA
Number of banks	–	7	8	8	10	9	19	–

6. Average Fabric Temperature and Voltage Derating Factors

Table 14 • **Average Temperature and Voltage Derating Factors for Fabric Timing Delays**
Normalized to T_J = 85°C, Worst-case VDD = 1.14 V

Array Voltage VDD (V)	Junction Temperature (°C)					
	–40°C	**0°C**	**25°C**	**70°C**	**85°C**	**100°C**
1.14	0.83	0.89	0.92	0.98	1.00	1.02
1.2	0.75	0.80	0.83	0.89	0.91	0.93
1.26	0.69	0.73	0.76	0.81	0.83	0.85

7. Timing Model

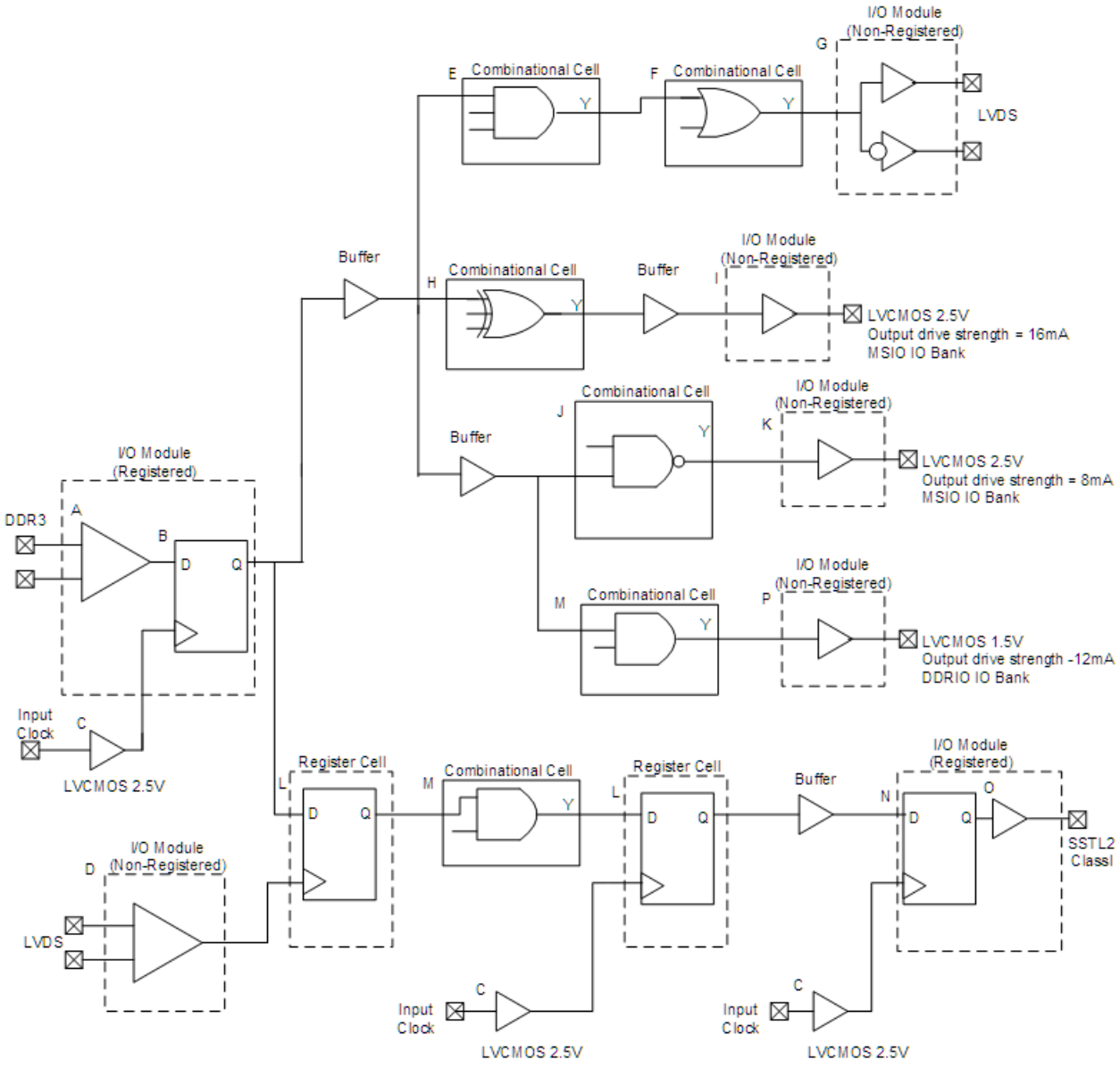

***Figure 1* • Timing Model**

Table 15 • **Timing Model Parameters**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Index	Parameter	Description	Speed Grade –1	Units	For More Information
A	t_{PY}	Propagation delay of DDR3 Receiver	1.605	ns	Refer to page 58
B	t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.16	ns	Refer to page 83
	t_{ISUD}	Setup Time of the Input Data Register	0.357	ns	Refer to page 83
C	t_{RCKH}	Input High Delay for Global Clock	1.53	ns	Refer to page 90
	t_{RCKL}	Input Low Delay for Global Clock	0.897	ns	Refer to page 90
D	t_{PY}	Input Propagation Delay of LVDS Receiver	2.774	ns	Refer to page 66
E	t_{DP}	Propagation Delay of a three-input AND Gate	0.198	ns	Refer to page 87
F	t_{DP}	Propagation Delay of an OR Gate	0.179	ns	Refer to page 87
G	t_{DP}	Propagation Delay of an LVDS Transmitter	2.136	ns	Refer to page 66
H	t_{DP}	Propagation Delay of a three-input XOR Gate	0.241	ns	Refer to page 87
I	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 16 mA on the MSIO Bank	2.412	ns	Refer to page 35
J	t_{DP}	Propagation Delay of a two-input NAND Gate	0.179	ns	Refer to page 87
K	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 8 mA on the MSIO Bank	2.309	ns	Refer to page 35
L	t_{CLKQ}	Clock-to-Q of the Data Register	0.108	ns	Refer to page 89
	t_{SUD}	Setup Time of the Data Register	0.254	ns	Refer to page 89
M	t_{DP}	Propagation Delay of a two-input AND Gate	0.179	ns	Refer to page 87
N	t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.263	ns	Refer to page 80
	t_{OSUD}	Setup Time of the Output Data Register	0.19	ns	Refer to page 80
O	t_{DP}	Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank	2.055	ns	Refer to page 52
P	t_{DP}	Propagation Delay of LVCMOS 1.5 V Transmitter, Drive strength of 12 mA, fast slew on the DDRIO Bank	3.316	ns	Refer to page 41

8. User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA Families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the "I/Os" section of the *IGLOO2 FPGA Fabric Architecture User Guide* or the *SmartFusion2 FPGA Fabric Architecture User Guide*.

8.1 Input Buffer and AC Loading

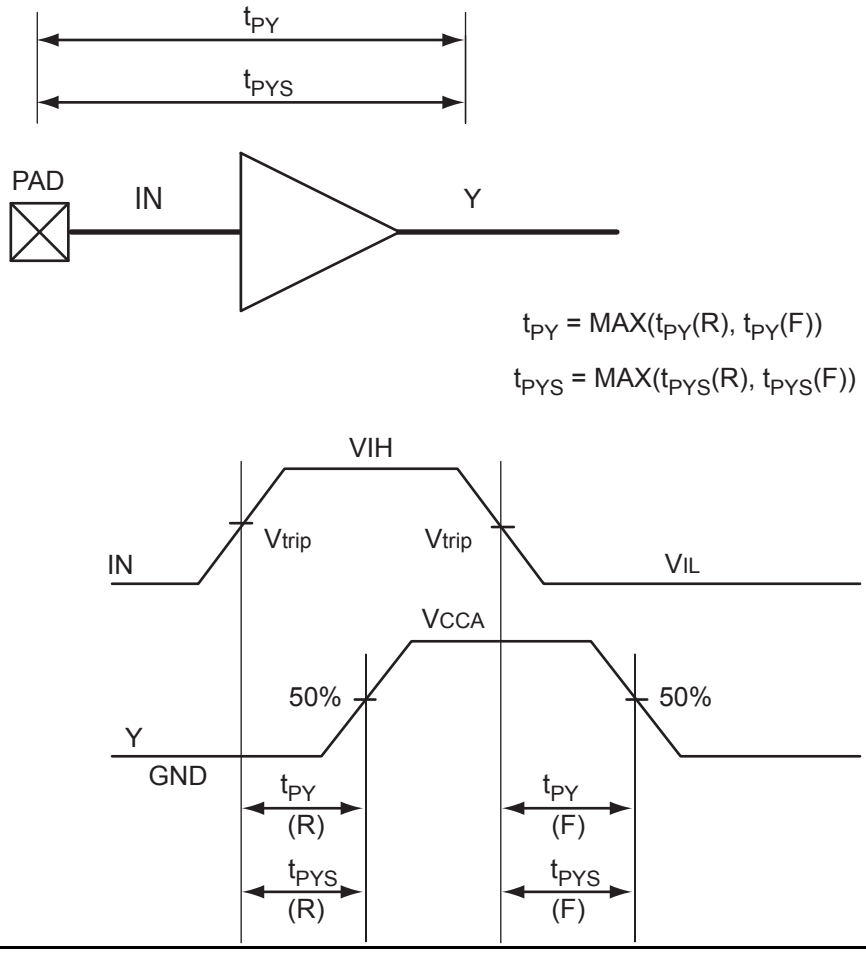

***Figure 2* • Input Buffer AC Loading**

8.2. Output Buffer and AC Loading

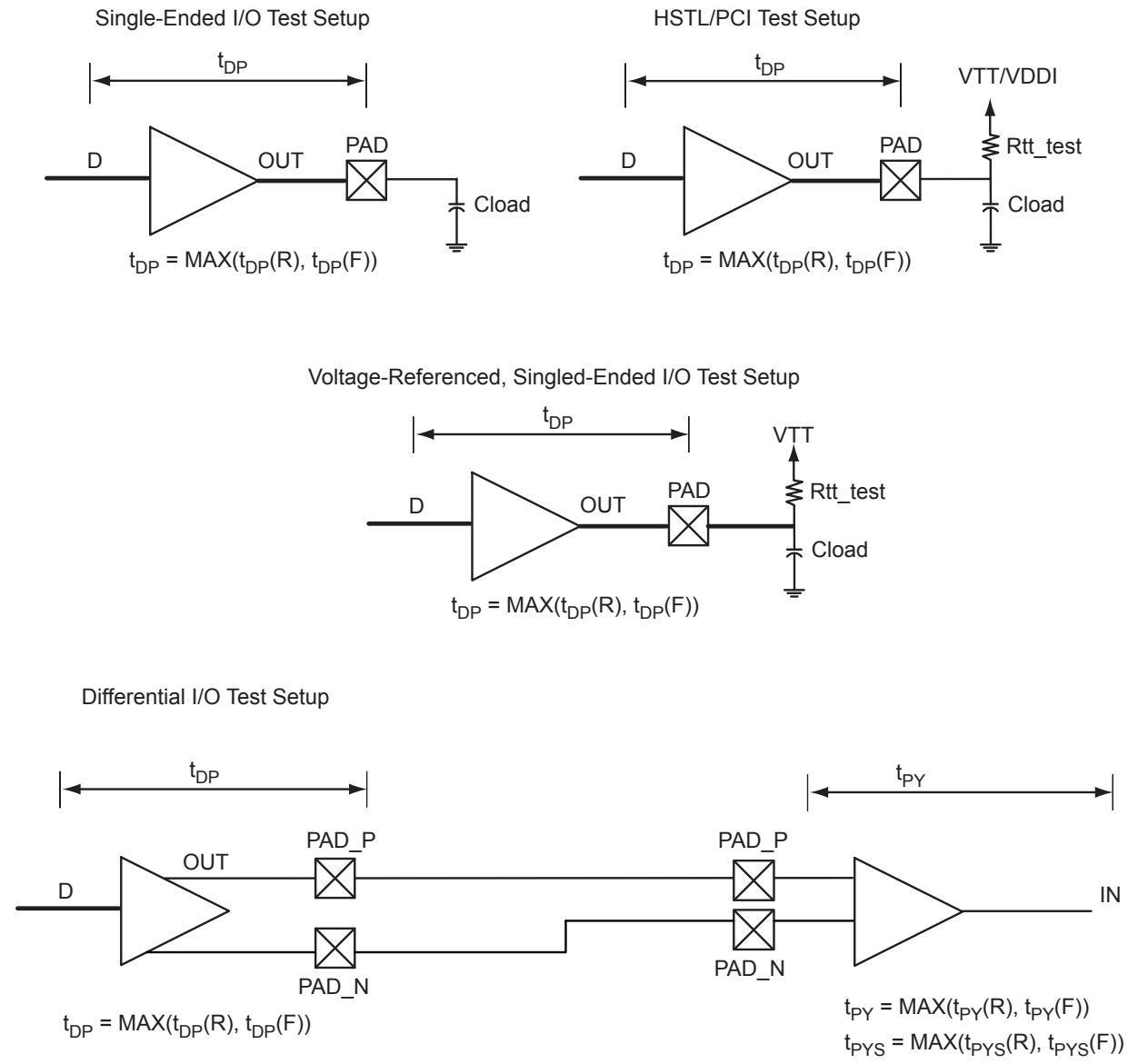

***Figure 3* • Output Buffer AC Loading**

8.3. Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point shown in Figure 4.

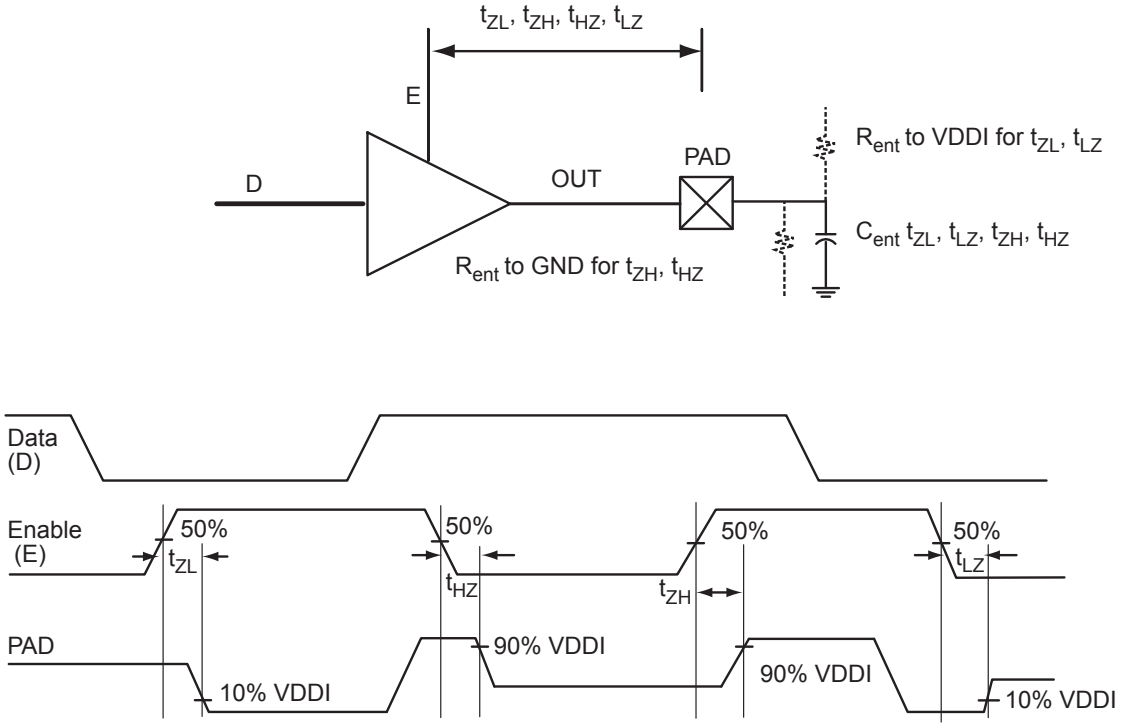

***Figure 4* • Tristate Buffer for Enable Path Test Point**

8.4 I/O Speeds

Table 16 • **Maximum Data Rate Summary Table for Worst-Case Industrial Conditions**

Single-Ended I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
PCI 3.3 V	630	–	–	Mbps
LVTTL 3.3 V	600	–	–	Mbps
LVCMOS 3.3 V	600	–	–	Mbps
LVCMOS 2.5 V	410	420	400	Mbps
LVCMOS 1.8 V	295	400	400	Mbps
LVCMOS 1.5 V	160	220	235	Mbps
LVCMOS 1.2 V	120	160	200	Mbps
LPDDR-LVCMOS 1.8 V Mode	–	–	400	Mbps
Voltage-Referenced I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LPDDR	–	–	400	Mbps
HSTL1.5 V	–	–	400	Mbps
SSTL 2.5 V	510	700	400	Mbps
Voltage-Referenced I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
SSTL 1.8 V	–	–	667	Mbps
SSTL 1.5 V	–	–	667	Mbps
Differential I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LVPECL (input only)	900	–	–	Mbps
LVDS 3.3 V	535	700	–	Mbps
LVDS 2.5 V	535	700	–	Mbps
RSDS	520	700	–	Mbps
BLVDS	500	–	–	Mbps
MLVDS	500	–	–	Mbps
Mini-LVDS	520	700	–	Mbps
Note: Refer to the individual I/O standards for operating conditions.				

Table 17 • **Maximum Frequency Summary Table for Worst-Case Industrial Conditions**

Single-Ended I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
PCI 3.3 V	315	–	–	MHz
LVTTL 3.3 V	300	–	–	MHz
LVCMOS 3.3 V	300	–	–	MHz
LVCMOS 2.5 V	205	210	200	MHz
LVCMOS 1.8 V	147.5	200	200	MHz
LVCMOS 1.5 V	80	110	118	MHz
LVCMOS 1.2 V	60	80	100	MHz
LPDDR– LVCMOS 1.8 V mode	–	–	200	MHz

Table 17 • **Maximum Frequency Summary Table for Worst-Case Industrial Conditions (continued)**

Voltage-Referenced I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LPDDR	–	–	200	MHz
HSTL1.5 V	–	–	200	MHz
SSTL 2.5 V	255	350	200	MHz
SSTL 1.8 V	–	–	334	MHz
SSTL 1.5 V	–	–	334	MHz
Differential I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LVPECL (input only)	450	–	–	MHz
LVDS 3.3 V	267.5	350	–	MHz
LVDS 2.5 V	267.5	350	–	MHz
RSDS	260	350	–	MHz
BLVDS	250	–	–	MHz
MLVDS	250	–	–	MHz
Mini-LVDS	260	350	–	MHz
Note: Refer to the individual I/O standards for operating conditions.				

8.5 Detailed I/O Characteristics

Table 18 • **Input Capacitance**

Symbol	Definition	Minimum	Maximum	Units
C_{IN}	Input capacitance	–	10	pF

Table 19 • **I/O Weak Pull-Up/Pull-Down Resistances for DDRIO I/O Bank**
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

	DDRIO I/O Bank				
	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		
VDDI Domain	Min	Max	Min	Max	Notes
2.5 V	10K	15.1K	9.98K	15.3K	1, 2
1.8 V	10.3K	16.2K	10.3K	16.6K	1, 2
1.5 V	10.6K	17.2K	10.6K	17.9K	1, 2
1.2 V	11.1K	19.3K	11.2K	20.9K	1, 2

Notes:

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN)*

Table 20 • **I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank**
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

	MSIO I/O Bank				
	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		
VDDI Domain	Min	Max	Min	Max	Notes
3.3 V	9.9K	14.5K	9.98K	14.9K	–
2.5 V	10K	15K	10.1K	15.6K	1, 2
1.8 V	10.4K	16.2K	10.4K	17.3K	1, 2
1.5 V	10.7K	17.3K	10.8K	18.9K	1, 2
1.2 V	11.3K	19.7K	11.5K	22.7K	1, 2

Notes:

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN)*

Table 21 • I/O Weak Pull-Up/Pull-Down Resistances for MSIOD I/O Bank
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

	MSIOD I/O Bank				
	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		
VDDI Domain	Min	Max	Min	Max	Notes
2.5 V	9.6K	14.1K	9.5K	13.9K	1, 2
1.8 V	9.7K	14.7K	9.7K	14.5K	1, 2
1.5 V	9.9K	15.3K	9.8K	15K	1, 2
1.2 V	10.3K	16.7K	10K	16.2K	1, 2

Notes:

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN)*

Table 22 • Schmitt Trigger Input Hysteresis
Hysteresis Voltage Value for Schmitt Trigger Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (Typical, unless otherwise noted)
3.3 V LVTTL / LVCMOS / PCI / PCI-X	0.05 × VDDI (Worst-case)
2.5 V LVCMOS	0.05 × VDDI (Worst-case)
1.8 V LVCMOS	0.1 × VDDI (Worst-case)
1.5 V LVCMOS	60 mV
1.2 V LVCMOS	20 mV

8.6 Single-Ended I/O Standards

8.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

8.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

8.6.2.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 23 • LVTTL/LVCMOS 3.3 V DC Voltage Specification (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	
LVTTL/LVCMOS 3.3 V DC Input Voltage Specification							
VIH (DC)	DC input logic High		2.0	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.8	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**	**Notes**
LVCMOS 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI – 0.4	–	–	V	*
VOL	DC output logic Low		–	–	0.4	V	*
LVTTL 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	
VOL	DC output logic Low		–	–	0.4	V	
*Note: * The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.*							

Table 24 • LVTTL/LVCMOS 3.3 V AC Specifications (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVTTL/LVCMOS 3.3 V Maximum Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	600	Mbps
LVTTL/LVCMOS 3.3 V AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	1.4	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

Table 25 • LVTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications

Output Drive Selection	VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank				
2 mA	VDDI – 0.4	0.4	2	2
4 mA	VDDI – 0.4	0.4	4	4
8 mA	VDDI – 0.4	0.4	8	8
12 mA	VDDI – 0.4	0.4	12	12
16 mA	VDDI – 0.4	0.4	16	16
20 mA	VDDI – 0.4	0.4	20	20
Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.				

8.6.2.2 AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 3.0 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 26 • LVTTL/LVCMOS 3.3 V Receiver Characteristics
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		Speed Grade				
		–1	Std	–1	Std	
LVTTL/LVCMOS 3.3 V (for MSIO I/O Bank)	None	2.262	2.663	2.289	2.695	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 27 • **LVTTL/LVCMOS 3.3 V Transmitter Characteristics**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

Output Drive Selection	Slew Control	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}*		t_{LZ}*		Units
		Speed Grade										
		–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
LVTTL/LVCMOS 3.3 V (for MSIO I/O Bank)												
2 mA	Slow	3.192	3.755	3.47	4.083	2.969	3.494	1.856	2.183	3.337	3.926	ns
4 mA	Slow	2.331	2.742	2.673	3.145	2.526	2.973	3.034	3.569	4.451	5.236	ns
8 mA	Slow	2.135	2.511	2.33	2.741	2.297	2.703	4.532	5.331	4.825	5.676	ns
12 mA	Slow	2.052	2.414	2.107	2.479	2.162	2.544	5.75	6.764	5.445	6.406	ns
16 mA	Slow	2.062	2.425	2.072	2.438	2.145	2.525	5.993	7.05	5.625	6.618	ns
20 mA	Slow	2.148	2.527	1.999	2.353	2.088	2.458	6.262	7.367	5.876	6.913	ns

*Note: *Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.*

8.6.3 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-5A.

8.6.3.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 28 • **LVCMOS 2.5 V DC Voltage Specification**

Symbol	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVCMOS 2.5 V DC Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
LVCMOS 2.5 V DC Input Voltage Specification							
VIH (DC)	DC input logic High (for MSIOD and DDRIO I/O Banks)		1.7	–	2.625	V	
VIH (DC)	DC input logic High (for MSIO I/O Bank)		1.7	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.7	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVCMOS 2.5 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI – 0.4	–	–	V	*
VOL	DC output logic Low		–	–	0.4	V	*
*Note: *The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.*							

Table 29 • LVCMOS 2.5 V AC Specifications

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 2.5 V AC Minimum and Maximum Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	400	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	410	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	420	Mbps
LVCMOS 2.5 V AC Calibrated Impedance Option						
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)		–	75, 60, 50, 33, 25, 20	–	Ω
LVCMOS 2.5 V AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	1.2	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

Table 30 • LVCMOS 2.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (With Software Default Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	VDDI – 0.4	0.4	2	2
4 mA	4 mA	4 mA	VDDI – 0.4	0.4	4	4
6 mA	6 mA	6 mA	VDDI – 0.4	0.4	6	6
8 mA	8 mA	8 mA	VDDI – 0.4	0.4	8	8
12 mA	12 mA	12 mA	VDDI – 0.4	0.4	12	12
16 mA	N/A	16 mA	VDDI – 0.4	0.4	16	16

Note: For board design considerations, output slew rates extraction, detailed output buffer resistances and I/V Curve use the corresponding IBIS models located at: www.microsemi.com/soc/download/ibis/default.aspx.

8.6.3.2 AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 31 • LVCMOS 2.5 V Receiver Characteristics
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		
		Speed Grade				
		–1	Std	–1	Std	Units
LVCMOS 2.5 V (for DDRIO I/O Bank)	None	1.823	2.145	1.932	2.274	ns
LVCMOS 2.5 V (for MSIO I/O Bank)	None	2.486	2.925	2.495	2.935	ns
LVCMOS 2.5 V (for MSIOD I/O Bank)	None	2.29	2.694	2.305	2.712	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 32 • **LVCMOS 2.5 V Transmitter Characteristics**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

Output Drive Selection	Slew Control	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}*		t_{LZ}*		Units
		Speed Grade										
		–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
LVCMOS 2.5 V (for DDRIO I/O Bank)												
2 mA	Slow	3.657	4.302	3.393	3.991	3.675	4.323	3.894	4.582	3.552	4.18	ns
	Medium	3.374	3.97	3.139	3.693	3.396	3.995	3.635	4.277	3.253	3.828	ns
	Medium fast	3.239	3.811	3.036	3.572	3.261	3.836	3.519	4.141	3.128	3.681	ns
	Fast	3.224	3.793	3.029	3.563	3.246	3.818	3.512	4.132	3.119	3.67	ns
4 mA	Slow	3.095	3.641	2.705	3.182	3.088	3.633	4.738	5.575	4.348	5.116	ns
	Medium	2.825	3.324	2.488	2.927	2.823	3.321	4.492	5.285	4.063	4.781	ns
	Medium fast	2.701	3.178	2.384	2.804	2.698	3.173	4.364	5.135	3.945	4.642	ns
	Fast	2.69	3.165	2.377	2.796	2.687	3.161	4.359	5.129	3.94	4.636	ns
6 mA	Slow	2.919	3.434	2.491	2.93	2.902	3.414	5.085	5.983	4.674	5.5	ns
	Medium	2.65	3.118	2.279	2.681	2.642	3.108	4.845	5.701	4.375	5.148	ns
	Medium fast	2.529	2.975	2.176	2.56	2.521	2.965	4.724	5.558	4.259	5.011	ns
	Fast	2.516	2.96	2.168	2.551	2.508	2.95	4.717	5.55	4.251	5.002	ns
8 mA	Slow	2.863	3.368	2.427	2.855	2.844	3.346	5.196	6.114	4.769	5.612	ns
	Medium	2.599	3.058	2.217	2.608	2.59	3.047	4.952	5.827	4.471	5.261	ns
	Medium fast	2.483	2.921	2.114	2.487	2.473	2.91	4.832	5.685	4.364	5.134	ns
	Fast	2.467	2.902	2.106	2.478	2.457	2.89	4.826	5.678	4.348	5.116	ns
12 mA	Slow	2.747	3.232	2.296	2.701	2.724	3.204	5.39	6.342	4.938	5.81	ns
	Medium	2.493	2.934	2.102	2.473	2.483	2.921	5.166	6.078	4.65	5.471	ns
	Medium fast	2.382	2.803	2.006	2.36	2.371	2.789	5.067	5.962	4.546	5.349	ns
	Fast	2.369	2.787	1.999	2.352	2.357	2.773	5.063	5.958	4.538	5.339	ns
16 mA	Slow	2.677	3.149	2.213	2.604	2.649	3.116	5.575	6.56	5.08	5.977	ns
	Medium	2.432	2.862	2.028	2.386	2.421	2.848	5.372	6.32	4.801	5.649	ns
	Medium fast	2.324	2.734	1.937	2.278	2.311	2.718	5.297	6.233	4.7	5.531	ns
	Fast	2.313	2.721	1.929	2.269	2.3	2.706	5.296	6.231	4.699	5.529	ns
LVCMOS 2.5 V (for MSIO I/O Bank)												
2 mA	Slow	3.48	4.095	3.855	4.534	3.785	4.453	2.12	2.494	3.45	4.059	ns
4 mA	Slow	2.583	3.039	3.042	3.579	3.138	3.691	4.143	4.874	4.687	5.513	ns
6 mA	Slow	2.392	2.815	2.669	3.139	2.82	3.317	4.909	5.775	5.083	5.98	ns
8 mA	Slow	2.309	2.717	2.565	3.017	2.74	3.223	5.812	6.837	5.523	6.497	ns
12 mA	Slow	2.333	2.745	2.437	2.867	2.626	3.089	6.131	7.213	5.712	6.72	ns
16 mA	Slow	2.412	2.838	2.335	2.747	2.533	2.979	6.54	7.694	6.007	7.067	ns

Table 32 • LVCMOS 2.5 V Transmitter Characteristics (continued)
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

Output Drive Selection	Slew Control	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}*		t_{LZ}*		Units
		Speed Grade										
		–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
LVCMOS 2.5 V (for MSIOD I/O Bank)												
2 mA	Slow	2.206	2.596	2.678	3.15	2.64	3.106	4.935	5.805	4.74	5.576	ns
4 mA	Slow	1.835	2.159	2.242	2.637	2.256	2.654	5.413	6.368	5.15	6.059	ns
6 mA	Slow	1.709	2.01	2.132	2.508	2.167	2.549	5.813	6.838	5.499	6.469	ns
8 mA	Slow	1.63	1.918	1.958	2.303	2.012	2.367	6.226	7.324	5.816	6.842	ns
12 mA	Slow	1.648	1.939	1.86	2.187	1.921	2.259	6.519	7.669	6.027	7.09	ns

*Note: *Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.*

8.6.4 1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

8.6.4.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 33 • LVCMOS 1.8 V DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.8 V DC Recommended Operating Conditions						
VDDI	Supply voltage		1.710	1.8	1.89	V
LVCMOS 1.8 V DC Input Voltage Specification						
VIH (DC)	DC input logic High (for MSIOD and DDRIO I/O Banks)		0.65 × VDDI	–	1.89	V
VIH (DC)	DC input logic High (for MSIO I/O Bank)		0.65 × VDDI	–	3.45	V
VIL (DC)	DC input logic Low		–0.3	–	0.35 × VDDI	V
IIH (DC)	Input current High		–	–	10	µA
IIL (DC)	Input current Low		–	–	10	µA
LVCMOS 1.8 V DC Output Voltage Specification						
VOH	DC output logic High		VDDI – 0.45	–	–	V
VOL	DC output logic Low		–	–	0.45	V

Table 34 • LVCMOS 1.8 V AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVCMOS 1.8 V Minimum and Maximum AC Switching Speed							
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	400	Mbps	*
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	295	Mbps	
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	400	Mbps	*

Table 34 • LVCMOS 1.8 V AC Specifications (continued)

Symbols	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVCMOS 1.8 V AC Calibrated Impedance Option							
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)		–	75, 60, 50, 33, 25, 20	–	Ω	
LVCMOS 1.8 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.9	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	
*Note: *Maximum Data Rate applies for Drive Strength 8mA and above, All Slews*							

Table 35 • LVCMOS 1.8 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max			
2 mA	2 mA	2 mA	VDDI – 0.45	0.45	2	2	
4 mA	4 mA	4 mA	VDDI – 0.45	0.45	4	4	
6 mA	6 mA	6 mA	VDDI – 0.45	0.45	6	6	
8 mA	8 mA	8 mA	VDDI – 0.45	0.45	8	8	
10 mA	10 mA	10 mA	VDDI – 0.45	0.45	10	10	
12 mA	N/A	12 mA	VDDI – 0.45	0.45	12	12	
N/A	N/A	16 mA	VDDI – 0.45	0.45	16	16	*
*Note: *16mA Drive Strengths, All Slews, meets LPDDR JEDEC Electrical Compliance*							

8.6.4.2. AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.71 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 36 • **LVCMOS 1.8 V Receiver Characteristics**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		Speed Grade				
		–1	Std	–1	Std	
LVCMOS 1.8 V (for DDRIO I/O Bank with FIXED CODES)	None	1.968	2.315	2.099	2.47	ns
LVCMOS 1.8 V (for MSIO I/O Bank)	None	2.898	3.411	2.883	3.393	ns
	50	3.05	3.59	3.044	3.583	ns
	75	2.999	3.53	2.987	3.516	ns
	150	2.947	3.469	2.933	3.452	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)	None	2.611	3.071	2.598	3.057	ns
	50	2.775	3.264	2.775	3.265	ns
	75	2.72	3.2	2.712	3.19	ns
	150	2.666	3.137	2.655	3.123	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 37 • **LVCMOS 1.8 V Transmitter Characteristics**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

Output Drive Selection	Slew Control	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}*		t_{LZ}*		Units
		Speed Grade										
		–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
LVCMOS 1.8 V (for DDRIO I/O Bank with Fixed Code)												
2 mA	Slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	Medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	Medium fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	Fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4 mA	Slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	Medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	Medium fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	Fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6 mA	Slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	Medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	Medium fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	Fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns

Table 37 • LVCMOS 1.8 V Transmitter Characteristics (continued)
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

Output Drive Selection	Slew Control	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}*		t_{LZ}*		Units
		Speed Grade										
		–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
8 mA	Slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns
	Medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	Medium fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	Fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10 mA	Slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	Medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	Medium fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	Fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12 mA	Slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	Medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	Medium fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	Fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16 mA	Slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	Medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	Medium fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	Fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns
LVCMOS 1.8 V (for MSIO I/O Bank)												
2 mA	Slow	3.441	4.047	4.165	4.9	4.413	5.192	4.891	5.755	5.138	6.044	ns
4 mA	Slow	3.218	3.786	3.642	4.284	3.941	4.636	5.665	6.665	5.568	6.551	ns
6 mA	Slow	3.141	3.694	3.501	4.118	3.823	4.498	6.587	7.75	6.032	7.096	ns
8 mA	Slow	3.165	3.723	3.319	3.904	3.654	4.298	6.898	8.115	6.216	7.313	ns
10 mA	Slow	3.202	3.767	3.278	3.857	3.616	4.254	7.25	8.529	6.435	7.571	ns
12 mA	Slow	3.277	3.855	3.175	3.736	3.519	4.139	7.392	8.697	6.538	7.692	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)												
2 mA	Slow	2.725	3.206	3.316	3.901	3.484	4.099	5.204	6.123	4.997	5.88	ns
4 mA	Slow	2.242	2.638	2.777	3.267	2.947	3.466	5.729	6.74	5.448	6.41	ns
6 mA	Slow	1.995	2.347	2.466	2.901	2.63	3.094	6.372	7.496	5.987	7.043	ns
8 mA	Slow	2.001	2.354	2.44	2.87	2.6	3.058	6.633	7.804	6.193	7.286	ns
10 mA	Slow	2.025	2.382	2.312	2.719	2.47	2.906	6.94	8.165	6.412	7.544	ns

*Note: *Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.*

8.6.5 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

8.6.5.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 38 • **LVCMOS 1.5 V DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.5 V DC Recommended Operating Conditions						
VDDI	Supply voltage		1.425	1.5	1.575	V
LVCMOS 1.5 V DC Input Voltage Specification						
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O Banks)		0.65 × VDDI	–	1.575	V
VIH (DC)	DC input logic High (for MSIO I/O Bank)		0.65 × VDDI	–	3.45	V
VIL (DC)	DC input logic Low		–0.3	–	0.35 × VDDI	V
IIH (DC)	Input current High		–	–	10	µA
IIL (DC	Input current Low		–	–	10	µA
LVCMOS 1.5 V DC Output Voltage Specification						
VOH	DC output logic High		VDDI × 0.75	–	–	V
VOL	DC output logic Low		–	–	VDDI × 0.25	V

Table 39 • **LVCMOS 1.5 V AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.5 V AC Minimum and Maximum Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	235	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	160	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	220	Mbps
LVCMOS 1.5 V AC Calibrated Impedance Option						
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)		–	75, 60, 50, 40	–	Ω
LVCMOS 1.5 V AC Test Parameters Specifications						
Vtrip	Measuring/trip point		–	0.75	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

Table 40 • LVCMOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max		
2 mA	2 mA	2 mA	VDDI × 0.75	VDDI × 0.25	2	2
4 mA	4 mA	4 mA	VDDI × 0.75	VDDI × 0.25	4	4
6 mA	6 mA	6 mA	VDDI × 0.75	VDDI × 0.25	6	6
8 mA	N/A	8 mA	VDDI × 0.75	VDDI × 0.25	8	8
N/A	N/A	10 mA	VDDI × 0.75	VDDI × 0.25	10	10
N/A	N/A	12 mA	VDDI × 0.75	VDDI × 0.25	12	12

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

8.6.5.2 AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.425 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 41 • LVCMOS 1.5 V Receiver Characteristics
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		Speed Grade				
		–1	Std	–1	Std	
LVCMOS 1.5 V (for DDRIO I/O Bank with FIXED CODES)	None	2.051	2.413	2.086	2.455	ns
LVCMOS 1.5 V (for MSIO I/O Bank)	None	3.311	3.896	3.285	3.865	ns
	50	3.654	4.299	3.623	4.263	ns
	75	3.533	4.156	3.501	4.119	ns
	150	3.415	4.018	3.388	3.986	ns
LVCMOS 1.5 V (for MSIOD I/O Bank)	None	2.959	3.481	2.93	3.447	ns
	50	3.298	3.88	3.268	3.845	ns
	75	3.162	3.719	3.128	3.68	ns
	150	3.053	3.592	3.021	3.554	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 42 • LVCMOS 1.5 V Transmitter Characteristics
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

Output Drive Selection	Slew Control	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}*		t_{LZ}*		Units
		Speed Grade										
		–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
LVCMOS 1.5 V (for DDRIO I/O Bank)												
2 mA	Slow	5.122	6.026	4.31	5.07	5.145	6.052	5.258	6.186	4.672	5.496	ns
	Medium	4.58	5.389	3.86	4.54	4.6	5.411	4.977	5.855	4.357	5.126	ns
	Medium fast	4.323	5.086	3.629	4.269	4.341	5.107	4.804	5.652	4.228	4.974	ns
	Fast	4.296	5.054	3.609	4.245	4.314	5.075	4.791	5.636	4.219	4.963	ns

Table 42 • LVCMOS 1.5 V Transmitter Characteristics (continued)
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

Output Drive Selection	Slew Control	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}*		t_{LZ}*		Units
		Speed Grade										
		–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
4 mA	Slow	4.449	5.235	3.707	4.361	4.443	5.227	6.058	7.127	5.458	6.421	ns
	Medium	3.961	4.66	3.264	3.839	3.954	4.651	5.778	6.797	5.116	6.018	ns
	Medium fast	3.729	4.387	3.043	3.579	3.72	4.376	5.63	6.624	4.981	5.86	ns
	Fast	3.704	4.358	3.027	3.56	3.695	4.347	5.624	6.617	4.973	5.851	ns
6 mA	Slow	4.244	4.993	3.465	4.076	4.233	4.979	6.39	7.518	5.736	6.748	ns
	Medium	3.774	4.44	3.05	3.587	3.762	4.426	6.114	7.193	5.397	6.35	ns
	Medium fast	3.544	4.17	2.839	3.339	3.529	4.152	5.978	7.033	5.27	6.2	ns
	Fast	3.519	4.14	2.82	3.317	3.504	4.122	5.965	7.017	5.259	6.187	ns
8 mA	Slow	4.099	4.823	3.311	3.894	4.087	4.807	6.584	7.746	5.854	6.888	ns
	Medium	3.656	4.301	2.927	3.443	3.642	4.284	6.311	7.425	5.553	6.533	ns
	Medium fast	3.437	4.044	2.731	3.213	3.42	4.023	6.182	7.273	5.435	6.394	ns
	Fast	3.41	4.012	2.715	3.193	3.393	3.991	6.178	7.269	5.425	6.383	ns
10 mA	Slow	4.029	4.74	3.238	3.809	4.015	4.723	6.732	7.921	5.965	7.018	ns
	Medium	3.601	4.237	2.867	3.372	3.586	4.218	6.473	7.615	5.669	6.669	ns
	Medium fast	3.384	3.981	2.672	3.143	3.365	3.958	6.351	7.471	5.55	6.529	ns
	Fast	3.357	3.949	2.655	3.123	3.338	3.927	6.345	7.464	5.54	6.518	ns
12 mA	Slow	3.974	4.675	3.196	3.759	3.958	4.656	6.842	8.049	6.068	7.139	ns
	Medium	3.55	4.176	2.827	3.326	3.534	4.157	6.584	7.746	5.751	6.766	ns
	Medium fast	3.345	3.935	2.638	3.103	3.325	3.911	6.488	7.633	5.641	6.637	ns
	Fast	3.316	3.902	2.621	3.083	3.297	3.878	6.486	7.63	5.626	6.619	ns
LVCMOS 1.5 V (for MSIO I/O Bank)												
2 mA	Slow	4.423	5.203	5.397	6.35	5.686	6.69	5.609	6.599	5.561	6.542	ns
4 mA	Slow	4.05	4.765	4.503	5.298	4.92	5.788	7.358	8.657	6.525	7.677	ns
6 mA	Slow	4.081	4.801	4.259	5.012	4.699	5.528	7.659	9.011	6.709	7.893	ns
8 mA	Slow	4.234	4.98	4.068	4.786	4.521	5.319	8.218	9.668	7.05	8.294	ns
LVCMOS 1.5 V (for MSIOD I/O Bank)												
2 mA	Slow	2.735	3.218	3.371	3.966	3.618	4.257	6.03	7.095	5.705	6.712	ns
4 mA	Slow	2.426	2.854	2.992	3.521	3.221	3.79	6.738	7.927	6.298	7.41	ns
6 mA	Slow	2.433	2.862	2.81	3.306	3.031	3.566	7.123	8.38	6.596	7.76	ns

*Note: *Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.*

8.6.6 1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-12A.

8.6.6.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 43 • **LVCMOS 1.2 V DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVCMOS 1.2 V DC Recommended DC Operating Conditions							
VDDI	Supply voltage		1.140	1.2	1.26	V	
LVCMOS 1.2 V DC Input Voltage Specification							
VIH (DC)	DC input logic High (for MSIOD and DDRIO I/O Banks)		0.65 × VDDI	–	1.26	V	
VIH (DC)	DC input logic High (for MSIO I/O Bank)		0.65 × VDDI	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.35 × VDDI	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVCMOS 1.2 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI × 0.75	–	–	V	
VOL	DC output logic Low		–	–	VDDI × 0.25	V	

Table 44 • **LVCMOS 1.2 V AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.2 V Minimum and Maximum AC Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	200	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	120	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	160	Mbps
LVCMOS 1.2 V AC Calibrated Impedance Option						
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)		–	75, 60, 50, 40	–	Ω
LVCMOS 1.2 V AC Test Parameters Specifications						
Vtrip	Measuring/trip point		–	0.6	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

Table 45 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max		
2 mA	2 mA	2 mA	VDDI × 0.75	VDDI × 0.25	2	2
4 mA	4 mA	4 mA	VDDI × 0.75	VDDI × 0.25	4	4
N/A	N/A	6 mA	VDDI × 0.75	VDDI × 0.25	6	6

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

8.6.6.2 AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.14 V

AC Switching Characteristics for Receiver (Input Buffers))

Table 46 • LVCMOS 1.2 V Receiver Characteristics
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		Speed Grade				
		–1	Std	–1	Std	
LVCMOS 1.2 V (for DDRIO I/O Bank with Fixed Code)	None	2.448	2.88	2.466	2.901	ns
LVCMOS 1.2 V (for MSIO I/O Bank)	None	4.714	5.545	4.675	5.5	ns
	50	6.668	7.845	6.579	7.74	ns
	75	5.832	6.862	5.76	6.777	ns
	150	5.162	6.073	5.111	6.014	ns
LVCMOS 1.2 V (for MSIOD I/O Bank)	None	4.154	4.887	4.114	4.84	ns
	50	6.918	8.139	6.806	8.008	ns
	75	5.613	6.603	5.533	6.509	ns
	150	4.716	5.549	4.657	5.479	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 47 • LVCMOS 1.2 V Transmitter Characteristics
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

Output Drive Selection	Slew Control	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}*		t_{LZ}*		Units
		Speed Grade										
		–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
LVCMOS 1.2 V (for DDRIO I/O Bank)												
2 mA	Slow	6.713	7.897	5.362	6.308	6.723	7.909	7.233	8.51	6.375	7.499	ns
	Medium	5.912	6.955	4.616	5.43	5.915	6.959	6.887	8.102	6.009	7.069	ns
	Medium fast	5.5	6.469	4.231	4.978	5.5	6.471	6.672	7.849	5.835	6.865	ns
	Fast	5.462	6.426	4.194	4.935	5.463	6.427	6.646	7.819	5.828	6.857	ns
4 mA	Slow	6.109	7.186	4.708	5.539	6.098	7.174	8.005	9.418	7.033	8.274	ns
	Medium	5.355	6.299	4.034	4.746	5.338	6.28	7.637	8.985	6.672	7.849	ns
	Medium fast	4.953	5.826	3.685	4.336	4.932	5.802	7.44	8.752	6.499	7.646	ns
	Fast	4.911	5.777	3.658	4.303	4.89	5.754	7.427	8.737	6.488	7.632	ns
6 mA	Slow	5.89	6.929	4.506	5.301	5.874	6.911	8.337	9.808	7.315	8.605	ns
	Medium	5.176	6.089	3.862	4.543	5.155	6.065	7.986	9.394	6.943	8.168	ns
	Medium fast	4.792	5.637	3.523	4.145	4.765	5.606	7.808	9.186	6.775	7.97	ns
	Fast	4.754	5.593	3.486	4.101	4.728	5.563	7.777	9.149	6.769	7.963	ns
LVCMOS 1.2 V (for MSIO I/O Bank)												
2 mA	Slow	6.746	7.937	7.458	8.774	8.172	9.614	9.867	11.608	8.393	9.874	ns
4 mA	Slow	7.068	8.315	6.678	7.857	7.474	8.793	10.986	12.924	9.043	10.638	ns
LVCMOS 1.2 V (for MSIOD I/O Bank)												
2 mA	Slow	3.883	4.568	4.868	5.726	5.329	6.269	7.994	9.404	7.527	8.855	ns
4 mA	Slow	3.774	4.44	4.188	4.926	4.613	5.426	8.972	10.555	8.315	9.782	ns

*Note: *Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.*

8.6.7 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

8.6.7.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 48 • PCI/PCI-X DC Voltage Specification (Applicable to MSIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCIX DC Recommended Operating Conditions						
VDDI	Supply voltage		3.15	3.3	3.45	V
PCI/PCIX DC Input Voltage Specification						
VI	DC input voltage		0	–	3.45	V
IIH(DC)	Input current High		–	–	10	µA
IIL(DC)	Input current Low		–	–	10	µA
PCI/PCIX DC Output Voltage Specification						
VOH	DC output logic High		Per PCI Specification			V
VOL	DC output logic Low		Per PCI Specification			V

Table 49 • PCI/PCI-X AC Specifications (Applicable to MSIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCI-X Minimum and Maximum AC Switching Speed						
Dmax	Maximum data rate (MSIO I/O Bank)	AC Loading: per JEDEC specifications	–	–	630	Mbps
PCI/PCI-X AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path (falling edge)		–	0.615 × VDDI	–	V
Vtrip	Measuring/trip point for data path (rising edge)		–	0.285 × VDDI	–	V
Rtt_test	Resistance for data test path		–	25	–	Ω
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	10	–	pF

8.6.7.2 AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 3.0 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 50 • PCI/PCIX AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

		t_{PY}		t_{PYS}		
		Speed Grade				
	On-Die Termination (ODT)	–1	Std	–1	Std	Units
PCI/PCIX (for MSIO I/O Bank)	None	2.229	2.623	2.238	2.633	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 51 • **PCI/PCIX AC switching Characteristics for Transmitter (Output Buffers)**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		
	Speed Grade										
	–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	Units
PCI/PCIX (for MSIO I/O Bank)	2.146	2.525	2.043	2.404	2.084	2.452	6.095	7.171	5.558	6.539	ns

8.7 Memory Interface and Voltage Referenced I/O Standards

8.7.1 High-Speed Transceiver Logic (HSTL)

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO2 FPGA and SmartFusion2 SoC FPGA devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

8.7.1.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 52 • **HSTL DC Voltage Specification (Applicable to DDRIO I/O Bank Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
HSTL Recommended DC Operating Conditions						
VDDI	Supply voltage		1.425	1.5	1.575	V
VTT	Termination voltage		0.698	0.750	0.803	V
VREF	Input reference voltage		0.698	0.750	0.803	V
HSTL DC Input Voltage Specification						
VIH (DC)	DC input logic High		VREF + 0.1	–	1.575	V
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.1	V
IIH (DC)	Input current High		–	–	10	µA
IIL (DC)	Input current Low		–	–	10	µA
HSTL DC Output Voltage Specification						
HSTL Class I						
VOH	DC output logic High		VDDI – 0.4	–	–	V
VOL	DC output logic Low		–	–	0.4	V
IOH at VOH	Output minimum source DC current (MSIO and DDRIO I/O Banks)		–8.0	–	–	mA
IOL at VOL	Output minimum sink current (MSIO and DDRIO I/O Banks)		8.0	–	–	mA
HSTL Class II (Applicable to DDRIO I/O Bank Only)						
VOH	DC output logic High		VDDI – 0.4	–	–	V
VOL	DC output logic Low		–	–	0.4	V
IOH at VOH	Output minimum source DC current		–16.0	–	–	mA
IOL at VOL	Output minimum sink current		16.0	–	–	mA
HSTL DC Differential Voltage Specifications						
VID (DC)	DC input differential voltage		0.2	–	–	V

Table 53 • **HSTL AC Specifications (Applicable to DDRIO Bank Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
HSTL AC Differential Voltage Specifications						
VDIFF	AC input differential voltage		0.4	–	–	V
Vx	AC differential cross point voltage		0.68	–	0.9	V
HSTL Minimum and Maximum AC Switching Speed						
Dmax	Maximum data rate	AC loading: per JEDEC specifications	–	–	400	Mbps
HSTL Impedance Specification						
Rref	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistance = 191 Ω	–	25.5, 47.8	–	Ω
RTT	Effective impedance value (ODT for DDRIO I/O Bank only)	Reference resistance = 191 Ω	–	47.8	–	Ω
HSTL AC Test Parameters Specification						
Vtrip	Measuring/trip point for data path		–	0.75	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Rtt_test	Reference resistance for data test path for HSTL15 Class I (t_{DP})		–	50	–	Ω
Rtt_test	Reference resistance for data test path for HSTL15 Class II (t_{DP})		–	25	–	Ω
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.7.1.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 54 • **HSTL Receiver Characteristics**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

		t_{PY}		
		Speed Grade		
	On-Die Termination (ODT)	–1	Std	Units
HSTL (for DDRIO I/O Bank with Fixed Code)				
Pseudo differential	None	1.605	1.888	ns
	47.8	1.614	1.898	ns
True differential	None	1.622	1.909	ns
	47.8	1.628	1.916	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 55 • **HSTL Transmitter Characteristics**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		
	Speed Grade										
	–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	Units
HSTL Class I (for DDRIO I/O Bank)											
Single-ended	2.6	3.059	2.514	2.958	2.514	2.958	2.431	2.86	2.431	2.86	ns
Differential	2.621	3.083	2.648	3.115	2.647	3.113	2.925	3.442	2.923	3.44	ns
HSTL Class II (for DDRIO I/O Bank)											
Single-ended	2.511	2.954	2.488	2.927	2.49	2.93	2.409	2.833	2.411	2.836	ns
Differential	2.528	2.974	2.552	3.003	2.551	3.001	2.897	3.409	2.896	3.408	ns

8.7.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

8.7.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.3.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 56 • **DDR1/SSTL2 DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
DDR/SSTL2 DC Recommended Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
VTT	Termination voltage		1.164	1.250	1.339	V
VREF	Input reference voltage		1.164	1.250	1.339	V
DDR/SSTL2 DC Input Voltage Specification						
VIH (DC)	DC input logic High		VREF + 0.15	–	2.625	V
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.15	V
IIH (DC)	Input current High		–	–	10	µA
IIL (DC)	Input current Lo		–	–	10	µA
DDR/SSTL2 DC Output Voltage Specification						
SSTL2 Class I (DDR Reduced Drive)						
VOH	DC output logic High		VTT + 0.608	–	–	V
VOL	DC output logic Low		–	–	VTT – 0.608	V
IOH at VOH	Output minimum source DC current		8.1	–	–	mA

Table 56 • **DDR1/SSTL2 DC Voltage Specification (continued)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
IOL at VOL	Output minimum sink current		–8.1	–	–	mA
SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Banks Only						
VOH	DC output logic High		VTT + 0.81	–	–	V
VOL	DC output logic Low		–	–	VTT – 0.81	V
IOH at VOH	Output minimum source DC current		16.2	–	–	mA
IOL at VOL	Output minimum sink current		–16.2	–	–	mA
SSTL2 DC Differential Voltage Specification						
VID (DC)	DC input differential voltage		0.3	–	–	V

Table 57 • **DDR1/SSTL2 AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
SSTL2 AC Differential Voltage Specification						
VDIFF (AC)	AC input differential voltage		0.7	–	–	V
Vx (AC)	AC differential cross point voltage		0.5 × VDDI – 0.2	–	0.5 × VDDI + 0.2	V
SSTL2 Minimum and Maximum AC Switching Speeds						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: per JEDEC specifications	–	–	400	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17pF load	–	–	575	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 3 pF / 50 Ω load	–	–	700	Mbps
		AC loading: 17pF load	–	–	510	Mbps
SSTL2 Impedance Specifications						
–	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistor = 150 Ω	–	20, 42	–	Ω
AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	1.25	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Rtt_test	Reference resistance for data test path for SSTL2 Class I (t_{DP})		–	50	–	Ω
Rtt_test	Reference resistance for data test path for SSTL2 Class II (t_{DP})		–	25	–	Ω
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.7.3.2. AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 58 • **DDR1/SSTL2 Receiver Characteristics**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY} Speed Grade –1	t_{PY} Speed Grade Std	Units
SSTL2 (for DDRIO I/O Bank)				
Pseudo differential	None	1.549	1.821	ns
True differential	None	1.589	1.87	ns
SSTL2 (for MSIO I/O Bank)				
Pseudo differential	None	2.798	3.293	ns
True differential	None	2.733	3.215	ns
SSTL2 (for MSIOD I/O Bank)				
Pseudo differential	None	2.476	2.913	ns
True differential	None	2.475	2.911	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 59 • **DDR1/SSTL2 Transmitter Characteristics**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		Units
	Speed Grade										
	–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
SSTL2 Class I (for DDRIO I/O Bank)											
Single-ended	2.26	2.66	1.99	2.341	1.985	2.335	2.135	2.512	2.13	2.505	ns
Differential	2.26	2.658	2.202	2.591	2.201	2.589	2.393	2.815	2.392	2.814	ns
SSTL2 Class I (for MSIO I/O Bank)											
Single-ended	2.055	2.417	2.037	2.396	2.03	2.388	2.068	2.433	2.061	2.425	ns
Differential	2.192	2.58	2.434	2.864	2.425	2.852	2.164	2.545	2.156	2.536	ns
SSTL2 Class I (for MSIOD I/O Bank)											
Single-ended	1.512	1.779	1.462	1.72	1.462	1.72	1.676	1.972	1.676	1.971	ns
Differential	1.676	1.971	1.774	2.087	1.766	2.077	1.854	2.181	1.845	2.171	ns
SSTL2 Class II (for DDRIO I/O Bank)											
Single-ended	2.122	2.497	1.906	2.243	1.902	2.237	2.061	2.424	2.056	2.418	ns
Differential	2.127	2.501	2.042	2.402	2.043	2.403	2.363	2.78	2.365	2.781	ns
SSTL2 Class I (for MSIO I/O Bank)											
Single-ended	2.29	2.693	1.988	2.338	1.978	2.326	1.989	2.34	1.979	2.328	ns
Differential	2.418	2.846	2.304	2.711	2.297	2.702	2.131	2.506	2.124	2.499	ns

8.7.4 Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double date rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.4.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 60 • **SSTL18 DC Minimum and Maximum DC Input and Output Levels**

Symbols	Parameters	Conditions	Min	Typ	Max	Units	Notes
SSTL18 DC Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	
VTT	Termination voltage		0.838	0.900	0.964	V	
VREF	Input reference voltage		0.838	0.900	0.964	V	
SSTL18 DC Input Voltage Specification							
VIH (DC)	DC input logic High		VREF + 0.125	–	1.89	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.125	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
SSTL18 DC Output Voltage Specification							
SSTL18 Class I (DDR2 Reduced Drive)							
VOH	DC output logic High		VTT + 0.603	–	–	V	
VOL	DC output logic Low		–	–	VTT– 0.603	V	
IOH at VOH	Output minimum source DC current (DDRIO I/O Bank only)		6.5	–	–	mA	
IOL at VOL	Output minimum sink current (DDRIO I/O Bank only)		–6.5	–	–	mA	
SSTL18 Class II (DDR2 Full Drive)							*
VOH	DC output logic High		VTT + 0.603	–	–	V	
VOL	DC output logic Low		–	–	VTT– 0.603	V	
IOH at VOH	Output minimum source DC current (DDRIO I/O Bank only)		13.4	–	–	mA	
IOL at VOL	Output minimum sink current (DDRIO I/O Bank only)		–13.4	–	–	mA	
SSTL18 DC Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.3	–	–	V	

*Note: *To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.*

Table 61 • **SSTL18 AC Specifications (Applicable to DDRIO Bank Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
SSTL18 AC Differential Voltage Specification						
VDIFF (AC)	AC input differential voltage		0.5	–	–	V
Vx (AC)	AC differential cross point voltage		0.5 × VDDI – 0.175	–	0.5 × VDDI + 0.175	V
SSTL18 Minimum and Maximum AC Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: per JEDEC specification	–	–	667	Mbps
SSTL18 Impedance Specifications						
Rref	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistor = 150 Ω	–	20, 42	–	Ω
RTT	Effective impedance value (ODT)	Reference resistor = 150 Ω	–	50, 75, 150	–	Ω
SSTL18 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	0.9	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Rtt_test	Reference resistance for data test path for SSTL18 Class I (t_{DP})		–	50	–	Ω
Rtt_test	Reference resistance for data test path for SSTL18 Class II (t_{DP})		–	25	–	Ω
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.7.4.2. AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.71 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 62 • **DDR2/SSTL18 Receiver Characteristics**

Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY}		Units
		Speed Grade		
		–1	Std	
SSTL18 (for DDRIO I/O Bank with Fixed Code)				
Pseudo differential	None	1.567	1.844	ns
True differential	None	1.588	1.869	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 63 • **DDR2/SSTL18 Transmitter Characteristics**

Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		Units
	Speed Grade										
	–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
SSTL18 Class I (for DDRIO I/O Bank)											
Single-ended	2.383	2.804	2.23	2.623	2.229	2.622	2.202	2.591	2.201	2.59	ns
Differential	2.413	2.84	2.797	3.29	2.797	3.29	2.282	2.685	2.282	2.685	ns
SSTL18 Class II (for DDRIO I/O Bank)											
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.171	2.555	2.17	2.554	ns
Differential	2.315	2.724	2.698	3.173	2.698	3.173	2.242	2.639	2.242	2.639	ns

8.7.5 Stub-Series Terminated Logic 1.5 V (SSTL15)

SSTL15 Class I and Class II are supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR3) standard. IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.5.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 64 • **SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
SSTL15 DC Recommended DC Operating Conditions						
VDDI	Supply voltage		1.425	1.5	1.575	V
VTT	Termination voltage		0.698	0.750	0.803	V
VREF	Input reference voltage		0.698	0.750	0.803	V
SSTL15 DC Input Voltage Specification						
VIH(DC)	DC input logic High		VREF + 0.1	–	1.575	V
VIL(DC)	DC input logic Low		–0.3	–	VREF – 0.1	V
IIH (DC)	Input current High		–	–	10	µA
IIL (DC)	Input current Low		–	–	10	µA
SSTL15 DC Output Voltage Specification						
DDR3/SSTL15 Class I (DDR3 Reduced Drive)						
VOH	DC output logic High		0.8 × VDDI	–	–	V
VOL	DC output logic Low		–	–	0.2 × VDDI	V
IOH at VOH	Output minimum source DC current		6.5	–	–	mA
IOL at VOL	Output minimum sink current		–6.5	–	–	mA
DDR3/SSTL15 Class II (DDR3 Full Drive)						
VOH	DC output logic High		0.8 × VDDI	–	–	V
VOL	DC output logic Low		–	–	0.2 × VDDI	V
IOH at VOH	Output minimum source DC current		7.6	–	–	mA
IOL at VOL	Output minimum sink current		–7.6	–	–	mA
SSTL15 Differential Voltage Specification						
VID	DC input differential voltage		0.2	–	–	V

*Note: *To meet JEDEC Electrical Compliance, use DDR3 Full Drive Transmitter.*

Table 65 • **SSTL15 AC Specifications (for DDRIO I/O Bank Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
SSTL15 Differential Voltage Specification						
VDIFF (AC)	AC input differential voltage		0.3	–	–	V
Vx (AC)	AC differential cross point voltage		0.5 × VDDI – 0.150	–	0.5 × VDDI + 0.150	V
SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Banks only)						
Dmax	Maximum data rate	AC loading: per JEDEC specifications	–	–	667	Mbps
SSTL15 AC Calibrated Impedance Option						
Rref	Supported output driver calibrated impedance	Reference resistor = 240 Ω	–	34, 40	–	Ω
RTT	Effective impedance value (ODT)	Reference resistor = 240 Ω	–	20, 30, 40, 60, 120	–	Ω
SSTL15 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	0.75	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Rtt_test	Reference resistance for data test path for SSTL15 Class I (t_{DP})		–	50	–	Ω
Rtt_test	Reference resistance for data test path for SSTL15 Class II (t_{DP})		–	25	–	Ω
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.7.5.2. AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.425 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 66 • **DDR3/SSTL15 Receiver Characteristics**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

		t_{PY}		
		Speed Grade		
	On-Die Termination (ODT)	–1	Std	Units
DDR3/SSTL15 (for DDRIO I/O Bank – with Calibration Only)				
Pseudo differential	None	1.605	1.888	ns
	20	1.616	1.901	ns
	30	1.613	1.897	ns
	40	1.611	1.895	ns
	60	1.609	1.893	ns
	120	1.607	1.89	ns
True differential	None	1.623	1.91	ns
	20	1.637	1.926	ns
	30	1.63	1.918	ns
	40	1.626	1.914	ns
	60	1.622	1.91	ns
	120	1.619	1.905	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 67 • **DDR3/SSTL15 Transmitter Characteristics**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		
	Speed Grade										
	–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	Units
DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)											
Single-ended	2.533	2.98	2.522	2.967	2.523	2.968	2.427	2.855	2.428	2.856	ns
Differential	2.555	3.005	3.073	3.615	3.073	3.615	2.416	2.843	2.416	2.843	ns
DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)											
Single-ended	2.53	2.977	2.514	2.958	2.516	2.96	2.422	2.849	2.425	2.852	ns
Differential	2.552	3.002	2.591	3.048	2.59	3.047	2.882	3.391	2.881	3.39	ns

8.7.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.6.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 68 • **LPDDR DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	
VTT	Termination voltage		0.838	0.900	0.964	V	
VREF	Input reference voltage		0.838	0.900	0.964	V	
LPDDR DC Input Voltage Specification							
VIH (DC)	DC input logic High		0.7 × VDDI	–	1.89	V	
VIL (DC)	DC input logic Low		–0.3	–	0.3 × VDDI	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LPDDR DC Output Voltage Specification Reduced Drive							
VOH	DC output logic High		0.9 × VDDI	–	–	V	
VOL	DC output logic Low		–	–	0.1 × VDDI	V	
IOH at VOH	Output minimum source DC current		0.1	–	–	mA	
IOL at VOL	Output minimum sink current		–0.1	–	–	mA	
LPDDR DC Output Voltage Specification Full Drive							*
VOH	DC output logic High		0.9 × VDDI	–	–	V	
VOL	DC output logic Low		–	–	0.1 × VDDI	V	
IOH at VOH	Output minimum source DC current		0.1	–	–	mA	
IOL at VOL	Output minimum sink current		–0.1	–	–	mA	
LPDDR Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.4 × VDDI	–	–	V	

*Note: *To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.*

Table 69 • **LPDDR AC Specifications (for DDRIO I/O Banks Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR AC Differential Voltage Specification						
VDIFF	AC input differential voltage		0.6 × VDDI	–	–	V
Vx	AC differential cross point voltage		0.4 × VDDI	–	0.6 × VDDI	V
LPDDR AC Specifications						
Dmax	Maximum data rate	AC loading: per JEDEC specifications	–	–	400	Mbps
Symbols	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
LPDDR AC Calibrated Impedance Option						
Rref	Supported output driver calibrated impedance	Reference resistor = 150 Ω	–	20, 42	–	Ω

Table 69 • LPDDR AC Specifications (for DDRIO I/O Banks Only) (continued)

Rtt	Effective impedance value (ODT)	Reference resistor = 150 Ω	–	50, 70, 150	–	Ω
LPDDR AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	0.9	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Rtt_test	Reference resistance for data test path for LPDDR (t_{DP})		–	50	–	Ω
Cload	Capacitive loading for data path (t_{DP})		–	5	–	Ω

8.7.6.2 AC Switching Characteristics

Table 70 • LPDDR Receiver Characteristics
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

		t_{PY}		
		Speed Grade		
	On-Die Termination (ODT)	–1	Std	Units
LPDDR (for DDRIO I/O Bank with FIXED CODES)				
Pseudo differential	None	1.568	1.845	ns
True differential	None	1.588	1.869	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 71 • LPDDR Transmitter Characteristics
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		
	Speed Grade										
	–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	Units
LPDDR Reduced Drive for DDRIO I/O Bank											
Single-ended	2.383	2.804	2.23	2.623	2.229	2.622	2.202	2.591	2.201	2.59	ns
Differential	2.396	2.819	2.764	3.252	2.764	3.252	2.255	2.653	2.255	2.653	ns
LPDDR Full Drive for DDRIO I/O Bank											
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.171	2.555	2.17	2.554	ns
Differential	2.298	2.703	2.288	2.692	2.288	2.692	2.593	3.051	2.593	3.051	ns

8.7.6.3. Minimum and Maximum DC/AC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode

Table 72 • LPDDR-LVCMOS 1.8 V Mode (Minimum and Maximum DC Input and Output Levels)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR-LVCMOS 1.8 V Recommended DC Operating Conditions						
VDDI	Supply Voltage		1.710	1.8	1.89	V
LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification						
VIH(dc)	DC input Logic HIGH (for MSIOD and DDRIO I/O Banks)		0.65 × VDDI	–	1.89	V
VIH(dc)	DC input Logic HIGH (for MSIO I/O Bank)		0.65 × VDDI	–	3.45	V
VIL(dc)	DC input Logic LOW		–0.3	–	0.35 × VDDI	V
IIH(dc)	Input current HIGH		–	–	10	uA
IIL(dc)	Input current LOW		–	–	10	uA
LPDDR-LVCMOS 1.8V Mode DC Output Voltage Specification						
VOH	DC output Logic HIGH		VDDI – 0.45	–	–	V
VOL	DC output Logic LOW		–	–	0.45	V

Table 73 • LPDDR-LVCMOS 1.8 V Minimum and Maximum AC Switching Speeds

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Dmax	Maximum Data Rate (for DDRIO I/O Bank)	AC Loading: 17pF Load, 8mA Drive and Above/All Slew	–	–	400	Mbps

Table 74 • LPDDR-LVCMOS 1.8 V Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR - LVCMOS 1.8 V Calibrated Impedence Option						
Rodt_cal	Supported Output Driver Calibrated Impedence (for DDRIO I/O Bank)		–	75,60,50,33,25,20	–	Ω
LPDDR- LVCMOS 1.8V AC Test Parameters Specifications						
Vtrip	Measuring/Trip Point for data path		–	0.9	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive Loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Cload	Capacitive Loading for data path (t_{DP})		–	5	–	pF

Table 75 • LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification

Output Drive Selection	VOH (V) Min	VOL (V) Max	IOH (at VOH) mA	IOL (at VOL) mA	Notes
DDRIO Bank					
2mA	VDDI – 0.45	0.45	2	2	
4mA	VDDI – 0.45	0.45	4	4	
6mA	VDDI – 0.45	0.45	6	6	
8mA	VDDI – 0.45	0.45	8	8	
10mA	VDDI – 0.45	0.45	10	10	
12mA	VDDI – 0.45	0.45	12	12	
16mA	VDDI – 0.45	0.45	16	16	*
*Note: *16mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance*					

Table 76 • LPDDR-LVCMOS 1.8V AC Switching Characteristics for Receiver (Input Buffers)

	ODT (On Die Termination)	Speed Grade				Units
		–1	Std	–1	Std	
LPDDR-LVCMOS 1.8 mode (for DDRIO I/O Bank with Fixed Code)	None	1.968	2.315	2.099	2.47	ns

Table 77 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Output Drive Selection	Slew Control	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}*		t_{LZ}*		Units
		Speed Grade										
		–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
LPDDR-LVCMOS 1.8 V Mode (for DDRIO I/O Bank)												
2mA	slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	medium_fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4mA	slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	medium_fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6mA	slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	medium_fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns
8mA	slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns
	medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	medium_fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10mA	slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	medium_fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12mA	slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	medium_fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16mA	slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	medium_fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

*Note: *Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management).*

8.8. Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

8.8.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

8.8.1.1 Minimum and Maximum Input and Output Levels

Table 78 • **LVDS DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVDS Recommended DC Operating Conditions						
VDDI	Supply voltage	2.5 V range	2.375	2.5	2.625	V
VDDI	Supply voltage	3.3 V range	3.15	3.3	3.45	V
LVDS DC Input Voltage Specification						
VI	DC Input voltage	2.5 V range	0	–	2.925	V
VI	DC input voltage	3.3 V range	0	–	3.45	V
IIH (DC)	Input current High		–	–	10	µA
IIL (DC)	Input current Low		–	–	10	µA
LVDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
LVDS Differential Voltage Specification						
VOD	Differential output voltage swing		250	350	450	mV
VOCM	Output common mode voltage		1.125	1.25	1.375	V
VICM	Input common mode voltage		0.05	1.25	2.35	V
VID	Input differential voltage		100	350	600	mV

Table 79 • **LVDS AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVDS Minimum and Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 12 pF / 100 Ω differential load	–	–	535	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank) no pre-emphasis	AC loading: 10 pF / 100 Ω differential load	–	–	620	Mbps
		AC loading: 2 pF / 100 Ω differential load	–	–	700	Mbps
LVDS Impedance Specification						
Rt	Termination resistance		–	100	–	Ω
LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

8.8.1.2 LVDS25 AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 80 • LVDS25 Receiver Characteristics
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY} Speed Grade		Units
		–1	Std	
LVDS (for MSIO I/O Bank)	None	2.774	3.263	ns
	100	2.775	3.264	ns
LVDS (for MSIOD I/O Bank)	None	2.554	3.004	ns
	100	2.549	2.999	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 81 • LVDS25 Transmitter Characteristics
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		Units
	Speed Grade										
	–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
LVDS (for MSIO I/O Bank)	2.136	2.513	2.416	2.842	2.402	2.825	2.423	2.85	2.409	2.833	ns
LVDS (for MSIOD I/O Bank)											
No pre-emphasis	1.61	1.893	1.749	2.058	1.735	2.041	1.897	2.231	1.866	2.195	ns
Min pre-emphasis	1.527	1.796	1.757	2.067	1.744	2.052	1.905	2.241	1.876	2.207	ns
Med pre-emphasis	1.496	1.76	1.765	2.077	1.751	2.06	1.914	2.252	1.884	2.216	ns

8.8.1.3 LVDS33 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 82 • LVDS33 Receiver Characteristics
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	On Die Termination (ODT)	t_{PY} Speed Grade		Units
		–1	Std	
LVDS33 (for MSIO I/O Bank)	None	2.572	3.025	ns
	100	2.569	3.023	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 83 • LVDS33 Transmitter Characteristics
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		Units
	Speed Grade										
	–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
LVDS33 (for MSIO I/O Bank)	1.942	2.284	1.98	2.33	1.97	2.318	1.953	2.298	1.96	2.307	ns

8.8.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

8.8.2.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 84 • **B-LVDS DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
Bus-LVDS DC Input Voltage Specification						
VI	DC input voltage		0	–	2.925	V
IIH (DC)	Input current High		–	–	10	µA
IIL (DC)	Input current Low		–	–	10	µA
Bus-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
Bus-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing (for MSIO I/O Bank Only)		65	–	460	mV
VOCM	Output common mode voltage (for MSIO I/O Bank Only)		1.1	–	1.5	V
VICM	Input common mode voltage		0.05	–	2.4	V
VID	Input differential voltage		0.1	–	VDDI	V

Table 85 • **B-LVDS AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Minimum and Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	500	Mbps
Bus-LVDS Impedance Specifications						
Rt	Termination resistance		–	27	–	Ω
Bus-LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

8.8.2.2. AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 86 • **B-LVDS AC Switching Characteristics for Receiver (Input Buffers)**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY}		Units
		Speed Grade		
		–1	Std	
Bus-LVDS (for MSIO I/O Bank)	None	2.738	3.221	ns
	100	2.735	3.218	ns
Bus-LVDS (for MSIOD I/O Bank)	None	2.495	2.934	ns
	100	2.495	2.935	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 87 • **B-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		Units
	Speed Grade										
	–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
Bus-LVDS (for MSIO I/O Bank)	2.258	2.656	2.343	2.756	2.329	2.74	2.12	2.494	2.123	2.497	ns

8.8.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

8.8.3.1 Minimum and Maximum Input and Output Levels

Table 88 • **M-LVDS DC Voltage Specification**

Symbols	Parameters	Min	Typ	Max	Units	Notes
M-LVDS Recommended DC Operating Conditions						
VDDI	Supply voltage	2.375	2.5	2.625	V	*
M-LVDS DC Input Voltage Specification						
VI	DC input voltage	0	–	2.925	V	
IIH (DC)	Input current High	–	–	10	µA	
IIL (DC)	Input current Low	–	–	10	µA	
M-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)						
VOH	DC output logic High	1.25	1.425	1.6	V	
VOL	DC output logic Low	0.9	1.075	1.25	V	
M-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing (for MSIO I/O Bank Only)	300	–	650	mV	
VOCM	Output common mode voltage (for MSIO I/O Bank Only)	0.3	–	2.1	V	
VICM	Input common mode voltage	0.3	–	1.2	V	
VID	Input differential voltage	50	–	2400	mV	
*Note: *Only M-LVDS TYPE I is supported*						

Table 89 • **M-LVDS AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
M-LVDS Minimum and Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	500	Mbps
M-LVDS Impedance Specification						
Rt	Termination resistance		–	50	–	Ω
M-LVDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

8.8.3.2. AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 90 • **M-LVDS AC Switching Characteristics for Receiver (Input Buffers)**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY}		
		Speed Grade		
		–1	Std	Units
M-LVDS (for MSIO I/O Bank)	None	2.738	3.221	ns
	100	2.735	3.218	ns
M-LVDS (for MSIOD I/O Bank)	None	2.495	2.934	ns
	100	2.495	2.935	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 91 • **M-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		
	Speed Grade										
	–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	Units
M-LVDS (for MSIO I/O Bank)	2.258	2.656	2.348	2.762	2.334	2.746	2.123	2.497	2.125	2.5	ns

8.8.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

8.8.4.1 Mini-LVDS Minimum and Maximum Input and Output Levels

Table 92 • **Mini-LVDS DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
Mini-LVDS DC Input Voltage Specification						
VI	DC Input voltage		0	–	2.925	V
Mini-LVDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
Mini-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing		300	–	600	mV
VOCM	Output common mode voltage		1	–	1.4	V
VICM	Input common mode voltage		0.3	–	1.2	V
VID	Input differential voltage		100	–	600	mV

Table 93 • Mini-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Mini-LVDS Minimum and Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	520	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	700	Mbps
Mini-LVDS Impedance Specification						
Rt	Termination resistance		–	100	–	Ω
Mini-LVDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

8.8.4.2 AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 94 • Mini-LVDS AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY} Speed Grade –1	t_{PY} Speed Grade Std	Units
Mini-LVDS (for MSIO I/O Bank)	None	2.855	3.359	ns
	100	2.85	3.353	ns
Mini-LVDS (for MSIOD I/O Bank)	None	2.602	3.061	ns
	100	2.597	3.055	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 95 • Mini-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		Units
	Speed Grade										
	–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	
Mini-LVDS (for MSIO I/O Bank)	2.097	2.467	2.308	2.715	2.296	2.701	1.964	2.31	1.949	2.293	ns
Mini-LVDS (for MSIOD I/O Bank)											
No pre-emphasis	1.614	1.899	1.562	1.837	1.553	1.826	1.593	1.874	1.578	1.856	ns
Min pre-emphasis	1.604	1.887	1.745	2.053	1.731	2.036	1.892	2.225	1.861	2.189	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

8.8.5 RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

8.8.5.1 Minimum and Maximum Input and Output Levels

Table 96 • **RSDS DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
RSDS DC Input Voltage Specification						
VI	DC input voltage		0	–	2.925	V
RSDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
RSDS Differential Voltage Specification						
VOD	Differential output voltage swing		100	–	600	mV
VOCM	Output common mode voltage		0.5	–	1.5	V
VICM	Input common mode voltage		0.3	–	1.5	V
VID	Input differential voltage		100	–	600	mV

Table 97 • **RSDS AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
RSDS Minimum and Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	520	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	700	Mbps
RSDS Impedance Specification						
Rt	Termination resistance		–	100	–	Ω
RSDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

8.8.5.2. AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 98 • **RSDS AC Switching Characteristics for Receiver (Input Buffers)**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY} Speed Grade –1	t_{PY} Speed Grade Std	Units
RSDS (for MSIO I/O Bank)	None	2.855	3.359	ns
	100	2.85	3.353	ns
RSDS (for MSIOD I/O Bank)	None	2.602	3.061	ns
	100	2.597	3.055	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 99 • **RSDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		
	Speed Grade										
	–1	Std	–1	Std	–1	Std	–1	Std	–1	Std	Units
RSDS (for MSIO I/O Bank)	2.097	2.467	2.303	2.709	2.291	2.695	1.961	2.307	1.947	2.29	ns
RSDS (for MSIOD I/O Bank)											
No pre-emphasis	1.614	1.899	1.559	1.834	1.55	1.823	1.59	1.87	1.575	1.852	ns
Min pre-emphasis	1.604	1.887	1.742	2.05	1.728	2.032	1.889	2.222	1.858	2.185	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

8.8.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

8.8.6.1 Minimum and Maximum Input and Output Levels

Table 100 • **LVPECL DC Voltage Specification (Applicable to MSIO I/O Banks Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		3.15	3.3	3.45	V
LVPECL DC Input Voltage Specification						
VI	DC input voltage		0	–	3.45	V
LVPECL Differential Voltage Specification						
VICM	Input common mode voltage		0.3		2.8	V
VIDIFF	Input differential voltage		100	300	1,000	mV

Table 101 • **LVPECL Minimum and Maximum AC Switching Speeds (Applicable to MSIO I/O Banks Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVPECL AC Specifications						
Dmax	Maximum data rate (for MSIO I/O Bank)		–	–	900	Mbps

8.8.6.2 AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 102 • **LVPECL Receiver Characteristics**
Worst-Case Commercial Conditions: T_J = 85°C, VDD = 1.14 V, Worst-Case VDDI

		t_{PY}		
		Speed Grade		
	On-Die Termination (ODT)	–1	Std	Units
LVPECL (for MSIO I/O Bank)	None	2.572	3.025	ns
	100	2.569	3.023	ns

8.9 I/O Register Specifications

8.9.1 Input Register

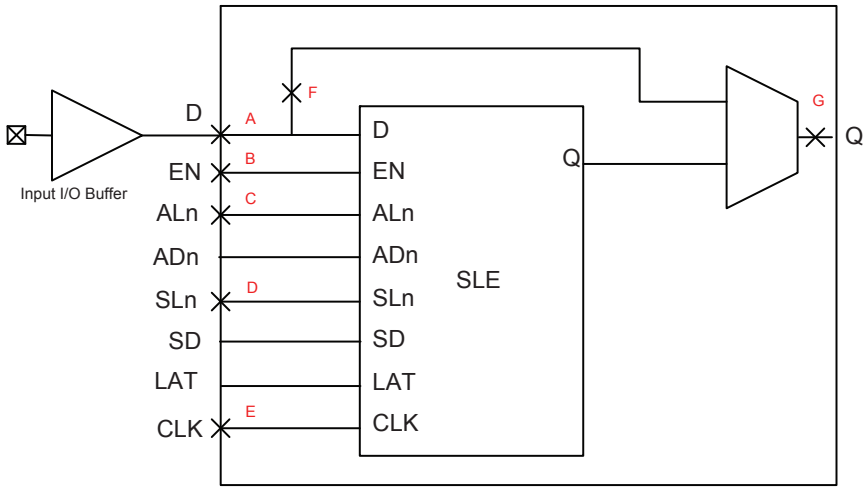

***Figure 5* • Timing Model for Input Register**

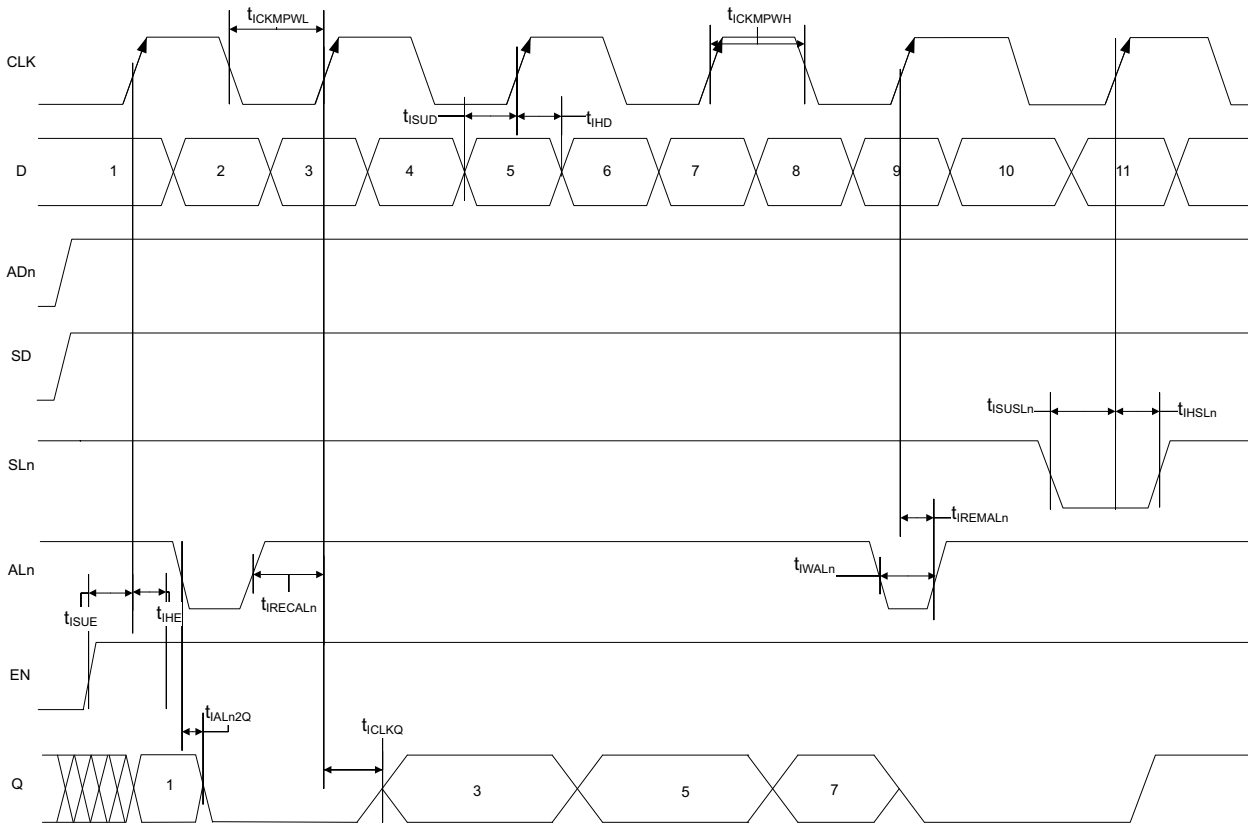

***Figure 6* • I/O Register Input Timing Diagram**

Table 103 • **Input Data Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade		Units
			–1	Std	
t_{IBYP}	Bypass Delay of the Input Register	F,G	0.353	0.415	ns
t_{ICLKQ}	Clock-to-Q of the Input Register	E,G	0.16	0.188	ns
t_{ISUD}	Data Setup Time for the Input Register	A, E	0.357	0.421	ns
t_{IHD}	Data Hold Time for the Input Register	A, E	0	0	ns
t_{ISUE}	Enable Setup Time for the Input Register	B, E	0.46	0.542	ns
t_{IHE}	Enable Hold Time for the Input Register	B, E	0	0	ns
t_{ISUSL}	Synchronous Load Setup Time for the Input Register	D, E	0.46	0.542	ns
t_{IHSL}	Synchronous Load Hold Time for the Input Register	D, E	0	0	ns
t_{IALn2Q}	Asynchronous Clear-to-Q of the Input Register (ADn=1)	C, G	0.625	0.735	ns
	Asynchronous Preset-to-Q of the Input Register (ADn=0)	C, G	0.587	0.69	ns
$t_{IREMALn}$	Asynchronous Load Removal Time for the Input Register	C, E	0	0	ns
$t_{IRECALn}$	Asynchronous Load Recovery Time for the Input Register	C, E	0.074	0.087	ns
t_{IWALn}	Asynchronous Load Minimum Pulse Width for the Input Register	C, C	0.304	0.357	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Register	E, E	0.075	0.088	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Register	E, E	0.159	0.187	ns

*Note: *For the derating values at specific junction temperature and voltage supply levels, refer to Table 14 on page 20 for derating values.*

8.9.2 Output/Enable Register

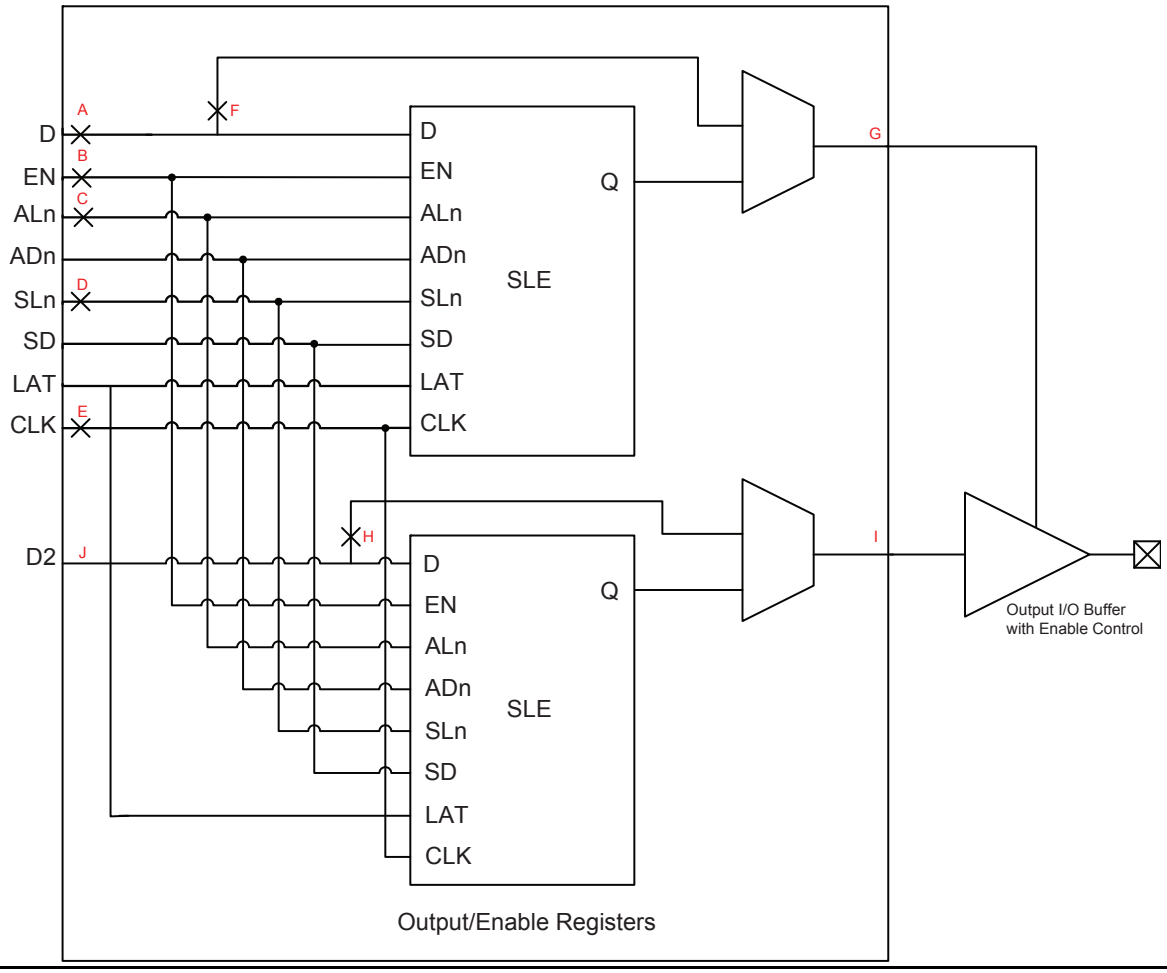

Figure 7 • **Timing Model for Output/Enable Register**

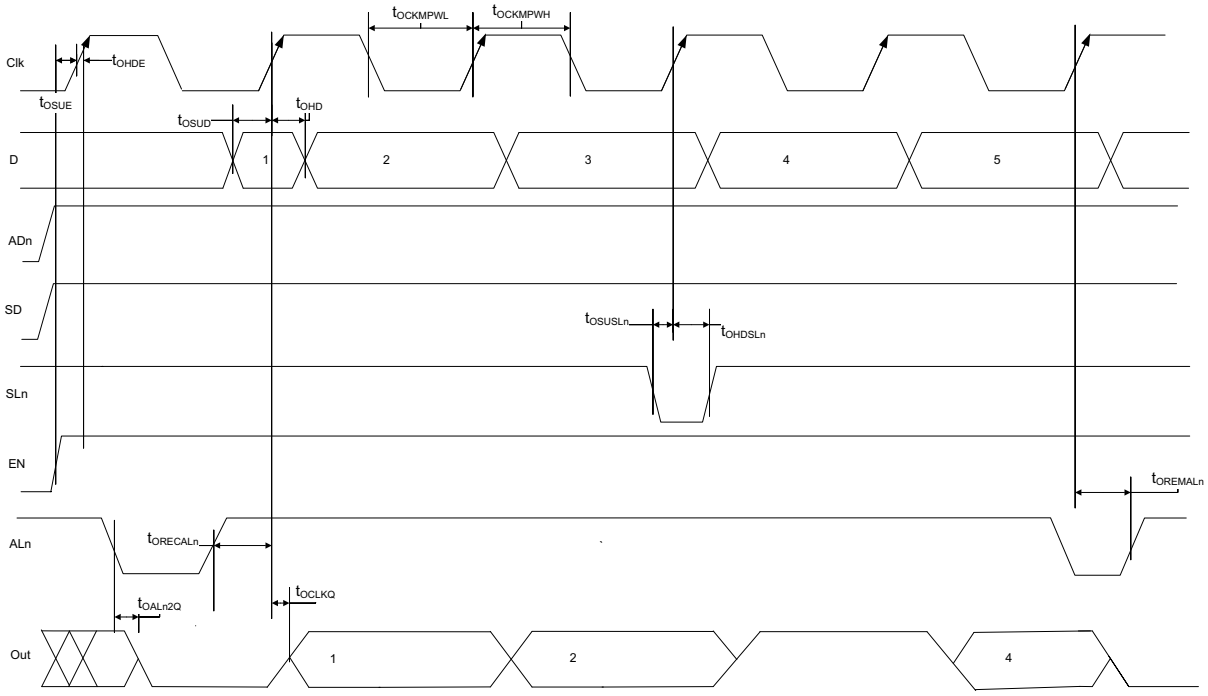

Figure 8 • **I/O Register Output Timing Diagram**

Table 104 • Output/Enable Data Register Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade		Units
			–1	Std	
t_{OBYP}	Bypass Delay of the Output/Enable Register	F, G or H, I	0.353	0.415	ns
t_{OCLKQ}	Clock-to-Q of the Output/Enable Register	E, G or E, I	0.263	0.309	ns
t_{OSUD}	Data Setup Time for the Output/Enable Register	A, E or J, E	0.19	0.223	ns
t_{OHD}	Data Hold Time for the Output/Enable Register	A, E or J, E	0	0	ns
t_{OSUE}	Enable Setup Time for the Output/Enable Register	B, E	0.419	0.493	ns
t_{OHE}	Enable Hold Time for the Output/Enable Register	B, E	0	0	ns
t_{OSUSL}	Synchronous Load Setup Time for the Output/Enable Register	D, E	0.196	0.231	ns
t_{OHSL}	Synchronous Load Hold Time for the Output/Enable Register	D, E	0	0	ns
t_{OALn2Q}	Asynchronous Clear-to-Q of the Output/Enable Register (ADn = 1)	C, G or C, I	0.505	0.594	ns
	Asynchronous Preset-to-Q of the Output/Enable Register (ADn = 0)	C, G or C, I	0.528	0.621	ns
$t_{OREMALn}$	Asynchronous Load Removal Time for the Output/Enable Register	C, E	0	0	ns
$t_{ORECALn}$	Asynchronous Load Recovery Time for the Output/Enable Register	C, E	0.034	0.04	ns
t_{OWALn}	Asynchronous Load Minimum Pulse Width for the Output/Enable Register	C, C	0.304	0.357	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output/Enable Register	E, E	0.075	0.088	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output/Enable Register	E, E	0.159	0.187	ns

*Note: *For the derating values at specific junction temperature and voltage supply levels, refer to Table 14 on page 20 for derating values.*

8.10. DDR Module Specification

8.10.1 Input DDR Module

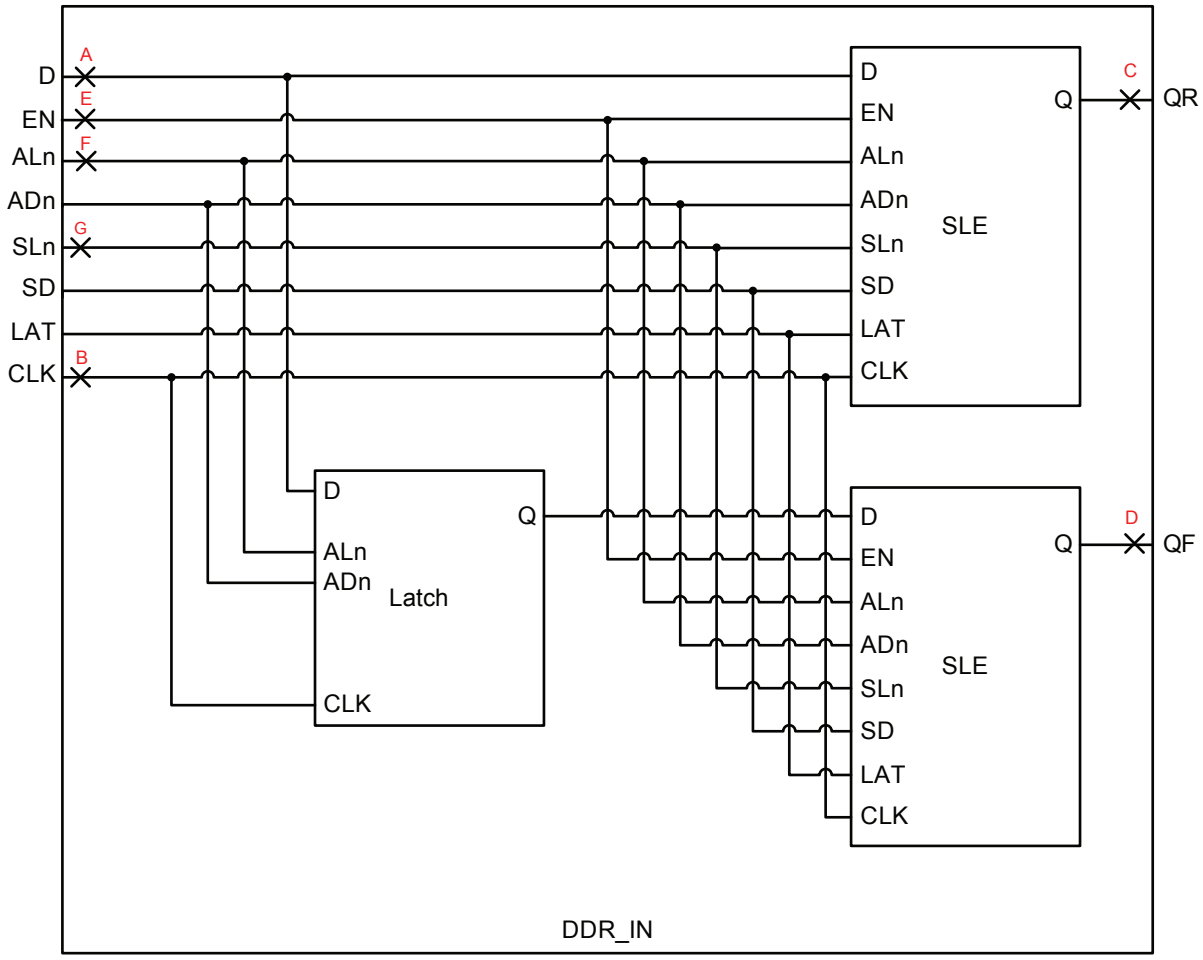

***Figure 9* • Input DDR Module**

8.10.2 Input DDR Timing Diagram

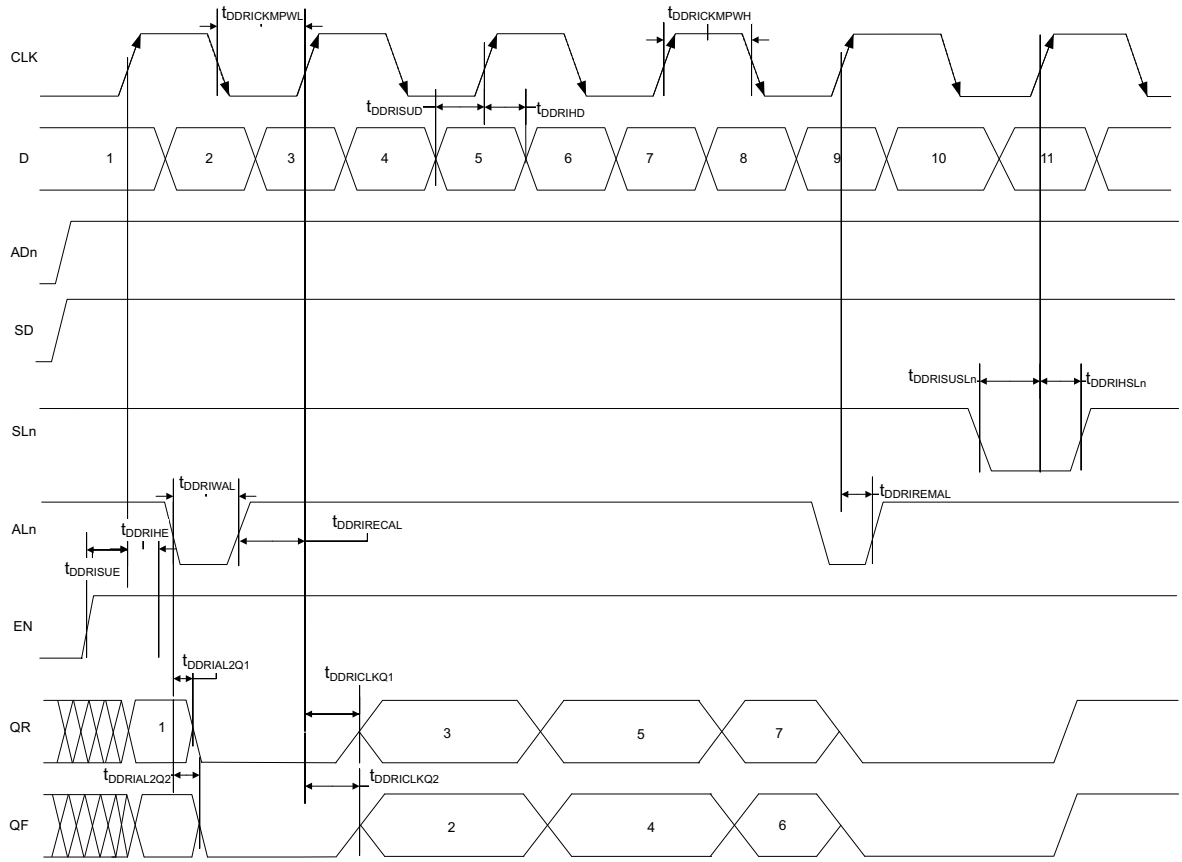

Figure 10 • **Input DDR Timing Diagram**

8.10.3 Timing Characteristics

Table 105 • Input DDR Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)	Speed Grade		Units
			–1	Std	
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	B,C	0.16	0.188	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	B,D	0.166	0.195	ns
$t_{DDRISUD}$	Data Setup for Input DDR	A,B	0.357	0.421	ns
t_{DDRIHD}	Data Hold for Input DDR	A,B	0	0	ns
$t_{DDRISUE}$	Enable Setup for Input DDR	E,B	0.46	0.542	ns
t_{DDRIHE}	Enable Hold for Input DDR	E,B	0	0	ns
$t_{DDRISUSLn}$	Synchronous Load Setup for Input DDR	G,B	0.46	0.542	ns
$t_{DDRIHSLn}$	Synchronous Load Hold for Input DDR	G,B	0	0	ns
$t_{DDRIAL2Q1}$	Asynchronous Load-to-Out QR for Input DDR	F,C	0.587	0.69	ns
$t_{DDRIAL2Q2}$	Asynchronous Load-to-Out QF for Input DDR	F,D	0.541	0.636	ns
$t_{DDRIREMAL}$	Asynchronous Load Removal time for Input DDR	F,B	0	0	ns
$t_{DDRIRECAL}$	Asynchronous Load Recovery time for Input DDR	F,B	0.074	0.087	ns
$t_{DDRIWAL}$	Asynchronous Load Minimum Pulse Width for Input DDR	F,F	0.304	0.357	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	B,B	0.075	0.088	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	B,B	0.159	0.187	ns

8.10.4 Output DDR Module

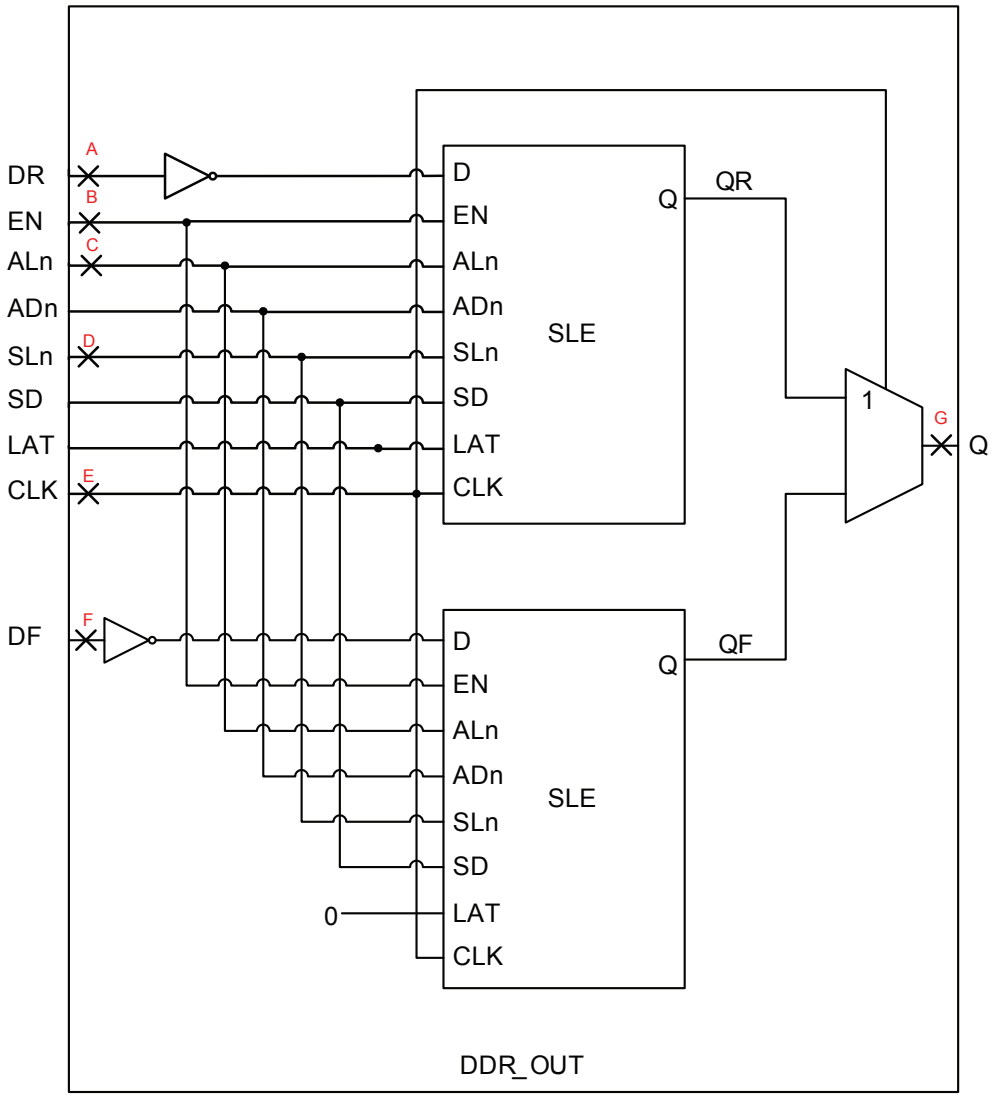

Figure 11 • **Output DDR Module**

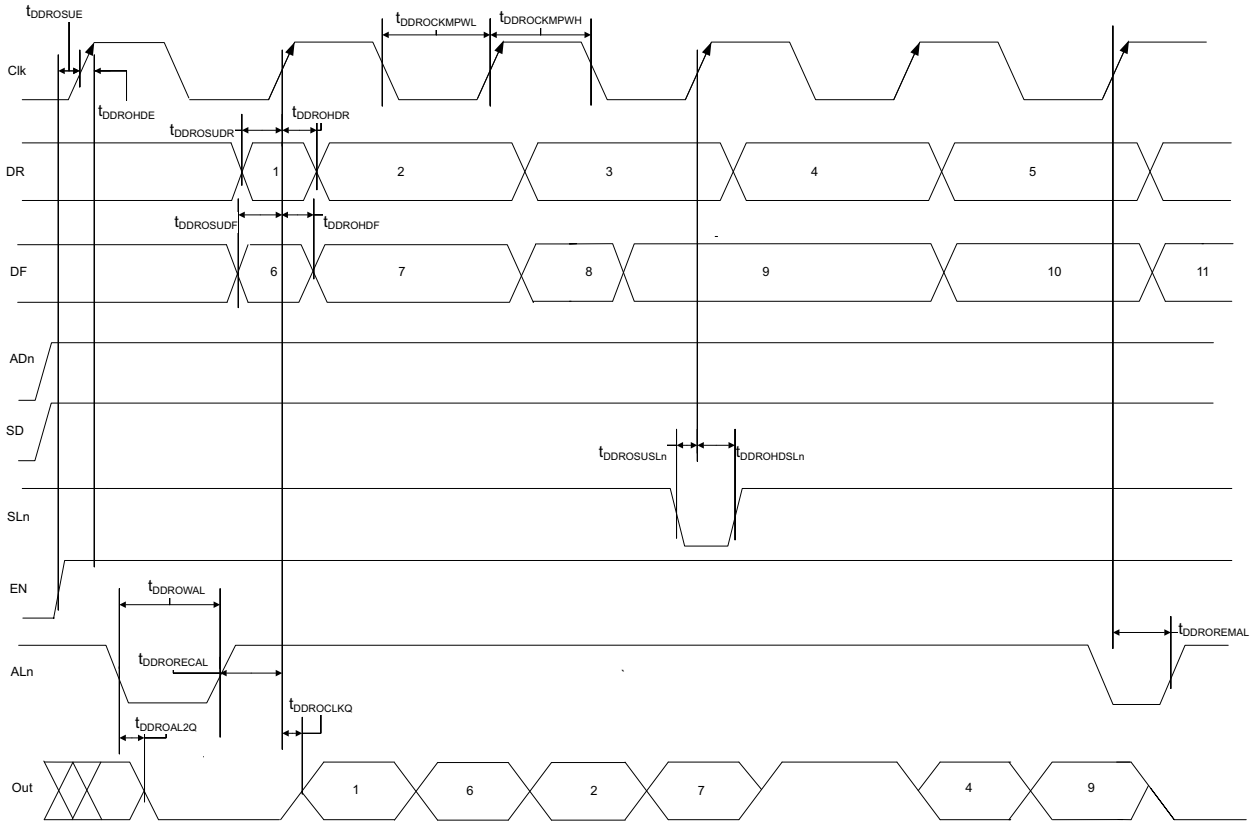

***Figure 12* • Output DDR Timing Diagram**

8.10.5 Timing Characteristics

Table 106 • **Output DDR Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)	Speed Grade		Units
			–1	Std	
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	E,G	0.263	0.309	ns
$t_{DDROSUDF}$	Data_F Data Setup for Output DDR	F,E	0.143	0.168	ns
$t_{DDROSUDR}$	Data_R Data Setup for Output DDR	A,E	0.19	0.223	ns
$t_{DDROHDF}$	Data_F Data Hold for Output DDR	F,E	0	0	ns
$t_{DDROHDR}$	Data_R Data Hold for Output DDR	A,E	0	0	ns
$t_{DDROSUE}$	Enable Setup for Input DDR	B,E	0.419	0.493	ns
t_{DDROHE}	Enable Hold for Input DDR	B,E	0	0	ns
$t_{DDROSUSLn}$	Synchronous Load Setup for Input DDR	D,E	0.196	0.231	ns
$t_{DDROHSLn}$	Synchronous Load Hold for Input DDR	D,E	0	0	ns
$t_{DDROAL2Q}$	Asynchronous Load-to-Out for Output DDR	C,G	0.528	0.621	ns
$t_{DDROREMAL}$	Asynchronous Load Removal time for Output DDR	C,E	0	0	ns
$t_{DDRORECAL}$	Asynchronous Load Recovery time for Output DDR	C,E	0.034	0.04	ns
$t_{DDROWAL}$	Asynchronous Load Minimum Pulse Width for Output DDR	C,C	0.304	0.357	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	E,E	0.075	0.088	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	E,E	0.159	0.187	ns

9. Logic Element Specifications

9.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO2 Macro Library Guide* or the *SmartFusion2 Macro Library Guide*.

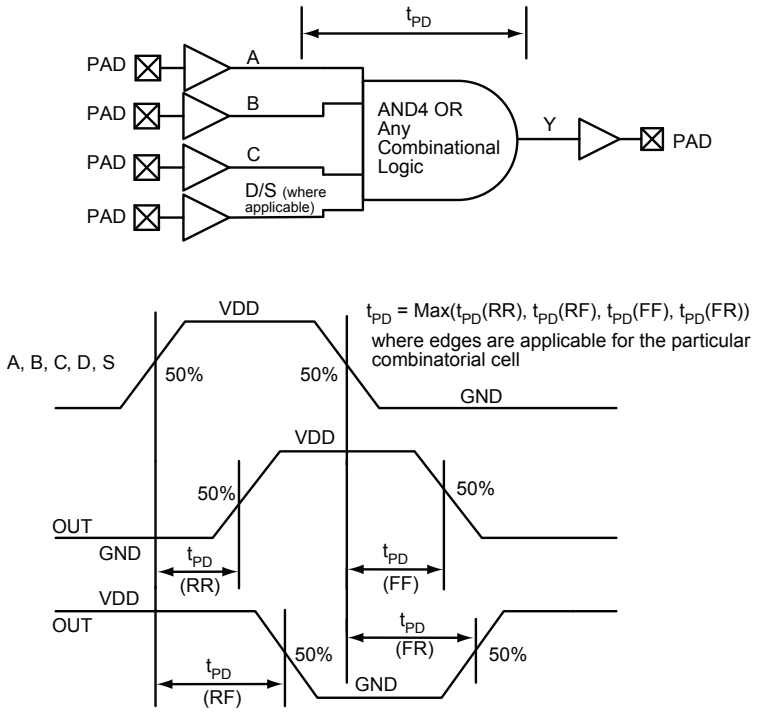

Figure 13 • **LUT-4**

Timing Characteristics

Table 107 • **Combinatorial Cell Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Combinatorial Cell	Equation	Parameter	Speed Grade		Units
			–1	Std	
INV	Y = !A	t_{PD}	0.102	0.12	ns
AND2	Y = A · B	t_{PD}	0.179	0.211	ns
NAND2	Y = !(A · B)	t_{PD}	0.144	0.169	ns
OR2	Y = A + B	t_{PD}	0.179	0.211	ns
NOR2	Y = !(A + B)	t_{PD}	0.144	0.169	ns
XOR2	Y = A ⊕ B	t_{PD}	0.179	0.211	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.241	0.283	ns
AND3	Y = A · B · C	t_{PD}	0.198	0.233	ns
AND4	Y = A · B · C · D	t_{PD}	0.371	0.436	ns

9.2 Sequential Module

IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

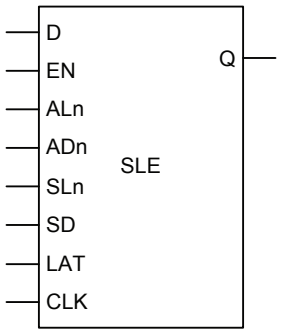

Figure 14 • **Sequential Module**

Figure 15 shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

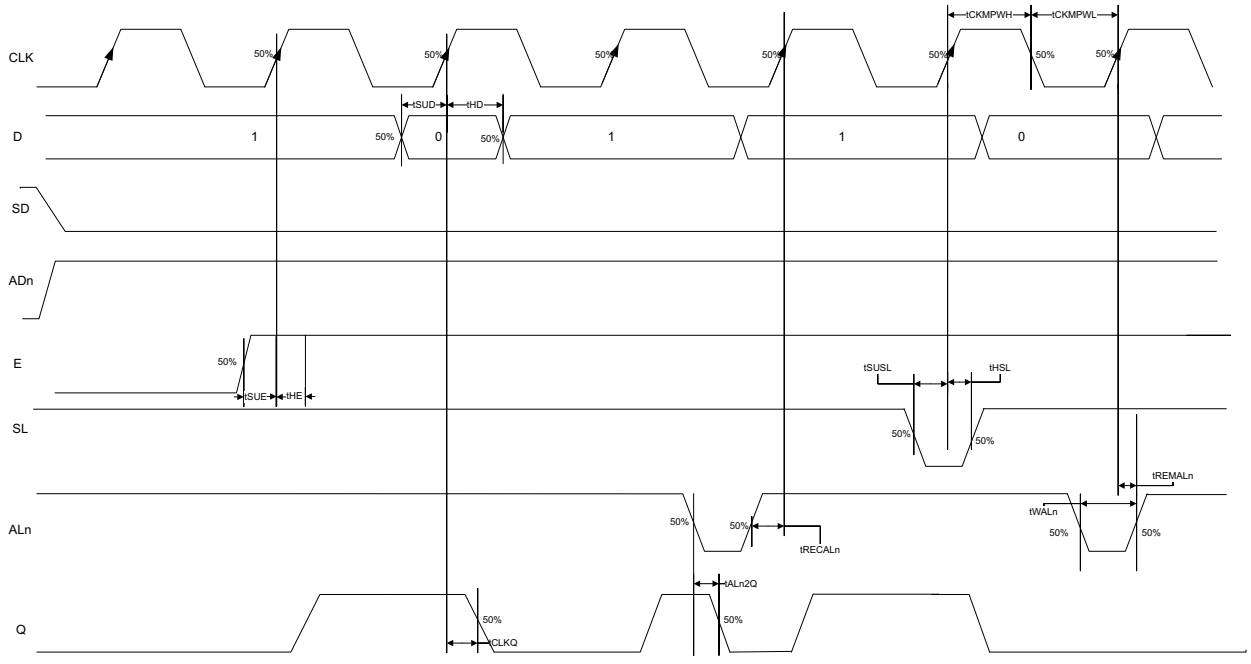

Figure 15 • **Sequential Module Timing Diagram**

9.2.1 Timing Characteristics

Table 108 • **Register Delays**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade		Units
		–1	Std	
t_{CLKQ}	Clock-to-Q of the Core register	0.108	0.127	ns
t_{SUD}	Data Setup Time for the Core register	0.254	0.298	ns
t_{HD}	Data Hold Time for the Core register	0	0	ns
t_{SUE}	Enable Setup Time for the Core register	0.335	0.394	ns
t_{HE}	Enable Hold Time for the Core register	0	0	ns
t_{SUSL}	Synchronous Load Setup Time for the Core register	0.335	0.394	ns
t_{HSL}	Synchronous Load Hold Time for the Core register	0	0	ns
t_{ALn2Q}	Asynchronous Clear-to-Q of the Core register (ADn = 1)	0.473	0.556	ns
	Asynchronous Preset-to-Q of the Core register (ADn = 0)	0.451	0.531	ns
t_{REMALn}	Asynchronous Load Removal Time for the Core register	0	0	ns
t_{RECALn}	Asynchronous Load Recovery Time for the Core register	0.353	0.415	ns
t_{WALn}	Asynchronous Load Minimum Pulse Width for the Core register	0.304	0.357	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core register	0.075	0.088	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core register	0.159	0.187	ns

10. Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. Refer to the *IGLOO2 FPGA Fabric User Guide* or the *SmartFusion2 FPGA Fabric Architecture User Guide* for the positions of various global routing resources. .

Table 109 • **150 Device Global Resource**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.83	0.911	0.831	0.913	ns
t_{RCKH}	Input High Delay for Global Clock	1.457	1.588	1.715	1.869	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.131	–	0.154	ns

Table 110 • **090 Device Global Resource**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.835	0.888	0.833	0.886	ns

Table 110 • 090 Device Global Resource (continued)
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{RCKH}	Input High Delay for Global Clock	1.405	1.489	1.654	1.752	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.084	–	0.098	ns

Table 111 • 050 Device Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.827	0.897	0.826	0.896	ns
t_{RCKH}	Input High Delay for Global Clock	1.419	1.53	1.671	1.8	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.111	–	0.129	ns

Table 112 • 025 Device Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.747	0.799	0.745	0.797	ns
t_{RCKH}	Input High Delay for Global Clock	1.294	1.378	1.522	1.621	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.084	–	0.099	ns

Table 113 • 010 Device Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.626	0.669	0.627	0.668	ns
t_{RCKH}	Input High Delay for Global Clock	1.112	1.182	1.308	1.393	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.07	–	0.085	ns

Table 114 • 005 Device Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.625	0.66	0.628	0.66	ns
t_{RCKH}	Input High Delay for Global Clock	1.126	1.187	1.325	1.397	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.061	–	0.072	ns

11. FPGA Fabric SRAM

Refer to the *IGLOO2 FPGA Fabric User Guide* or *SmartFusion2 FPGA Fabric User Guide* for more information.

11.1 FPGA Fabric Large SRAM (LSRAM)

***Table 115* • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1Kx18**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{CY}	Clock period	2.5	–	2.941	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	1.125	–	1.323	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	1.125	–	1.323	–	ns
t_{PLCY}	Pipelined clock period	2.5	–	2.941	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	1.125	–	1.323	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	1.125	–	1.323	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.334	–	0.393	ns
	Read access time without pipeline register	–	2.273	–	2.674	ns
	Access time with feed-through write timing	–	1.529	–	1.799	ns
t_{ADDRSU}	Address setup time	0.441	–	0.519	–	ns
t_{ADDRHD}	Address hold time	0.274	–	0.322	–	ns
t_{DSU}	Data setup time	0.341	–	0.401	–	ns
t_{DHD}	Data hold time	0.107	–	0.126	–	ns
t_{BLKSU}	Block select setup time	0.207	–	0.244	–	ns
t_{BLKHD}	Block select hold time	0.216	–	0.254	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	1.529	–	1.799	ns
t_{BLKMPW}	Block select minimum pulse width	0.186	–	0.219	–	ns
t_{RDESU}	Read enable setup time	0.449	–	0.528	–	ns
t_{RDEHD}	Read enable hold time	0.167	–	0.197	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.248	–	0.291	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	0.102	–	0.12	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.506	–	1.772	ns
t_{RSTREM}	Asynchronous reset removal time	0.506	–	0.595	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.004	–	0.005	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.301	–	0.354	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.279	–	–0.328	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.327	–	0.385	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.282	–	0.332	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.226	–	0.265	–	ns
t_{SRSTHD}	Synchronous reset hold time	0.036	–	0.043	–	ns
t_{WESU}	Write enable setup time	0.39	–	0.458	–	ns
t_{WEHD}	Write enable hold time	0.242	–	0.285	–	ns
f_{MAX}	Maximum frequency	–	400	–	340	MHz

Table 116 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2Kx9**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{CY}	Clock period	2.5	–	2.941	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	1.125	–	1.323	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	1.125	–	1.323	–	ns
t_{PLCY}	Pipelined clock period	2.5	–	2.941	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	1.125	–	1.323	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	1.125	–	1.323	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.334	–	0.393	ns
	Read access time without pipeline register	–	2.273	–	2.674	ns
	Access time with feed-through write timing	–	1.529	–	1.799	ns
t_{ADDRSU}	Address setup time	0.475	–	0.559	–	ns
t_{ADDRHD}	Address hold time	0.274	–	0.322	–	ns
t_{DSU}	Data setup time	0.336	–	0.395	–	ns
t_{DHD}	Data hold time	0.082	–	0.096	–	ns
t_{BLKSU}	Block select setup time	0.207	–	0.244	–	ns
t_{BLKHD}	Block select hold time	0.216	–	0.254	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	1.529	–	1.799	ns
t_{BLKMPW}	Block select minimum pulse width	0.186	–	0.219	–	ns
t_{RDESU}	Read enable setup time	0.485	–	0.57	–	ns
t_{RDEHD}	Read enable hold time	0.071	–	0.083	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.248	–	0.291	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	0.102	–	0.12	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.514	–	1.781	ns
t_{RSTREM}	Asynchronous reset removal time	0.506	–	0.595	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.004	–	0.005	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.301	–	0.354	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.279	–	–0.328	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.327	–	0.385	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.282	–	0.332	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.226	–	0.265	–	ns
t_{SRSTHD}	Synchronous reset hold time	0.036	–	0.043	–	ns
t_{WESU}	Write enable setup time	0.415	–	0.488	–	ns
t_{WEHD}	Write enable hold time	0.048	–	0.057	–	ns
f_{MAX}	Maximum frequency	–	400	–	340	MHz

Table 117 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4Kx4
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{CY}	Clock period	2.5	–	2.941	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	1.125	–	1.323	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	1.125	–	1.323	–	ns
t_{PLCY}	Pipelined clock period	2.5	–	2.941	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	1.125	–	1.323	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	1.125	–	1.323	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.323	–	0.38	ns
	Read access time without pipeline register	–	2.273	–	2.673	ns
	Access time with feed-through write timing	–	1.511	–	1.778	ns
t_{ADDRSU}	Address setup time	0.543	–	0.638	–	ns
t_{ADDRHD}	Address hold time	0.274	–	0.322	–	ns
t_{DSU}	Data setup time	0.334	–	0.393	–	ns
t_{DHD}	Data hold time	0.082	–	0.096	–	ns
t_{BLKSU}	Block select setup time	0.207	–	0.244	–	ns
t_{BLKHD}	Block select hold time	0.216	–	0.254	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	1.511	–	1.778	ns
t_{BLKMPW}	Block select minimum pulse width	0.186	–	0.219	–	ns
t_{RDESU}	Read enable setup time	0.516	–	0.607	–	ns
t_{RDEHD}	Read enable hold time	0.071	–	0.083	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.248	–	0.291	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	0.102	–	0.12	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.507	–	1.773	ns
t_{RSTREM}	Asynchronous reset removal time	0.506	–	0.595	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.004	–	0.005	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.301	–	0.354	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.279	–	–0.328	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.327	–	0.385	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.282	–	0.332	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.226	–	0.265	–	ns
t_{SRSTHD}	Synchronous reset hold time	0.036	–	0.043	–	ns
t_{WESU}	Write enable setup time	0.458	–	0.539	–	ns
t_{WEHD}	Write enable hold time	0.048	–	0.057	–	ns
f_{MAX}	Maximum frequency	–	400	–	340	MHz

Table 118 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8Kx2
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{CY}	Clock period	2.5	–	2.941	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	1.125	–	1.323	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	1.125	–	1.323	–	ns
t_{PLCY}	Pipelined clock period	2.5	–	2.941	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	1.125	–	1.323	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	1.125	–	1.323	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.32	–	0.377	ns
	Read access time without pipeline register	–	2.272	–	2.673	ns
	Access time with feed-through write timing	–	1.511	–	1.778	ns
t_{ADDRSU}	Address setup time	0.612	–	0.72	–	ns
t_{ADDRHD}	Address hold time	0.274	–	0.322	–	ns
t_{DSU}	Data setup time	0.33	–	0.388	–	ns
t_{DHD}	Data hold time	0.082	–	0.096	–	ns
t_{BLKSU}	Block select setup time	0.207	–	0.244	–	ns
t_{BLKHD}	Block select hold time	0.216	–	0.254	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	1.511	–	1.778	ns
t_{BLKMPW}	Block select minimum pulse width	0.186	–	0.219	–	ns
t_{RDESU}	Read enable setup time	0.529	–	0.622	–	ns
t_{RDEHD}	Read enable hold time	0.071	–	0.083	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.248	–	0.291	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	0.102	–	0.12	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.528	–	1.797	ns
t_{RSTREM}	Asynchronous reset removal time	0.506	–	0.595	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.004	–	0.005	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.301	–	0.354	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.279	–	–0.328	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.327	–	0.385	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.282	–	0.332	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.226	–	0.265	–	ns
t_{SRSTHD}	Synchronous reset hold time	0.036	–	0.043	–	ns
t_{WESU}	Write enable setup time	0.488	–	0.574	–	ns
t_{WEHD}	Write enable hold time	0.048	–	0.057	–	ns
f_{MAX}	Maximum frequency	–	400	–	340	MHz

Table 119 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16Kx1
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{CY}	Clock period	2.5	–	2.941	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	1.125	–	1.323	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	1.125	–	1.323	–	ns
t_{PLCY}	Pipelined clock period	2.5	–	2.941	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	1.125	–	1.323	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	1.125	–	1.323	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.32	–	0.377	ns
	Read access time without pipeline register	–	2.269	–	2.669	ns
	Access time with feed-through write timing	–	1.51	–	1.777	ns
t_{ADDRSU}	Address setup time	0.626	–	0.737	–	ns
t_{ADDRHD}	Address hold time	0.274	–	0.322	–	ns
t_{DSU}	Data setup time	0.322	–	0.378	–	ns
t_{DHD}	Data hold time	0.082	–	0.096	–	ns
t_{BLKSU}	Block select setup time	0.207	–	0.244	–	ns
t_{BLKHD}	Block select hold time	0.216	–	0.254	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	1.51	–	1.777	ns
t_{BLKMPW}	Block select minimum pulse width	0.186	–	0.219	–	ns
t_{RDESU}	Read enable setup time	0.53	–	0.624	–	ns
t_{RDEHD}	Read enable hold time	0.071	–	0.083	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.248	–	0.291	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	0.102	–	0.12	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.547	–	1.82	ns
t_{RSTREM}	Asynchronous reset removal time	0.506	–	0.595	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.004	–	0.005	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.301	–	0.354	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.279	–	–0.328	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.327	–	0.385	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.282	–	0.332	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.226	–	0.265	–	ns
t_{SRSTHD}	Synchronous reset hold time	0.036	–	0.043	–	ns
t_{WESU}	Write enable setup time	0.454	–	0.534	–	ns
t_{WEHD}	Write enable hold time	0.048	–	0.057	–	ns
f_{MAX}	Maximum frequency	–	400	–	340	MHz

Table 120 • **RAM1K18 – Two-Port Mode for Depth × Width Configuration 512x36**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{CY}	Clock period	2.5	–	2.941	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	1.125	–	1.323	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	1.125	–	1.323	–	ns
t_{PLCY}	Pipelined clock period	2.5	–	2.941	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	1.125	–	1.323	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	1.125	–	1.323	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.334	–	0.393	ns
	Read access time without pipeline register	–	2.25	–	2.647	ns
t_{ADDRSU}	Address setup time	0.313	–	0.368	–	ns
t_{ADDRHD}	Address hold time	0.274	–	0.322	–	ns
t_{DSU}	Data setup time	0.337	–	0.396	–	ns
t_{DHD}	Data hold time	0.111	–	0.13	–	ns
t_{BLKSU}	Block select setup time	0.207	–	0.244	–	ns
t_{BLKHD}	Block select hold time	0.201	–	0.237	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	2.25	–	2.647	ns
t_{BLKMPW}	Block select minimum pulse width	0.186	–	0.219	–	ns
t_{RDESU}	Read enable setup time	0.449	–	0.528	–	ns
t_{RDEHD}	Read enable hold time	0.167	–	0.197	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.248	–	0.291	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	0.102	–	0.12	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.506	–	1.772	ns
t_{RSTREM}	Asynchronous reset removal time	0.506	–	0.595	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.004	–	0.005	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.301	–	0.354	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.279	–	–0.328	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.327	–	0.385	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.282	–	0.332	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.226	–	0.265	–	ns
t_{SRSTHD}	Synchronous reset hold time	0.036	–	0.043	–	ns
t_{WESU}	Write enable setup time	0.39	–	0.458	–	ns
t_{WEHD}	Write enable hold time	0.242	–	0.285	–	ns
f_{MAX}	Maximum frequency	–	400	–	340	MHz

11.2. FPGA Fabric Micro SRAM (uSRAM)

Table 121 • **uSRAM (RAM64x18) in 64x18 Mode**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{CY}	Read clock period	4	–	4	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{PLCY}	Read pipeline clock period	4	–	4	–	ns
$t_{PLCLKMPWH}$	Read pipeline clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{PLCLKMPWL}$	Read pipeline clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.266	–	0.313	ns
	Read access time without pipeline register	–	1.677	–	1.973	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.301	–	0.354	–	ns
	Read address setup time in asynchronous mode	1.856	–	2.184	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.091	–	0.107	–	ns
	Read address hold time in asynchronous mode	–0.778	–	–0.915	–	ns
t_{RDENSU}	Read enable setup time	0.278	–	0.327	–	ns
t_{RDENHD}	Read enable hold time	0.057	–	0.067	–	ns
t_{BLKSU}	Read block select setup time	1.839	–	2.163	–	ns
t_{BLKHD}	Read block select hold time	–0.65	–	–0.765	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.036		2.396	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	–0.023	–	–0.027	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.046	–	0.054	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.507	–	0.597	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.236	–	0.278	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	0.839		0.987	ns
t_{SRSTSU}	Read synchronous reset setup time	0.271	–	0.319	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.061	–	0.071	–	ns
t_{CCY}	Write clock period	4	–	4	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{BLKCSU}	Write block setup time	0.404	–	0.476	–	ns
t_{BLKCHD}	Write block hold time	0.007	–	0.008	–	ns
t_{DINCSU}	Write input data setup time	0.115	–	0.135	–	ns
t_{DINCHD}	Write input data hold time	0.15	–	0.177	–	ns
$t_{ADDRCSU}$	Write address setup time	0.088	–	0.104	–	ns
$t_{ADDRCHD}$	Write address hold time	0.128	–	0.15	–	ns

Table 121 • **uSRAM (RAM64x18) in 64x18 Mode (continued)**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{WECSU}	Write enable setup time	0.397	–	0.467	–	ns
t_{WECHD}	Write enable hold time	–0.026		–0.03	–	ns
f_{MAX}	Maximum frequency	–	250	–	250	MHz

Table 122 • **uSRAM (RAM64x16) in 64x16 Mode**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{CY}	Read clock period	4	–	4	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{PLCY}	Read pipeline clock period	4	–	4	–	ns
$t_{PLCLKMPWH}$	Read pipeline clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{PLCLKMPWL}$	Read pipeline clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.266	–	0.313	ns
	Read access time without pipeline register	–	1.677	–	1.973	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.301	–	0.354	–	ns
	Read address setup time in asynchronous mode	1.856	–	2.184	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.091	–	0.107	–	ns
	Read address hold time in asynchronous mode	–0.778	–	–0.915	–	ns
t_{RDENSU}	Read enable setup time	0.278	–	0.327	–	ns
t_{RDENHD}	Read enable hold time	0.057	–	0.067	–	ns
t_{BLKSU}	Read block select setup time	1.839	–	2.163	–	ns
t_{BLKHD}	Read block select hold time	–0.65	–	–0.765	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.036	–	2.396	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	–0.023	–	–0.027	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.046	–	0.054	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.507	–	0.597	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.236	–	0.278	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	0.835	–	0.983	ns
t_{SRSTSU}	Read synchronous reset setup time	0.271	–	0.319	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.061	–	0.071	–	ns
t_{CCY}	Write clock period	4	–	4	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	1.8	–	1.8	–	ns

Table 122 • **uSRAM (RAM64x16) in 64x16 Mode (continued)**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{BLKCSU}	Write block setup time	0.404	–	0.476	–	ns
t_{BLKCHD}	Write block hold time	0.007	–	0.008	–	ns
t_{DINCSU}	Write input data setup time	0.115	–	0.135	–	ns
t_{DINCHD}	Write input data hold time	0.15	–	0.177	–	ns
$t_{ADDRCSU}$	Write address setup time	0.088	–	0.104	–	ns
$t_{ADDRCHD}$	Write address hold time	0.128	–	0.15	–	ns
t_{WECSU}	Write enable setup time	0.397	–	0.467	–	ns
t_{WECHD}	Write enable hold time	–0.026	–	–0.03	–	ns
f_{MAX}	Maximum frequency	–	250	–	250	MHz

Table 123 • **uSRAM (RAM128x9) in 128x9 Mode**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{CY}	Read clock period	4	–	4	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{PLCY}	Read pipeline clock period	4	–	4	–	ns
$t_{PLCLKMPWH}$	Read pipeline clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{PLCLKMPWL}$	Read pipeline clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.266	–	0.313	ns
	Read access time without pipeline register	–	1.677	–	1.973	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.301	–	0.354	–	ns
	Read address setup time in asynchronous mode	1.856	–	2.184	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.091	–	0.107	–	ns
	Read address hold time in asynchronous mode	–0.778	–	–0.915	–	ns
t_{RDENSU}	Read enable setup time	0.278	–	0.327	–	ns
t_{RDENHD}	Read enable hold time	0.057	–	0.067	–	ns
t_{BLKSU}	Read block select setup time	1.839	–	2.163	–	ns
t_{BLKHD}	Read block select hold time	–0.65	–	–0.765	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.036	–	2.396	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	–0.023	–	–0.027	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.046	–	0.054	–	ns

Table 123 • **uSRAM (RAM128x9) in 128x9 Mode (continued)**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.507	–	0.597	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.236	–	0.278	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)		0.835		0.982	ns
t_{SRSTSU}	Read synchronous reset setup time	0.271	–	0.319	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.061	–	0.071	–	ns
t_{CCY}	Write clock period	4	–	4	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{BLKCSU}	Write block setup time	0.404	–	0.476	–	ns
t_{BLKCHD}	Write block hold time	0.007	–	0.008	–	ns
t_{DINCSU}	Write input data setup time	0.115	–	0.135	–	ns
t_{DINCHD}	Write input data hold time	0.15	–	0.177	–	ns
$t_{ADDRCSU}$	Write address setup time	0.088	–	0.104	–	ns
$t_{ADDRCHD}$	Write address hold time	0.128	–	0.15	–	ns
t_{WECSU}	Write enable setup time	0.397	–	0.467	–	ns
t_{WECHD}	Write enable hold time	–0.026	–	–0.03	–	ns
f_{MAX}	Maximum frequency	–	250	–	250	MHz

Table 124 • **uSRAM (RAM128x8) in 128x8 Mode**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{CY}	Read clock period	4	–	4	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{PLCY}	Read pipeline clock period	4	–	4	–	ns
$t_{PLCLKMPWH}$	Read pipeline clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{PLCLKMPWL}$	Read pipeline clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.266	–	0.313	ns
	Read access time without pipeline register	–	1.677	–	1.973	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.301	–	0.354	–	ns
	Read address setup time in asynchronous mode	1.856	–	2.184	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.091	–	0.107	–	ns
	Read address hold time in asynchronous mode	–0.778	–	–0.915	–	ns
t_{RDENSU}	Read enable setup time	0.278	–	0.327	–	ns

Table 124 • **uSRAM (RAM128x8) in 128x8 Mode (continued)**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{RDENHD}	Read enable hold time	0.057	–	0.067	–	ns
t_{BLKSU}	Read block select setup time	1.839	–	2.163	–	ns
t_{BLKHD}	Read block select hold time	–0.65	–	–0.765	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)		2.036		2.396	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	–0.023	–	–0.027	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.046	–	0.054	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.507	–	0.597	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.236	–	0.278	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	0.835	–	0.982	ns
t_{SRSTSU}	Read synchronous reset setup time	0.271	–	0.319	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.061	–	0.071	–	ns
t_{CCY}	Write clock period	4	–	4	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{BLKCSU}	Write block setup time	0.404	–	0.476	–	ns
t_{BLKCHD}	Write block hold time	0.007	–	0.008	–	ns
t_{DINCSU}	Write input data setup time	0.115	–	0.135	–	ns
t_{DINCHD}	Write input data hold time	0.15	–	0.177	–	ns
$t_{ADDRCSU}$	Write address setup time	0.088	–	0.104	–	ns
$t_{ADDRCHD}$	Write address hold time	0.128	–	0.15	–	ns
t_{WECSU}	Write enable setup time	0.397	–	0.467	–	ns
t_{WECHD}	Write enable hold time	–0.026	–	–0.03	–	ns
f_{MAX}	Maximum frequency	–	250	–	250	MHz

Table 125 • **uSRAM (RAM256x4) in 256x4 Mode**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{CY}	Read clock period	4	–	4	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{PLCY}	Read pipeline clock period	4	–	4	–	ns
$t_{PLCLKMPWH}$	Read pipeline clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{PLCLKMPWL}$	Read pipeline clock minimum pulse width Low	1.8	–	1.8	–	ns

Table 125 • **uSRAM (RAM256x4) in 256x4 Mode (continued)**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{CLK2Q}	Read access time with pipeline register	–	0.27		0.31	ns
	Read access time without pipeline register	–	1.75		2.06	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.301	–	0.354	–	ns
	Read address setup time in asynchronous mode	1.931	–	2.272	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.121	–	0.142	–	ns
	Read address hold time in asynchronous mode	–0.65	–	–0.76	–	ns
t_{RDENSU}	Read enable setup time	0.278	–	0.327	–	ns
t_{RDENHD}	Read enable hold time	0.057	–	0.067	–	ns
t_{BLKSU}	Read block select setup time	1.839	–	2.163	–	ns
t_{BLKHD}	Read block select hold time	–0.65		–0.77		ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.09	–	2.46	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	–0.02	–	–0.03	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.046	–	0.054	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.507	–	0.597	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.236	–	0.278	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	0.83	–	0.98	ns
t_{SRSTSU}	Read synchronous reset setup time	0.271	–	0.319	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.061	–	0.071	–	ns
t_{CCY}	Write clock period	4	–	4	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{BLKCSU}	Write block setup time	0.404	–	0.476	–	ns
t_{BLKCHD}	Write block hold time	0.007	–	0.008	–	ns
t_{DINCSU}	Write input data setup time	0.101	–	0.118	–	ns
t_{DINCHD}	Write input data hold time	0.137	–	0.161	–	ns
$t_{ADDRCSU}$	Write address setup time	0.088	–	0.104	–	ns
$t_{ADDRCHD}$	Write address hold time	0.245	–	0.288	–	ns
t_{WECSU}	Write enable setup time	0.397	–	0.467	–	ns
t_{WECHD}	Write enable hold time	–0.03	–	–0.03	–	ns
f_{MAX}	Maximum frequency	–	250	–	250	MHz

Table 126 • **uSRAM (RAM512x2) in 512x2 Mode**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{CY}	Read clock period	4	–	4	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{PLCY}	Read pipeline clock period	4	–	4	–	ns
$t_{PLCLKMPWH}$	Read pipeline clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{PLCLKMPWL}$	Read pipeline clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.27	–	0.31	ns
	Read access time without pipeline register	–	1.76	–	2.08	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.301	–	0.354	–	ns
	Read address setup time in asynchronous mode	1.96	–	2.306	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.137	–	0.161	–	ns
	Read address hold time in asynchronous mode	–0.58	–	–0.68	–	ns
t_{RDENSU}	Read enable setup time	0.278	–	0.327	–	ns
t_{RDENHD}	Read enable hold time	0.057	–	0.067	–	ns
t_{BLKSU}	Read block select setup time	1.839	–	2.163	–	ns
t_{BLKHD}	Read block select hold time	–0.65	–	–0.77	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.14	–	2.52	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	–0.02	–	–0.03	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.046	–	0.054	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.507	–	0.597	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.236	–	0.278	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	0.83	–	0.98	ns
t_{SRSTSU}	Read synchronous reset setup time	0.271	–	0.319	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.061	–	0.071	–	ns
t_{CCY}	Write clock period	4	–	4	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{BLKCSU}	Write block setup time	0.404	–	0.476	–	ns
t_{BLKCHD}	Write block hold time	0.007	–	0.008	–	ns
t_{DINCSU}	Write input data setup time	0.101	–	0.118	–	ns
t_{DINCHD}	Write input data hold time	0.137	–	0.161	–	ns
$t_{ADDRCSU}$	Write address setup time	0.088	–	0.104	–	ns
$t_{ADDRCHD}$	Write address hold time	0.247	–	0.29	–	ns
t_{WECSU}	Write enable setup time	0.397	–	0.467	–	ns

Table 126 • **uSRAM (RAM512x2) in 512x2 Mode (continued)**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{WECHD}	Write enable hold time	–0.03	–	–0.03	–	ns
f_{MAX}	Maximum frequency	–	250	–	250	MHz

Table 127 • **uSRAM (RAM1024x1) in 1024x1 Mode**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{CY}	Read clock period	4	–	4	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{PLCY}	Read pipeline clock period	4	–	4	–	ns
$t_{PLCLKMPWH}$	Read pipeline clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{PLCLKMPWL}$	Read pipeline clock minimum pulse width Low	1.8	–	1.8	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.27	–	0.31	ns
	Read access time without pipeline register	–	1.78	–	2.1	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.301	–	0.354	–	ns
	Read address setup time in asynchronous mode	1.978	–	2.327	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.137	–	0.161	–	ns
	Read address hold time in asynchronous mode	–0.6	–	–0.71	–	ns
t_{RDENSU}	Read enable setup time	0.278	–	0.327	–	ns
t_{RDENHD}	Read enable hold time	0.057	–	0.067	–	ns
t_{BLKSU}	Read block select setup time	1.839	–	2.163	–	ns
t_{BLKHD}	Read block select hold time	–0.65	–	–0.77	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.16	–	2.54	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	–0.02	–	–0.03	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.046	–	0.054	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.507	–	0.597	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.236	–	0.278	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	0.83	–	0.98	ns
t_{SRSTSU}	Read synchronous reset setup time	0.271	–	0.319	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.061	–	0.071	–	ns
t_{CCY}	Write clock period	4	–	4	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	1.8	–	1.8	–	ns
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	1.8	–	1.8	–	ns

Table 127 • **uSRAM (RAM1024x1) in 1024x1 Mode (continued)**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{BLKCSU}	Write block setup time	0.404	–	0.476	–	ns
t_{BLKCHD}	Write block hold time	0.007	–	0.008	–	ns
t_{DINCSU}	Write input data setup time	0.003	–	0.004	–	ns
t_{DINCHD}	Write input data hold time	0.137	–	0.161	–	ns
$t_{ADDRCSU}$	Write address setup time	0.088	–	0.104	–	ns
$t_{ADDRCHD}$	Write address hold time	0.247	–	0.29	–	ns
t_{WECSU}	Write enable setup time	0.397	–	0.467	–	ns
t_{WECHD}	Write enable hold time	–0.03	–	–0.03	–	ns
f_{MAX}	Maximum frequency	–	250	–	250	MHz

12. Embedded NVM (eNVM) Characteristics

Table 128 • **eNVM Read Performance**
Worst-Case Conditions: VDD = 1.14 V, VPPNVM = VPP = 2.375 V

Symbol	Description	Operating Temperature Range						Unit
T_j	Junction Temperature Range	-55°C to 125°C		-40°C to 100°C		0°C to 85°C		°C
Speed grade		-1	Std	-1	Std	-1	Std	
$F_{MAXREAD}$	eNVM Maximum Read Frequency	25	25	25	25	25	25	MHz

Table 129 • **eNVM Page Programming**
Worst-Case Conditions: VDD = 1.14 V, VPPNVM = VPP = 2.375 V

Symbol	Description	Operating Temperature Range						Unit
T_j	Junction Temperature Range	-55°C to 125°C		-40°C to 100°C		0°C to 85°C		°C
Speed grade		-1	Std	-1	Std	-1	Std	
$t_{PAGEPGM}$	eNVM Page Programming Time	40	40	40	40	40	40	ms

13. Crystal Oscillator

Table 130 describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

Table 130 • **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)**

Parameter	Description	Condition	Min	Typ	Max	Units
FXTAL	Operating frequency		–	20	–	MHz
ACCXTAL	Accuracy	005, 010, 025, 050, and 090 Devices	–	–	0.0047	%
		150 Devices	–	–	0.0058	%
CYCXTAL	Output duty cycle		–	49–51	47–53	%
JITPERXTAL	Output Period Jitter (peak to peak)		–	200	300	ps
JITCYCXTAL	Output Cycle to Cycle Jitter (peak to peak)	010, 025, and 050 Devices	–	200	300	ps
		150 Devices	–	250	410	ps
		005 and 090 Devices	–	250	550	ps
IDYNXTAL	Operating current	010 and 050 Devices	–	1.5	–	mA
		005, 025, 090, and 150 Devices	–	1.65	–	mA
VIHXTAL	Input logic level High		0.9 VPP	–	–	V
VILXTAL	Input logic level Low		–	–	0.1 VPP	V
SUXTAL	Startup time (with regard to stable oscillator output)	005, 010, 025, and 050 Devices	–	–	0.8	ms
		090 and 150 Devices	–	–	1.0	ms

Table 131 • **Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)**

Parameter	Description	Condition	Min	Typ	Max	Units
FXTAL	Operating frequency		–	2	–	MHz
ACCXTAL	Accuracy	050 Devices	–	–	0.00105	%
		005, 010, 025, 090, and 150 Devices	–	–	0.003	%
CYCXTAL	Output duty cycle		–	49–51	47–53	%
JITPERXTAL	Output Period Jitter (peak to peak)		–	1	5	ns
JITCYCXTAL	Output Cycle to Cycle Jitter (peak to peak)		–	1	5	ns
IDYNXTAL	Operating current		–	0.3	–	mA
VIHXTAL	Input logic level High		0.9 VPP	–	–	V
VILXTAL	Input logic level Low		–	–	0.1 VPP	V

Table 131 • **Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz) (continued)**

SUXTAL	Startup time (with regard to stable oscillator output)	010 and 050 Devices	–	–	4.5	ms
		005 and 025 Devices	–	–	5	ms
		090 and 150 Devices	–	–	7	ms

Table 132 • **Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)**

Parameter	Description	Condition	Min	Typ	Max	Units
FXTAL	Operating frequency		–	32	–	kHz
ACCXTAL	Accuracy	005, 010, 025, 050, and 090 Devices	–	–	0.004	%
		150 Devices	–	–	0.005	%
CYCXTAL	Output duty cycle		–	49–51	47–53	%
JITPERXTAL	Output Period Jitter (peak to peak)		–	150	300	ns
JITCYCXTAL	Output Cycle to Cycle Jitter (peak to peak)		–	150	300	ns
IDYNXTAL	Operating current	010 and 050 Devices	–	0.044	–	mA
		005, 025, 090, and 150 Devices	–	0.060	–	mA
VIHXTAL	Input logic level High		0.9 VPP	–	–	V
VILXTAL	Input logic level Low		–	–	0.1 VPP	V
SUXTAL	Startup time (with regard to stable oscillator output)	005, 025, 050, 090, and 150 Devices	–	–	115	ms
		010 Devices	–	–	126	ms

14. On-Chip Oscillator

Table 133 and Table 134 describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

Table 133 • **Electrical Characteristics of the 50 MHz RC Oscillator**

Parameter	Description	Condition	Min	Typ	Max	Units
F50RC	Operating frequency		–	50	–	MHz
ACC50RC	Accuracy	050 Devices	–	1	4	%
		005 and 025 Devices	–	1	5	%
		090 Devices	–	1	6.3	%
		010 and 150 Devices	–	1	7.1	%
CYC50RC	Output duty cycle		–	49–51	46.5–53.5	%
JIT50RC	Output jitter (peak to peak)	Period Jitter				
		005, 010, 050 Devices	–	200	300	ps
		150 Devices	–	200	400	ps
		025 and 090 Devices	–	300	500	ps
		Cycle-to-Cycle Jitter				
		005 and 050Devices	–	200	300	ps
		010 and 150 Devices	–	320	420	ps
		025 and 090 Devices	–	320	850	ps
IDYN50RC	Operating current		–	6.5	–	mA

Table 134 • **Electrical Characteristics of the 1 MHz RC Oscillator**

Parameter	Description	Condition	Min	Typ	Max	Units
F1RC	Operating frequency		–	1	–	MHz
ACC1RC	Accuracy	005, 010, 025, and 050 Devices	–	1	3	%
		150 Devices	–	1	4.5	%
		090 Devices	–	1	5.6	%
CYC1RC	Output duty cycle		–	49–51	46.5–53.5	%
JIT1RC	Output jitter (peak to peak)	Period Jitter				
		005, 010, 025, and 050 Devices	–	10	20	ns
		090 and 150 Devices	–	10	28	ns
		Cycle-to-Cycle Jitter				
		005, 010, and 050 Devices	–	10	20	ns
		025 and 150 Devices	–	10	35	ns
		090 Devices	–	10	45	ns
IDYN1RC	Operating current		–	0.1	–	mA
SU1RC	Startup time	050, 090, and 150 Devices	–	–	17	µs
		005, 010, and 025 Devices	–	–	18	µs

15. Clock Conditioning Circuits (CCC)

Table 135 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Parameter	Conditions	Minimum	Typical	Maximum	Units	Notes
Clock conditioning circuitry input frequency f_{IN_CCC}	All CCC	1	–	200	MHz	
	32 kHz capable CCC	0.032	–	200	MHz	
Clock conditioning circuitry output frequency f_{OUT_CCC}		0.078	–	400	MHz	1
PLL VCO frequency		500	–	1000	MHz	2
Delay increments in programmable delay blocks		–	75	100	ps	
Number of programmable values in each programmable delay block		–	–	64	–	
Acquisition time		–	70	100	µs	
Input duty cycle (Reference Clock)	Internal Feedback					
	1 MHz ≤ f_{IN_CCC} ≤ 25 MHz	10	–	90	%	
	25 MHz ≤ f_{IN_CCC}≤ 100 MHz	25	–	75	%	
	100 MHz ≤ f_{IN_CCC} ≤ 150 MHz	35	–	65	%	
	150 MHz ≤ f_{IN_CCC} ≤ 200 MHz	45	–	55	%	
	External Feedback (CCC, FPGA, Off-chip)					
	1 MHz ≤ f_{IN_CCC} ≤ 25 MHz	25	–	75	%	
	25 MHz ≤ f_{IN_CCC} ≤ 35 MHz	35	–	65	%	
	35 MHz ≤ f_{IN_CCC} ≤ 50 MHz	45	–	55	%	
Output duty cycle	050 Devices Fout ≤ 400 MHz	48	–	52	%	
	005, 010, and 025 Devices Fout < 350 MHz	48	–	52	%	
	005, 010, and 025 Devices 350 MHz ≤ Fout ≤ 400 MHz	46	–	54	%	
	090 Devices Fout ≤ 100 MHz	48	–	52	%	
	090 Devices 100 MHz ≤ Fout ≤ 400 MHz	44	–	52	%	
	150 Devices Fout ≤ 120 MHz	48	–	52	%	
	150 Devices 120 MHz ≤ Fout ≤ 400 MHz	45	–	52	%	
Spread Spectrum Characteristics						
Modulation frequency range		25	35	50	k	
Modulation depth range		0	–	1.5	%	

Table 135 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification (continued)**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Modulation depth control		–	0.5	–	%	

Note:

1. *The minimum output clock frequency is limited by the PLL. For more information, refer to the SmartFusion2 SoC FPGA Clocking Resources User Guide*
2. *The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance is limited by the CCC output frequency.*

Table 136 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

CCC Output Maximum Peak-to-Peak Period Jitter fOUT_CCC							
Parameter	**Conditions/Package Combinations**					**Units**	**Notes**
010, 050 FG896/FG484 Packages	SSO = 0	0 < SSO <= 2	SSO <= 4	SSO <= 8	SSO <= 16		*
20 MHz to 100 MHz	Max(110, ± 1% x (1/fOUT_CCC))	Max(150, ± 1% x (1/fOUT_CCC))				ps	
100 MHz to 400 MHz	Max(120, ± 1% x (1/fOUT_CCC))	Max(150, ± 1% x (1/fOUT_CCC))			Max(170, ± 1% x (1/fOUT_CCC))	ps	
025 FG484 Package	0 < SSO <=16						*
20 MHz to 74 MHz	± 1% x (1/fOUT_CCC))					ps	
74 MHz to 400 MHz	210					ps	
005 FG484 Package	0 < SSO <=16						*
20 MHz to 53 MHz	± 1% x (1/fOUT_CCC))					ps	
53 MHz to 400 MHz	270					ps	
090 FG676 and FC325 Package	0 < SSO <=16						*
20 MHz to 100 MHz	± 1% x (1/fOUT_CCC))					ps	
100 MHz to 400 MHz	150					ps	
150 FC1152 Package	0 < SSO <=16						*
20 MHz to 100 MHz	± 1% x (1/fOUT_CCC))					ps	
100 MHz to 400 MHz	120					ps	

*Note: *SSO Data is based on LVCMOS 2.5 V MSIO and/or MSIOD Bank I/Os*

16. JTAG

Table 137 • **JTAG 1532**

Parameter	Description	Speed Grade												Units
		–1	Std	–1	Std	–1	Std	–1	Std.	–1	Std	–1	Std	
		005		010		025		050		090		150		
tTCK2Q	Clock to Q (data out)	7.47	8.79	7.73	9.09	7.75	9.12	7.89	9.28	8.96	10.54	8.66	10.19	ns
tRSTB2Q	Reset to Q (data out)	7.65	9	6.43	7.56	6.13	7.21	7.40	8.70	7.75	9.12	8.79	10.34	ns
tDISU	Test Data Input Setup Time	-1.05	-0.89	-0.69	-0.59	-0.67	-0.57	-0.30	-0.25	-1.31	-1.11	-0.96	-0.82	ns
tDIHD	Test Data Input Hold Time	2.38	2.8	2.38	2.8	2.42	2.85	2.09	2.45	2.68	3.15	2.57	3.02	ns
tTMSSU	Test Mode Select Setup Time	-0.73	-0.62	-1.03	-1.21	-1.1	-0.94	0.28	0.33	-1.02	-0.87	-0.53	-0.45	ns
tTMDHD	Test Mode Select Hold Time	1.36	1.6	1.43	1.68	1.93	2.27	0.16	0.19	1.67	1.96	1.02	1.2	ns
tTRSTREM	ResetB Removal Time	-0.77	-0.65	-1.08	-0.92	-1.33	-1.13	-0.45	-0.38	-0.76	-0.65	-1.03	-0.88	ns
tTRSTREC	ResetB Recovery Time	-0.76	-0.65	-1.07	-0.91	-1.34	-1.14	-0.45	-0.38	-0.77	-0.65	-1.03	-0.88	ns
FTCKMAX	TCK Maximum frequency	25	21.25	25	21.25	25	21.25	25.00	21.25	25	21.25	25	21.25	MHz

17. DEVRST_N Characteristics

Table 138 • **DEVRST_N Characteristics**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Symbol	Description	All Devices/Speed Grades			Units	Notes
		Min	Typ	Max		
TRAMPDEVRSTN	DEVRST_N ramp rate	—	—	10	ns	*
Note: * Slower ramp rates are susceptible to board level noise.						

18. System Controller SPI Characteristics

Table 139 • **System Controller SPI Characteristics**
Worst-Case Industrial Conditions: TJ = 100°C, VDD = 1.14 V

Symbol	Description	Conditions	All Devices/Speed Grades			Units	Notes
			Min	Typ	Max		
sp1	SC_SPI_SCK minimum period		20	–	–	ns	
sp2	SC_SPI_SCK minimum pulse width high		10	–	–	ns	
sp3	SC_SPI_SCK minimum pulse width low		10	–	–	ns	
sp4	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%–90%) 1	IO Configuration: LVTTL 3.3 V-20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.239	–	ns	*
sp5	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%–90%) 1	IO Configuration: LVTTL 3.3 V-20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.245	–	ns	*
sp6	Data from master (SC_SPI_SDO) setup time		160	–	–	ns	
sp7	Data from master (SC_SPI_SDO) hold time		160	–	–	ns	
sp8	SC_SPI_SDI setup time		20	–	–	ns	
sp9	SC_SPI_SDI hold time		20	–	–	ns	

*Note: *For specific Rise/Fall Times , board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx. Use the supported I/O Configurations for the System Controller SPI in Table 140.*

Table 140 • **Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)**

Voltage Supply	I/O Drive Configuration	Units
3.3 V	20	mA
2.5 V	16	mA
1.8 V	12	mA
1.5 V	8	mA
1.2 V	4	mA

19. Mathblock Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC mathblock supports 18x18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently.

Table 141 • **Mathblocks with all Registers Used**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{MISU}	Input, control register setup time	0.149	–	0.176	–	ns
t_{MIHD}	Input, control register hold time	1.68	–	1.976	–	ns
$t_{MOCDINSU}$	CDIN input setup time	0.185	–	0.218	–	ns
$t_{MOCDINHD}$	CDIN input hold time	0.08	–	0.094	–	ns
$t_{MSRSTENSU}$	Synchronous reset/enable setup time	–0.419	–	–0.493	–	ns
$t_{MSRSTENHD}$	Synchronous reset/enable hold time	0.011	–	0.013	–	ns
$t_{MARSTREM}$	Asynchronous reset removal time	0	–	0	–	ns
$t_{MARSTREC}$	Asynchronous reset recovery time	0.088	–	0.104	–	ns
t_{MOCQ}	Output register clock to out delay	–	0.232	–	0.273	ns
t_{MCLKMP}	CLK minimum period	2.245	–	2.641	–	ns

Table 142 • **Mathblock with Input Bypassed and Output Registers Used**
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{MOSU}	Output register setup time	2.294	–	2.699	–	ns
t_{MOHD}	Output register hold time	1.68	–	1.976	–	ns
$t_{MOCDINSU}$	CDIN input setup time	0.115	–	0.136	–	ns
$t_{MOCDINHD}$	CDIN input hold time	–0.444	–	–0.522	–	ns
$t_{MSRSTENSU}$	Synchronous reset/enable setup time	–0.419	–	–0.493	–	ns
$t_{MSRSTENHD}$	Synchronous reset/enable hold time	0.011	–	0.013	–	ns
$t_{MARSTREM}$	Asynchronous reset removal time	0	–	0	–	ns
$t_{MARSTREC}$	Asynchronous reset recovery time	0.014	–	0.017	–	ns
t_{MOCQ}	Output register clock to out delay	–	0.232	–	0.273	ns
t_{MCLKMP}	CLK minimum period	2.179	–	2.563	–	ns

Table 143 • Mathblock with Input Register Used and Output in Bypass Mode
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{MISU}	Input register setup time	0.149	–	0.176	–	ns
t_{MIHD}	Input register hold time	0.185	–	0.218	–	ns
$t_{MSRSTENSU}$	Synchronous reset/enable setup time	0.08	–	0.094	–	ns
$t_{MSRSTENHD}$	Synchronous reset/enable hold time	–0.012	–	–0.014	–	ns
$t_{MARSTREM}$	Asynchronous reset removal time	–0.005	–	–0.005	–	ns
$t_{MARSTREC}$	Asynchronous reset recovery time	0.088	–	0.104	–	ns
t_{MICQ}	Input register clock to output delay	–	2.52	–	2.964	ns
$t_{MCDIN2Q}$	CDIN to output delay	–	1.951	–	2.295	ns

Table 144 • Mathblock with Input and Output in Bypass Mode
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Speed Grade				Units
		–1		Std		
		Min	Max	Min	Max	
t_{MIQ}	Input to output delay	–	2.568	–	3.022	ns
$t_{MCDIN2Q}$	CDIN to output delay	–	1.951	–	2.295	ns

20. Flash*Freeze Timing Characteristics

Table 145 • **Flash*Freeze Entry and Exit Times**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Symbols	Parameters	Conditions	005, 010, 025, 090, and 150	050	Units	Notes
TFF_ENTRY	Entry time	eNVM and MSS/HPMS PLL = ON	160	150	µs	1
		eNVM and MSS/HPMS PLL=OFF	215	200	µs	1
TFF_EXIT	Exit time with respect to the MSS PLL Lock	eNVM and MSS/HPMS PLL = ON during F*F	100	100	µs	1
		eNVM=ON and MSS/HPMS PLL =OFF during F*F and MSS/HPMS PLL turned back on at exit	136	120	µs	1
		eNVM and MSS/HPMS PLL=OFF during F*F and both are turned back on at exit	200	200	µs	1
		eNVM=OFF and MSS/HPMS PLL = ON during F*F and eNVM turned back on at exit	200	200	µs	1
	Exit time with respect to the Fabric PLL Lock	eNVM and MSS/HPMS PLL = ON during F*F	1.5	1.5	ms	1,2
		eNVM and MSS/HPMS PLL=OFF during F*F and both are turned back on at exit	1.5	1.5	ms	1,2
	Exit time with respect to the Fabric buffer output	eNVM and MSS/HPMS PLL = ON during F*F	21	15	µs	1
		eNVM and MSS/HPMS PLL=OFF during F*F and both are turned back on at exit	65	55	µs	1

Notes:

1. *F*F entry and exit times were measured with FCLK = 100MHz*
2. *PLL Lock Delay set to 1024 cycles (default)*

21. DDR Memory Interface Characteristics

Table 146 • **DDR Memory Interface Characteristics**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Standard	Supported Data Rate			Unit
	Min	Typ	Max	
DDR3	667			Mbps
DDR2	667			Mbps
LPDDR	50	—	400	Mbps

22. SFP Transceiver Characteristics

IGLOO2 and SmartFusion2 SERDES complies with small form-factor pluggable (SFP) requirements as specified in SFP INF-80741. Table 147 provides the electrical characteristics.

Table 147 • **SFP Transceiver Electrical Characteristics**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Pin	Direction	Differential Peak-Peak Voltage			Unit	Note
		Min	Typ	Max		
RD+/-	Output	1600	—	2400	mV	1
TD+/-	Input	350	—	2400	mV	2

Notes:

1. *Based on default SERDES transmitter settings for PCIe Gen1. Lower amplitudes are available through programming changes to TX_AMP setting.*
2. *Based on Input Voltage Common-Mode (VICM) = 0 V. Requires AC Coupling.*

23. PCIe Electrical and Timing AC and DC Characteristics

PCIe® is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block.

Table 148 • **Transmitter Parameters**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
VTX-DIFF-PP	Differential swing PCIe Gen1 and 2	0.8	–	1.2	V
VTX-CM-AC-P	Output common mode voltage PCIe Gen1	–	–	20	mV
VTX-CM-AC-PP	Output common mode voltage PCIe Gen2	–	–	100	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%) PCIe Gen1	0.125	–	–	UI
	Rise and fall time (20% to 80%) PCIe Gen2	0.15	–	–	UI
ZTX-DIFF-DC	Output impedance – differential	80	–	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SERDES block PCIe Gen1	–	–	500 ps+ 2 UI	ps
	Lane-to-lane TX skew within a SERDES block PCIe Gen2	–	–	500 ps+4 UI	ps
RLTX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
	Return loss differential mode PCIe Gen2 0.05 GHz to 1.25 GHz	–10	–	–	dB
	1.25 GHz to 2.5 GHz	–8	–	–	dB
RLTX-CM	Return loss common mode PCIe Gen1 and 2	–6	–	–	dB
TX-LOCK-RST	Transmit PLL lock time from reset	–	–	10	µs

Table 149 • **Receiver Parameters**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
VRX-DIFF-PP-CC	Input levels PCIe Gen1	0.175	–	1.2	V
	Input levels PCIe Gen2	0.12	–	1.2	V
VRX-CM-DC-P	Input common mode range (DC coupled) Note: PCIe standard mandates AC coupling	NA	NA	NA	–
VRX-CM-AC-P	Input common mode range (AC coupled)	–	–	150	mV
VRX-DIFF-PP-CC	Differential input sensitivity PCIe Gen1	0.175	–	–	mV
	Differential input sensitivity PCIe Gen2	0.12	–	–	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset	–	–	15	µs
RLRX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
	Return loss differential mode PCIe Gen2 0.05 GHz to 1.25 GHz	–10	–	–	dB
	1.25 GHz to 2.5 GHz	–8	–	–	dB
RLRX-CM	Return loss common mode PCIe Gen1 and 2	–6	–	–	dB

Table 149 • **Receiver Parameters (continued)**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

	CID limit (set by 8B/10B coding, not the receiver PLL)	–	–	4	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65	–	175	mV

Table 150 • **SERDES Reference Clock AC Specifications**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Symbols	Description	Min	Typ	Max	Units
FREFCLK	Reference Clock Frequency	100	–	160	MHz
TRISE	Reference Clock Rise Time	0.6	–	4	V/ns
TFALL	Reference Clock Fall Time	0.6	–	4	V/ns
TCYC	Reference Clock Duty Cycle	40	–	60	%
Mmrefclk	Reference Clock Mismatch	–300	–	300	ppm
SSCref	Reference Spread Spectrum Clock	0	–	5000	ppm

Table 151 • **HCSL Minimum and Maximum DC Input Levels (Applicable to SERDES REFCLK Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply Voltage		2.375	2.5	2.625	V
HCSL DC Input Voltage Specification						
VI	DC Input voltage		0	–	2.625	V
HCSL Differential Voltage Specification						
VICM	Input common mode voltage		0.05	–	2.4	V
VIDIFF	Input differential voltage		100	–	1100	mV

Table 152 • **HCSL Minimum and Maximum AC Switching Speeds (Applicable to SERDES REFCLK Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
HCSL AC Specifications						
Fmax	Maximum Data Rate (for MSIO IO Bank)		–	–	350	Mbps
HCSL Impedance Specifications						
Rt	Termination Resistance		–	100	–	Ω

24. SmartFusion2 Specifications

24.1 MSS Clock Frequency

Table 153 • **Maximum Frequency for MSS Main Clock**
Worst-Case Industrial Conditions: T_J= 100°C, VDD = 1.14 V

Symbol	Description	Speed Grade		Units
		–1	Std	
M3_CLK	Maximum frequency for the MSS Main Clock	166	142	MHz

24.2 SmartFusion2 Inter-Integrated Circuit (I^2C) Characteristics

This section describes the DC and switching of the I^2C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 16 on page 125.

Table 154 • **I2C Characteristics**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Parameter	Definition	Conditions	Min	Typ	Max	Units	Notes
VIL	Input low voltage	Refer to the "Single-Ended I/O Standards" section on page 29 for more information. I/O standard used for illustration: MSIO bank – LVTTL 8 mA low drive.	–0.3	–	0.8	V	
VIH	Input high voltage	Refer to the "Single-Ended I/O Standards" section on page 29 for more information. I/O standard used for illustration: MSIO bank – LVTTL 8 mA low drive.	2	–	3.45	V	
VHYS	Hysteresis of Schmitt triggered inputs for VDDI > 2 V	Refer to Table 22 on page 29 for more information.	0.05 × VDDI	–	–	V	
IIL	Input current high	Refer to the "Single-Ended I/O Standards" section on page 29 for more information.	–	–	10	µA	
IIH	Input current low	Refer to the "Single-Ended I/O Standards" section on page 29 for more information.	–	–	10	µA	
Tir	Input rise time	Standard Mode	–	–	1000	ns	
		Fast Mode	–	–	300	ns	
Tif	Input fall time	Standard Mode	–	–	300	ns	
		Fast Mode	–	–	300	ns	
VOL	Maximum output voltage low (open drain) at 3 mA sink current for VDDI > 2 V	Refer to the "Single-Ended I/O Standards" section on page 29 for more information. I/O standard used for illustration: MSIO bank – LVTTL 8 mA low drive.	–	–	0.4	V	
Cin	Pin capacitance	VIN = 0, f = 1.0 MHz	–	–	10	pF	
t_{OF}	Output fall time from VIHMin to VILMax	VIHmin to VILMax, Cload = 400 pF	–	21.04	–	ns	1
		VIHmin to VILMax, Cload = 100 pF	–	5.556	–	ns	

Table 154 • I2C Characteristics (continued)
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Parameter	Definition	Conditions	Min	Typ	Max	Units	Notes
t_{OR}	Output rise time from VILMax to VIHMin	VILMax to VIHmin, Cload = 400pF	–	19.887	–	ns	1
		VILMax to VIHmin, Cload = 100pF	–	5.218	–	ns	
Rpull-up	Output buffer maximum pull-down resistance		–	–	50	Ω	2, 3
Rpull-down	Output buffer maximum pull-up resistance		–	–	131.25	Ω	2, 4
Dmax	Maximum data rate	Fast mode	–	–	400	Kbps	
		Standard mode	–	–	100	Kbps	
t_{FILT}	Pulse width of spikes which must be suppressed by the input filter	Fast mode	–	50	–	ns	

Notes:

1. *These values are provided for MSIO Bank – LVTTL 8 mA Low Drive at 25°C, typical conditions. For Board Design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VDDIx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
3. *R(PULL-DOWN-MAX) = (VOLspec) / IOLspec*
4. *R(PULL-UP-MAX) = (VDDImax – VOHspec) / IOHspec*

Table 155 • I2C Switching Characteristics
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Parameter	Definition	Conditions	Speed Grade				Units
			–1		Std		
			Min	Max	Min	Max	
t_{LOW}	Low period of I2C_x_SCL	–	1	–	1	–	pclk cycles
t_{HIGH}	High period of I2C_x_SCL	–	1	–	1	–	pclk cycles
$t_{HD;STA}$	START hold time	–	1	–	1	–	pclk cycles
$t_{SU;STA}$	START setup time	–	1	–	1	–	pclk cycles
$t_{HD;DAT}$	DATA hold time	–	1	–	1	–	pclk cycles
$t_{SU;DAT}$	DATA setup time	–	1	–	1	–	pclk cycles
$t_{SU;STO}$	STOP setup time	–	1	–	1	–	pclk cycles

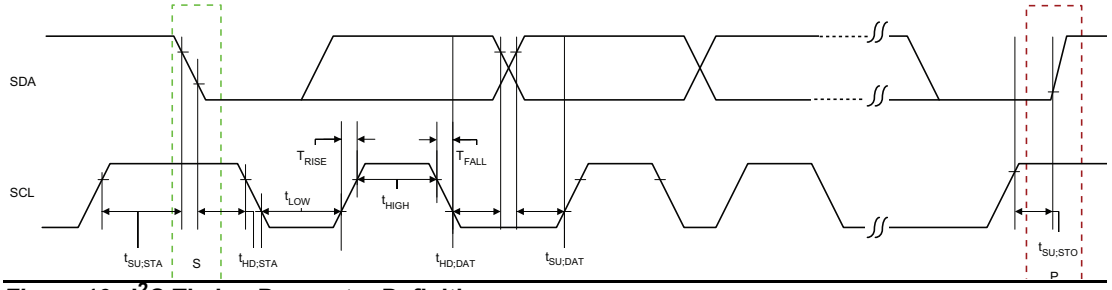

Figure 16 • **I^2C Timing Parameter Definition**

24.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 17 on page 127.

Table 156 • **SPI Characteristics**

Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp1	SPI_[0|1]_CLK minimum period						
	SPI_[0|1]_CLK = PCLK/2		12	–	–	ns	
	SPI_[0|1]_CLK = PCLK/4		24.1	–	–	ns	
	SPI_[0|1]_CLK = PCLK/8		48.2	–	–	ns	
	SPI_[0|1]_CLK = PCLK/16		0.1	–	–	µs	
	SPI_[0|1]_CLK = PCLK/32		0.19	–	–	µs	
	SPI_[0|1]_CLK = PCLK/64		0.39	–	–	µs	
	SPI_[0|1]_CLK = PCLK/128		0.77	–	–	µs	
sp2	SPI_[0|1]_CLK minimum pulse width high						
	SPI_[0|1]_CLK = PCLK/2		6	–	–	ns	
	SPI_[0|1]_CLK = PCLK/4		12.05	–	–	ns	
	SPI_[0|1]_CLK = PCLK/8		24.1	–	–	ns	
	SPI_[0|1]_CLK = PCLK/16		0.05	–	–	µs	
	SPI_[0|1]_CLK = PCLK/32		0.095	–	–	µs	
	SPI_[0|1]_CLK = PCLK/64		0.195	–	–	µs	
	SPI_[0|1]_CLK = PCLK/128		0.385	–	–	µs	

Table 156 • **SPI Characteristics (continued)**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp3	SPI_[0|1]_CLK minimum pulse width low						
	SPI_[0|1]_CLK = PCLK/2		6	–	–	ns	
	SPI_[0|1]_CLK = PCLK/4		12.05	–	–	ns	
	SPI_[0|1]_CLK = PCLK/8		24.1	–	–	ns	
	SPI_[0|1]_CLK = PCLK/16		0.05	–	–	µs	
	SPI_[0|1]_CLK = PCLK/32		0.095	–	–	µs	
	SPI_[0|1]_CLK = PCLK/64		0.195	–	–	µs	
	SPI_[0|1]_CLK = PCLK/128		0.385	–	–	µs	
sp4	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS rise time (10%–90%)	IO Configuration: LVCMOS 2.5 V-8mA AC Loading: 35pF Test Conditions: Typical Voltage, 25°C	–	2.77	–	ns	1
sp5	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS fall time (10%–90%)	IO Configuration: LVCMOS 2.5 V-8mA AC Loading: 35pF Test Conditions: Typical Voltage, 25°C	–	2.906	–	ns	1
SPI Master Configuration							
sp6m	SPI_[0|1]_DO setup time		(SPI_x_CLK_period/2) – 3.0	–	–	ns	2
sp7m	SPI_[0|1]_DO hold time		(SPI_x_CLK_period/2) – 2.5	–	–	ns	2
sp8m	SPI_[0|1]_DI setup time		8	–	–	ns	2
sp9m	SPI_[0|1]_DI hold time		2.5	–	–	ns	2
SPI Slave Configuration							
sp6s	SPI_[0|1]_DO setup time		(SPI_x_CLK_period/2) – 12.0	–	–	ns	2
sp7s	SPI_[0|1]_DO hold time		(SPI_x_CLK_period/2) + 3.0	–	–	ns	2
sp8s	SPI_[0|1]_DI setup time		2	–	–	ns	2
sp9s	SPI_[0|1]_DI hold time		3	–	–	ns	2

Notes:

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion2 ARM Cortex-M3 and Microcontroller Subsystem User's Guide.*

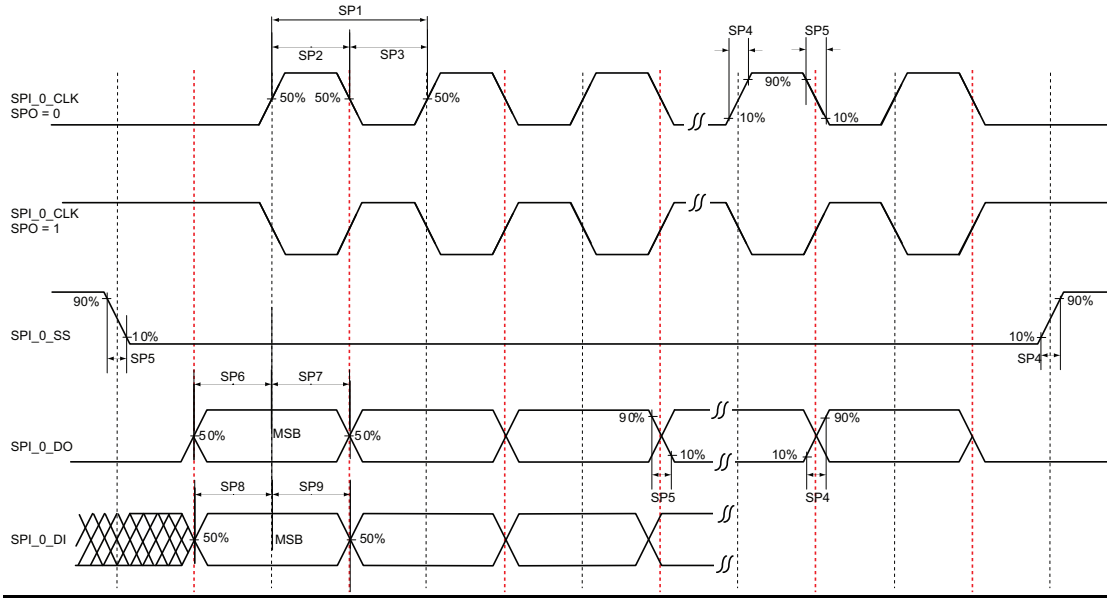

***Figure 17* • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**

25. CAN Controller Characteristics

Table 157 • **CAN Controller Characteristics**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Parameter	Description	Speed Grade		Units	Notes
		–1	Std		
FCANREFCLK	Internally Sourced CAN Reference Clock Frequency	160	136	MHz	*
BAUDCANMAX	Maximum CAN Performance Baud Rate	1	1	Mbps	
BAUDCANMIN	Minimum CAN Performance Baud Rate	0.05	0.05	Mbps	
Note: PCLK to CAN controller must be a multiple of 8 MHz.					

26. USB Characteristics

Table 158 • **USB Characteristics**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Parameter	Description	Speed Grade		Units
		–1	Std	
FUSBREFCLK	Internally Sourced USB Reference Clock Frequency	166	142	MHz
TUSBCLK	USB Clock Period	16.66	16.66	ns
TUSBPD	Clock to USB Data Propagation Delay	9.0	9.0	ns
TUSBSU	Setup Time for USB Data	6.0	6.0	ns
TUSBHD	Hold Time for USB Data	0	0	ns

27. IGLOO2 Specifications

27.1 HPMS Clock Frequency

Table 159 • **Maximum Frequency for HPMS Main Clock**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Symbol	Description	Speed Grade		Units
		–1	Std	
HPMS_CLK	Maximum Frequency for the HPMS Main Clock	166	142	MHz

27.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, refer to Figure 18 on page 132.

Table 160 • **SPI Characteristics**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp1	SPI_[0|1]_CLK minimum period						
	SPI_[0|1]_CLK = PCLK/2		12	–	–	ns	
	SPI_[0|1]_CLK = PCLK/4		24.1	–	–	ns	
	SPI_[0|1]_CLK = PCLK/8		48.2	–	–	ns	
	SPI_[0|1]_CLK = PCLK/16		0.1	–	–	µs	
	SPI_[0|1]_CLK = PCLK/32		0.19	–	–	µs	
	SPI_[0|1]_CLK = PCLK/64		0.39	–	–	µs	
	SPI_[0|1]_CLK = PCLK/128		0.77	–	–	µs	
sp2	SPI_[0|1]_CLK minimum pulse width high						
	SPI_[0|1]_CLK = PCLK/2		6	–	–	ns	
	SPI_[0|1]_CLK = PCLK/4		12.05	–	–	ns	
	SPI_[0|1]_CLK = PCLK/8		24.1	–	–	ns	
	SPI_[0|1]_CLK = PCLK/16		0.05	–	–	µs	
	SPI_[0|1]_CLK = PCLK/32		0.095	–	–	µs	
	SPI_[0|1]_CLK = PCLK/64		0.195	–	–	µs	
	SPI_[0|1]_CLK = PCLK/128		0.385	–	–	µs	

Notes:

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion2 ARM Cortex-M3 and Microcontroller Subsystem User's Guide.*

Table 160 • **SPI Characteristics (continued)**
Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp3	SPI_[0|1]_CLK minimum pulse width low						
	SPI_[0|1]_CLK = PCLK/2		6	–	–	ns	
	SPI_[0|1]_CLK = PCLK/4		12.05	–	–	ns	
	SPI_[0|1]_CLK = PCLK/8		24.1	–	–	ns	
	SPI_[0|1]_CLK = PCLK/16		0.05	–	–	µs	
	SPI_[0|1]_CLK = PCLK/32		0.095	–	–	µs	
	SPI_[0|1]_CLK = PCLK/64		0.195	–	–	µs	
	SPI_[0|1]_CLK = PCLK/128		0.385	–	–	µs	
sp4	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS rise time (10%–90%)	IO Configuration: LVCMOS 2.5 V-8mA AC Loading: 35pF Test Conditions: Typical Voltage, 25°C	–	2.77	–	ns	1
sp5	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS fall time (10%–90%)	IO Configuration: LVCMOS 2.5 V-8mA AC Loading: 35pF Test Conditions: Typical Voltage, 25°C	–	2.906	–	ns	1
SPI Master Configuration							
sp6m	SPI_[0|1]_DO setup time		(SPI_x_CLK_period/2) – 3.0	–	–	ns	2
sp7m	SPI_[0|1]_DO hold time		(SPI_x_CLK_period/2) – 2.5	–	–	ns	2
sp8m	SPI_[0|1]_DI setup time		8	–	–	ns	2
sp9m	SPI_[0|1]_DI hold time		2.5	–	–	ns	2
SPI Slave Configuration							
sp6s	SPI_[0|1]_DO setup time		(SPI_x_CLK_period/2) – 12.0	–	–	ns	2
sp7s	SPI_[0|1]_DO hold time		(SPI_x_CLK_period/2) + 3.0	–	–	ns	2
sp8s	SPI_[0|1]_DI setup time		2	–	–	ns	2
sp9s	SPI_[0|1]_DI hold time		3	–	–	ns	2

Notes:

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion2 ARM Cortex-M3 and Microcontroller Subsystem User's Guide.*

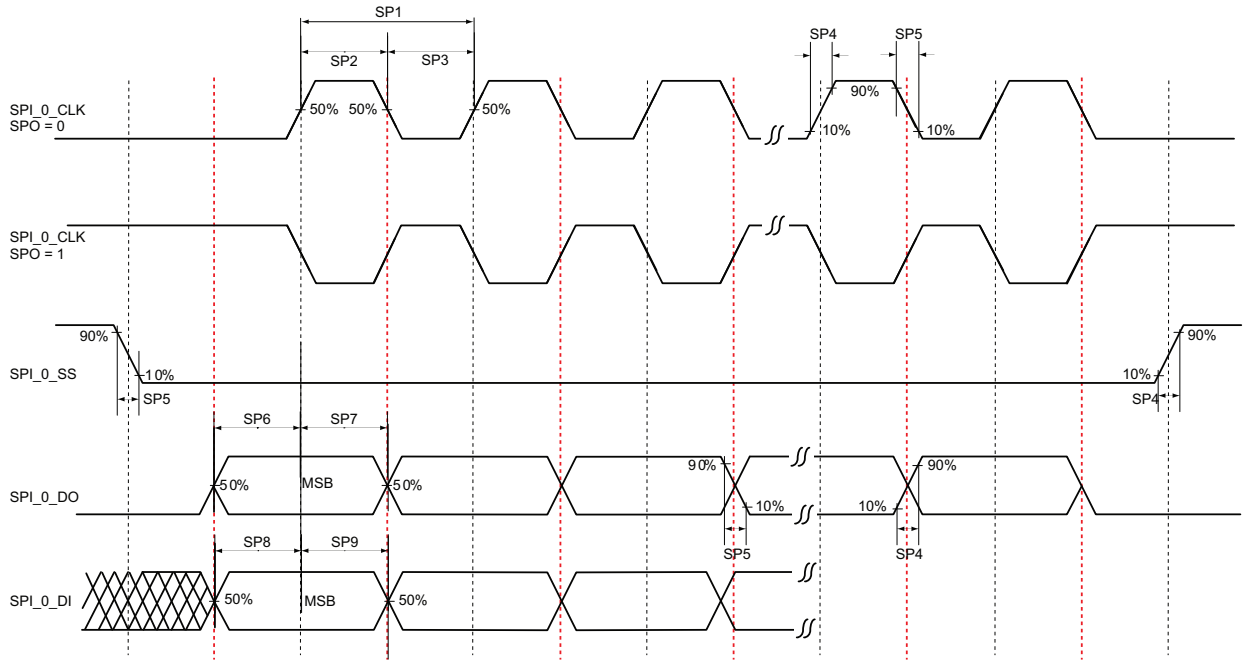

Figure 18 • **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**

Datasheet Information

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 7 (June 2015)	Updated Table 1: "IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status" (SAR 68620).	11
Revision 6 (May 2015)	Updated Table 4: "FPGA Operating Limits" (SAR 65949).	14
	Updated Table 7: "Package Thermal Resistance" (SAR 62995).	16
	Updated Table 61: "SSTL18 AC Specifications (Applicable to DDRIO Bank Only)" and Table 65: "SSTL15 AC Specifications (for DDRIO I/O Bank Only)" (SAR 67210).	54, 57
	Added "Embedded NVM (eNVM) Characteristics" (SAR 52509).	106
	Updated Table 130: "Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)" (SAR 64855).	107
	Updated Table 135: "IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification" (SAR 65958 and SAR 56666).	110
	Added "DDR Memory Interface Characteristics" (SAR 66223).	119
	Added "SFP Transceiver Characteristics" (SAR 63105).	120
	Updated Table 153: "Maximum Frequency for MSS Main Clock" and Table 159: "Maximum Frequency for HPMS Main Clock" (SAR 66314).	123, 130
Revision 5 (March 2015)	Updated Table 1: "IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status"	11
	Updated Table 3: "Recommended Operating Conditions" for T_J symbol information.	13
	Updated Table 4: "FPGA Operating Limits" (SAR 63109).	14
	Updated Table 7: "Package Thermal Resistance"	16
	Updated Table 135: "IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification" (SAR 62012).	110
	Added Table 138: "DEVRST_N Characteristics" (SAR 64100).	114
	Added Table 157: "CAN Controller Characteristics", Table 158: "USB Characteristics" (SAR 50424).	128, 129
Revision 4 (November 2014)	Updated Table 1. Changed the Status of 090 devices to "Production" (SAR 62750).	11
	Updated Figure 9. Removed inverter bubble from DDR_IN latch (SAR 61418).	81
	Updated "PCIe Electrical and Timing AC and DC Characteristics" (SAR 62836).	121
Revision 3 (October 2014)	Updated Theta B/C columns and FCS325 package in Table 7 (SAR 62002).	16

Revision	Changes	Page
Revision 2 (October 2014)	"IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status" table was updated (SAR 59056).	11
	Table 6 temperature and data retention information was updated SAR (61363).	15
	Storage Operating Table was updated and split into three tables – Table 4-Table 6 (SAR 58725).	15–19
	Updated Theta B/C columns and FCS325 package in Table 7 (SAR 62002).	16
	Added 090-FCS325 thermal resistance to Table 7 (SAR 59384).	16
	TQ144 package was added to Table 7 (SAR 57708).	16
	Added PLL jitter data for the VF400 package (SAR 53162).	16
	Added Additional Worst Case IDD to Table 9 and Table 10 (SAR 59077).	18
	Table 11, Table 12, and Table 13 were added to verify Inrush currents (SAR 56348).	19
	Table 16 and Table 17 – I/O speeds were replaced.	26, 26
	Max speed was changed in Table 29 (SAR 57221) and in Table 34 (SAR 57113).	34, 36
	"Minimum and Maximum DC/AC Input and Output Levels Specification" and Table 33–Table 37 were added.	36–38
	Added Cload to Table 49 (SAR 56238).	46
	Removed "Rs" information in DDR Timing Measurement Table 61, Table 65, and Table 69.	54, 57, 59
	Updated drive programming for M/B-LVDS outputs (SAR 58154).	69
	Added an inverter bubble to DDR_IN latch in Figure 9 (SAR 61418).	81
	QF waveform in the Input DDR Timing Diagram was updated (SAR 59816).	82
	uSRAM Write Clock minimum values were updated in Table 121–Table 127 (SAR 55236).	97–104
	Fixed typo in the 32 kHz Crystal (XTAL) oscillator accuracy data section (SAR 59669).	108
	The "On-Chip Oscillator" section was split, and the "Embedded NVM (eNVM) Characteristics" section was added. Table 130–Table 134 were revised.(SARs 57898 and 59669).	109
	PLL VCP Frequency and conditions were added to Table 135 (SAR 57416).	110
	Fixed typo for PLL jitter data in the 100-400 MHz range (SAR 60727).	110
	Updated FCCC information in Table 135 and Table 136 (SAR 60799).	110
	Device 025 specifications were added to Table 136 (SAR 51625).	112
	JTAG Table 137 was replaced (SAR 51188).	113
	Flash*Freeze Table 145 was replaced (SAR 57828).	118
	Added support for HCSL I/O Standard for SERDES reference clocks in Table 151 and Table 152 (SAR 50748).	122
	Tir and Tif parameters were added to Table 154 (SAR 52203).	123
	Speed grade consistency was fixed in tables throughout the datasheet (SAR 50722).	NA
	Added jitter attenuation information (SAR 59405).	NA
Revision 1 (May 2014)	The IGLOO2 v2 and the SmartFusion2 v5 datasheets are combined into this single product family datasheet.	N/A

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in Table 1 on page 11 is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

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The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

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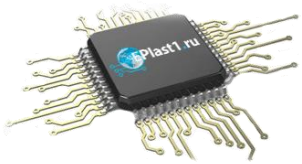

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