



PESD24VL1BA

Low capacitance bidirectional ESD protection diode in SOD323

12 July 2018

Product data sheet

1. General description

Bidirectional ElectroStatic Discharge (ESD) protection diode in a very small SOD323 (SC-76) SMD plastic package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of one line
- Max. peak pulse power: $P_{PPM} = 200 \text{ W}$
- Low clamping voltage: $V_{(CL)R} = 70 \text{ V}$
- Ultra low leakage current: $I_{RM} < 1 \text{ nA}$
- ESD protection $> 23 \text{ kV}$
- IEC 61000-4-2, level 4 (ESD)
- IEC 61000-4-5 (surge); $I_{PPM} = 3 \text{ A}$
- Very small SMD plastic package

3. Applications

- Computers and peripherals
- Communication systems
- Audio and video equipment
- Data lines
- CAN bus protection


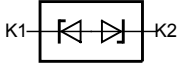
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25 \text{ }^{\circ}\text{C}$	-	-	24	V
C_d	diode capacitance	$f = 1 \text{ MHz}; V_R = 0 \text{ V}; T_{amb} = 25 \text{ }^{\circ}\text{C}$	-	11	-	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode 1	 SOD323	 sym045
2	K2	cathode 2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD24VL1BA	SOD323	plastic, surface-mounted package; 2 leads; 1.3 mm pitch; 1.7 mm x 1.25 mm x 0.95 mm body	SOD323

7. Marking

Table 4. Marking codes

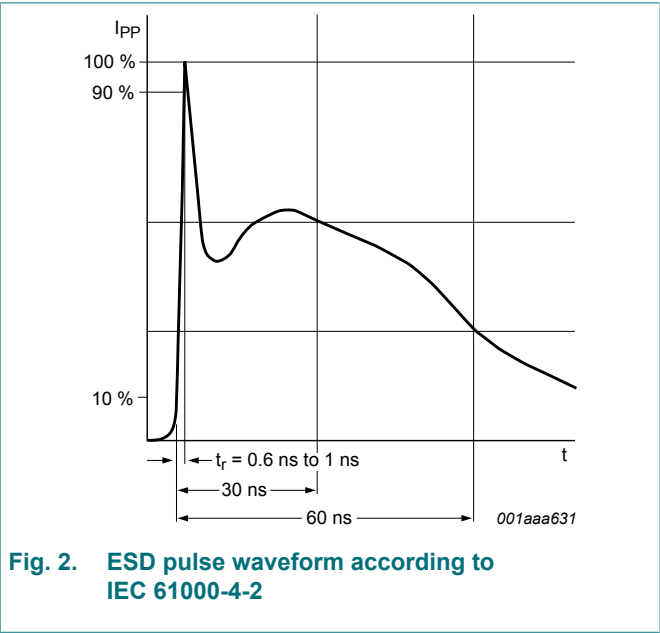
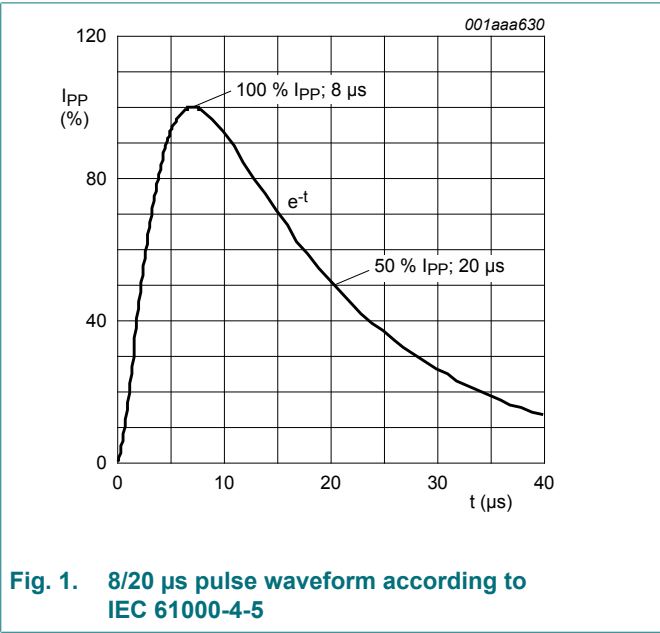
Type number	Marking code
PESD24VL1BA	AF

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P _{PPM}	rated peak pulse power	t _p = 8/20 μs	[1]	-	200	W
I _{PPM}	rated peak pulse current		[1]	-	3	A
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2]	-	23	kV
		HBM (MIL-STD 883)	[2]	-	10	kV

- [1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC61000-4-5.
[2] Device stressed with ten non-repetitive ESD pulses.

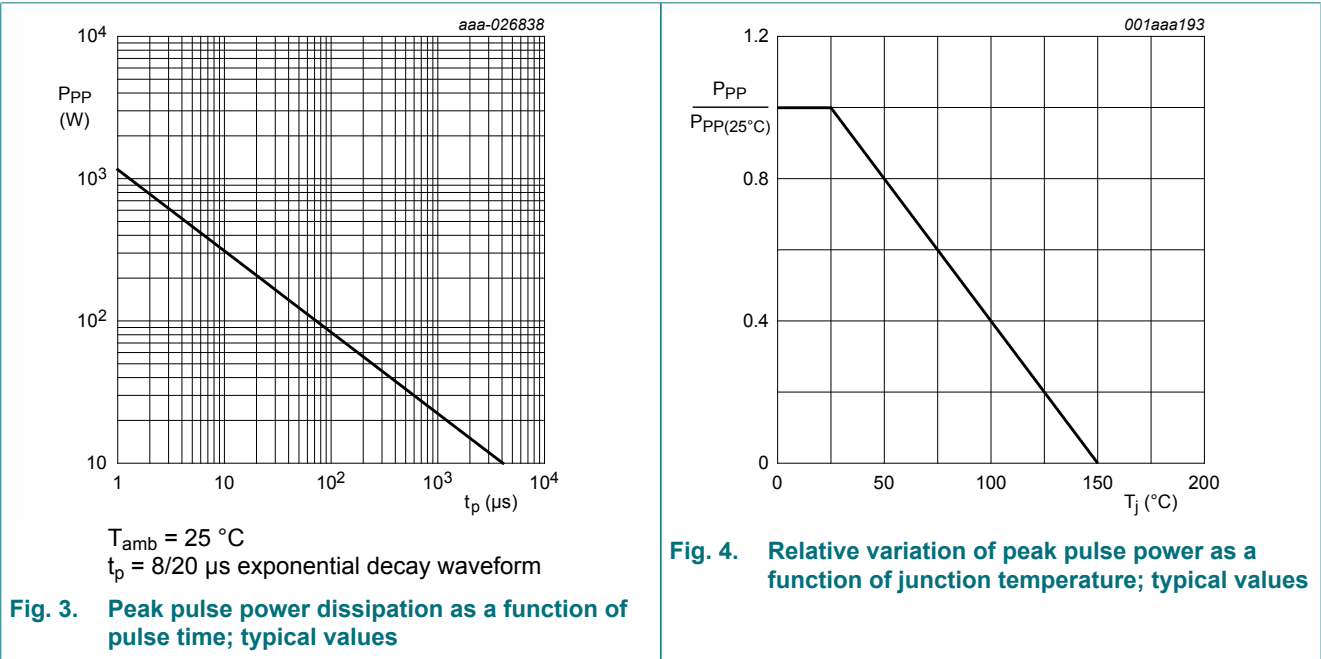


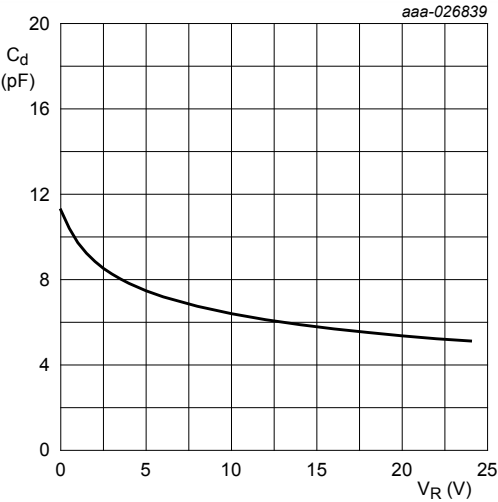
9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	24	V
V _{BR}	breakdown voltage	I _R = 5 mA; T _{amb} = 25 °C		25.4	27.8	30.3	V
I _{RM}	reverse leakage current	V _{RWM} = 24 V; T _{amb} = 25 °C		-	1	50	nA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	11	-	pF
V _{CL}	clamping voltage	I _{PP} = 1 A; T _{amb} = 25 °C	[1]	-	-	40	V
		I _{PP} = 3 A; T _{amb} = 25 °C	[1]	-	-	70	V
r _{dif}	differential resistance	I _R = 1 mA; T _{amb} = 25 °C		-	-	300	Ω

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC61000-4-5.





$T_{amb} = 25\text{ °C}; f = 1\text{ MHz}$

Fig. 5. Diode capacitance as a function of reverse voltage; typical values

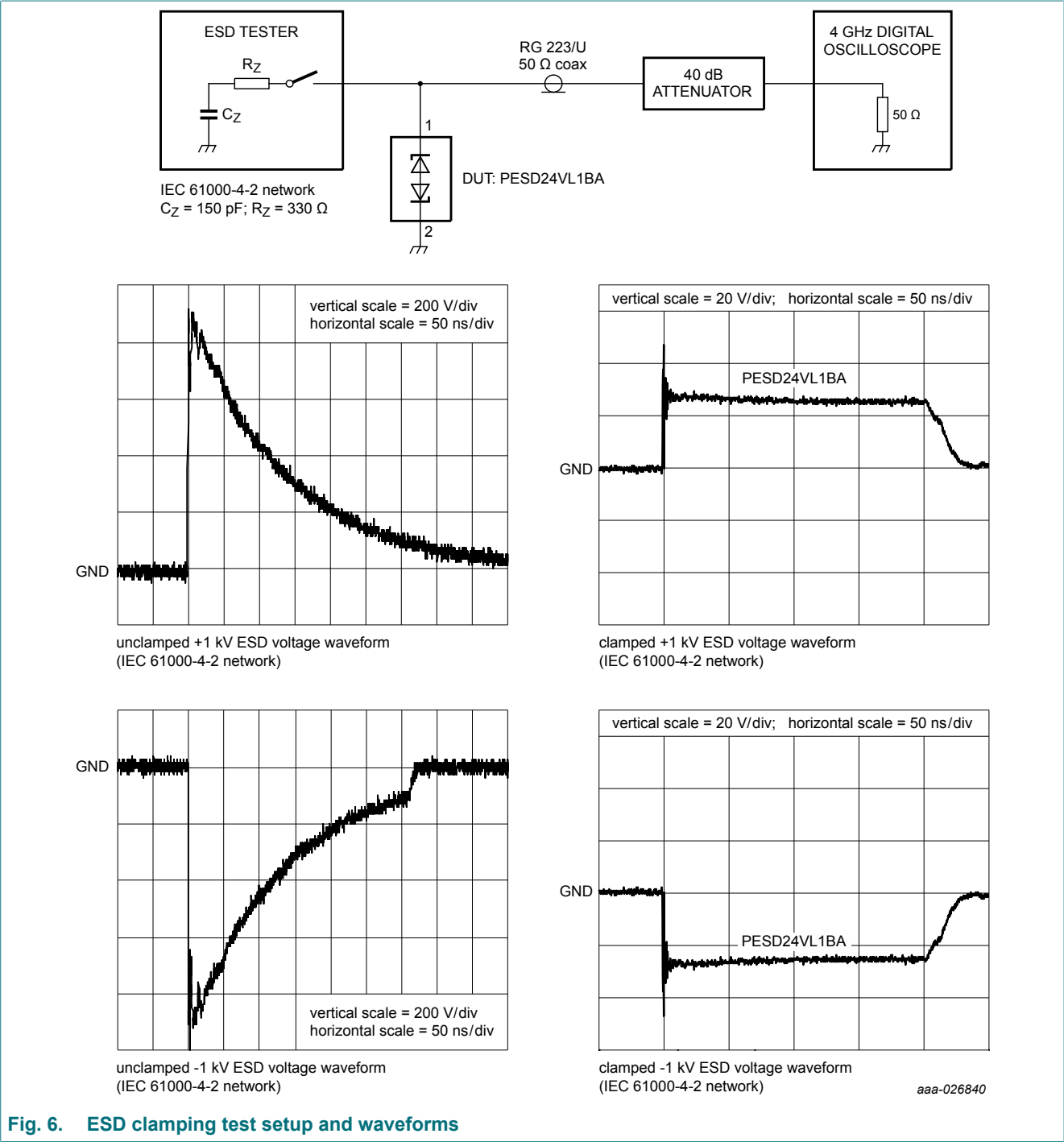


Fig. 6. ESD clamping test setup and waveforms

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground. The device is not designed to be used on lines connected to a DC supply.

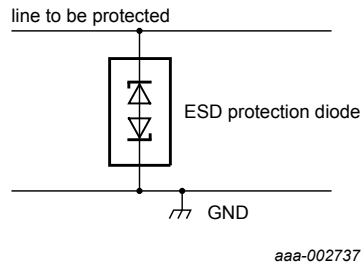


Fig. 7. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

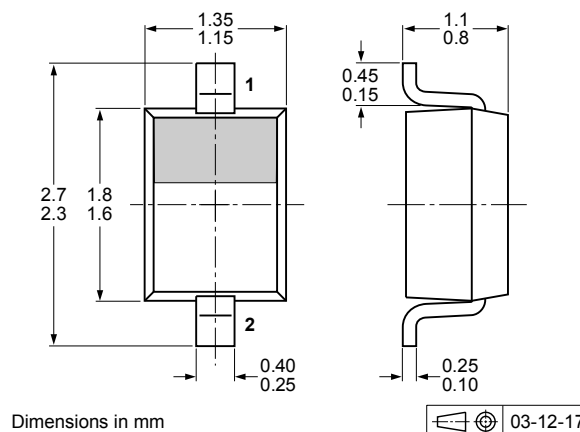
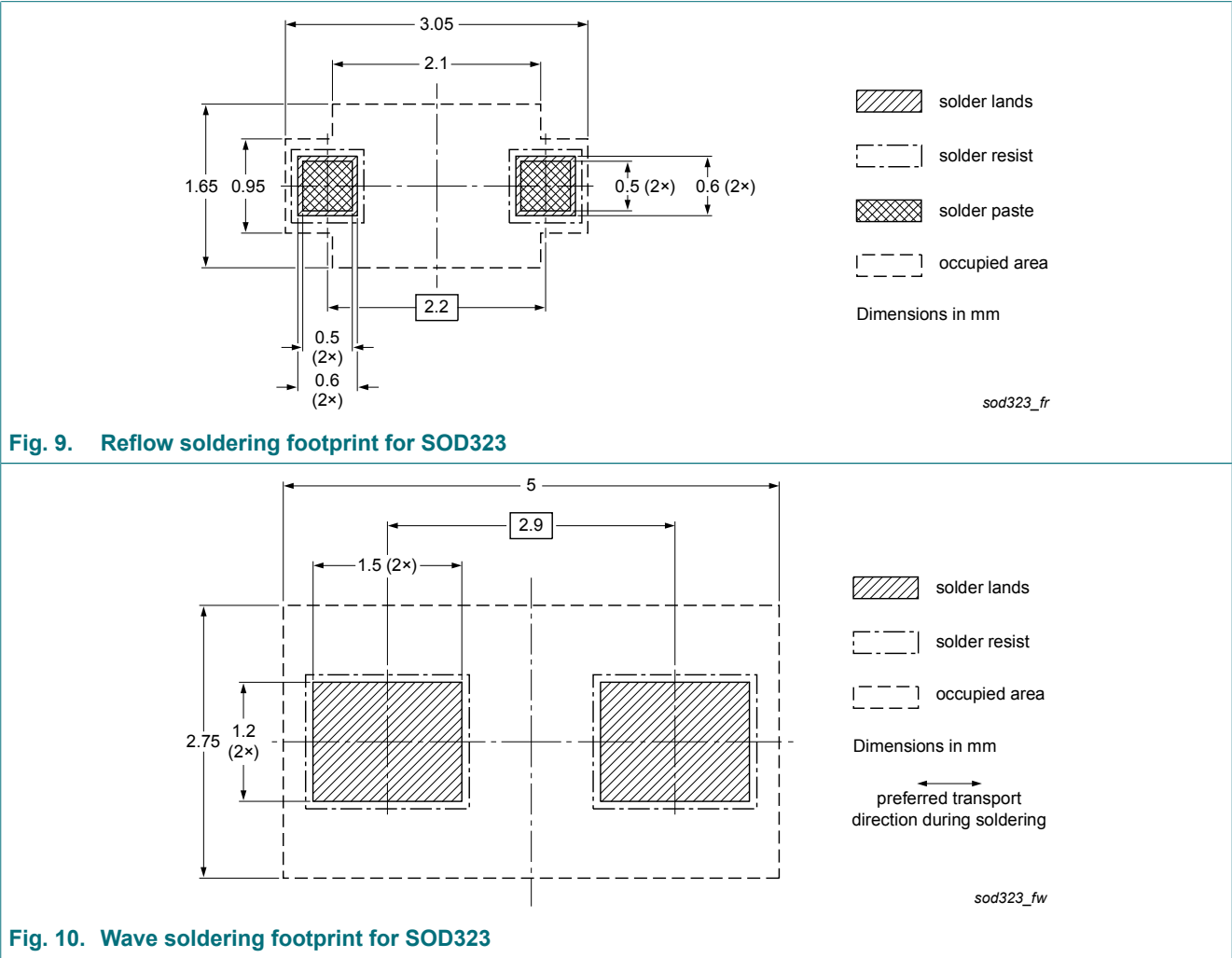


Fig. 8. Package outline SOD323

12. Soldering



13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD24VL1BA v.2	20180711	Product data sheet	-	PESD24VL1BA v.1
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.• Legal texts have been adapted to the new company name where appropriate.• Limiting values: minimum ambient temperature corrected• Characteristics: Figure 6 corrected			
PESD24VL1BA v.1	20170724	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 12 July 2018



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