SCBS160C - DECEMBER 1992 - REVISED MAY 1997

GND

2D7

2D8

2LE

28

27

26

25

 Members of the Texas Instruments Widebus™ Family State of the Art EBIC UBIM BiCMOS Design 	SN54ABT16373A WD PACKAGE SN74ABT16373A DGG OR DL PACKAGE (TOP VIEW)					
 State-of-the-Art EPIC-IIB[™] BiCMOS Design Significantly Reduces Power Dissipation 	10E		1LE			
 Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17 	1Q1 [1Q2 [2 47] 1D1] 1D2			
• Typical V _{OLP} (Output Ground Bounce)	GND [1Q3 [4 45	GND 1D3			
< 0.8 V at V _{CC} = 5 V, T _A = 25°C • High-Impedance State During Power Up and Power Down	1Q4 [V _{CC} [6 43	1D4 V _{CC}			
 Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise 	1Q5 [1Q6 [8 41 9 40] 1D5] 1D6			
 Flow-Through Architecture Optimizes PCB Layout 	GND [1Q7 [1Q8 [11 38	GND 1D7 1D8			
 High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL}) 	2Q1 [13 36] 2D1			
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink 	2Q2 [GND [15 34] 2D2] GND			
Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package	2Q3 [2Q4 [2D3 2D4			
Using 25-mil Center-to-Center Spacings	V _{CC} [2Q5 [] V _{CC}] 2D5			
description	2Q6 [2D6			

The 'ABT16373A are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

GND

2Q7 🛛

2Q8

20E

21

22

23

24

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16373A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16373A is characterized for operation from –40°C to 85°C.



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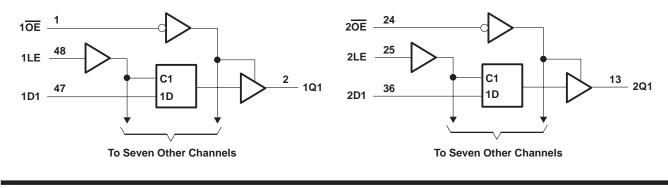
FUNCTION TABLE (each 8-bit section) INPUTS OUTPUT Q OE LE D L Н Н Н L н L L L Х L Q_0 Н Х Х Ζ

logic symbol[†]

			_	
1 <mark>0E</mark>	1	1EN		
1LE	48	C3		
20E	24	2EN		
	25			
2LE		C4		
1D1	47	3D 1 ▽	2	1Q1
1D2	46		3	1Q2
1D3	44	-	5	1Q3
1D4	43		6	1Q4
1D5	41	-	8	1Q5
1D6	40	-	9	1Q6
1D7	38	-	11	1Q7
1D8	37	-	12	1Q8
2D1	36	4D 2 ⊽	13	2Q1
2D2	35		14	2Q2
2D3	33		16	2Q3
2D4	32		17	2Q4
2D5	30		19	2Q5
2D6	29		20	2Q6
2D7	27		22	2Q7
2D8	26		23	2Q8
			J	

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} Input voltage range applied to any output in the high or power-off state, V_O Current into any output in the low state, I_O : SN54ABT16373A SN74ABT16373A Input clamp current, I_{IK} ($V_I < 0$) Output clamp current, I_{OK} ($V_O < 0$) Package thermal impedance, θ_{JA} (see Note 2): DGG package DL package	-0.5 V to 7 V -0.5 V to 5.5 V
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABT	16373A	SN74ABT1	16373A	UNIT
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		V	
VIL	Low-level input voltage		0.8		0.8	V	
VI	Input voltage	0	VCC	0	VCC	V	
ЮН	High-level output current			-24		-32	mA
IOL	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST OO	NDITIONS	Т	A = 25°0	;	SN54ABT	16373A	SN74ABT1	16373A	UNIT	
r	ARAMETER	TESTCO	NDITIONS	MIN	TYP [†]	MAX	MIN	MAX	MIN	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	lj = -18 mA			-1.2		-1.2		-1.2	V	
		V _{CC} = 4.5 V,	I _{OH} = -3 mA	2.5			2.5		2.5			
∨он		V _{CC} = 5 V,	I _{OH} = -3 mA	3			3		3		V	
VOH		V _{CC} = 4.5 V	I _{OH} = -24 mA	2			2				V	
	V.U -		$I_{OH} = -32 \text{ mA}$	2*					2			
VOL		V _{CC} = 4.5 V	I _{OL} = 48 mA			0.55		0.55			V	
VOL		VCC = 4.3 V	I _{OL} = 64 mA			0.55*				0.55	v	
V _{hys}					100						mV	
II.		$V_{CC} = 0$ to 5.5 V V _I = V _{CC} or GN				±1		±1		±1	μΑ	
IOZPU	‡ر	$V_{CC} = 0 \text{ to } 2.1 \text{ V}$ $V_{O} = 0.5 \text{ V to } 2.1 \text{ V}$	V, 7 V, OE = X			±50		±50		±50	μA	
IOZPE) [‡]	$V_{CC} = 2.1 V to$ $V_{O} = 0.5 V to 2.000 V_{O}$	0, 7 V, OE = X			±50		±50		±50	μA	
IOZH		$V_{CC} = 2.1 \text{ V} \text{ to}$ $V_{O} = 2.7 \text{ V}, \overline{\text{OE}}$				10		10		10	μΑ	
I _{OZL}		$V_{CC} = 2.1 \text{ V} \text{ to}$ $V_{O} = 0.5 \text{ V}, \overline{\text{OE}}$				-10		-10		-10	μΑ	
l _{off}		$V_{CC} = 0, V_{I} \text{ or } V_{I}$	/ _O ≤ 4.5 V			±100				±100	μΑ	
ICEX	Outputs high	V _{CC} = 5.5 V,	V _O = 5.5 V			50		50		50	μΑ	
ΙΟ§		V _{CC} = 5.5 V,	V _O = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA	
	Outputs high					2		2		2		
ICC	Outputs low	V _{CC} = 5.5 V, I _O V _I = V _{CC} or GN				85		85		85	mA	
	Outputs disabled					2		2		2		
∆ICC	T		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND			1.5		1.5		1.5	mA	
Ci		V _I = 2.5 V or 0.5	5 V		3.5						pF	
Co		V _O = 2.5 V or 0.	.5 V		9.5						рF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

[†] All typical values are at $V_{CC} = 5$ V.

[‡] This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

 \P This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = 5 V, T _A = 25°C [#]		SN54ABT1	16373A	SN74ABT	UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	
tw	Pulse duration, LE high	3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE \downarrow	1.5		2.4		1.5		ns
t _h	Hold time, data after LE \downarrow	1		2.2		1		ns

[#] These values apply only to the SN74ABT16373A.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

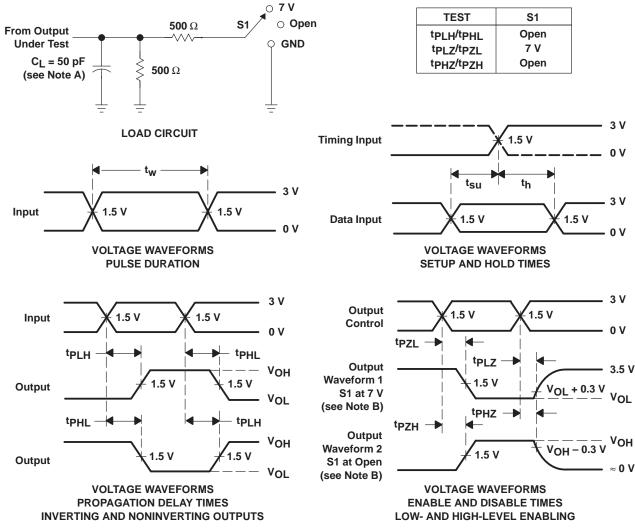
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V(Tj	CC = 5 V A = 25°C	l, ;	MIN	МАХ	UNIT
			MIN	TYP	MAX			
^t PLH	D	Q	1.4	3.7	5.3	1.4	6.5	ns
^t PHL	D	Q	2	4	5.4	2	6.5	115
^t PLH	LE	Q	1.7	4.1	5.7	1.7	7	ns
^t PHL	LL	Q	2.3	4.3	5.6	2.3	6.3	115
^t PZH	OE	Q	1.1	3.4	5	1.1	6.4	ns
^t PZL	ÛE	Q	1.5	3.5	4.9	1.5	5.8	115
^t PHZ	ŌĒ	Q	2.4	5.1	7.1	2.4	8.3	ne
^t PLZ	UE	Q	1.6	4.4	6.3	1.6	8	ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER								
	FROM (INPUT)	TO (OUTPUT)	Vo Тį	CC = 5 V A = 25°C	/, ;	MIN	МАХ	UNIT
			MIN	TYP	MAX			
tPLH	D	Q	1.4	3.7	5.3	1.4	6.3	ns
^t PHL	D	Q.	2	4	5.4	2	6.2	115
^t PLH	LE	Q	1.7	4.1	5.7	1.7	6.7	ns
^t PHL	LL	Q	2.3	4.3	5.6	2.3	6.1	115
^t PZH	OE	Q	1.1	3.4	5	1.1	6.1	ns
^t PZL	ÛE	4	1.5	3.5	4.9	1.5	5.6	115
^t PHZ	ŌĒ	Q	2.4	5.1	7.1	2.4	8.1	ns
tPLZ	UE	Q	1.6	4.4	5.8	1.6	6.5	115



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2.5 ns, t_f \leq 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9320001QXA	ACTIVE	CFP	WD	48	1	TBD	Call TI	Call TI	
74ABT16373ADGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ABT16373ADGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16373ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16373ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16373ADLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16373ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16373ADLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54ABT16373AWD	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



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OTHER QUALIFIED VERSIONS OF SN54ABT16373A, SN74ABT16373A :

Catalog: SN74ABT16373A

- Enhanced Product: SN54ABT16373A-EP, SN74ABT16373A-EP
- Military: SN54ABT16373A

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

Texas Instruments





TAPE AND REEL INFORMATION

TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16373ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ABT16373ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

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PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16373ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ABT16373ADLR	SSOP	DL	48	1000	367.0	367.0	55.0

MECHANICAL DATA

MCFP010B - JANUARY 1995 - REVISED NOVEMBER 1997

CERAMIC DUAL FLATPACK

WD (R-GDFP-F**)

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only
 - E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 - GDFP1-F56 and JEDEC MO-146AB



MECHANICAL DATA

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

DL (R-PDSO-G**)



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118



MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный) **Факс:** 8 (812) 320-02-42 **Электронная почта:** <u>org@eplast1.ru</u> **Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.