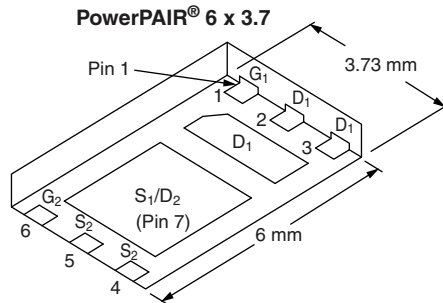


N-Channel 20 V (D-S) MOSFETs

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
Channel-1	20	0.0068 at V _{GS} = 10 V	16 ^a	6.9 nC
		0.0090 at V _{GS} = 4.5 V	16 ^a	
Channel-2	20	0.0033 at V _{GS} = 10 V	35 ^a	18.2 nC
		0.0043 at V _{GS} = 4.5 V	35 ^a	



Ordering Information:
SiZ710DT-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

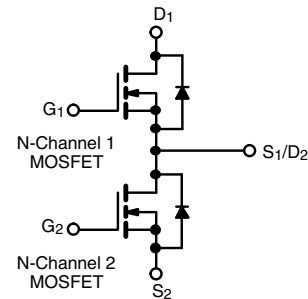
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFETs
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Notebook System Power
- POL
- Synchronous Buck Converter



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
Parameter	Symbol	Channel-1	Channel-2	Unit	
Drain-Source Voltage	V _{DS}	20		V	
Gate-Source Voltage	V _{GS}	± 20			
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	16 ^a	35 ^a	A
		T _C = 70 °C	16 ^a	35 ^a	
		T _A = 25 °C	16 ^{a, b, c}	30 ^{b, c}	
		T _A = 70 °C	15 ^{b, c}	24 ^{b, c}	
Pulsed Drain Current	I _{DM}	70	100	A	
Continuous Source Drain Diode Current	I _S	T _C = 25 °C	16 ^a		35 ^a
		T _A = 25 °C	3.2 ^{b, c}	3.8 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	20	30	mJ	
Single Pulse Avalanche Energy	E _{AS}	20	45		
Maximum Power Dissipation	P _D	T _C = 25 °C	27	48	W
		T _C = 70 °C	17	31	
		T _A = 25 °C	3.9 ^{b, c}	4.6 ^{b, c}	
		T _A = 70 °C	2.5 ^{b, c}	3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260			

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Channel-1		Channel-2		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	24	32	20	27	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	3.5	4.6	2	2.6	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 67 °C/W for channel-1 and 65 °C/W for channel-2.

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1	20			V	
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-2	20				
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1		19		mV/ $^\circ\text{C}$	
		$I_D = 250\text{ }\mu\text{A}$	Ch-2		20			
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1		- 4.8			
		$I_D = 250\text{ }\mu\text{A}$	Ch-2		- 5.3			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1		2.2	V	
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-2	1		2.2		
Gate Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch-1			± 100	nA	
			Ch-2			± 100		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	Ch-1			1	μA	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	Ch-2			1		
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1			5		
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-2			5		
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	15			A	
		$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-2	20				
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 19\text{ A}$	Ch-1		0.0055	0.0068	Ω	
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2		0.0027	0.0033		
		$V_{GS} = 4.5\text{ V}, I_D = 16.5\text{ A}$	Ch-1		0.0072	0.0090		
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	Ch-2		0.0034	0.0043		
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 19\text{ A}$	Ch-1		45		S	
		$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2		85			
Dynamic^a								
Input Capacitance	C_{iss}	Channel-1 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		820		pF	
			Ch-2		2310			
Output Capacitance	C_{oss}		Channel-2 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		290		
				Ch-2		730		
Reverse Transfer Capacitance	C_{rss}	Channel-1 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		Ch-1		115		
				Ch-2		305		
Total Gate Charge	Q_g		$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 19\text{ A}$	Ch-1		11.5	18	nC
				Ch-2		38	60	
		$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-1		6.9	11		
			Ch-2		18.2	28		
Gate-Source Charge	Q_{gs}	Channel-1 $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 16.8\text{ A}$	Ch-1		2.4			
			Ch-2		6.6			
Gate-Drain Charge	Q_{gd}		Channel-2 $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	Ch-1		1.7		
				Ch-2		4.8		
Gate Resistance	R_g	$f = 1\text{ MHz}$		Ch-1	0.3	1.3	2.6	Ω
				Ch-2	0.2	0.8	1.6	

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



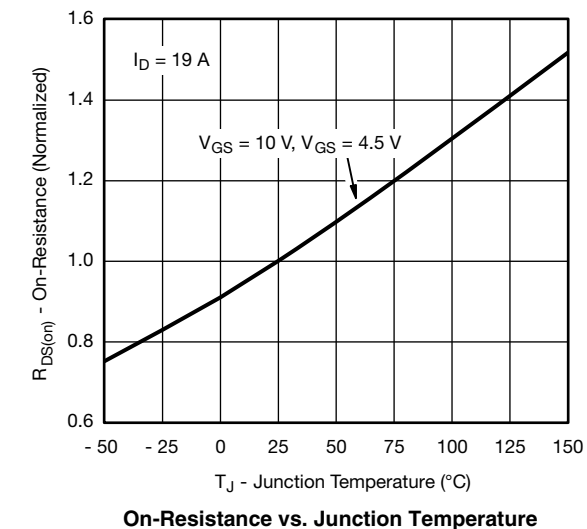
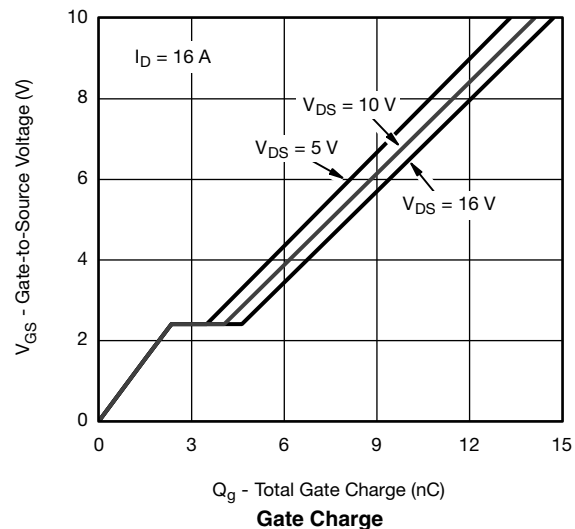
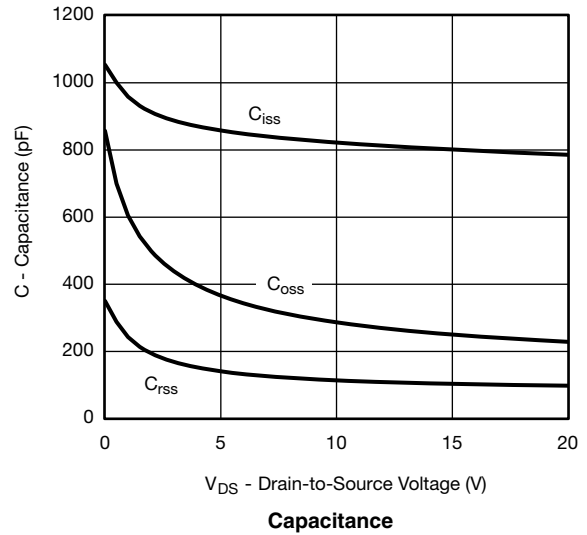
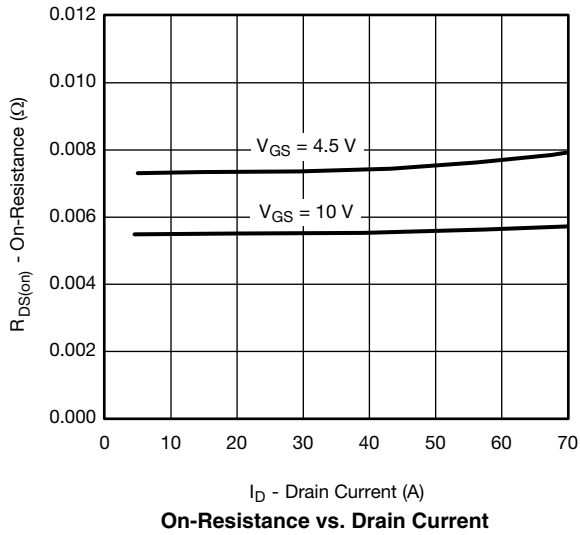
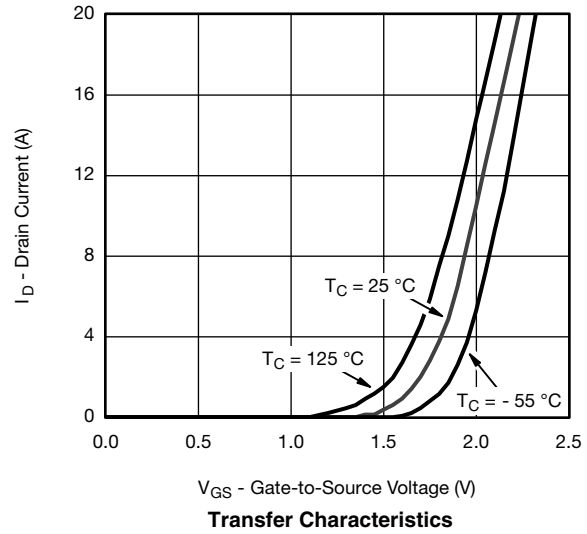
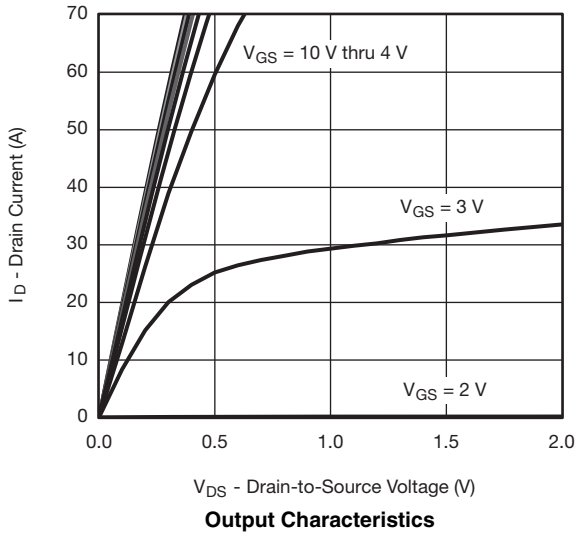
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
Dynamic^a								
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 10\text{ V}, R_L = 1\ \Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\ \Omega$	Ch-1		15	30	ns	
			Ch-2		25	50		
Rise Time	t_r		Ch-1		15	30		
			Ch-2		15	30		
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 10\text{ V}, R_L = 1\ \Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\ \Omega$	Ch-1		20	40		
			Ch-2		30	60		
Fall Time	t_f		Ch-1		12	25		
			Ch-2		12	25		
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 10\text{ V}, R_L = 1\ \Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	Ch-1		10	20		
			Ch-2		15	30		
Rise Time	t_r		Ch-1		12	25		
			Ch-2		8	15		
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 10\text{ V}, R_L = 1\ \Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	Ch-1		20	40		
			Ch-2		30	60		
Fall Time	t_f		Ch-1		10	20		
			Ch-2		10	20		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	Ch-1			16	A	
			Ch-2			35		
Pulse Diode Forward Current ^a	I_{SM}		Ch-1			70		
			Ch-2			100		
Body Diode Voltage	V_{SD}	$I_S = 10\text{ A}, V_{GS} = 0\text{ V}$	Ch-1		0.8	1.2	V	
		$I_S = 10\text{ A}, V_{GS} = 0\text{ V}$	Ch-2		0.78	1.2		
Body Diode Reverse Recovery Time	t_{rr}	Channel-1 $I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	Ch-1		15	30	ns	
			Ch-2		25	50		
Body Diode Reverse Recovery Charge	Q_{rr}			Ch-1		5.5	11	nC
				Ch-2		17	35	
Reverse Recovery Fall Time	t_a	Channel-2 $I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	Ch-1		6		ns	
			Ch-2		14			
Reverse Recovery Rise Time	t_b			Ch-1		9		
				Ch-2		11		

Notes:

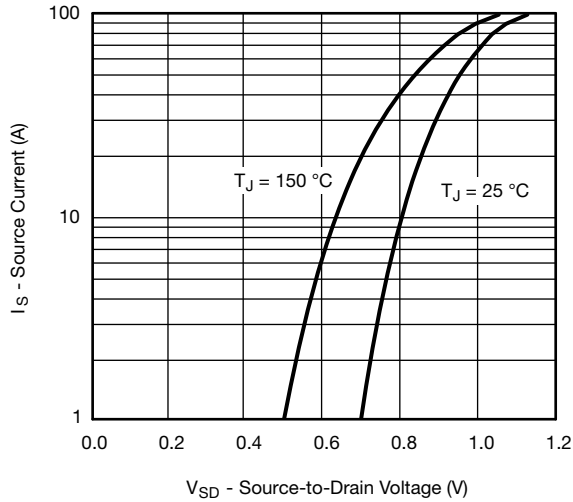
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

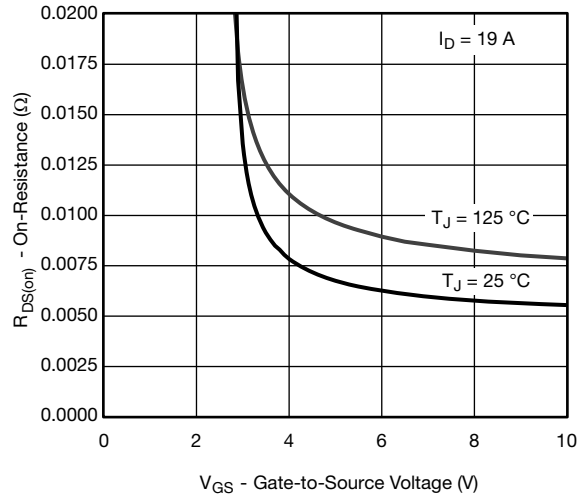
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



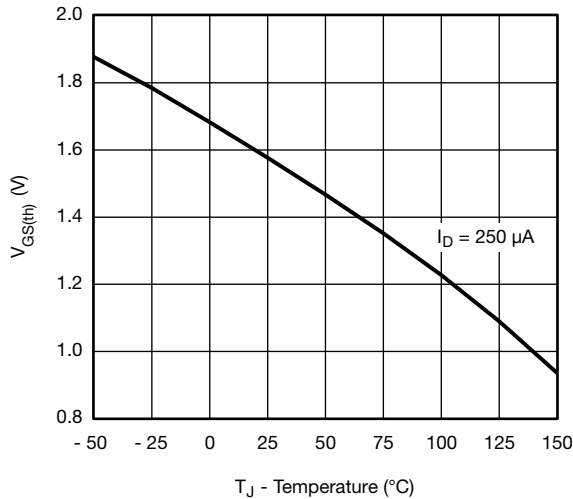
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



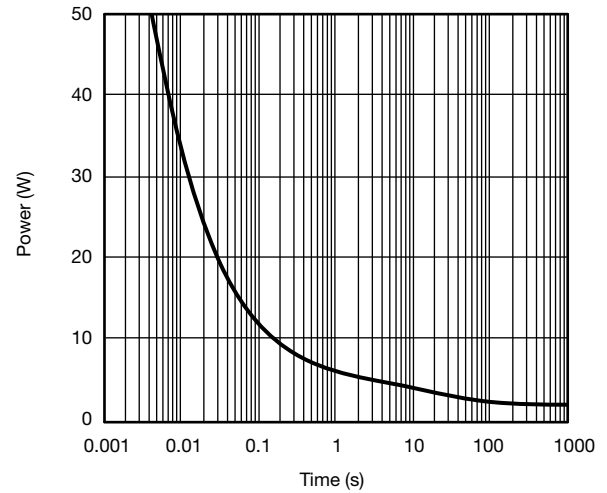
Source-Drain Diode Forward Voltage



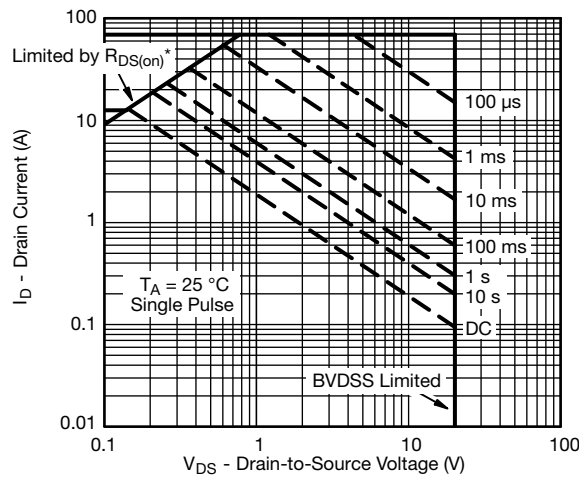
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



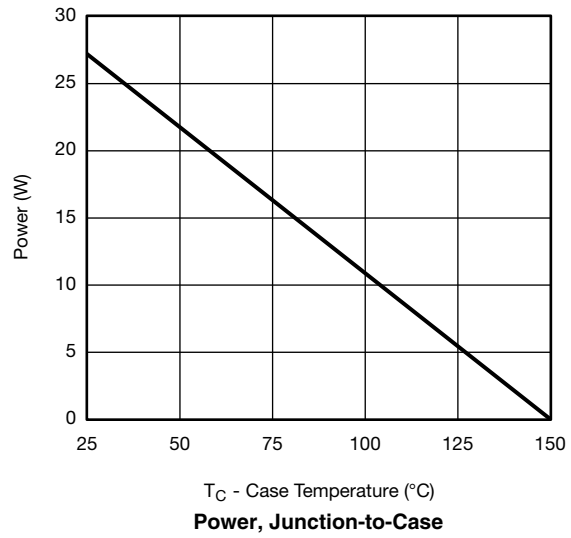
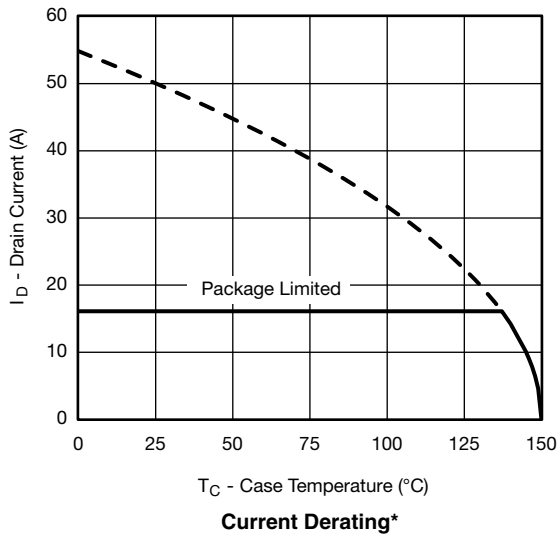
Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

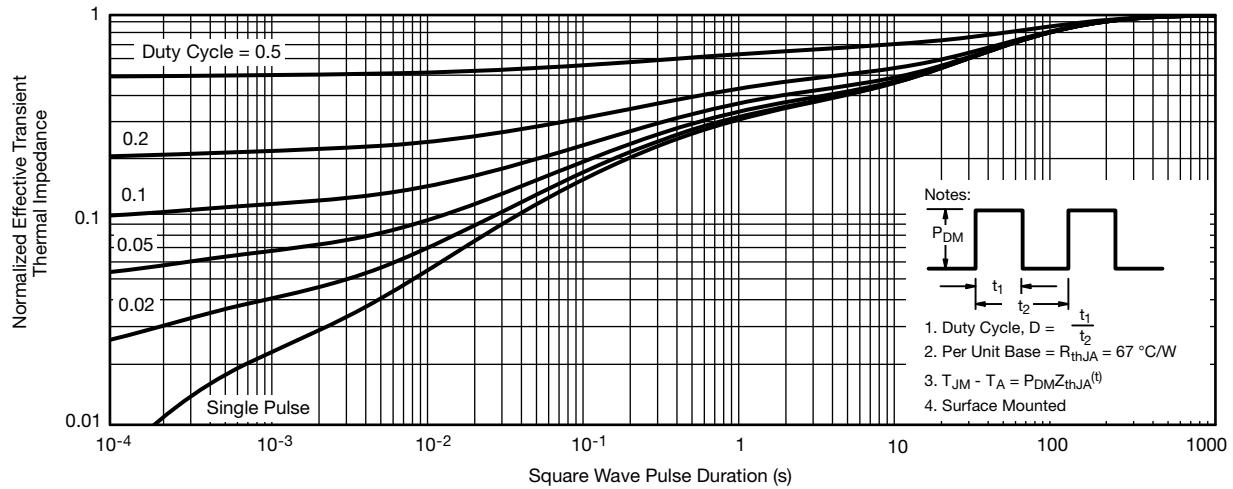
Safe Operating Area, Junction-to-Ambient

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

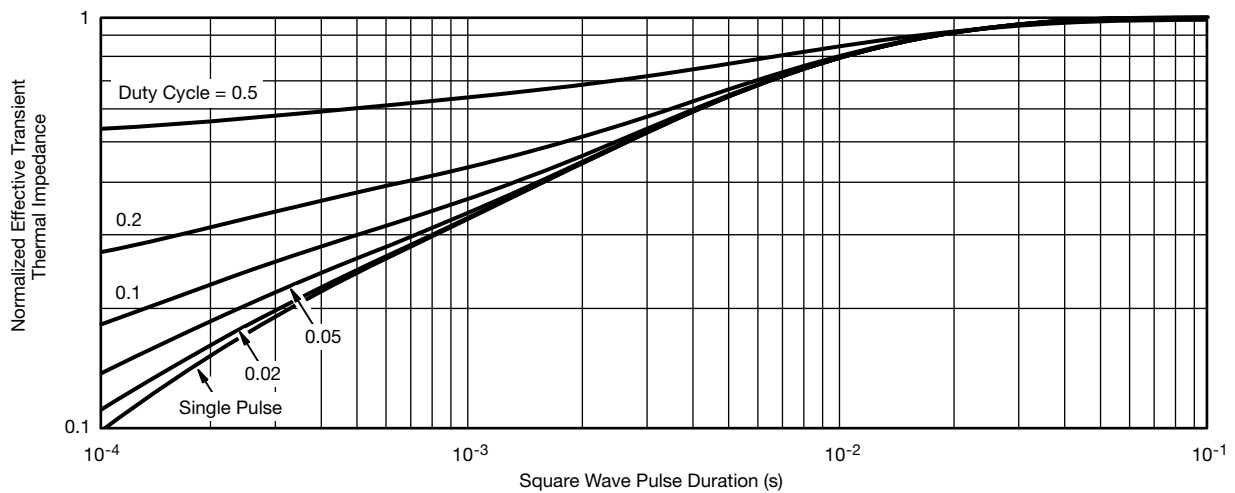


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

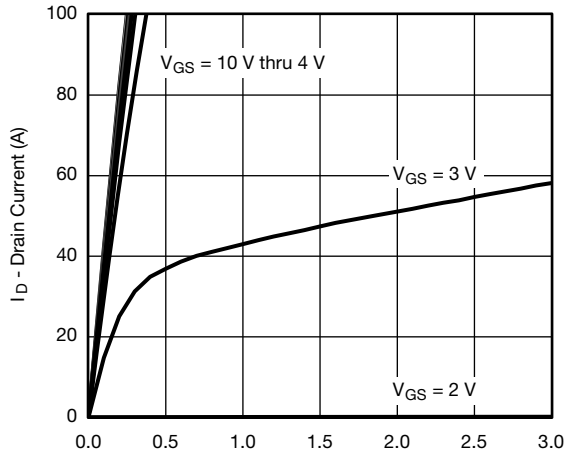


Normalized Thermal Transient Impedance, Junction-to-Ambient

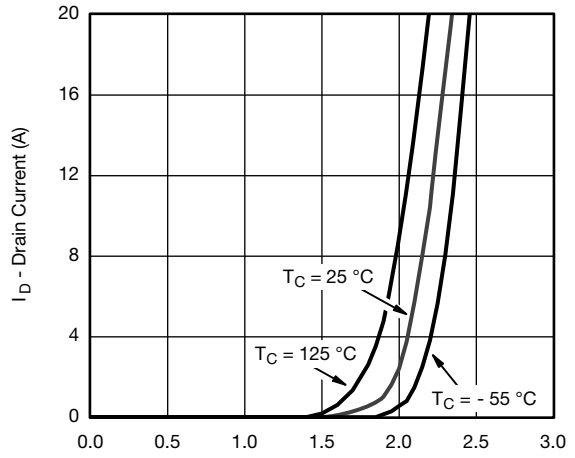


Normalized Thermal Transient Impedance, Junction-to-Case

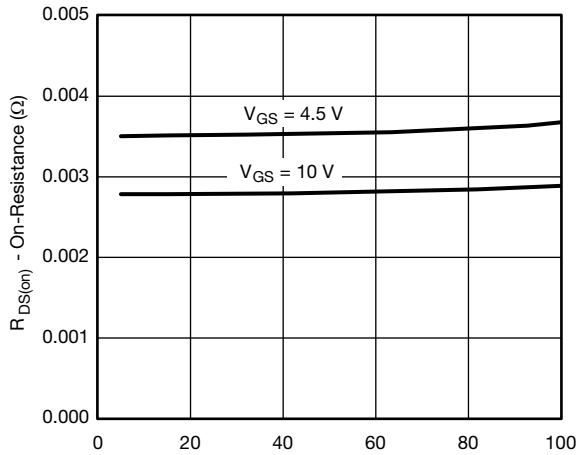
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



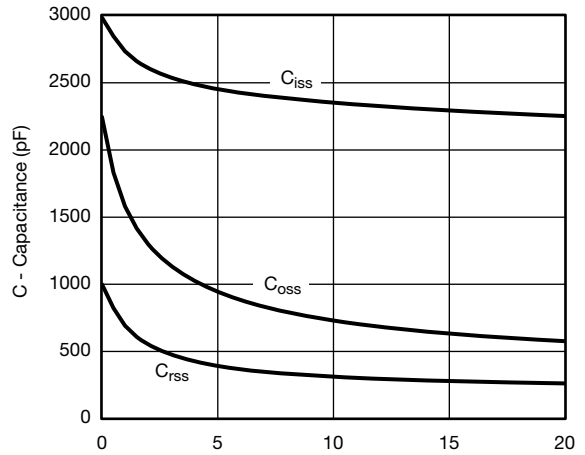
Output Characteristics



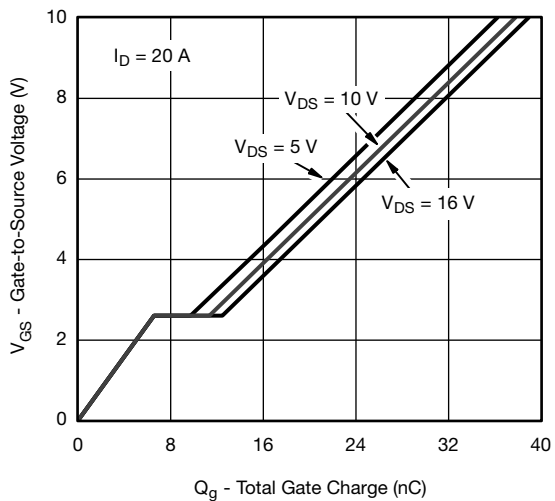
Transfer Characteristics



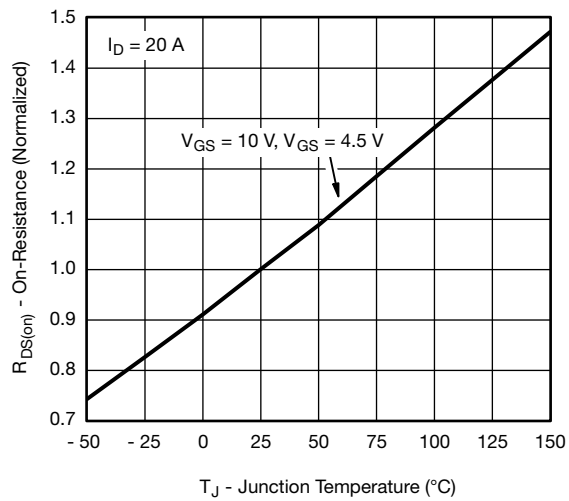
On-Resistance vs. Drain Current



Capacitance

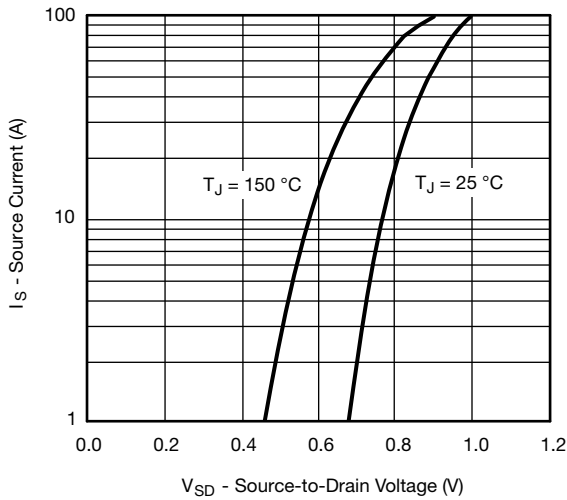


Gate Charge

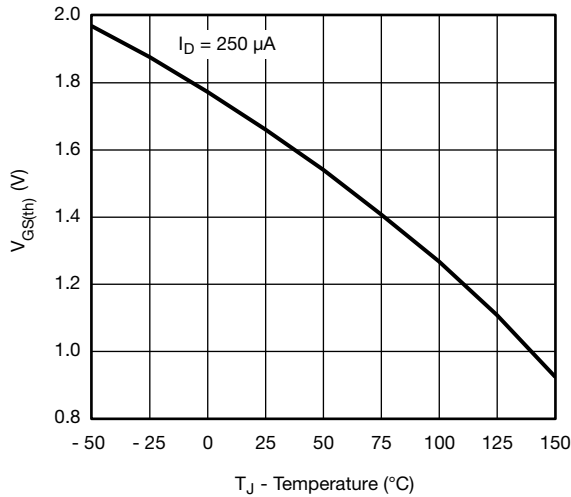


On-Resistance vs. Junction Temperature

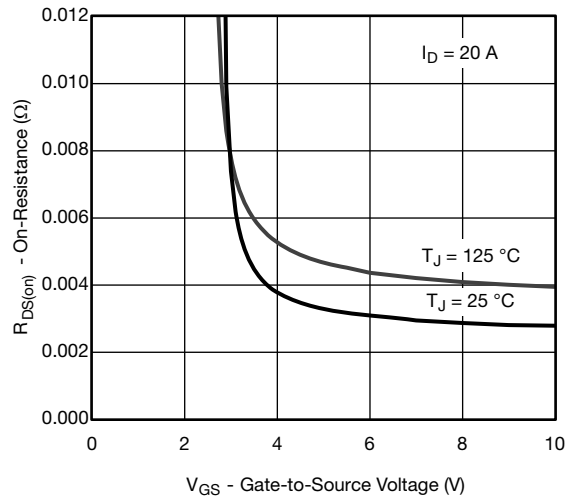
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



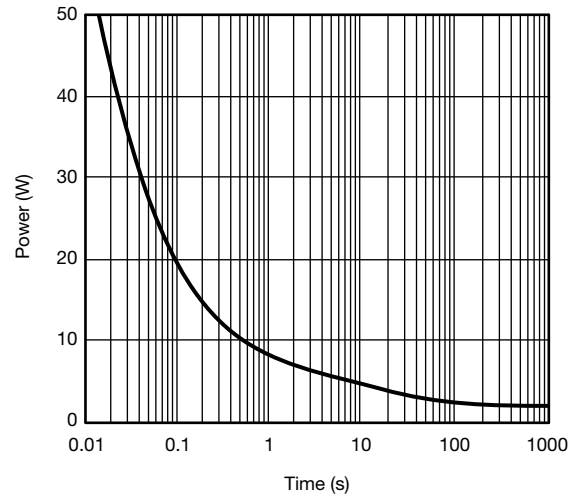
Source-Drain Diode Forward Voltage



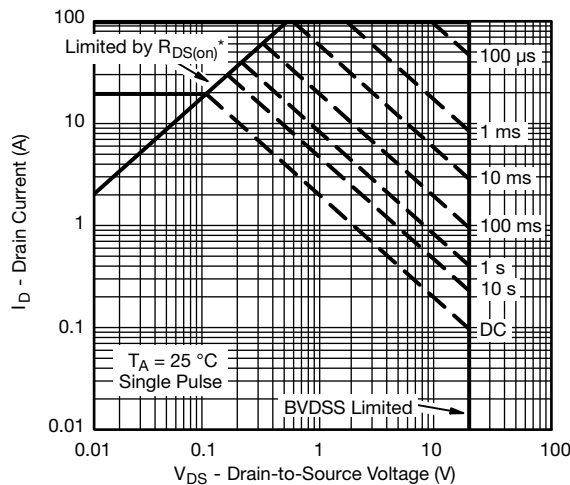
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



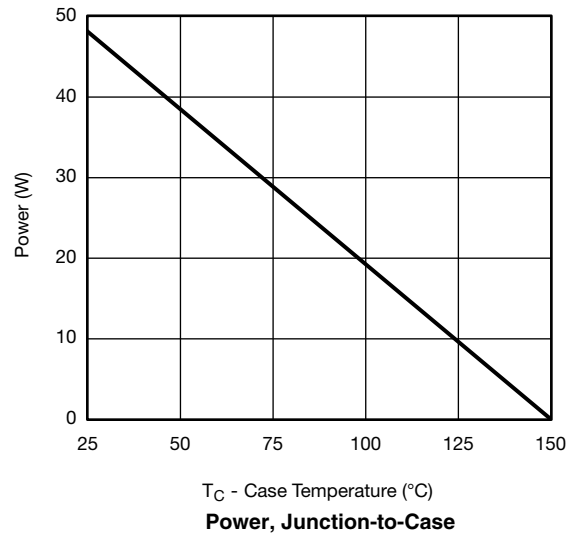
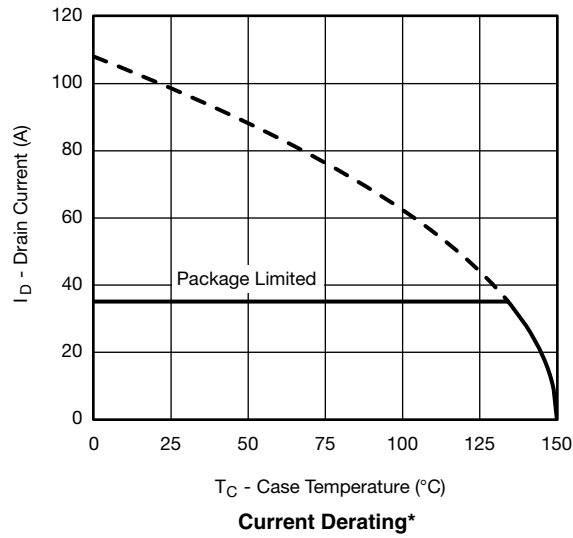
Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

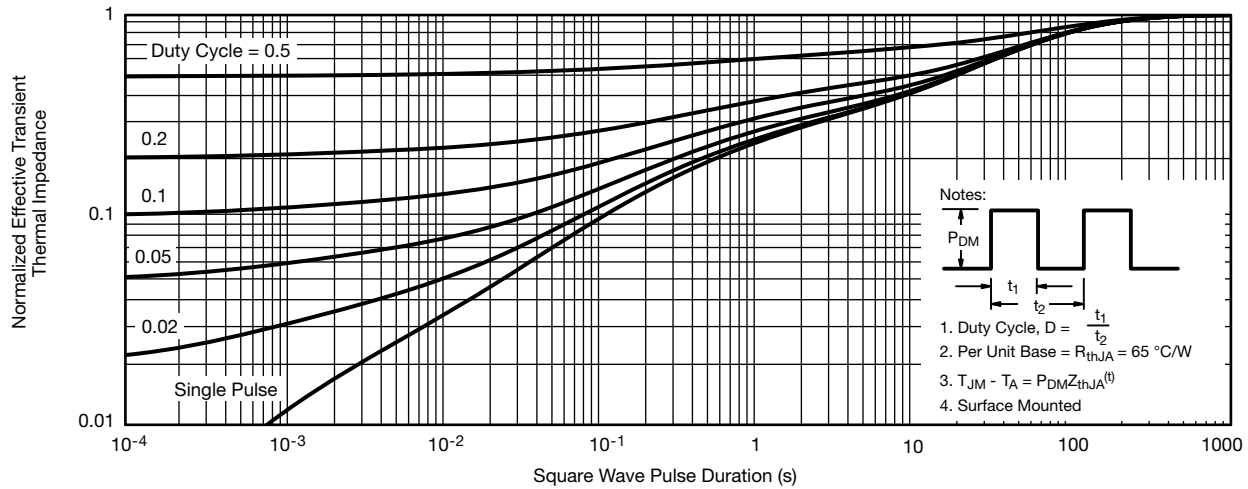
Safe Operating Area, Junction-to-Ambient

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

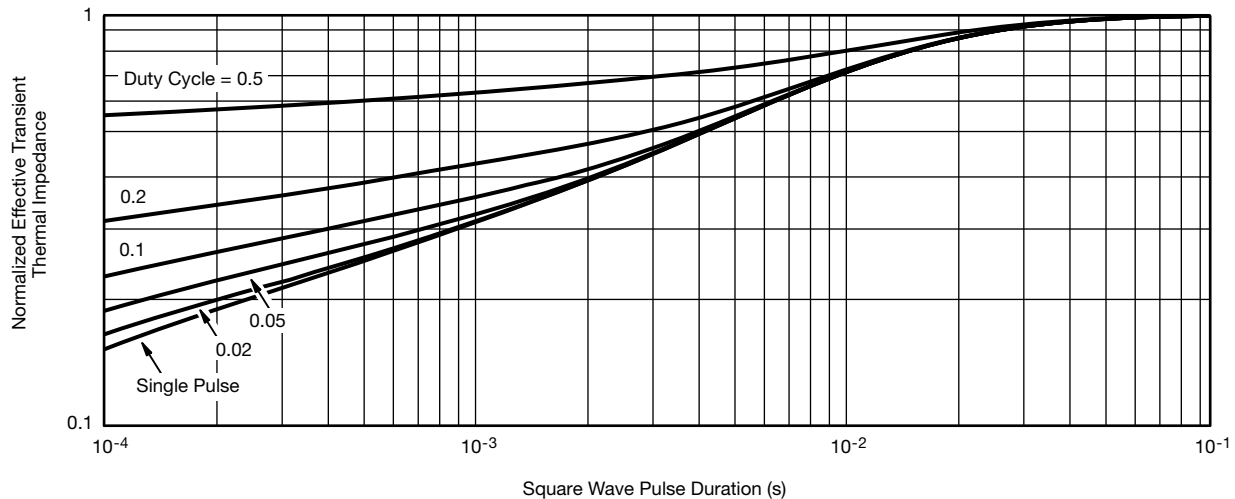


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65733.

PowerPAIR™ 6 x 3.7 CASE OUTLINE



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	-	0.05	0.000	-	0.002
b	0.46	0.51	0.56	0.018	0.020	0.022
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	3.65	3.73	3.81	0.144	0.147	0.150
D1	2.41	2.53	2.65	0.095	0.100	0.104
E	5.92	6.00	6.08	0.233	0.236	0.239
E1	2.62	2.67	2.72	0.103	0.105	0.107
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.05 BSC		
K	0.45 TYP.			0.018 TYP.		
K1	0.66 TYP.			0.026 TYP.		
K2	0.60 TYP.			0.024 TYP.		
L	0.38	0.43	0.48	0.015	0.017	0.019
ECN: S-82772-Rev. B, 17-Nov-08 DWG: 5979						

RECOMMENDED PAD FOR PowerPAIR™ 6 x 3.7



Recommended PAD for PowerPAIR 6 x 3.7
Dimensions in inches (mm)
Keep-out 0.3520 (8.94) x 0.4390 (11.151)



Disclaimer

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Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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