MAX9291/MAX9293

3.12Gbps GMSL Serializers for Coax or STP Output and HDMI Input

General Description

The MAX9291/MAX9293 GMSL serializers convert an HDMI input to a gigabit multimedia serial link (GMSL) output for transmission of video, audio, and control signals over 15m or more of 50Ω coax or 100Ω shielded twisted-pair (STP) cable. The MAX9293 has HDCP content protection, but is otherwise the same as the MAX9291. The serializers pair with any GMSL deserializer capable of coax input. When programmed for STP output, the serializers are backward compatible with any GMSL deserializer. The output amplitude is programmable 100mV to 500mV single-ended (coax) or 100mV to 400mV differential (STP).

The audio channel supports L-PCM I²S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth up to 32 bits.

The embedded control channel operates at 9.6kbps to 1Mbps in UART-to-UART and UART-to-I²C modes, and up to 1Mbps in I²C-to-I²C mode. Using the control channel, a µC can program serializer, deserializer, and peripheral device registers at any time, independent of video timing and manage HDCP operation (MAX9293). A GPO output supports touch-screen controller interrupt requests from the remote end of the link.

For use with longer cables, the serializers have programmable pre/deemphasis. Programmable spread spectrum is available on the serial output. The serial output meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply is 1.8V and 3.3V and the I/O supply is 1.7V to 3.6V. The package is a lead(Pb)-free, 56-pin, 8mm x 8mm TQFN with exposed pad and 0.5mm lead pitch.

Applications

- High-Resolution Automotive Navigation
- Rear-Seat Infotainment
- Megapixel Camera Systems

Ordering Information ***appears at end of data sheet.***

Benefits and Features

- Ideal for High-Definition Video Applications
  - HDMI 1.4a Input with Integrated Input Equalizer, DDC, and Input Termination
  - Drives Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP Cable
  - 104MHz High-Bandwidth Mode Supports 1920 x 720p/60Hz Display with 24-Bit Color
  - Serializer Pre/Deemphasis Allows 15m Cable at Full Speed
  - Up to 192kHz Sample Rate and 32-Bit Sample Depth for 7.1 Channel HD Audio
- Multiple Data Rates for System Flexibility
  - Up to 3.12Gbps Serial-Bit Rate
  - 25MHz to 104MHz Pixel Clock
  - 9.6kbps to 1Mbps Control Channel in UART, Mixed UART/I²C, or I²C Mode with Clock-Stretch Capability
- Reduces EMI and Shielding Requirements
  - Serial Output Programmable for 100mV to 500mV Single-Ended or 100mV to 400mV Differential
  - Programmable Spread Spectrum Reduces EMI
  - Tracks Spread Spectrum on Input
  - High-Immunity Mode for Maximum Control-Channel Noise Rejection
- Peripheral Features for System Power-Up and Verification
  - Built-In PRBS Generator for BER Testing of the Serial Link
  - Programmable Choice of 9 Default Device Addresses
  - Dedicated “Up/Down” GPO for Touch-Screen Interrupt and Other Uses
  - Remote/Local Wake-Up from Sleep Mode
- Meets Rigorous Automotive and Industrial Requirements
  - -40°C to +105°C Operating Temperature
  - ±8kV Contact and ±15kV Air ISO 10605 and IEC 61000-4-2 ESD Protection

19-7544; Rev 1; 9/15

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Absolute Maximum Ratings (Note 1)

AVDD to EP .....-0.5V to +1.9V
DVDD to EP .....-0.5V to +1.9V
RVDD to EP .....-0.5V to +1.9V
IOVDD to EP .....-0.5V to +3.9V
HVDD to EP .....-0.5V to +3.9V
PLLVDD to EP .....-0.5V to +3.9V
XVDD to EP .....-0.5V to +3.9V
RX_, RXC_ to EP .....-0.5V to +3.9V
LMN_ to EP (15mA current limit) .....-0.5V to +3.9V
OUT+, OUT- to EP .....-0.5V to +1.9V
All Other Pins to EP ..... -0.5V to + (V_{IOVDD} + 0.5V)
OUT+, OUT- Short Circuit to Ground or Supply .....Continuous
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 47.6mW/°C above +70°C) 3809.5mW
Junction Temperature .....+150°C
Storage Temperature Range .....-65ºC to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: EP connected to PCB ground.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....21°C/W
Junction-to-Case Thermal Resistance (θ_{JA}) .....1°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{RVDD} = V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TWO-LEVEL INPUTS (HSPD, I2CSEL, $\overline{PWDN}$, CDS, MS, $\overline{AUTOS}$, CX/TP, SD, SCK, WS, CNTL1, CNTL2, SSEN, DRS, HIM)						
High-Level Input Voltage	V_{IH1}		0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}				0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0 to V_{IOVDD}	-20		+20	µA
THREE-LEVEL INPUTS (ADD0, ADD1, BWS)						
High-Level Input Voltage	V_{IH2}		0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}				0.3 x V_{IOVDD}	V
Mid-Level Input Current	I_{INM}	(Note 3)	-10		+10	µA
Input Current	I_{IN2}		-150		+150	µA

DC Electrical Characteristics (continued)

(V_{RVDD} = V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
HOT-PLUG DETECT OUTPUT (HPD)							
High-Level Output Voltage	V_{OH1}	I_{OH} = -2mA		V_{HVDD} - 0.2			V
Low-Level Output Voltage	V_{OL1}	I_{OL} = 2mA				0.2	V
Output Short-Circuit Current	I_{OS1}	V_O = 0V		16	35	64	mA
SINGLE-ENDED OUTPUTS (GPO, SD, SCK, WS, INTOUT)							
High-Level Output Voltage	V_{OH2}	I_{OH} = -2mA		V_{IOVDD} – 0.2			V
Low-Level Output Voltage	V_{OL2}	I_{OL} = 2mA				0.2	V
Output Short-Circuit Current	I_{OS2}	V_O = 0V	V_{IOVDD} = 3.0V to 3.6V	16	35	64	mA
			V_{IOVDD} = 1.7V to 1.9V	3	12	21	
OPEN-DRAIN INPUT/OUTPUTS (RX/SDA, TX/SCL, DDCSDA, DDCSCL, $\overline{LFLT}$)							
High-Level Input Voltage	V_{IH3}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL3}					0.3 x V_{IOVDD}	V
Input Current	I_{IN3}	(Note 4)	RX/SDA, TX/SCL, DDCSDA, DDCSCL	-110		5	µA
			$\overline{LFLT}$	-80		5	
Low-Level Output Voltage	V_{OL3}	I_{OL} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
Capacitance	C_i	Each pin (Note 5)				10	pF
GMSL DIFFERENTIAL OUTPUTS (OUT+, OUT-)							
Differential Output Voltage	V_{OD}	Pre/deemphasis off		300	400	500	mV
		3.3dB preemphasis (Note 5)		350		610	
		3.3dB deemphasis		240		425	
Change in V_{OD} Between Complimentary Output States	ΔV_{OD}	Preemphasis off and deemphasis only				25	mV
Output Offset Voltage (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	Preemphasis off		1.1	1.4	1.56	V

DC Electrical Characteristics (continued)

(V_{RVDD} = V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Change in V_{OS} Between Complimentary Output States	ΔV_{OS}				25	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V	-62			mA
		V_{OUT+} or V_{OUT-} = 1.9V			25	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V			25	mA
Output Termination Resistance (Internal)	R_O	From OUT+ or OUT- to V_{AVDD}	45	54	63	Ω
REVERSE CONTROL-CHANNEL RECEIVER (Internally Connected to OUT+, OUT-)						
High Switching Threshold	V_{CHR}	Legacy			27	mV
		High-immunity			40	
Low Switching Threshold	V_{CLR}	Legacy	-27			mV
		High-immunity	-40			
GMSL SINGLE-ENDED OUTPUTS (OUT+, OUT-)						
Single-Ended Output Voltage	V_{OUT}	Pre/deemphasis off	375	500	625	mV
		3.3dB preemphasis (Note 5)	435		765	
		3.3dB deemphasis	300		535	
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V	-69			mA
		V_{OUT+} or V_{OUT-} = 1.9V			32	
Output Termination Resistance (Internal)	R_O	From OUT+ or OUT- to V_{AVDD}	45	54	63	Ω
LINE-FAULT DETECTION INPUTS (LMN0, LMN1)						
Short-to-GND Threshold	V_{TG}				0.3	V
Normal Thresholds	V_{TN}		0.57		1.07	V
Open Thresholds	V_{TO}		1.45		V_{IO} + 0.06	V
Open Input Voltage	V_{IO}		1.47		1.75	V
Short-to-Battery Threshold	V_{TE}		2.47			V
HDMI DIFFERENTIAL INPUTS (RX_, RXC_)						
Input Differential Voltage Level	V_{IDIFF1}	(Note 5)	150		1200	mV_{P-P}

DC Electrical Characteristics (continued)

(V_{RVDD} = V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Voltage Level	V_{DIFFD}	Source disabled or disconnected		-10		10	mV
Input Common-Mode Voltage	V_{ICM}	DC-coupled (Note 5)		V_{HVDD} - 300		V_{HVDD} - 37.5	mV
		AC-coupled (Note 5)		V_{HVDD} - 10		V_{HVDD} + 10	
Termination Resistance	R_T	Each pin to V_{HVDD} (Note 5)	TERM_CNTL = '010' (default)	49	55	61	Ω
			TERM_CNTL = '011'	44	50	56	
CRYSTAL OSCILLATOR (X1, X2)							
Frequency		Fundamental mode only; includes crystal tolerance			27		MHz
Input Capacitance	C_{X1}, C_{X2}	Each pin			4		pF
Load Capacitance	C_{L1}, C_{L2}	XTAL property			18		pF
OSCILLATOR INPUT (X1)							
High-Level Input Voltage	V_{IHX}	X1 as frequency Input		0.70 x V_{XVDD}			V
Low-Level Input Voltage	V_{ILX}	X1 as frequency Input				0.30 x V_{XVDD}	V
Input Current	I_{INX}	V_{IN} = 0 to V_{XVDD}		-5		+5	µA
Input Frequency Range		X1 as frequency Input (Note 5)		26		28.5	MHz

DC Electrical Characteristics (continued)

(V_{RVDD} = V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Worst-Case Pattern Supply Current, DRS = low) (Notes 6, 7)	I_{WCS2}	$f_{RXC_}$ = 25MHz BWS = high	HVDD		46	61	mA
			RVDD + AVDD + DVDD		172	237	
			PLLVDD + XVDD		11	16	
			IOVDD (3.0V to 3.6V)		2	2	
			IOVDD (1.7V to 1.9)		0.5	0.6	
		$f_{RXC_}$ = 78MHz BWS = high	HVDD		46	61	
			RVDD + AVDD + DVDD		297	425	
			PLLVDD + XVDD		11	16	
			IOVDD (3.0V to 3.6V)		2	2	
			IOVDD (1.7V to 1.9)		0.5	0.6	
		$f_{RXC_}$ = 36.66MHz BWS = open	HVDD		46	61	
			RVDD + AVDD + DVDD		195	275	
			PLLVDD + XVDD		11	16	
			IOVDD (3.0V to 3.6V)		2	2	
			IOVDD (1.7V to 1.9)		0.5	0.6	
		$f_{RXC_}$ = 104MHz BWS = open	HVDD		46	61	
			RVDD + AVDD + DVDD		347	500	
			PLLVDD + XVDD		11	16	
			IOVDD (3.0V to 3.6V)		2	2	
			IOVDD (1.7V to 1.9)		0.5	0.6	

DC Electrical Characteristics (continued)

(V_{RVDD} = V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Sleep-Mode Supply Current	I_{CCS}	Single wake-up receiver enabled				2	mA
Power-Down Supply Current	I_{CCZ}	$\overline{PWDN}$ = EP				2	mA
ESD PROTECTION							
OUT+, OUT- (Pin to EP)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF			±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge		±8		
			Air discharge		±12		
		ISO 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge		±10		
			Air discharge		±25		
All Other Pins (to EP or Supply)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF			±4		kV
		Machine Model			±250		V
All Other Pins (to All Other Pins)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF			±2.5		kV

AC Electrical Characteristics

(V_{RVDD} =V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ±1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OPEN-DRAIN OUTPUTS (RX/SDA, TX/SCL)							
Output Rise Time	t_R	0.3 x V_{IOVDD} to 0.7 x V_{IOVDD}, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		150	ns
Output Fall Time	t_F	0.7 x V_{IOVDD} to 0.3 x V_{IOVDD}, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		150	ns
I^2C (SDA, SCL, DDCSDA, DDCSCL) (see Figure 6) (Note 8)							
SCL Clock Frequency	f_{SCL}		Low range	9.6		100	kHz
			Mid range	> 100		400	
			High range	> 400		1000	
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range	Low	4.0			µs
			Mid	0.6			
			High	0.26			

AC Electrical Characteristics (continued)

(V_{RVDD} =V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ±1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low Period of SCL Clock	t_{LOW}	f_{SCL} range	Low	4.7			µs
			Mid	1.3			
			High	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range	Low	4.0			µs
			Mid	0.6			
			High	0.26			
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range	Low	4.7			µs
			Mid	0.6			
			High	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range	Low	0			µs
			Mid	0			
			High	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range	Low	250			ns
			Mid	100			
			High	50			
Setup Time for STOP Condition	$t_{SU:STO}$	f_{SCL} range	Low	4.0			µs
			Mid	0.6			
			High	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range	Low	4.7			µs
			Mid	1.3			
			High	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range	Low			3.45	µs
			Mid			0.9	
			High			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range	Low			3.45	µs
			Mid			0.9	
			High			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range	Low			50	ns
			Mid			50	
			High			50	
Capacitive Load Each Bus Line	C_B					100	pF
SINGLE-ENDED OUTPUTS (GPO, SD, SCK, WS, INTOUT)							
Rise-and-Fall Time	t_R, t_F	20% to 80%, C_L = 10pF (Note 5)	V_{IOVDD} = 1.7V to 1.9V	0.5		3.6	ns
			V_{IOVDD} = 3.0 to 3.6V	0.3		2.2	

AC Electrical Characteristics (continued)

(V_{RVDD} =V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ±1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GMSL DIFFERENTIAL OUTPUTS (OUT+, OUT-)							
Rise-and-Fall Time	t_R, t_F	20% to 80%, V_{OD} ≥ 400mV, R_L = 100Ω, serial bit rate = 3.12Gbps (Note 5)			90	160	ps
Total Serial Output Jitter	t_{TSOJ1}	3.12Gbps PRBS, measured at V_{OD} = 0V, pre/deemphasis disabled			0.25		UI
Deterministic Serial Output Jitter	t_{DSOJ2}	3.12Gbps PRBS, measured at V_{OD} = 0V, pre/deemphasis disabled			0.15		UI
GMSL SINGLE-ENDED OUTPUT (OUT+ or OUT-)							
Rise-and-Fall Time	t_R, t_F	20% to 80%, V_O ≥ 500mV, R_L = 50Ω, serial bit rate = 3.12Gbps (Note 5)			90	160	ps
Total Serial Output Jitter	t_{TSOJ1}	3.12Gbps PRBS, measured at V_O/2, pre/deemphasis disabled			0.25		UI
Deterministic Serial Output Jitter	t_{DSOJ2}	3.12Gbps PRBS, measured at V_O/2, pre/deemphasis disabled			0.15		UI
HDMI DIFFERENTIAL INPUTS (RX_ _, RXC_) (Note 5)							
Input Differential Voltage Level	V_{IDIFF2}	.		150		1560	mV_{P-P}
Intra-Pair Skew	t_{SKEW1}					0.4 x t_{BIT}	ns
Inter-Pair Skew	t_{SKEW2}					0.2 x t_{CHAR} + 1.78	ns
Clock Frequency	f_{RxC}	BWS = high, DRS = low		25		78	MHz
		BWS = open, DRS = low		36.6		104	
		BWS = open, DRS bit = high		25		52	
TMDS Clock-Jitter Tolerance	t_{JTMDS}	Relative to ideal recovery clock				0.3 x t_{BIT}	ns
Termination Impedance	Z_{TERM}	TDR rise time ≤ 200ps, 10% to 90%	V_{ICM} within V_{ICM2} range, AC-coupled, V_{HVDD} ±10mV (Note 9)	65	100	135	Ω
GENERAL TIMING							
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to MAX9291/MAX9293 GPO				350	µs

AC Electrical Characteristics (continued)

(V_{RVDD} =V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ±1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

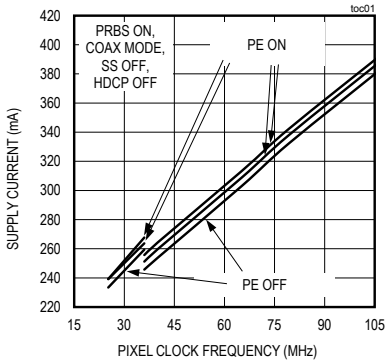
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Device Delay	t_{SD}	(Notes 5, 10)	Spread spectrum enabled	83		174	Bits
			Spread spectrum disabled	99		126	
Link Start Time	t_{LOCK}	PLLs locked				3.5	ms
Power-Up Time	t_{PU}					8	ms
I^2S/TDM							
WS Frequency	f_{WS}			8		192	kHz
Sample Word Length	n_{WS}			8		32	Bits
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times (2 \text{ or } 8)$		(8 x 8) x 2		(192 x 32) x 8	kHz
SCK Clock High Time	t_{HC}	$V_{SCK} \geq V_{IH}$, $t_{SCK} = 1/f_{SCK}$		0.35 x t_{SCK}			ns
SCK Clock Low Time	t_{LC}	$V_{SCK} \leq V_{IL}$, $t_{SCK} = 1/f_{SCK}$		0.35 x t_{SCK}			ns
SD, WS Setup Time	t_{SET}			2			ns
SD, WS Hold Time	t_{HOLD}			2			ns

Note 3: For mid-level, leave the input open. If driven, put driver in high impedance with high-impedance leakage current ±10µA (max).
Note 4: IIN MIN due to voltage drop across the internal pullup resistor.
Note 5: Not production tested. Guaranteed by design.
Note 6: Typical values measured at V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, V_{RVDD} = V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V.
Note 7: HDCP not enabled (MAX9293 only).
Note 8: DDCSDA and DDCSCL specified for operation in 100kHz (low range) only. Characterized at 100kHz and 400kHz..
Note 9: A single excursion is permitted to 100Ω ±25% with duration less than 250ps.
Note 10: Measured in serial link bit times. Bit time = 1/(30 x f_{PCLKIN}) for BWS = open. Bit time = 1/(40 x f_{PCLKIN}) for BWS = high.

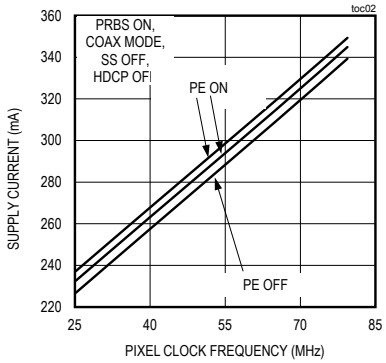
Typical Operating Characteristics

(V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C, unless otherwise noted.)

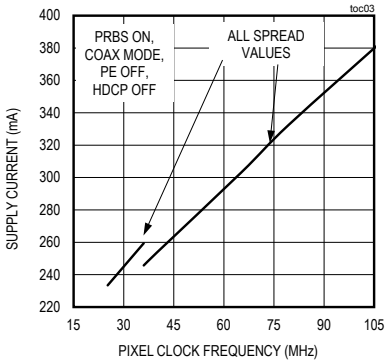
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = OPEN)



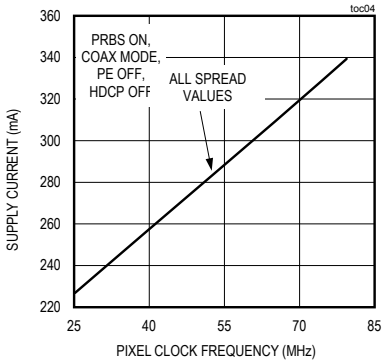
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = HIGH)



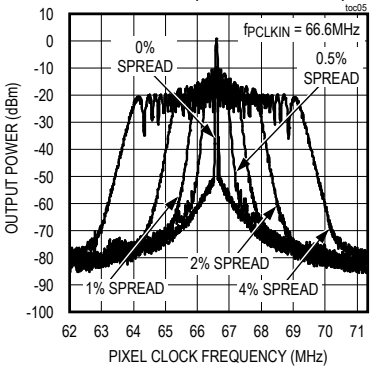
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = OPEN)



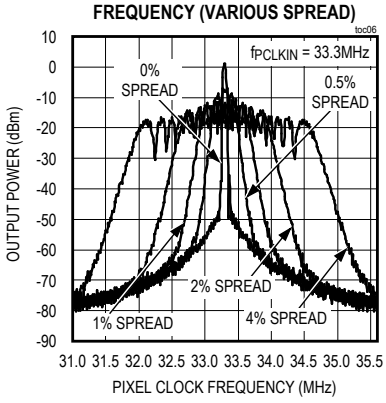
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = HIGH)



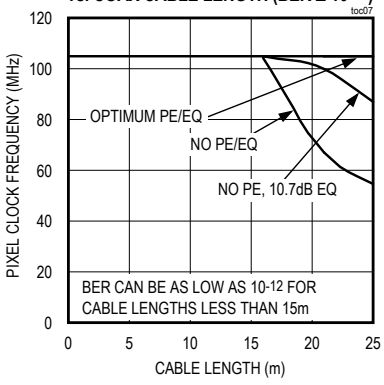
OUTPUT SPECTRUM vs. PIXEL CLOCK FREQUENCY (VARIOUS SPREAD)



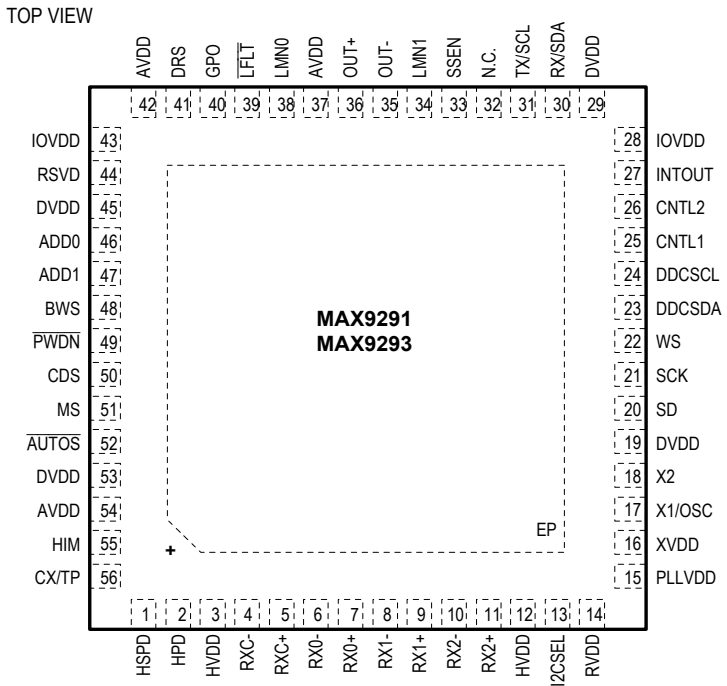
OUTPUT SPECTRUM vs. PIXEL CLOCK FREQUENCY (VARIOUS SPREAD)



MAXIMUM PIXEL CLOCK FREQUENCY vs. COAX CABLE LENGTH (BER ≤ 10^{-10})



Pin Configuration



TQND
(8mm x 8mm)

Pin Description

PIN	NAME	FUNCTION
1	HSPD	HDMI Source Power-Detect Input. Internal pulldown to EP Connect a voltage-divider to divide the 5V HDMI voltage down to V_{IOVDD}.
2	HPD	HDMI Hot-Plug Detect Output
3, 12	HVDD	3.135 to 3.465V HDMI Input Termination Power Supply. Bypass HVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to HVDD.
4, 5	RXC-, RXC+	HDMI Clock Inputs with Internal 50Ω Termination to HVDD
6–11	RX_-, RX_+	HDMI Data Inputs with Internal 50Ω Termination to HVDD
13	I2CSEL	I^2C Select. Control-channel interface protocol select input with internal pulldown to EP. Set I2CSEL = high to select I^2C-to-I^2C interface. Set I2CSEL = low to select UART-to-UART or UART-to-I^2C interface.
14	RVDD	1.8V HDMI Receiver Input Power Supply. Bypass RVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to RVDD.
15	PLLVDD	3.3V PLL Power Supply. Bypass PLLVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to PLLVDD.
16	XVDD	3.3V Crystal Oscillator Power Supply. Bypass XVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to XVDD.
17	X1/OSC	Crystal/Oscillator Input. If crystal used, connect to one terminal of a 27MHz crystal..

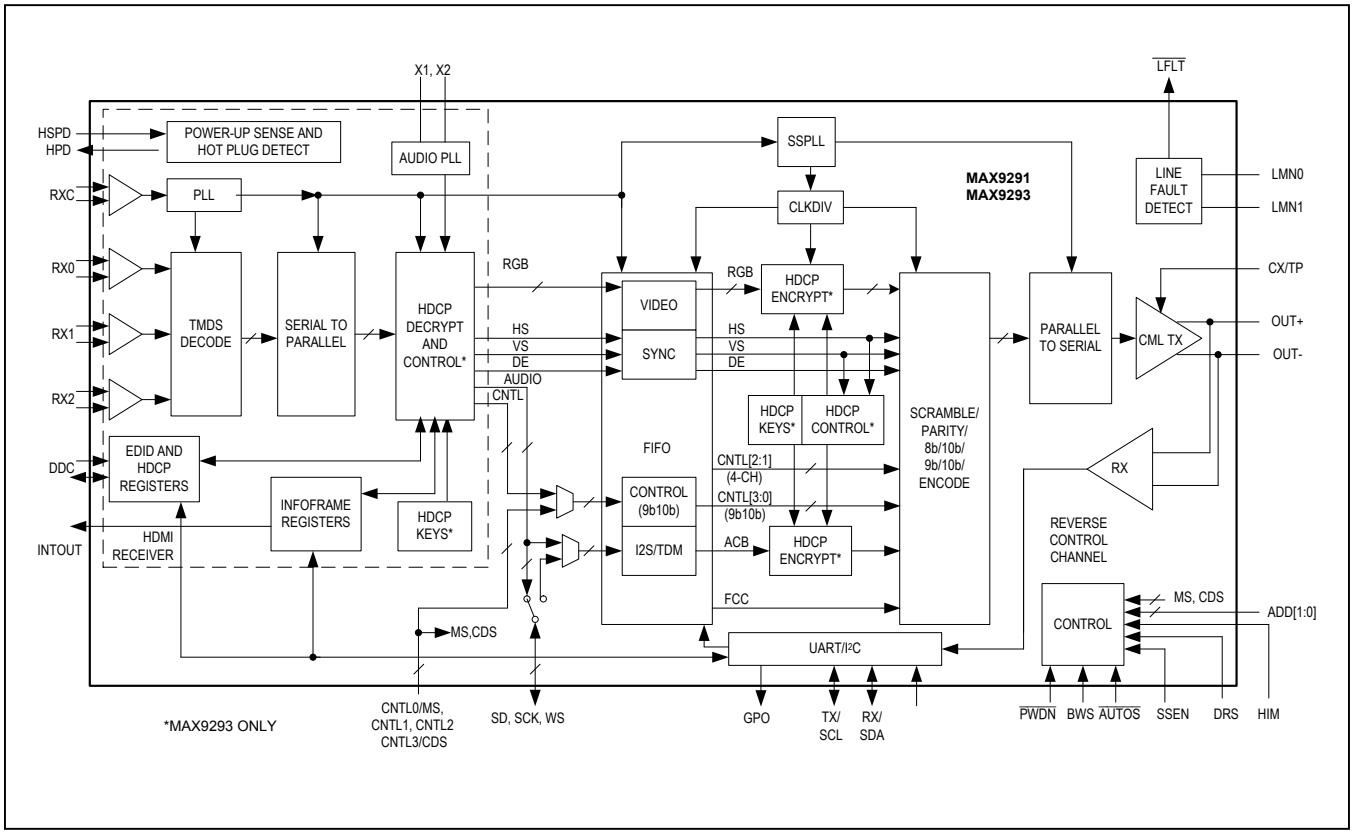
Pin Description (continued)

PIN	NAME	FUNCTION
18	X2	Crystal Input. Connect to one terminal of a 27MHz crystal.
19, 29, 45, 53	DVDD	1.8V Digital Power Supply. Bypass DVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
20	SD	I^2S/TDM Serial-Data Input/Output with Internal Pulldown to EP. Outputs HDMI audio data or accepts external audio data (encrypted when HDCP is enabled). Disable I^2S/TDM encoding to use SD as an additional control/data input valid on the selected edge of the pixel clock.
21	SCK	I^2S/TDM Serial-Clock Input/Output with Internal Pulldown to EP. Outputs HDMI audio bit clock data or accepts external audio bit clock.
22	WS	I^2S/TDM Word-Select Input/Output with Internal Pulldown to EP. Outputs HDMI audio word select clock or accepts external audio word select clock.
23	DDCSDA	DDC I^2C Serial-Data Input/Output with Internal 40kΩ Pullup to IOVDD. Used by the HDMI source to read the EDID.
24	DDCSCL	DDC I^2C Serial-Clock Input/Output with Internal 40kΩ Pullup to IOVDD. Used by the HDMI source to read the EDID.
25	CNTL1	Control Input with Internal Pulldown to EP. Input data is latched every PCLK cycle (Figure 15). CNTL1 or the HDMI control signal is mapped to internal bit DIN27/CNTL1. CNTL1 not encrypted when HDCP is on (MAX9293 only).
26	CNTL2	Control Input with Internal Pulldown to EP. Input data is latched every PCLK cycle (Figure 15). CNTL1 or the HDMI control signal is mapped to internal bit DIN28/CNTL2. CNTL2 not encrypted when HDCP is on (MAX9293 only).
27	INTOUT	A/V Status Register Interrupt Output. Indicates new data in the A/V status registers. INTOUT is reset when the A/V status registers are read.
28, 43	IOVDD	I/O Supply Voltage. 1.8V to 3.3V Logic I/O Power Supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.
30	RX/SDA	UART Receive/I^2C Serial Data Input/Output with Internal 40kΩ Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. RX/SDA has an open-drain driver and requires a pullup resistor. RX: Input of the serializer's UART. SDA: Data input/output of the serializer's I^2C master/slave.
31	TX/SCL	UART Transmit/I^2C Serial-Clock Input/Output with Internal 40kΩ Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. TX/SCL has an open-drain driver and requires a pullup resistor. TX: Output of the serializer's UART. SCL: Clock input/output of the serializer's I^2C master/slave.
32	N.C.	Not Connected. Not internally connected.
33	SSEN	Spread-Spectrum Enable Input with Internal Pulldown to EP. The state of SSEN latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set SSEN = high for ±0.5% spread spectrum on the serial link. Set SSEN = low to use the serial link without spread spectrum.
34	LMN1	Line-Fault Monitor Input 1 (see Figure 4 for details)
35	OUT-	Inverting Coax/Twisted-Pair Serial-Data Output
36	OUT+	Non-inverting Coax/Twisted-Pair Serial-Data Output

Pin Description (continued)

PIN	NAME	FUNCTION
37, 42, 54	AVDD	1.8V Analog Power Supply. Bypass AVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
38	LMN0	Line-Fault Monitor Input 0 (see Figure 4 for details)
39	$\overline{\text{LFLT}}$	Active-Low Open-Drain Line-Fault Output. $\overline{\text{LFLT}}$ has a 60kΩ internal pullup to IOVDD. $\overline{\text{LFLT}}$ = low indicates a line fault. $\overline{\text{LFLT}}$ is output high when $\overline{\text{PWDN}}$ = low.
40	GPO	General-Purpose Output. GPO is low after power-up or when $\overline{\text{PWDN}}$ is low. GPO follows the state of the GPI (or INT) input on the deserializer.
41	DRS	Data-Rate Select Input with Internal Pulldown to EP. Set DRS = low, to select high data-rate mode. Set DRS = high, to select low data-rate mode.
44	RSVD	Reserved. Connect to IOVDD.
46	ADD0	Three-Level Address Selection Input. The state of ADD0 latches at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 1 for details.
47	ADD1	Three-Level Address Selection Input. The state of ADD1 latches at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 1 for details.
48	BWS	Three-Level Bus-Width Select Input. Set BWS to the same level on both sides of the serial link. Set BWS = high for 32-bit mode. Set BWS = open for high-bandwidth mode. Do not set BWS = low.
49	$\overline{\text{PWDN}}$	Active-Low, Power-Down Input with Internal Pulldown to EP. Set $\overline{\text{PWDN}}$ low to enter power-down mode to reduce power consumption.
50	CDS	Control Direction Selection with Internal Pulldown to EP. Set CDS = low when the control-channel master µC is connected to the MAX9291/MAX9293. Set CDS = high when the control-channel master µC is connected to the deserializer.
51	MS	Mode Select input with Internal Pulldown to EP. Set MS = low, to select base mode. MS sets the control-link (see the *Control Channel and Register Programming* section).
52	$\overline{\text{AUTOS}}$	Active-Low Auto-Start Input With Internal Pulldown to GND. Set $\overline{\text{AUTOS}}$ = high, to disable serialization at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). Set $\overline{\text{AUTOS}}$ = low, to enable serialization and automatic PLL range selection power-up or when resuming from power-down mode.
55	HIM	High-Immunity Mode Input. Default HIGHIMM bit value is latched at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low) and is active-high. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the deserializer must be set to the same value.
56	CX/TP	Coax/Twisted-Pair Input with Internal Pulldown to GND. Set CX/TP low for twisted-pair cable drive (differential output). Set CX/TP high for coax cable drive (single-ended output).
—	EP	Exposed Pad. EP is internally connected to device ground. EP **must** be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagram



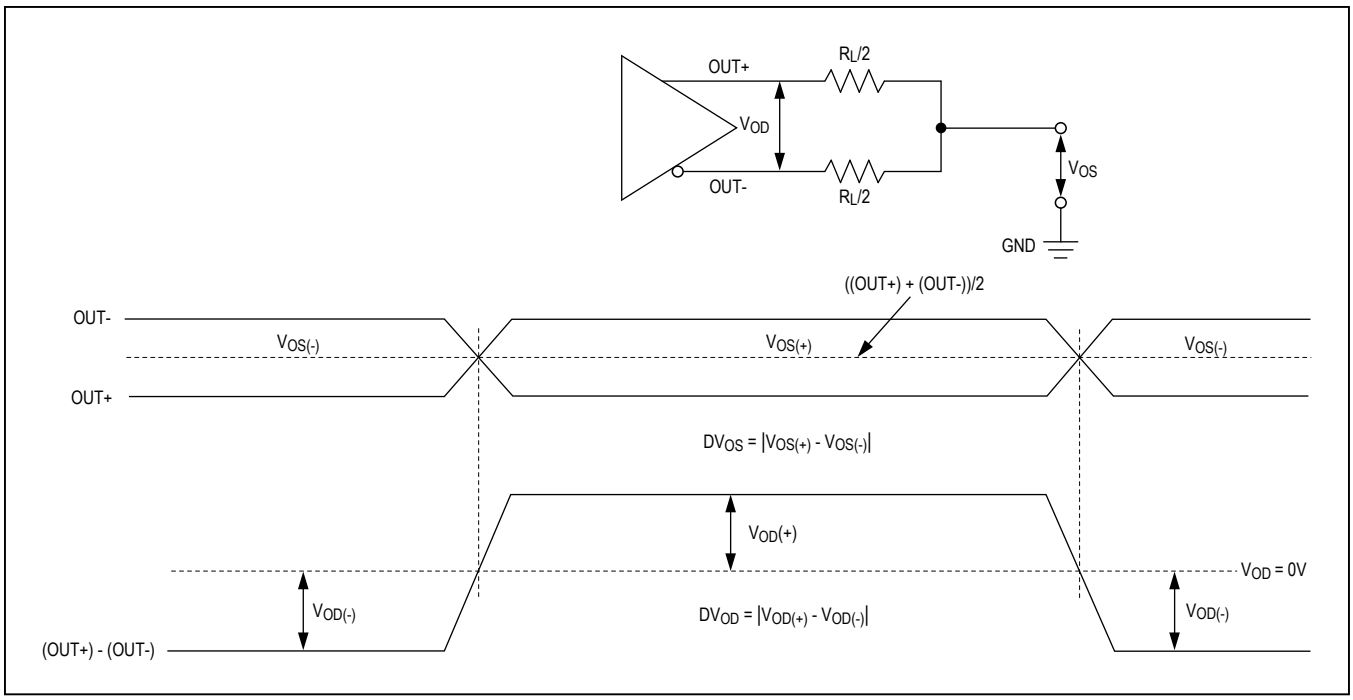


Figure 1. Serial Output Parameters

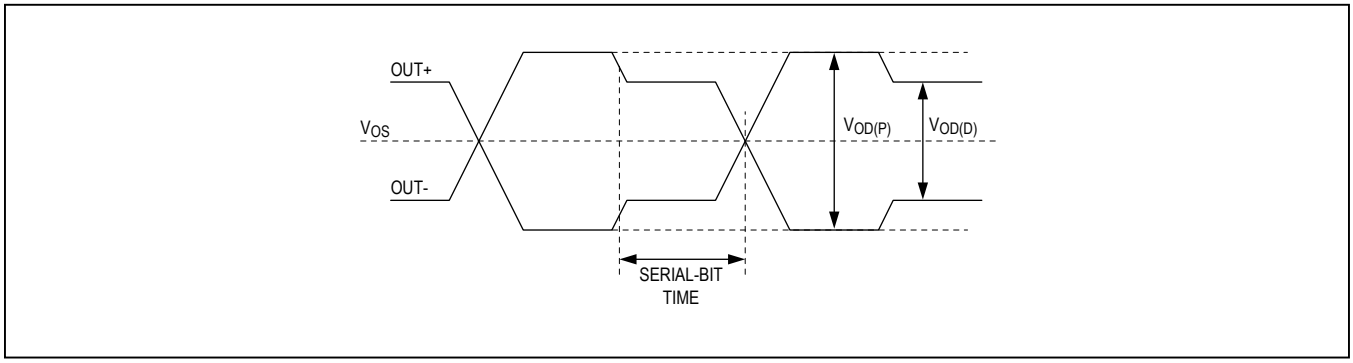


Figure 2. Output Waveforms at OUT+, OUT-

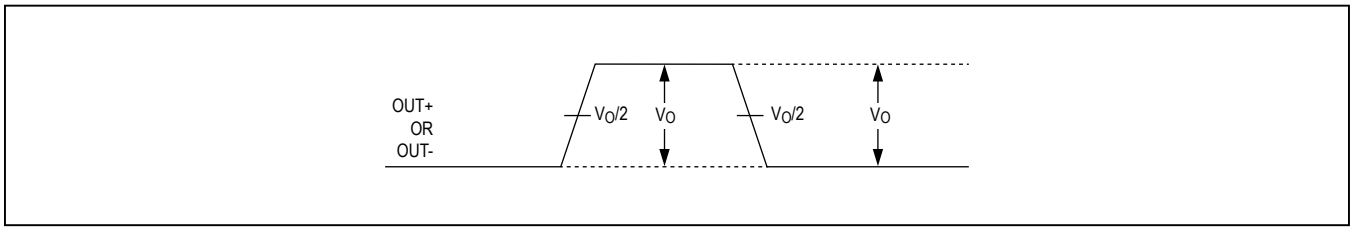


Figure 3. Single-Ended Output Template

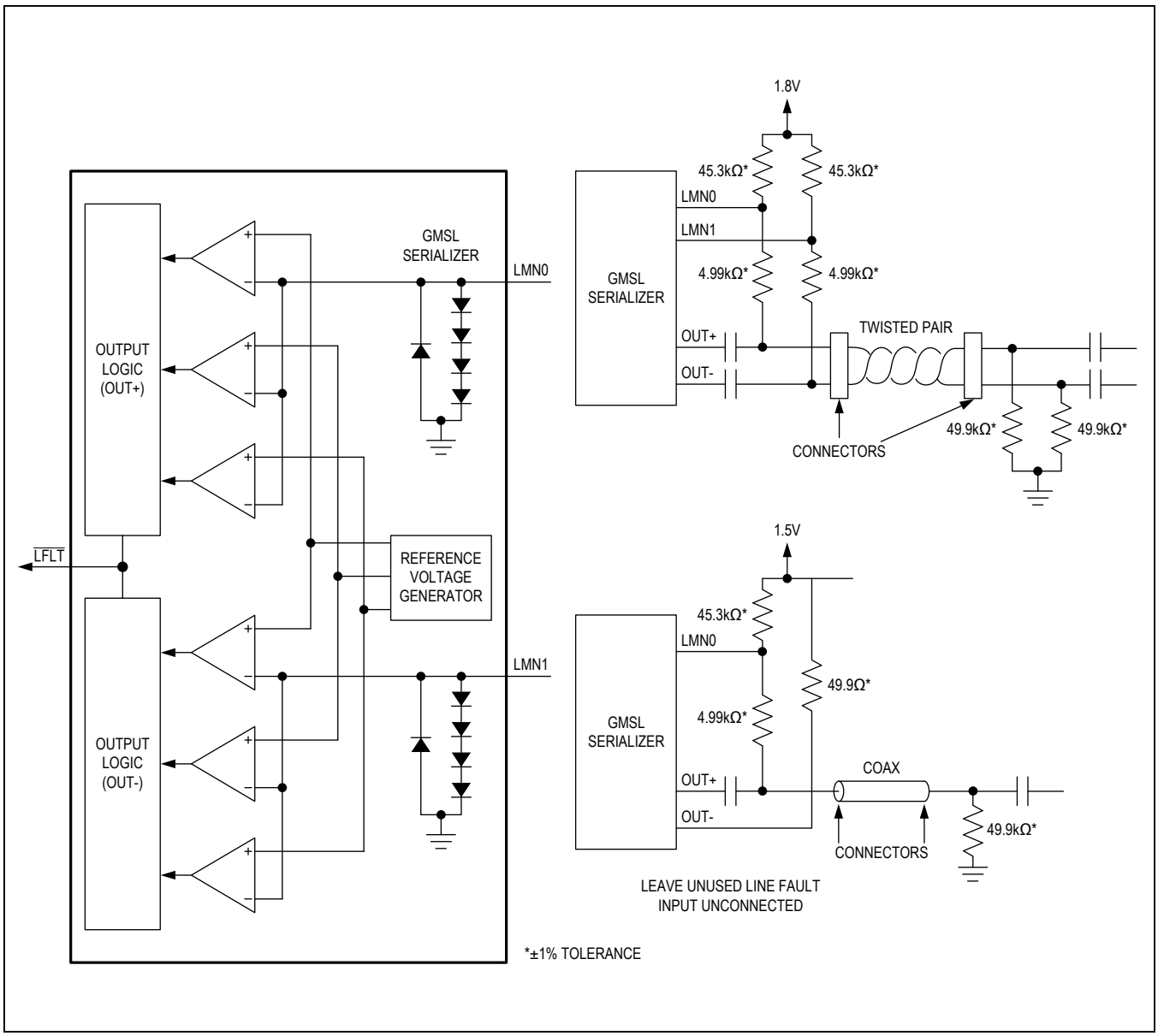


Figure 4. Line-Fault Detector Circuit

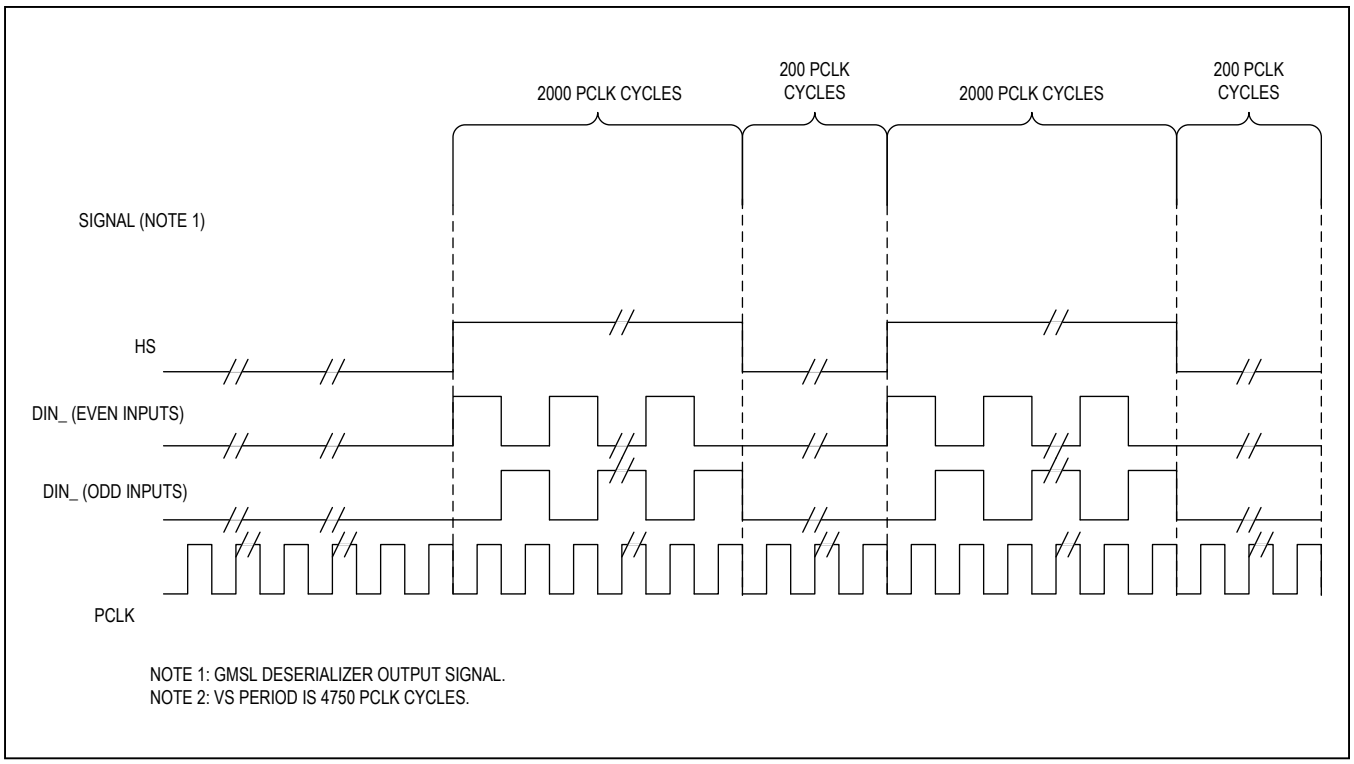


Figure 5. Worst-Case Pattern Input

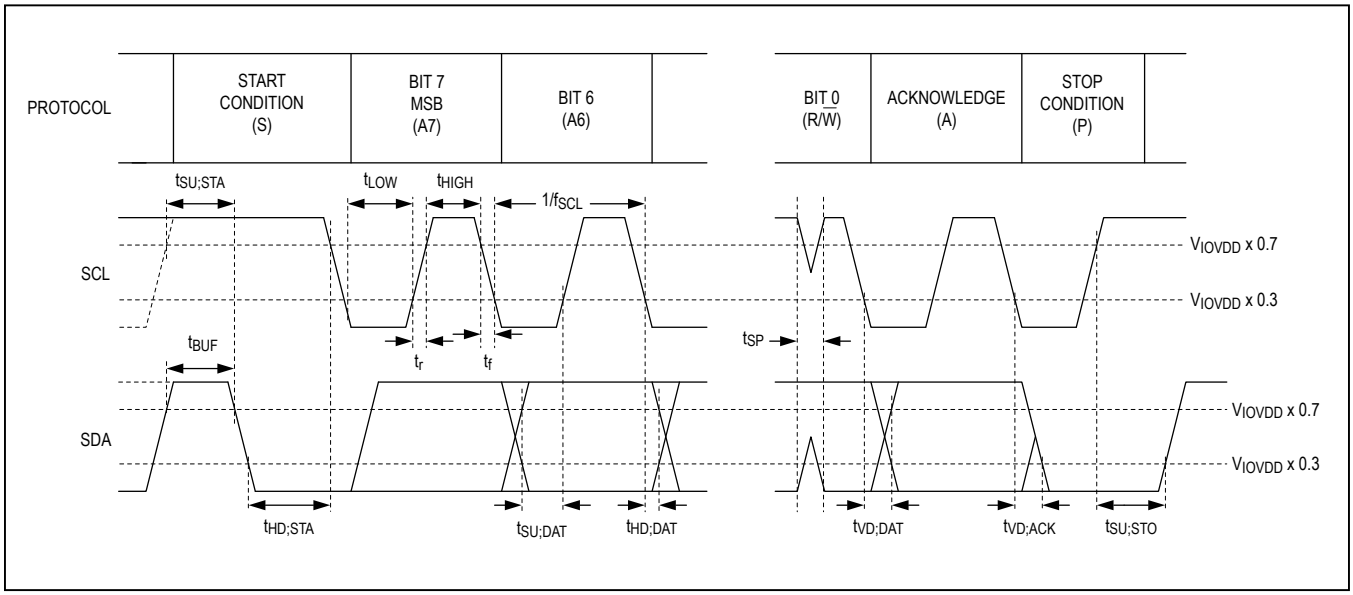


Figure 6. I^2C Timing Parameters

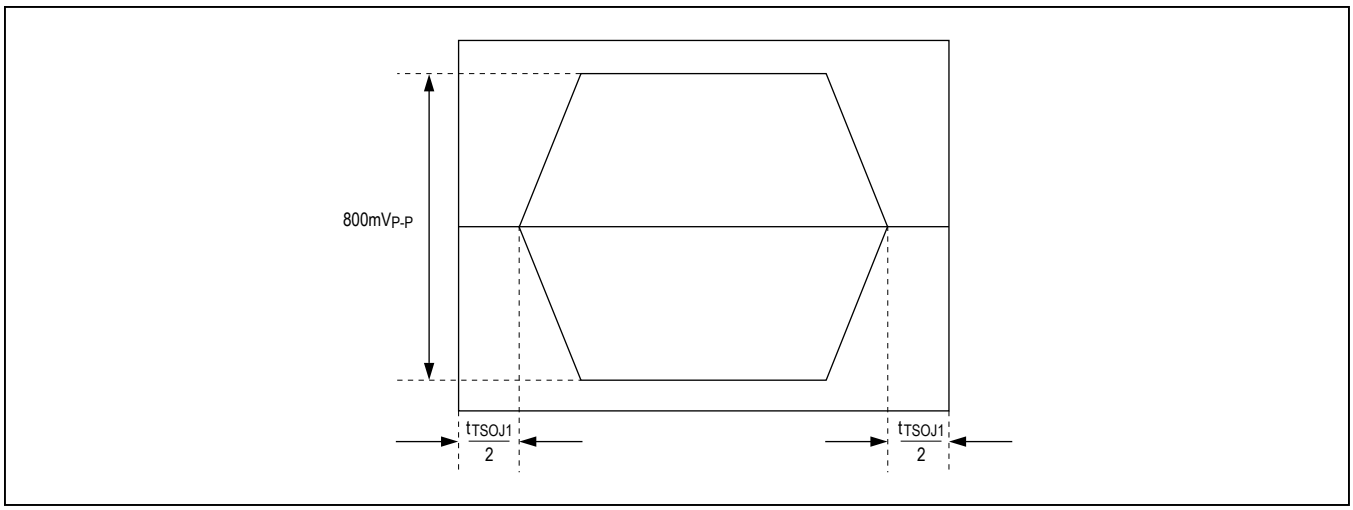


Figure 7. Differential Output Template

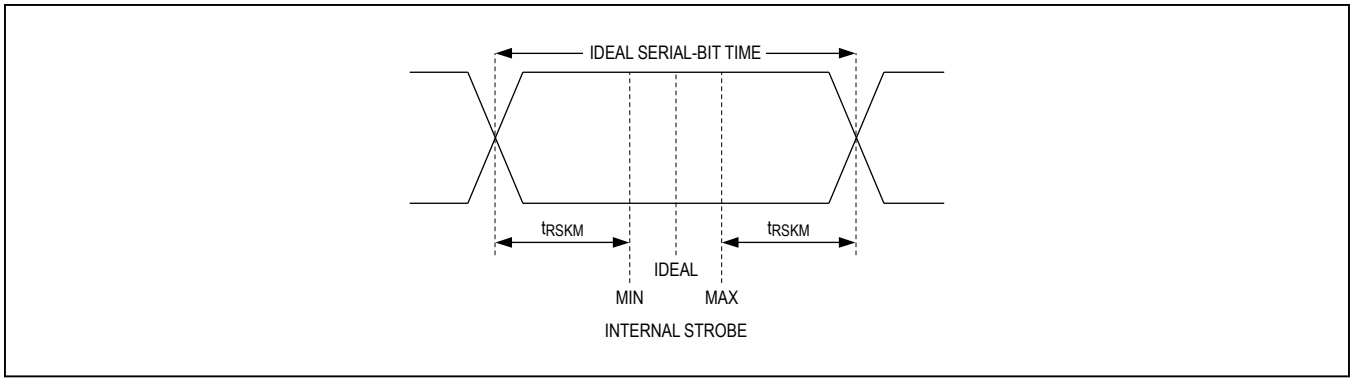


Figure 8. HDMI Receiver Input Skew Margin

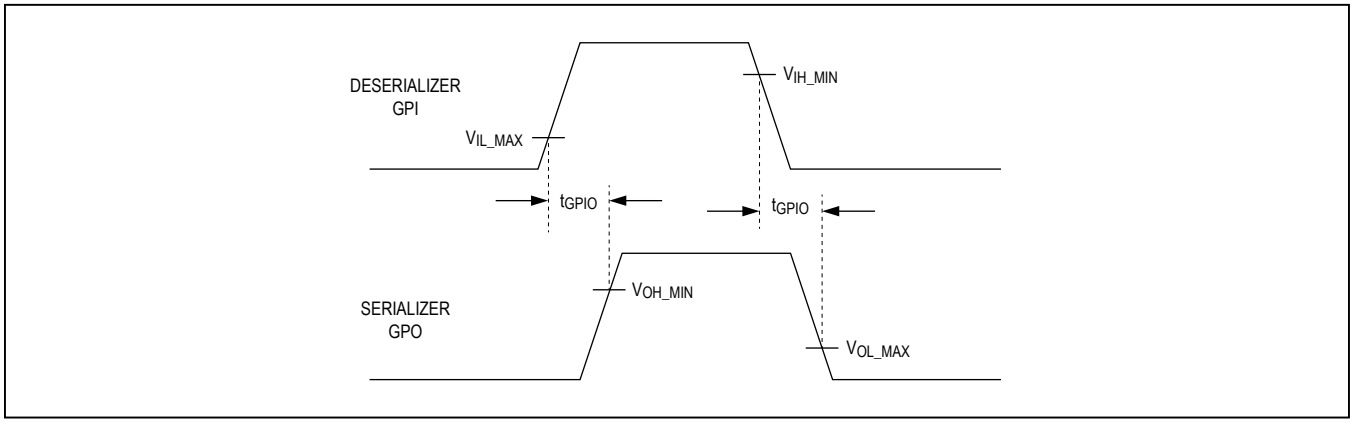


Figure 9. GPI-to-GPO Delay

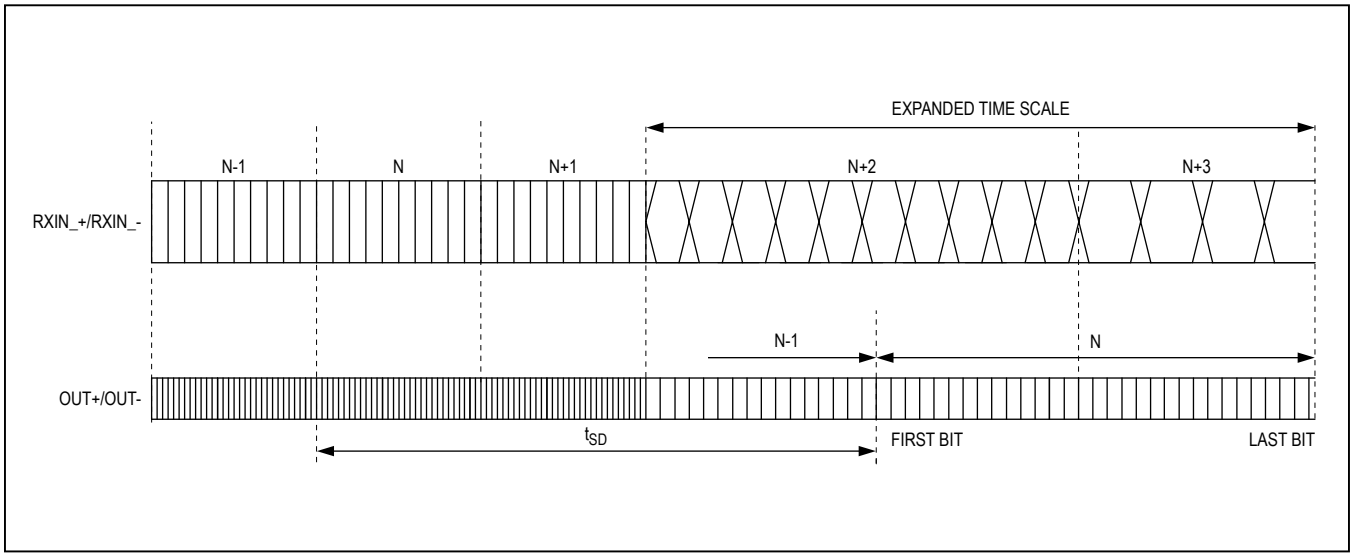


Figure 10. Serializer Delay

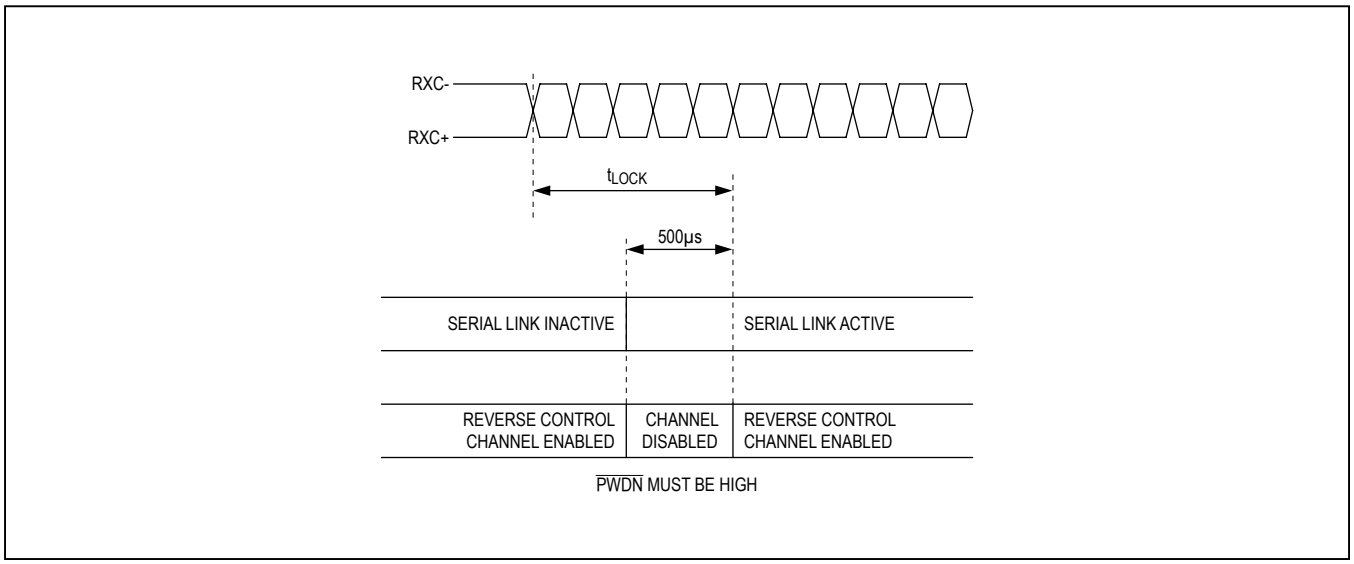


Figure 11. Link Startup Time

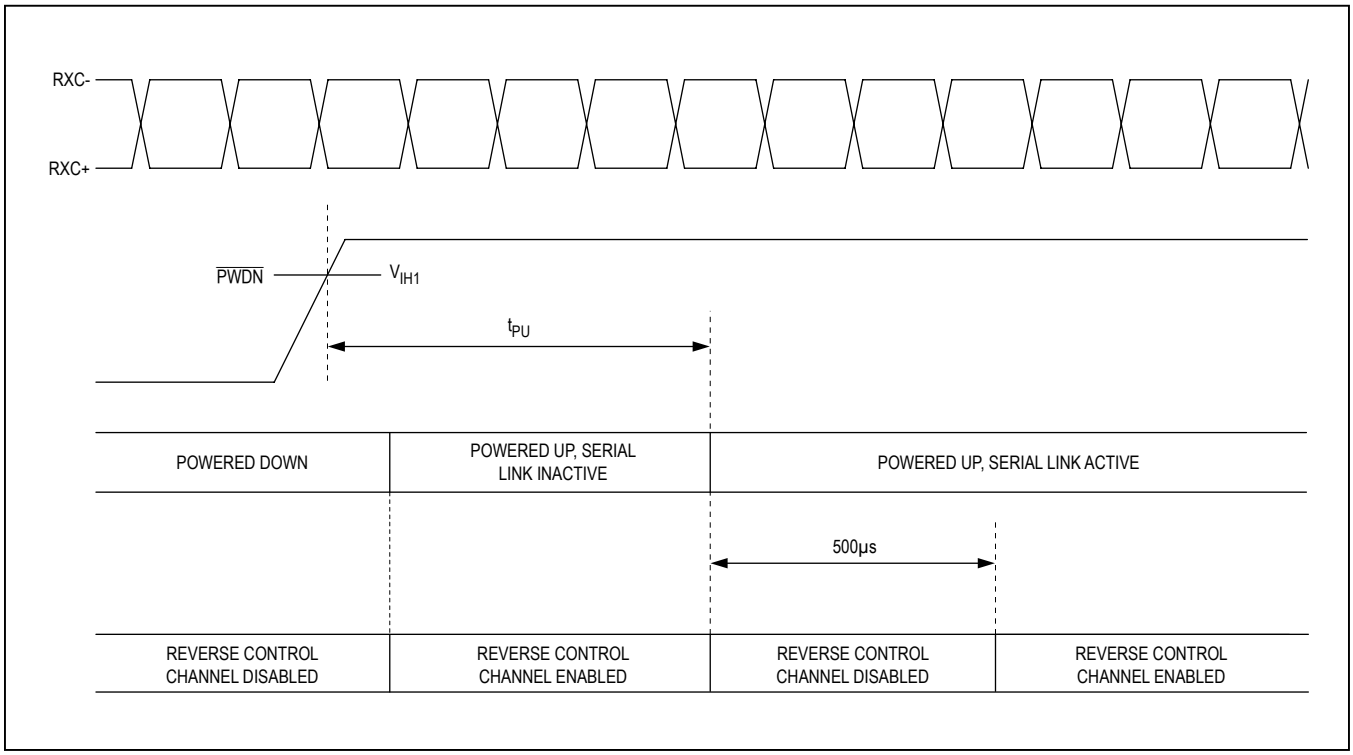


Figure 12. Power-Up Delay

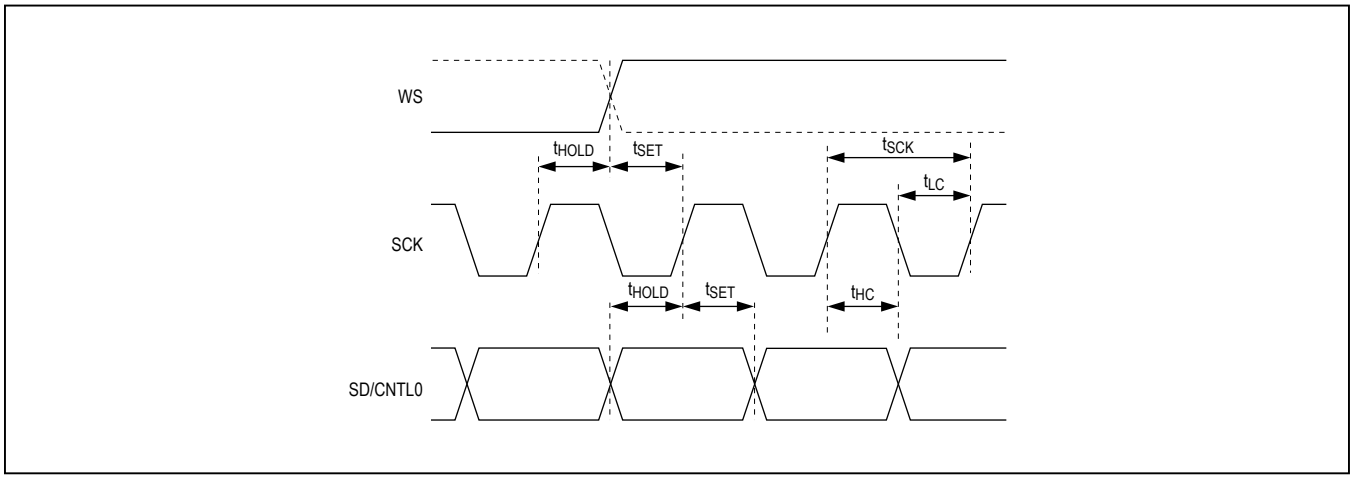


Figure 13. Input I^2S Timing Parameters

Detailed Description

The MAX9291/MAX9293 serializers, when paired with the MAX9276/MAX9280 deserializers, provide the full set of operating features, but is backward compatible with the MAX9249–MAX9270 family of Gigabit multimedia serial link (GMSL) devices, and has basic functionality when paired with any GMSL device. The MAX9293 has high-bandwidth digital content protection (HDCP), while the MAX9291 does not.

The serializers have a maximum serial-bit rate of 3.12Gbps for up to 15m of cable and operate up to a maximum output clock of 104MHz in 27-bit high-bandwidth mode, or 78MHz in 32-bit mode. This bit rate and output flexibility support a wide range of displays, from QVGA (320 x 240) to 1920 x 720 and higher with 24-bit color, as well as megapixel image sensors. An encoded audio channel supports L-PCM I2S stereo and up to 8 channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth from 8 to 32 bits. Output pre/deemphasis, combined with GMSL deserializer equalization, extends the cable length and enhances link reliability.

The control channel enables a µC to program the serializer and deserializer registers and program registers on peripherals. The control channel is also used to perform HDCP functions (MAX9281 only). The µC can be located at either end of the link, or when using two µCs, at both ends. Two modes of control-channel operation are available. Base mode uses either I2C or GMSL UART protocol, while bypass mode uses a user-defined UART protocol. UART protocol allows full-duplex communication, while I2C allows half-duplex communication.

Spread spectrum is available to reduce EMI on the serial output. The serial output and HDMI input complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

Registers set the operating conditions of the serializers and are programmed using the control channel in base mode. The MAX9291/MAX9293 hold their own device address and the device address of the deserializer it is paired with. Similarly, the deserializer holds its own device address and the address of the MAX9291/MAX9293. Whenever a device address is changed be sure to write the new address to both devices. The default device address of the deserializer is set by the ADD[1:0] inputs (see Table 1). Registers 0x00 and 0x01 hold the device addresses.

Table 1. Device Address Defaults (Register 0x00, 0x01)

PIN		DEVICE ADDRESS (BIN)								SERIALIZER DEVICE ADDRESS (HEX)	DESERIALIZER DEVICE ADDRESS (HEX)
ADD1	ADD0	D7	D6	D5	D4	D3	D2	D1	D0		
Low	Low	1	0	0	X*	0	0	0	R/$\overline{W}$	80	90
Low	High	1	0	0	X*	0	1	0	R/$\overline{W}$	84	94
Low	Open	1	0	0	X*	1	0	0	R/$\overline{W}$	88	98
High	Low	1	1	0	X*	0	0	0	R/$\overline{W}$	C0	D0
High	High	1	1	0	X*	0	1	0	R/$\overline{W}$	C4	D4
High	Open	1	1	0	X*	1	0	0	R/$\overline{W}$	C8	D8
Open	Low	0	1	0	X*	0	0	0	R/$\overline{W}$	40	50
Open	High	0	1	0	X*	0	1	0	R/$\overline{W}$	44	54
Open	Open	0	1	0	X*	1	0	0	R/$\overline{W}$	48	58

**X = 0 for the serializer address, X = 1 for the deserializer address.*

GMSL Input Bit Map

The input bit width depends on settings of the bus width (BWS) pin. Table 2 lists the bit map.

Serial Link Signaling and Data Format

The serializer uses differential CML signaling to drive twisted-pair cable and single-ended CML to drive coaxial cable with programmable pre/deemphasis and AC-coupling. The deserializer uses AC-coupling and programmable channel equalization.

Input data is scrambled and then 8b/10b coded (9b/10b in high-bandwidth mode). The deserializer recovers the embedded serial clock, then samples, decodes, and descrambles the data. In 32-bit mode, the first 29 bits contain video data. In high-bandwidth mode, the first 24 bits contain video data, or special control signal packets. The last 3 bits contain the embedded audio channel, the embedded forward control channel, and the parity bit of the serial word (see Figure 14 and Figure 15).

Table 2. GMSL Equivalent Input Map

SIGNAL	INPUT PIN/BIT POSITION	HIGH-BANDWIDTH MODE (BWS = MID)	32-BIT MODE (BWS = HIGH)
R[5:0]	DIN[5:0]	Used	Used
G[5:0]	DIN [11:6]	Used	Used
B[5:0]	DIN [17:12]	Used	Used
HS, VS, DE	DIN18/HS, DIN19/VS, DIN20/DE	Used*	Used*
R[7:6]	DIN [22:21]	Used	Used
G[7:6]	DIN [24:23]	Used	Used
B[7:6]	DIN [26:25]	Used	Used
CNTL[2:1]	CNTL[2:1]	Used*/**	Used*
CNTL3, CNTL0	CNTL3, CNTL0	Used*/**	Not used
I^2S/TDM	WS, SCK, SD	Used	Used
AUX SIGNAL		Used	Used

*Not encrypted when HDCP is enabled (MAX9293 only).
***See the High-Bandwidth Mode section for details on timing requirements.*

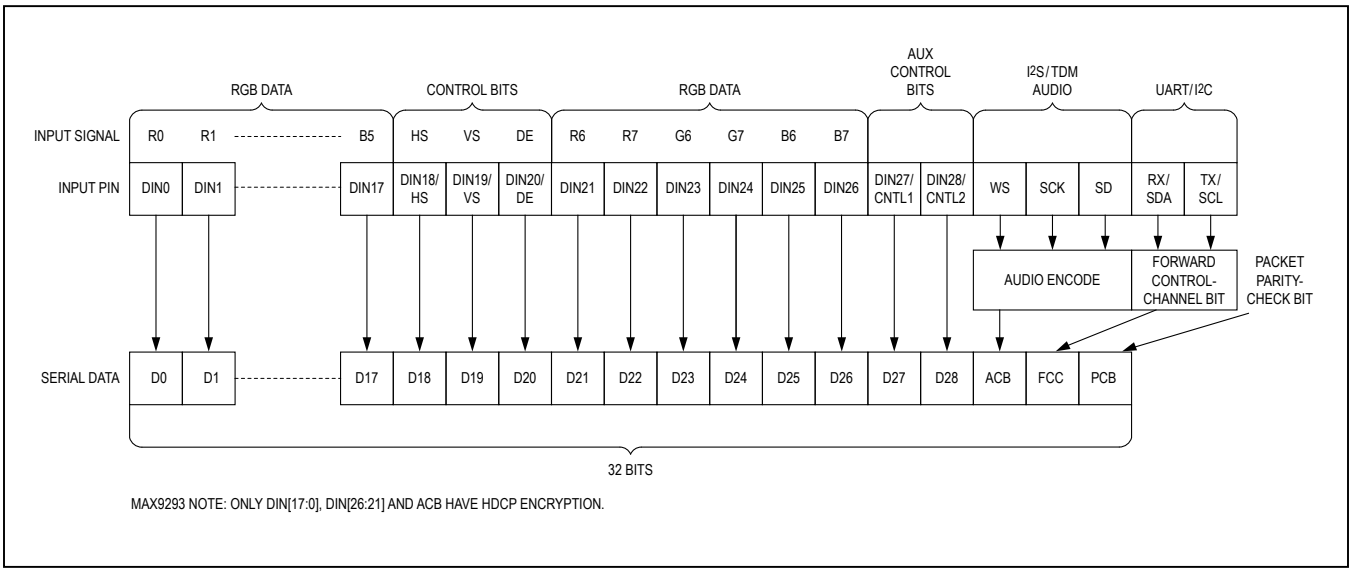


Figure 14. 32-Bit Mode Serial Data Format

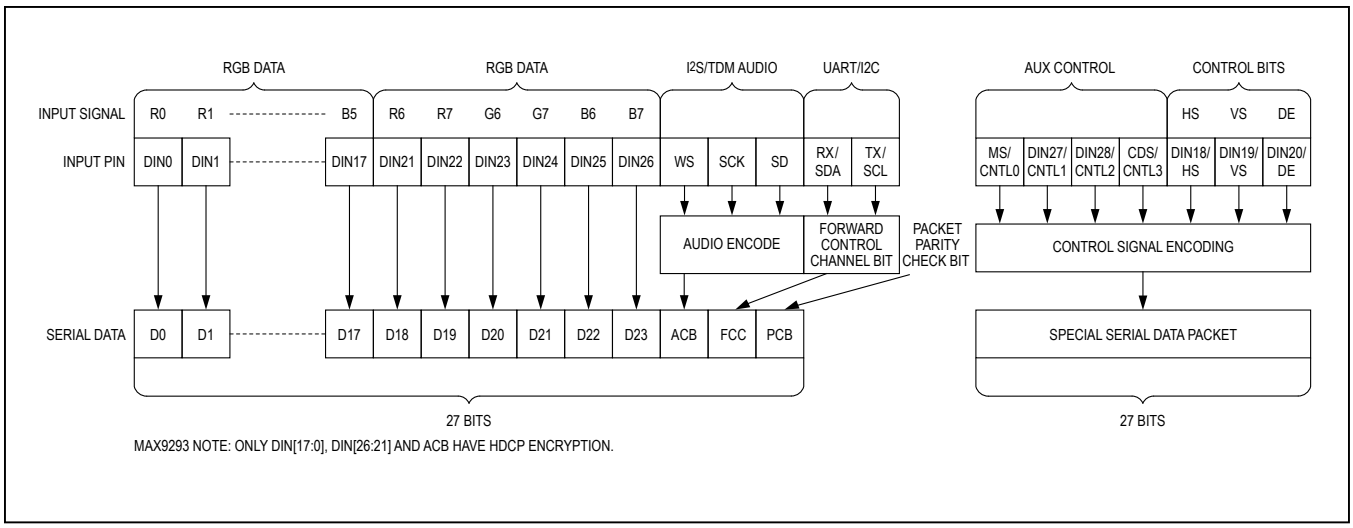


Figure 15. High-Bandwidth Mode Serial Data Format

Table 3. Data-Rate Selection Table

DRS BIT SETTING	BWS PIN SETTING	HDMI OUTPUT FREQUENCY RANGE* (MHZ)
0 (high data rate)	Mid (high bandwidth mode)	36.66 to 104
	High (32-bit mode)	12.5 to 78
1 (low data rate)	Mid	18.33 to 36.66
	High	6.25 to 12.5

**HDMI output frequency can be 1x, 1/2x, or 1/4x the RXC_ clock frequency.*

Data-Rate Selection

The RXC_ clock frequency is specified to be ≥ 25MHz, however, pixel repetition could divide the HDMI receiver output frequency up to a factor of four. Set the DRS bit, and BWS input according to the HDMI output frequency range (Table 3). Set DRS = 1 for low data rate RXC_ frequency range. Set DRS = 0 for high data rate output frequency range.

High-Bandwidth Mode

Each serializer uses a 27-bit high-bandwidth mode to support 24-bit RGB at 104MHz pixel clock. Set BWS = open in both the serializer and deserializer to use high-bandwidth mode. In high-bandwidth mode, the serializer encodes HS, VS, DE, and CNTL[3:0] to special packets. Packets are sent by replacing a pixel before the rising edge and after the falling edge of HS, VS, DE signals. However, for CNTL[3:0], packets always replace a pixel before the transition of CNTL[3:0]. Keep HS, VS, and DE low pulse widths at least two pixel clock cycles. By default, CNTL[3:0] are sampled continuously when DE is low. CNTL[3:0] are sampled only on HS/VS transitions when DE is high. If DE triggering of encoded packets is not desired, set the serializer's DISDETRIG = 0 and the CNTLTRIG bits to their desired value (register 0x15) to change the CNTL triggering behavior. Set DETREN = 0 on the deserializer when DE is not periodic.

Video Bit Mapping

HDMI video data is mapped to the equivalent input bits shown in Table 4.

Table 4. RGB/YUV Input Map

GMSL INPUT BITS[1]	RGB888		YCBCR444		YCBCR422 SELVESA = 0[3]
	SELVESA = 1 (VESA)	SELVESA = 0 (oLDI[2])	SELVESA = 1 (VESA)	SELVESA = 0 (oLDI[2])	
DIN[0]	R[0]	R[2]	CR[0]	CR[2]	Cb/Cr [0]
DIN[1]	R[1]	R[3]	CR[1]	CR[3]	Cb/Cr [1]
DIN[2]	R[2]	R[4]	CR[2]	CR[4]	Cb/Cr [2]
DIN[3]	R[3]	R[5]	CR[3]	CR[5]	Cb/Cr [3]
DIN[4]	R[4]	R[6]	CR[4]	CR[6]	Cb/Cr [4]
DIN[5]	R[5]	R[7]	CR[5]	CR[7]	Cb/Cr [5]
DIN[6]	G[0]	G[2]	Y[0]	Y[2]	Cb/Cr [6]
DIN[7]	G[1]	G[3]	Y[1]	Y[3]	Cb/Cr [7]
DIN[8]	G[2]	G[4]	Y[2]	Y[4]	Y[0]
DIN[9]	G[3]	G[5]	Y[3]	Y[5]	Y[1]
DIN[10]	G[4]	G[6]	Y[4]	Y[6]	Y[2]
DIN[11]	G[5]	G[7]	Y[5]	Y[7]	Y[3]
DIN[12]	B[0]	B[2]	CB[0]	CB[2]	Y[4]
DIN[13]	B[1]	B[3]	CB[1]	CB[3]	Y[5]
DIN[14]	B[2]	B[4]	CB[2]	CB[4]	Y[6]
DIN[15]	B[3]	B[5]	CB[3]	CB[5]	Y[7]
DIN[16]	B[4]	B[6]	CB[4]	CB[6]	—
DIN[17]	B[5]	B[7]	CB[5]	CB[7]	—
DIN[18]	HS	HS	HS	HS	HS
DIN[19]	VS	VS	VS	VS	VS
DIN[20]	DE	DE	DE	DE	DE
DIN[21]	R[6]	R[0]	CR[6]	CR[0]	—
DIN[22]	R[7]	R[1]	CR[7]	CR[1]	—
DIN[23]	G[6]	G[0]	Y[6]	Y[0]	—
DIN[24]	G[7]	G[1]	Y[7]	Y[1]	—
DIN[25]	B[6]	B[0]	CB[6]	CB[0]	—
DIN[26]	B[7]	B[1]	CB[7]	CB[1]	—

Note 1: Equivalent GMSL input bit. Refer to the MAX9276/MAX9280 IC data sheet for details.
Note 2: oLDI bit weights shown. oLDI bit names remain the same as SELVESA = 1.
Note 3: Do not use SELVESA = 1.

Audio Channel

The audio channel supports 8kHz to 192kHz audio sampling rates and audio word lengths from 8 bits to 32 bits (2-channel I2S) or 64 to 256 bits (TDM64 to TDM256). The audio bit clock (SCK) does not have to be synchronized with RXC_. The serializer automatically encodes audio data into a single bit stream synchronous with RXC_. The deserializer decodes the audio stream and stores audio words in a FIFO. Audio rate detection uses an internal oscillator to continuously determine the audio data rate and output the audio in I2S format. For audio output on the I2S/TDM pins, WS and SCK clocks can be driven by the audio source or sink. The audio channel is enabled by default. When the audio channel is disabled, SD is treated as an auxiliary control signal.

Since the audio data sent through the serial link is synchronized with RXC_, low RXC_ frequencies limit the maximum audio sampling rate. Table 5 lists the maximum audio sampling rate for various RXC_ frequencies. Spread-spectrum settings do not affect the I2S/TDM data rate or WS clock frequency.

Table 5. Maximum Audio WS Frequency (kHz) for Various RXC_ Frequencies

CHANNELS	BITS PER CHANNEL	RXC_ FREQUENCY (DRS = 0*) (MHZ)										
		12.5	15.0	16.6	20.0	25.0	30.0	35.0	40.0	45.0	50.0	100
2	8	+	+	+	+	+	+	+	+	+	+	+
	16	+	+	+	+	+	+	+	+	+	+	+
	18	185.5	+	+	+	+	+	+	+	+	+	+
	20	174.6	+	+	+	+	+	+	+	+	+	+
	24	152.2	182.7	+	+	+	+	+	+	+	+	+
	32	123.7	148.4	164.3	+	+	+	+	+	+	+	+
4	8	+	+	+	+	+	+	+	+	+	+	+
	16	123.7	148.4	164.3	+	+	+	+	+	+	+	+
	18	112.0	134.4	148.8	179.2	+	+	+	+	+	+	+
	20	104.2	125.0	138.3	166.7	+	+	+	+	+	+	+
	24	88.6	106.3	117.7	141.8	177.2	+	+	+	+	+	+
	32	69.9	83.8	92.8	111.8	139.7	167.6	+	+	+	+	+
6	8	152.2	182.7	+	+	+	+	+	+	+	+	+
	16	88.6	106.3	117.7	141.8	177.2	+	+	+	+	+	+
	18	80.2	93.3	106.6	128.4	160.5	+	+	+	+	+	+
	20	73.3	88.0	97.3	117.3	146.6	175.9	+	+	+	+	+
	24	62.5	75.0	83.0	100	125	150	175	+	+	+	+
	32	48.3	57.9	64.1	77.2	96.5	115.9	135.2	154.5	173.8	+	+
8	8	123.7	148.4	164.3	+	+	+	+	+	+	+	+
	16	69.9	83.8	92.8	111.8	139.7	167.6	+	+	+	+	+
	18	62.5	75.0	83.0	100.0	125.0	150.0	175.0	+	+	+	+
	20	57.1	68.5	75.8	91.3	114.2	137.0	159.9	182.7	+	+	+
	24	48.3	57.9	64.1	77.2	96.5	115.9	135.2	154.5	173.8	+	+
	32	37.1	44.5	49.3	59.4	74.2	89.1	103.9	118.8	133.6	148.4	+

COLOR CODING
< 48kHz
48kHz to 96kHz
96kHz to 192kHz
> 192kHz

**DRS = 0 RXC_ frequency is equal to 2x the DRS = 1 RXC_ frequency.*

+Max WS rate is greater than 192kHz.

Audio Channel from HDMI

Audio from the HDMI source can be output from the serializer, deserializer, or both. When the device uses the HDMI audio source, the output formats are the same as the HDMI source.

Audio from the HDMI source is stored in a FIFO and clocked out by a master clock. The master clock is generated by an audio PLL. The audio PLL uses N and CTS values from the HDMI source, calculated from a crystal reference and the TMDS pixel clock, to stay synchronized with the HDMI source.

Audio infoframes describe the audio characteristics for the next video frame. When a new audio infoframe arrives, an interrupt is generated on INTOUT. The link µC responds and writes relevant infoframe data to remote registers in the deserializer, SoC or audio packet header.

Audio in one of four formats is output at the I²S/TDM pins of the MAX9291/MAX9293, the deserializer, or both. Format selection is based on sink capability and preferences indicated in the EDID and on the audio available at the source. The audio formats are:

Format 1: 2-channel (stereo) I²S

Format 2: 8-channel TDM

Format 3: 8-channel TDM with packet header and packed 16-bit samples

Format 4: 8-channel TDM with packet header and packed 24-bit samples

HDMI TDM Audio Channel Allocation

HDMI TDM channel content is assigned according to channel allocation data received in audio infoframes. Table 7 shows the CEA-861-E mapping of channel allocation data to TDM channels. If more than one speaker channel can be mapped to a TDM channel, the EDID tells the HDMI source which speaker channel to send.

HDMI Audio Infoframe Data Used in the Packet Header

Infoframe data relevant to audio packet header generation is shown in Table 6.

The HDMI controller should offer channel allocation according to CEA-861-E (specified by HDMI 1.4). The controller should have an automatic channel mapping option, which changes the audio output whenever the audio infoframe changes. If it does, the default should be “automatic.”

Table 6. Packet Header Infoframe

BITS	NAME	VALUE	FUNCTION
D15	DATA_VALID	0	Samples in the packet are not valid
		1	Samples in the packet are valid
D14	STREAM_MODULATION	0	Compressed modulation
		1	LPCM modulation
D[13:12]	SAMPLE_RATE	00	32kHz sample rate
		01	44.1kHz sample rate
		10	48kHz sample rate
		11	Reserved
D11	SAMPLE_SIZE	0	16-bit sample size
		1	24-bit sample size
D[10:8]	—	—	Reserved
D[7:0]	CHANNEL_ALLOCATION	—	Indicates which samples in the TDM packet are active (Table 7)

Table 7. Channel Allocation

CA (BIN)								CA (HEX)	CHANNEL NUMBER							
D7	D6	D5	D4	D3	D2	D1	D0		8	7	6	5	4	3	2	1
0	0	0	0	0	0	0	0	0x00	—	—	—	—	—	—	FR	FL
0	0	0	0	0	0	0	1	0x01	—	—	—	—	—	LFE	FR	FL
0	0	0	0	0	0	1	0	0x02	—	—	—	—	FC	—	FR	FL
0	0	0	0	0	0	1	1	0x03	—	—	—	—	FC	LFE	FR	FL
0	0	0	0	0	1	0	0	0x04	—	—	—	RC	—	—	FR	FL
0	0	0	0	0	1	0	1	0x05	—	—	—	RC	—	LFE	FR	FL
0	0	0	0	0	1	1	0	0x06	—	—	—	RC	FC	—	FR	FL
0	0	0	0	0	1	1	1	0x07	—	—	—	RC	FC	LFE	FR	FL
0	0	0	0	1	0	0	0	0x08	—	—	RR	RL	—	—	FR	FL
0	0	0	0	1	0	0	1	0x09	—	—	RR	RL	—	LFE	FR	FL
0	0	0	0	1	0	1	0	0x0A	—	—	RR	RL	FC	—	FR	FL
0	0	0	0	1	0	1	1	0x0B	—	—	RR	RL	FC	LFE	FR	FL
0	0	0	0	1	1	0	0	0x0C	—	RC	RR	RL	—	—	FR	FL
0	0	0	0	1	1	0	1	0x0D	—	RC	RR	RL	—	LFE	FR	FL
0	0	0	0	1	1	1	0	0x0E	—	RC	RR	RL	FC	-	FR	FL
0	0	0	0	1	1	1	1	0x0F	—	RC	RR	RL	FC	LFE	FR	FL
0	0	0	1	0	0	0	0	0x10	RRC	RLC	RR	RL	—	—	FR	FL
0	0	0	1	0	0	0	1	0x11	RRC	RLC	RR	RL	—	LFE	FR	FL
0	0	0	1	0	0	1	0	0x12	RRC	RLC	RR	RL	FC	—	FR	FL
0	0	0	1	0	0	1	1	0x13	RRC	RLC	RR	RL	FC	LFE	FR	FL
0	0	0	1	0	1	0	0	0x14	FRC	FLC	—	—	—	—	FR	FL
0	0	0	1	0	1	0	1	0x15	FRC	FLC	—	—	—	LFE	FR	FL
0	0	0	1	0	1	1	0	0x16	FRC	FLC	—	—	FC	-	FR	FL
0	0	0	1	0	1	1	1	0x17	FRC	FLC	—	—	FC	LFE	FR	FL
0	0	0	1	1	0	0	0	0x18	FRC	FLC	—	RC	—	—	FR	FL
0	0	0	1	1	0	0	1	0x19	FRC	FLC	—	RC	—	LFE	FR	FL
0	0	0	1	1	0	1	0	0x1A	FRC	FLC	—	RC	FC	—	FR	FL
0	0	0	1	1	0	1	1	0x1B	FRC	FLC	—	RC	FC	LFE	FR	FL
0	0	0	1	1	1	0	0	0x1C	FRC	FLC	RR	RL	—	—	FR	FL
0	0	0	1	1	1	0	1	0x1D	FRC	FLC	RR	RL	—	LFE	FR	FL
0	0	0	1	1	1	1	0	0x1E	FRC	FLC	RR	RL	FC	—	FR	FL
0	0	0	1	1	1	1	1	0x1F	FRC	FLC	RR	RL	FC	LFE	FR	FL
0	0	1	0	0	0	0	0	0x20	—	FCH	RR	RL	FC	—	FR	FL
0	0	1	0	0	0	0	1	0x21	—	FCH	RR	RL	FC	LFE	FR	FL

Table 7. Channel Allocation (continued)

CA (BIN)								CA (HEX)	CHANNEL NUMBER							
D7	D6	D5	D4	D3	D2	D1	D0		8	7	6	5	4	3	2	1
0	0	1	0	0	0	1	0	0x22	TC	—	RR	RL	FC	—	FR	FL
0	0	1	0	0	0	1	1	0x23	TC	—	RR	RL	FC	LFE	FR	FL
0	0	1	0	0	1	0	0	0x24	FRH	FLH	RR	RL	—	—	FR	FL
0	0	1	0	0	1	0	1	0x25	FRH	FLH	RR	RL	—	LFE	FR	FL
0	0	1	0	0	1	1	0	0x26	FRW	FLW	RR	RL	—	-	FR	FL
0	0	1	0	0	1	1	1	0x27	FRW	FLW	RR	RL	—	LFE	FR	FL
0	0	1	0	1	0	0	0	0x28	TC	RC	RR	RL	FC	—	FR	FL
0	0	1	0	1	0	0	1	0x29	TC	RC	RR	RL	FC	LFE	FR	FL
0	0	1	0	1	0	1	0	0x2A	FCH	RC	RR	RL	FC	—	FR	FL
0	0	1	0	1	0	1	1	0x2B	FCH	RC	RR	RL	FC	LFE	FR	FL
0	0	1	0	1	1	0	0	0x2C	TC	FCH	RR	RL	FC	—	FR	FL
0	0	1	0	1	1	0	1	0x2D	TC	FCH	RR	RL	FC	LFE	FR	FL
0	0	1	0	1	1	1	0	0x2E	FRH	FLH	RR	RL	FC	—	FR	FL
0	0	1	0	1	1	1	1	0x2F	FRH	FLH	RR	RL	FC	LFE	FR	FL
0	0	1	1	0	0	0	0	0x30	FRW	FLW	RR	RL	FC	—	FR	FL
0	0	1	1	0	0	0	1	0x31	FRW	FLW	RR	RL	FC	LFE	FR	FL

Note: *Table 8 shows the labels abbreviations.*

Table 8. Channel Allocation Label ID

LABEL	LOCATION
FL	Front Left
FC	Front Center
FR	Front Right
FLC	Front-Left Center
FRC	Front-Right Center
RL	Rear Left
RC	Rear Center
RR	Rear Right
RLC	Rear-Left Center

LABEL	LOCATION
RRC	Rear-Right Center
LFE	Lower Frequency Effect
FLW	Front-Left Wide
FRW	Front-Right Wide
FLH	Front-Left High
FCH	Front-Center High
FRH	Front-Right High
TC	Top Center

Audio Channel from External Input

The audio channel input works with 8-channel TDM and stereo I2S, as well as nonstandard formats. Figure 16 shows the input format.

The period of the WS can be 8 to 256 SCK periods. The WS frame starts with the falling edge and can be low for 1 to 255 SCK periods. SD is one SCK period, sampled on the rising edge. MSB/LSB order, zero padding or any other significance assigned to the serial data does not affect operation of the audio channel. The polarity for WS and SCK edges is programmable.

Figure 17, Figure 18, Figure 19, and Figure 20 are examples of acceptable input formats.

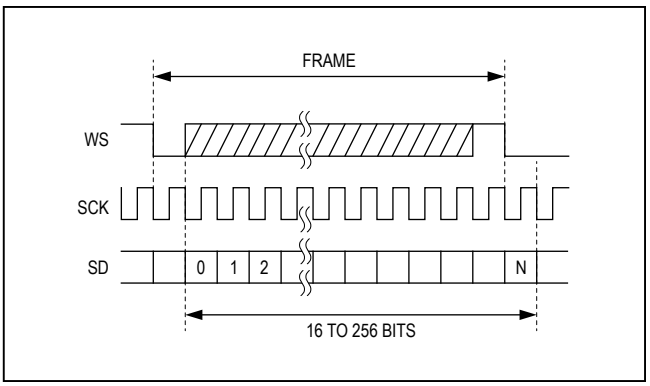


Figure 16. Audio Channel Input Format

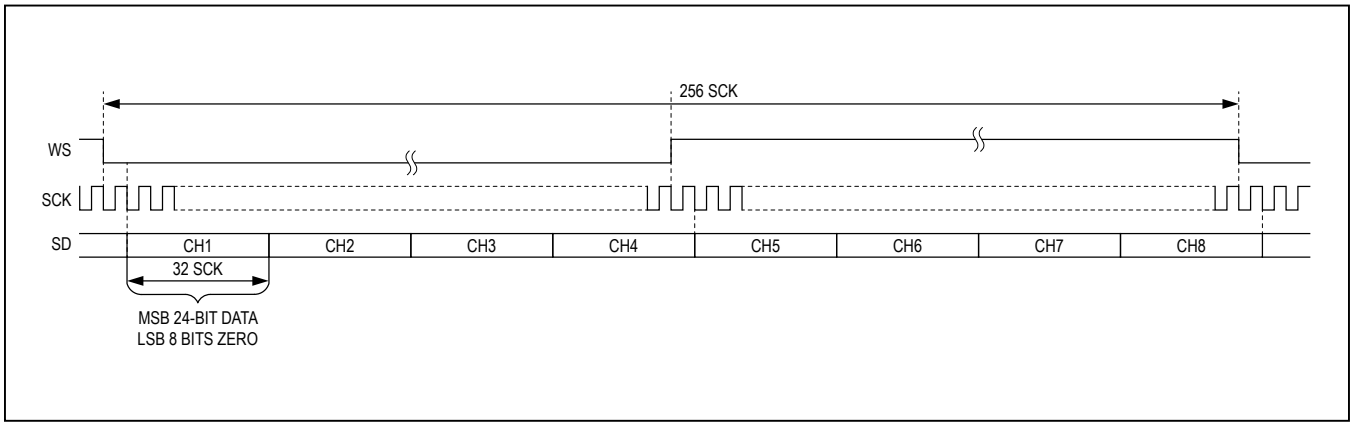


Figure 17. 8-Channel TDM (24-Bit Samples, Padded with Zeros)

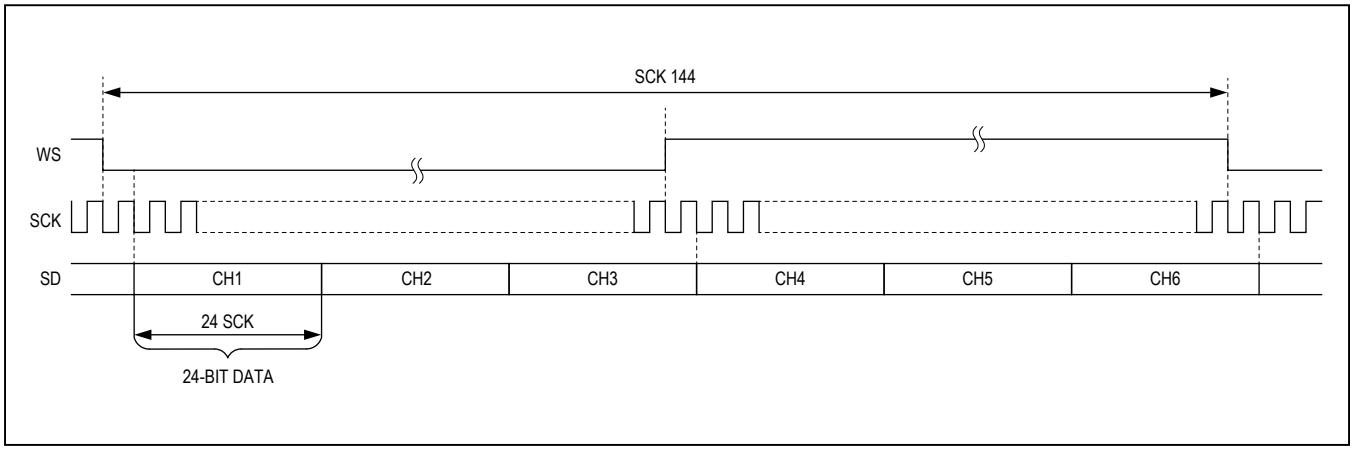


Figure 18. 6-Channel TDM (24-Bit Samples, No Padding)

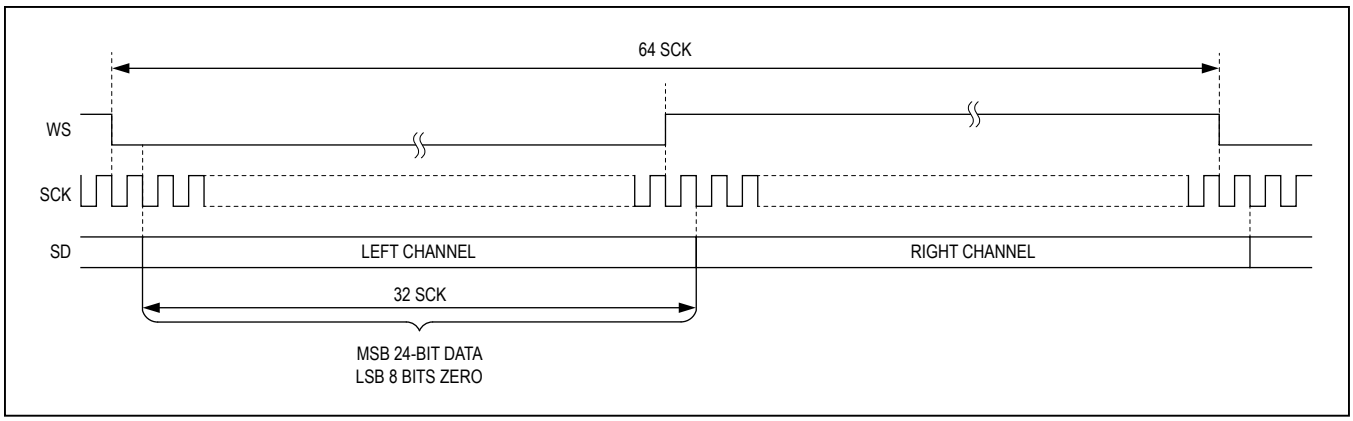


Figure 19. Stereo I²S (24-Bit Samples, Padded with Zeros)

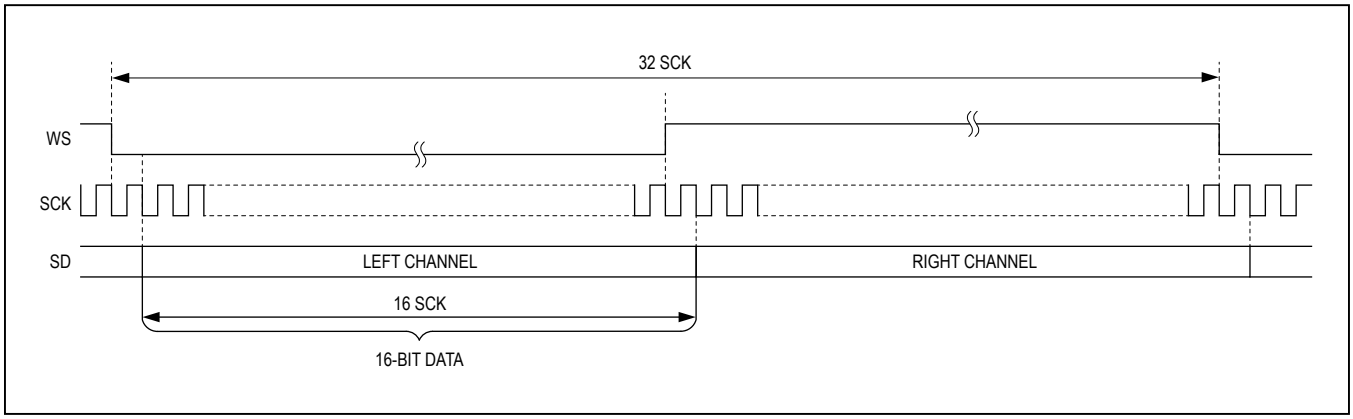


Figure 20. Stereo I²S (16-Bit Samples, No Padding)

Reverse Control Channel

The serializer uses the reverse control channel to receive I²C/UART and GPO signals from the deserializer in the opposite direction of the video stream. The reverse control channel and forward video data coexist on the same serial cable forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 2ms after power-up. The serializer temporarily disables the reverse control channel for 500µs after starting/stopping the forward serial link.

Control Channel and Register Programming

The control channel is available for the µC to send and receive control data over the serial link simultaneously with the high-speed data. The µC controls the link from either the serializer or the deserializer side to support video-display or image-sensing applications. The control channel between the µC and serializer or deserializer runs in base mode or bypass mode according to the mode selection (MS) input of the device connected to the µC. Base mode is a half-duplex control channel and the bypass mode is a full-duplex control channel. The total maximum forward or reverse control-channel delay is 2µs (UART) or 2 bit times (I²C) from the input of one device to the output of the other. I²C delay is measured from a START condition to START condition.

UART Interface

In base mode, the µC is the host and can access the GMSL registers of both the serializer and deserializer from either side of the link using the GMSL UART protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer, with the UART packets converted to I²C by the device on the remote side of the link. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings), using the half-duplex default GMSL UART protocol of the serializer/deserializer. The device addresses of the serializer and deserializer in base mode are programmable.

When the peripheral interface is I2C, the serializer/deserializer converts UART packets to I2C that have device addresses different from those of the serializer or deserializer. The converted I2C bit rate is the same as the original UART bit rate.

The deserializer uses differential line coding to send signals over the reverse channel to the serializer. The bit rate of the control channel is 9.6kbps to 1Mbps in both directions. The serializer and deserializer automatically detect the control-channel bit rate in base mode. Packet bit rate changes can be made in steps of up to 3.5 times higher or lower than the previous bit rate. See the *Changing the Clock Frequency* section for more information on changing the control-channel bit rate.

Figure 21 shows the UART protocol for writing and reading in base mode between the µC and the serializer/deserializer.

Figure 22 shows the UART data format. Even parity is used. Figure 23 and Figure 24 detail the formats of the SYNC byte (0x79) and the ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Events such as device wake-up and GPI generate transitions on the control channel that can be ignored by the µC. Data written to the serializer registers do not take effect until after the acknowledge byte is sent. This allows the µC to verify that write commands are received without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART's data rate. If the GPI or MS inputs of the deserializer toggle while there is control-channel communication, or if a line fault occurs, the control-channel communication will be corrupted. In the event of a missed or delayed acknowledge (~1ms due to control-channel timeout), the µC should assume there was an error in the packet transmission or response. In base mode, the µC must keep the UART Tx/Rx lines high no more than four bit times between bytes in a packet. Keep UART Tx/Rx lines high for at least 16 bit times before starting to send a new packet.

As shown in Figure 25, the remote-side device converts packets going to or coming from the peripherals from UART format to I2C format and vice versa. The remote device removes the byte number count and adds or receives the ACK between the data bytes of I2C. The I2C bit rate is the same as the UART bit rate.

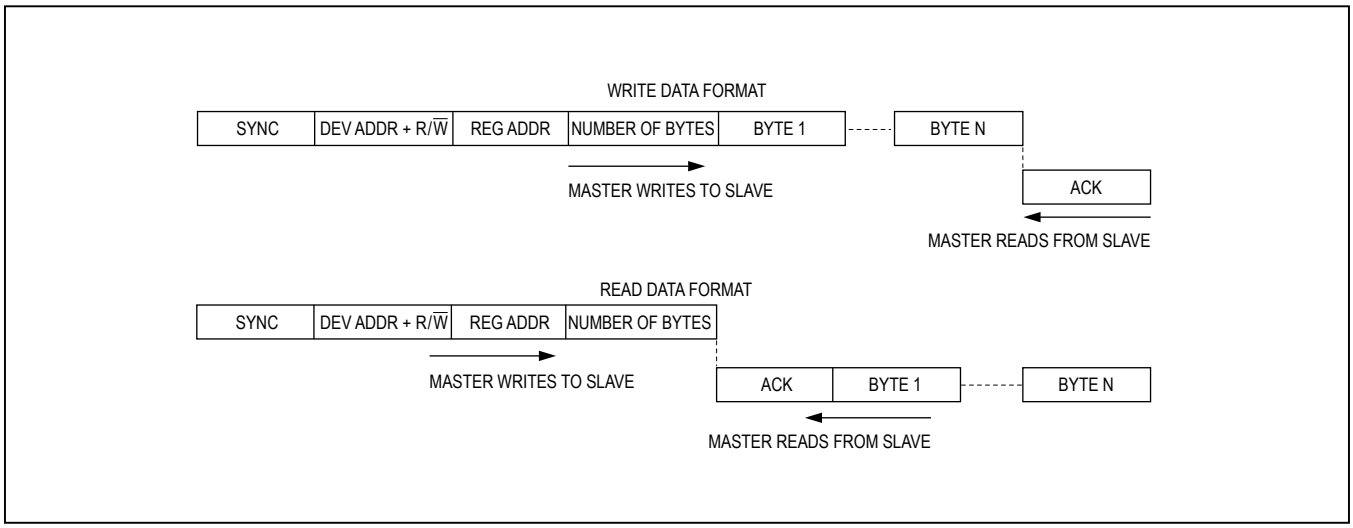


Figure 21. GMSL UART Protocol for Base Mode

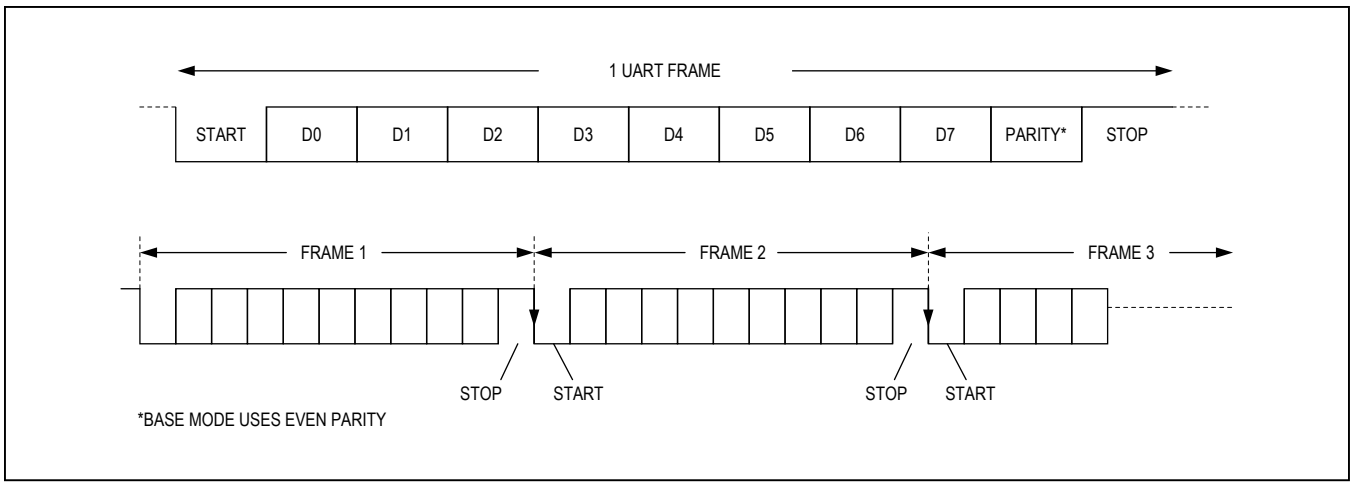


Figure 22. GMSL UART Data Format for Base Mode

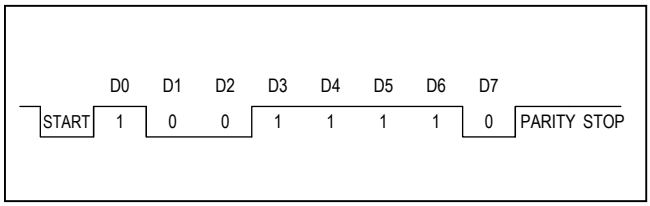


Figure 23. Sync Byte (0x79)

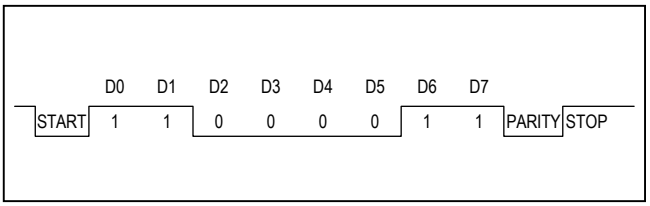


Figure 24. ACK Byte (0xC3)

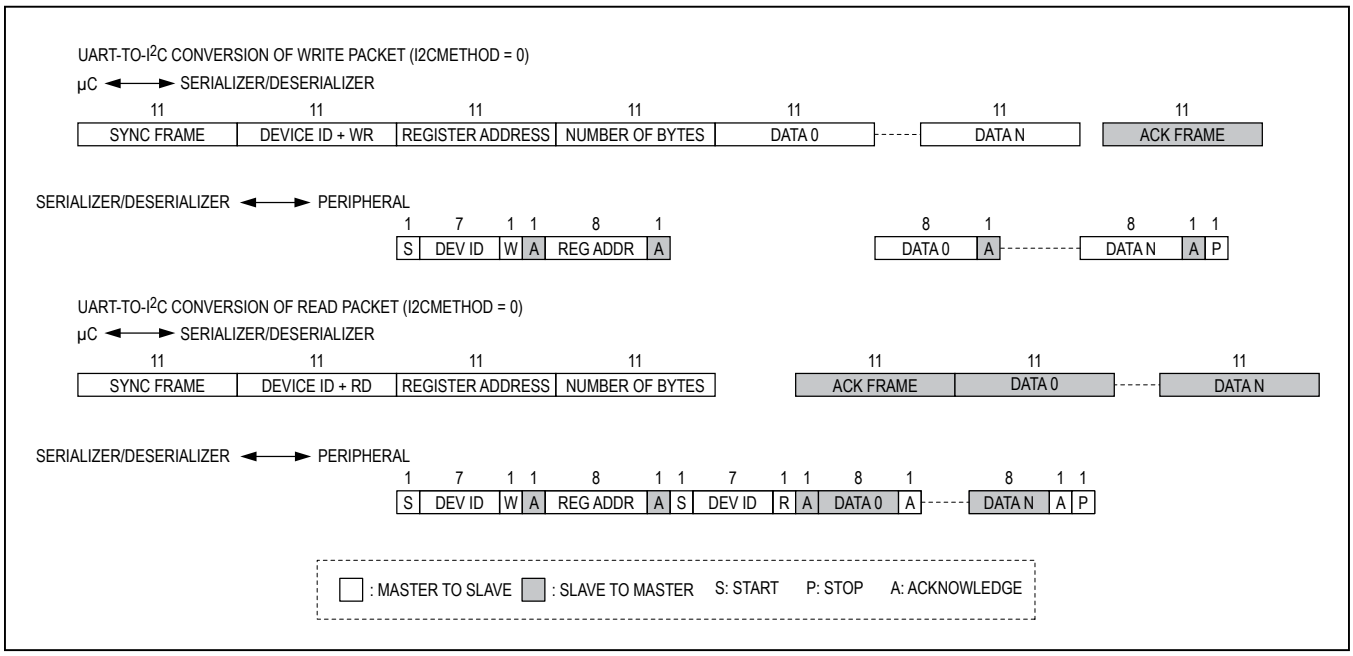


Figure 25. Format Conversion Between GMSL UART and I²C with Register Address (I2CMETHOD = 0)

Interfacing Command-Byte-Only I²C Devices with UART

The serializers' UART-to-I²C conversion can interface with devices that do not require register addresses, such as the MAX7324 GPIO expander. In this mode, the I²C master ignores the register address byte and directly reads/writes the subsequent data bytes (Figure 26). Change the communication method of the I²C master using the I2CMETHOD bit. I2CMETHOD = 1 sets command-byte-only mode, while I2CMETHOD = 0 sets normal mode where the first byte in the data stream is the register address.

UART Bypass Mode

In bypass mode, the serializers ignore UART commands from the µC and the µC communicates with the peripherals directly using its own defined UART protocol. The µC cannot access the serializer/deserializer's registers in this mode. Peripherals accessed through the forward control channel using the UART interface need to handle at least one RXC_ period ±10ns of jitter due to the asynchronous sampling of the UART signal by RXC_. Set MS/HVEN = high to put the control channel into bypass mode. For applications with the µC connected to the deserializer, there is a 1ms wait time between setting MS high and the bypass control channel being active. There is no delay time when switching to bypass mode when the µC is connected to the serializer. Do not send a logic-low value longer than 100µs to ensure proper GPO functionality. Bypass mode accepts bit rates down to 10kbps in either direction. See the *GPO/GPI Control* section for GPI functionality limitations. The control-channel data pattern should not be held low longer than 100µs if GPI control is used.

I²C Interface

In I²C-to-I²C mode, the serializer's control-channel interface sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master and slave(s). A µC master initiates all data transfers to and from the device and generates the SCL clock that synchronizes the data transfer. When an I²C transaction starts on the local side device's control-channel port, the remote side device's control-channel port becomes an I²C master that interfaces with remote side I²C peripherals. The I²C master must accept clock-stretching which is imposed by the serializer (holding SCL low) The SDA and SCL lines operate as both an input and an open-drain output. Pullup resistors are required on SDA and SCL. Each transmission consists of a START condition (Figure 6) sent by a master, followed by the device's 7-bit slave address plus a R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition.

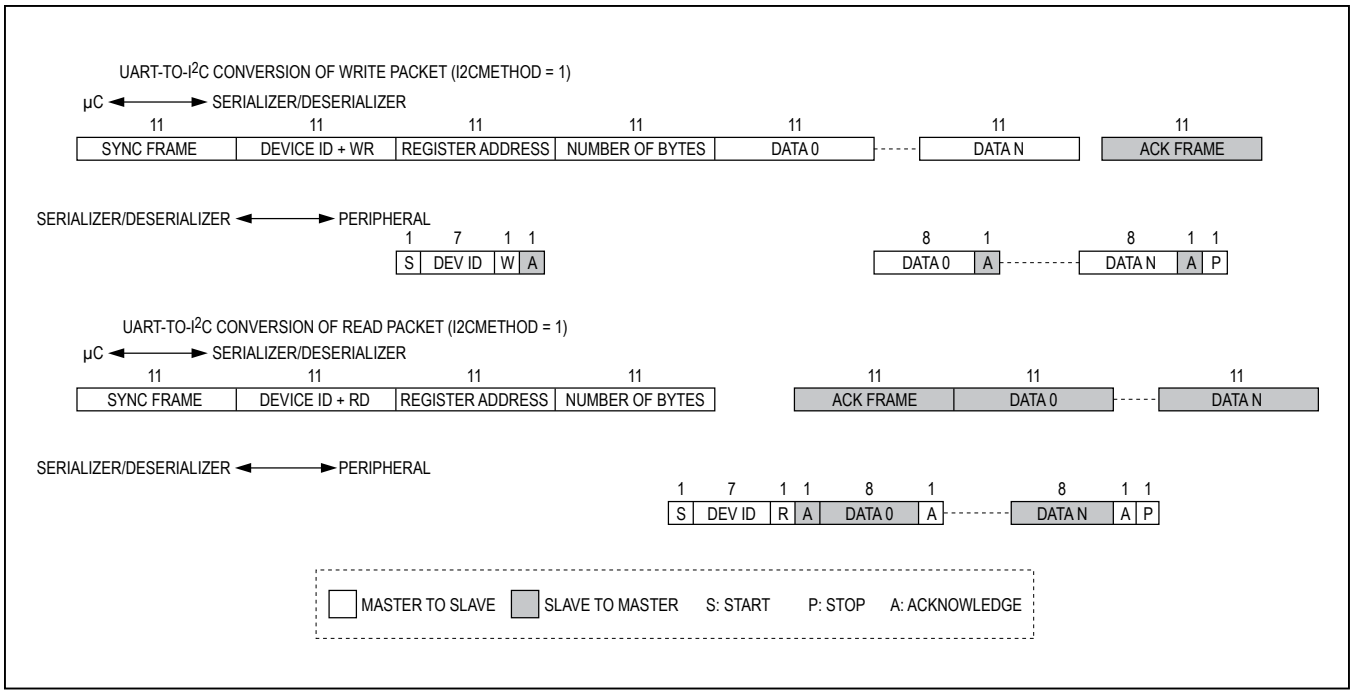


Figure 26. Format Conversion Between GMSL UART and I²C Register Address (I2CMETHOD = 1)

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (Figure 27). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 28). The data on SDA must remain stable while SCL is high.

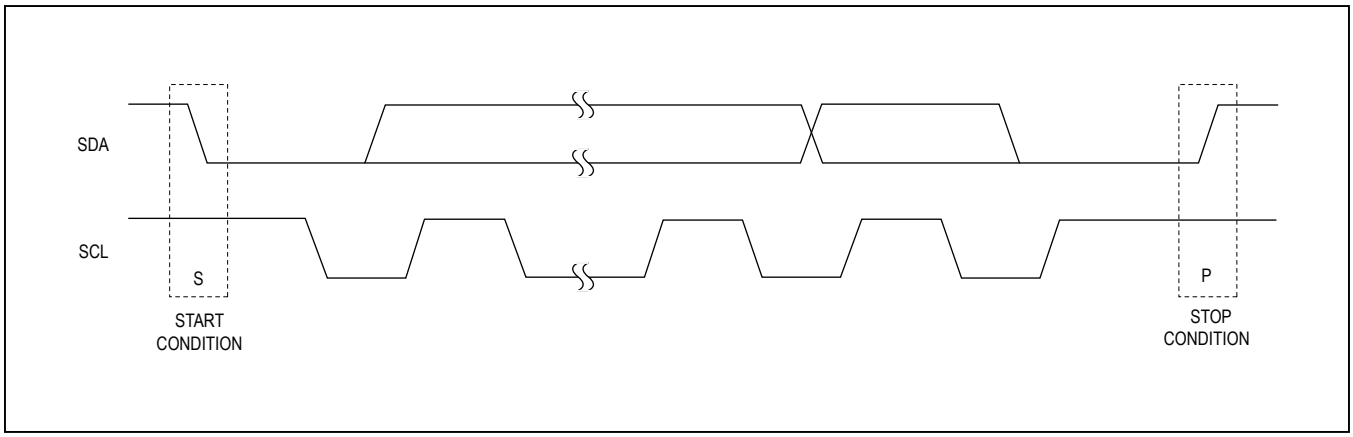


Figure 27. START and STOP Conditions

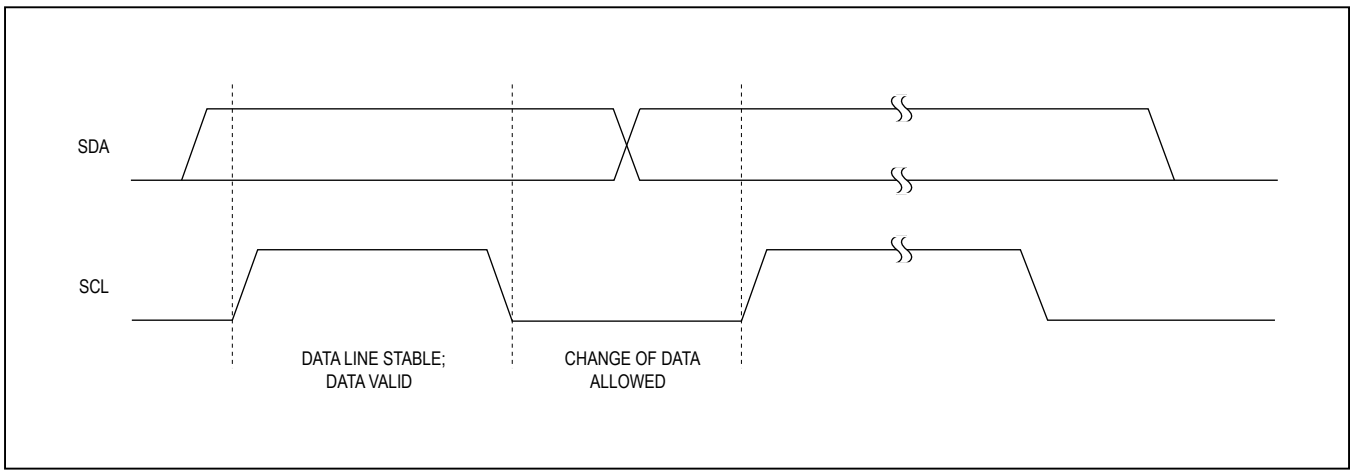


Figure 28. Bit Transfer

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 29). Thus, each byte transferred effectively requires nine bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the slave device, the slave device generates the acknowledge bit because the slave device is the recipient. When the slave device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. The device generates an acknowledge even when the forward control channel is not active. To prevent acknowledge generation when the forward control channel is not active, set the I2CLOCACK bit low.

Slave Address

The serializers have 7-bit long slave addresses. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The slave address for the serializer is XX00XX01 for read commands and XX00XX00 for write commands. See Figure 30.

Bus Reset

The device resets the bus with the I^2C START condition for reads. When the R/$\overline{W}$ bit is set to 1, the serializers transmit data to the master, thus the master is reading from the device.

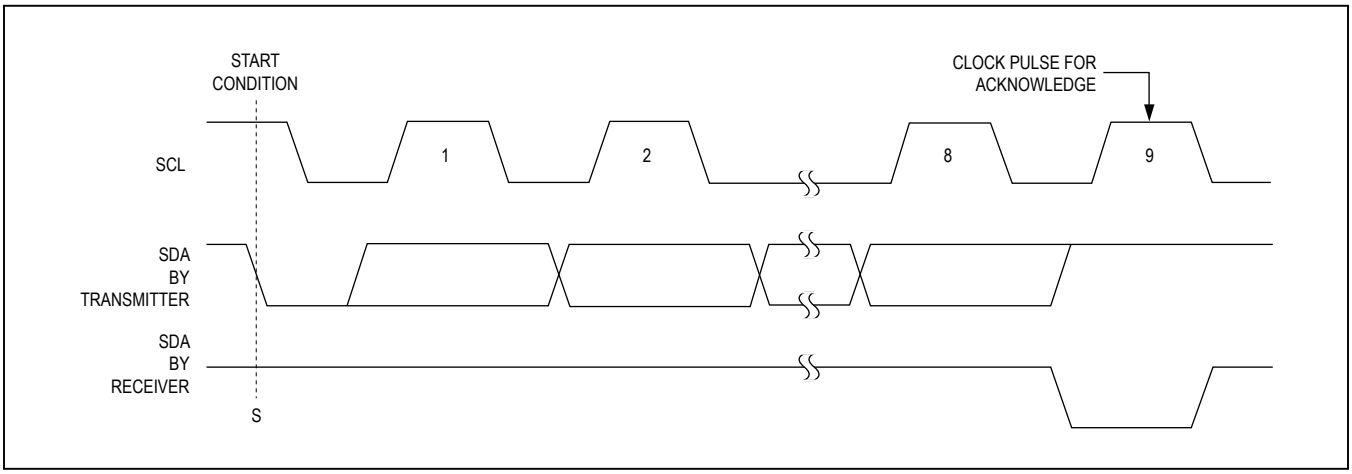


Figure 29. Acknowledge

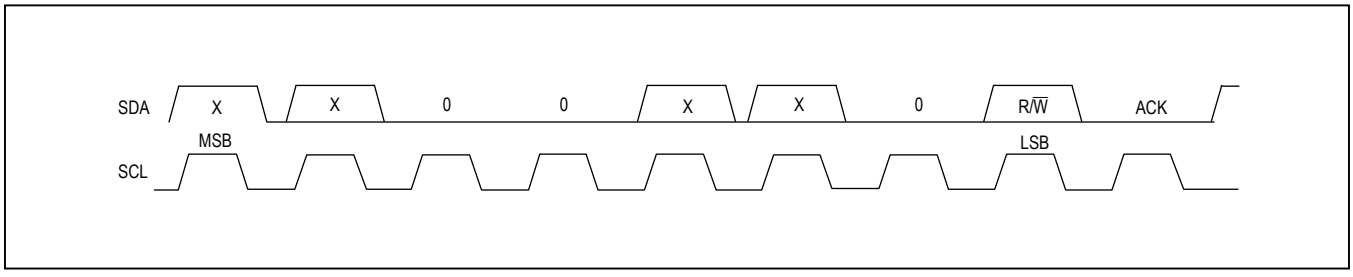


Figure 30. Slave Address

Format for Writing

Writes to the serializers comprise the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least one byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, the device takes no further action beyond storing the register address (Figure 31). Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address, and subsequent data bytes go into subsequent registers (Figure 32). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses autoincrements.

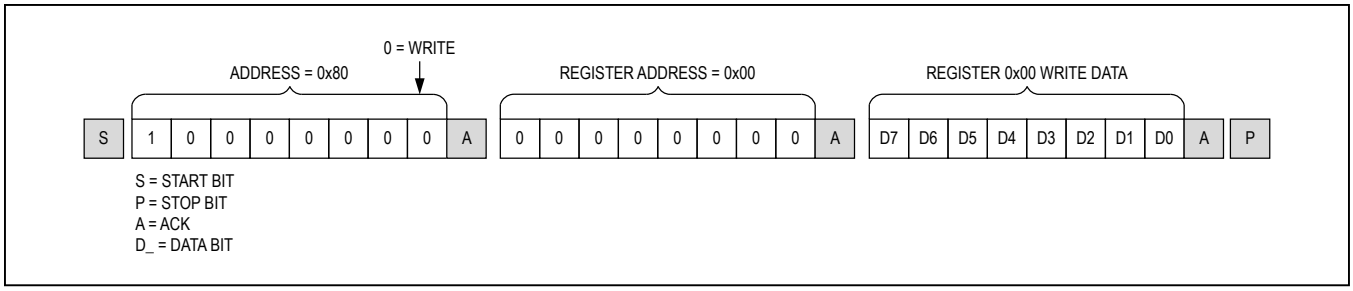


Figure 31. Format for I²C Write

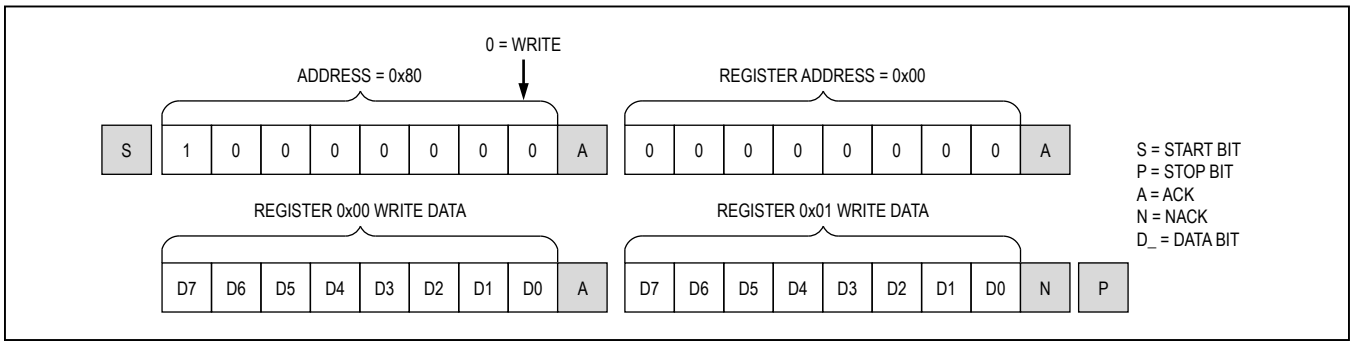


Figure 32. Format for I²C Write to Multiple Registers

Format for Reading

The serializers are read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 33). The master can now read consecutive bytes from the device, with the first data byte being read from the register address pointed by the previously written register address. Once the master sends a NACK, the device stops sending valid data.

I²C Communication with Remote-Side Devices

The serializers support I²C communication with a peripheral on the remote side of the communication link using SCL clock stretching. While multiple masters can reside on either side of the communication link, arbitration is not provided. The connected masters need to support SCL clock stretching. The remote side I²C bit rate range must be set according to the local side I²C bit rate. Supported remote side bit rates can be found in Table 9. Set the I2CMSTBT (register 0x1C) to set the remote I²C bit rate. If using a bit rate different from 400kbps, local and remote side I²C setup and hold times should be adjusted by setting the I2CSLVSH register settings on both sides.

I²C Address Translation

The serializers support I²C address translation for up to two device addresses. Use address translation to assign unique device addresses to peripherals with limited I²C addresses. Source addresses (address to translate from) are stored in registers 0x0F and 0x11. Destination addresses (address to translate to) are stored in registers 0x10 and 0x12.

Table 9. I²C Bit Rate Ranges

LOCAL BIT RATE	REMOTE BIT RATE RANGE	I2CMSTBT SETTING
f > 50kbps	Up to 1Mbps	ANY
20kbps < f < 50kbps	Up to 400kbps	Up to 110
f < 20kbps	Up to 10kbps	000

In a multilink situation where there are multiple deserializers and/or peripheral devices connected to these serializers, the deserializers support broadcast commands to control these multiple devices. Select an unused device address to use as a broadcast device address. Program all the remote side serializer devices to translate the broadcast device address (source address stored in registers 0x0F, 0x11) to the peripherals' address (destination address stored in registers 0x10, 0x12). Any commands sent to the broadcast address (selected unused address) will be sent to all deserializers and/or peripheral devices connected to the deserializers whose addresses match the translated broadcast address.

GPO/GPI Control

GPO on the serializer follows GPI transitions on the deserializer. This GPO/GPI function can be used to transmit signals such as a frame sync in a surround-view camera system. The GPI-to-GPO delay is 0.35ms max. Keep time between GPI transitions to a minimum 0.35ms. This includes transitions from the other deserializer in coax splitter mode. Bit D4 of register 0x06 in the deserializer stores the GPI input state. GPO is low after power-up. The µC can set GPO by writing to the SETGPO register bit. Do not send a logic-low value on the deserializer RX/SDA input (UART mode) longer than 100µs in either base or bypass mode to ensure proper GPO/GPI functionality.

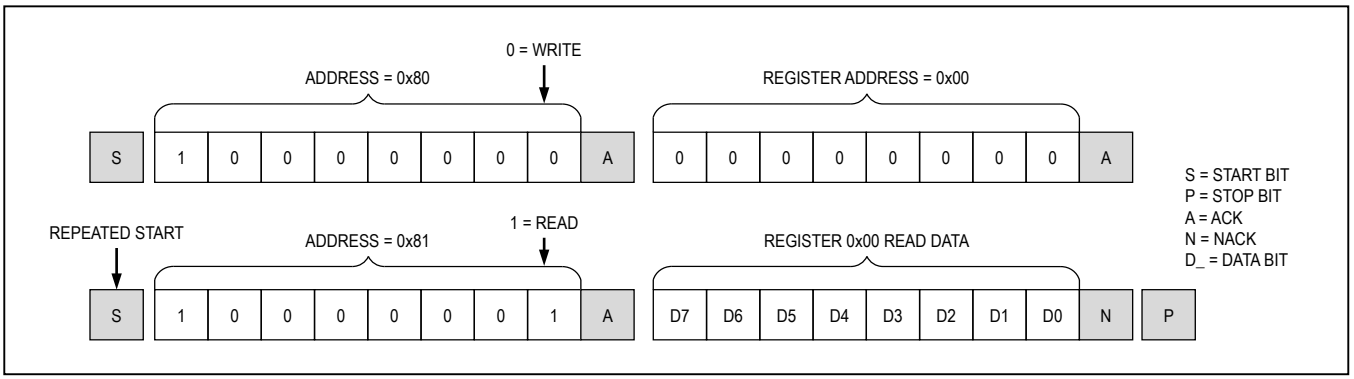


Figure 33. Format for I²C Read

Pre/Deemphasis Driver

The serial line driver employs current-mode logic (CML) signaling. The driver is differential when programmed for twisted pair. When programmed for coax, one side of the CML driver is used. The line driver has programmable pre/deemphasis, which modifies the output to compensate for cable length. There are 13 preemphasis settings as shown in Table 10. Negative preemphasis levels are deemphasis levels in which the preemphasized swing level is the same as normal swing, but the no-transition data is deemphasized. Program the preemphasis levels through register 0x05 D[3:0] of the serializer. This preemphasis function compensates the high frequency loss of the cable and enables reliable transmission over longer link distances. Current drive for both TP and coax modes is programmable. CMLLVL bits (0x05, D[5:4]) program drive current in TP mode. CMLLVLCX (0x14, D[7:4]) program drive current in coax mode.

Spread Spectrum

To reduce the EMI generated by the transitions on the serial link, the deserializer output is programmable for spread spectrum. If the deserializer, paired with the MAX9291/MAX9293, has programmable spread spectrum, do not enable spread for both at the same time or their interaction will cancel benefits. The deserializer will track the serializer spread and will pass the spread to the deserializer output. The programmable spread-spectrum amplitudes are ±0.5%, ±1%, ±1.5%, ±2%, ±3%, and ±4% (Table 11). Some spread-spectrum amplitudes can only be used at lower RXC_ frequencies (Table 12). There is no RXC_ frequency limit for the ±0.5% spread rate.

The deserializer includes a sawtooth divider to control the spread modulation rate. Autodetection of the RXC_ operation range guarantees a spread-spectrum modulation frequency within 20kHz to 40kHz. Additionally, manual configuration of the sawtooth divider (SDIV: 0x03, D[5:0]) allows the user to set a modulation frequency according to the RXC_ frequency. When ranges are manually selected, program the SDIV value for a fixed modulation frequency around 20kHz.

Table 10. TP/COAX Drive Current (400mV Output Drive Levels)

PREEMPHASIS LEVEL (dB)*	PREEMPHASIS SETTING (0x06 D[3:0])	I_{CML} (mA)	I_{PRE} (mA)	SINGLE-ENDED VOLTAGE SWING	
				BOOSTED LEVEL (mV)	UNBOOSTED LEVEL (mV)
-6.0	0100	12	4	400	200
-4.1	0011	13	3	400	250
-2.5	0010	14	2	400	300
-1.2	0001	15	1	400	350
0	0000	16	0	400	400
1.1	1000	16	1	425	375
2.2	1001	16	2	450	350
3.3	1010	16	3	475	325
4.4	1011	16	4	500	300
6.0	1100	15	5	500	250
8.0	1101	14	6	500	200
10.5	1110	13	7	500	150
14.0	1111	12	8	500	100

**Negative preemphasis levels denote deemphasis.*

Manual Programming of the Spread-Spectrum Divider

The modulation rate relates to the RXC_ frequency as follows:

$$f_M = (1 + DRS)\ f_{PCLKIN}/(MOD \times SDIV)$$

where:

f_M = Modulation frequency

DRS = DRS value (0 or 1)

$f_{RXC_}$ = RXC_ frequency

MOD = Modulation coefficient given in Table 13

SDIV = 6-bit SDIV setting, manually programmed by the µC

To program the SDIV setting, first look up the modulation coefficient according to the desired bus-width and spread-spectrum settings. Solve the above equation for SDIV using the desired pixel clock and modulation frequencies. If the calculated SDIV value is larger than the maximum allowed SDIV value in Table 13, set SDIV to the maximum value.

Table 11. Output Spread

SS	SPREAD (%)
000	No spread spectrum. **Power-up default when SSEN = low.**
001	±0.5% spread spectrum. **Power-up default when SSEN = high.**
010	±1.5% spread spectrum.
011	±2% spread spectrum.
100	No spread spectrum.
101	±1% spread spectrum.
110	±3% spread spectrum.
111	±4% spread spectrum.

Table 12. Spread Limitations

HIGH-BANDWIDTH MODE RXC_FREQUENCY (MHz)	32-BIT MODE RXC_ FREQUENCY (MHz)	SERIAL LINK BIT-RATE (Mbps)	AVAILABLE SPREAD RATES
< 33.3	< 25	< 1000	All rates available
33.3 to < 66.7	25 to < 50	1000 to < 2000	1.5%, 1.0%, 0.5%
66.7+	50+	2000+	0.5%

Table 13. Modulation Coefficients and Maximum SDIV Settings

BIT WIDTH MODE	SPREAD SPECTURM SETTING (%)	MODULATION COEFFICIENT MOD (DEC)	SDIV UPPER LIMIT (DEC)
32-bit mode	1	104	40
	0.5	104	63
	6	152	27
	1.5	152	54
	4	204	15
	2	204	30
High-bandwidth mode	1	80	52
	0.5	80	63
	3	112	37
	1.5	112	63
	4	152	21
	2	152	42

Serial Output

The driver output is programmable for two kinds of cable: 100Ω twisted pair and 50Ω coax (contact the factory for devices compatible with 75Ω cables).

Coax Splitter Mode

In coax mode, OUT+ and OUT- of the serializer are active. This enables the use as a 1:2 splitter (Figure 34). In coax mode, connect OUT+ to IN+ of the deserializer. Connect OUT- to IN- of the second deserializer. Control-channel data is broadcast from the serializer to both deserializers and their attached peripherals. Assign a unique address to send control data to one deserializer. Leave all unused IN_ pins unconnected, or connect them to ground through 50Ω and a capacitor for increased power-supply rejection. If OUT- is not used, connect OUT- to V_{DD} through a 50Ω resistor (Figure 35). When there are µCs at the serializer, and at each deserializer, only one µC can communicate at a time. Disable forward and reverse channel links according to the communicating deserializer connection to prevent contention in I^2C-to-I^2C mode. Use ENREVP or ENREVN register bits to disable/enable the control-channel link. In UART mode, the serializer provides arbitration of the control-channel link.

High-Immunity Reverse Control-Channel Mode

The serializers contain a high-immunity reverse control-channel mode, which has increased robustness at half the bit rate over the standard GMSL reverse control channel link (Table 14).Connect a 30kΩ resistor to HIM on the serializer, and SD/HIM on the deserializer to use high-immunity mode at power-up. Set the HIGHIMM bit high in both the serializer and deserializer to enable high-immunity mode at any time after power-up. Set the HIGHIMM bit low in both the serializer and deserializer to use the legacy reverse control-channel mode. The serializer reverse channel mode is not available for 500µs/1.92ms after the reverse control-channel mode is changed through the serializer/deserializer's HIGHIMM bit setting, respectively. The user must set SD/HIM and HIM or the HIGHIMM bits to the same value for proper reverse control-channel communication.

In high-immunity mode, set HPFTUNE = 00 in the equalizer, if the serial bit rate = [RXC_ x 30 (BWS = open) or 40 (BWS = high)] is larger than 1Gbps when BWS is high. When BWS = open, set HPFTUNE = 00 when the serial bit rate is larger than 2GBps. In addition, use 47nF AC-coupling capacitors. Note that legacy reverse control-channel mode may not function when using 47nF AC-coupling capacitors.

Table 14. Reverse Control-Channel Modes

HIGHIMM BIT OR HIM PIN SETTING	REVFAST BIT	REVERSE CONTROL-CHANNEL MODE	MAX UART/I^2C BITRATE (kbps)
Low (1)	X	Legacy reverse control-channel mode (compatible with all GMSL devices)	1000
High (1)	0	High-immunity mode	500
	1	Fast high-immunity mode	1000

X = Don't care.

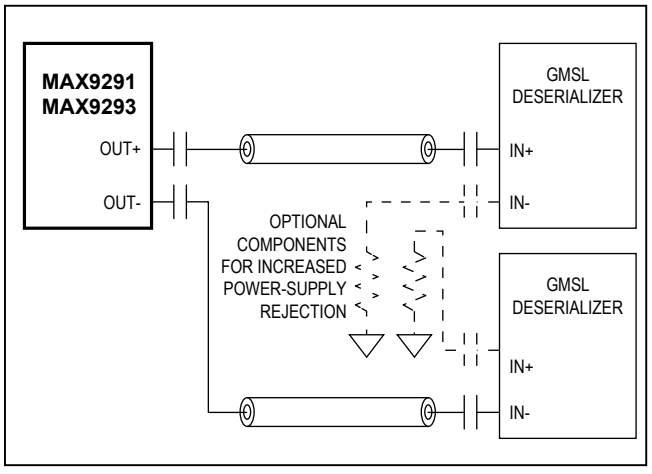


Figure 34. Coax Splitter Connection Diagram

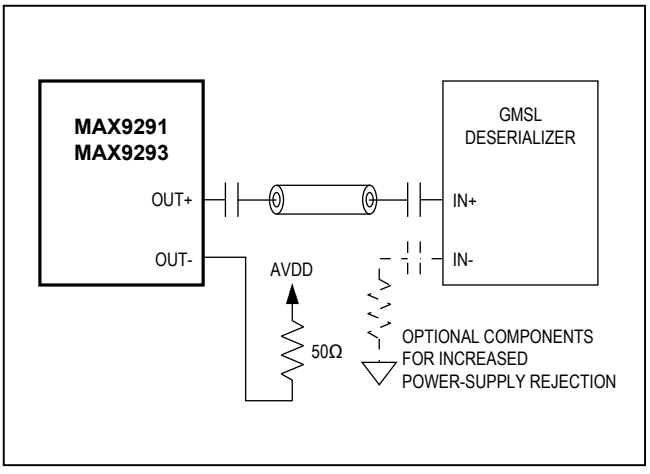


Figure 35. Coax Connection Diagram

By default, high-immunity mode uses a 500kbps bit rate. Set REVFAST =1 (D7 in register 0x1A in the serializer and register 0x11 in the deserializer) in both devices to use a 1Mbps bit rate. Certain limitations apply when using the fast high-immunity mode (Table 15).

Sleep Mode

The serializers have sleep mode to reduce power consumption when powered up. The devices enter or exit sleep mode by a command from a local µC or a remote µC using the control channel. Set the SLEEP bit to 1 to initiate sleep mode. Entering sleep mode resets the HDCP registers, but not the configuration registers. The serializer sleeps immediately after setting its SLEEP = 1. The serial outputs has a wake-up receiver to accept wake-up commands from the attached deserializer. Wake-up from the remote side is not supported in coax splitter mode. Disable the wake-up receiver (through DISRWAKE), if wake-up from remote side is not used in order to reduce sleep mode current. If the wake-up receiver is disabled, the device can only be woken up from the local control channel. See the *Link Startup Procedure* section for details on waking up the device for different µC and starting conditions.

To wake up from the local or remote side, send an arbitrary control-channel command to serializer, wait for 5ms for the chip to power up and then write 0 to SLEEP register bit to make the wake-up permanent.

The serializer cannot power up into sleep mode when CDS = 0 (for LCD applications), however after power-up, the device can be put to sleep.

Power-Down Mode

The serializers have a power-down mode that further reduces power consumption compared to sleep mode. Set $\overline{\text{PWDN}}$ low to enter power-down mode. In power-down, the serial outputs remain high impedance. Entering power-down resets the device's registers. Upon exiting power-down, the state of external pins SSEN, DRS, $\overline{\text{AUTOS}}$, ADD[1:0], CX/TP, HIM, and BWS are latched.

Configuration Link

The control channel can operate in a low-speed mode called configuration link in the absence of a clock input. This allows a microprocessor to program configuration registers before starting the video link. An internal oscillator provides the clock for the configuration link. Set CLINKEN = 1 on the serializer to enable configuration link. Configuration link is active until the video link is enabled. The video link overrides the configuration link and attempts to lock when SEREN = 1.

HDMI Power and Support Pins

HDMI Source Power Detect (HSPD)

The HDMI source supplies 5V ±0.3V when using the DDC or TMDS signals. Connect a voltage-divider between the 5V source power and HSPD, so that 5V at the input of the divider corresponds with V_{IOVDD} input high voltage at HSPD. The power-on circuitry senses when 5V power is applied and stable.

Hot-Plug Detect (HPD)

HPD should be driven high when the EDID is ready to read, and HSPD is asserted (source power is detected). HPD is pulsed by the control-channel µC when a new device is connected, or after the EDID is programmed. The HPD buffer is powered by HVDD. The output impedance of HPD is 1000Ω ±20% HPD is high impedance during power-down or sleep mode.

Display Data Channel (DDC)

The HDMI source uses the DDC I^2C port to read the EDID. The MAX9291/MAX9293 limit DDC access to EDID registers to prevent contention between DDC and GMSL control-channel operations. DDC accessible registers reside at DDC address 0x74, while DDC EDID resides at DDC address 0xA0. DDC is disabled by default.

EDID

The MAX9291/MAX9293 store EDID information in a 256-byte memory EDID is undefined at power-up. Program EDID through the GMSL I^2C interface (address 0xFE). DDC has access to the EDID through DDC address 0xA0.

HDMI Termination Supply (HVDD)

HVDD is the 3.3V ±5% input termination supply for the TMDS inputs. Each pin of the RX_ inputs is pulled up to HVDD through a 50Ω ±10% termination resistor. HVDD must be powered-up by the time the source finishes reading the EDID.

Table 15. Fast High-Immunity Mode Requirements

BWS SETTING	ALLOWED RXC_ FREQUENCY (MHz)
High	> 30
Open	> 83.33

Note: *Fast high-immunity mode requires DRS = 0.*

Link Startup Procedure

Table 16 lists the startup procedure for display applications (CDS = low). Table 17 lists the startup procedure for image-sensing applications (CDS = high). The control channel is available after the video link or the configuration link is established. If the deserializer powers up after the serializer, the control channel becomes unavailable for 2ms after power-up.

Table 16. Startup Procedure for Video-Display Applications (CDS = Low, See Figure 36)

NO.	µC	SERIALIZER		DESERIALIZER
		(AUTOSTART ENABLED)	(AUTOSTART DISABLED)	
—	µC connected to serializer	Set all configuration inputs. Set . If any configuration inputs are available on one end of the link but not the other, always connects that configuration input low.	Set all configuration inputs. If any configuration inputs are available on one end of the link but not the other, always connects that configuration input low.	Set all configuration inputs. If any configuration inputs are available on one end of the link but not the other, always connects that configuration input low.
1	Powers up	Powers up and loads default settings. Establishes video link when valid RXC_ available.	Powers up and loads default settings.	Powers up and loads default settings. Locks to video link signal if available.
2	Enables serial link by setting SEREN = 1 or configuration link by setting SEREN = 0 and CLINKEN = 1 (if valid RXC_ not available) and gets an acknowledge. Waits for link to be establish (~3ms).	—	Establishes configuration or video link	Locks to configuration or video link signal.
3	Writes configuration bits in the serializer/deserializer and gets an acknowledge.	Configuration changed from default settings.		Configuration changed from default settings.
4	If not already enabled, sets SEREN = 1, gets an acknowledge and waits for video link to be established (~3ms).	Establishes video link when valid RXC_ available (if not already enabled).		Locks to video link signal (if not already locked).
5	Begin sending video data to input	Video data serialized and sent across serial link.		Video data received and deserialized.

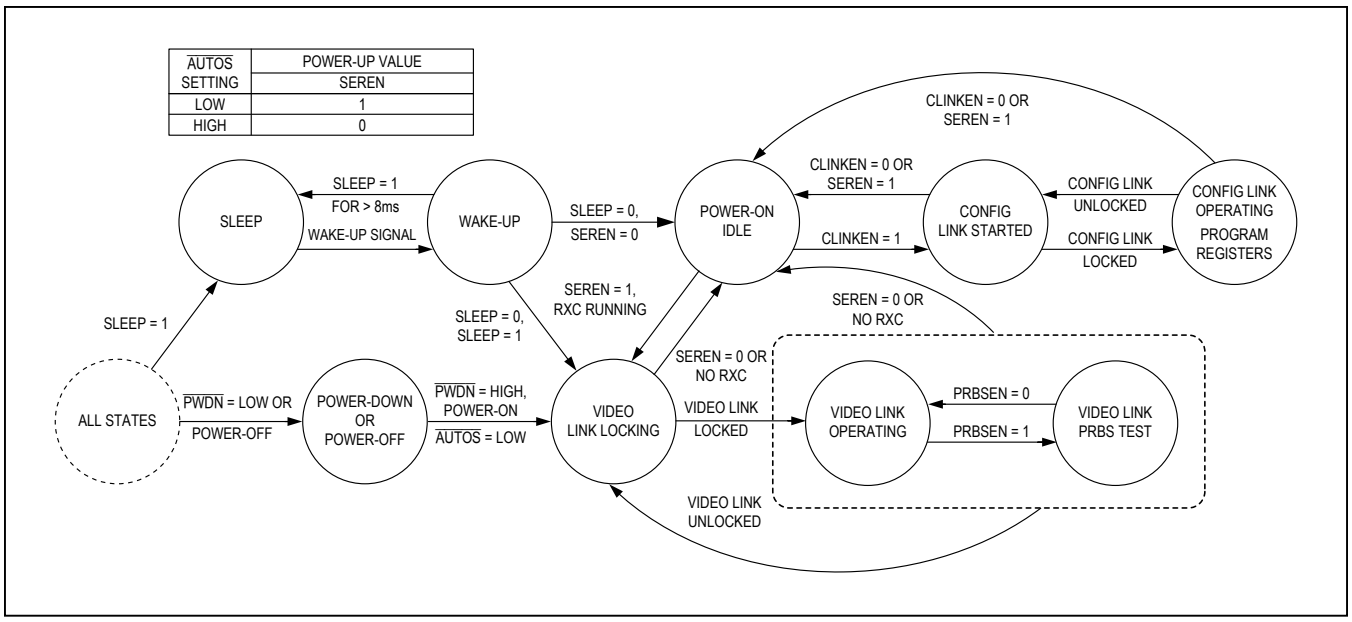


Figure 36. State Diagram, CDS = Low (Display Applications)

Table 17. Startup Procedure for Image-Sensing Applications (CDS = High, See Figure 37)

NO.	µC	SERIALIZER		DESERIALIZER
		(AUTOSTART ENABLED)	(AUTOSTART DISABLED)	
—	µC connected to deserializer.	Set all configuration inputs.	Set all configuration inputs.	Set all configuration inputs.
1	Powers up.	Powers up and loads default settings. Establishes video link when valid RXC_ available.	Powers up and loads default settings. Goes to sleep after 8ms.	Powers up and loads default settings. Locks to video link signal if available.
2	Writes deserializer configuration bits and gets an acknowledge.	—	—	Configuration changed from default settings.
3	Wakes up the serializer by sending dummy packet, and then writing SLEEP = 0 within 8ms. May not get an acknowledge (or gets a dummy acknowledge) if not locked.	—	Wakes up.	—
4	Writes serializer configuration bits. May not get an acknowledge (or gets a dummy acknowledge) if not locked.	Configuration changed from default settings.		—
5	If not already enabled, sets SEREN = 1, gets an acknowledge and waits for serial link to be established (~3ms).	Establishes video link when valid RXC_ available (if not already enabled).		Locks to video link signal (if not already locked).
6	Begin sending video data to input.	Video data serialized and sent across serial link.		Video data received and deserialized.

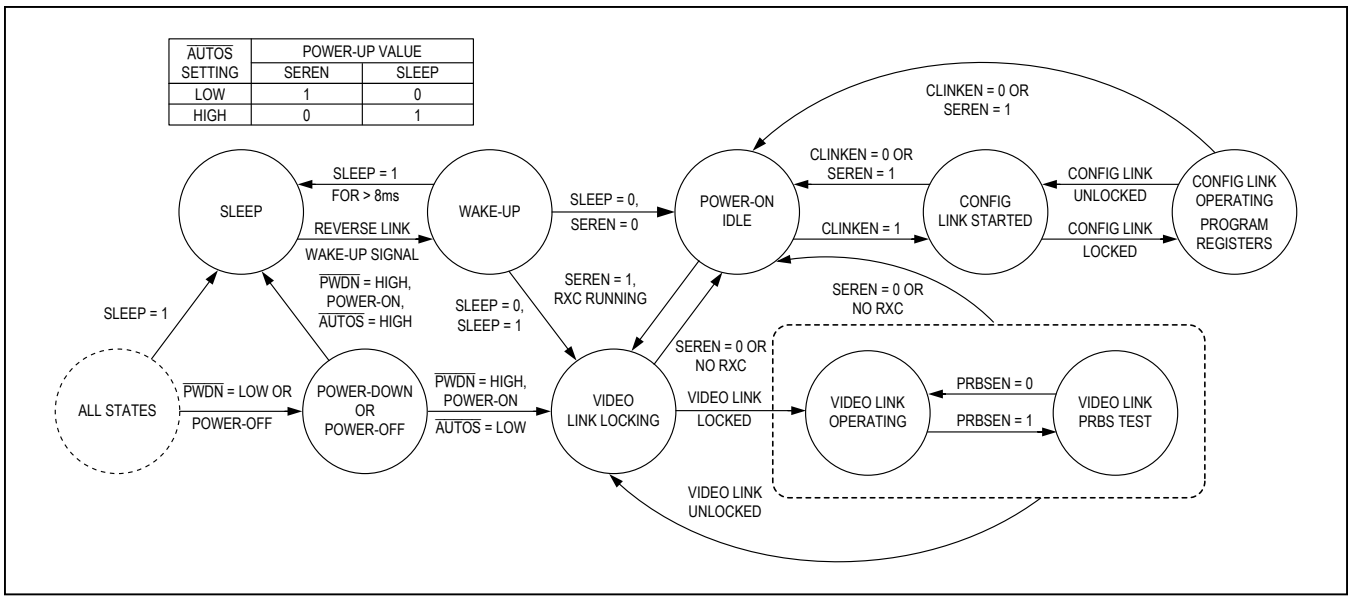


Figure 37. State Diagram, CDS = High (Image Sensing)

High-Bandwidth Digital Content Protection (HDCP)

Note: HDMI HDCP operation is explained in the HDMI HDCP System documents. The explanation of HDCP operation in this data sheet is provided as a guide for general understanding. Implementation of HDCP in a product must meet the requirements given in the HDCP System v1.3 Amendment for GMSL, which is available from DCP.

HDCP has two main phases of operation, authentication and the link integrity check. The µC starts authentication by writing to the START_AUTHENTICATION bit in the GMSL serializer. The GMSL serializer generates a 64-bit random number. The host µC first reads the 64-bit random number from the GMSL serializer and writes it to the deserializer. The µC then reads the GMSL serializer public key selection vector (AKSV) and writes it to the deserializer. The µC then reads the deserializer KSV (BKSV) and writes it to the GMSL serializer. The µC begins checking BKSV against the revocation list. Using the cipher, the GMSL serializer and deserializer calculate a 16-bit response value, R0 and R0', respectively. The GMSL amendment for HDCP reduces the 100ms minimum wait time allowed for the receiver to generate R0' (specified in HDCP rev 1.3) to 128 pixel clock cycles in the GMSL amendment.

There are two response-value comparison modes, internal comparison and µC comparison. Set EN_INT_COMP = 1 to select internal comparison mode. Set EN_INT_COMP = 0 to select µC comparison mode. In internal comparison mode, the µC reads the deserializer response R0' and writes it to the GMSL serializer. The GMSL serializer compares R0' to its internally generated response value R0, and sets R0_RI_MATCHED. In µC comparison mode, the µC reads and compares the R0/R0' values from the GMSL serializer/deserializer.

During response-value generation and comparison, the host µC checks for a valid BKSV (having 20 1s and 20 0s is also reported in BKSV_INVALID) and checks BKSV against the revocation list. If BKSV is not on the list and the response values match, the host authenticates the link. If the response values do not match, the µC resamples the response values (as described in HDCP rev 1.3, Appendix C). If resampling fails, the µC restarts authentication by setting the RESET_HDCP bit in the GMSL serializer. If BKSV appears on the revocation list, the host cannot transmit data that requires protection. The host knows when the link is authenticated and decides when to output data requiring protection. The µC performs a link integrity check every 128 frames or every 2s ±0.5s. The GMSL serializer/deserializer generate response values every 128 frames. These values are compared internally (internal comparison mode) or can be compared in the host µC.

In addition, the GMSL serializer/deserializer provide response values for the enhanced link verification. Enhanced link verification is an optional method of link verification for faster detection of loss-of-synchronization.

For this option, the GMSL serializer and deserializer generate 8-bit enhanced link-verification response values (PJ and PJ') every 16 frames. The host must detect three consecutive PJ/PJ' mismatches before resampling.

Encryption Enable

The GMSL link transfers either encrypted or nonencrypted data. To encrypt data, the host µC sets the encryption enable (ENCRYPTION_ENABLE) bit in both the GMSL serializer and deserializer. The µC must set ENCRYPTION_ENABLE in the same VSYNC cycle in both the GMSL serializer and deserializer (no internal VSYNC falling edges between the two writes). The same timing applies when clearing ENCRYPTION_ENABLE to disable encryption.

Note: ENCRYPTION_ENABLE enables/disables encryption on the GMSL irrespective of the content. To comply with HDCP, the µC must not allow content requiring encryption to cross the GMSL unencrypted.

The µC must complete the authentication process before enabling encryption. In addition, encryption must be disabled before starting a new authentication session.

Synchronization of Encryption

The video vertical sync (VSYNC) synchronizes the start of encryption. Once encryption has started, the GMSL generates a new encryption key for each frame and each line, with the internal falling edge of VSYNC and HSYNC. Rekeying is transparent to data and does not disrupt the encryption of video or audio data.

Repeater Support

The GMSL serializer/deserializer include features to build an HDCP repeater. An HDCP repeater receives and decrypts HDCP content and then encrypts and transmits on one or more downstream links. A repeater can also use decrypted HDCP content (e.g., to display on a screen). To support HDCP repeater-authentication protocol, the HDMI deserializer has a REPEATER register bit. This register bit must be set to 1 by a µC (most likely on the repeater module). Both the GMSL serializer and deserializer use SHA-1 hash-value calculation over the assembled KSV lists. HDCP GMSL links support a maximum of 15 receivers (total number including the ones in repeater modules). If the total number of downstream receivers exceeds 14, the µC must set the MAX_DEVS_EXCEEDED register bit when it assembles the KSV list.

HDCP Authentication Procedures

The GMSL serializer generates a 64-bit random number exceeding the HDCP requirement. The GMSL serializer/deserializer internal one-time programmable (OTP) memories contain a unique HDCP keyset programmed at the factory. The host µC initiates and controls the HDCP authentication procedure. The GMSL serializer and deserializer generate HDCP authentication response values for the verification of authentication. Use the following procedures to authenticate the HDCP GMSL encryption (refer to the HDCP 1.3 Amendment for GMSL for details). The µC must perform link integrity checks while encryption is enabled (see Table 18). Any event that indicates that the deserializer has lost link synchronization should retrigger authentication. The µC must first write 1 to the RESET_HDCP bit in the GMSL serializer before starting a new authentication attempt.

HDCP Protocol Summary

Table 18, Table 19, and Table 20 list the summaries of the HDCP protocol. These tables serve as an implementation guide only. Meet the requirements in the GMSL amendment for HDCP to be in full compliance.

GMSL HDMI HDCP Protocol Summary

After initial setup of the HDMI PWD registers (device address 0x30), the device automatically performs required functions needed when the HDMI source runs the first part of authentication, encryption enable/disable, and link integrity checks. During the second part of authentication, the microcontroller enters the downstream topology, populates the KSV list, triggers SHA calculation and sets the HDMI receiver's KSV_READY bit (Table 21). The HDMI source then verifies the SHA calculation and checks the KSV list against the revocation list to complete the second part of authentication.

Example Repeater Network—Three µCs

The example shown in Figure 38 has two repeaters and three µCs. Table 21 summarizes the authentication operation.

Detection and Action Upon New Device Connection

When a new device is connected to the system, the device must be authenticated and the device's KSV checked against the revocation list. The downstream µCs can set the NEW_DEV_CONN bit of the upstream receiver and invoke an interrupt to notify upstream µCs.

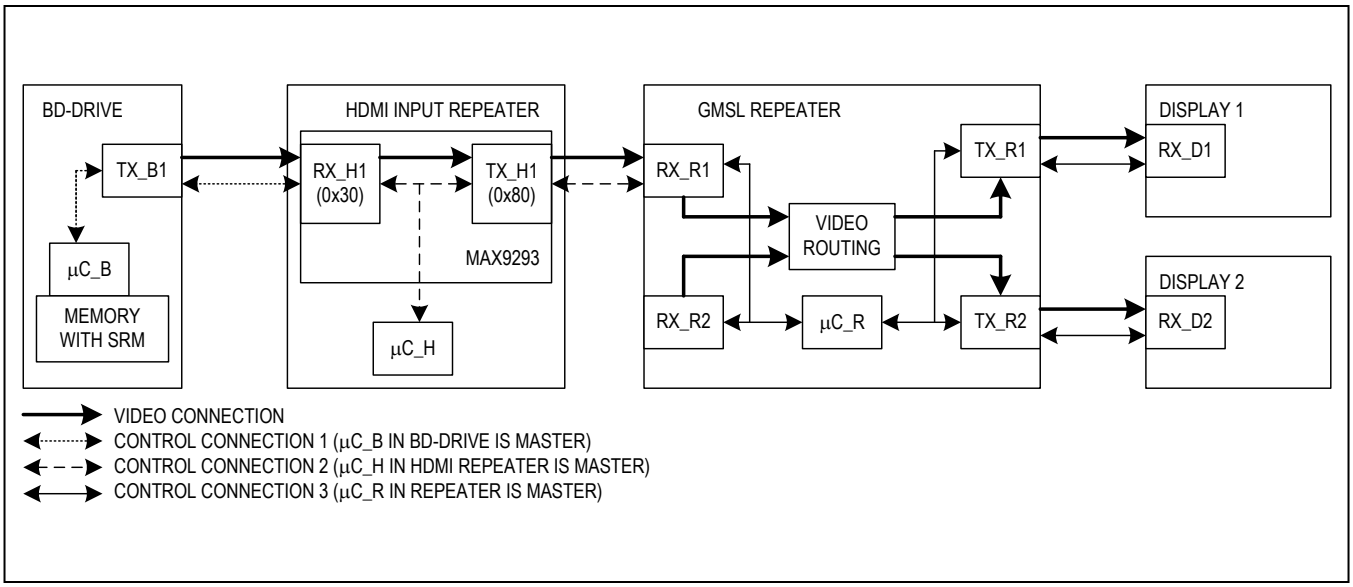


Figure 38. Example Repeater Network—Three µCs

Table 18. Startup, HDCP Authentication, and Normal Operation (Deserializer is Not a Repeater)—First Part of the HDCP Authentication Protocol

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	Initial state after power-up.	Powers up waiting for HDCP authentication.	Powers up waiting for HDCP authentication.
2	Makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, uses the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer to mask A/V data at the input of the GMSL serializer. Starts the link by writing SEREN = H or link starts automatically if AUTOS is low.	—	—
3	—	Starts serialization and transmits low-value content A/V data.	Locks to incoming data stream and outputs low-value content A/V data.
4	Reads the locked bit of the deserializer and makes sure the link is established.	—	—
5	Optionally writes a random-number seed to the GMSL serializer.	Combines seed with internally generated random number. If no seed provided, only internal random number is used.	—
6	If HDCP encryption is required, starts authentication by writing 1 to the START_AUTHENTICATION bit of the GMSL serializer.	Generates (stores) AN, and resets the START_AUTHENTICATION bit to 0.	—

Table 18. Startup, HDCP Authentication, and Normal Operation (Deserializer is Not a Repeater)—First Part of the HDCP Authentication Protocol (continued)

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
7	Reads AN and AKSV from the GMSL serializer and writes to the deserializer.	—	Generates R0' triggered by the µC's write of AKSV.
8	Reads the BKSV and REPEATER bit from the deserializer and writes to the GMSL serializer.	Generates R0, triggered by the µC's write of BKSV.	—
9	Reads the INVALID_BKSV bit of the GMSL serializer and continues with authentication if it is 0. Authentication can be restarted if it fails (set RESET_HDCP = 1 before restarting authentication).	—	—
10	Reads R0' from the deserializer and reads R0 from the GMSL serializer. If they match, continues with authentication; otherwise, retries up to two more times (optionally, GMSL serializer comparison can be used to detect if R0/R0' match). Authentication can be restarted if it fails (set RESET_HDCP = 1 before restarting authentication).	—	—
11	Waits for the VSYNC falling edge (internal to the GMSL serializer) and then sets the ENCRYPTION_ENABLE bit to 1 in the deserializer and GMSL serializer (if the FC is not able to monitor VSYNC, it can utilize the VSYNC_DET bit in the GMSL serializer).	Encryption enabled after the next VSYNC falling edge.	Decryption enabled after the next VSYNC falling edge.
12	Checks that BKSV is not in the Key Revocation list and continues if it is not. Authentication can be restarted if it fails. **Note:** Revocation list check can start after BKSV is read in step 8.	—	—
13	Starts transmission of A/V content that needs protection.	Performs HDCP encryption on high-value content A/V data.	Performs HDCP decryption on high-value content A/V data.

Table 19. Link Integrity Check (Normal)—Performed Every 128 Frames After Encryption is Enabled

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	—	Generates Ri and updates the RI register every 128 VSYNC cycles.	Generates Ri' and updates the RI' register every 128 VSYNC cycles.
2	—	Continues to encrypt and transmit A/V data.	Continues to receive, decrypt, and output A/V data.
3	Every 128 video frames (VSYNC cycles) or every 2s.	—	—
4	Reads RI from the GMSL serializer.	—	—
5	Reads RI' from the deserializer.	—	—
6	Reads RI again from the GMSL serializer and makes sure it is stable (matches the previous RI that it has read from the GMSL serializer). If RI is not stable, go back to step 5.	—	—
7	If RI matches RI', the link integrity check is successful; go back to step 3.	—	—
8	If RI does not match RI', the link integrity check fails. After the detection of failure of link integrity check, the FC makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer can be used to mask A/V data input of the GMSL serializer.	—	—
9	Writes 0 to the ENCRYPTION_ENABLE bit of the GMSL serializer and deserializer.	Disables encryption and transmits low-value content A/V data.	Disables decryption and outputs low-value content A/V data.
10	Restarts authentication by writing 1 to the RESET_HDCP bit followed by writing 1 to the START_AUTHENTICATION bit in the GMSL serializer.	—	—

Table 20. Optional Enhanced Link Integrity Check—Performed Every 16 Frames After Encryption is Enabled

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	—	Generates PJ and updates the PJ register every 16 VSYNC cycles.	Generates PJ' and updates the PJ' register every 16 VSYNC cycles.
2	—	Continues to encrypt and transmit A/V data.	Continues to receive, decrypt, and output A/V data.
3	Every 16 video frames, reads PJ from the GMSL serializer and PJ' from the deserializer.	—	—
4	If PJ matches PJ', the enhanced link integrity check is successful; go back to step 3.	—	—
5	If there is a mismatch, retry up to two more times from step 3. Enhanced link integrity check fails after 3 mismatches. After the detection of failure of enhanced link integrity check, the µC makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer can be used to mask A/V data input of the GMSL serializer.	—	—
6	Writes 0 to the ENCRYPTION_ENABLE bit of the GMSL serializer and deserializer.	Disables encryption and transmits low-value content A/V data.	Disables decryption and outputs low-value content A/V data.
7	Restarts authentication by writing 1 to the RESET_HDCP bit followed by writing 1 to the START_AUTHENTICATION bit in the GMSL serializer.	—	—

Table 21. HDCP Authentication and Normal Operation (Two Repeaters)—First and Second Parts of the HDCP Authentication Protocol

NO.	HDMI SOURCE (µC_B, TX_B1)	µC_H	MAX9293 HDMI INPUT GMSL SERIALIZER (RX_H1, TX_H1)	HDCP GMSL REPEATER AND DOWNSTREAM DEVICES (RX_R1, µC_R, etc.)
1	Initial state after power-up.	Initial state after power-up.	All: Power-up waiting for HDCP authentication.	All: Power-up waiting for HDCP authentication.
2	—	Writes REPEATER = 1 in RX_H1. Retries until proper acknowledge frame received. **Note:** This step must be completed before the first part of authentication is started between TX_B1 and RX_H1 by the µC_B (step 7). For example, to satisfy this requirement, write the REPEATER bit before enabling DDC or setting HPD output.	—	µC_R sets up RX_R1 as a repeater. **Note:** This step must be completed before the first part of authentication is started between TX_H1 and RX_R1
3	Makes sure that A/V data not requiring protection (low-value content) is available from TX_B1 (such as blue or informative screen).	—	RX_H1: Locks to incoming data stream.	
4	—	Starts downstream link by writing SEREN = H to TX_H1, or links start automatically if AUTOS of transmitters are low.	TX_H1: Starts serialization and transmits low-value content A/V data.	µC_R starts all downstream links. all links are locked and outputs low-value content A/V data.
5	Ensures the link between TX_B1 and RX_H1 is established.	Reads the locked bit of RX_R1 and makes sure the link between TX_H1 and RX_R1 is established.	—	µC_R makes sure the downstream links are established.
6	—	Sets up authentication interrupts (Register 0x50)	—	Writes 1 to the GPIO_0_FUNCTION and GPIO_1_FUNCTION bits in RX_R1 to change GPIO functionality used for HDCP purpose
7	Starts and completes the first part of the authentication protocol between TX_B1, RX_H1	—	RX_H1: According to commands from µC_B, computes R0'.	Waits for authentication start from upstream devices

Table 21. HDCP Authentication and Normal Operation (Two Repeaters)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	HDMI SOURCE (µC_B, TX_B1)	µC_H	MAX9293 HDMI INPUT GMSL SERIALIZER (RX_H1, TX_H1)	HDCP GMSL REPEATER AND DOWNSTREAM DEVICES (RX_R1, µC_R, etc.)
8	—	When authentication start interrupt is detected, starts and completes the first part of the authentication protocol between the TX_H1, RX_R1 links (see steps 6–10 in Table 18).	TX_H1: According to commands from µC_R, generates AN, computes R0.	RX_H1: According to commands from µC_B, computes R0'. µC_R : When GPIO_1 = 1 is detected, starts and completes the first part of the authentication protocol for downstream links
9	Enables encryption on the (TX_B1, RX_H1) link. Full authentication is not complete yet so it makes sure A/V content that needs protection is not transmitted. Since REPEATER = 1 was read from RX_H1, the second part of authentication is required.	—	RX_H1: Decryption enabled.	—
10	—	Waits until authentication done interrupt is detected. Then waits for the VSYNC falling edge (polling VSYNC_DET in TX_H1) sets the ENCRYPTION_ENABLE = 1 in TX_H1.	TX_H1: Encryption enabled after next VSYNC falling edge.	RX_R1: Decryption enabled after next VSYNC falling edge. µC_R: When GPIO_0 = 1 is detected, enables encryption on downstream links.
11	Waits for some time to allow µC_H to make the KSV list ready in RX_H1. Then polls (reads) the KSV_LIST_READY bit of RX_H1 regularly until bit is read as 1.	Waits for some time to allow µC_R to make the KSV list ready in RX_R1. Then polls (reads) the KSV_LIST_READY bit of RX_R1 regularly until bit is read as 1.	—	µC_R: Performs second part of authentication. Stores KSV list and KSV_READY = 1 to RX_R1. RX_R1: calculates hash value (V')
12	—	Reads the KSV list and BINFO from RX_R1 and writes them to TX_H1. If any of the MAX_DEVS_EXCEEDED or MAX_CASCADE_EXCEEDED bits is 1, then authentication fails. **Note:** BINFO must be written after the KSV list.	TX_H1: Triggered by µC_H's write of BINFO, calculates hash value (V) on the KSV list, BINFO and the secret-value M0	—
13	—	Reads V from TX_H1 and V' from RX_R1. If they match, continues with authentication; otherwise, retries up to two more times.	—	—

Table 21. HDCP Authentication and Normal Operation (Two Repeaters)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	HDMI SOURCE (µC_B, TX_B1)	µC_H	MAX9293 HDMI INPUT GMSL SERIALIZER (RX_H1, TX_H1)	HDCP GMSL REPEATER AND DOWNSTREAM DEVICES (RX_R1, µC_R, etc.)
14	—	Appends BKSV from RX_R1 to the KSV list. Writes the appended KSV list, list length, list start pointer, and BINFO to RX_H1 and triggers SHA calculation.	RX_H1: calculates hash value (V') on the KSV list, BINFO and the secret-value M0'	—
15	—	Writes 1 to the KSV_LIST_ READY bit of RX_H1.	—	—
16	Reads the KSV list and BINFO from RX_H1. If any of the PT_CASC_EXCEED or DEVS_EXCEEDED bits is 1, then authentication fails.	—	—	—
17	Reads V from TX_B1 and V' from RX_H1. If they match, continues with authentication; otherwise, retries up to two more times.	—	—	—
18	Searches for each KSV in the KSV list and BKSV of RX_H1 in the Key Revocation list.	—	—	—
19	If keys are not revoked, the second part of the authentication protocol is completed.	—	—	—
20	Starts transmission of A/V content that needs protection.	—	All: Perform HDCP encryption on high-value A/V data.	All: Perform HDCP decryption on high-value A/V data.

Notification of Start of Authentication and Enable of Encryption to Downstream Links

HDCP repeaters do not immediately begin authentication upon startup or detection of a new device, but instead wait for an authentication request from the upstream transmitter/repeaters.

Use the following procedure to notify downstream links of the start of a new authentication request:

1) HDMI µC begins authentication with the HDCP repeater's input receiver.
2) When HDMI authentication starts, the HDCP repeater's HDMI input receiver, HDCP_AUTH_START_INTR interrupt triggers (if interrupts are set).
3) HDCP repeater's µC waits for the HDCP_AUTH_START_INTR interrupt starts authentication downstream.

Set HDCP_AUTH_DONE_INTR interrupt and then poll the HDCP_DECRYPTING bit to follow encryption enable from the HDMI Transmitter.

Applications Information

Self-PRBS Test

The serializers include a PRBS pattern generator that works with bit-error verification in the deserializer. To run the PRBS test, first disable HDCP encryption. Next, set DISHSFILT, DISVSFILT and DISDEFILT to 1, to disable glitch filter in the deserializer. Then, set PRBSEN = 1 (0x04, D5) in the serializer and then in the deserializer. To exit the PRBS test, set PRBSEN = 0 (0x04, D5) in the deserializer and then in the serializer.

Dual µC Control

Usually, systems have one microcontroller to run the control channel, located on the serializer side for display applications or on the deserializer side for image-sensing applications. However, a µC can reside on each side simultaneously, and trade off running the control channel. In this case, each µC can communicate with the serializer and deserializer and any peripheral devices.

Contention will occur if both µCs attempt to use the control channel at the same time. It is up to the user to prevent this contention by implementing a higher level protocol. In addition, the control channel does not provide arbitration between I^2C masters on both sides of the link. An acknowledge frame is not generated when communication fails due to contention. If communication across the serial link is not required, the µCs can disable the forward and reverse control channel using the FWDCCEN and REVCCEN bits (0x04, D[1:0]) in the serializer/deserializer. Communication across the serial link is stopped and contention between µCs cannot occur.

As an example of dual µC use in an image-sensing application, the serializer can be in sleep mode and waiting for wake-up by µC on the deserializer side. After wake-up, the serializer-side µC assumes master control of the serializer's registers.

RXC_ Spread Tracking

The serializers can operate with a spread RXC_ signal. Do not exceed 0.5% spread for $f_{RXC_}$ > 50MHz, and 1% spread for $f_{RXC_}$ < 50MHz, and keep modulation less than 40kHz. In addition, turn off spread spectrum in the serializer and deserializer. The serializer and deserializer track the spread on RXC_.

Table 22. MAX9291/MAX9293 Feature Compatibility

MAX9291/MAX9293 FEATURES	GMSL DESERIALIZER
High-bandwidth mode	If feature not supported in deserializer, must only use 32-bit mode.
I^2C to I^2C	If feature not supported in deserializer, must use UART to I^2C or UART to UART.
Coax	If feature not supported in deserializer, must connect unused serial input through 200nF and 50Ω in series to V_{DD} and set the reverse control channel amplitude to 100mV.
High-immunity control channel	If feature not supported in deserializer, must use the legacy reverse control channel mode.
TDM encoding	If feature not supported in deserializer, must use I^2S encoding (with 50% WS duty cycle),if supported.
I^2S encoding	If feature not supported in deserializer, must disable I^2S in the MAX9291/MAX9293.
HDCP (MAX9293 only)	If feature not supported in deserializer, must not be turned on in the MAX9293.

Changing the Clock Frequency

It is recommended that the serial link be enabled after the video clock ($f_{RXC_}$) and the control-channel clock ($f_{UART}/f_{\mu C}$) are stable. When changing the clock frequency, stop the video clock for 5µs, apply the clock at the new frequency, then restart the serial link or toggle SEREN. On-the-fly changes in clock frequency are possible if the new frequency is immediately stable and without glitches. The reverse control channel remains unavailable for 500µs after serial link start or stop. When using the UART interface, limit on-the-fly changes in f_{UART} to factors of less than 3.5 at a time to ensure that the device recognizes the UART sync pattern. For example, when lowering the UART frequency from 1Mbps to 100kbps, first send data at 333kbps then at 100kbps for reduction ratios of 3 and 3.333, respectively.

Fast Detection of Loss of Synchronization

A measure of link quality is the recovery time from loss of synchronization. The host can be quickly notified of loss-of-lock by connecting the deserializer's LOCK output to the GPI input. If other sources use the GPI input, such as a touch-screen controller, the µC can implement a routine to distinguish between interrupts from loss-of-sync and normal interrupts. Reverse control-channel communication does not require an active forward link to operate and accurately tracks the LOCK status of the GMSL link. LOCK asserts for video link only and not for the configuration link.

Providing a Frame Sync (Camera Applications)

The GPI/GPO provide a simple solution for camera applications that require a frame sync signal from the ECU (e.g., surround view systems). Connect the ECU frame sync signal to the GPI input, and connect GPO output to the camera frame sync input. GPI/GPO has a typical delay of 275µs. Skew between multiple GPI/GPO channels is typically 115µs. If a lower skew signal is required, connect the camera's frame sync input one of the deserializer's GPIOs and use an I^2C broadcast write command to change the GPIO output state. This has a maximum skew of 0.5µs + 1 I^2C bit time.

Selection and Programming of the Device Addresses

The serializers and deserializers have selectable and programmable device addresses. This allows multiple GMSL devices, along with I^2C peripherals, to coexist on the same control channel.

GMSL Registers Device Address

The serializer GMSL device address is in register 0x00 of each device, while the deserializer device address is in register 0x01 of each device (see Table 26). ADD_ pins set the default GMSL register device address To change a device address, first write to the device whose address changes (register 0x00 of the serializer for serializer GMSL device address change, or register 0x01 of the deserializer for deserializer device address change). Then write the same address into the corresponding register on the other

Table 23. Line-Fault Mapping

REGISTER ADDRESS	BITS	NAME	VALUE	LINE-FAULT TYPE
0x08	D[3:2]	LFNEG	00	Negative cable wire shorted to supply voltage
			01	Negative cable wire shorted to ground
			10	Normal operation
			11	Negative cable wire disconnected
	D[1:0]	LFPOS	00	Positive cable wire shorted to supply voltage
			01	Positive cable wire shorted to ground
			10	Normal operation
			11	Positive cable wire disconnected

Table 24. Suggested Connectors and Cables for GMSL

VENDOR	CONNECTOR	CABLE	TYPE
Rosenberger	59S2AX-400A5-Y	Dacar 302	Coax
Rosenberger	D4S10A-40ML5-Z	Dacar 538	STP
Nissei	GT11L-2S	F-2WME AWG28	STP
JAE	MX38-FF	A-BW-Lxxxxx	STP

device (register 0x00 of the deserializer for serializer GMSL device address change, or register 0x01 of the serializer for deserializer device address change).

HDMI Registers Device Address

Register device addresses for the HDMI registers (see Table 28, Table 29, Table 30, Table 31, Table 32, Table 33, Table 34, and Table 35) can be changed by using this procedure:

1) Choose ADD pins such that GMSL register bank is not conflicting with any other device on the bus. ADD pins do not affect default addresses of HDMI register banks.
2) HDMI has nine register banks and a bank for PHY registers and out of these nine, AON controls the addresses of the remaining eight register banks. Unlike the rest, PHY register bank's address(10th bank) is not register programmable but has only two alternative addresses (0x64, 0x66), which are selectable by the I2C_PAGE_ADDR_CTRL bit in GMSL.
    a. If AON has a conflict, the same GMSL register bit used for selecting the alternative address of PHY bank (I2C_PAGE_ADDR_CTRL) is used to change default address of AON page from 0x60 to 0x62. If both of these addresses conflict, go to step 3.
    b. If AON does not have a conflict, programming registers in AON sets all other eight register bank's addresses.
3. If both possible addresses 0x60 and 0x62 of AON bank conflicts then the conflicting device needs to be powered down and the device address for AON needs to be changed to any desired value by setting registers in AON register bank. Go to 2.b.

3-Level Configuration Inputs

ADD[1:0] and BWS are 3-level inputs that control the serial interface configuration and power-up defaults. Connect 3-level inputs through a pullup resistor to IOVDD to set a high level, a pulldown resistor to GND to set a low level, or open to set a mid level. For digital control, use three-state logic to drive the 3-level logic input.

Configuration Blocking

The serializers can block changes to registers. Set CFGBLOCK to make registers 0x00 to registers 0x1F as read only. Once set, the registers remain blocked until the supplies are removed or until $\overline{PWDN}$ is low.

Compatibility with Other GMSL Devices

The serializers are designed to pair with the MAX9276–MAX9290 deserializers but interoperates with any GMSL serializers. See Table 22 for operating limitations.

HS/VS/DE Inversion

The serializer uses an active high HS, VS, and DE for encoding and HDCO encryption. Set INVHSYNC, INVVSYNC, and INVDE in the serializer (registers 0x0D, 0x0E) to invert active low input signals for use with the GMSL devices. Set INVHSYNC, INVVSYNC, and INVDE in the deserializer (register 0x0E) to output active-low signals for use with downstream devices.

WS/SCK Inversion

The serializer uses standard polarities for I^2S. Set INVWS, INVSCK in the serializer (register 0x1B) to invert opposite polarity signals for use with the GMSL devices. Set INVWS, INVSCK in the deserializer (register 0x1D) to output reverse polarity signals for downstream use.

Line-Fault Detection

The line-fault detector in the serializer monitors for line failures such as short to ground, short to battery, and open link for system fault diagnosis. Figure 4 shows the required external resistor connections. $\overline{LFLT}$ = low when a line fault is detected and $\overline{LFLT}$ goes high when the line returns to normal. The line-fault type is stored in 0x08 D[3:0] of the serializer. Filter $\overline{LFLT}$ with the µC to reduce the detector's susceptibility to short ground shifts. The fault detector threshold voltages are referenced to the serializer ground. Additional passive components set the DC level of the cable (Figure 4). If the serializer and GMSL deserializer grounds are different, the link DC voltage during normal operation can vary and cross one of the fault-detection thresholds.

For the fault-detection circuit, select the resistor's power rating to handle a short to the battery. In coax mode, leave the unused line-fault inputs unconnected. To detect the short-together case, refer to *Application Note 4709: MAX9259 GMSL Line Fault Detection*.

Table 19 lists the mapping for line-fault types.

Internal Input Pulldowns

The control and configuration inputs (except 3-level inputs) include a pulldown resistor to GND. External pulldown resistors are not needed.

Choosing I²C/UART Pullup Resistors

I²C and UART open-drain lines require a pullup resistor to provide a logic-high level. There are tradeoffs between power dissipation and speed, and a compromise may be required when choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times (30% to 70%) for fast mode, which is defined for data rates up to 400kbps (see the I²C specifications in the *AC Electrical Characteristics* table for details). To meet the fast-mode rise-time requirement, choose the pullup resistors so that rise time t_R = 0.85 x R_{PULLUP} x C_{BUS} < 300ns. The waveforms are not recognized if the transition time becomes too slow. The device supports I²C/UART rates up to 1Mbps.

AC-Coupling

AC-coupling isolates the receiver from DC voltages up to the voltage rating of the capacitor. Capacitors at the serializer output and at the deserializer input are needed for proper link operation and to provide protection if either end of the cable is shorted to a battery. AC-coupling blocks low-frequency ground shifts and low-frequency common-mode noise.

Selection of AC-Coupling Capacitors

Voltage droop and the digital sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is fixed, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML/coax receiver termination resistor (R_{TR}), the CML/coax driver termination resistor (R_{TD}), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is (C x (R_{TD} + R_{TR}))/4. R_{TD} and R_{TR} are required to match the transmission line impedance (usually 100Ω differential, 50Ω single ended). This leaves the capacitor selection to change the system time constant. Use at 0.22µF (using legacy reverse control channel), 47nF (using high-immunity reverse control channel), or larger high-frequency surface-mount ceramic capacitors, with sufficient voltage rating to withstand a short to battery, to pass the lower speed reverse control-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower parasitic effects to the high-speed signal.

Power-Supply Circuits and Bypassing

The serializers use an V_{AVDD} and V_{DVDD} of 1.7V to 1.9V. All single-ended inputs and outputs except for the serial output derive power from an V_{IOVDD} of 1.7V to 3.6V, which scale with IOVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

Cables and Connectors

Interconnect for CML typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Coax cables typically have a characteristic impedance of 50Ω. Contact the factory for 75Ω operation. Table 24 lists the suggested cables and connectors used in the GMSL link.

Board Layout

Separate HDMI, CMOS logic signals, and CML/coax high-speed signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, CML/coax, and LVCMOS/HDMI logic signals. Layout PCB traces close to each other for a 100Ω differential characteristic impedance for STP. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together—the impedance goes down when the traces are brought closer. Use a 50Ω trace for the single-ended output when driving coax. Route the PCB traces for differential CML channel in parallel to maintain the differential characteristic impedance.

Avoid vias. Keep PCB traces that make up a differential pair equal length to avoid skew within the differential pair.

ESD Protection

ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. The serial link inputs are rated for ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All pins are tested for the Human Body Model. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 39). The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 40). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 41).

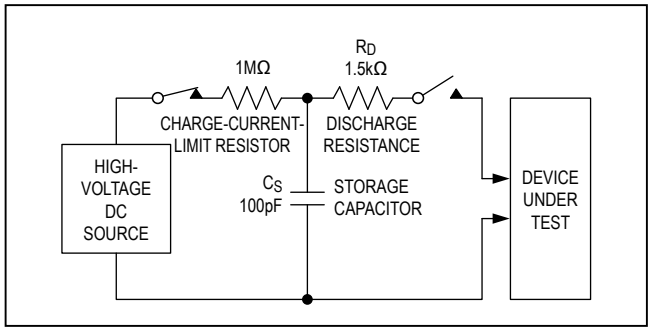


Figure 39. Human Body Model ESD Test Circuit

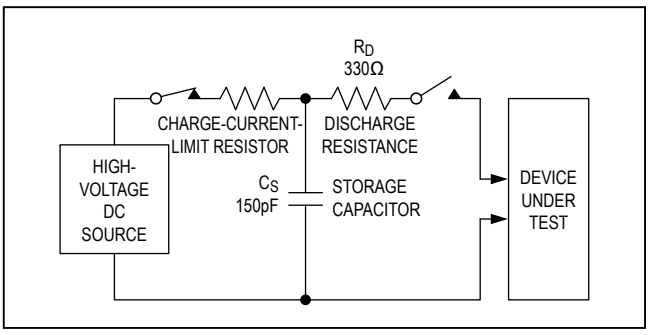


Figure 40. IEC 61000-4-2 Contact Discharge ESD Test Circuit

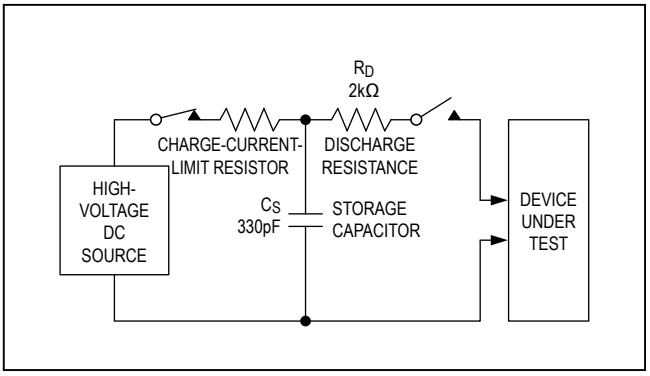


Figure 41. ISO 10605 Contact Discharge ESD Test Circuit

Table 25. Register Table Map

DEFAULT I²C DEVICE ADDRESS	DDC DEVICE ADDRESS	DESCRIPTION
0x60	N/A	AON System Control and Status registers 0x00 to 0x2A: AON System Control and Status 0x70 to 0x93: AON Interrupt Serializer Device Address
0x10	N/A	Audio registers (PWD Domain)
0x30	N/A	HDMI HDCP registers (PWD Domain)
0x4E	N/A	Depacketization-1 register
0xF0	N/A	MHL registers
0xA0	N/A	Video registers (PWD Domain)
0xFE	N/A	EDID Write and Read Accessible registers
0xDE	N/A	Depacketization-2 register
0xE0	N/A	TMDS Bist registers
0x64	N/A	HDMI PHY registers
N/A	0xA0	EDID Read Accessible registers (read-only copy of the EDIC Write and Read Accessible registers)
N/A	0x74	HDMI compliant data map of “HDMI HDCP registers”
0xXX	N/A	GMSL registers (includes GMSL HDCP registers)

Table 26. GMSL Register Table

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:1]	SERADDR	XXXXXXX	Serializer device address (power-up default value depends on latched address pin level)	XX00XX0
	D0	CFGBLOCK	0	Normal operation	0
			1	Registers 0x00 to 0x1F are read only	
0x01	D[7:1]	DESADDR	XXXXXXX	Deserializer device address (power-up default value depends on latched address pin level)	XX01XX0
	D0	—	0	Reserved	0
0x02	D[7:5]	SS	000	No spread spectrum. (Power-up default values depend on values of CONF[1:0] at power-up)	000, 001
			001	±0.5% spread spectrum (Power-up default values depend on values of CONF[1:0] at power-up)	
			010	±1.5% spread spectrum	
			011	±2% spread spectrum	
			100	No spread spectrum	
			101	±1% spread spectrum	
			110	±3% spread spectrum	
			111	±4% spread spectrum	
	D4	AUDIOEN	0	Disable I^2S/TDM channel	1
			1	Enable I^2S/TDM channel	
	D[3:2]	PRNG	00	12.5MHz to 25MHz pixel clock	11
			01	25MHz to 50MHz pixel clock	
			10	50MHz to 104MHz pixel clock	
			11	Automatically detect the pixel clock range	
	D[1:0]	SRNG	00	0.5 to 1Gbps serial bit rate	11
			01	1 to 2Gbps serial bit rate	
			10	2 to 3.12Gbps serial bit rate	
			11	Automatically detect serial bit rate	
0x03	D[7:6]	AUTOFM	00	Calibrate spread modulation rate only once after locking	00
			01	Calibrate spread modulation rate every 2ms after locking	
			10	Calibrate spread modulation rate every 16ms after locking	
			11	Calibrate spread modulation rate every 256ms after locking	
	D[5:0]	SDIV	000000	Auto calibrate sawtooth divider	000000
			XXXXXX	Manual SDIV setting. See Manual Programming of Spread Spectrum Divider section.	

Table 26. GMSL Register Table (continued)

0x04	D7	SEREN	0	Disable serial link. (Power-up default when $\overline{AUTOS}$ = high. Reverse control channel communication remains unavailable for 500µs after the serializer starts/stops the serial link	0, 1
			1	Enable serial link. Power-up default when $\overline{AUTOS}$ = low. Reverse control channel communication remains unavailable for 500µs after the serializer starts/stops the serial link	
	D6	CLINKEN	0	Disable configuration link	0
			1	Enable configuration link	
	D5	PRBSEN	0	Disable PRBS test	0
			1	Enable PRBS test	
	D4	SLEEP	0	Normal mode (power-up default value depends on CDS/CNTL3 and $\overline{AUTOS}$ pin values at power-up).	0, 1
			1	Activate sleep mode. (power-up default value depends on CDS/CNTL3 and $\overline{AUTOS}$ pin values at power-up)	
	D[3:2]	INTTYPE	00	Base mode uses I^2C interface when I2CSEL = 0, CDS = 1	01
			01	Base mode uses UART interface when I2CSEL = 0, CDS = 1	
			1X	Local control channel disabled	
	D1	REVCCEN	0	Disable reverse control channel from deserializer (receiving)	1
			1	Enable reverse control channel from deserializer (receiving)	
	D0	FWDCCEN	0	Disable forward control channel to deserializer (sending)	1
			1	Enable forward control channel to deserializer (sending)	

Table 26. GMSL Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x05	D7	I2CMETHOD	0	I²C conversion sends the register address when converting UART to I²C	0
			1	Disable sending of I²C register address when converting UART to I²C (command-byte-only mode)	
	D6	PRBSTYPE	0	Deserializer uses standard PRBS test	0
			1	Deserializer uses MAX9272 compatible PRBS test	
	D[5:4]	CMLLVL	00	100mV CML twisted-pair output level (see Table 7).	11
			01	200mV CML twisted-pair output level	
			10	300mV CML twisted-pair output level	
			11	400mV CML twisted-pair output level	
	D[3:0]	PREEMP	0000	Preemphasis off	0000
			0001	-1.2dB Preemphasis	
			0010	-2.5dB Preemphasis	
			0011	-4.1dB Preemphasis	
			0100	-6.0dB Preemphasis	
			0101	Do not use	
			0110	Do not use	
			0111	Do not use	
			1000	1.1dB Preemphasis	
			1001	2.2dB Preemphasis	
			1010	3.3dB Preemphasis	
			1011	4.4dB Preemphasis	
			1100	6.0dB Preemphasis	
			1101	8.0dB Preemphasis	
			1110	10.5dB Preemphasis	
			1111	14.0dB Preemphasis	
0x06	D[7:0]	—	01000000	Reserved	01000000
0x07	D[7:0]	—	00100010	Reserved	00100010
0x08	D[7:4]	—	0000	Reserved	0000 (Read only)
	D[3:2]	LFNEG	00	Negative cable wire shorted to supply voltage	10 (Read only)
			01	Negative cable wire shorted to ground	
			10	Normal operation	
			11	Negative cable wire disconnected	
	D[1:0]	LFPOS	00	Positive cable wire shorted to supply voltage	10 (Read only)
			01	Positive cable wire shorted to ground	
			10	Normal operation	
			11	Positive cable wire disconnected	

Table 26. GMSL Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x09	D[7:0]	—	XXXXXXXX	Reserved	(Read only)
0x0A	D[7:0]	—	XXXXXXXX	Reserved	(Read only)
0x0B	D[7:0]	—	XXXXXXXX	Reserved	(Read only)
0x0C	D[7:6]	I2SCFG	00	HDMI audio sent to deserializer only	10
			01	HDMI audio sent out of serializer I^2S only	
			10	HDMI audio sent to both serializer and deserializer I^2S	
			11	Local I^2S audio sent to deserializer	
	D[5:4]	I2STDMCFG	00	Audio uses stereo I^2S	10
			01	Audio uses TDM	
			10	Auto select Audio format	
			11	Do not use	
	D[3:2]	I2SHDRCFG	00	Use auto extracted audio header information	10
			01	Use audio header information programmed in registers AUDHDR_	
			10	No audio header used	
			11	Do not use	
	D1	INVSCK	0	Do not invert SCK input	0
			1	Invert SCK input	
	D0	INVWS	0	Do not invert WS input	0
			1	Invert WS input	

Table 26. GMSL Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x0D	D7	SETGPO	0	Set GPO to output low	0
			1	Set GPO to output high	
	D[6:5]	PRBSLEN	00	Continuous PRBS test length (when using MAX9272 compatible test)	00
			01	9.83Mbits PRBS test length (when using MAX9272 compatible test)	
			10	167.1Mbits PRBS test length (when using MAX9272 compatible test)	
			11	1341.5Mbits PRBS test length (when using MAX9272 compatible test)	
	D4	—	0	Reserved	0
	D3	AUTOCLINK	0	Configuration link enabled only when CLINKEN = 1 and SEREN = 0	0
			1	Automatically enable configuration link if HDMI input is invalid (when SEREN = 1)	
	D2	SELCNTL	0	HDMI CNTL bits sent to deserializer	0
			1	Serializer CNTL bits sent to deserializer	
	D1	AUTOINT	0	INTOUT pin controlled by INTOUTX bit below	1
			1	INTOUT pin controlled by HDMI receiver register settings	
	D0	INTOUTX	0	Drive INTOUT low when AUTOINT = 0	0
			1	Drive INTOUT high when AUTOINT = 0	
0x0E	D[7:2]	-	100000	Reserved	100000
	D1	ENLFLTCXP	0	Disable line fault monitoring on OUT+ in coax mode.	1
			1	Enable line fault monitoring on OUT+ in coax mode. **Power-on default**.	
	D0	ENLFLTCXM	0	Disable line fault monitoring on OUT- in coax mode. **Power-on default**.	0
			1	Enable line fault monitoring on OUT- in coax mode.	
0x0F	D[7:1]	I2CSRCA	XXXXXXX	I²C address translator source A	0000000
	D0	—	0	Reserved	0
0x10	D[7:1]	I2CDSTA	XXXXXXX	I²C address translator destination A	0000000
	D0	—	0	Reserved	0
0x11	D[7:1]	I2CSRCB	XXXXXXX	I²C address translator source B	0000000
	D0	—	0	Reserved	0
0x12	D[7:1]	I2CDSTB	XXXXXXX	I²C address translator destination B	0000000
	D0	—	0	Reserved	0

Table 26. GMSL Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x13	D7	I2CLOCACK	0	Acknowledge not generated when forward channel is not available	1
			1	I^2C to I^2C-slave generates local acknowledge when forward channel is not available	
	D[6:5]	I2CMSTBT	00	352ns/117ns I^2C setup/hold time	01
			01	469ns/234ns I^2C setup/hold time	
			10	938ns/352ns I^2C setup/hold time	
			11	1046ns/469ns I^2C setup/hold time	
	D[4:2]	I2CSLVSH	000	8.47kbps (typ) I^2C to I^2C-master bit rate setting	101
			001	28.3kbps (typ) I^2C to I^2C-master bit rate setting	
			010	84.7kbps (typ) I^2C to I^2C-master bit rate setting	
			011	105kbps (typ) I^2C to I^2C-master bit rate setting	
			100	173kbps (typ) I^2C to I^2C-master bit rate setting	
			101	339kbps (typ) I^2C to I^2C-master bit rate setting	
			110	533kbps (typ) I^2C to I^2C-master bit rate setting	
			111	837kbps (typ) I^2C to I^2C-master bit rate setting	
	D[1:0]	I2CMSTBT	00	64µs (typ) I^2C to I^2C-slave remote timeout	10
			01	256µs (typ) I^2C to I^2C-slave remote timeout	
			10	1024µs (typ) I^2C to I^2C-slave remote timeout	
			11	No I^2C to I^2C-slave remote timeout	
0x14	D[7:4]	CMLLVLCX	0000	Do not use	1010
			0001	50mV CML coax output level	
			0010	100mV CML coax output level	
			0011	150mV CML coax output level	
			0100	200mV CML coax output level	
			0101	250mV CML coax output level	
			0110	300mV CML coax output level	
			0111	350mV CML coax output level	
			1000	400mV CML coax output level	
			1001	450mV CML coax output level	
			1010	500mV CML coax output level	
			1011	Do not use	
			11XX	Do not use	
	D[3:2]	—	00	Reserved	00
	D1	SELVESA	0	Output uses oLDI bitmapping	1
			1	Output uses VESA bitmapping	
	D0	DISRWAKE	0	Enable wake-up receiver (enable remote wakeup	0
			1	Disable wake-up receiver (disable remote wakeup)	

Table 26. GMSL Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x15	D7	DISDETRIG	0	Enable DE trigger of encoded packets in high-bandwidth mode	0
			1	Disable DE trigger of encoded packets in high-bandwidth mode	
	D[6:5]	CNTLTRIG	00	No trigger of encoded CNTL packets in high-bandwidth mode	10
			01	Always trigger encoded CNTL packets in high-bandwidth mode	
			10	Trigger encoded CNTL packets in high-bandwidth mode when DE is low	
			11	Trigger encoded CNTL packets in high-bandwidth mode when HS is low	
	D4	ENREVP	0	Disable reverse channel from positive input with coax cable	1
			1	Enable reverse channel from positive input with coax cable	
	D3	ENREVN	0	Disable reverse channel from negative input with coax cable	0
			1	Enable reverse channel from negative input with coax cable	
	D[2:0]	—	000	Reserved	000
0x16	D7	—	X	Reserved	X
	D[6:5]	COLORMAP	00	Auto detect color map from HDMI source	00
			01	HDMI source is YCC422	
			10	HDMI source is YCC422 muxed	
			11	HDMI source is YCC444 or RGB444	
	D[4:0]	—	XXXXX	Reserved	XXXXX
0x17	D7	HIGHIMM	0	Set reverse channel to legacy mode. (power-up default value depends on HIM pin value at power-up)	0, 1
			1	Set reverse channel to high-immunity mode (power-up default value depends on HIM pin value at power-up)	
	D[6:0]	—	0011111	Reserved	0011111
0x18	D7	FRMINDSEL	0	Do not use HDMI even/odd frame indicator as CNTL1	0
			1	Use HDMI even/odd frame indicator as CNTL1 (when SELCNTL = 0)	
	D6	HDMIAONADDR	0	AON, PHY block uses I^2C addresses 0x60 and 0x64 respectively	0
			1	AON, PHY block uses alternate I^2C addresses 0x62 and 0x66, respectively	
	D[5:0]	—	000000	Reserved	000000

Table 26. GMSL Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x19	D[7:0]	—	01001010	Reserved	01001010
0x1A	D7	REVFAST	0	High-Immunity Reverse Channel Mode uses 500kbps bit rate	0
			1	High-Immunity Reverse Channel Mode uses 1Mbps bit rate	
	D6	—	0	Reserved	0
	D5	MSCNTL0	0	MS functions as MS input	0
			1	MS functions as CNTL0 input (when SELCNTL = 1)	
	D4	CDSCNTL3	0	CDS functions as CDS input	0
			1	CDS functions as CNTL3 input (when SELCNTL = 1)	
	D[3:1]	—	000	Reserved	000
	D0	REVARBTO	0	256µs reverse channel arbitration time out duration (coax splitter mode only)	0
			1	4ms reverse channel arbitration time out duration (coax splitter mode only)	
0x1B	D[7:0]	AUDHDR1	XXXXXXXX	First byte of audio header data (DV, SM, SR1, SR0, SS, Reserved[2:0]). Used when I2SHDRCFG = 01	00000000
0x1C	D[7:0]	AUDHDR2	XXXXXXXX	Second byte of audio header data (C8C, C7C, C6C, C5C, C4C, C3C, C2C, C1C, C0C). Used when I2SHDRCFG = 01	00000000
0x1D	D[7:0]	AUDHDR3	XXXXXXXX	Third byte of audio header data. Used for packed 24-bit samples only when I2SHDRCFG = 01	00000000
0x1E	D[7:0]	DEVID	00101111	Device is a MAX9291 (0x2F)	(Read only)
			00101001	Device is a MAX9293 (0x29)	
0x1F	D[7:6]	—	00	Reserved	00 (Read only)
	D[5:4]	CAPS	00	Not HDCP capable (MAX9291)	(Read only)
			11	HDCP capable (MAX9293)	
	D[3:0]	REVISION	XXXX	Device revision	(Read only)

Table 27. HDCP Register Table (MAX9293 Only)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0x80 to 0x84	5	BKSV	Read/write	HDCP receiver KSV	0x0000000000
0x85 to 0x86	2	RI/RI'	Read/write	RI (read only) of the transmitter when EN_INT_COMP = 0 RI' (read/write) of the receiver when EN_INT_COMP = 1	0x0000
0x87	1	PJ/PJ'	Read/write	PJ (read only) of the transmitter when EN_INT_COMP = 0 PJ' (read/write) of the receiver when EN_INT_COMP = 1	0x00
0x88 to 0x8F	8	AN	Read only	Session random number	(Read only)
0x90 to 0x94	5	AKSV	Read only	HDCP transmitter KSV	(Read only)
0x95	1	ACTRL	Read/write	D7 = PD_HDCP 1 = Power-down HDCP circuits 0 = HDCP circuits normal	0x00
				D6 = EN_INT_COMP 1 = Internal comparison mode 0 = µC comparison mode	
				D5 = FORCE_AUDIO 1 = Force audio data to 0 0 = Normal operation	
				D4 = FORCE_VIDEO 1 = Force video data DFORCE value 0 = Normal operation	
				D3 = RESET_HDCP 1 = Reset HDCP circuits. Automatically set to 0 upon completion. 0 = Normal operation	
				D2 = START_AUTHENTICATION 1 = Start authentication. Automatically set to 0 once authentication starts. 0 = Normal operation	
				D1 = VSYNC_DET 1 = Internal falling edge on VSYNC detected 0 = No falling edge detected	
				D0 = ENCRYPTION_ENABLE 1 = Enable encryption 0 = Disable encryption	

Table 27. HDCP Register Table (MAX9293 Only) (continued)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0x96	1	ASTATUS	Read only	D[7:4] = Reserved	0x00 (Read only)
				D3 = V_MATCHED 1 = V matches V' (when EN_INT_COMP = 1) 0 = V does not match V' or EN_INT_COMP = 0	
				D2 = PJ_MATCHED 1 = PJ matches PJ' (when EN_INT_COMP = 1) 0 = PJ does not match PJ' or EN_INT_COMP = 0	
				D1 = R0_RI_MATCHED 1 = RI matches RI' (when EN_INT_COMP = 1) 0 = RI does not match RI' or EN_INT_COMP = 0	
				D0 = BKSV_INVALID 1 = BKSV is not valid 0 = BKSV is valid	
0x97	1	BCAPS	Read/write	D[7:1] = RESERVED	0x00
				D0 = REPEATER 1 = Set to one if device is a repeater 0 = Set to zero if device is not a repeater	
0x98 to 0x9C	5	ASEED	Read/write	internal random number generator optional seed value	0x0000000000
0x9D to 0x9F	3	DFORCE	Read/write	Forced video data transmitted when FORCE_VIDEO = 1. R[7:0] = DFORCE[7:0] G[7:0] = DFORCE[15:8] B[7:0] = DFORCE[23:16]	0x000000
0xA0 to 0xA3	4	V.H0, V'.H0	Read/write	H0 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xA4 to 0xA7	4	V.H1, V'.H1	Read/write	H1 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000

Table 27. HDCP Register Table (MAX9293 Only) (continued)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0xA8 to 0xAB	4	V.H2, V'.H2	Read/write	H2 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xAC to 0xAF	4	V.H3, V'.H3	Read/write	H3 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xB0 to 0xB3	4	V.H4, V'.H4	Read/write	H4 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xB4 to 0xB5	2	BINFO	Read/write	D[15:12] = Reserved	0x0000
				D11 = MAX_CASCADE_EXCEEDED 1 = Set to one if more than 7 cascaded devices attached 0 = Set to zero if 7 or fewer cascaded devices attached	
				D[10:8] = DEPTH Depth of cascaded devices	
				D7 = MAX_DEVS_EXCEEDED 1 = Set to one if more than 14 devices attached 0 = Set to zero if 14 or fewer devices attached	
				D[6:0] = DEVICE_COUNT Number of devices attached	
0xB6	1	GPMEM	Read/write	General purpose memory byte	0x00
0xB7 to 0xB9	3	—	Read only	Reserved	0x000000
0xBA to 0xFF	70	KSV_LIST	Read/write	List of KSVs downstream repeaters and receivers (Maximum of 14 devices)	All Zero

Table 28. HDMI Audio Register Table (I^2C Address 0x10)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:5]	—	000	Reserved	000
	D4	CTS_HW_SW_SEL	0	Auto-clock-regeneration uses hardware determined CTS value	0
			1	Auto-clock-regeneration uses software determined CTS value	
	D3	N_HW_SW_SEL	0	Auto-clock-regeneration uses hardware determined N value	0
			1	Auto-clock-regeneration uses software determined N value	
	D[2:0]	—	100	Reserved	000
0x03	D[7:0]	N_VALUE_SW [7:0]	XXXXXXXX	Bits [7:0] of Audio clock regeneration N value (effective when REG_N_HW_SW _SEL = 1).	00000000
0x04	D[7:0]	N_VALUE_SW [15:8]	XXXXXXXX	Bits [15:8] of Audio clock regeneration N value (effective when REG_N_HW_SW _SEL = 1).	00000000
0x05	D[7:4]	—	0000	Reserved	0000
	D[3:0]	N_VALUE_SW [19:6]	XXXX	Bits [19:16] of Audio clock regeneration N value (effective when REG_CTS_HW_SW _SEL = 1).	0000
0x09	D[7:0]	CTS_VAL_SW [7:0]	XXXXXXXX	Bits [7:0] of Audio clock regeneration CTS value (effective when REG_CTS_HW_SW _SEL = 1).	00000000
0x0A	D[7:0]	CTS_VAL_SW [15:8]	XXXXXXXX	Bits [15:8] of Audio clock regeneration CTS value (effective when REG_CTS_HW_SW _SEL = 1).	00000000
0x0B	D[7:4]	—	0000	Reserved	0000
	D[3:0]	CTS_VAL_SW [19:6]	XXXX	Bits [19:16] of Audio clock regeneration CTS value (effective when REG_CTS_HW_SW _SEL = 1).	0000
0x29	D[7:6]	—	00	Reserved	00
	D5	HW_MUTE_EN	0	Hardware would repeat the previous good sample (during audio mute)	0
			1	Hardware would do a gradual decrement to 0 (during audio mute)	
	D[4:0]	—	00000	Reserved	00000
0x37	D[7:2]	—	000000	Reserved	000000
	D1	AUDIO_MUTE	0	Do not mute Audio	0
			1	Mute Audio (method determined by HW_MUTE_EN)	
	D0	—	0	Reserved	0

Table 29. HDMI PWD Register Table (I^2C Address 0x30)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0x40	1	INT	Read/write	D[7:2] = Reserved	0x00
				D1 = HDCP_AUTH_START_INTR 0 = No HDCP authentication start interrupt invoked. 1 = HDCP authentication start interrupt invoked. Write a 1 to this bit to clear	
				D0 = HDCP_AUTH_DONE_INTR 0 = No HDCP authentication done interrupt invoked. 1 = HDCP authentication done interrupt invoked. Write a 1 to this bit to clear	
0x50	1	INT_EN	Read/write	D[7:2] = Reserved	0x00
				D1 = HDCP_AUTH_START_INTR_EN 0 = disable HDCP authentication start interrupt. 1 = enable HDCP authentication start interrupt	
				D0 = HDCP_AUTH_DONE_INTR_EN 0 = disable HDCP authentication done interrupt. 1 = enable HDCP authentication done interrupt	
0x8A to 0x8E	5	BKSV	Read only	HDCP receiver KSV	(Read only)
0x8F to 0x90	2	RI’	Read only	Link verification response	(Read only)
0x91 to 0x95	5	AKSV	Read/write	HDCP transmitter KSV	0x0000000000
0x96 to 0x9D	8	AN	Read/write	Session random number	0x0000000000000000
0x9E	1	—	Read/write	D7 = HDMI_CAPABLE (Shadowed in DDC BCAPS register) 1 = Device is HDMI capable 0 = 1 = Device is not HDMI capable	0x00
				D6 = REPEATER 1 = Set to one if device is a repeater 0 = Set to zero if device is not a repeater	
				D5 = FIFO_READY bit cleared when write to last AKSV clears 1 = Set to 1 if KSV list and BINFO is ready 0 = Set to 0 if KSV list or BINFO is not ready	
				D4 = FAST 1 = 400kbps I^2C available 0 = 100kbps I^2C available	
				D[3:0] = Reserved	

Table 29. HDMI PWD Register Table (I^2C Address 0x30) (continued)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0x9F to 0xA0	2	BINFO	Read/write	D[15:13] = BSTATUS bits D12 = HDMI_MODE (Read only) 1 = Receiver is in HDMI mode 0 = Receiver is in DVI mode D11 = RPT_CASC_EXCEED 1 = Set to one if more than seven cascaded devices attached 0 = Set to zero if seven or fewer cascaded devices attached D[10:8] = DEPTH Depth of cascaded devices D7 = DEV_EXCEEDED 1 = Set to one if more than 16 devices attached 0 = Set to zero if 16 or fewer devices attached D[6:0] = DEVICE_COUNT Number of devices attached	0x0000
0xA2	1	BCTRL	Read only	D[7:6] = Reserved D5 = HDCP_DECRYPTING 1 = HDCP is decrypting 0 = HDCP is not decrypting D4 HDCP_AUTHENTICATED 1 = HDCP is Authenticated 0 = HDCP is not Authenticated D[3:0] = Reserved	0x00
0xA3 to 0xA4	2	F_ADDR	Read/write	D[15:10] = Reserved D[9:0] = START_ADDR, KSV FIFO start pointer or pointer to the SHA stack: Pointer to the address within KSV FIFO. When I^2C transaction starts with offset address of 0x38h then HDCP repeater takes over decoding instead of register block. Firmware from the local side allowed to read or write from any location within KSV FIFO. The value in KSV_FIFO_start register points to the start address of the read or write I^2C transaction	0x0000
0xA5 to 0xA6	2	SHA_L	Read/write	D[15:10] = Reserved D[9:0] = SHA_LENGTH Number of KSVs to process in bytes (16 x 5 = 80 byte limit)	0x0000

Table 29. HDMI PWD Register Table (I^2C Address 0x30) (continued)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0xA7	1	SHA_C	Read/write	D[7:3] = Reserved D2 = SHA_MODE 1 = SHA set for downstream use 0 = SHA set for internal use D1 = Reserved D0 = SHA_GO_STAT write a 1 to this bit to begin calculation. SHA_ GO_STAT remains low until the SHA calculation is complete 1 = SHA calculation is done 0 = SHA calculation is not done	0x00
0xA8	1	KSV_F_O	Read/write	D[7:0] = KSV FIFO Output port When the firmware starts a I^2C transaction with the offset address set at 38h the access control will be transferred to the KSV FIFO. The address located inside the “KSV Start Address” register acts as the start offset within the KSV FIFO space. Consecutive I^2C transactions to address 38h will be auto- incremented in the KSV FIFO Address space.	0x00
0xD5 to 0xD6	2	DS_BINFO	Read/write	D[15:13] = Downstream BSTATUS bits D12 = DS_HDMI_MODE (Read only) 1 = Downstream receiver is in HDMI mode 0 = Downstream receiver is in DVI mode D11 = DS_ CASC_EXCEED 1 = Set to one if more than seven cascaded devices attached downstream 0 = Set to zero if seven or fewer cascaded devices attached downstream D[10:8] = DS_DEPTH Depth of downstream cascaded devices D7 = DEV_EXCEEDED 1 = Set to one if the device count is exceeded downstream 0 = Set to zero if the downstream device count is not exceeded D[6:0] = DEVICE_COUNT Number of downstream devices attached	0x0000

Table 29. HDMI PWD Register Table (I^2C Address 0x30) (continued)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0xD7 to 0xDE	8	RX_DS_ MO	Read/write	D[63:0] = Down Stream M0 bits	0x0000000000000000
0xDF to 0xE2	4	RX_VH0	Read/write	H0 part of SHA-1 hash value	0x00000000
0xE3 to 0xE6	4	RX_VH1	Read/write	H1 part of SHA-1 hash value	0x00000000
0xE7 to 0xEA	4	RX_VH2	Read/write	H2 part of SHA-1 hash value	0x00000000
0xEB to 0xEE	4	RX_VH3	Read/write	H3 part of SHA-1 hash value	0x00000000
0xEF to xF2	4	RX_VH4	Read/write	H4 part of SHA-1 hash value	0x00000000

Table 30. HDMI Depacketization Register Table (I^2C Address 0x4E)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x22	D[7:1]	—	0000000	Reserved	0000000
	D0	VIDEO_MUTE	0	Do not mute video	0
			1	Video muted (0 output from HDMI)	

Table 31. HDMI Always On (AON) Register Table (I^2C Address 0x60 or 0x62)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x05	D[7:5]	—	000	Reserved	000
	D4	SW_RST_AUTO	0	Manual software reset	1
			1	Auto software reset whenever SCDT = 0	
	D[3:0]	—	0000	Reserved	0000
0x09	D[7:5]	—	100	Reserved	100
	D4	DDC_EN	0	DDC communication disabled	0
			1	Enable DDC communication	
	D[3:0]	—	0000	Reserved	0000
0x0C	D[7:4]	—	0000	Reserved	0000 (Read only)
	D3	HDMI_TX_CONNECTION	0	HSPD input is low	0 (Read only)
			1	HSPD input is high	
	D[2:1]	—	00	Reserved	00 (Read only)
	D0	SCDT	0	Valid HDMI sync not detected	0 (Read only)
			1	Valid HDMI sync detected	

Table 31. HDMI Always On (AON) Register Table (I^2C Address 0x60 or 0x62) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x20	D[7:2]	SLAVE_ADDR_AON	XXXXXX	MSBs D[7:2] of the HDMI AON page's programmable I^2C slave address. Bit D1 of the AON page's I^2C address is determined by HDMI_AON_ADDR (D0 is the R/$\overline{W}$ bit)	011000
	D[1:0]	—	00	Reserved	00
0x21	D[7:1]	SLAVE_ADDR_MHL	XXXXXXX	HDMI MHL page programmable I^2C slave address.	1111000
	D0	—	0	Reserved	0
0x24	D[7:1]	SLAVE_ADDR_AUDIO	XXXXXXX	HDMI audio page programmable I^2C slave address.	0001000
	D0	—	0	Reserved	0
0x25	D[7:1]	SLAVE_ADDR_VIDEO	XXXXXXX	HDMI video page programmable I^2C slave address.	1010000
	D0	—	0	Reserved	0
0x26	D[7:1]	SLAVE_ADDR_EDID	XXXXXXX	HDMI EDID page programmable I^2C slave address.	1111111
	D0	—	0	Reserved	0
0x27	D[7:1]	SLAVE_ADDR_DEPACK1	XXXXXXX	HDMI depacketization 1 page programmable I^2C slave address.	0100111
	D0	—	0	Reserved	0
0x28	D[7:1]	SLAVE_ADDR_DEPACK2	XXXXXXX	HDMI depacketization 2 page programmable I^2C slave address.	1101111
	D0	—	0	Reserved	0
0x29	D[7:1]	SLAVE_ADDR_PWD	XXXXXXX	HDMI PWD page programmable I^2C slave address.	0011000
	D0	—	0	Reserved	0
0x2A	D[7:1]	SLAVE_ADDR_TBIST	XXXXXXX	HDMI TMDS BIST page programmable I^2C slave address.	1110000
	D0	—	0	Reserved	0
0x70	D[7:1]	—	0000000	Reserved	0000000 (Read only)
	D0	INTR	0	Interrupt is not active	0 (Read-only)
			1	Interrupt is active	
0x79	D[7:4]	—	0000	Reserved	0000
	D3	SOFT_INTR_EN	0	Do not trigger software interrupt	0
			1	Trigger software interrupt until SOFT_INTR_EN is cleared	
	D2	—	0	Reserved	0
	D1	INTR_POLARITY	0	INTOUT output set to 1 when interrupt is asserted	0
			1	INTOUT output set to 0 when interrupt is asserted	
	D0	—	0	Reserved	0

Table 31. HDMI Always On (AON) Register Table (I^2C Address 0x60 or 0x62) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x80	D[7:6]	—	00	Reserved	00
	D5	SW_INDUCED_INTR	0	Software-induced interrupt not asserted	0
			1	Software-induced interrupt asserted. Write 1 to SW_INDUCED_INTR to clear	
	D4	—	0	Reserved	0
	D3	SW_DETECT_INTR	0	Sync-detect interrupt not asserted	0
			1	Sync-detect interrupt asserted (Valid HDMI sync signal is detected). Write 1 to SYNC_ DETECT_INTR to clear (for the change of sync detect when going from 1 to 0 to be effective, SW_RST_AUTO should be programmed to 1.)	
	D[2:0]	—	000	Reserved	000
0x81	D[7:1]	—	0000000	Reserved	0000000
	D0	HSPD_UNPLUG_INTR	0	No HDMI cable unplug interrupt asserted	0
			1	HDMI cable unplug interrupt asserted (HSPD falling and rising edge detected). Write a 1 to HSPD_UNPLUG_INTR to clear. (To be effective when there is no valid HDMI input, set SW_RST_AUTO = 1.)	
0x83	D[7:2]	—	000000	Reserved	000000
	D1	HSPD_PLUGGED_INTR	0	No HDMI cable plugged-in interrupt asserted	0
			1	HDMI cable plugged-in interrupt asserted (HSPD rising edge detected). Write a 1 to HSPD_PLUGGED_INTR to clear. (To be effective when there is no valid HDMI input, set SW_RST_AUTO = 1.)	
	D0	—	0	Reserved	0
0x90	D[7:6]	—	00	Reserved	00
	D5	SW_INDUCED_IN_EN	0	Software-induced interrupts disabled	0
			1	Enable software-induced interrupts	
	D4	—	0	Reserved	0
	D3	SYNC_DETECT_INTR_EN	0	HDMI sync-detect interrupts disabled	0
			1	Enable sync-detect interrupts	
	D[2:0]	—	000	Reserved	000
0x91	D[7:1]	—	0000000	Reserved	0000000
	D0	HSPD_UNPLUG_INTR_EN	0	HDMI cable unplug interrupts disabled	0
			1	HDMI cable unplug interrupts enabled	
0x93	D[7:2]	—	000000	Reserved	000000
	D1	HSPD_PLUGGED_INTR_EN	0	HDMI cable plugged-in interrupts disabled	0
			1	HDMI cable plugged-in interrupts enabled	
	D0	—	0	Reserved	0

Table 32. HDMI PHY Register Table (I²C Address 0x64 or 0x62)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x82	D[7:5]	—	000	Reserved	000
	D[4:2]	TERM_CNTL	000	50Ω termination set to 65Ω (nominal)	010
			001	50Ω termination set to 60Ω (nominal)	
			010	50Ω termination set to 55Ω (nominal)	
			011	50Ω termination set to 50Ω (nominal)	
			100	50Ω termination set to 45Ω (nominal)	
			101	Do not use	
			110	Do not use	
			111	Do not use	
	D[1:0]	TERM_SEL	00	HDMI uses 50Ω termination	00
			01	HDMI uses 50Ω data termination and 100Ω clock termination (dual link)	
			10	HDMI uses 3kΩ termination (hot plugging)	
			11	HDMI termination open	

Table 33. HDMI Video Register Table (I²C Address 0xA0)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x48	D7	INVERT_ VSYNC	0	Do not invert TMDS decoded VSYNC	0
			1	Invert TMDS decoded VSYNC	
	D6	INVERT_ HSYNC	0	Do not invert TMDS decoded HSYNC	0
			1	Invert TMDS decoded HSYNC	
	D[5:3]	—	000	Reserved	000
	D2	YCBCR2RGB_ MODE	0	YCbCr Color space conversion uses BT601	0
			1	YCbCr Color space conversion uses BT709	
	D1	—	0	Reserved	0
	D0	RGB2YCBCR_ MODE	0	RGB color space use BT601 conversion	0
			1	RGB color space use BT709 conversion	
0x49	D[7:3]	—	00000	Reserved	00000
	D2	EN_ YCBCR2RGB	0	Disable YCbCr to RGB conversion	0
			1	Enable YCbCr to RGB conversion	
	D[1:0]	—	00	Reserved	00

Table 33. HDMI Video Register Table (I²C Address 0xA0) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x4A	D[7:4]	—	0000	Reserved	0000
	D3	EN_ RGB2YCBCR	0	Disable RGB to YCbCr conversion	0
			1	Enable RGB to YCbCr conversion	
	D2	EN_UP_ SAMPLE	0	Disable 4:2:2 to 4:4:4 chroma up sampler	0
			1	Enable 4:2:2 to 4:4:4 chroma up sampler	
	D1	EN_DOWN_ SAMPLE	0	Disable 4:4:4 to 4:2:2 chroma down sampler	0
			1	Enable 4:4:4 to 4:2:2 chroma down sampler	
	D0	—	0	Reserved	0
0xBC	D[7:6]	OCLKDIV	00	HDMI output clock uses divide by 1	00
			01	HDMI output clock uses divide by 2	
			10	Do not use	
			11	HDMI output clock uses divide by 4	
	D[5:4]	ICLK	00	HDMI input uses 1x clock (no pixel replication)	00
			01	HDMI input uses 2x clock (pixels sent twice)	
			10	Do not use	
			11	HDMI input uses 4x clock (pixels sent four times)	
	D[3:0]	—	0000	Reserved	0000

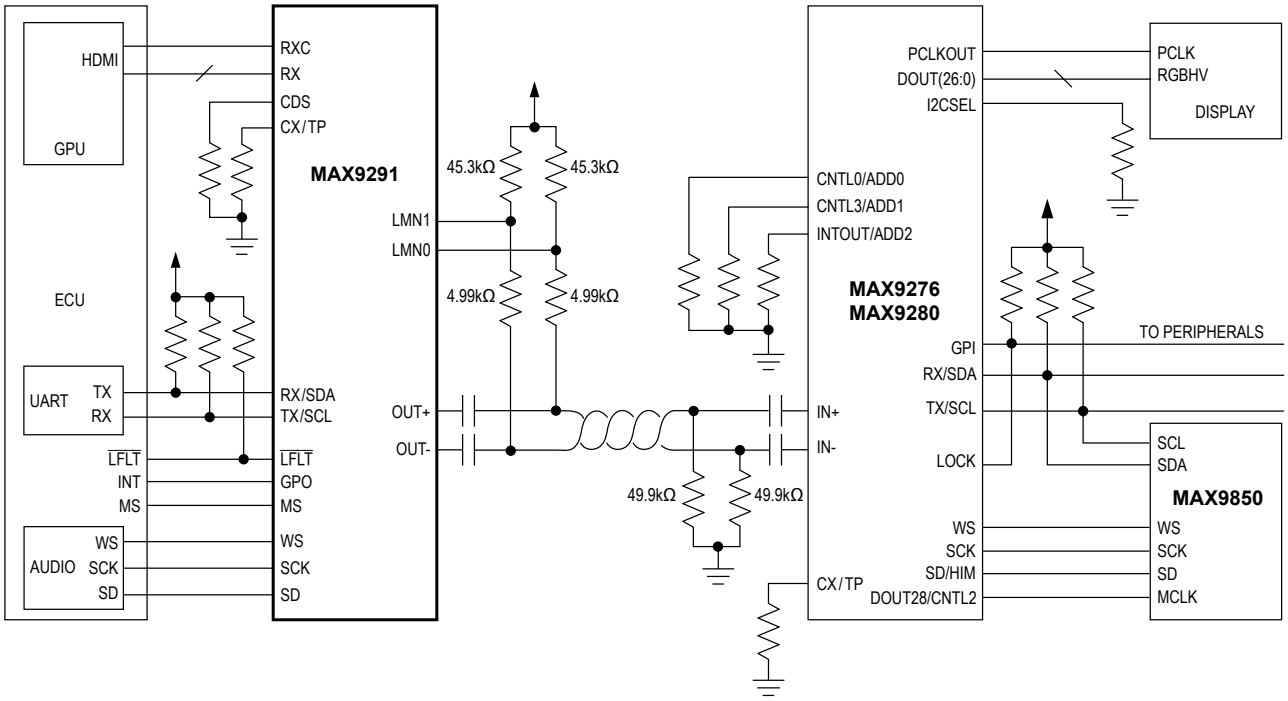
Table 34. HDMI MHL Register Table (I²C Address 0xF0)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0xE9	D[7:1]	—	0000000	Reserved	0000000
	D0	HPD_C_CTRL	0	Reset HPD output to 0	0
			1	Set HPD output to 1	
0xEA	D[7:1]	—	0000000	Reserved	0000000
	D0	HPD_OEN_CTRL	0	Disable HPD output pin control	0
			1	Enable HPD output pin control	

Table 35. HDMI EDID Register Table (GMSL I²C Address 0xFE, DDC I²C Address 0xA0)

REGISTER ADDRESS	SIZE (BYTES)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0x00 to 0xFF	256	—	Read/write	EDID	Undefined

Typical Application Circuit



NOTE: NOT ALL PULLUP/PULLDOWN RESISTORS ARE SHOWN. SEE PIN DESCRIPTION FOR DETAILS.

VIDEO-DISPLAY APPLICATION

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
56 TQFN-EP	T5688+5	21-0135	90-0046

Ordering Information

PART	HDCP	PIN-PACKAGE
MAX9291GTN+	No	56 TQFN-EP*
MAX9291GTN/V+	No	56 TQFN-EP*
MAX9293GTN+	Yes**	56 TQFN-EP*
MAX9293GTN/V+	Yes**	56 TQFN-EP*

Note: *All devices operate over the -40°C to +105°C operating temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.

/V denotes an automotive qualified product.
**EP = Exposed pad.*
***HDCP parts require registration with Digital Content Protection, LLC.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/15	Initial release	—
1	9/15	Added MAX9293 to data sheet; corrected *Thermal Package Characteristics for TQFN package;* deleted last sentence in the *I^2C Interface* section and corrected a typo in the Figure 38 and Figure 38 captions; changed TQFN package code to T56888+5 in *Package Information*; changed MAX9291GGN/V+ OPN to MAX9291GTN/VY+ in *Ordering Information*, removed QFND package	1–84

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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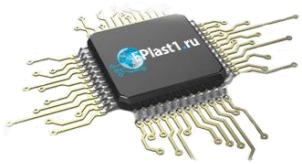
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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