

DDR4 SDRAM

MT40A2G4 MT40A1G8 MT40A512M16

Features	Options ¹	Marking
 V_{DD} = V_{DDQ} = 1.2V ±60mV V_{PP} = 2.5V, −125mV, +250mV On-die, internal, adjustable V_{REFDQ} generation 1.2V pseudo open-drain I/O Refresh time of 8192-cycle at T_C temperature range: 64ms at -40°C to 85°C 32ms at >85°C to 95°C 16ms at >95°C to 105°C 16 internal banks (x4, x8): 4 groups of 4 banks each 8 internal banks (x16): 2 groups of 4 banks each 8n-bit prefetch architecture Programmable data strobe preambles Data strobe preamble training Command/Address latency (CAL) Multipurpose register READ and WRITE capability Write leveling Self refresh mode Low-power auto self refresh (LPASR) Temperature controlled refresh (TCR) Fine granularity refresh Self refresh abort Maximum power saving 	 Configuration 2 Gig x 4 1 Gig x 8 512 Meg x 16 78-ball FBGA package (Pb-free) – x4, x8 9mm x 13.2mm – Rev. A 8mm x 12mm – Rev. B, D, G 7.5mm x 11mm – Rev. E, H, J 96-ball FBGA package (Pb-free) – x16 9mm x 14mm – Rev. A 8mm x 14mm – Rev. B 7.5mm x 13.5mm – Rev. D, E, H 7.5mm x 13mm – Rev. J Timing – cycle time 0.625ns @ CL = 22 (DDR4-3200) 0.682ns @ CL = 21 (DDR4-2933) 0.750ns @ CL = 19 (DDR4-2666) 0.750ns @ CL = 18 (DDR4-2666) 0.833ns @ CL = 17 (DDR4-2400) 0.833ns @ CL = 16 (DDR4-2400) 0.937ns @ CL = 15 (DDR4-2133) 	2G4 1G8 512M16 PM WE SA HA JY LY TB -062E -068 -075 -075E -083 -083E -093E
 Output driver calibration Nominal, park, and dynamic on-die termination 	 1.071ns @ CL = 13 (DDR4-1866) Operating temperature 	-107E
 (ODT) Data bus inversion (DBI) for data bus Command/Address (CA) parity Databus write cyclic redundancy check (CRC) Par-DRAM addressability 	 Commercial (0° ≤ T_C ≤ 95°C) Industrial (-40° ≤ T_C ≤ 95°C) Automotive (-40° ≤ T_C ≤ 105°C) Revision 	None IT AT :A, :B, :D, :E, :G, :H, :J

Table 1: Key Timing Parameters

· Per-DRAM addressability

• sPPR and hPPR capability

• JEDEC JESD-79-4 compliant

• Connectivity test

Speed Grade ¹	Data Rate (MT/s)	Target CL-nRCD-nRP	^t AA (ns)	^t RCD (ns)	^t RP (ns)
-062Y	3200	22-22-22	13.75 (13.32)	13.75 (13.32)	13.75 (13.32)
-062E	3200	22-22-22	13.75	13.75	13.75
-068	2933	21-21-21	14.32 (13.75)	14.32 (13.75)	14.32 (13.75)

Note: 1. Not all options listed can be combined to

for available offerings.

define an offered product. Use the part

catalog search on http://www.micron.com



Table 1: Key Timing Parameters (Continued)

Speed Grade ¹	Data Rate (MT/s)	Target CL-nRCD-nRP	^t AA (ns)	^t RCD (ns)	^t RP (ns)
-075E	2666	18-18-18	13.50	13.50	13.50
-075	2666	19-19-19	14.25 (13.75)	14.25 (13.75)	14.25 (13.75)
-083E	2400	16-16-16	13.32	13.32	13.32
-083	2400	17-17-17	14.16 (13.75)	14.16 (13.75)	14.16 (13.75)
-093E	2133	15-15-15	14.06 (13.50)	14.06 (13.50)	14.06 (13.50)
-093	2133	16-16-16	15.00	15.00	15.00
-107E	1866	13-13-13	13.92 (13.50)	13.92 (13.50)	13.92 (13.50)

Note: 1. Refer to the Speed Bin Tables for additional details.

Table 2: Addressing

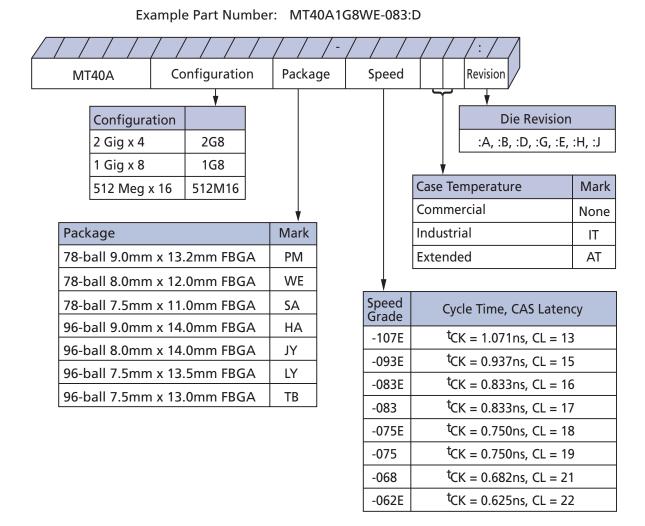
Parameter	2048 Meg x 4	1024 Meg x 8	512 Meg x 16
Number of bank groups	4	4	2
Bank group address	BG[1:0]	BG[1:0]	BG0
Bank count per group	4	4	4
Bank address in bank group	BA[1:0]	BA[1:0]	BA[1:0]
Row addressing	128K (A[16:0])	64K (A[15:0])	64K (A[15:0])
Column addressing	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])
Page size ¹	512B	1KB	2KB

Note: 1. Page size is per bank, calculated as follows:

Page size = 2^{COLBITS} × ORG/8, where COLBIT = the number of column address bits and ORG = the number of DQ bits.



Figure 1: Order Part Number Example







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Important Notes and Warnings

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General Notes and Description

Description

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM for the x16 configuration and as a 16-bank DRAM for the



x4 and x8 configurations. The DDR4 SDRAM uses an 8n-prefetch architecture to achieve high-speed operation. The 8n-prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins.

A single READ or WRITE operation for the DDR4 SDRAM consists of a single 8n-bit wide, four-clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Industrial Temperature

An industrial temperature (IT) device option requires that the case temperature not exceed below -40°C or above 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when operating outside of the commercial temperature range, when T_C is between -40°C and 0°C .

Automotive Temperature

The automotive temperature (AT) device option requires that the case temperature not exceed below -40°C or above 105°C . The specifications require the refresh rate to 2X when T_{C} exceeds 85°C ; 4X when T_{C} exceeds 95°C . Additionally, ODT resistance and the input/output impedance must be derated when operating temperature $T_{\text{C}} < 0^{\circ}\text{C}$.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation), unless specifically stated otherwise.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise
- The terms "_t" and "_c" are used to represent the true and complement of a differential signal pair. These terms replace the previously used notation of "#" and/or overbar characters. For example, differential data strobe pair DQS, DQS# is now referred to as DQS_t, DQS_c.
- The term "_n" is used to represent a signal that is active LOW and replaces the previously used "#" and/or overbar characters. For example: CS# is now referred to as CS n.
- The terms "DQS" and "CK" found throughout the data sheet are to be interpreted as DQS t, DQS c and CK t, CK c respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the entire document; any page
 or diagram may have been simplified to convey a topic and may not be inclusive of all
 requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated here within is considered undefined, illegal, and not supported, and can result in unknown operation.
- Addressing is denoted as BG[*n*] for bank group, BA[*n*] for bank address, and A[*n*] for row/col address.
- The NOP command is not allowed, except when exiting maximum power savings mode or when entering gear-down mode, and only a DES command should be used.



- Not all features described within this document may be available on the Rev. A (first) version.
- Not all specifications listed are finalized industry standards; best conservative estimates have been provided when an industry standard has not been finalized.
- Although it is implied throughout the specification, the DRAM must be used after V_{DD} has reached the stable power-on level, which is achieved by toggling CKE at least once every 8192 \times ^tREFI. However, in the event CKE is fixed HIGH, toggling CS_n at least once every 8192 \times ^tREFI is an acceptable alternative. Placing the DRAM into self refresh mode also alleviates the need to toggle CKE.
- Not all features designated in the data sheet may be supported by earlier die revisions due to late definition by JEDEC.
- A x16 device's DQ bus is comprised of two bytes. If only one of the bytes needs to be used, use the lower byte for data transfers and terminate the upper byte as noted:
 - Connect UDQS_t to VDDQ or VSS/ VSSQ via a resistor in the 200 Ω range.
 - Connect UDQS_c to the opposite rail via a resistor in the same 200Ω range.
 - Connect UDM to VDDQ via a large (10,000 Ω) pull-up resistor.
 - Connect UDBI to VDDQ via a large (10,000 Ω) pull-up resistor.
 - Connect DQ [15:8] individually to VDDQ via a large (10,000 Ω) resistors, or float DQ [15:8] .

Definitions of the Device-Pin Signal Level

- HIGH: A device pin is driving the logic 1 state.
- LOW: A device pin is driving the logic 0 state.
- High-Z: A device pin is tri-state.
- ODT: A device pin terminates with the ODT setting, which could be terminating or tristate depending on the mode register setting.

Definitions of the Bus Signal Level

- HIGH: One device on the bus is HIGH, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally V_{DDO}.
- LOW: One device on the bus is LOW, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally $V_{OL(DC)}$ if ODT was enabled, or V_{SSQ} if High-Z.
- High-Z: All devices on the bus are High-Z. The voltage level on the bus is undefined as the bus is floating.
- ODT: At least one device on the bus is ODT, and all others are High-Z. The voltage level on the bus is nominally V_{DDO}.
- The specification requires 8,192 refresh commands within 64ms between 0 °C and 85 °C. This allows for a ^tREFI of 7.8125μs (the use of "7.8μs" is truncated from 7.8125μs). The specification also requires 8,192 refresh commands within 32ms between 85 °C and 95 °C. This allows for a ^tREFI of 3.90625μs (the use of "3.9μs" is truncated from 3.90625μs).



Functional Block Diagrams

DDR4 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 16-bank (4-banks per Bank Group) DRAM.

Figure 2: 2 Gig x 4 Functional Block Diagram

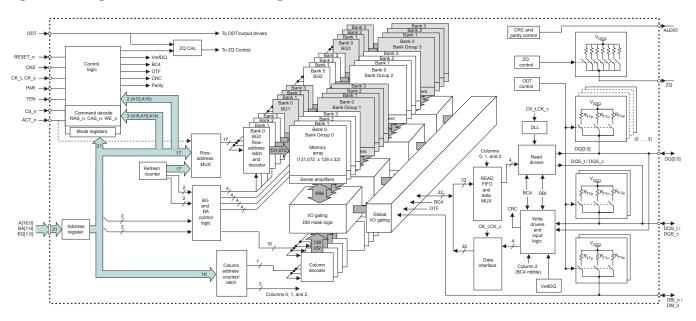


Figure 3: 1 Gig x 8 Functional Block Diagram

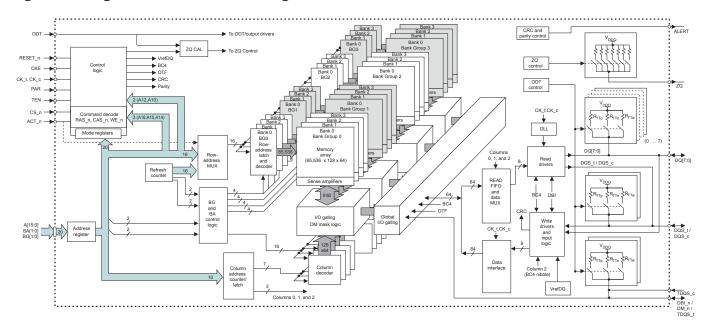
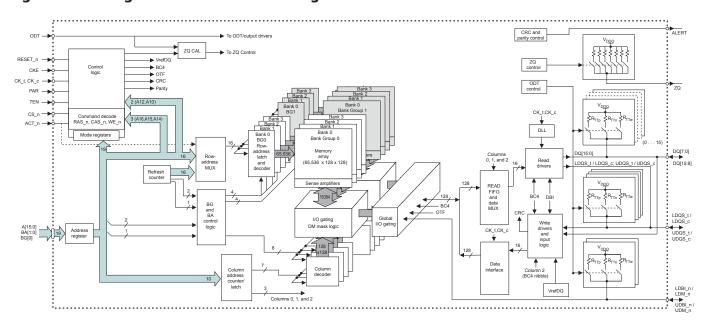




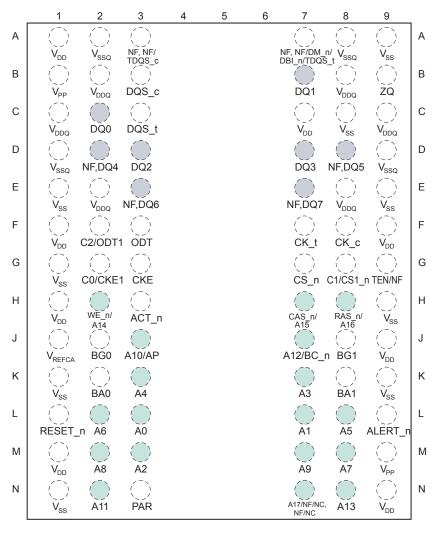
Figure 4: 512 Meg x 16 Functional Block Diagram





Ball Assignments

Figure 5: 78-Ball x4, x8 Ball Assignments

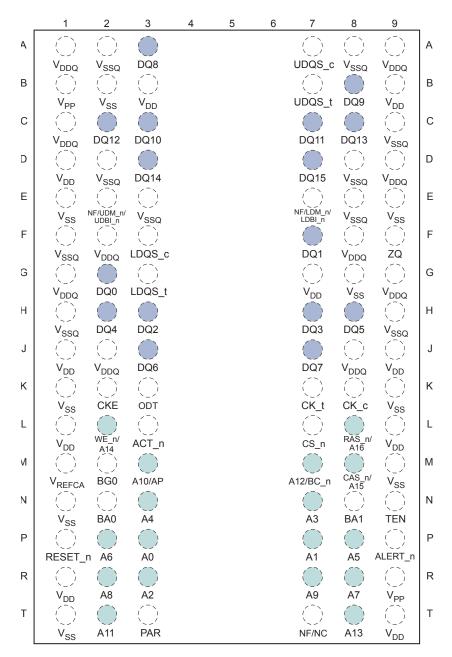


Notes: 1.

- 1. See Ball Descriptions.
- 2. A comma "," separates the configuration; a slash "/" defines a mode register selectable function, command/address function, density, or package dependence.
- 3. Address bits (including bank groups) are density- and configuration-dependent (see Addressing).



Figure 6: 96-Ball x16 Ball Assignments



Notes:

- 1. See Ball Descriptions.
- 2. A slash "/" defines a mode register selectable function, command/address function, density, or package dependence.
- 3. Address bits (including bank groups) are density- and configuration-dependent (see Addressing).



Ball Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR4 devices. All pins listed may not be supported on the device defined in this data sheet. See the Ball Assignments section to review all pins used on this device.

Table 3: Ball Descriptions

Symbol	Туре	Description
A[17:0]	Input	Address inputs: Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, RAS_n/A16 have additional functions, see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb and 16Gb parts. A17 connection is part-number specific; Contact vendor for more information.
A10/AP	Input	Auto precharge: A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	Burst chop: A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst chopped). See the Command Truth Table.
ACT_n	Input	Command input: ACT_n indicates an ACTIVATE command. When ACT_n (along with CS_n) is LOW, the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as row address inputs for the ACTIVATE command. When ACT_n is HIGH (along with CS_n LOW), the input pins RAS_n/ A16, CAS_n/A15, and WE_n/A14 are treated as normal commands that use the RAS_n, CAS_n, and WE_n signals. See the Command Truth Table.
BA[1:0]	Input	Bank address inputs: Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command.
BG[1:0]	Input	Bank group address inputs: Define the bank group to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. BG1 is not used in the x16 configuration.
C0/CKE1, C1/CS1_n, C2/ODT1	Input	Stack address inputs: These inputs are used only when devices are stacked; that is, they are used in 2H, 4H, and 8H stacks for x4 and x8 configurations (these pins are not used in the x16 configuration). DDR4 will support a traditional DDP package, which uses these three signals for control of the second die (CS1_n, CKE1, ODT1). DDR4 is not expected to support a traditional QDP package. For all other stack configurations, such as a 4H or 8H, it is assumed to be a single-load (master/slave) type of configuration where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT signal.
CK_t, CK_c	Input	Clock: Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.



Table 3: Ball Descriptions (Continued)

Symbol	Туре	Description
CKE	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit, however, timing parameters such as ^t XS are still calculated from the first rising clock edge where CKE HIGH satisfies ^t IS. After V _{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CS_n	Input	Chip select: All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
DM_n, UDM_n LDM_n	Input	Input data mask: DM_n is an input mask signal for write data. Input data is masked when DM is sampled LOW coincident with that input data during a write access. DM is sampled on both edges of DQS. DM is not supported on x4 configurations. The UDM_n and LDM_n pins are used in the x16 configuration: UDM_n is associated with DQ[15:8]; LDM_n is associated with DQ[7:0]. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Mask section.
ODT	Input	On-die termination: ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for the x4 and x8 configurations (when the TDQS function is enabled via mode register). For the x16 configuration, R_{TT} is applied to each DQ, UDQS_t, UDQS_c, LDQS_t, LDQS_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT} .
PAR	Input	Parity for command and address: This function can be enabled or disabled via the mode register. When enabled, the parity signal covers all command and address inputs, including ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, A[17:0], A10/AP, A12/BC_n, BA[1:0], and BG[1:0] with C0, C1, and C2 on 3DS only devices. Control pins NOT covered by the parity signal are CS_n, CKE, and ODT. Unused address pins that are density- and configuration-specific should be treated internally as 0s by the DRAM parity logic. Command and address inputs will have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is LOW.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n and ACT_n) define the command and/or address being entered. See the ACT_n description in this table.
RESET_n	Input	Active LOW asynchronous reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V _{DD} (960 mV for DC HIGH and 240 mV for DC LOW).
TEN	Input	Connectivity test mode: TEN is active when HIGH and inactive when LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V _{DD} (960mV for DC HIGH and 240mV for DC LOW). On Micron 3DS devices, connectivity test mode is not supported and the TEN pin should be considered NF maintained LOW at all times.



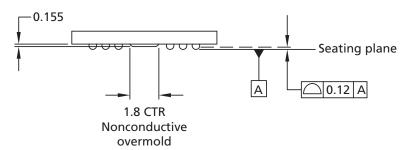
Table 3: Ball Descriptions (Continued)

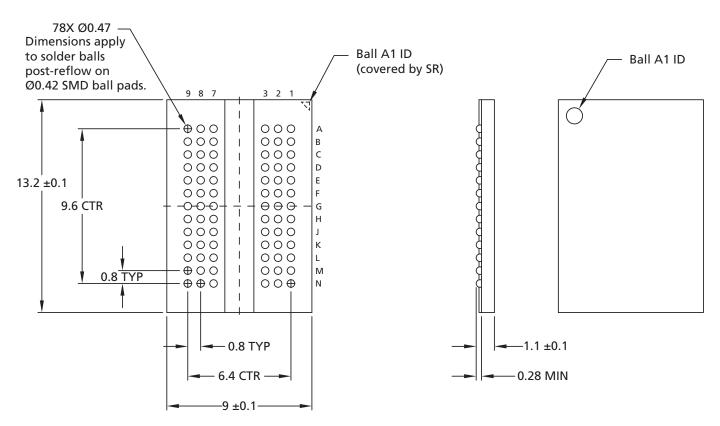
Symbol	Туре	Description
DQ	I/O	Data input/output: Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If write CRC is enabled via mode register, the write CRC code is added at the end of data burst. Any one or all of DQ0, DQ1, DQ2, and DQ3 may be used to monitor the internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH, training times change when enabled. During this mode, the R_{TT} value should be set to High-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DBI_n, UDBI_n, LDBI_n	I/O	DBI input/output: Data bus inversion. DBI_n is an input/output signal used for data bus inversion in the x8 configuration. UDBI_n and LDBI_n are used in the x16 configuration; UDBI_n is associated with DQ[7:0]. The DBI feature is not supported on the x4 configuration. DBI is not supported for 3DS devices and should be disabled in MR5. DBI can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Bus Inversion section.
DQS_t, DQS_c, UDQS_t, UDQS_c, LDQS_t, LDQS_c	I/O	Data strobe: Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For the x16, LDQS corresponds to the data on DQ[7:0]; UDQS corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	Alert output: This signal allows the DRAM to indicate to the system's memory controller that a specific alert or event has occurred. Alerts will include the command/address parity error and the CRC data error when either of these functions is enabled in the mode register.
TDQS_t, TDQS_c	Output	Termination data strobe: TDQS_t and TDQS_c are used by x8 DRAMs only. When enabled via the mode register, the DRAM will enable the same R _{TT} termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin will provide the DATA MASK (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations.
V _{DD}	Supply	Power supply: 1.2V ±0.060V.
V_{DDQ}	Supply	DQ power supply: 1.2V ±0.060V.
V _{PP}	Supply	DRAM activating power supply: 2.5V -0.125V/+0.250V.
V _{REFCA}	Supply	Reference voltage for control, command, and address pins.
V _{SS}	Supply	Ground.
V _{SSQ}	Supply	DQ ground.
ZQ	Reference	Reference ball for ZQ calibration: This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ} .
RFU	_	Reserved for future use.
NC	_	No connect: No internal electrical connection is present.
NF	_	No function: Internal connection is present but has no function.



Package Dimensions

Figure 7: 78-Ball FBGA - x4, x8 (PM)

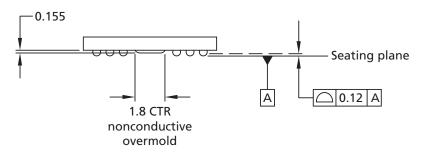




Notes: 1. All dimensions are in millimeters.



Figure 8: 78-Ball FBGA - x4, x8 (WE)



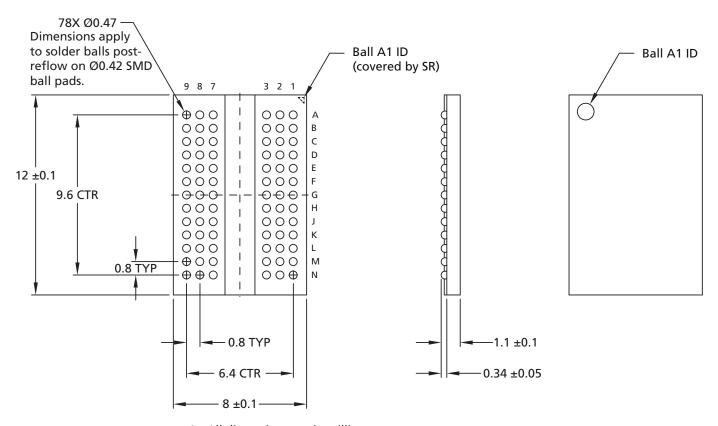
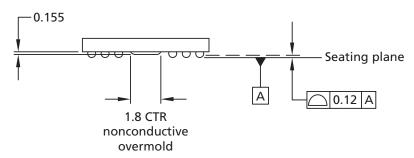




Figure 9: 78-Ball FBGA - x4, x8 (SA)



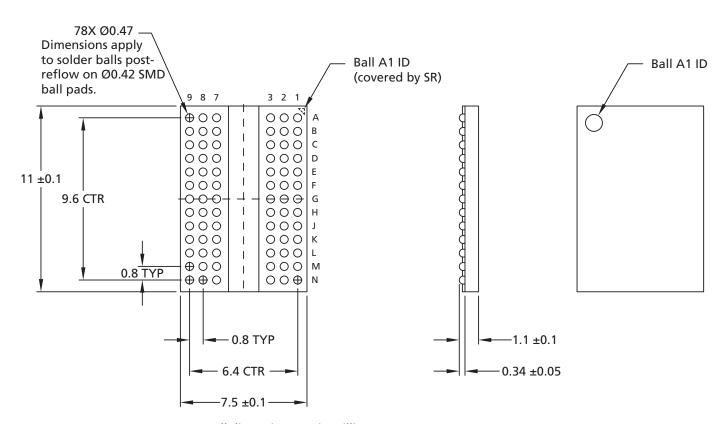
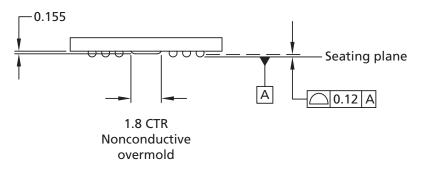




Figure 10: 96-Ball FBGA - x16 (HA)



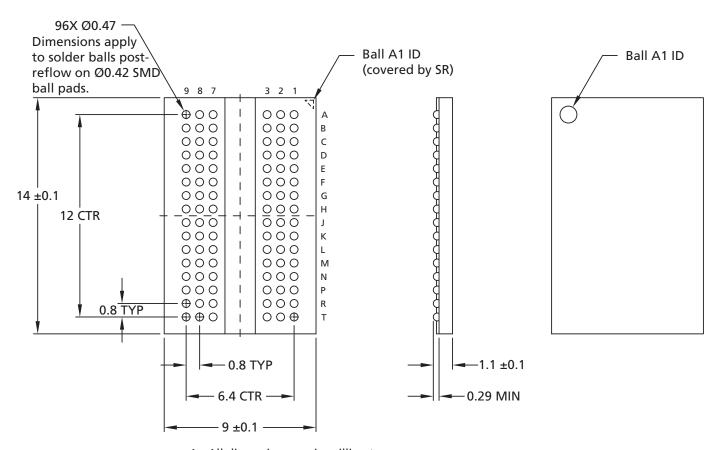
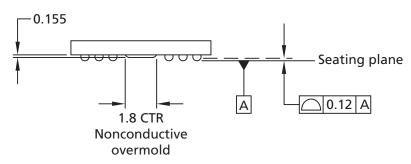




Figure 11: 96-Ball FBGA - x16 (JY)



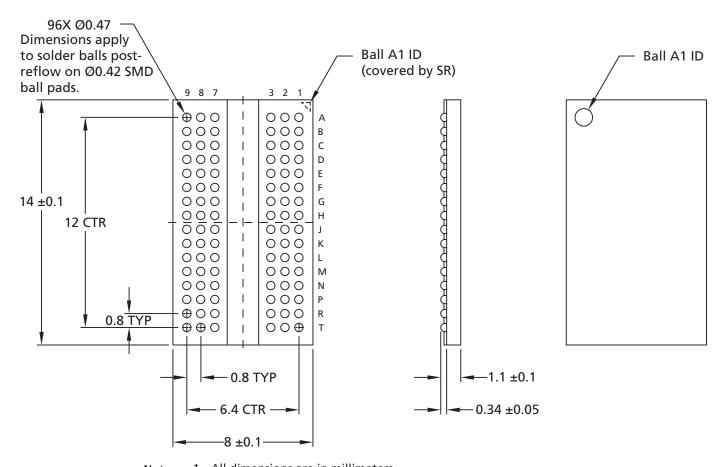
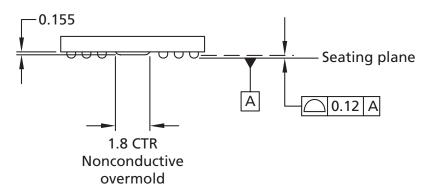




Figure 12: 96-Ball FBGA - x16 (LY)



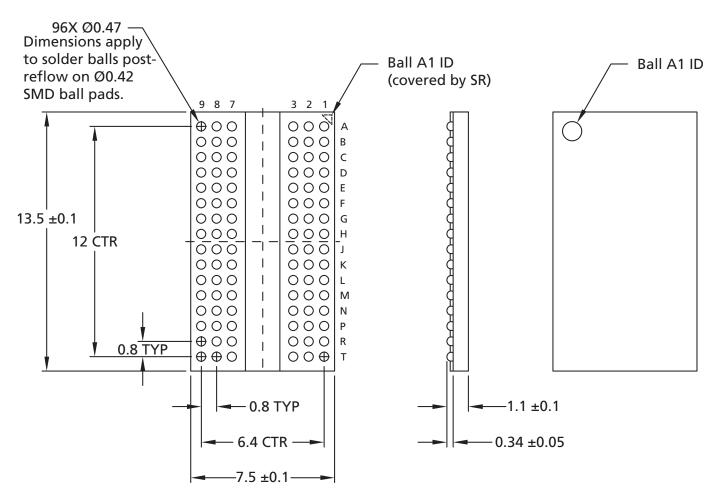
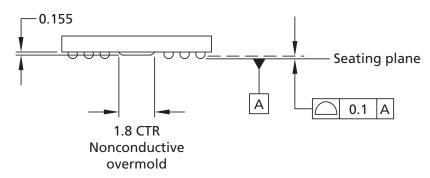
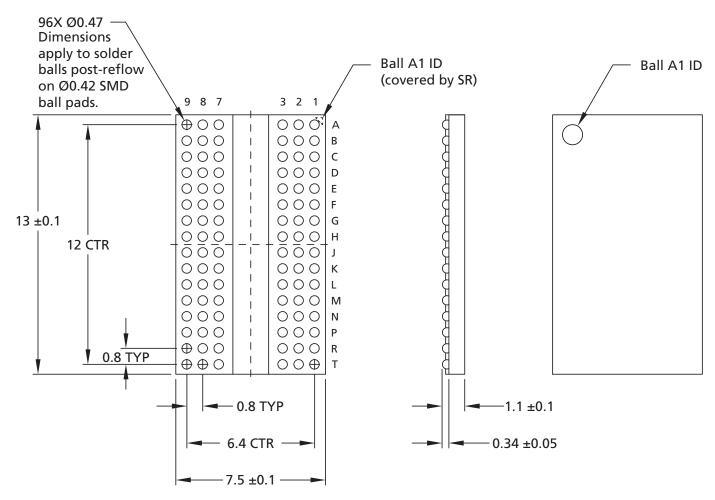




Figure 13: 96-Ball FBGA - x16 (TB)







State Diagram

This simplified state diagram provides an overview of the possible state transitions and the commands to control them. Situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

Figure 14: Simplified State Diagram

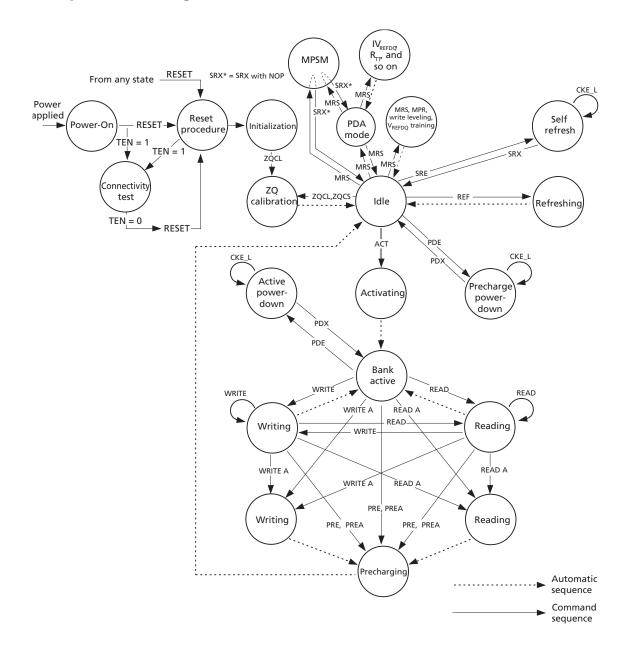




Table 4: State Diagram Command Definitions

Command	Description
ACT	Active
MPR	Multipurpose register
MRS	Mode register set
PDE	Enter power-down
PDX	Exit power-down
PRE	Precharge
PREA	Precharge all
READ	RD, RDS4, RDS8
READ A	RDA, RDAS4, RDAS8
REF	Refresh, fine granularity refresh
RESET	Start reset procedure
SRE	Self refresh entry
SRX	Self refresh exit
TEN	Boundary scan mode enable
WRITE	WR, WRS4, WRS8 with/without CRC
WRITE A	WRA, WRAS4, WRAS8 with/without CRC
ZQCL	ZQ calibration long
ZQCS	ZQ calibration short

Note: 1. See the Command Truth Table for more details.



Functional Description

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen banks (4 bank groups with 4 banks for each bank group) for x4/x8 devices, and as eight banks for each bank group (2 bank groups with 4 banks each) for x16 devices. The device uses double data rate (DDR) architecture to achieve high-speed operation. DDR4 architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for a device module effectively consists of a single 8*n*-bit-wide, four-clock-cycle-data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the device are burst-oriented. Accesses start at a selected location and continue for a burst length of eight or a chopped burst of four in a programmed sequence. Operation begins with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BG[1:0] select the bank group for x4/x8, and BG0 selects the bank group for x16; BA[1:0] select the bank, and A[17:0] select the row. See the Addressing section for more details). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst operation, determine if the auto PRECHARGE command is to be issued (via A10), and select BC4 or BL8 mode on-the-fly (OTF) (via A12) if enabled in the mode register.

Prior to normal operation, the device must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

NOTE: The use of the NOP command is allowed only when exiting maximum power saving mode or when entering gear-down mode.



RESET and Initialization Procedure

To ensure proper device function, the power-up and reset initialization default values for the following mode register (MR) settings are defined as:

- Gear-down mode (MR3 A[3]): 0 = 1/2 rate
- Per-DRAM addressability (MR3 A[4]): 0 = disable
- Maximum power-saving mode (MR4 A[1]): 0 = disable
- CS to command/address latency (MR4 A[8:6]): 000 = disable
- CA parity latency mode (MR5 A[2:0]): 000 = disable
- Hard post package repair mode (MR4 A[13]): 0 = disable
- Soft post package repair mode (MR4 A[5]): 0 = disable

Power-Up and Initialization Sequence

The following sequence is required for power-up and initialization:

1. Apply power (RESET_n and TEN should be maintained below $0.2 \times V_{DD}$ while supplies ramp up; all other inputs may be undefined). When supplies have ramped to a valid stable level, RESET_n must be maintained below $0.2 \times V_{DD}$ for a minimum of tPW_RESET_L and TEN must be maintained below $0.2 \times V_{DD}$ for a minimum of 700µs. CKE is pulled LOW anytime before RESET_n is de-asserted (minimum time of 10ns). The power voltage ramp time between 300mV to $V_{DD,min}$ must be no greater than 200ms, and during the ramp, V_{DD} must be greater than or equal to V_{DDQ} and $(V_{DD}$ - $V_{DDQ}) < 0.3 V. V_{PP}$ must ramp at the same time or up to 10 minutes prior to V_{DD} , and V_{PP} must be equal to or higher than V_{DD} at all times. The total time for which V_{PP} is powered and V_{DD} is unpowered should not exceed 360 cumulative hours. After V_{DD} has ramped and reached a stable level, RESET_n must go high within 10 minutes. After RESET_n goes high, the initialization sequence must be started within 3 seconds. For debug purposes, the 10 minute and 3 second delay limits may be extended to 60 minutes each provided the DRAM is operated in this debug mode for no more than 360 cumulative hours.

During power-up, the supply slew rate is governed by the limits stated in the table below and either condition A or condition B listed below must be met.

Table 5: Supply Power-up Slew Rate

Symbol	Min	Max	Unit	Comment
$V_{DD_}$ SL, $V_{DDQ_}$ SL, $V_{PP_}$ SL	0.004	600	V/ms	Measured between 300mV and 80% of supply minimum
V _{DD} _ona	N/A	200	ms	V_{DD} maximum ramp time from 300mV to V_{DD} minimum
V _{DDQ} _ona	N/A	200	ms	V_{DDQ} maximum ramp time from 300mV to V_{DDQ} minimum

Note: 1. 20 MHz band-limited measurement.

- Condition A:
 - Apply V_{PP} without any slope reversal before or at the same time as $V_{\rm DD}$ and $V_{\rm DDQ}.$



- V_{DD} and V_{DDQ} are driven from a single-power converter output and apply V_{DD}/V_{DDQ} without any slope reversal before or at the same time as V_{TT} and V_{RFFCA} .
- The voltage levels on all balls other than V_{DD} , V_{DDQ} , V_{SS} , and V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be greater than or equal to V_{SSQ} and V_{SS} on the other side.
- V_{TT} is limited to 0.76V MAX when the power ramp is complete.
- V_{REFCA} tracks V_{DD}/2.
- Condition B:
 - Apply V_{PP} without any slope reversal before or at the same time as V_{DD} .
 - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ} .
 - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} and V_{REFCA} .
 - The voltage levels on all pins other than V_{PP} , V_{DD} , V_{DDQ} , V_{SS} , and V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSO} and V_{SS} on the other side.
- 2. After RESET_n is de-asserted, wait for a minimum of 500us, but no longer than 3 seconds, before allowing CKE to be registered HIGH at clock edge Td. During this time, the device will start internal state initialization; this will be done independently of external clocks. A reasonable attempt was made in the design to power up with the following default MR settings: gear-down mode (MR3 A[3]): 0 = 1/2 rate; per-DRAM addressability (MR3 A[4]): 0 = disable; maximum power-down (MR4 A[1]): 0 = disable; CS to command/address latency (MR4 A[8:6]): 000 = disable; CA parity latency mode (MR5 A[2:0]): 000 = disable. However, it should be assumed that at power up the MR settings are undefined and should be programmed as shown below.
- 3. Clocks (CK_t, CK_c) need to be started and stabilized for at least 10ns or 5 ^tCK (whichever is larger) before CKE is registered HIGH at clock edge Td. Because CKE is a synchronous signal, the corresponding setup time to clock (^tIS) must be met. Also, a DESELECT command must be registered (with ^tIS setup time to clock) at clock edge Td. After the CKE is registered HIGH after RESET, CKE needs to be continuously registered HIGH until the initialization sequence is finished, including expiration of ^tDLLK and ^tZQinit.
- 4. The device keeps its ODT in High-Z state as long as RESET_n is asserted. Further, the SDRAM keeps its ODT in High-Z state after RESET_n de-assertion until CKE is registered HIGH. The ODT input signal may be in an undefined state until t IS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held either LOW or HIGH. If $R_{TT(NOM)}$ is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power-up initialization sequence is finished, including the expiration of t DLLK and t ZQinit.
- 5. After CKE is registered HIGH, wait a minimum of RESET CKE EXIT time, ${}^{t}XPR$, before issuing the first MRS command to load mode register (${}^{t}XPR = MAX$ (${}^{t}XS$, 5 × ${}^{t}CK$).
- 6. Issue MRS command to load MR3 with all application settings, wait ^tMRD.
- 7. Issue MRS command to load MR6 with all application settings, wait ^tMRD.
- 8. Issue MRS command to load MR5 with all application settings, wait ^tMRD.
- 9. Issue MRS command to load MR4 with all application settings, wait ${}^t\!MRD.$
- 10. Issue MRS command to load MR2 with all application settings, wait ^tMRD.
- 11. Issue MRS command to load MR1 with all application settings, wait ^tMRD.



8Gb: x4, x8, x16 DDR4 SDRAM RESET and Initialization Procedure

- 12. Issue MRS command to load MR0 with all application settings, wait ^tMOD.
- 13. Issue a ZQCL command to start ZQ calibration.
- 14. Wait for ^tDLLK and ^tZQinit to complete.
- 15. The device will be ready for normal operation. Once the DRAM has been initialized, if the DRAM is in an idle state longer than 960ms, then either (a) REF commands must be issued within ^tREFI constraints (specification for posting allowed) or (b) CKE or CS_n must toggle once within every 960ms interval of idle time. For debug purposes, the 960ms delay limit maybe extended to 60 minutes provided the DRAM is operated in this debug mode for no more than 360 cumulative hours.

A stable valid V_{DD} level is a set DC level (0Hz to 250 KHz) and must be no less than $V_{DD,min}$ and no greater than $V_{DD,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is stable. AC noise of $\pm 60 \text{mV}$ (greater than 250 KHz) is allowed on V_{DD} provided the noise doesn't alter V_{DD} to less than $V_{DD,min}$ or greater than $V_{DD,max}$.

A stable valid V_{DDQ} level is a set DC level (0Hz to 250 KHz) and must be no less than $V_{DDQ,min}$ and no greater than $V_{DDQ,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is stable. AC noise of ± 60 mV (greater than 250 KHz) is allowed on V_{DDQ} provided the noise doesn't alter V_{DDQ} to less than $V_{DDQ,min}$ or greater than $V_{DDQ,max}$.

A stable valid V_{PP} level is a set DC level (0Hz to 250 KHz) and must be no less than $V_{PP,min}$ and no greater than $V_{PP,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is stable. AC noise of ± 120 mV (greater than 250KHz) is allowed on V_{PP} provided the noise doesn't alter V_{PP} to less than $V_{PP,min}$ or greater than $V_{PP,max}$.



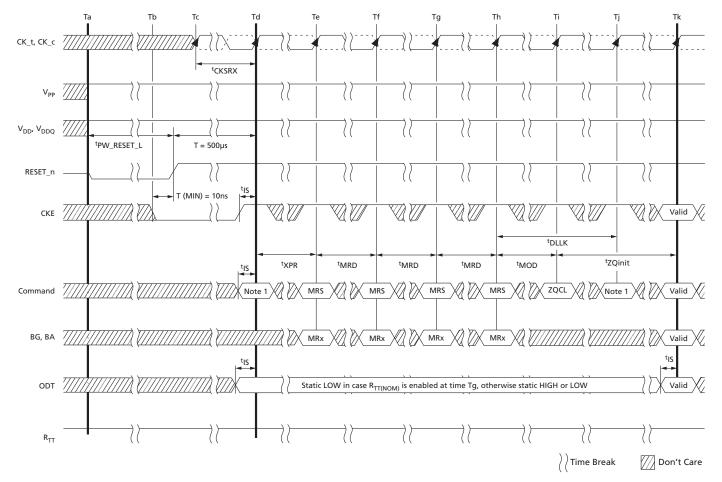


Figure 15: RESET and Initialization Sequence at Power-On Ramping

Notes:

- From time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
- 2. MRS commands must be issued to all mode registers that have defined settings.
- 3. In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).
- 4. TEN is not shown; however, it is assumed to be held LOW.

RESET Initialization with Stable Power Sequence

The following sequence is required for RESET at no power interruption initialization:

- 1. Assert RESET_n below $0.2 \times V_{DD}$ any time when reset is needed (all other inputs may be undefined). RESET_n needs to be maintained for minimum ^tPW_RESET. CKE is pulled LOW before RESET_n being de-asserted (minimum time 10ns).
- 2. Follow Steps 2 through 10 in the Reset and Initialization Sequence at Power-On Ramping procedure.

When the reset sequence is complete, all counters except the refresh counters have been reset and the device is ready for normal operation.



^tCKSRX $V_{\mathrm{DD}}, V_{\mathrm{DDQ}}$ tPW_RESET_S T = 500µs RESET n T (MIN) = 10ns V) [// ^tDLLK ^tXPR ^tMRD ^tMRD ^tMRD ^tMOD ^tZQinit Note 1 MRS ZQCL Note 1 MRx MRx MRx MRx Static LOW in case $R_{TT(NOM)}$ is enabled at time Tg, otherwise static HIGH or LOW Don't Care Time Break

Figure 16: RESET Procedure at Power Stable Condition

Notes:

- From time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
- 2. MRS commands must be issued to all mode registers that have defined settings.
- 3. In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).
- 4. TEN is not shown; however, it is assumed to be held LOW.

Uncontrolled Power-Down Sequence

In the event of an uncontrolled ramping down of V_{PP} supply, V_{PP} is allowed to be less than V_{DD} provided the following conditions are met:

- Condition A: V_{PP} and V_{DD}/V_{DDQ} are ramping down (as part of turning off) from normal operating levels.
- \bullet Condition B: The amount that V_{PP} may be less than V_{DD}/V_{DDQ} is less than or equal to 500mV
- Condition C: The time V_{PP} may be less than V_{DD} is ≤10ms per occurrence with a total accumulated time in this state ≤100ms.



• Condition D: The time V_{PP} may be less than 2.0V and above V_{SS} while turning off is ≤15ms per occurrence with a total accumulated time in this state ≤150ms.

Programming Mode Registers

For application flexibility, various functions, features, and modes are programmable in seven mode registers (MRn) provided by the device as user defined variables that must be programmed via a MODE REGISTER SET (MRS) command. Because the default values of the mode registers are not defined, contents of mode registers must be fully initialized and/or re-initialized; that is, they must be written after power-up and/or reset for proper operation. The contents of the mode registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS and DLL RESET commands do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

The MRS command cycle time, ^tMRD, is required to complete the WRITE operation to the mode register and is the minimum time required between the two MRS commands shown in the ^tMRD Timing figure.

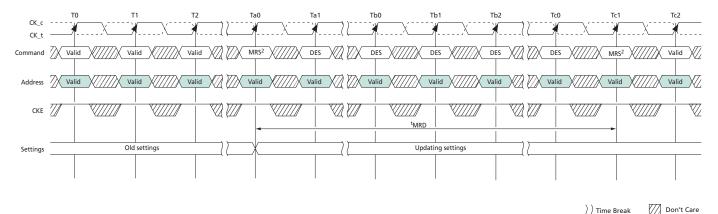
Some of the mode register settings affect address/command/control input functionality. In these cases, the next MRS command can be allowed when the function being updated by the current MRS command is completed. These MRS commands don't apply ^tMRD timing to the next MRS command; however, the input cases have unique MR setting procedures, so refer to individual function descriptions:

- · Gear-down mode
- · Per-DRAM addressability
- CMD address latency
- CA parity latency mode
- V_{REFDO} training value
- V_{REFDO} training mode
- V_{REFDO} training range

Some mode register settings may not be supported because they are not required by certain speed bins.



Figure 17: ^tMRD Timing



Notes: 1

- 1. This timing diagram depicts CA parity mode "disabled" case.
- 2. tMRD applies to all MRS commands with the following exceptions:

Gear-down mode

CA parity latency mode

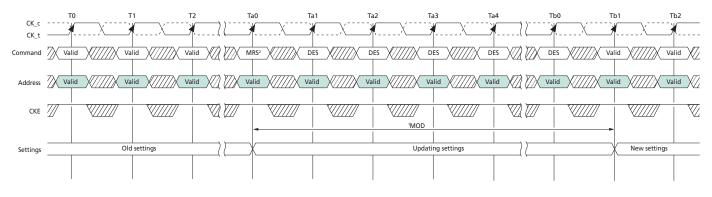
CMD address latency

Per-DRAM addressability mode

V_{REFDO} training value, V_{REFDO} training mode, and V_{REFDO} training range

The MRS command to nonMRS command delay, ^tMOD, is required for the DRAM to update features, except for those noted in note 2 in figure below where the individual function descriptions may specify a different requirement. ^tMOD is the minimum time required from an MRS command to a nonMRS command, excluding DES, as shown in the ^tMOD Timing figure.

Figure 18: ^tMOD Timing



Time Break Don't Care

Notes

- 1. This timing diagram depicts CA parity mode "disabled" case.
- 2. t MOD applies to all MRS commands with the following exceptions: DLL enable, DLL RESET, Gear-down mode V_{REFDO} training value, internal V_{REF} training monitor, V_{REFDO} training mode, and V_{REFDO}

training range





Maximum power savings mode , Per-DRAM addressability mode, and CA parity latency mode

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the device is in idle state; that is, all banks are in the precharged state with ${}^{\rm t}RP$ satisfied, all data bursts are completed, and CKE is HIGH prior to writing into the mode register. If the $R_{\rm TT(NOM)}$ feature is enabled in the mode register prior to and/or after an MRS command, the ODT signal must continuously be registered LOW, ensuring $R_{\rm TT}$ is in an off state prior to the MRS command. The ODT signal may be registered HIGH after ${}^{\rm t}MOD$ has expired. If the $R_{\rm TT(NOM)}$ feature is disabled in the mode register prior to and after an MRS command, the ODT signal can be registered either LOW or HIGH before, during, and after the MRS command. The mode registers are divided into various fields depending on functionality and modes.

In some mode register setting cases, function updating takes longer than ^tMOD. This type of MRS does not apply ^tMOD timing to the next valid command, excluding DES. These MRS command input cases have unique MR setting procedures, so refer to individual function descriptions.



Mode register 0 (MR0) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR0 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR0 Register Definition table.

Table 6: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS _n	CAS _n	WE _n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	1	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 7: MR0 Register Definition

Mode Register	Description
21	RFU 0 = Must be programmed to 0 1 = Reserved
20:18	MR select 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	N/A on 4Gb and 8Gb, RFU 0 = Must be programmed to 0 1 = Reserved
13,11:9	WR (WRITE recovery)/RTP (READ-to-PRECHARGE) 0000 = 10 / 5 clocks 0001 = 12 / 6 clocks 0010 = 14 / 7 clocks 0011 = 16 / 8 / clocks 0100 = 18 / 9 clocks 0101 = 20 / 10 clocks 0110 = 24 / 12 clocks 0111 = 22 / 11 clocks 1000 = 26 / 13 clocks 1001 = 28 / 14 clocks 1001 = 28 / 14 clocks 1010 through 1111 = Reserved



Table 7: MR0 Register Definition (Continued)

Mode	
Register	Description
8	DLL reset
	0 = No
	1 = Yes
7	Test mode (TM) – Manufacturer use only
	0 = Normal operating mode, must be programmed to 0
12, 6:4, 2	CAS latency (CL) – Delay in clock cycles from the internal READ command to first data-out
	$00000 = 9 \text{ clocks}^1$
	00001 = 10 clocks
	$00010 = 11 \text{ clocks}^1$
	00011 = 12 clocks
	$00100 = 13 \text{ clocks}^1$
	00101 = 14 clocks
	$00110 = 15 \text{ clocks}^1$
	00111 = 16 clocks
	01000 = 18 clocks
	01001 = 20 clocks
	01010 = 22 clocks
	01011 = 24 clocks
	$01100 = 23 \text{ clocks}^1$
	$01101 = 17 \text{ clocks}^1$
	$01110 = 19 \text{ clocks}^1$
	01111 = 21 clocks ¹
	10000 = 25 clocks
	10001 = 26 clocks
	10011 = 28 clocks
	$10100 = 29 \text{ clocks}^1$
	10101 = 30 clocks
	10110 = 31 clocks ¹
	10111 = 32 clocks
3	Burst type (BT) – Data burst ordering within a READ or WRITE burst access
	0 = Nibble sequential
	1 = Interleave
1:0	Burst length (BL) – Data burst size associated with each read or write access
	00 = BL8 (fixed)
	01 = BC4 or BL8 (on-the-fly)
	10 = BC4 (fixed)
	11 = Reserved

- Notes: 1. Not allowed when 1/4 rate gear-down mode is enabled.
 - 2. If WR requirement exceeds 28 clocks or RTP exceeds 14 clocks, WR should be set to 28 clocks and RTP should be set to 14 clocks.

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The ordering of accesses within a burst is determined by the burst length, burst type,



and the starting column address as shown in the following table. Burst length options include fixed BC4, fixed BL8, and on-the-fly (OTF), which allows BC4 or BL8 to be selected coincidentally with the registration of a READ or WRITE command via A12/BC_n.

Table 8: Burst Type and Burst Order

Note 1 applies to the entire table

		Starting			
Burst Length	READ/ WRITE	Column Address (A[2, 1, 0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
BC4	READ	0 0 0	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T	2, 3
		0 0 1	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T	2, 3
		0 1 0	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T	2, 3
		0 1 1	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T	2, 3
		100	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T	2, 3
		1 0 1	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T	2, 3
		1 1 0	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T	2, 3
		111	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T	2, 3
	WRITE	0, V, V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	2, 3
		1, V, V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	2, 3
BL8	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	
		110	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	
		111	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	
	WRITE	V, V, V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	3

- Notes: 1. 0...7 bit number is the value of CA[2:0] that causes this bit to be the first read during a
 - 2. When setting burst length to BC4 (fixed) in MR0, the internal WRITE operation starts two clock cycles earlier than for the BL8 mode, meaning the starting point for ^tWR and ^tWTR will be pulled in by two clocks. When setting burst length to OTF in MR0, the internal WRITE operation starts at the same time as a BL8 (even if BC4 was selected during column time using A12/BC4_n) meaning that if the OTF MR0 setting is used, the starting point for tWR and tWTR will not be pulled in by two clocks as described in the BC4 (fixed) case.
 - 3. T = Output driver for data and strobes are in High-Z. V = Valid logic level (0 or 1), but respective buffer input ignores level on input pins. X = "Don't Care."

CAS Latency

The CAS latency (CL) setting is defined in the MR0 Register Definition table. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The device does not support half-clock latencies. The



overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL): RL = AL + CL.

Test Mode

The normal operating mode is selected by MR0[7] and all other bits set to the desired values shown in the MR0 Register Definition table. Programming MR0[7] to a value of 1 places the device into a DRAM manufacturer-defined test mode to be used only by the manufacturer, not by the end user. No operations or functionality is specified if MR0[7] = 1.

Write Recovery (WR)/READ-to-PRECHARGE

The programmed write recovery (WR) value is used for the auto precharge feature along with [†]RP to determine [†]DAL. WR for auto precharge (MIN) in clock cycles is calculated by dividing [†]WR (in ns) by [†]CK (in ns) and rounding to the next integer using the rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section. The WR value must be programmed to be equal to or larger than [†]WR (MIN). When both DM and write CRC are enabled in the mode register, the device calculates CRC before sending the write data into the array; [†]WR values will change when enabled. If there is a CRC error, the device blocks the WRITE operation and discards the data.

Internal READ-to-PRECHARGE (RTP) command delay for auto precharge (MIN) in clock cycles is calculated by dividing ^tRTP (in ns) by ^tCK (in ns) and rounding to the next integer using the rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section. The RTP value in the mode register must be programmed to be equal to or larger than RTP (MIN). The programmed RTP value is used with ^tRP to determine the ACT timing to the same bank.

DLL RESET

The DLL reset bit is self-clearing, meaning that it returns to the value of 0 after the DLL RESET function has been issued. After the DLL is enabled, a subsequent DLL RESET should be applied. Any time the DLL RESET function is used, ^tDLLK must be met before functions requiring the DLL can be used. Such as READ commands or synchronous ODT operations, for example.



Mode register 1 (MR1) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR1 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR1 Register Definition table.

Table 9: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS _n	CAS _n	WE _n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	1	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 10: MR1 Register Definition

Mode Register	Description
21	RFU 0 = Must be programmed to 0 1 = Reserved
20:18	MR select 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	N/A on 4Gb and 8Gb, RFU 0 = Must be programmed to 0 1 = Reserved
12	Data output disable (Qoff) – Output buffer disable 0 = Enabled (normal operation) 1 = Disabled (both ODI and R _{TT})
11	Termination data strobe (TDQS) – Additional termination pins (x8 configuration only) 0 = TDQS disabled 1 = TDQS enabled



Table 10: MR1 Register Definition (Continued)

Mode Register	Description
10, 9, 8	Nominal ODT (R _{TT(NOM)} – Data bus termination setting
	$000 = R_{TT(NOM)}$ disabled
	001 = RZQ/4 (60 ohm)
	010 = RZQ/2 (120 ohm)
	011 = RZQ/6 (40 ohm)
	100 = RZQ/1 (240 ohm)
	101 = RZQ/5 (48 ohm)
	110 = RZQ/3 (80 ohm)
	111 = RZQ/7 (34 ohm)
7	Write leveling (WL) – Write leveling mode
	0 = Disabled (normal operation)
	1 = Enabled (enter WL mode)
13, 6, 5	Rx CTLE Control
	000 = Vendor Default
	001 = Vendor Defined
	010 = Vendor Defined
	011 = Vendor Defined
	100 = Vendor Defined
	101 = Vendor Defined
	110 = Vendor Defined
	111 = Vendor Defined
4, 3	Additive latency (AL) – Command additive latency setting
	00 = 0 (AL disabled)
	$01 = CL - 1^1$
	10 = CL - 2
	11 = Reserved
2, 1	Output driver impedance (ODI) – Output driver impedance setting
	00 = RZQ/7 (34 ohm)
	01 = RZQ/5 (48 ohm)
	10 = Reserved (Although not JEDEC-defined and not tested, this setting will provide RZQ/6 or 40 ohm)
	11 = Reserved
0	DLL enable - DLL enable feature
	0 = DLL disabled
	1 = DLL enabled (normal operation)

Note: 1. Not allowed when 1/4 rate gear-down mode is enabled.

DLL Enable/DLL Disable

The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation (DLL enabled with MR1[0]) the DLL is automatically disabled when entering the SELF REFRESH operation and is automatically re-enabled upon exit of the SELF REFRESH operation. Any time the DLL is enabled and subsequently reset, [†]DLLK clock cycles must occur before a READ or SYNCHRONOUS ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Fail-



ing to wait for synchronization to occur may result in a violation of the ^tDQSCK, ^tAON, or ^tAOF parameters.

During ^tDLLK, CKE must continuously be registered HIGH. The device does not require DLL for any WRITE operation, except when R_{TT(WR)} is enabled and the DLL is required for proper ODT operation.

The direct ODT feature is not supported during DLL off mode. The ODT resistors must be disabled by continuously registering the ODT pin LOW and/or by programming the $R_{TT(NOM)}$ bits MR1[9,6,2] = 000 via an MRS command during DLL off mode.

The dynamic ODT feature is not supported in DLL off mode; to disable dynamic ODT externally, use the MRS command to set $R_{TT(WR)}$, MR2[10:9] = 00.

Output Driver Impedance Control

The output driver impedance of the device is selected by MR1[2,1], as shown in the MR1 Register Definition table.

ODT R_{TT(NOM)} Values

The device is capable of providing three different termination values: $R_{TT(Park)}$, $R_{TT(NOM)}$, and $R_{TT(WR)}$. The nominal termination value, $R_{TT(NOM)}$, is programmed in MR1. A separate value, $R_{TT(WR)}$, may be programmed in MR2 to enable a unique R_{TT} value when ODT is enabled during WRITE operations. The $R_{TT(WR)}$ value can be applied during WRITE commands even when $R_{TT(NOM)}$ is disabled. A third R_{TT} value, $R_{TT(Park)}$, is programed in MR5. $R_{TT(Park)}$ provides a termination value when the ODT signal is LOW.

Additive Latency

The ADDITIVE LATENCY (AL) operation is supported to make command and data buses efficient for sustainable bandwidths in the device. In this operation, the device allows a READ or WRITE command (either with or without auto precharge) to be issued immediately after the ACTIVATE command. The command is held for the time of AL before it is issued inside the device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. WRITE latency (WL) is controlled by the sum of the AL and CAS WRITE latency (CWL) register settings.

Table 11: Additive Latency (AL) Settings

A4	А3	AL
0	0	0 (AL disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

Note: 1. AL has a value of CL - 1 or CL - 2 based on the CL values programmed in the MR0 register.

Rx CTLE Control

The Mode Register for Rx CTLE Control MR1[A13,A6,A5] is vendor specific. Since CTLE circuits can not be typically bypassed a disable option is not provided. Instead, a vendor optimized setting is given. It should be noted that the settings are not specifically linear



in relationship to the vendor optimized setting, so the host may opt to instead walk through all the provided options and use the setting that works best in their environment.

Write Leveling

For better signal integrity, the device uses fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology benefits from a reduced number of stubs and their lengths, but it causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain [†]DQSS, [†]DSS, and [†]DSH specifications. Therefore, the device supports a write leveling feature that allows the controller to compensate for skew.

Output Disable

The device outputs may be enabled/disabled by MR1[12] as shown in the MR1 Register Definition table. When MR1[12] is enabled (MR1[12] = 1) all output pins (such as DQ and DQS) are disconnected from the device, which removes any loading of the output drivers. For example, this feature may be useful when measuring module power. For normal operation, set MR1[12] to 0.

Termination Data Strobe

Termination data strobe (TDQS) is a feature of the x8 device and provides additional termination resistance outputs that may be useful in some system configurations. Because this function is available only in a x8 configuration, it must be disabled for x4 and x16 configurations.

While TDQS is not supported in x4 or x16 configurations, the same termination resistance function that is applied to the TDQS pins is applied to the DQS pins when enabled via the mode register.

The TDQS, DBI, and DATA MASK (DM) functions share the same pin. When the TDQS function is enabled via the mode register, the DM and DBI functions are not supported. When the TDQS function is disabled, the DM and DBI functions can be enabled separately.

Table 12: TDQS Function Matrix

TDQS	Data Mask (DM)	WRITE DBI	READ DBI
Disabled	Enabled	Disabled	Enabled or disabled
	Disabled	Enabled	Enabled or disabled
	Disabled	Disabled	Enabled or disabled
Enabled	Disabled	Disabled	Disabled



Mode register 2 (MR2) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR2 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR2 Register Definition table.

Table 13: Address Pin Mapping

Address	BG1	BG0	BA1	ВА0	A17	RAS	CAS	WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	А3	A2	A1	A0
bus						_'''	_'''	_'''														
Mode	21	20	19	18	17	_	_	_	13	12	11	10	9	8	7	6	5	4	3	2	1	0
register																						

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 14: MR2 Register Definition

Mode Register	Description
21	RFU 0 = Must be programmed to 0 1 = Reserved
20:18	MR select 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	N/A on 4Gb and 8Gb, RFU 0 = Must be programmed to 0 1 = Reserved
13	RFU 0 = Must be programmed to 0 1 = Reserved
12	WRITE data bus CRC 0 = Disabled 1 = Enabled



Table 14: MR2 Register Definition (Continued)

Mode Register	Description
11:9	Dynamic ODT (R _{TT(WR)}) – Data bus termination setting during WRITES 000 = R _{TT(WR)} disabled (WRITE does not affect R _{TT} value) 001 = RZQ/2 (120 ohm) 010 = RZQ/1 (240 ohm) 011 = High-Z 100 = RZQ/3 (80 ohm) 101 = Reserved 110 = Reserved 111 = Reserved
7:6	Low-power auto self refresh (LPASR) – Mode summary 00 = Manual mode - Normal operating temperature range (T _C : -40°C–85°C) 01 = Manual mode - Reduced operating temperature range (T _C : -40°C–45°C) 10 = Manual mode - Extended operating temperature range (T _C : -40°C–105°C) 11 = ASR mode - Automatically switching among all modes
5:3	CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 1 ^t CK WRITE preamble 000 = 9 (DDR4-1600) ¹ 001 = 10 (DDR4-1866) 010 = 11 (DDR4-2133/1600) ¹ 011 = 12 (DDR4-2400/1866) 100 = 14 (DDR4-2666/2133) 101 = 16 (DDR4-2933,3200/2400) 110 = 18 (DDR4-2666) 111 = 20 (DDR4-2933, 3200)
	CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 2 ^t CK WRITE preamble 000 = N/A 001 = N/A 010 = N/A 011 = N/A 100 = 14 (DDR4-2400) 101 = 16 (DDR4-2666/2400) 110 = 18 (DDR4-2933, 3200/2666) 111 = 20 (DDR4-2933, 3200)
8, 2	RFU 0 = Must be programmed to 0 1 = Reserved
1:0	RFU 0 = Must be programmed to 0 1 = Reserved

Note: 1. Not allowed when 1/4 rate gear-down mode is enabled.



CAS WRITE Latency

CAS WRITE latency (CWL) is defined by MR2[5:3] as shown in the MR2 Register Definition table. CWL is the delay, in clock cycles, between the internal WRITE command and the availability of the first bit of input data. The device does not support any half-clock latencies. The overall WRITE latency (WL) is defined as additive latency (AL) + parity latency (PL) + CAS WRITE latency (CWL): WL = AL +PL + CWL.

Low-Power Auto Self Refresh

Low-power auto self refresh (LPASR) is supported in the device. Applications requiring SELF REFRESH operation over different temperature ranges can use this feature to optimize the I_{DD6} current for a given temperature range as specified in the MR2 Register Definition table.

Dynamic ODT

In certain applications and to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the device without issuing an MRS command. This may be done by configuring the dynamic ODT $(R_{TT(WR)})$ settings in MR2[11:9]. In write leveling mode, only $R_{TT(NOM)}$ is available.

Write Cyclic Redundancy Check Data Bus

The write cyclic redundancy check (CRC) data bus feature during writes has been added to the device. When enabled via the mode register, the data transfer size goes from the normal 8-bit (BL8) frame to a larger 10-bit UI frame, and the extra two UIs are used for the CRC information.



Mode register 3 (MR3) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR3 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR3 Register Definition table.

Table 15: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS _n	CAS _n	WE _n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	1	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 16: MR3 Register Definition

Mode Register	Description
21	RFU
	0 = Must be programmed to 0
	1 = Reserved
20:18	MR select
	000 = MR0
	001 = MR1
	010 = MR2 011 = MR3
	100 = MR4
	100 = MR4 101 = MR5
	110 = MR6
	111 = DNU
17	N/A on 4Gb and 8Gb, RFU
	0 = Must be programmed to 0
	1 = Reserved
13	RFU
	0 = Must be programmed to 0
	1 = Reserved
12:11	Multipurpose register (MPR) – Read format
	00 = Serial
	01 = Parallel
	10 = Staggered
	11 = Reserved
10:9	WRITE CMD latency when CRC/DM enabled
	00 = 4CK (DDR4-1600)
	01 = 5CK (DDR4-1866/2133/2400/2666)
	10 = 6CK (DDR4-2933/3200)
	11 = Reserved



Table 16: MR3 Register Definition (Continued)

Mode Register	Description
8:6	Fine granularity refresh mode 000 = Normal mode (fixed 1x) 001 = Fixed 2x 010 = Fixed 4x 011 = Reserved 100 = Reserved 101 = On-the-fly 1x/2x 111 = Reserved
5	Temperature sensor status 0 = Disabled 1 = Enabled
4	Per-DRAM addressability 0 = Normal operation (disabled) 1 = Enable
3	Gear-down mode – Ratio of internal clock to external data rate 0 = [1:1]; (1/2 rate data) 1 = [2:1]; (1/4 rate data)
2	Multipurpose register (MPR) access 0 = Normal operation 1 = Data flow from MPR
1:0	MPR page select 00 = Page 0 01 = Page 1 10 = Page 2 11 = Page 3 (restricted for DRAM manufacturer use only)

Multipurpose Register

The multipurpose register (MPR) is used for several features:

- Readout of the contents of the MRn registers
- WRITE and READ system patterns used for data bus calibration
- Readout of the error frame when the command address parity feature is enabled

To enable MPR, issue an MRS command to MR3[2] = 1. MR3[12:11] define the format of read data from the MPR. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and ${}^{t}RP$ met). After MPR is enabled, any subsequent RD or RDA commands will be redirected to a specific mode register.

The mode register location is specified with the READ command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power-down mode, SELF REFRESH, and any other nonRD/RDA or nonWR/WRA commands are not allowed during MPR mode. The RESET function is supported during MPR mode, which requires device re-initialization.



WRITE Command Latency When CRC/DM is Enabled

The WRITE command latency (WCL) must be set when both write CRC and DM are enabled for write CRC persistent mode. This provides the extra time required when completing a WRITE burst when write CRC and DM are enabled. This means at data rates less than or equal to 1600 MT/s then 4nCK is used, 5nCK or 6nCK are not allowed; at data rates greater than 1600 MT/s and less than or equal to 2666 MT/s then 5nCK is used, 4nCK or 6nCK are not allowed; and at data rates greater than 2666 MT/s and less than or equal to 3200 MT/s then 6nCK is used; 4nCK or 5nCK are not allowed.

Fine Granularity Refresh Mode

This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening ^tRFC and decreasing cycle time allows more accesses to the chip and allows for increased scheduling flexibility.

Temperature Sensor Status

This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; when an MPR read of the temperature sensor status bits occurs, the temperature sensor status should be no older than 32ms.

Per-DRAM Addressability

This mode allows commands to be masked on a per device basis providing any device in a rank (devices sharing the same command and address signals) to be programmed individually. As an example, this feature can be used to program different ODT or V_{REF} values on DRAM devices within a given rank.

Gear-Down Mode

The device defaults in 1/2 rate (1N) clock mode and uses a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS_n, CKE, and ODT when in 1/4 rate (2N) mode. For operation in 1/2 rate mode, no MRS command or sync pulse is required.



Mode register 4 (MR4) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR4 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR4 Register Definition table.

Table 17: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS _n	CAS _n	WE _n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	1	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET (MRS) command.

Table 18: MR4 Register Definition

Mode Register	Description
21	RFU 0 = Must be programmed to 0 1 = Reserved
20:18	MR select 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	N/A on 4Gb and 8Gb, RFU 0 = Must be programmed to 0 1 = Reserved
13	Hard Post Package Repair (hPPR mode) 0 = Disabled 1 = Enabled
12	WRITE preamble setting 0 = 1 ^t CK toggle ¹ 1 = 2 ^t CK toggle (When operating in 2 ^t CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^t CK range.)
11	READ preamble setting $0 = 1^{t}CK toggle^{1}$ $1 = 2^{t}CK toggle$
10	READ preamble training 0 = Disabled 1 = Enabled



Table 18: MR4 Register Definition (Continued)

Mode Register	Description
9	Self refresh abort mode
	0 = Disabled
	1 = Enabled
8:6	CMD (CAL) address latency
	000 = 0 clocks (disabled)
	001 =3 clocks ¹
	010 = 4 clocks
	$011 = 5 \text{ clocks}^1$
	100 = 6 clocks
	101 = 8 clocks
	110 = Reserved
	111 = Reserved
5	soft Post Package Repair (sPPR mode)
	0 = Disabled
	1 = Enabled
4	Internal V _{REF} monitor
	0 = Disabled
	1 = Enabled
3	Temperature controlled refresh mode
	0 = Disabled
	1 = Enabled
2	Temperature controlled refresh range
	0 = Normal temperature mode
	1 = Extended temperature mode
1	Maximum power savings mode
	0 = Normal operation
	1 = Enabled
0	RFU
	0 = Must be programmed to 0
	1 = Reserved

Note: 1. Not allowed when 1/4 rate gear-down mode is enabled.

Hard Post Package Repair Mode

The hard post package repair (hPPR) mode feature is JEDEC optional for 4Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [7] indicates whether hPPR mode is available (A7 = 1) or not available (A7 = 0). hPPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank can be repaired. The repair process is irrevocable so great care should be exercised when using.

Soft Post Package Repair Mode

The soft post package repair (sPPR) mode feature is JEDEC optional for 4Gb and 8Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [6] indicates whether sPPR mode is available (A6 = 1) or not available (A6 = 0). sPPR mode provides a simple and



easy repair method of the device after placed in the system. One row per bank can be repaired. The repair process is revocable by either doing a reset or power-down or by rewriting a new address in the same bank.

WRITE Preamble

Programmable WRITE preamble, ^tWPRE, can be set to 1^tCK or 2^tCK via the MR4 register. The 1^tCK setting is similar to DDR3. However, when operating in 2^tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^tCK range.

Some even settings will require addition of 2 clocks. If the alternate longer CWL was used, the additional clocks will not be required.

READ Preamble

Programmable READ preamble ^tRPRE can be set to 1^tCK or 2^tCK via the MR4 register. Both the 1^tCK and 2^tCK DDR4 preamble settings are different from that defined for the DDR3 SDRAM. Both DDR4 READ preamble settings may require the memory controller to train (or read level) its data strobe receivers using the READ preamble training.

READ Preamble Training

Programmable READ preamble training can be set to 1^tCK or 2^tCK. This mode can be used by the memory controller to train or READ level its data strobe receivers.

Temperature-Controlled Refresh

When temperature-controlled refresh mode is enabled, the device may adjust the internal refresh period to be longer than ^tREFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio. For example, the DRAM temperature sensor detected less than 45°C. Normal temperature mode covers the range of -40°C to 85°C, while the extended temperature range covers -40°C to 105°C.

Command Address Latency

COMMAND ADDRESS LATENCY (CAL) is a power savings feature and can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles (tCAL) between a CS_n registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register according to the tCAL(ns)/tCK(ns) rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section.

Internal V_{REF} Monitor

This mode enables output of internally generated V_{REFDQ} for monitoring on DQ0, DQ1, DQ2, and DQ3. May be used during V_{REFDQ} training and test. While in this mode, R_{TT} should be set to High-Z. V_{REF_time} must be increased by 10ns if DQ load is 0pF, plus an additional 15ns per pF of loading. This measurement is for verification purposes and is NOT an external voltage supply pin.



Maximum Power Savings Mode

This mode provides the lowest power mode where data retention is not required. When the device is in the maximum power saving mode, it does not need to guarantee data retention or respond to any external command (except the MAXIMUM POWER SAVING MODE EXIT command and during the assertion of RESET_n signal LOW).



Mode register 5 (MR5) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR5 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR5 Register Definition table.

Table 19: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS _n	CAS _n	WE _n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	1	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 20: MR5 Register Definition

Mode Register	Description
21	RFU
	0 = Must be programmed to 0
	1 = Reserved
20:18	MR select
	000 = MR0
	001 = MR1
	010 = MR2
	011 = MR3
	100 = MR4
	101 = MR5
	110 = MR6
	111 = DNU
17	N/A on 4Gb and 8Gb, RFU
	0 = Must be programmed to 0
	1 = Reserved
13	RFU
	0 = Must be programmed to 0
	1 = Reserved
12	Data bus inversion (DBI) – READ DBI enable
	0 = Disabled
	1 = Enabled
11	Data bus inversion (DBI) – WRITE DBI enable
	0 = Disabled
	1 = Enabled
10	Data mask (DM)
	0 = Disabled
	1 = Enabled



Table 20: MR5 Register Definition (Continued)

Mode Register	Description
9	CA parity persistent error mode 0 = Disabled 1 = Enabled
8:6	Parked ODT value (R _{TT(Park)}) 000 = R _{TT(Park)} disabled 001 = RZQ/4 (60 ohm) 010 = RZQ/2 (120 ohm) 011 = RZQ/6 (40 ohm) 100 = RZQ/1 (240 ohm) 101 = RZQ/5 (48 ohm) 110 = RZQ/3 (80 ohm) 111 = RZQ/7 (34 ohm)
5	ODT input buffer for power-down 0 = Buffer enabled 1 = Buffer disabled
4	CA parity error status 0 = Clear 1 = Error
3	CRC error status 0 = Clear 1 = Error
2:0	CA parity latency mode 000 = Disable 001 = 4 clocks (DDR4-1600/1866/2133) 010 = 5 clocks (DDR4-2400/2666) ¹ 011 = 6 clocks (DDR4-2933/3200) 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved

Note: 1. Not allowed when 1/4 rate gear-down mode is enabled.

Data Bus Inversion

The DATA BUS INVERSION (DBI) function has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DBI function shares a common pin with the DM and TDQS functions. The DBI function applies to both READ and WRITE operations; Write DBI cannot be enabled at the same time the DM function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI). DBI is not allowed during MPR READ operation; during an MPR read, the DRAM ignores the read DBI enable setting in MR5 bit A12.

DBI is not supported for 3DS devices and should be disabled in MR5.



Data Mask

The DATA MASK (DM) function, also described as a partial write, has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DM function shares a common pin with the DBI and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the write DBI function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI).

CA Parity Persistent Error Mode

Normal CA parity mode (CA parity persistent mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA parity persistent mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

ODT Input Buffer for Power-Down

This feature determines whether the ODT input buffer is on or off during power-down. If the input buffer is configured to be on (enabled during power-down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power-down), the ODT input signal may be floating and the device does not provide $R_{\rm TT(NOM)}$ termination. However, the device may provide $R_{\rm TT(Park)}$ termination depending on the MR settings. This is primarily for additional power savings.

CA Parity Error Status

The device will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

CRC Error Status

The device will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

CA Parity Latency Mode

CA parity is enabled when a latency value, dependent on ^tCK, is programmed; this accounts for parity calculation delay internal to the device. The normal state of CA parity is to be disabled. If CA parity is enabled, the device must ensure there are no parity errors before executing the command. CA parity signal (PAR) covers ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, and the address bus including bank address and bank group bits. The control signals CKE, ODT, and CS_n are not included in the parity calculation.



Mode register 6 (MR6) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR6 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR6 Register Definition table.

Table 21: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS _n	CAS _n	WE _n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	1	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 22: MR6 Register Definition

Mode Register	Description
21	RFU 0 = Must be programmed to 0 1 = Reserved
20:18	MR select 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	NA on 4Gb and 8Gb, RFU 0 = Must be programmed to 0 1 = Reserved
12:10	Data Rate 000 = Data rate≤ 1333 Mb/s (1333 Mb/s) 001 = 1333 Mb/s <data (1600,="" (2133,="" (2666="" (2933,="" 010="1866" 011="2400" 100="2666" 101="Reserved" 110="Reserved" 111="Reserved</td" 1866="" 2400="" 3200="" <data="" mb="" rate="" s="" s)="" ≤1866="" ≤2400="" ≤2666="" ≤3200=""></data>



Table 22: MR6 Register Definition (Continued)

Mode Register	Description							
13, 9, 8	RFU							
	Default = 000; Must be programmed to 000							
	001 = Reserved							
	010 = Reserved							
	011 = Reserved							
	100 = Reserved							
	101 = Reserved							
	110 = Reserved							
	111 = Reserved							
7	V _{REF} Calibration Enable							
	0 = Disable							
	1 = Enable							
6	V _{REF} Calibration Range							
	0 = Range 1							
	1 = Range 2							
5:0	V _{REF} Calibration Value							
	See the V _{REFDQ} Range and Levels table in the V _{REFDQ} Calibration section							

Data Rate Programming

The device controller must program the correct data rate according to the operating frequency.

V_{REFDQ} Calibration Enable

 V_{REFDQ} calibration is where the device internally generates its own V_{REFDQ} to be used by the DQ input receivers. The V_{REFDQ} value will be output on any DQ of DQ[3:0] for evaluation only. The device controller is responsible for setting and calibrating the internal V_{REFDQ} level using an MRS protocol (adjust up, adjust down, and so on). It is assumed that the controller will use a series of writes and reads in conjunction with V_{REFDQ} adjustments to optimize and verify the data eye. Enabling V_{REFDQ} calibration must be used whenever values are being written to the MR6[6:0] register.

V_{REFDQ} Calibration Range

The device defines two V_{REFDQ} calibration ranges: Range 1 and Range 2. Range 1 supports V_{REFDQ} between 60% and 92% of V_{DDQ} while Range 2 supports V_{REFDQ} between 45% and 77% of V_{DDQ} , as seen in V_{REFDQ} Specification table. Although not a restriction, Range 1 was targeted for module-based designs and Range 2 was added to target point-to-point designs.

V_{REFDO} Calibration Value

Fifty settings provide approximately 0.65% of granularity steps sizes for both Range 1 and Range 2 of V_{REFDQ} , as seen in V_{REFDQ} Range and Levels table in the V_{REFDQ} Calibration section.

Truth Tables

Table 23: Truth Table - Command

Notes 1–5 apply to the entire table; Note 6 applies to all READ/WRITE commands

Function		Symbol	Prev. CKE	Pres. CKE	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	BG[1:0]	BA [1:0]	C[2:0]	A12/BC_n	A[13,11]	A10/AP	A[9:0]	Notes
MODE REGISTER SET		MRS	Н	Н	L	Н	L	L	L	BG	ВА	>		OP o	code		7
REFRESH		REF	Н	Н	L	Н	L	L	Н	V	V	٧	V	V	V	V	
Self refresh entry		SRE	Н	L	L	Н	L	L	Н	V	V	>	V	V	V	V	8, 9, 10
Self refresh exit		SRX	L	Н	Н	Х	Х	Х	Χ	Х	Х	Χ	Х	Х	Х	Х	8, 9, 10,
					L	Н	Н	Н	Н	V	V	٧	V	V	V	V	11
Single-bank PRECHARGE		PRE	Н	Н	L	Н	L	Н	L	BG	ВА	>	V	V	L	V	
PRECHARGE all banks		PREA	Н	Н	L	Н	L	Н	L	V	V	>	V	V	Н	V	
Reserved for	or future use	RFU	Н	Н	L	Н	L	Н	Н		RFU						
Bank ACTIVATE		ACT	Н	Н	L	L	Row	address	(RA)	BG	BG BA V Row address (RA)		A)				
WRITE	BL8 fixed, BC4 fixed	WR	Н	Н	L	Н	Н	L	L	BG	ВА	V	V	V	L	CA	
	BC4OTF	WRS4	Н	Н	L	Н	Н	L	L	BG	ВА	V	L	V	L	CA	
	BL8OTF	WRS8	Н	Н	L	Н	Н	L	L	BG	ВА	V	Н	V	L	CA	
WRITE	BL8 fixed, BC4 fixed	WRA	Н	Н	L	Н	Н	L	L	BG	ВА	V	V	V	Н	CA	
with auto	BC4OTF	WRAS4	Н	Н	L	Н	Н	L	L	BG	ВА	V	L	V	Н	CA	
precharge	BL8OTF	WRAS8	Н	Н	L	Н	Н	L	L	BG	ВА	V	Н	V	Н	CA	
READ	BL8 fixed, BC4 fixed	RD	Н	Н	L	Н	Н	L	Н	BG	ВА	V	V	V	L	CA	
	BC4OTF	RDS4	Н	Н	L	Н	Н	L	Н	BG	ВА	V	L	V	L	CA	
	BL8OTF	RDS8	Н	Н	L	Н	Н	L	Н	BG	ВА	V	Н	V	L	CA	
READ with auto precharge	BL8 fixed, BC4 fixed	RDA	Н	Н	L	Н	Н	L	Н	BG	ВА	V	V	V	Н	CA	
	BC4OTF	RDAS4	Н	Н	L	Н	Н	L	Н	BG	ВА	V	L	V	Н	CA	
	BL8OTF	RDAS8	Н	Н	L	Н	Н	L	Н	BG	ВА	V	Н	V	Н	CA	
NO OPERATION		NOP	Н	Н	L	Н	Н	Н	Н	V	V	V	V	V	V	V	12
Device DESELECTED		DES	Н	Н	Н	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	13
Power-down entry		PDE	Н	L	Н	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	10, 14
Power-down exit		PDX	L	Н	Н	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	10, 14
ZQ CALIBRATION LONG		ZQCL	Н	Н	L	Н	Н	Н	L	Х	Х	Х	Х	Х	Н	Х	
ZQ CALIBRATION SHORT		ZQCS	Н	Н	L	Н	Н	Н	L	Х	Х	Х	Х	Х	L	Х	



8Gb: x4, x8, x16 DDR4 SDRAM Truth Tables



Notes: 1. • BG = Bank group address

- BA = Bank address
- RA = Row address
- CA = Column address
- BC_n = Burst chop
- X = "Don't Care"
- V = Valid
- 2. All DDR4 SDRAM commands are defined by states of CS_n, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, and CKE at the rising edge of the clock. The MSB of BG, BA, RA, and CA are device density- and configuration-dependent. When ACT_n = H, pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as command pins RAS_n, CAS_n, and WE_n, respectively. When ACT_n = L, pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as address pins A16, A15, and A14, respectively.
- 3. RESET_n is enabled LOW and is used only for asynchronous reset and must be maintained HIGH during any function.
- 4. Bank group addresses (BG) and bank addresses (BA) determine which bank within a bank group is being operated upon. For MRS commands, the BG and BA selects the specific mode register location.
- 5. V means HIGH or LOW (but a defined logic level), and X means either defined or undefined (such as floating) logic level.
- 6. READ or WRITE bursts cannot be terminated or interrupted, and fixed/on-the-fly (OTF) BL will be defined by MRS.
- 7. During an MRS command, A17 is RFU and is device density- and configuration-dependent.
- 8. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh.
- 9. V_{PP} and V_{REF} (V_{REFCA}) must be maintained during SELF REFRESH operation.
- 10. Refer to the Truth Table CKE table for more details about CKE transition.
- 11. Controller guarantees self refresh exit to be synchronous. DRAM implementation has the choice of either synchronous or asynchronous.
- 12. The NO OPERATION (NOP) command may be used only when exiting maximum power saving mode or when entering gear-down mode.
- 13. The NOP command may not be used in place of the DESELECT command.
- 14. The power-down mode does not perform any REFRESH operation.



Table 24: Truth Table - CKE

Notes 1-7, 9, and 20 apply to the entire table

	CI	KE			
Current State	Previous Cycle (n - 1)	Present Cycle (n)	Command (n)	Action (n)	Notes
Power-down	L	L	Х	Maintain power-down	8, 10, 11
	L	Н	DES	Power-down exit	8, 10, 12
Self refresh	L	L	Х	Maintain self refresh	11, 13
	L	Н	DES	Self refresh exit	8, 13, 14, 15
Bank(s) active	Н	L	DES	Active power-down entry	8, 10, 12, 16
Reading	Н	L	DES	Power-down entry	8, 10, 12, 16, 17
Writing	Н	L	DES	Power-down entry	8, 10, 12, 16, 17
Precharging	Н	L	DES	Power-down entry	8, 10, 12, 16, 17
Refreshing	Н	L	DES	Precharge power-down entry	8, 12
All banks idle	Н	L	DES	Precharge power-down entry	8, 10, 12, 16, 18
	Н	L	REFRESH	Self refresh	16, 18, 19

- Notes: 1. Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge n.
 - 2. CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.
 - 3. COMMAND (n) is the command registered at clock edge n, and ACTION (n) is a result of COMMAND (n); ODT is not included here.
 - 4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
 - 5. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh.
 - 6. During any CKE transition (registration of CKE H->L), the CKE level must be maintained until 1 nCK prior to ^tCKE (MIN) being satisfied (at which time CKE may transition again).
 - 7. DESELECT and NOP are defined in the Truth Table Command table.
 - 8. For power-down entry and exit parameters, see the Power-Down Modes section.
 - 9. CKE LOW is allowed only if ^tMRD and ^tMOD are satisfied.
 - 10. The power-down mode does not perform any REFRESH operations.
 - 11. X = "Don't Care" (including floating around V_{RFF}) in self refresh and power-down. X also applies to address pins.
 - 12. The DESELECT command is the only valid command for power-down entry and exit.
 - 13. V_{PP} and V_{RFFCA} must be maintained during SELF REFRESH operation.
 - 14. On self refresh exit, the DESELECT command must be issued on every clock edge occurring during the ^tXS period. READ or ODT commands may be issued only after ^tXSDLL is satisfied.
 - 15. The DESELECT command is the only valid command for self refresh exit.
 - 16. Self refresh cannot be entered during READ or WRITE operations. For a detailed list of restrictions see the SELF REFRESH Operation and Power-Down Modes sections.
 - 17. If all banks are closed at the conclusion of the READ, WRITE, or PRECHARGE command, then precharge power-down is entered; otherwise, active power-down is entered.



- 18. Idle state is defined as all banks are closed ([†]RP, [†]DAL, and so on, satisfied), no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied ([†]MRD, [†]MOD, [†]RFC, [†]ZQinit, [†]ZQoper, [†]ZQCS, and so on), as well as all self refresh exit and power-down exit parameters are satisfied ([†]XS, [†]XP, [†]XSDLL, and so on).
- 19. Self refresh mode can be entered only from the all banks idle state.
- 20. For more details about all signals, see the Truth Table Command table; must be a legal command as defined in the table.

NOP Command

The NO OPERATION (NOP) command was originally used to instruct the selected DDR4 SDRAM to perform a NOP (CS_n = LOW and ACT_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 = HIGH). This prevented unwanted commands from being registered during idle or wait states. NOP command general support has been removed and the command should not be used unless specifically allowed, which is when exiting maximum power-saving mode or when entering gear-down mode.

DESELECT Command

The deselect function (CS_n HIGH) prevents new commands from being executed; therefore, with this command, the device is effectively deselected. Operations already in progress are not affected.

DLL-Off Mode

DLL-off mode is entered by setting MR1 bit A0 to 0, which will disable the DLL for subsequent operations until the A0 bit is set back to 1. The MR1 A0 bit for DLL control can be switched either during initialization or during self refresh mode. Refer to the Input Clock Frequency Change section for more details.

The maximum clock frequency for DLL-off mode is specified by the parameter ^tCKDLL OFF.

Due to latency counter and timing restrictions, only one CL value and CWL value (in MR0 and MR2 respectively) are supported. The DLL-off mode is only required to support setting both CL = 10 and CWL = 9.

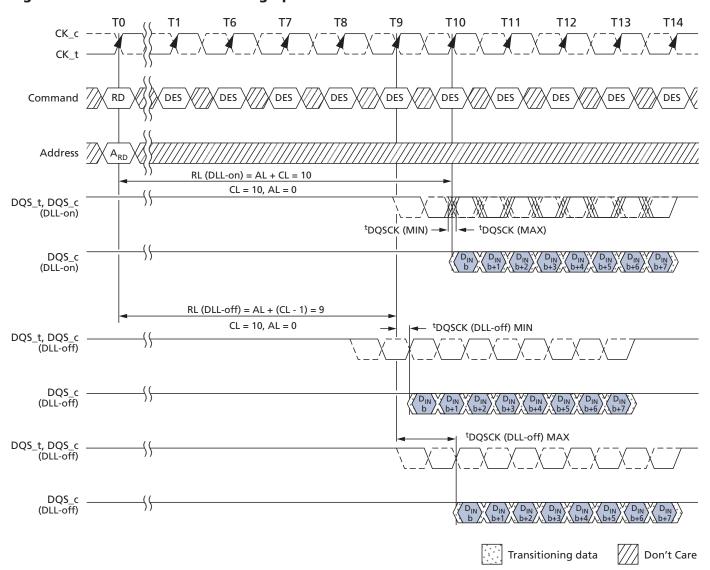
DLL-off mode will affect the read data clock-to-data strobe relationship (^tDQSCK), but not the data strobe-to-data relationship (^tDQSQ, ^tQH). Special attention is needed to line up read data to the controller time domain.

Compared with DLL-on mode, where tDQSCK starts from the rising clock edge (AL + CL) cycles after the READ command, the DLL-off mode tDQSCK starts (AL + CL - 1) cycles after the READ command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK), and the difference between tDQSCK (MIN) and tDQSCK (MAX) is significantly larger than in DLL-on mode. The tDQSCK (DLL-off) values are undefined and the user is responsible for training to the data-eye.

The timing relations on DLL-off mode READ operation are shown in the following diagram, where CL = 10, AL = 0, and BL = 8.



Figure 19: DLL-Off Mode Read Timing Operation





DLL-On/Off Switching Procedures

The DLL-off mode is entered by setting MR1 bit A0 to 0; this will disable the DLL for subsequent operations until the A0 bit is set back to 1.

DLL Switch Sequence from DLL-On to DLL-Off

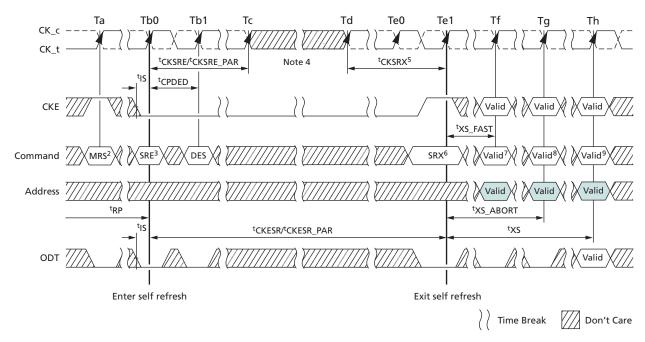
To switch from DLL-on to DLL-off requires the frequency to be changed during self refresh, as outlined in the following procedure:

- 1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and, to disable the DLL, the DRAM on-die termination resistors, $R_{TT(NOM)}$, must be in High-Z before MRS to MR1.)
- 2. Set MR1 bit A0 to 1 to disable the DLL.
- 3. Wait ^tMOD.
- 4. Enter self refresh mode; wait until ^tCKSRE/^tCKSRE_PAR is satisfied.
- 5. Change frequency, following the guidelines in the Input Clock Frequency Change section.
- 6. Wait until a stable clock is available for at least ^tCKSRX at device inputs.
- 7. Starting with the SELF REFRESH EXIT command, CKE must continuously be registered HIGH until all ^tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW until all ^tMOD timings from any MRS command are satisfied. If R_{TT(NOM)} was disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
- 8. Wait ^tXS_FAST, ^tXS_ABORT, or ^tXS, and then set mode registers with appropriate values (an update of CL, CWL, and WR may be necessary; a ZQCL command can also be issued after ^tXS_FAST).
 - ^tXS_FAST: ZQCL, ZQCS, and MRS commands. For MRS commands, only CL and WR/RTP registers in MR0, the CWL register in MR2, and gear-down mode in MR3 may be accessed provided the device is not in per-DRAM addressability mode. Access to other device mode registers must satisfy ^tXS timing.
 - ^tXS_ABORT: If MR4 [9] is enabled, then the device aborts any ongoing refresh
 and does not increment the refresh counter. The controller can issue a valid
 command after a delay of ^tXS_ABORT. Upon exiting from self refresh, the device
 requires a minimum of one extra REFRESH command before it is put back into
 self refresh mode. This requirement remains the same regardless of the MRS bit
 setting for self refresh abort.
 - ^tXS: ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, and RDAS8.
- 9. Wait ^tMOD to complete.

The device is ready for the next command.



Figure 20: DLL Switch Sequence from DLL-On to DLL-Off



- Notes: 1. Starting in the idle state. R_{TT} in stable state.
 - 2. Disable DLL by setting MR1 bit A0 to 0.
 - 3. Enter SR.
 - 4. Change frequency.
 - 5. Clock must be stable ^tCKSRX.
 - 6. Exit SR.
 - 7. Update mode registers allowed with DLL-off settings met.



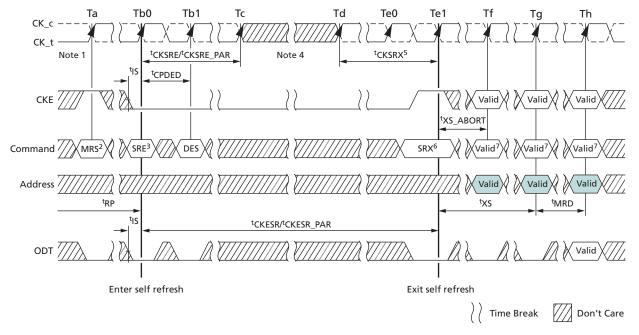
DLL-Off to DLL-On Procedure

To switch from DLL-off to DLL-on (with required frequency change) during self refresh:

- 1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and DRAM ODT resistors ($R_{TT(NOM)}$) must be in High-Z before self refresh mode is entered.)
- 2. Enter self refresh mode; wait until ^tCKSRE/^tCKSRE_PAR are satisfied.
- 3. Change frequency (following the guidelines in the Input Clock Frequency Change section).
- 4. Wait until a stable clock is available for at least ^tCKSRX at device inputs.
- 5. Starting with the SELF REFRESH EXIT command, CKE must continuously be registered HIGH until ^tDLLK timing from the subsequent DLL RESET command is satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW or HIGH until ^tDLLK timing from the subsequent DLL RESET command is satisfied. If R_{TT(NOM)} disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
- 6. Wait ^tXS or ^tXS_ABORT, depending on bit 9 in MR4, then set MR1 bit A0 to 0 to enable the DLL.
- 7. Wait ^tMRD, then set MR0 bit A8 to 1 to start DLL reset.
- 8. Wait ^tMRD, then set mode registers with appropriate values; an update of CL, CWL, and WR may be necessary. After ^tMOD is satisfied from any proceeding MRS command, a ZQCL command can also be issued during or after ^tDLLK.
- 9. Wait for ^tMOD to complete. Remember to wait ^tDLLK after DLL RESET before applying any command requiring a locked DLL. In addition, wait for ^tZQoper in case a ZQCL command was issued.

The device is ready for the next command.

Figure 21: DLL Switch Sequence from DLL-Off to DLL-On



Notes: 1. Starting in the idle state.



- 2. Enter SR.
- 3. Change frequency.
- 4. Clock must be stable ^tCKSRX.
- 5. Exit SR.
- 6. Set DLL to on by setting MR1 to A0 = 0.
- 7. Update mode registers.
- 8. Issue any valid command.

Input Clock Frequency Change

After the device is initialized, it requires the clock to be stable during almost all states of normal operation. This means that after the clock frequency has been set and is in the stable state, the clock period is not allowed to deviate except for what is allowed by the clock jitter and spread spectrum clocking (SSC) specifications. The input clock frequency can be changed from one stable clock rate to another stable clock rate only when in self refresh mode. Outside of self refresh mode, it is illegal to change the clock frequency.

After the device has been successfully placed in self refresh mode and ^tCKSRE/ ^tCKSRE_PAR have been satisfied, the state of the clock becomes a "Don't Care." Following a "Don't Care," changing the clock frequency is permissible, provided the new clock frequency is stable prior to ^tCKSRX. When entering and exiting self refresh mode for the sole purpose of changing the clock frequency, the self refresh entry and exit specifications must still be met as outlined in SELF REFRESH Operation.

For the new clock frequency, additional MRS commands to MR0, MR2, MR3, MR4, MR5, and MR6 may need to be issued to program appropriate CL, CWL, gear-down mode, READ and WRITE preamble, Command Address Latency, and data rate values.

When the clock rate is being increased (faster), the MR settings that require additional clocks should be updated prior to the clock rate being increased. In particular, the PL latency must be disabled when the clock rate changes, ie. while in self refresh mode. For example, if changing the clock rate from DDR4-2133 to DDR4-2933 with CA parity mode enabled, MR5[2:0] must first change from PL = 4 to PL = disable prior to PL = 6. The correct procedure would be to (1) change PL = 4 to disable via MR5 [2:0], (2) enter self refresh mode, (3) change clock rate from DDR4-2133 to DDR4-2933, (4) exit self refresh mode, (5) Enable CA parity mode setting PL = 6 vis MR5 [2:0].

If the MR settings that require additional clocks are updated after the clock rate has been increased, for example. after exiting self refresh mode, the required MR settings must be updated prior to removing the DRAM from the IDLE state, unless the DRAM is RESET. If the DRAM leaves the IDLE state to enter self refresh mode or ZQ Calibration, the updating of the required MR settings may be deferred to the next time the DRAM enters the IDLE state.

If MR6 is issued prior to self refresh entry for the new data rate value, DLL will relock automatically at self refresh exit. However, if MR6 is issued after self refresh entry, MR0 must be issued to reset the DLL.

The device input clock frequency can change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL-on mode to DLL-off mode transition sequence (see DLL-On/Off Switching Procedures).

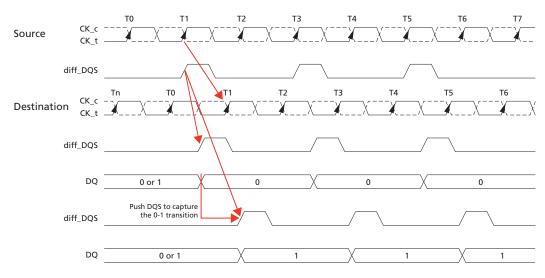


Write Leveling

For better signal integrity, DDR4 memory modules use fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology has benefits from the reduced number of stubs and their length, but it also causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain [†]DQSS, [†]DSS, and [†]DSH specifications. Therefore, the device supports a write leveling feature to allow the controller to compensate for skew. This feature may not be required under some system conditions, provided the host can maintain the [†]DQSS, [†]DSS, and [†]DSH specifications.

The memory controller can use the write leveling feature and feedback from the device to adjust the DQS (DQS_t, DQS_c) to CK (CK_t, CK_c) relationship. The memory controller involved in the leveling must have an adjustable delay setting on DQS to align the rising edge of DQS with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK, sampled with the rising edge of DQS, through the DQ bus. The controller repeatedly delays DQS until a transition from 0 to 1 is detected. The DQS delay established though this exercise would ensure the ¹DQSS specification. Besides ¹DQSS, ¹DSS and ¹DSH specifications also need to be fulfilled. One way to achieve this is to combine the actual ¹DQSS in the application with an appropriate duty cycle and jitter on the DQS signals. Depending on the actual ¹DQSS in the application, the actual values for ¹DQSL and ¹DQSH may have to be better than the absolute limits provided in the AC Timing Parameters section in order to satisfy ¹DSS and ¹DSH specifications. A conceptual timing of this scheme is shown below.

Figure 22: Write Leveling Concept, Example 1



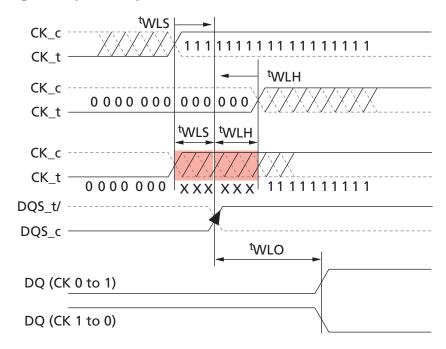
DQS driven by the controller during leveling mode must be terminated by the DRAM based on the ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits carry the leveling feedback to the controller across the DRAM configurations: x4, x8, and x16. On a x16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS)-to-clock relationship; the lower data bits would indicate the lower diff_DQS(diff_LDQS)-to-clock relationship.



The figure below is another representative way to view the write leveling procedure. Although it shows the clock varying to a static strobe, this is for illustrative purpose only; the clock does not actually change phase, the strobe is what actually varies. By issuing multiple WL bursts, the DQS strobe can be varied to capture with fair accuracy the time at which the clock edge arrives at the DRAM clock input buffer.

Figure 23: Write Leveling Concept, Example 2



DRAM Setting for Write Leveling and DRAM TERMINATION Function in that Mode

The DRAM enters into write leveling mode if A7 in MR1 is HIGH. When leveling is finished, the DRAM exits write leveling mode if A7 in MR1 is LOW (see the MR Leveling Procedures table). Note that in write leveling mode, only DQS terminations are activated and deactivated via the ODT pin, unlike normal operation (see DRAM DRAM TERMINATION Function in Leveling Mode table).

Table 25: MR Settings for Leveling Procedures

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Q off)	A12	0	1

Table 26: DRAM TERMINATION Function in Leveling Mode

ODT Pin at DRAM	DQS_t/DQS_c Termination	DQ Termination		
R _{TT(NOM)} with ODT HIGH	On	Off		



Table 26: DRAM TERMINATION Function in Leveling Mode (Continued)

ODT Pin at DRAM	DQS_t/DQS_c Termination	DQ Termination
R _{TT(Park)} with ODT LOW	On	Off

Notes

- 1. In write leveling mode, with the mode's output buffer either disabled (MR1[bit7] = 1 and MR1[bit12] = 1) or with its output buffer enabled (MR1[bit7] = 1 and MR1[bit12] = 0), all $R_{TT(NOM)}$ and $R_{TT(Park)}$ settings are supported.
- 2. R_{TT(WR)} is not allowed in write leveling mode and must be set to disable prior to entering write leveling mode.

Procedure Description

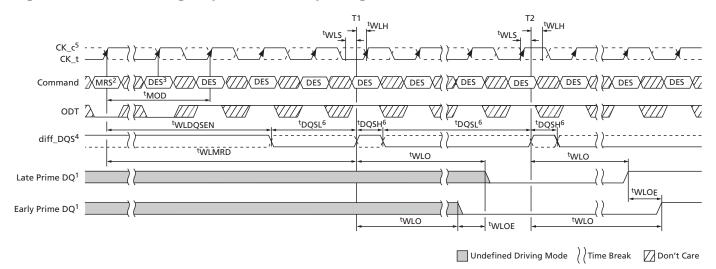
The memory controller initiates the leveling mode of all DRAM by setting bit 7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only the DESELECT command is supported, other than MRS commands to change the Qoff bit (MR1[A12]) and to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7] = 0) may also change the other MR1 bits. Because the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The controller may assert ODT after $^{\rm t}$ MOD, at which time the DRAM is ready to accept the ODT signal, unless DODTLon or DODTLoff have been altered (the ODT internal pipe delay is increased when increasing WRITE latency [WL] or READ latency [RL] by the previous MR command), then ODT assertion should be delayed by DODTLon after $^{\rm t}$ MOD is satisfied, which means the delay is now $^{\rm t}$ MOD + DODTLon.

The controller may drive DQS_t LOW and DQS_c HIGH after a delay of twLDQSEN, at which time the DRAM has applied ODT to these signals. After tDQSL and tWLMRD, the controller provides a single DQS_t, DQS_c edge, which is used by the DRAM to sample CK driven from the controller. tWLMRD (MAX) timing is controller dependent.

The DRAM samples CK status with the rising edge of DQS and provides feedback on all the DQ bits asynchronously after ^tWLO timing. There is a DQ output uncertainty of ^tWLOE defined to allow mismatch on DQ bits. The ^tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS_t, DQS_c) needed for these DQs. The controller samples incoming DQ and either increments or decrements DQS delay setting and launches the next DQS pulse after some time, which is controller dependent. After a 0-to-1 transition is detected, the controller locks the DQS delay setting, and write leveling is achieved for the device. The following figure shows the timing diagram and parameters for the overall write leveling procedure.



Figure 24: Write Leveling Sequence (DQS Capturing CK LOW at T1 and CK HIGH at T2)



Notes

- 1. The device drives leveling feedback on all DQs.
- 2. MRS: Load MR1 to enter write leveling mode.
- 3. diff_DQS is the differential data strobe. Timing reference points are the zero crossings. DQS_t is shown with a solid line; DQS_c is shown with a dotted line.
- 4. CK_t is shown with a solid dark line; CK_c is shown with a dotted line.
- 5. DQS needs to fulfill minimum pulse width requirements, ^tDQSH (MIN) and ^tDQSL (MIN), as defined for regular WRITEs; the maximum pulse width is system dependent.
- 6. ${}^{t}WLDQSEN$ must be satisfied following equation when using ODT:
 - DLL = Enable, then ^tWLDQSEN > ^tMOD (MIN) + DODTLon + ^tADC
 - DLL = Disable, then ^tWLDQSEN > ^tMOD (MIN) + ^tAONAS

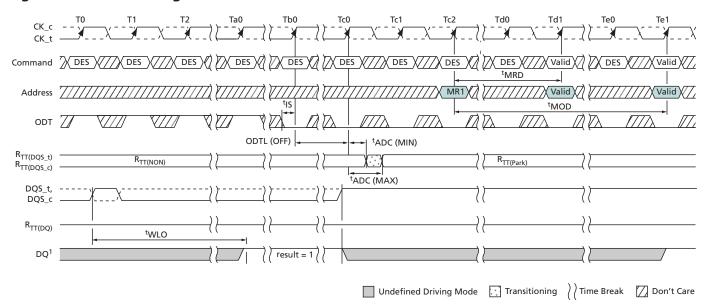
Write Leveling Mode Exit

Write leveling mode should be exited as follows:

- 1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note that from this point on, DQ pins are in undefined driving mode and will remain undefined, until ^tMOD after the respective MR command (Te1).
- 2. Drive ODT pin LOW (tIS must be satisfied) and continue registering LOW (see Tb0).
- 3. After R_{TT} is switched off, disable write leveling mode via the MRS command (see Tc2).
- 4. After ^tMOD is satisfied (Te1), any valid command can be registered. (MR commands can be issued after ^tMRD [Td1]).



Figure 25: Write Leveling Exit



otes: 1. The DQ result = 1 between Ta0 and Tc0 is a result of the DQS signals capturing CK_t HIGH just after the T0 state.

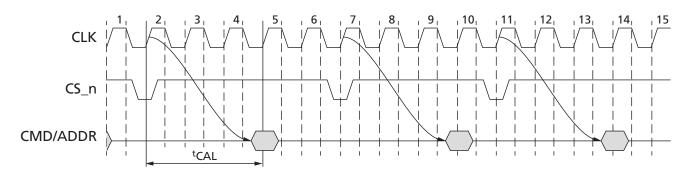
2. See previous figure for specific ^tWLO timing.



Command Address Latency

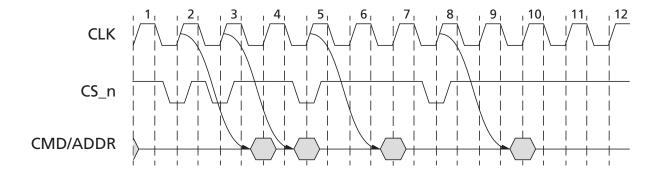
DDR4 supports the command address latency (CAL) function as a power savings feature. This feature can be enabled or disabled via the MRS setting. CAL timing is defined as the delay in clock cycles (^tCAL) between a CS_n registered LOW and its corresponding registered command and address. The value of CAL in clocks must be programmed into the mode register (see MR1 Register Definition table) and is based on the ^tCAL(ns)/
^tCK(ns) rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section.

Figure 26: CAL Timing Definition



CAL gives the DRAM time to enable the command and address receivers before a command is issued. After the command and the address are latched, the receivers can be disabled if CS_n returns to HIGH. For consecutive commands, the DRAM will keep the command and address input receivers enabled for the duration of the command sequence.

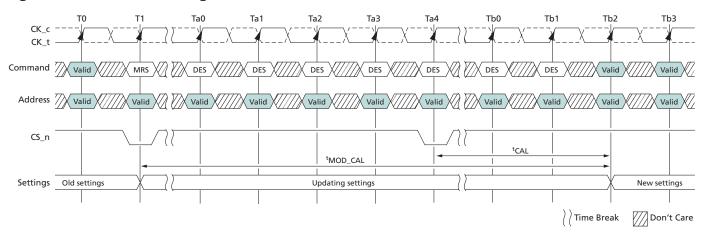
Figure 27: CAL Timing Example (Consecutive CS n = LOW)





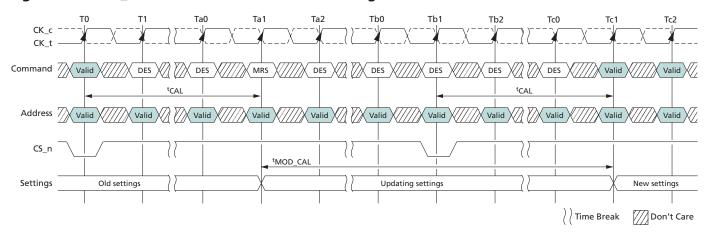
When the CAL mode is enabled, additional time is required for the MRS command to complete. The earliest the next valid command can be issued is ${}^{t}MOD_CAL$, which should be equal to ${}^{t}MOD + {}^{t}CAL$. The two following figures are examples.

Figure 28: CAL Enable Timing – ^tMOD_CAL



Note: 1. CAL mode is enabled at T1.

Figure 29: tMOD_CAL, MRS to Valid Command Timing with CAL Enabled

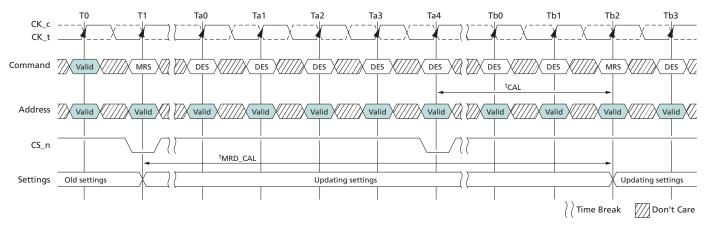


Note: 1. MRS at Ta1 may or may not modify CAL, ^tMOD_CAL is computed based on new ^tCAL setting if modified.



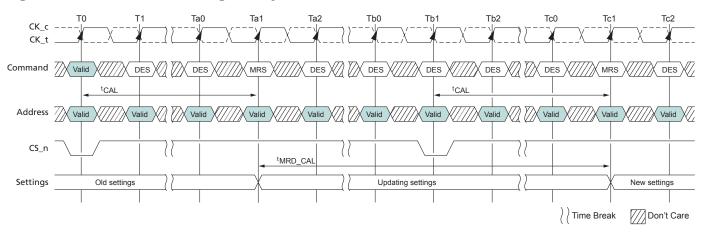
When the CAL mode is enabled or being enabled, the earliest the next MRS command can be issued is ^tMRD_CAL is equal to ^tMOD + ^tCAL. The two following figures are examples.

Figure 30: CAL Enabling MRS to Next MRS Command, ^tMRD_CAL



Note: 1. Command address latency mode is enabled at T1.

Figure 31: tMRD_CAL, Mode Register Cycle Time With CAL Enabled

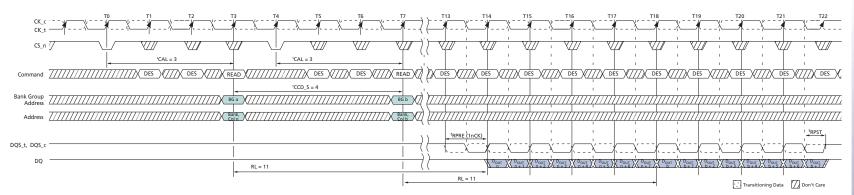


Note: 1. MRS at Ta1 may or may not modify CAL, ^tMRD_CAL is computed based on new ^tCAL setting if modified.

CAL Examples: Consecutive READ BL8 with two different CALs and 1^tCK preamble in different bank group shown in the following figures.

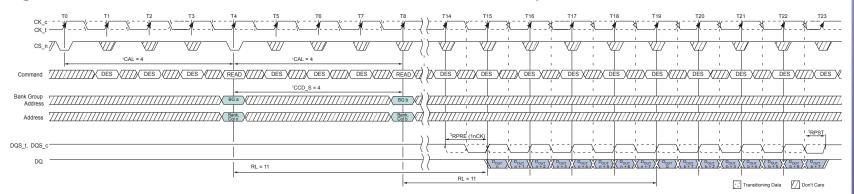
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Figure 32: Consecutive READ BL8, CAL3, 1^tCK Preamble, Different Bank Group



- Notes: 1. BL = 8, AL = 0, CL = 11, CAL = 3, Preamble = 1^tCK.
 - 2. D_{OUT} n = data-out from column n; D_{OUT} b = data-out from column b.
 - 3. DES commands are shown for ease of illustration, other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T3 and T7.
 - 5. CA parity = Disable, CS to CA latency = Enable, Read DBI = Disable.
 - 6. Enabling CAL mode does not impact ODT control timings. ODT control timings should be maintained with the same timing relationship relative to the command/address bus as when CAL is disabled.

Figure 33: Consecutive READ BL8, CAL4, 1^tCK Preamble, Different Bank Group



- Notes: 1. BL = 8, AL = 0, CL = 11, CAL = 4, Preamble = 1^tCK.
 - 2. D_{OUT} n = data-out from column n; D_{OUT} b = data-out from column b.
 - 3. DES commands are shown for ease of illustration, other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T4 and T8.



8Gb: x4, x8, x16 DDR4 Command Address

SDRAM Latency

- 5. CA parity = Disable, CS to CA latency = Enable, Read DBI = Disable.
- 6. Enabling CAL mode does not impact ODT control timings. ODT control timings should be maintained with the same timing relationship relative to the command/address bus as when CAL is disabled.



Low-Power Auto Self Refresh Mode

An auto self refresh mode is provided for application ease. Auto self refresh mode is enabled by setting MR2[6] = 1 and MR2[7] = 1. The device will manage self refresh entry over the supported temperature range of the DRAM. In this mode, the device will change its self refresh rate as the DRAM operating temperature changes, going lower at low temperatures and higher at high temperatures.

Manual Self Refresh Mode

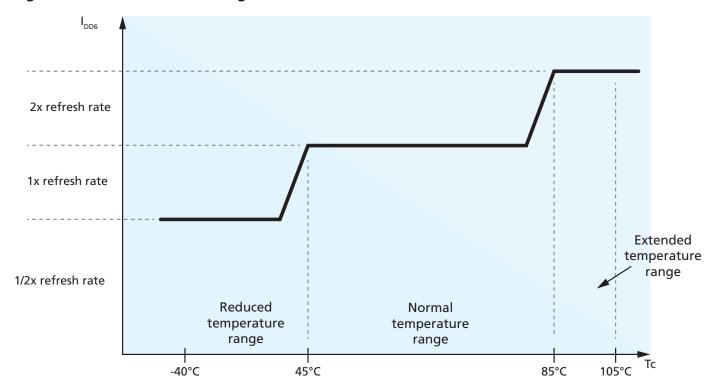
If auto self refresh mode is not enabled, the low-power auto self refresh mode register must be manually programmed to one of the three self refresh operating modes. This mode provides the flexibility to select a fixed self refresh operating mode at the entry of the self refresh, according to the system memory temperature conditions. The user is responsible for maintaining the required memory temperature condition for the mode selected during the SELF REFRESH operation. The user may change the selected mode after exiting self refresh and before entering the next self refresh. If the temperature condition is exceeded for the mode selected, there is a risk to data retention resulting in loss of data.

Table 27: Auto Self Refresh Mode

MR2[7]	MR2[6]	Low-Power Auto Self Refresh Mode	SELF REFRESH Operation	Operating Temperature Range for Self Refresh Mode (DRAM T _{CASE})
0	0	Normal	Variable or fixed normal self refresh rate maintains data retention at the normal operating temperature. User is required to ensure that 85°C DRAM T _{CASE} (MAX) is not exceeded to avoid any risk of data loss.	-40°C to 85°C
1	0	Extended temperature	Variable or fixed high self refresh rate optimizes data retention to support the extended temperature range.	-40°C to 105°C
0	1	Reduced temperature	Variable or fixed self refresh rate or any other DRAM power consumption reduction control for the reduced temperature range. User is required to ensure 45°C DRAM T _{CASE} (MAX) is not exceeded to avoid any risk of data loss.	-40°C to 45°C
1	1	Auto self refresh	Auto self refresh mode enabled. Self refresh power consumption and data retention are optimized for any given operating temperature condition.	All of the above



Figure 34: Auto Self Refresh Ranges





Multipurpose Register

The MULTIPURPOSE REGISTER (MPR) function, MPR access mode, is used to write/read specialized data to/from the DRAM. The MPR consists of four logical pages, MPR Page 0 through MPR Page 3, with each page having four 8-bit registers, MPR0 through MPR3. Page 0 can be read by any of three readout modes (serial, parallel, or staggered) while Pages 1, 2, and 3 can be read by only the serial readout mode. Page 3 is for DRAM vendor use only. MPR mode enable and page selection is done with MRS commands. Data bus inversion (DBI) is not allowed during MPR READ operation.

Once the MPR access mode is enabled (MR3[2] = 1), only the following commands are allowed: MRS, RD, RDA WR, WRA, DES, REF, and RESET; RDA/WRA have the same functionality as RD/WR which means the auto precharge part of RDA/WRA is ignored. Power-down mode and SELF REFRESH command are not allowed during MPR enable mode. No other command can be issued within ^tRFC after a REF command has been issued; 1x refresh (only) is to be used during MPR access mode. While in MPR access mode, MPR read or write sequences must be completed prior to a REFRESH command.

Figure 35: MPR Block Diagram

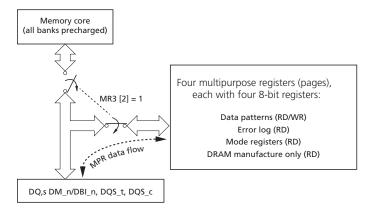


Table 28: MR3 Setting for the MPR Access Mode

Address	Operation Mode	Description
A[12:11]	MPR data read format	00 = Serial 01 = Parallel
		10 = Staggered 11 = Reserved
A2	MPR access	0 = Standard operation (MPR not enabled)
		1 = MPR data flow enabled
A[1:0]	MPR page selection	00 = Page 0 01 = Page 1
		10 = Page 2 11 = Page 3

Table 29: DRAM Address to MPR UI Translation

MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
DRAM address – Ax	A7	A6	A5	A4	A3	A2	A1	A0
MPR UI – UIx	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7



Table 30: MPR Page and MPRx Definitions

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note	
MPR Page	0 – Read or Wri	te (Data F	atterns)			•					
BA[1:0]	00 = MPR0	0	1	0	1	0	1	0	1	Read/	
	01 = MPR1	0	0	1	1	0	0	1	1	Write	
	10 = MPR2	0	0	0	0	1	1	1	1	(default value lis-	
	11 = MPR3	0	0	0	0	0	0	0	0	ted)	
MPR Page	1 – Read-only (I	Error Log)									
BA[1:0]	00 = MPR0	A7	A6	A5	A4	A3	A2	A1	A0	Read-on-	
	01 = MPR1	CAS_n/A 15	WE_n/A1 4	A13	A12	A11	A10	A9	A8	ly	
	10 = MPR2	PAR	ACT_n	BG1	BG0	BA1	BA0	A17	RAS_n/A 16		
	11 = MPR3	CRC er- ror sta- tus	CA pari- ty error status		rity latency [4] = MR5 MR5[0]		C2	C1	C0		
MPR Page	2 – Read-only (I	MRS Read	out)								
BA[1:0]	00 = MPR0	hPPR support	sPPR support	11(VII)				R _{TT(WR)} N	/IR2[10:9]	Read-on- ly	
	01 = MPR1	V _{REFDQ} traing- ing range MR6[6]		V _{REFDQ} tı	raining val	ue: [6:1] =	MR6[5:0]	Gear- down enable MR3[3]			
	10 = MPR2	C	AS latency	: [7:3] = M	R0[6:4,2,1	2]		te latency MR2[5:3]	[2:0] =		
	11 = MPR3	R _{TT(NOM)}	: [7:5] = M	R1[10:8]	R _{TT(Park}	(): [4:2] = N	/IR5[8:6]	R _{ON} : [1:0] = MR2[2:1]			
MPR Page	3 – Read-only (I	Restricted	l, except f	or MPR3	[3:0])						
BA[1:0]	00 = MPR0	DC	DC	DC	DC	DC	DC	DC	DC	Read-on-	
	01 = MPR1	DC	DC	DC	DC	DC	DC	DC	DC	ly	
	10 = MPR2	DC	DC	DC	DC	DC	DC	DC	DC		
	11 = MPR3	DC	DC	DC	DC	MAC	MAC	MAC	MAC		

- Notes: 1. DC = "Don't Care"
 - 2. MPR[4:3] 00 = Sub 1X refresh; MPR[4:3] 01 = 1X refresh; MPR[4:3] 10 = 2X refresh; MPR[4:3] 11 = Reserved

MPR Reads

MPR reads are supported using BL8 and BC4 modes. Burst length on-the-fly is not supported for MPR reads. Data bus inversion (DBI) is not allowed during MPR READ operation; the device will ignore the Read DBI enable setting in MR5 [12] when in MPR mode. READ commands for BC4 are supported with a starting column address of A[2:0] = 000



or 100. After power-up, the content of MPR Page 0 has the default values, which are defined in Table 30. MPR page 0 can be rewritten via an MPR WRITE command. The device maintains the default values unless it is rewritten by the DRAM controller. If the DRAM controller does overwrite the default values (Page 0 only), the device will maintain the new values unless re-initialized or there is power loss.

Timing in MPR mode:

- Reads (back-to-back) from Page 0 may use ^tCCD_S or ^tCCD_L timing between READ commands
- Reads (back-to-back) from Pages 1, 2, or 3 may not use ^tCCD_S timing between READ commands; ^tCCD_L must be used for timing between READ commands

The following steps are required to use the MPR to read out the contents of a mode register (MPR Page x, MPRy).

- 1. The DLL must be locked if enabled.
- 2. Precharge all; wait until ^tRP is satisfied.
- 3. MRS command to MR3[2] = 1 (Enable MPR data flow), MR3[12:11] = MPR read format, and MR3[1:0] MPR page.
 - a. MR3[12:11] MPR read format:
 - 1. 00 = Serial read format
 - 2. 01 = Parallel read format
 - 3. 10 = staggered read format
 - 4. 11 = RFU
 - b. MR3[1:0] MPR page:
 - 1. 00 = MPR Page 0
 - 2. 01 = MPR Page 1
 - 3. 10 = MPR Page 2
 - 4. 11 = MPR Page 3
- 4. ^tMRD and ^tMOD must be satisfied.
- 5. Redirect all subsequent READ commands to specific MPRx location.
- 6. Issue RD or RDA command.
 - a. BA1 and BA0 indicate MPRx location:
 - 1. 00 = MPR0
 - 2. 01 = MPR1
 - 3. 10 = MPR2
 - 4. 11 = MPR3
 - b. A12/BC = 0 or 1; BL8 or BC4 fixed-only, BC4 OTF not supported.
 - 1. If BL = 8 and MR0 A[1:0] = 01, A12/BC must be set to 1 during MPR READ commands.
 - c. A2 = burst-type dependant:
 - 1. BL8: A2 = 0 with burst order fixed at 0, 1, 2, 3, 4, 5, 6, 7
 - 2. BL8: A2 = 1 not allowed
 - 3. BC4: A2 = 0 with burst order fixed at 0, 1, 2, 3, T, T, T, T
 - 4. BC4: A2 = 1 with burst order fixed at 4, 5, 6, 7, T, T, T,
 - d. A[1:0] = 00, data burst is fixed nibble start at 00.
 - e. Remaining address inputs, including A10, and BG1 and BG0 are "Don't Care."
- 7. After RL = AL + CL, DRAM bursts data from MPRx location; MPR readout format determined by MR3[A12,11,1,0].
- 8. Steps 5 through 7 may be repeated to read additional MPRx locations.
- 9. After the last MPRx READ burst, ^tMPRR must be satisfied prior to exiting.
- 10. Issue MRS command to exit MPR mode; MR3[2] = 0.



11. After the ^tMOD sequence is completed, the DRAM is ready for normal operation from the core (such as ACT).

MPR Readout Format

The MPR read data format can be set to three different settings: serial, parallel, and staggered.

MPR Readout Serial Format

The serial format is required when enabling the MPR function to read out the contents of an MR*x*, temperature sensor status, and the command address parity error frame. However, data bus calibration locations (four 8-bit registers) can be programmed to read out any of the three formats. The DRAM is required to drive associated strobes with the read data similar to normal operation (such as using MRS preamble settings).

Serial format implies that the same pattern is returned on all DQ lanes, as shown the table below, which uses values programmed into the MPR via [7:0] as 0111 1111.

Table 31: MPR Readout Serial Format

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7		
x4 Device										
DQ0	0	1	1	1	1	1	1	1		
DQ1	0	1	1	1	1	1	1	1		
DQ2	0	1	1	1	1	1	1	1		
DQ3	0	1	1	1	1	1	1	1		
x8 Device										
DQ0	0	1	1	1	1	1	1	1		
DQ1	0	1	1	1	1	1	1	1		
DQ2	0	1	1	1	1	1	1	1		
DQ3	0	1	1	1	1	1	1	1		
DQ4	0	1	1	1	1	1	1	1		
DQ5	0	1	1	1	1	1	1	1		
DQ6	0	1	1	1	1	1	1	1		
DQ7	0	1	1	1	1	1	1	1		
x16 Device										
DQ0	0	1	1	1	1	1	1	1		
DQ1	0	1	1	1	1	1	1	1		
DQ2	0	1	1	1	1	1	1	1		
DQ3	0	1	1	1	1	1	1	1		
DQ4	0	1	1	1	1	1	1	1		
DQ5	0	1	1	1	1	1	1	1		
DQ6	0	1	1	1	1	1	1	1		
DQ7	0	1	1	1	1	1	1	1		
DQ8	0	1	1	1	1	1	1	1		



Table 31: MPR Readout Serial Format (Continued)

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ9	0	1	1	1	1	1	1	1
DQ10	0	1	1	1	1	1	1	1
DQ11	0	1	1	1	1	1	1	1
DQ12	0	1	1	1	1	1	1	1
DQ13	0	1	1	1	1	1	1	1
DQ14	0	1	1	1	1	1	1	1
DQ15	0	1	1	1	1	1	1	1

MPR Readout Parallel Format

Parallel format implies that the MPR data is returned in the first data UI and then repeated in the remaining UIs of the burst, as shown in the table below. Data pattern location 0 is the only location used for the parallel format. RD/RDA from data pattern locations 1, 2, and 3 are not allowed with parallel data return mode. In this example, the pattern programmed in the data pattern location 0 is 0111 1111. The x4 configuration only outputs the first four bits (0111 in this example). For the x16 configuration, the same pattern is repeated on both the upper and lower bytes.

Table 32: MPR Readout - Parallel Format

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
x4 Device								
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
x8 Device								
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
x16 Device								
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1



Table 32: MPR Readout - Parallel Format (Continued)

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
DQ8	0	0	0	0	0	0	0	0
DQ9	1	1	1	1	1	1	1	1
DQ10	1	1	1	1	1	1	1	1
DQ11	1	1	1	1	1	1	1	1
DQ12	1	1	1	1	1	1	1	1
DQ13	1	1	1	1	1	1	1	1
DQ14	1	1	1	1	1	1	1	1
DQ15	1	1	1	1	1	1	1	1

MPR Readout Staggered Format

Staggered format of data return is defined as the staggering of the MPR data across the lanes. In this mode, an RD/RDA command is issued to a specific data pattern location and then the data is returned on the DQ from each of the different data pattern locations. For the x4 configuration, an RD/RDA to data pattern location 0 will result in data from location 0 being driven on DQ0, data from location 1 being driven on DQ1, data from location 2 being driven on DQ2, and so on, as shown below. Similarly, an RD/RDA command to data pattern location 1 will result in data from location 1 being driven on DQ0, data from location 2 being driven on DQ1, data from location 3 being driven on DQ2, and so on. Examples of different starting locations are also shown.

Table 33: MPR Readout Staggered Format, x4

x4 READ MPR0 Command		x4 READ MI	PR1 Command	x4 READ MF	PR2 Command	x4 READ MPR3 Command		
Stagger	UI[7:0]	Stagger	UI[7:0]	Stagger	UI[7:0]	Stagger	UI[7:0]	
DQ0	MPR0	DQ0	MPR1	DQ0	MPR2	DQ0	MPR3	
DQ1	MPR1	DQ1	MPR2	DQ1	MPR3	DQ1	MPR0	
DQ2	MPR2	DQ2	MPR3	DQ2	MPR0	DQ2	MPR1	
DQ3	MPR3	DQ3	MPR0	DQ3	MPR1	DQ3	MPR2	

It is expected that the DRAM can respond to back-to-back RD/RDA commands to the MPR for all DDR4 frequencies so that a sequence (such as the one that follows) can be created on the data bus with no bubbles or clocks between read data. In this case, the system memory controller issues a sequence of RD(MPR0), RD(MPR1), RD(MPR2), RD(MPR3), RD(MPR0), RD(MPR1), RD(MPR2), and RD(MPR3).

Table 34: MPR Readout Staggered Format, x4 - Consecutive READs

Stagger	UI[7:0]	UI[15:8]	UI[23:16]	UI[31:24]	UI[39:32]	UI[47:40]	UI[55:48]	UI[63:56]
DQ0	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ1	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0



Table 34: MPR Readout Staggered Format, x4 - Consecutive READs (Continued)

Stagger	UI[7:0]	UI[15:8]	UI[23:16]	UI[31:24]	UI[39:32]	UI[47:40]	UI[55:48]	UI[63:56]
DQ2	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ3	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2

For the x8 configuration, the same pattern is repeated on the lower nibble as on the upper nibble. READs to other MPR data pattern locations follow the same format as the x4 case. A read example to MPR0 for x8 and x16 configurations is shown below.

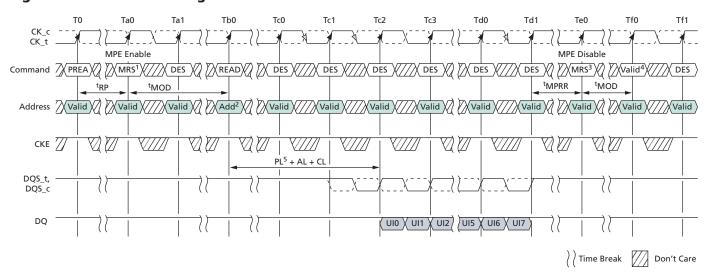
Table 35: MPR Readout Staggered Format, x8 and x16

x8 READ MPI	x8 READ MPR0 Command		R0 Command	x16 READ MPR0 Command		
Stagger	UI[7:0]	Stagger	UI[7:0]	Stagger	UI[7:0]	
DQ0	MPR0	DQ0	MPR0	DQ8	MPR0	
DQ1	MPR1	DQ1	MPR1	DQ9	MPR1	
DQ2	MPR2	DQ2	MPR2	DQ10	MPR2	
DQ3	MPR3	DQ3	MPR3	DQ11	MPR3	
DQ4	MPR0	DQ4	MPR0	DQ12	MPR0	
DQ5	MPR1	DQ5	MPR1	DQ13	MPR1	
DQ6	MPR2	DQ6	MPR2	DQ14	MPR2	
DQ7	MPR3	DQ7	MPR3	DQ15	MPR3	

MPR READ Waveforms

The following waveforms show MPR read accesses.

Figure 36: MPR READ Timing



Notes: 1. ${}^{t}CCD_{S} = 4{}^{t}CK$, Read Preamble = $1{}^{t}CK$.

2. Address setting:

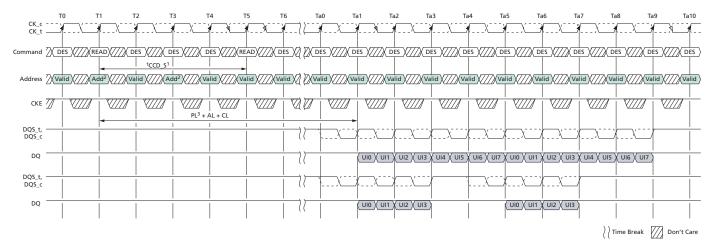
A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)



A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care," including BG1 and BG0. A12 is "Don't Care" when MR0 A[1:0] = 00 or 10 and must be 1b when MR0 A[1:0] = 01

- 3. Multipurpose registers read/write disable (MR3 A2 = 0).
- 4. Continue with regular DRAM command.
- 5. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

Figure 37: MPR Back-to-Back READ Timing



Notes: 1. ${}^{t}CCD$ S = $4{}^{t}CK$, Read Preamble = $1{}^{t}CK$.

2. Address setting:

A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7; for BC = 4, burst order is fixed at 0, 1, 2, 3, T, T, T)

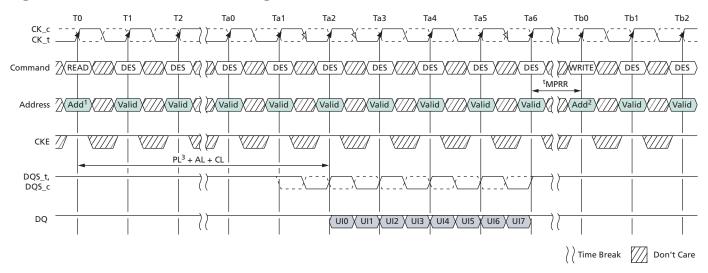
BA1 and BA0 indicate the MPR location

A10 and other address pins are "Don't Care," including BG1 and BG0. A12 is "Don't Care" when MR0 A[1:0] = 00 or 10 and must be 1b when MR0 A[1:0] = 01

3. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.



Figure 38: MPR READ-to-WRITE Timing



Notes: 1. Address setting:

A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)

A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)

BA1 and BA0 indicate the MPR location

A10 and other address pins are "Don't Care," including BG1 and BG0. A12 is "Don't Care" when MR0 A[1:0] = 00 and must be 1b when MR0 A[1:0] = 01

2. Address setting:

BA1 and BA0 indicate the MPR location

A[7:0] = data for MPR

BA1 and BA0 indicate the MPR location

A10 and other address pins are "Don't Care"

3. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

MPR Writes

MPR access mode allows 8-bit writes to the MPR Page 0 using the address bus A[7:0]. Data bus inversion (DBI) is not allowed during MPR WRITE operation. The DRAM will maintain the new written values unless re-initialized or there is power loss.

The following steps are required to use the MPR to write to mode register MPR Page 0.

- 1. The DLL must be locked if enabled.
- 2. Precharge all; wait until ^tRP is satisfied.
- 3. MRS command to MR3[2] = 1 (enable MPR data flow) and MR3[1:0] = 00 (MPR Page 0); writes to 01, 10, and 11 are not allowed.
- 4. ^tMRD and ^tMOD must be satisfied.
- 5. Redirect all subsequent WRITE commands to specific MPRx location.
- 6. Issue WR or WRA command:
 - a. BA1 and BA0 indicate MPRx location
 - 1. 00 = MPR0
 - 2. 01 = MPR1
 - 3. 10 = MPR2
 - 4. 11 = MPR3
 - b. A[7:0] = data for MPR Page 0, mapped A[7:0] to UI[7:0].

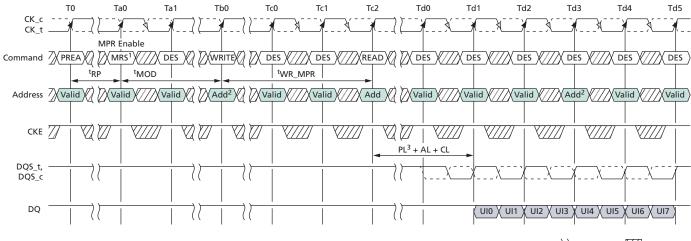


- c. Remaining address inputs, including A10, and BG1 and BG0 are "Don't Care."
- 7. tWR_MPR must be satisfied to complete MPR WRITE.
- 8. Steps 5 through 7 may be repeated to write additional MPRx locations.
- 9. After the last MPRx WRITE, ^tMPRR must be satisfied prior to exiting.
- 10. Issue MRS command to exit MPR mode; MR3[2] = 0.
- 11. When the ^tMOD sequence is completed, the DRAM is ready for normal operation from the core (such as ACT).

MPR WRITE Waveforms

The following waveforms show MPR write accesses.

Figure 39: MPR WRITE and WRITE-to-READ Timing



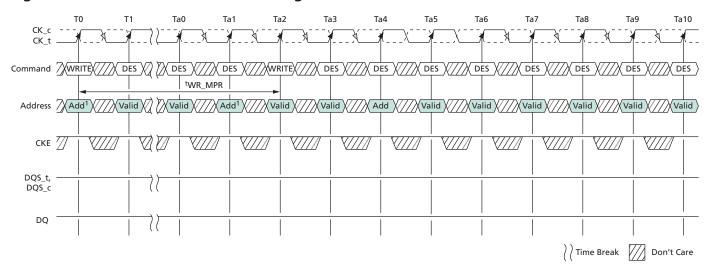
Time Break Don't Care

Notes:

- 1. Multipurpose registers read/write enable (MR3 A2 = 1).
- Address setting:
 BA1 and BA0 indicate the MPR location
 A10 and other address pins are "Don't Care"
- 3. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.



Figure 40: MPR Back-to-Back WRITE Timing



Note: 1. Address setting:

BA1 and BA0 indicate the MPR location

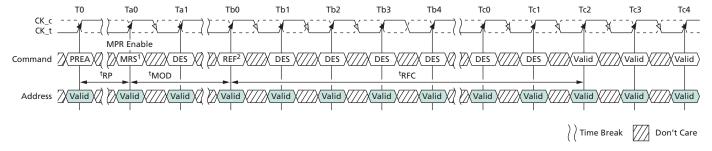
A[7:0] = data for MPR

A10 and other address pins are "Don't Care"

MPR REFRESH Waveforms

The following waveforms show MPR accesses interaction with refreshes.

Figure 41: REFRESH Timing

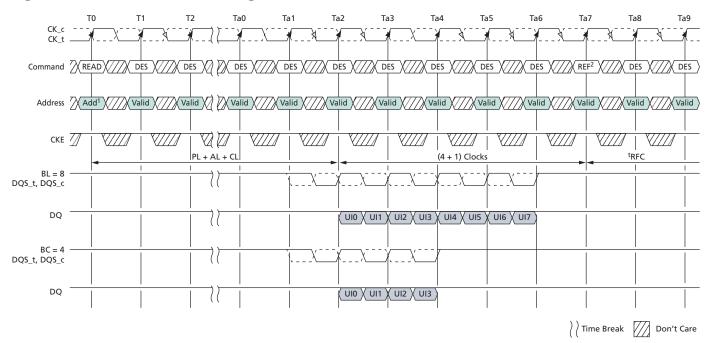


Notes: 1. Multipurpose registers read/write enable (MR3 A2 = 1). Redirect all subsequent read and writes to MPR locations.

2. 1x refresh is only allowed when MPR mode is enabled.



Figure 42: READ-to-REFRESH Timing



Notes: 1. Address setting:

A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)

A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)

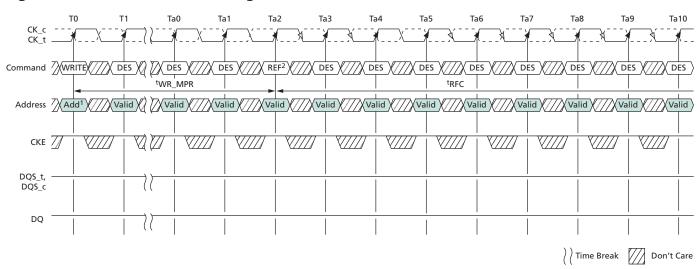
BA1 and BA0 indicate the MPR location

A10 and other address pins are "Don't Care," including BG1 and BG0. A12 is "Don't

Care" when MR0 A[1:0] = 00 or 10, and must be 1b when MR0 A[1:0] = 01

2. 1x refresh is only allowed when MPR mode is enabled.

Figure 43: WRITE-to-REFRESH Timing



Notes: 1. Address setting:

BA1 and BA0 indicate the MPR location





A[7:0] = data for MPR A10 and other address pins are "Don't Care"

2. 1x refresh is only allowed when MPR mode is enabled.



Gear-Down Mode

The DDR4 SDRAM defaults in 1/2 rate (1N) clock mode and uses a low-frequency MRS command (the MRS command has relaxed setup and hold) followed by a sync pulse (first CS pulse after MRS setting) to align the proper clock edge for operating the control lines CS_n, CKE, and ODT when in 1/4 rate (2N) mode. Gear-down mode is only supported at DDR4-2666 and faster. For operation in 1/2 rate mode, neither an MRS command or a sync pulse is required. Gear-down mode may only be entered during initialization or self refresh exit and may only be exited during self refresh exit. CAL mode and CA parity mode must be disabled prior to gear-down mode entry. The two modes may be enabled after 'SYNC_GEAR and 'CMD_GEAR periods have been satisfied. The general sequence for operation in 1/4 rate during initialization is as follows:

- 1. The device defaults to a 1N mode internal clock at power-up/reset.
- 2. Assertion of reset.
- 3. Assertion of CKE enables the DRAM.
- 4. MRS is accessed with a low-frequency N \times ^tCK gear-down MRS command. (N^tCK static MRS command is qualified by 1N CS_n.)
- 5. The memory controller will send a 1N sync pulse with a low-frequency N \times ^tCK NOP command. ^tSYNC_GEAR is an even number of clocks. The sync pulse is on an even edge clock boundary from the MRS command.
- 6. Initialization sequence, including the expiration of ^tDLLK and ^tZQinit, starts in 2N mode after ^tCMD_GEAR from 1N sync pulse.

The device resets to 1N gear-down mode after entering self refresh. The general sequence for operation in gear-down after self refresh exit is as follows:

- 1. MRS is set to 1, via MR3[3], with a low-frequency N \times ^tCK gear-down MRS command.
 - a. The N^tCK static MRS command is qualified by 1N CS_n, which meets ^tXS or ^tXS ABORT.
 - b. Only a REFRESH command may be issued to the DRAM before the N^tCK static MRS command.
- 2. The DRAM controller sends a 1N sync pulse with a low-frequency N \times ^tCK NOP command.
 - a. tSYNC_GEAR is an even number of clocks.
 - b. The sync pulse is on even edge clock boundary from the MRS command.
- 3. A valid command not requiring locked DLL is available in 2N mode after ^tCMD_GEAR from the 1N sync pulse.
 - a. A valid command requiring locked DLL is available in 2N mode after ^tXSDLL or ^tDLLK from the 1N sync pulse.
- 4. If operation is in 1N mode after self refresh exit, N × ^tCK MRS command or sync pulse is not required during self refresh exit. The minimum exit delay to the first valid command is ^tXS, or ^tXS_ABORT.

The DRAM may be changed from 2N to 1N by entering self refresh mode, which will reset to 1N mode. Changing from 2N to by any other means can result in loss of data and make operation of the DRAM uncertain.

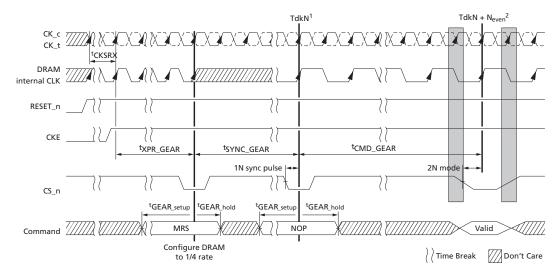
When operating in 2N gear-down mode, the following MR settings apply:

- CAS latency (MR0[6:4,2]): Even number of clocks
- Write recovery and read to precharge (MR0[11:9]): Even number of clocks
- Additive latency (MR1[4:3]): CL 2
- CAS WRITE latency (MR2 A[5:3]): Even number of clocks



- CS to command/address latency mode (MR4[8:6]): Even number of clocks
- CA parity latency mode (MR5[2:0]): Even number of clocks

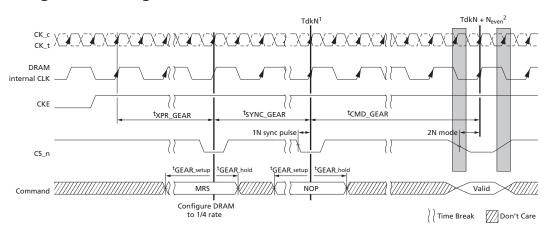
Figure 44: Clock Mode Change from 1/2 Rate to 1/4 Rate (Initialization)



Notes: 1. After tSYNC_GEAR from GEAR-DOWN command, internal clock rate is changed at TdkN.

2. After ^tSYNC_GEAR + ^tCMD_GEAR from GEAR-DOWN command, both internal clock rate and command cycle are changed at TdkN + Neven.

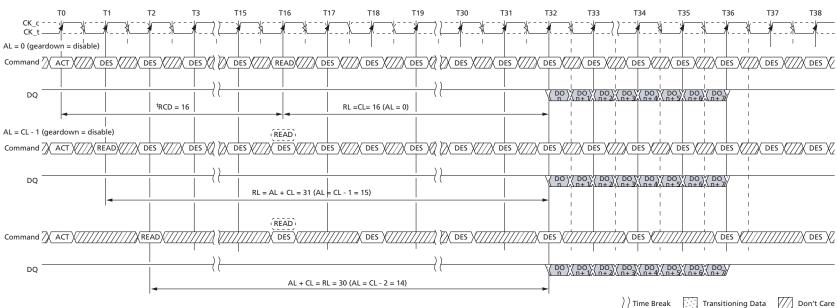
Figure 45: Clock Mode Change After Exiting Self Refresh



Notes: 1. After tSYNC_GEAR from GEAR-DOWN command, internal clock rate is changed at TdkN.

2. After ^tSYNC_GEAR + ^tCMD_GEAR from GEAR-DOWN command, both internal clock rate and command cycle are changed at TdkN + Neven.

8Gb: x4, x8, x16 DDR4 SDRAM Gear-Down Mode





Maximum Power-Saving Mode

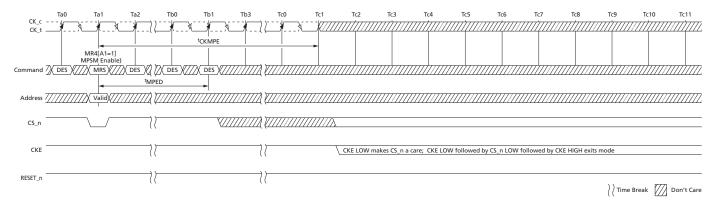
Maximum power-saving mode provides the lowest power mode where data retention is not required. When the device is in the maximum power-saving mode, it does not maintain data retention or respond to any external command, except the MAXIMUM POWER SAVING MODE EXIT command and during the assertion of RESET_n signal LOW. This mode is more like a "hibernate mode" than a typical power-saving mode. The intent is to be able to park the DRAM at a very low-power state; the device can be switched to an active state via the per-DRAM addressability (PDA) mode.

Maximum Power-Saving Mode Entry

Maximum power-saving mode is entered through an MRS command. For devices with shared control/address signals, a single DRAM device can be entered into the maximum power-saving mode using the per-DRAM addressability MRS command. Large CS_n hold time to CKE upon the mode exit could cause DRAM malfunction; as a result, CA parity, CAL, and gear-down modes must be disabled prior to the maximum power-saving mode entry MRS command.

The MRS command may use both address and DQ information, as defined in the Per-DRAM Addressability section. As illustrated in the figure below, after ^tMPED from the mode entry MRS command, the DRAM is not responsive to any input signals except CKE, CS_n, and RESET_n. All other inputs are disabled (external input signals may become High-Z). The system will provide a valid clock until ^tCKMPE expires, at which time clock inputs (CK) should be disabled (external clock signals may become High-Z).

Figure 47: Maximum Power-Saving Mode Entry

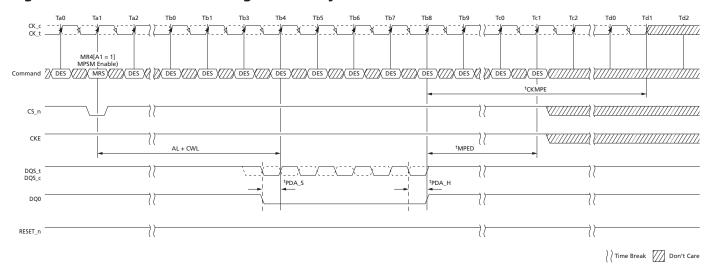




Maximum Power-Saving Mode Entry in PDA

The sequence and timing required for the maximum power-saving mode with the per-DRAM addressability enabled is illustrated in the figure below.

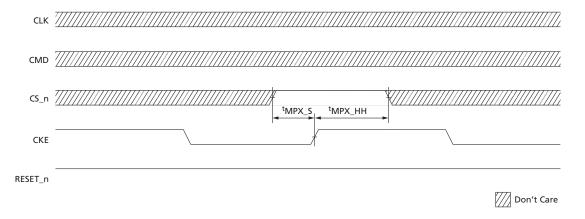
Figure 48: Maximum Power-Saving Mode Entry with PDA



CKE Transition During Maximum Power-Saving Mode

The following figure shows how to maintain maximum power-saving mode even though the CKE input may toggle. To prevent the device from exiting the mode, CS_n should be HIGH at the CKE LOW-to-HIGH edge, with appropriate setup (tMPX_S) and hold (tMPX_H) timings.

Figure 49: Maintaining Maximum Power-Saving Mode with CKE Transition



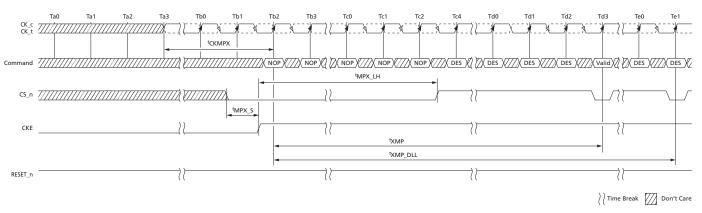
Maximum Power-Saving Mode Exit

To exit the maximum power-saving mode, CS_n should be LOW at the CKE LOW-to-HIGH transition, with appropriate setup (the MPX_S) and hold (the MPX_LH) timings, as



shown in the figure below. Because the clock receivers (CK_t, CK_c) are disabled during this mode, CS_n = LOW is captured by the rising edge of the CKE signal. If the CS_n signal level is detected LOW, the DRAM clears the maximum power-saving mode MRS bit and begins the exit procedure from this mode. The external clock must be restarted and be stable by ^tCKMPX before the device can exit the maximum power-saving mode. During the exit time (^tXMP), only NOP and DES commands are allowed: NOP during ^tMPX_LH and DES the remainder of ^tXMP. After ^tXMP expires, valid commands not requiring a locked DLL are allowed; after ^tXMP_DLL expires, valid commands requiring a locked DLL are allowed.

Figure 50: Maximum Power-Saving Mode Exit

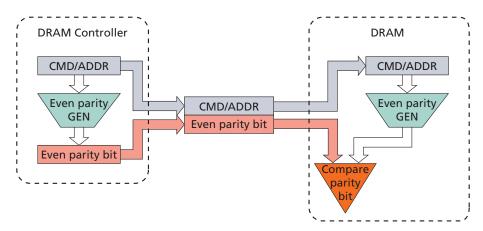




Command/Address Parity

Command/address (CA) parity takes the CA parity signal (PAR) input carrying the parity bit for the generated address and commands signals and matches it to the internally generated parity from the captured address and commands signals. CA parity is supported in the DLL enabled state only; if the DLL is disabled, CA parity is not supported.

Figure 51: Command/Address Parity Operation



CA parity is disabled or enabled via an MRS command. If CA parity is enabled by programming a non-zero value to CA parity latency in the MR, the DRAM will ensure that there is no parity error before executing commands. There is an additional delay required for executing the commands versus when parity is disabled. The delay is programmed in the MR when CA parity is enabled (parity latency) and applied to all commands which are registered by CS_n (rising edge of CK_t and falling CS_n). The command is held for the time of the parity latency (PL) before it is executed inside the device. The command captured by the input clock has an internal delay before executing and is determined with PL. ALERT_n will go active when the DRAM detects a CA parity error.

CA parity covers ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, the address bus including bank address and bank group bits, and C[2:0] on 3DS devices; the control signals CKE, ODT, and CS_n are not covered. For example, for a 4Gb x4 monolithic device, parity is computed across BG[1:0], BA[1:0], A16/RAS_n, A15/CAS_n, A14/WE_n, A[13:0], and ACT_n. The DRAM treats any unused address pins internally as zeros; for example, if a common die has stacked pins but the device is used in a monolithic application, then the address pins used for stacking and not connected are treated internally as zeros.

The convention for parity is even parity; for example, valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words, the parity bit is chosen so that the total number of ones in the transmitted signal, including the parity bit, is even.

If a DRAM device detects a CA parity error in any command qualified by CS_n, it will perform the following steps:

1. Ignore the erroneous command. Commands in the MAX N*n*CK window (¹PAR_UNKNOWN) prior to the erroneous command are not guaranteed to be executed. When a READ command in this N*n*CK window is not executed, the device



- does not activate DQS outputs. If WRITE CRC is enabled and a WRITE CRC occurs during the ^tPAR_UNKNOWN window, the WRITE CRC Error Status Bit located at MR5[3] may or may not get set. When CA Parity and WRITE CRC are both enabled and a CA Parity occurs, the WRITE CRC Error Status Bit should be reset.
- 2. Log the error by storing the erroneous command and address bits in the MPR error log.
- 3. Set the parity error status bit in the mode register to 1. The parity error status bit must be set before the ALERT_n signal is released by the DRAM (that is, 'PAR_ALERT_ON + 'PAR_ALERT_PW (MIN)).
- 4. Assert the ALERT_n signal to the host (ALERT_n is active LOW) within ^tPAR_ALERT_ON time.
- 5. Wait for all in-progress commands to complete. These commands were received ^tPAR_UNKOWN before the erroneous command.
- 6. Wait for ^tRAS (MIN) before closing all the open pages. The DRAM is not executing any commands during the window defined by (^tPAR_ALERT_ON + ^tPAR_ALERT_PW).
- 7. After ^tPAR_ALERT_PW (MIN) has been satisfied, the device may de-assert ALERT_n.
 - a. When the device is returned to a known precharged state, ALERT_n is allowed to be de-asserted.
- 8. After ('PAR_ALERT_PW (MAX)) the DRAM is ready to accept commands for normal operation. Parity latency will be in effect; however, parity checking will not resume until the memory controller has cleared the parity error status bit by writing a zero. The DRAM will execute any erroneous commands until the bit is cleared; unless persistent mode is enabled.
- It is possible that the device might have ignored a REFRESH command during ^tPAR_ALERT_PW or the REFRESH command is the first erroneous frame, so it is recommended that extra REFRESH cycles be issued, as needed.
- The parity error status bit may be read anytime after ^tPAR_ALERT_ON + ^tPAR_ALERT_PW to determine which DRAM had the error. The device maintains the error log for the first erroneous command until the parity error status bit is reset to a zero or a second CA parity occurs prior to resetting.

The mode register for the CA parity error is defined as follows: CA parity latency bits are write only, the parity error status bit is read/write, and error logs are read-only bits. The DRAM controller can only program the parity error status bit to zero. If the DRAM controller illegally attempts to write a 1 to the parity error status bit, the DRAM can not be certain that parity will be checked; the DRAM may opt to block the DRAM controller from writing a 1 to the parity error status bit.

The device supports persistent parity error mode. This mode is enabled by setting MR5[9] = 1; when enabled, CA parity resumes checking after the ALERT_n is de-asserted, even if the parity error status bit remains a 1. If multiple errors occur before the error status bit is cleared the error log in MPR Page 1 should be treated as "Don't Care." In persistent parity error mode the ALERT_n pulse will be asserted and de-asserted by the DRAM as defined with the MIN and MAX value ${}^{\rm t}$ PAR_ALERT_PW. The DRAM controller must issue DESELECT commands once it detects the ALERT_n signal, this response time is defined as ${}^{\rm t}$ PAR_ALERT_RSP. The following figures capture the flow of events on the CA bus and the ALERT_n signal.



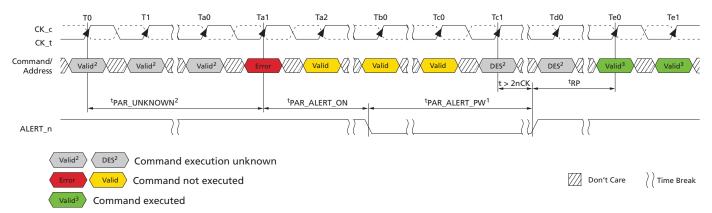
Table 36: Mode Register Setting for CA Parity

CA Parity Latency MR5[2:0] ¹	Applicable Speed Bin	Parity Error Status	Parity Persistent Mode	Erroneous CA Frame		
000 = Disabled	N/A					
001 = 4 clocks	1600, 1866, 2133					
010 = 5 clocks	2400, 2666			C[2:0], ACT_n, BG1,		
011 = 6 clocks	2933, 3200	MR5 [4] 0 = Clear	MR5 [9] 0 = DisabledMR5	BG0, BA[1:0], PAR, A17, A16/RAS_n, A15/		
100 = 8 clocks	RFU	MR5 [4] 1 = Error	[9] 1 = Enabled	CAS n, A14/WE n,		
101 = Reserved	RFU			A[13:0]		
110 = Reserved	RFU					
111 = Reserved	RFU					

Notes:

- 1. Parity latency is applied to all commands.
- 2. Parity latency can be changed only from a CA parity disabled state; for example, a direct change from PL = 3 to PL = 4 is not allowed. The correct sequence is PL = 3 to disabled to PL = 4.
- 3. Parity latency is applied to WRITE and READ latency. WRITE latency = AL + CWL + PL. READ latency = AL + CL + PL.

Figure 52: Command/Address Parity During Normal Operation

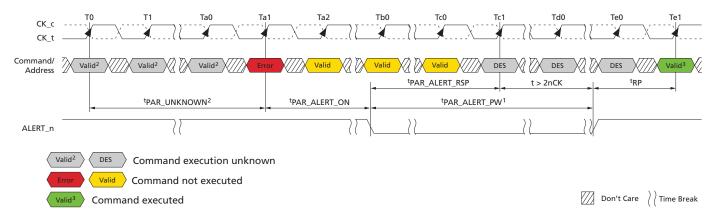


Notes:

- 1. DRAM is emptying queues. Precharge all and parity checking are off until parity error status bit is cleared.
- Command execution is unknown; the corresponding DRAM internal state change may
 or may not occur. The DRAM controller should consider both cases and make sure that
 the command sequence meets the specifications. If WRITE CRC is enabled and a WRITE
 CRC occurs during the ^tPAR_UNKNOWN window, the WRITE CRC Error Status Bit located
 at MR5[3] may or may not get set.
- 3. Normal operation with parity latency (CA parity persistent error mode disabled). Parity checking is off until parity error status bit is cleared.



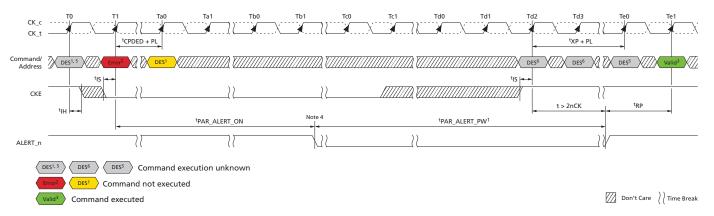
Figure 53: Persistent CA Parity Error Checking Operation



Notes:

- DRAM is emptying queues. Precharge all and parity check re-enable finished by [†]PAR_ALERT_PW.
- Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications. If WRITE CRC is enabled and a WRITE CRC occurs during the ^tPAR_UNKNOWN window, the WRITE CRC Error Status Bit located at MR5[3] may or may not get set
- 3. Normal operation with parity latency and parity checking (CA parity persistent error mode enabled).

Figure 54: CA Parity Error Checking - SRE Attempt

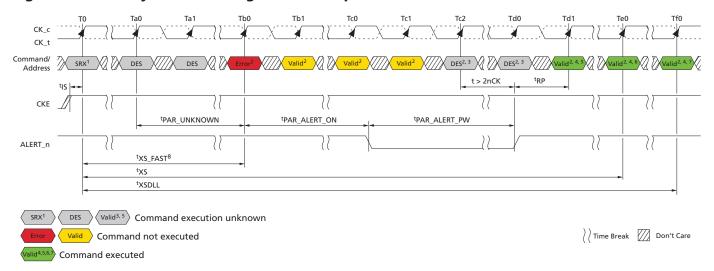


Notes:

- 1. Only DESELECT command is allowed.
- 2. SELF REFRESH command error. The DRAM masks the intended SRE command and enters precharge power-down.
- 3. Normal operation with parity latency (CA parity persistent error mode disabled). Parity checking is off until the parity error status bit cleared.
- 4. The controller cannot disable the clock until it has been capable of detecting a possible CA parity error.
- 5. Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
- 6. Only a DESELECT command is allowed; CKE may go HIGH prior to Tc2 as long as DES commands are issued.

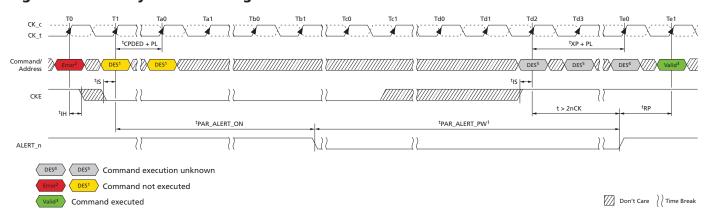


Figure 55: CA Parity Error Checking - SRX Attempt



- Notes: 1. Self refresh abort = disable: MR4 [9] = 0.
 - 2. Input commands are bounded by ^tXSDLL, ^tXS, ^tXS_ABORT, and ^tXS_FAST timing.
 - 3. Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
 - 4. Normal operation with parity latency (CA parity persistent error mode disabled). Parity checking off until parity error status bit cleared.
 - 5. Only an MRS (limited to those described in the SELF REFRESH Operation section), ZQCS, or ZQCL command is allowed.
 - 6. Valid commands not requiring a locked DLL.
 - 7. Valid commands requiring a locked DLL.
 - 8. This figure shows the case from which the error occurred after ^tXS_FAST. An error may also occur after tXS_ABORT and tXS.

Figure 56: CA Parity Error Checking - PDE/PDX

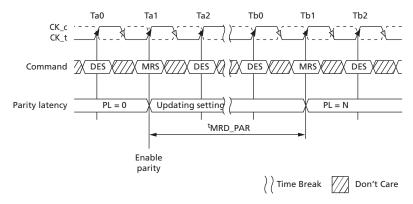


- Notes: 1. Only DESELECT command is allowed.
 - 2. Error could be precharge or activate.
 - 3. Normal operation with parity latency (CA parity persistent error mode disabled). Parity checking is off until parity error status bit cleared.



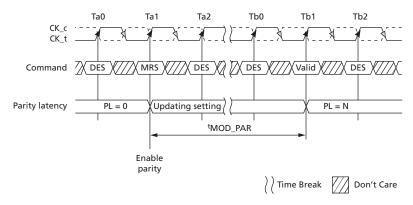
- 4. Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
- Only a DESELECT command is allowed; CKE may go HIGH prior to Td2 as long as DES commands are issued.

Figure 57: Parity Entry Timing Example – ^tMRD_PAR



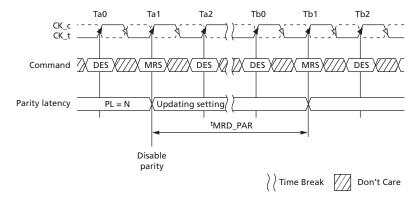
Note: 1. ${}^{t}MRD_{PAR} = {}^{t}MOD + N$; where N is the programmed parity latency.

Figure 58: Parity Entry Timing Example – ^tMOD_PAR



Note: 1. tMOD_PAR = tMOD + N; where N is the programmed parity latency.

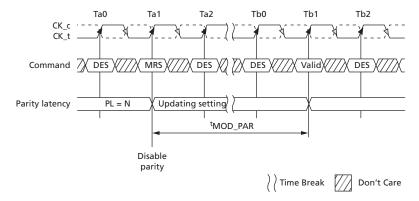
Figure 59: Parity Exit Timing Example – ^tMRD_PAR



Note: 1. ${}^{t}MRD_{PAR} = {}^{t}MOD + N$; where N is the programmed parity latency.

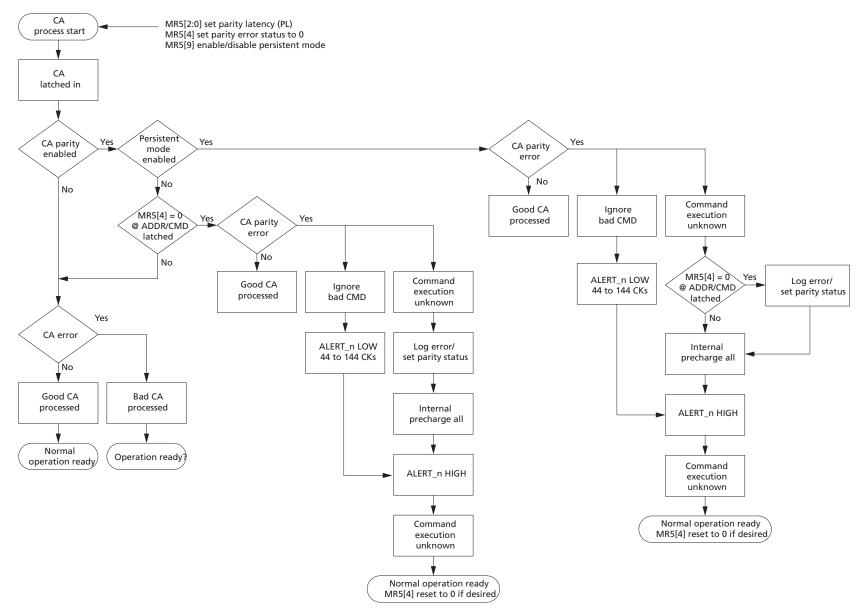


Figure 60: Parity Exit Timing Example – tMOD_PAR



Note: 1. ${}^{t}MOD_{PAR} = {}^{t}MOD + N$; where N is the programmed parity latency.

Figure 61: CA Parity Flow Diagram





Per-DRAM Addressability

DDR4 allows programmability of a single, specific DRAM on a rank. As an example, this feature can be used to program different ODT or V_{REF} values on each DRAM on a given rank. Because per-DRAM addressability (PDA) mode may be used to program optimal V_{REF} for the DRAM, the data set up for first DQ0 transfer or the hold time for the last DQ0 transfer cannot be guaranteed. The DRAM may sample DQ0 on either the first falling or second rising DQS transfer edge. This supports a common implementation between BC4 and BL8 modes on the DRAM. The DRAM controller is required to drive DQ0 to a stable LOW or HIGH state during the length of the data transfer for BC4 and BL8 cases. Note, both fixed and on-the-fly (OTF) modes are supported for BC4 and BL8 during PDA mode.

- 1. Before entering PDA mode, write leveling is required.
 - BL8 or BC4 may be used.
- 2. Before entering PDA mode, the following MR settings are possible:
 - $R_{TT(Park)}$ MR5 A[8:6] = Enable
 - R_{TT(NOM)} MR1 A[10:8] = Enable
- 3. Enable PDA mode using MR3 [4] = 1. (The default programed value of MR3[4] = 0.)
- 4. In PDA mode, all MRS commands are qualified with DQ0. The device captures DQ0 by using DQS signals. If the value on DQ0 is LOW, the DRAM executes the MRS command. If the value on DQ0 is HIGH, the DRAM ignores the MRS command. The controller can choose to drive all the DQ bits.
- 5. Program the desired DRAM and mode registers using the MRS command and DQ0.
- 6. In PDA mode, only MRS commands are allowed.
- 7. The MODE REGISTER SET command cycle time in PDA mode, AL + CWL + BL/2 0.5^tCK + ^tMRD_PDA + PL, is required to complete the WRITE operation to the mode register and is the minimum time required between two MRS commands.
- 8. Remove the device from PDA mode by setting MR3[4] = 0. (This command requires DQ0 = 0.)

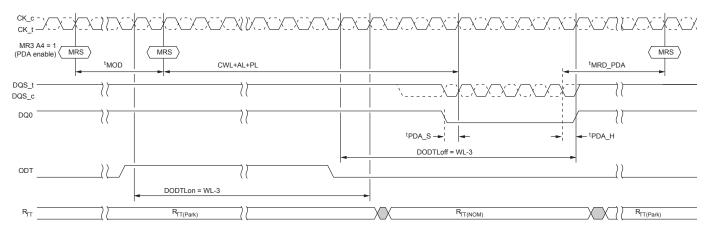
Note: Removing the device from PDA mode will require programming the entire MR3 when the MRS command is issued. This may impact some PDA values programmed within a rank as the EXIT command is sent to the rank. To avoid such a case, the PDA enable/disable control bit is located in a mode register that does not have any PDA mode controls.

In PDA mode, the device captures DQ0 using DQS signals the same as in a normal WRITE operation; however, dynamic ODT is not supported. Extra care is required for the ODT setting. If $R_{TT(NOM)}$ MR1 [10:8] = enable, device data termination needs to be controlled by the ODT pin, and applies the same timing parameters (defined below).

Symbol	Parameter
DODTLon	Direct ODT turnon latency
DODTLoff	Direct ODT turn off latency
^t ADC	R _{TT} change timing skew
^t AONAS	Asynchronous R _{TT(NOM)} turn-on delay
^t AOFAS	Asynchronous R _{TT(NOM)} turn-off delay

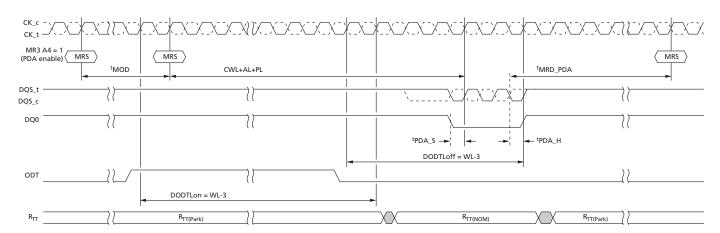


Figure 62: PDA Operation Enabled, BL8



Note: 1. $R_{TT(Park)} = Enable$; $R_{TT(NOM)} = Enable$; WRITE preamble set = $2^{t}CK$; and DLL = On.

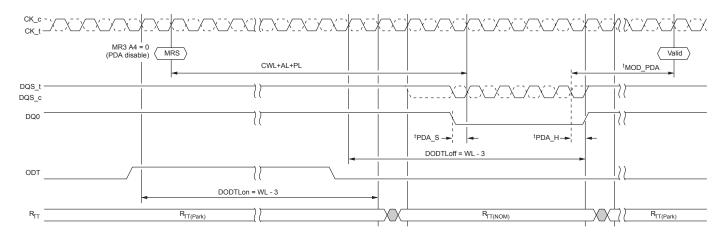
Figure 63: PDA Operation Enabled, BC4



Note: 1. $R_{TT(Park)}$ = Enable; $R_{TT(NOM)}$ = Enable; WRITE preamble set = $2^{t}CK$; and DLL = On.



Figure 64: MRS PDA Exit



Note: 1. $R_{TT(Park)}$ = Enable; $R_{TT(NOM)}$ = Enable; WRITE preamble set = 2^tCK ; and DLL = On.

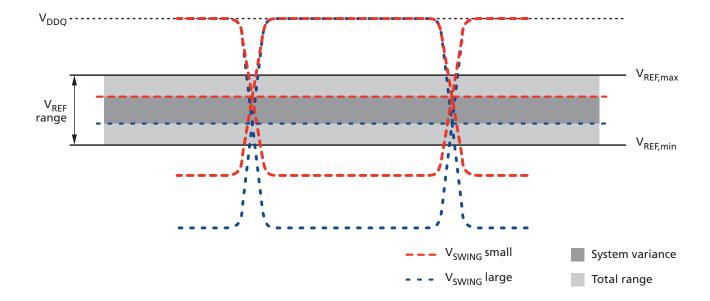


V_{REFDO} Calibration

The V_{REFDQ} level, which is used by the DRAM DQ input receivers, is internally generated. The DRAM V_{REFDQ} does not have a default value upon power-up and must be set to the desired value, usually via V_{REFDQ} calibration mode. If PDA or PPR modes (hPPR or sPPR) are used prior to V_{REFDQ} calibration, V_{REFDQ} should initially be set at the midpoint between the $V_{DD,max}$, and the LOW as determined by the driver and ODT termination selected with wide voltage swing on the input levels and setup and hold times of approximately 0.75UI. The memory controller is responsible for V_{REFDQ} calibration to determine the best internal V_{REFDQ} level. The V_{REFDQ} calibration is enabled/disabled via MR6[7], MR6[6] selects Range 1 (60% to 92.5% of V_{DDQ}) or Range 2 (45% to 77.5% of V_{DDQ}), and an MRS protocol using MR6[5:0] to adjust the V_{REFDQ} level up and down. MR6[6:0] bits can be altered using the MRS command if MR6[7] is enabled. The DRAM controller will likely use a series of writes and reads in conjunction with V_{REFDQ} adjustments to obtain the best V_{REFDQ} , which in turn optimizes the data eye.

The internal V_{REFDQ} specification parameters are voltage range, step size, V_{REF} step time, V_{REF} full step time, and V_{REF} valid level. The voltage operating range specifies the minimum required V_{REF} setting range for DDR4 SDRAM devices. The minimum range is defined by $V_{REFDQ,min}$ and $V_{REFDQ,max}$. As noted, a calibration sequence, determined by the DRAM controller, should be performed to adjust V_{REFDQ} and optimize the timing and voltage margin of the DRAM data input receivers. The internal V_{REFDQ} voltage value may not be exactly within the voltage range setting coupled with the V_{REF} set tolerance; the device must be calibrated to the correct internal V_{REFDQ} voltage.

Figure 65: V_{REFDQ} Voltage Range





V_{REFDO} Range and Levels

Table 37: V_{REFDO} Range and Levels

MR6[5:0]	Range 1 MR6[6] 0	Range 2 MR6[6] 1	MR6[5:0]	Range 1 MR6[6] 0	Range 2 MR6[6] 1
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 1	11 1111 = Reserved	

V_{REFDQ} Step Size

The V_{REF} step size is defined as the step size between adjacent steps. V_{REF} step size ranges from $0.5\%\,V_{DDQ}$ to $0.8\%\,V_{DDQ}$. However, for a given design, the device has one value for V_{REF} step size that falls within the range.

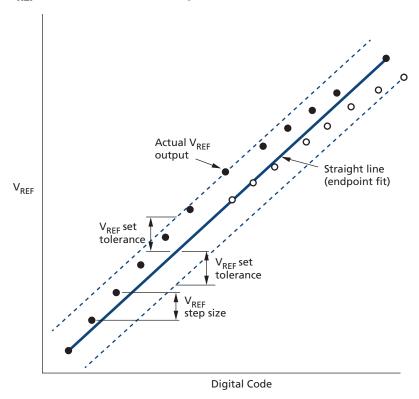
The V_{REF} set tolerance is the variation in the V_{REF} voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V_{REF} set tolerance uncertainty. The range of V_{REF} set tolerance uncertainty is a function of number of steps n.

The V_{REF} set tolerance is measured with respect to the ideal line, which is based on the MIN and MAX V_{REF} value endpoints for a specified range. The internal V_{REFDO} voltage



value may not be exactly within the voltage range setting coupled with the V_{REF} set tolerance; the device must be calibrated to the correct internal V_{REFDO} voltage.

Figure 66: Example of V_{REF} Set Tolerance and Step Size



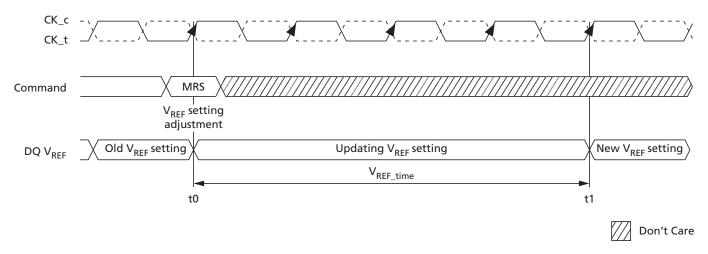
Note: 1. Maximum case shown.

V_{REFDQ} Increment and Decrement Timing

The V_{REF} increment/decrement step times are defined by $V_{REE,time}$. $V_{REE,time}$ is defined from t0 to t1, where t1 is referenced to the V_{REF} voltage at the final DC level within the V_{REF} valid tolerance (V_{REE,val_tol}). The V_{REF} valid level is defined by $V_{REE,val}$ tolerance to qualify the step time t1. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any V_{REF} increment/decrement adjustment.



Figure 67: V_{REFDO} Timing Diagram for V_{REF,time} Parameter



Note: 1. t0 is referenced to the MRS command clock t1 is referenced to V_{REE,tol}

 V_{REFDQ} calibration mode is entered via an MRS command, setting MR6[7] to 1 (0 disables V_{REFDQ} calibration mode) and setting MR6[6] to either 0 or 1 to select the desired range (MR6[5:0] are "Don't Care"). After V_{REFDQ} calibration mode has been entered, V_{REFDQ} calibration mode legal commands may be issued once ${}^{t}V_{REFDQ}$ has been satisfied. Legal commands for V_{REFDQ} calibration mode are ACT, WR, WRA, RD, RDA, PRE, DES, and MRS to set V_{REFDQ} values, and MRS to exit V_{REFDQ} calibration mode. Also, after V_{REFDQ} calibration mode has been entered, "dummy" WRITE commands are allowed prior to adjusting the V_{REFDQ} value the first time V_{REFDQ} calibration is performed after initialization.

Setting V_{REFDQ} values requires MR6[7] be set to 1 and MR6[6] be unchanged from the initial range selection; MR6[5:0] may be set to the desired V_{REFDQ} values. If MR6[7] is set to 0, MR6[6:0] are not written. $V_{REE,time-short}$ or $V_{REE,time-long}$ must be satisfied after each MR6 command to set V_{REFDQ} value before the internal $V_{REE,time}$ value is valid.

If PDA mode is used in conjunction with V_{REFDQ} calibration, the PDA mode requirement that only MRS commands are allowed while PDA mode is enabled is not waived. That is, the only V_{REFDQ} calibration mode legal commands noted above that may be used are the MRS commands: MRS to set V_{REFDQ} values and MRS to exit V_{REFDQ} calibration mode.

The last MR6[6:0] setting written to MR6 prior to exiting V_{REFDQ} calibration mode is the range and value used for the internal V_{REFDQ} setting. V_{REFDQ} calibration mode may be exited when the DRAM is in idle state. After the MRS command to exit V_{REFDQ} calibration mode has been issued, DES must be issued until ${}^{t}VREFDQX$ has been satisfied where any legal command may then be issued. V_{REFDQ} setting should be updated if the die temperature changes too much from the calibration temperature.

The following are typical script when applying the above rules for V_{REFDQ} calibration routine when performing V_{REFDQ} calibration in Range 1:

• MR6[7:6]10 [5:0]XXXXXXX.



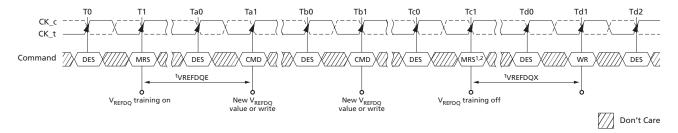
- Subsequent legal commands while in V_{REFDQ} calibration mode: ACT, WR, WRA, RD, RDA, PRE, DES, and MRS (to set V_{REFDQ} values and exit V_{REFDQ} calibration mode).
- All subsequent V_{REFDQ} calibration MR setting commands are MR6[7:6]10 [5:0]VVVVV.
 - "VVVVV" are desired settings for V_{REFDO}.
- Issue ACT/WR/RD looking for pass/fail to determine V_{CENT} (midpoint) as needed.
- ullet To exit V_{REFDO} calibration, the last two V_{REFDO} calibration MR commands are:
 - MR6[7:6]10 [5:0]VVVVVV* where VVVVVV* = desired value for V_{REFDO} .
 - MR6[7]0 [6:0]XXXXXXX to exit V_{REFDO} calibration mode.

The following are typical script when applying the above rules for V_{REFDQ} calibration routine when performing V_{REFDQ} calibration in Range 2:

- MR6[7:6]11 [5:0]XXXXXXX.
 - Subsequent legal commands while in V_{REFDQ} calibration mode: ACT, WR, WRA, RD, RDA, PRE, DES, and MRS (to set V_{REFDQ} values and exit V_{REFDQ} calibration mode).
- All subsequent $V_{\rm REFDQ}$ calibration MR setting commands are MR6[7:6]11 [5:0]VVVVV.
 - "VVVVV" are desired settings for V_{REFDO}.
- Issue ACT/WR/RD looking for pass/fail to determine V_{CENT} (midpoint) as needed.
- To exit V_{REFDO} calibration, the last two V_{REFDO} calibration MR commands are:
 - MR6[7:6]11 [5:0]VVVVV* where VVVVVV* = desired value for V_{REFDO} .
 - MR6[7]0 [6:0]XXXXXXX to exit V_{REFDO} calibration mode.

Note: Range may only be set or changed when entering V_{REFDQ} calibration mode; changing range while in or exiting V_{REFDQ} calibration mode is illegal.

Figure 68: V_{REFDO} Training Mode Entry and Exit Timing Diagram



Notes: 1. New V_{REFDQ} values are not allowed with an MRS command during calibration mode entry.

2. Depending on the step size of the latest programmed V_{REF} value, V_{REF} must be satisfied before disabling V_{REFDO} training mode.



Figure 69: V_{REF} Step: Single Step Size Increment Case

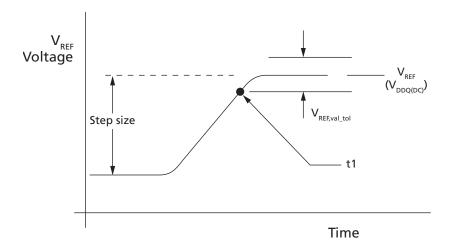


Figure 70: V_{REF} Step: Single Step Size Decrement Case

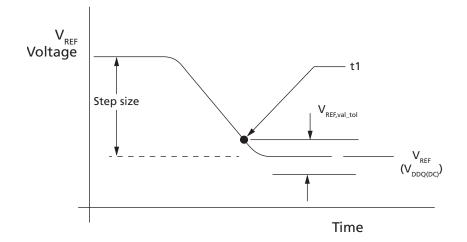




Figure 71: V_{REF} Full Step: From $V_{REF,min}$ to $V_{REF,max}$ Case

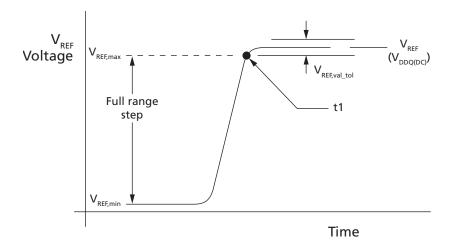
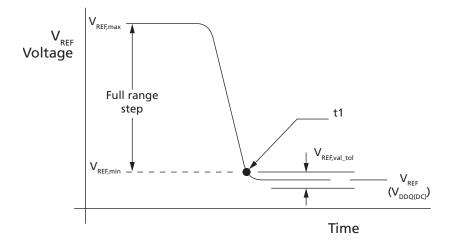


Figure 72: V_{REF} Full Step: From V_{REF,max} to V_{REF,min}Case



V_{REFDQ} Target Settings

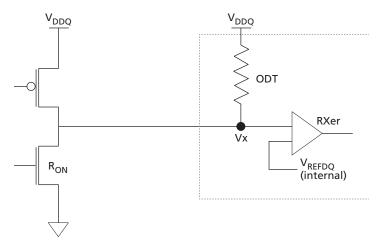
The V_{REFDQ} initial settings are largely dependant on the ODT termination settings. The table below shows all of the possible initial settings available for V_{REFDQ} training; it is unlikely the lower ODT settings would be used in most cases.



Table 38: V_{REFDQ} Settings ($V_{DDQ} = 1.2V$)

R _{ON}	ODT	Vx - V _{IN} LOW (mV)	V _{REFDQ} (mv)	V _{REFDQ} (%V _{DDQ})
	34 ohm	600	900	75%
	40 ohm	550	875	73%
	48 ohm	500	850	71%
34 ohm	60 ohm	435	815	68%
	80 ohm	360	780	65%
	120 ohm	265	732	61%
	240 ohm	150	675	56%
	34 ohm	700	950	79%
	40 ohm	655	925	77%
	48 ohm	600	900	75%
48 ohm	60 ohm	535	865	72%
	80 ohm	450	825	69%
	120 ohm	345	770	64%
	240 ohm	200	700	58%

Figure 73: V_{REFDQ} Equivalent Circuit





Connectivity Test Mode

Connectivity test (CT) mode is similar to boundary scan testing but is designed to significantly speed up the testing of electrical continuity of pin interconnections between the device and the memory controller on the PC boards. Designed to work seamlessly with any boundary scan device, CT mode is supported in all ×4, ×8, and ×16 non-3DS devices (JEDEC states CT mode for ×4 and ×8 is not required on 4Gb and is an optional feature on 8Gb and above). 3DS devices do not support CT mode and the TEN pin should be considered RFU maintained LOW at all times.

Contrary to other conventional shift-register-based test modes, where test patterns are shifted in and out of the memory devices serially during each clock, the CT mode allows test patterns to be entered on the test input pins in parallel and the test results to be extracted from the test output pins of the device in parallel. These two functions are also performed at the same time, significantly increasing the speed of the connectivity check. When placed in CT mode, the device appears as an asynchronous device to the external controlling agent. After the input test pattern is applied, the connectivity test results are available for extraction in parallel at the test output pins after a fixed propagation delay time.

Note: A reset of the device is required after exiting CT mode (see RESET and Initialization Procedure).

Pin Mapping

Only digital pins can be tested using the CT mode. For the purposes of a connectivity check, all the pins used for digital logic in the device are classified as one of the following types:

- Test enable (TEN): When asserted HIGH, this pin causes the device to enter CT mode. In CT mode, the normal memory function inside the device is bypassed and the I/O pins appear as a set of test input and output pins to the external controlling agent. Additionally, the device will set the internal V_{REFDQ} to V_{DDQ} × 0.5 during CT mode (this is the only time the DRAM takes direct control over setting the internal V_{REFDQ}). The TEN pin is dedicated to the connectivity check function and will not be used during normal device operation.
- Chip select (CS_n): When asserted LOW, this pin enables the test output pins in the device. When de-asserted, these output pins will be High-Z. The CS_n pin in the device serves as the CS_n pin in CT mode.
- **Test input:** A group of pins used during normal device operation designated as test input pins. These pins are used to enter the test pattern in CT mode.
- Test output: A group of pins used during normal device operation designated as test
 output pins. These pins are used for extraction of the connectivity test results in CT
 mode.
- RESET n: This pin must be fixed high level during CT mode, as in normal function.



Table 39: Connectivity Mode Pin Description and Switching Levels

CT Mode Pins		Pin Name During Normal Memory Operation	Switching Level	Notes
Test enable	9	TEN	CMOS (20%/80% V _{DD})	1, 2
Chip select		CS_n	V _{REFCA} ±200mV	3
	А	BA[1:0], BG[1:0], A[9:0], A10/AP, A11, A12/BC_n, A13, WE_n/A14, CAS_n/A15, RAS_n/A16, A17, CKE, ACT_n, ODT, CLK_t, CLK_c, PAR	V _{REFCA} ±200mV	3
Test	В	LDM_n/LDBI_n, UDM_n/UDBI_n; DM_n/DBI_n	V _{REFDQ} ±200mV	4
input	С	ALERT_n	CMOS (20%/80% V _{DD})	2, 5
	D	RESET_n	CMOS (20%/80% V _{DD})	2
Test output		DQ[15:0], UDQS_t, UDQS_c, LDQS_t, LDQS_c; DQS_t, DQS_c	V _{TT} ±100mV	6

Notes:

- TEN: Connectivity test mode is active when TEN is HIGH and inactive when TEN is LOW.
 TEN must be LOW during normal operation.
- 2. CMOS is a rail-to-rail signal with DC HIGH at 80% and DC LOW at 20% of V_{DD} (960mV for DC HIGH and 240mV for DC LOW.)
- 3. V_{REFCA} should be V_{DD}/2.
- 4. V_{REFDO} should be V_{DDO}/2.
- 5. ALERT_n switching level is not a final setting.
- 6. V_{TT} should be set to $V_{DD}/2$.

Minimum Terms Definition for Logic Equations

The test input and output pins are related by the following equations, where INV denotes a logical inversion operation and XOR a logical exclusive OR operation:

MT0 = XOR (A1, A6, PAR)

 $MT1 = XOR (A8, ALERT_n, A9)$

MT2 = XOR (A2, A5, A13) or XOR (A2, A5, A13, A17)

MT3 = XOR (A0, A7, A11)

 $MT4 = XOR (CK_c, ODT, CAS_n/A15)$

MT5 = XOR (CKE, RAS_n/A16, A10/AP)

 $MT6 = XOR (ACT_n, A4, BA1)$

 $MT7 = \times 16$: XOR (DMU_n/DBIU_n, DML_n/DBIL_n, CK_t)

= x8: XOR (BG1, DML_n/DBIL_n, CK_t)

 $= x4: XOR (BG1, CK_t)$

 $MT8 = XOR (WE_n/A14, A12 / BC, BA0)$

MT9 = XOR (BG0, A3, RESET n and TEN)

Logic Equations for a x4 Device

DQ0 = XOR (MT0, MT1)

DQ1 = XOR (MT2, MT3)

DQ2 = XOR (MT4, MT5)

DQ3 = XOR (MT6, MT7)

 $DQS_t = MT8$

 $DQS_c = MT9$



Logic Equations for a x8 Device

DQ0 = MT0	DQ5 = MT5
DQ1 = MT1	DQ6 = MT6
DQ2 = MT2	DQ7 = MT7
DQ3 = MT3	$DQS_t = MT8$
DQ4 = MT4	$DQS_c = MT9$

Logic Equations for a x16 Device

DQ0 = MT0	DQ10 = INV DQ2
DQ1 = MT1	DQ11 = INV DQ3
DQ2 = MT2	DQ12 = INV DQ4
DQ3 = MT3	DQ13 = INV DQ5
DQ4 = MT4	DQ14 = INV DQ6
DQ5 = MT5	DQ15 = INV DQ7
DQ6 = MT6	$LDQS_t = MT8$
DQ7 = MT7	$LDQS_c = MT9$
DQ8 = INV DQ0	$UDQS_t = INV LDQS_t$
DQ9 = INV DQ1	$UDQS_c = INV LDQS_c$

CT Input Timing Requirements

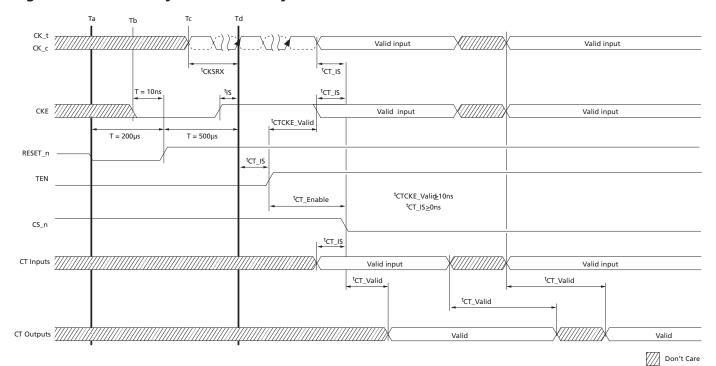
Prior to the assertion of the TEN pin, all voltage supplies, including V_{REFCA} , must be valid and stable and RESET_n registered high prior to entering CT mode. Upon the assertion of the TEN pin HIGH with RESET_n, CKE, and CS_n held HIGH; CLK_t, CLK_c, and CKE signals become test inputs within tCTECT_Valid . The remaining CT inputs become valid tCT_Enable after TEN goes HIGH when CS_n allows input to begin sampling, provided inputs were valid for at least tCT_Valid . While in CT mode, refresh activities in the memory arrays are not allowed; they are initiated either externally (auto refresh) or internally (self refresh).

The TEN pin may be asserted after the DRAM has completed power-on. After the DRAM is initialized and V_{REFDQ} is calibrated, CT mode may no longer be used. The TEN pin may be de-asserted at any time in CT mode. Upon exiting CT mode, the states and the integrity of the original content of the memory array are unknown. A full reset of the memory device is required.

After CT mode has been entered, the output signals will be stable within ^tCT_Valid after the test inputs have been applied as long as TEN is maintained HIGH and CS_n is maintained LOW.



Figure 74: Connectivity Test Mode Entry





Excessive Row Activation

Rows can be accessed a limited number of times within a certain time period before adjacent rows require refresh. The maximum activate count (MAC) is the maximum number of activates that a single row can sustain within a time interval of equal to or less than the maximum activate window (tMAW) before the adjacent rows need to be refreshed, regardless of how the activates are distributed over tMAW.

Micron's DDR4 devices automatically perform a type of TRR mode in the background and provide an MPR Page 3 MPR3[3:0] of 1000, indicating there is no restriction to the number of ACTIVATE commands to a given row in a refresh period provided DRAM timing specifications are not violated. However, specific attempts to by-pass TRR may result in data disturb.

Table 40: MAC Encoding of MPR Page 3 MPR3

[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	MAC	Comments
Х	х	х	х	0	0	0	0	Untested	The device has not been tested for MAC.
Х	х	х	х	0	0	0	1	^t MAC = 700K	
Х	х	Х	х	0	0	1	0	^t MAC = 600K	
Х	х	Х	х	0	0	1	1	^t MAC = 500K	
Х	х	Х	х	0	1	0	0	^t MAC = 400K	
Х	х	х	х	0	1	0	1	^t MAC = 300K	
Х	х	х	х	0	1	1	0	Reserved	
Х	х	х	х	0	1	1	1	^t MAC = 200K	
Х	х	X	х	1	0	0	0	Unlimited	There is no restriction to the number of AC- TIVATE commands to a given row in a re- fresh period provided DRAM timing specifi- cations are not violated.
Х	х	х	х	1	0	0	1	Reserved	
Х	х	х	х	:	:	:	:	Reserved	
Х	х	х	х	1	1	1	1	Reserved	

Note: 1. MAC encoding in MPR Page 3 MPR3.



Post Package Repair

Post Package Repair

JEDEC defines two modes of Post Package Repair (PPR): soft Post Package Repair (sPPR) and hard Post Package Repair (hPPR). sPPR is non-persistent so the repair row maybe altered; that is, sPPR is NOT a permanent repair and even though it will repair a row, the repair can be reversed, reassigned via another sPPR, or made permanent via hPPR. Hard Post Package Repair is persistent so once the repair row is assigned for a hPPR address, further PPR commands to a previous hPPR section should not be performed, that is, hPPR is a permanent repair; once repaired, it cannot be reversed. The controller provides the failing row address in the hPPR/sPPR sequence to the device to perform the row repair. hPPR Mode and sPPR Mode may not be enabled at the same time.

JEDEC states hPPR is optional for 4Gb and sPPR is optional for 4Gb and 8Gb parts however Micron 4Gb and 8Gb DDR4 DRAMs should have both sPPR and hPPR support. The hPPR support is identified via an MPR read from MPR Page 2, MPR0[7] and sPPR support is identified via an MPR read from MPR Page 2, MPR0[6].

The JEDEC minimum support requirement for DDR4 PPR (hPPR or sPPR) is to provide one row of repair per bank group (BG), x4/x8 have 4 BG and x16 has 2 BG; this is a total of 4 repair rows available on x4/x8 and 2 repair rows available on x16. Micron PPR support exceeds the JEDEC minimum requirements; Micron DDR4 DRAMs have at least one row of repair for each bank which is essentially 4 row repairs per BG for a total of 16 repair rows for x4 and x8 and 8 repair rows for x16; a 4x increase in repair rows.

JEDEC requires the user to have all sPPR row repair addresses reset and cleared prior to enabling hPPR Mode. Micron DDR4 PPR does not have this restriction, the existing sPPR row repair addresses are not required to be cleared prior to entering hPPR mode. Each bank in a BG is PPR independent: sPPR or hPPR issued to a bank will not alter a sPPR row repair existing in a different bank.

sPPR followed by sPPR to same bank

When PPR is issued to a bank for the first time and is a sPPR command, the repair row will be a sPPR. When a subsequent sPPR is issued to the same bank, the previous sPPR repair row will be cleared and used for the subsequent sPPR address as the sPPR operation is non-persistent.

sPPR followed by hPPR to same bank

When a PPR is issued to a bank for the first time and is a sPPR command, the repair row will be a sPPR. When a subsequent hPPR is issued to the same bank, the initial sPPR repair row will be cleared and used for the hPPR address. If a further subsequent PPR (hPPR or sPPR) is issued to the same bank, the further subsequent PPR (hPPR or sPPR) repair row will not clear or overwrite the previous hPPR address as the hPPR operation is persistent.

hPPR followed by hPPR or sPPR to same bank

When a PPR is issued to a bank for the first time and is a hPPR command, the repair row will be a hPPR. When a subsequent PPR (hPPR or sPPR) is issued to the same bank, the subsequent PPR (hPPR or sPPR) repair row will not clear or overwrite the initial hPPR address as the initial hPPR is persistent.



Hard Post Package Repair

All banks must be precharged and idle. DBI and CRC modes must be disabled. Both sPPR and hPPR must be disabled. sPPR is disabled with MR4[5] = 0. hPPR is disabled with MR4[13] = 0, which is the normal state, and hPPR is enabled with MR4 [13]= 1, which is the hPPR enabled state. There are two forms of hPPR mode. Both forms of hPPR have the same entry requirement as defined in the sections below. The first command sequence uses a WRA command and supports data retention with a REFRESH operation except for the bank containing the row that is being repaired; JEDEC has relaxed this requirement and allows BA[0] to be a don't care regarding the banks which are not required to maintain data a REFRESH operation during hPPR. The second command sequence uses a WR command (a REFRESH operation can't be performed in this command sequence). The second command sequence doesn't support data retention for the target DRAM.

hPPR Row Repair - Entry

As stated above, all banks must be precharged and idle. DBI and CRC modes must be disabled, and all timings must be followed as shown in the timing diagram that follows.

All other commands except those listed in the following sequences are illegal.

- 1. Issue MR4[13] 1 to enter hPPR mode enable.
 - a. All DO are driven HIGH.
- 2. Issue four consecutive guard key commands (shown in the table below) to MR0 with each command separated by ^tMOD. The PPR guard key settings are the same whether performing sPPR or hPPR mode.
 - a. Any interruption of the key sequence by other commands, such as ACT, WR, RD, PRE, REF, ZQ, and NOP, are not allowed.
 - b. If the guard key bits are not entered in the required order or interrupted with other MR commands, hPPR will not be enabled, and the programming cycle will result in a NOP.
 - c. When the hPPR entry sequence is interrupted and followed by ACT and WR commands, these commands will be conducted as normal DRAM commands.
 - d. JEDEC allows A6:0 to be "Don't Care" on 4Gb and 8Gb devices from a supplier perspective and the user should rely on vendor datasheet.

Table 41: PPR MR0 Guard Key Settings

MR0	BG1:0	BA1:0	A17:12	A11	A10	A9	A8	A7	A6:0
First guard key	0	0	xxxxxx	1	1	0	0	1	1111111
Second guard key	0	0	xxxxxx	0	1	1	1	1	1111111
Third Guard key	0	0	xxxxxx	1	0	1	1	1	1111111
Fourth guard key	0	0	xxxxxx	0	0	1	1	1	1111111

hPPR Row Repair - WRA Initiated (REF Commands Allowed)

- 1. Issue an ACT command with failing BG and BA with the row address to be repaired.
- 2. Issue a WRA command with BG and BA of failing row address.
 - a. The address must be at valid levels, but the address is "Don't Care."



- 3. All DQ of the target DRAM should be driven LOW for 4nCK (bit 0 through bit 7) after WL (WL = CWL + AL + PL) in order for hPPR to initiate repair.
 - a. Repair **will be** initiated to the target DRAM only if all DQ during bit 0 through bit 7 are LOW. The bank under repair does not get the REFRESH command applied to it.
 - b. Repair **will not be** initiated to the target DRAM if any DQ during bit 0 through bit 7 is HIGH.
 - JEDEC states: All DQs of target DRAM should be LOW for 4^tCK. If HIGH is driven to all DQs of a DRAM consecutively for equal to or longer than 2^tCK, then DRAM does not conduct hPPR and retains data if REF command is properly issued; if all DQs are neither LOW for 4^tCK nor HIGH for equal to or longer than 2^tCK, then hPPR mode execution is unknown.
 - c. DQS should function normally.
- 4. REF command may be issued anytime after the WRA command followed by WL + $4nCK + {}^{t}WR + {}^{t}RP$.
 - a. Multiple REF commands are issued at a rate of ^tREFI or ^tREFI/2, however back-to-back REF commands must be separated by at least ^tREFI/4 when the DRAM is in hPPR mode.
 - b. All banks except the bank under repair will perform refresh.
- 5. Issue PRE after ^tPGM time so that the device can repair the target row during ^tPGM time.
 - a. Wait ^tPGM_Exit after PRE to allow the device to recognize the repaired target row address.
- 6. Issue MR4[13] 0 command to hPPR mode disable.
 - a. Wait ^tPGMPST for hPPR mode exit to complete.
 - b. After tPGMPST has expired, any valid command may be issued.

The entire sequence from hPPR mode enable through hPPR mode disable may be repeated if more than one repair is to be done.

After completing hPPR mode, MR0 must be re-programmed to a prehPPR mode state if the device is to be accessed.

After hPPR mode has been exited, the DRAM controller can confirm if the target row was repaired correctly by writing data into the target row and reading it back.



Figure 75: hPPR WRA - Entry

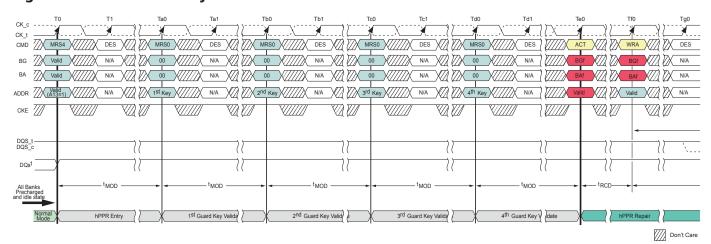
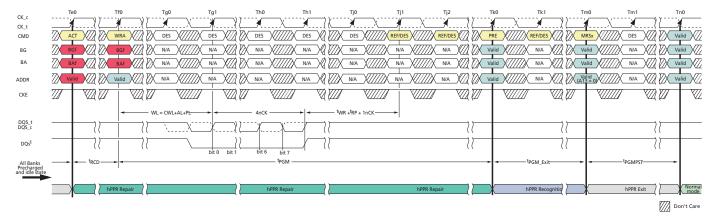


Figure 76: hPPR WRA - Repair and Exit



hPPR Row Repair - WR Initiated (REF Commands NOT Allowed)

- 1. Issue an ACT command with failing BG and BA with the row address to be repaired.
- 2. Issue a WR command with BG and BA of failing row address.
 - a. The address must be at valid levels, but the address is "Don't Care."
- 3. All DQ of the target DRAM should be driven LOW for 4nCK (bit 0 through bit 7) after WL (WL = CWL + AL + PL) in order for hPPR to initiate repair.
 - a. Repair **will be** initiated to the target DRAM only if all DQ during bit 0 through bit 7 are LOW.
 - b. Repair **will not be** initiated to the target DRAM if any DQ during bit 0 through bit 7 is HIGH.
 - 1. JEDEC states: All DQs of target DRAM should be LOW for 4^tCK. If HIGH is driven to all DQs of a DRAM consecutively for equal to or longer than 2^tCK, then DRAM does not conduct hPPR and retains data if REF command is properly issued; if all DQs are neither LOW for 4^tCK nor HIGH for equal to or longer than 2^tCK, then hPPR mode execution is unknown.



- c. DQS should function normally.
- 4. REF commands may NOT be issued at anytime while in PPT mode.
- 5. Issue PRE after ^tPGM time so that the device can repair the target row during ^tPGM time.
 - a. Wait ^tPGM_Exit after PRE to allow the device to recognize the repaired target row address.
- 6. Issue MR4[13] 0 command to hPPR mode disable.
 - a. Wait ^tPGMPST for hPPR mode exit to complete.
 - b. After tPGMPST has expired, any valid command may be issued.

The entire sequence from hPPR mode enable through hPPR mode disable may be repeated if more than one repair is to be done.

After completing hPPR mode, MR0 must be re-programmed to a prehPPR mode state if the device is to be accessed.

After hPPR mode has been exited, the DRAM controller can confirm if the target row was repaired correctly by writing data into the target row and reading it back.

Figure 77: hPPR WR - Entry

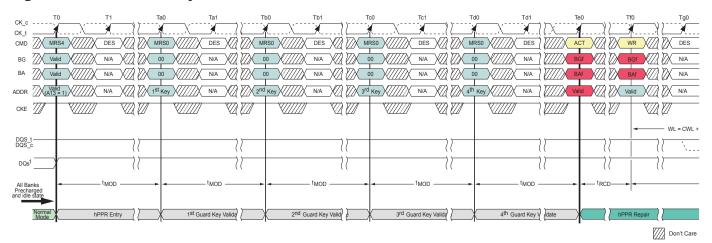


Figure 78: hPPR WR - Repair and Exit

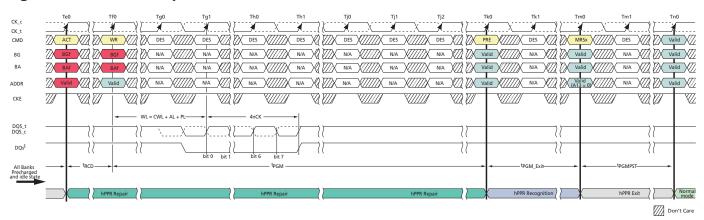




Table 42: DDR4 hPPR Timing Parameters DDR4-1600 through DDR4-3200

Parameter	Symbol		Min	Мах	Unit
hPPR programming time	^t PGM	×4, ×8	1000	_	ms
		×16	2000	_	ms
hPPR precharge exit time	^t PGM_Exit		15	_	ns
hPPR exit time	^t PGMPS1	Γ	50	_	μs

sPPR Row Repair

Soft post package repair (sPPR) is a way to quickly, but temporarily, repair a row element in a bank on a DRAM device, where hPPR takes longer but permanently repairs a row element. sPPR mode is entered in a similar fashion as hPPR, sPPR uses MR4[5] while hPPR uses MR4[13]. sPPR is disabled with MR4[5] = 0, which is the normal state, and sPPR is enabled with MR4[5] = 1, which is the sPPR enabled state.

sPPR requires the same guard key sequence as hPPR to qualify the MR4 PPR entry. After sPPR entry, an ACT command will capture the target bank and target row, herein seed row, where the row repair will be made. After ^tRCD time, a WR command is used to select the individual DRAM, through the DQ bits, to transfer the repair address into an internal register in the DRAM. After a write recovery time and PRE command, the sPPR mode can be exited and normal operation can resume.

The DRAM will retain the soft repair information as long as V_{DD} remains within the operating region unless rewritten by a subsequent sPPR entry to the same bank. If DRAM power is removed or the DRAM is reset, the soft repair will revert to the unrepaired state. hPPR and sPPR should not be enabled at the same time; Micron sPPR does not have to be disabled and cleared prior to entering hPPR mode.

With sPPR, Micron DDR4 can repair one row per bank. When a subsequent sPPR request is made to the same bank, the subsequently issued sPPR address will replace the previous sPPR address. When the hPPR resource for a bank is used up, the bank should be assumed to not have available resources for sPPR. If a repair sequence is issued to a bank with no repair resource available, the DRAM will ignore the programming sequence.

The bank receiving sPPR change is expected to retain memory array data in all rows except for the seed row and its associated row addresses. If the data in the memory array in the bank under sPPR repair is not required to be retained, then the handling of the seed row's associated row addresses is not of interest and can be ignored. If the data in the memory array is required to be retained in the bank under sPPR mode, then prior to executing the sPPR mode, the seed row and its associated row addresses should be backed up and subsequently restored after sPPR has been completed. sPPR associated seed row addresses are specified in the Table below; BA0 is not required by Micron DRAMs however it is JEDEC reserved.

Table 43: sPPR Associated Rows

	sPPR Associated Row Address										
BA0*	A17	A16	A15	A14	A13	A1	A0				



All banks must be precharged and idle. DBI and CRC modes must be disabled, and all sPPR timings must be followed as shown in the timing diagram that follows.

All other commands except those listed in the following sequences are illegal.

- 1. Issue MR4[5] 1 to enter sPPR mode enable.
 - a. All DQ are driven HIGH.
- 2. Issue four consecutive guard key commands (shown in the table below) to MR0 with each command separated by ^tMOD. Please note that JEDEC recently added the four guard key entry used for hPPR to sPPR entry; early DRAMs may not require four guard key entry code. A prudent controller design should accommodate either option in case an earlier DRAM is used.
 - a. Any interruption of the key sequence by other commands, such as ACT, WR, RD, PRE, REF, ZQ, and NOP, are not allowed.
 - b. If the guard key bits are not entered in the required order or interrupted with other MR commands, sPPR will not be enabled, and the programming cycle will result in a NOP.
 - c. When the sPPR entry sequence is interrupted and followed by ACT and WR commands, these commands will be conducted as normal DRAM commands.
 - d. JEDEC allows A6:0 to be "Don't Care" on 4Gb and 8Gb devices from a supplier perspective and the user should rely on vendor datasheet.

Table 44: PPR MR0 Guard Key Settings

MR0	BG1:0	BA1:0	A17:12	A11	A10	A9	A8	A7	A6:0
First guard key	0	0	xxxxxx	1	1	0	0	1	1111111
Second guard key	0	0	xxxxxx	0	1	1	1	1	1111111
Third guard key	0	0	xxxxxx	1	0	1	1	1	1111111
Fourth guard key	0	0	xxxxxx	0	0	1	1	1	1111111

- 3. After ^tMOD, issue an ACT command with failing BG and BA with the row address to be repaired.
- 4. After ^tRCD, issue a WR command with BG and BA of failing row address.
 - a. The address must be at valid levels, but the address is a "Don't Care."
- 5. All DQ of the target DRAM should be driven LOW for 4nCK (bit 0 through bit 7) after WL (WL = CWL + AL + PL) in order for sPPR to initiate repair.
 - Repair will be initiated to the target DRAM only if all DQ during bit 0 through bit 7 are LOW.
 - b. Repair **will not be** initiated to the target DRAM if any DQ during bit 0 through bit 7 is HIGH.
 - 1. JEDEC states: All DQs of target DRAM should be LOW for 4^tCK. If HIGH is driven to all DQs of a DRAM consecutively for equal to or longer than the first 2^tCK, then DRAM does not conduct hPPR and retains data if REF command is properly issued; if all DQs are neither LOW for 4^tCK nor HIGH for equal to or longer than the first 2^tCK, then hPPR mode execution is unknown.
 - c. DQS should function normally.
- 6. REF command may NOT be issued at anytime while in sPPR mode.
- 7. Issue PRE after ^tWR time so that the device can repair the target row during ^tWR time.
 - a. Wait ^tPGM_Exit_s after PRE to allow the device to recognize the repaired target row address.



- 8. Issue MR4[5] 0 command to sPPR mode disable.
 - a. Wait ^tPGMPST_s for sPPR mode exit to complete.
 - b. After tPGMPST_s has expired, any valid command may be issued.

The entire sequence from sPPR mode enable through sPPR mode disable may be repeated if more than one repair is to be done.

After sPPR mode has been exited, the DRAM controller can confirm if the target row was repaired correctly by writing data into the target row and reading it back.

Figure 79: sPPR - Entry

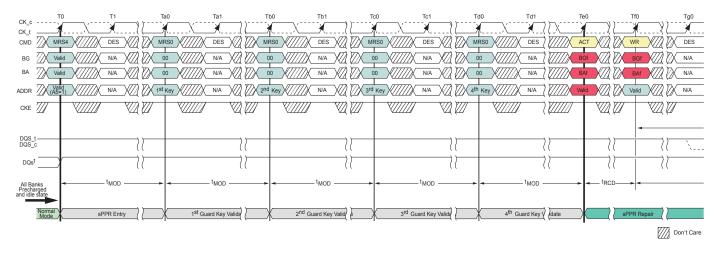


Figure 80: sPPR - Repair, and Exit

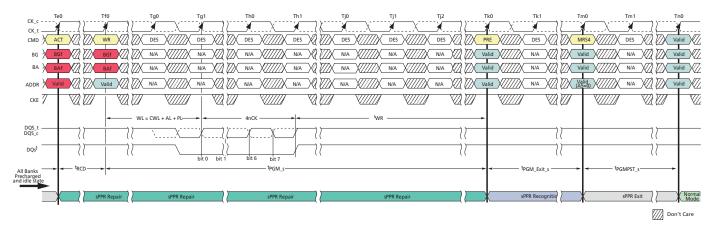


Table 45: DDR4 sPPR Timing Parameters DDR4-1600 through DDR4-3200

Parameter	Symbol	Min	Max	Unit
sPPR programming time	^t PGM_s	^t RCD(MIN)+ WL + 4nCK + ^t WR(MIN)	-	ns
sPPR precharge exit time	^t PGM_Exit_s	20	_	ns
sPPR exit time	^t PGMPST_s	^t MOD	-	ns



hPPR/sPPR Support Identifier

Table 46: DDR4 Repair Mode Support Identifier

MPR Page 2	A7	A6	A5	A4	A3	A2	A1	A0
	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
MPR0	hPPR ¹	sPPR ²	R _{TT_WR}	Temp sensor		CRC	R _{TT_WR}	

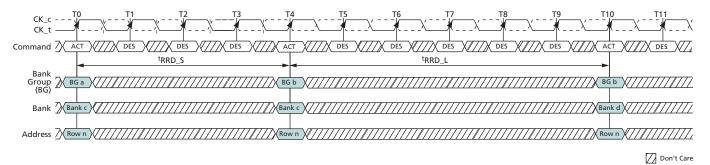
Notes:

- 1. 0 = hPPR mode is not available, 1 = hPPR mode is available.
- 2. 0 = sPPR mode is not available, 1 = sPPR mode is available.
- 3. Gray shaded areas are for reference only.

ACTIVATE Command

The ACTIVATE command is used to open (activate) a row in a particular bank for subsequent access. The values on the BG[1:0] inputs select the bank group, the BA[1:0] inputs select the bank within the bank group, and the address provided on inputs A[17:0] selects the row within the bank. This row remains active (open) for accesses until a PRE-CHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank. Bank-to-bank command timing for AC-TIVATE commands uses two different timing parameters, depending on whether the banks are in the same or different bank group. [†]RRD_S (short) is used for timing between banks located in different bank groups. [†]RRD_L (long) is used for timing between banks located in the same bank group. Another timing restriction for consecutive ACTIVATE commands [issued at [†]RRD (MIN)] is [†]FAW (four activate window). Because there is a maximum of four banks in a bank group, the [†]FAW parameter applies across different bank groups (five ACTIVATE commands issued at [†]RRD_L (MIN) to the same bank group would be limited by [†]RC).

Figure 81: ^tRRD Timing

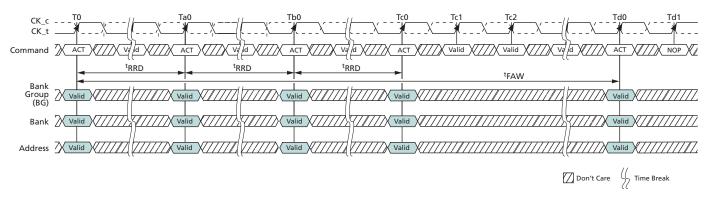


Notes

- 1. tRRD_S; ACTIVATE-to-ACTIVATE command period (short); applies to consecutive ACTIVATE commands to different bank groups (that is, T0 and T4).
- 2. ^tRRD_L; ACTIVATE-to-ACTIVATE command period (long); applies to consecutive ACTI-VATE commands to the different banks in the same bank group (that is, T4 and T10).



Figure 82: tFAW Timing



Note: 1. tFAW; four activate windows.

PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation for a specified time (^tRP) after the PRECHARGE command is issued. An exception to this is the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters.

After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

The auto precharge feature is engaged when a READ or WRITE command is issued with A10 HIGH. The auto precharge feature uses the RAS lockout circuit to internally delay the PRECHARGE operation until the ARRAY RESTORE operation has completed. The RAS lockout circuit feature allows the PRECHARGE operation to be partially or completely hidden during burst READ cycles when the auto precharge feature is engaged. The PRECHARGE operation will not begin until after the last data of the burst write sequence is properly stored in the memory array.

REFRESH Command

The REFRESH command (REF) is used during normal operation of the device. This command is nonpersistent, so it must be issued each time a refresh is required. The device requires REFRESH cycles at an average periodic interval of ^tREFI. When CS_n, RAS_n/A16, and CAS_n/A15 are held LOW and WE_n/A14 HIGH at the rising edge of the clock, the device enters a REFRESH cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time, ^tRP (MIN), before the REFRESH command can be applied. The refresh addressing is generated by the internal DRAM refresh controller. This makes the address bits "Don't Care" during a REFRESH command. An internal address counter supplies the addresses during the REFRESH cycle. No control of the external address bus is required once this cycle has started. When the REFRESH cycle has completed, all banks of the SDRAM will be in the precharged (idle)



state. A delay between the REFRESH command and the next valid command, except DES, must be greater than or equal to the minimum REFRESH cycle time ^tRFC (MIN), as shown in Figure 83 (page 144).

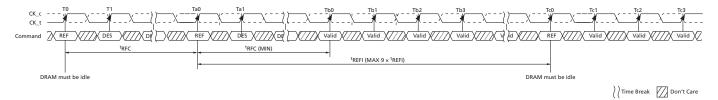
Note: The ^tRFC timing parameter depends on memory density.

In general, a REFRESH command needs to be issued to the device regularly every treating the transfer of the device regularly every treating the second secon interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pullingin the REFRESH command. A limited number REFRESH commands can be postponed depending on refresh mode: a maximum of 8 REFRESH commands can be postponed when the device is in 1X refresh mode; a maximum of 16 REFRESH commands can be postponed when the device is in 2X refresh mode; and a maximum of 32 REFRESH commands can be postponed when the device is in 4X refresh mode.

When 8 consecutive REFRESH commands are postponed, the resulting maximum interval between the surrounding REFRESH commands is limited to $9 \times {}^{t}$ REFI (see Figure 84 (page 145)). For both the 2X and 4X refresh modes, the maximum interval between surrounding REFRESH commands allowed is limited to 17 × ^tREFI2 and 33 × ^tREFI4, respectively.

A limited number REFRESH commands can be pulled-in as well. A maximum of 8 additional REFRESH commands can be issued in advance or "pulled-in" in 1X refresh mode, a maximum of 16 additional REFRESH commands can be issued when in advance in 2X refresh mode, and a maximum of 32 additional REFRESH commands can be issued in advance when in 4X refresh mode. Each of these REFRESH commands reduces the number of regular REFRESH commands required later by one. The resulting maximum interval between two surrounding REFRESH commands is limited to 9 × ^tREFI (Figure 85 (page 145)), 17 × ^tRFEI2, or 33 × ^tREFI4. At any given time, a maximum of 16 REF commands can be issued within 2 × ^tREFI, 32 REF2 commands can be issued within 4 × t REFI2, and 64 REF4 commands can be issued within $8 \times ^{t}$ REFI4 (larger densities are limited by tRFC1, tRFC2, and tRFC4, respectively, which must still be met).

Figure 83: REFRESH Command Timing



1. Only DES commands are allowed after a REFRESH command is registered until ^tRFC

- (MIN) expires.
- Time interval between two REFRESH commands may be extended to a maximum of 9 × tREFI.



Figure 84: Postponing REFRESH Commands (Example)

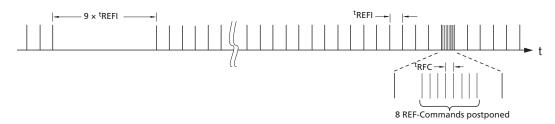
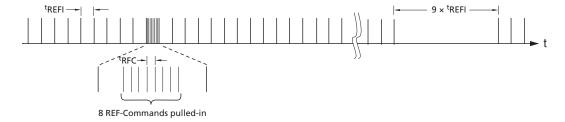


Figure 85: Pulling In REFRESH Commands (Example)





Temperature-Controlled Refresh Mode

During normal operation, temperature-controlled refresh (TCR) mode disabled, the device must have a REFRESH command issued once every $^t\text{REFI}$, except for what is allowed by posting (see REFRESH Command section). This means a REFRESH command must be issued once every 7.8µs if T_C is less than or equal to 85°C, once every 3.9µs if T_C is greater than 95°C, once every 3.9µs if T_C is greater than 95°C, regardless of which Temperature Mode is selected (MR4[2]). TCR mode is disabled by setting MR4[3] = 0 while TCR mode is enabled by setting MR4[3] = 1. When TCR mode is enabled (MR4[3] = 1), the Temperature Mode must be selected where MR4[2] = 0 enables the Normal Temperature Mode while MR4[2] = 1 enables the Extended Temperature Mode.

When TCR mode is enabled, the device will register the externally supplied REFRESH command and adjust the internal refresh period to be longer than ^tREFI of the normal temperature range, when allowed, by skipping REFRESH commands with the proper gear ratio. TCR mode has two Temperature Modes to select between the normal temperature range and the extended temperature range; the correct Temperature Mode must be selected so the internal control operates correctly. The DRAM must have the correct refresh rate applied externally; the internal refresh rate is determined by the DRAM based upon the temperature.

Normal Temperature Mode

REFRESH commands should be issued to the device with the refresh period equal to $^t\!REFI$ of normal temperature range (-40°C to 85°C). The system must guarantee that the T_C does not exceed 85°C when $^t\!REFI$ of the normal temperature range is used. The device may adjust the internal refresh period to be longer than $^t\!REFI$ of the normal temperature range by skipping external REFRESH commands with the proper gear ratio when T_C is below 85°C. The internal refresh period is automatically adjusted inside the DRAM, and the DRAM controller does not need to provide any additional control.

Extended Temperature Mode

REFRESH commands should be issued to the device with the refresh period equal to ${}^{t}\!\text{REFI}$ of extended temperature range (85°C to 95°C, or 95°C to 105°C) . The system must guarantee that the T_C does not exceed 95°C, or 105°C. Even though the external refresh supports the extended temperature range, the device may adjust its internal refresh period to be equal to or longer than ${}^{t}\!\text{REFI}$ of the normal temperature range (-40°C to 85°C) by skipping external REFRESH commands with the proper gear ratio when T_C is equal to or below 85°C. The internal refresh period is automatically adjusted inside the DRAM, and the DRAM controller does not need to provide any additional control.

Table 47: Normal ^tREFI Refresh (TCR Enabled)

	Normal Temp	erature Mode	Extended Temperature Mode			
Temperature	External Refresh Period			Internal Refresh Period		
T _C ≤ 85°C	7.8µs	≥7.8µs	3.9µs¹	≥7.8µs		
85°C < T _C ≤ 95°C		3.9	θμs			



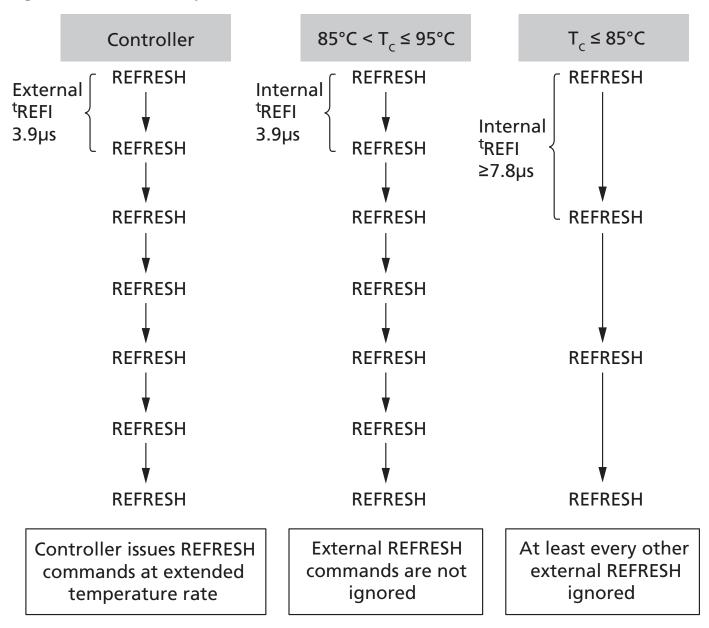
Table 47: Normal ^tREFI Refresh (TCR Enabled) (Continued)

	Normal Temp	erature Mode	Extended Temperature Mode				
Temperature	External Refresh Period	Internal Refresh Period	External Refresh Period	Internal Refresh Period			
95°C < T _C ≤ 105°C	1.95μs						

Note: 1. If the external refresh period is slower than 3.9µs, the device will refresh internally at too slow of a refresh rate and will violate refresh specifications.



Figure 86: TCR Mode Example¹



Note: 1. TCR enabled with Extended Temperature Mode selected.



Fine Granularity Refresh Mode

Mode Register and Command Truth Table

The REFRESH cycle time (^tRFC) and the average refresh interval (^tREFI) can be programmed by the MRS command. The appropriate setting in the mode register will set a single set of REFRESH cycle times and average refresh interval for the device (fixed mode), or allow the dynamic selection of one of two sets of REFRESH cycle times and average refresh interval for the device (on-the-fly mode [OTF]). OTF mode must be enabled by MRS before any OTF REFRESH command can be issued.

Table 48: MRS Definition

MR3[8]	MR3[7]	MR3[6]	Refresh Rate Mode
0	0	0	Normal mode (fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	On-the-fly 1x/2x
1	1	0	On-the-fly 1x/4x
1	1	1	Reserved

There are two types of OTF modes (1x/2x and 1x/4x modes) that are selectable by programming the appropriate values into the mode register MR3 [8:6]. When either of the two OTF modes is selected, the device evaluates the BG0 bit when a REFRESH command is issued, and depending on the status of BG0, it dynamically switches its internal refresh configuration between 1x and 2x (or 1x and 4x) modes, and then executes the corresponding REFRESH operation.

Table 49: REFRESH Command Truth Table

Refresh	CS_n	ACT_n	RAS_n/A 15	CAS_n/A 14	WE_n/ A13	BG1	BG0	A10/ AP	A[9:0], A[12:11], A[20:16]	MR3[8:6
Fixed rate	L	Н	L	L	Н	V	V	V	V	0vv
OTF: 1x	L	Н	L	L	Н	V	L	V	V	1vv
OTF: 2x	L	Н	L	L	Н	V	Н	V	V	101
OTF: 4x	L	Н	L	L	Н	V	Н	V	V	110

^tREFI and ^tRFC Parameters

The default refresh rate mode is fixed 1x mode where REFRESH commands should be issued with the normal rate; that is, ${}^{t}REFI1 = {}^{t}REFI(base)$ (for $T_C \le 85^{\circ}C$), and the duration of each REFRESH command is the normal REFRESH cycle time (${}^{t}RFC1$). In 2x mode (either fixed 2x or OTF 2x mode), REFRESH commands should be issued to the device at the double frequency (${}^{t}REFI2 = {}^{t}REFI(base)/2$) of the normal refresh rate. In 4x mode, the REFRESH command rate should be quadrupled (${}^{t}REFI4 = {}^{t}REFI(base)/4$). Per





each mode and command type, the ^tRFC parameter has different values as defined in the following table.

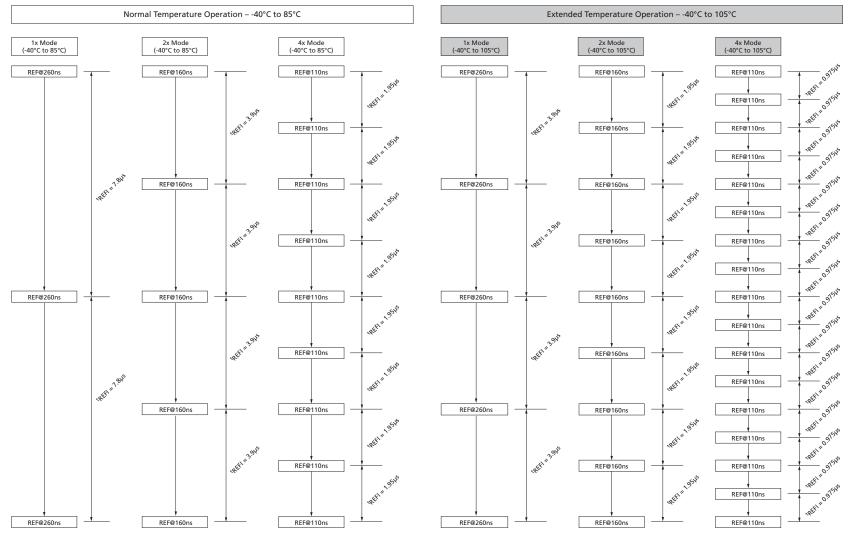
For discussion purposes, the REFRESH command that should be issued at the normal refresh rate and has the normal REFRESH cycle duration may be referred to as an REF1x command. The REFRESH command that should be issued at the double frequency (t REFI2 = t REFI(base)/2) may be referred to as a REF2x command. Finally, the REFRESH command that should be issued at the quadruple rate (t REFI4 = t REFI(base)/4) may be referred to as a REF4x command.

In the fixed 1x refresh rate mode, only REF1x commands are permitted. In the fixed 2x refresh rate mode, only REF2x commands are permitted. In the fixed 4x refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the OTF 1x/4x refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

Table 50: tREFI and tRFC Parameters

Refresh Mode	Parameter		2Gb	4Gb	8Gb	16Gb	Units
	^t REFI (base)		7.8	7.8	7.8	7.8	μs
1x mode	^t REFI1	-40°C ≤ T _C ≤ 85°C	^t REFI(base)	^t REFI(base)	^t REFI(base)	tREFI(base)	μs
		85°C ≤ T _C ≤ 95°C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	^t REFI(base)/2	μs
		95°C ≤ T _C ≤ 105°C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	^t REFI(base)/4	μs
	tRFC1		160	260	350	350	ns
2x mode	tREFI2	-40°C ≤ T _C ≤ 85°C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	^t REFI(base)/2	μs
		85°C ≤ T _C ≤ 95°C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	^t REFI(base)/4	μs
		95°C ≤ T _C ≤ 105°C	tREFI(base)/8	tREFI(base)/8	tREFI(base)/8	^t REFI(base)/8	μs
	tRFC2		110	160	260	260	ns
4x mode	^t REFI4	-40°C ≤ T _C ≤ 85°C	^t REFI(base)/4	tREFI(base)/4	tREFI(base)/4	^t REFI(base)/4	μs
		85°C ≤ T _C ≤ 95°C	^t REFI(base)/8	tREFI(base)/8	tREFI(base)/8	^t REFI(base)/8	μs
		95°C ≤ T _C ≤ 105°C	^t REFI(base)/16	tREFI(base)/16	tREFI(base)/16	^t REFI(base)/16	μs
	^t RFC4		90	110	160	160	ns

Figure 87: 4Gb with Fine Granularity Refresh Mode Example





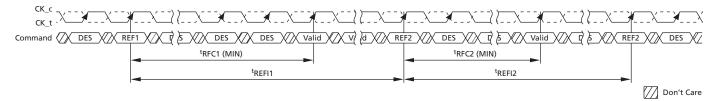
8Gb: x4, x8, x16 DDR4 SDRAM Fine Granularity Refresh Mode



Changing Refresh Rate

If the refresh rate is changed by either MRS or OTE New ^tREFI and ^tRFC parameters will be applied from the moment of the rate change. When the REF1x command is issued to the DRAM, ^tREF1 and ^tRFC1 are applied from the time that the command was issued; when the REF2x command is issued, ^tREF2 and ^tRFC2 should be satisfied.

Figure 88: OTF REFRESH Command Timing



The following conditions must be satisfied before the refresh rate can be changed. Otherwise, data retention cannot be guaranteed.

- In the fixed 2x refresh rate mode or the OTF 1x/2x refresh mode, an even number of REF2x commands must be issued because the last change of the refresh rate mode with an MRS command before the refresh rate can be changed by another MRS command.
- In the OTF1x/2x refresh rate mode, an even number of REF2x commands must be issued between any two REF1x commands.
- In the fixed 4x refresh rate mode or the OTF 1x/4x refresh mode, a multiple-of-four number of REF4x commands must be issued because the last change of the refresh rate with an MRS command before the refresh rate can be changed by another MRS command.
- In the OTF1x/4x refresh rate mode, a multiple-of-four number of REF4x commands must be issued between any two REF1x commands.

There are no special restrictions for the fixed 1x refresh rate mode. Switching between fixed and OTF modes keeping the same rate is not regarded as a refresh rate change.

Usage with TCR Mode

If the temperature controlled refresh mode is enabled, only the normal mode (fixed 1x mode, MR3[8:6] = 000) is allowed. If any other refresh mode than the normal mode is selected, the temperature controlled refresh mode must be disabled.

Self Refresh Entry and Exit

The device can enter self refresh mode anytime in 1x, 2x, and 4x mode without any restriction on the number of REFRESH commands that have been issued during the mode before the self refresh entry. However, upon self refresh exit, extra REFRESH command(s) may be required, depending on the condition of the self refresh entry.

The conditions and requirements for the extra REFRESH command(s) are defined as follows:

In the fixed 2x refresh rate mode or the enable-OTF 1x/2x refresh rate mode, it is recommended there be an even number of REF2x commands before entry into self refresh after the last self refresh exit, REF1x command, or MRS command that set the





refresh mode. If this condition is met, no additional REFRESH commands are required upon self refresh exit. In the case that this condition is not met, either one extra REF1x command or two extra REF2x commands must be issued upon self refresh exit. These extra REFRESH commands are not counted toward the computation of the average refresh interval (^tREFI).

• In the fixed 4x refresh rate mode or the enable-OTF 1x/4x refresh rate mode, it is recommended there be a multiple-of-four number of REF4x commands before entry into self refresh after the last self refresh exit, REF1x command, or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon self refresh exit. When this condition is not met, either one extra REF1x command or four extra REF4x commands must be issued upon self refresh exit. These extra REFRESH commands are not counted toward the computation of the average refresh interval (tREFI).

There are no special restrictions on the fixed 1x refresh rate mode.

This section does not change the requirement regarding postponed REFRESH commands. The requirement for the additional REFRESH command(s) described above is independent of the requirement for the postponed REFRESH commands.



SELF REFRESH Operation

The SELF REFRESH command can be used to retain data in the device, even if the rest of the system is powered down. When in self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate SELF REFRESH operation. The SELF REFRESH command is defined by having CS_n, RAS_n, CAS_n, and CKE held LOW with WE_n and ACT_n HIGH at the rising edge of the clock.

Before issuing the SELF REFRESH ENTRY command, the device must be idle with all banks in the precharge state and [†]RP satisfied. Idle state is defined as: All banks are closed ([†]RP, [†]DAL, and so on, satisfied), no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied ([†]MRD, [†]MOD, [†]RFC, [†]ZQinit, [†]ZQoper, [†]ZQCS, and so on). After the SELF REFRESH ENTRY command is registered, CKE must be held LOW to keep the device in self refresh mode. The DRAM automatically disables ODT termination, regardless of the ODT pin, when it enters self refresh mode and automatically enables ODT upon exiting self refresh. During normal operation (DLL_on), the DLL is automatically disabled upon entering self refresh and is automatically enabled (including a DLL reset) upon exiting self refresh.

When the device has entered self refresh mode, all of the external control signals, except CKE and RESET_n, are "Don't Care." For proper SELF REFRESH operation, all power supply and reference pins (V_{DD} , V_{DDQ} , V_{SS} , V_{SSQ} , V_{PP} , and V_{REFCA}) must be at valid levels. The DRAM internal V_{REFDQ} generator circuitry may remain on or be turned off depending on the MR6 bit 7 setting. If the internal V_{REFDQ} circuit is on in self refresh, the first WRITE operation or first write-leveling activity may occur after ^{t}XS time after self refresh exit. If the DRAM internal V_{REFDQ} circuitry is turned off in self refresh, it ensures that the V_{REFDQ} generator circuitry is powered up and stable within the $^{t}XSDLL$ period when the DRAM exits the self refresh state. The first WRITE operation or first write-leveling activity may not occur earlier than $^{t}XSDLL$ after exiting self refresh. The device initiates a minimum of one REFRESH command internally within the ^{t}CKE period once it enters self refresh mode.

The clock is internally disabled during a SELF REFRESH operation to save power. The minimum time that the device must remain in self refresh mode is ^tCKESR/ ^tCKESR_PAR. The user may change the external clock frequency or halt the external clock ^tCKSRE/^tCKSRE_PAR after self refresh entry is registered; however, the clock must be restarted and ^tCKSRX must be stable before the device can exit SELF REFRESH operation.

The procedure for exiting self refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a SELF REFRESH EXIT command (SRX, combination of CKE going HIGH and DESELECT on the command bus) is registered, the following timing delay must be satisfied:

Commands that do not require locked DLL:

- tXS = ACT, PRE, PREA, REF, SRE, and PDE.
- tXS_FAST = ZQCL, ZQCS, and MRS commands. For an MRS command, only DRAM CL, WR/RTP register, and DLL reset in MR0; R_{TT(NOM)} register in MR1; the CWL and R_{TT(WR)} registers in MR2; and gear-down mode register in MR3; WRITE and READ preamble registers in MR4; R_{TT(PARK)} register in MR5; Data rate and V_{REFDQ} calibration value registers in MR6 may be accessed provided the DRAM is not in per-DRAM mode. Access to other DRAM mode registers must satisfy tXS timing. WRITE commands (WR, WRS4, WRS8, WRA, WRAS4, and WRAS8) that require synchronous ODT and dynamic ODT controlled by the WRITE command require a locked DLL.



Commands that require locked DLL in the normal operating range:

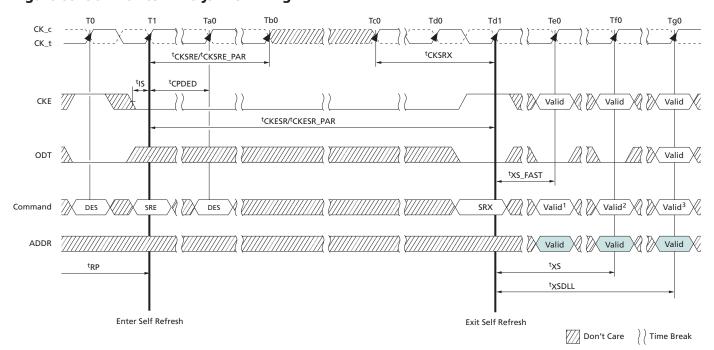
• ^tXSDLL – RD, RDS4, RDS8, RDA, RDAS4, and RDAS8 (unlike DDR3, WR, WRS4, WRS8, WRA, WRAS4, and WRAS8 because synchronous ODT is required).

Depending on the system environment and the amount of time spent in self refresh, ZQ CALIBRATION commands may be required to compensate for the voltage and temperature drift described in the ZQ CALIBRATION Commands section. To issue ZQ CALIBRATION commands, applicable timing requirements must be satisfied (see the ZQ Calibration Timing figure).

CKE must remain HIGH for the entire self refresh exit period ^tXSDLL for proper operation except for self refresh re-entry. Upon exit from self refresh, the device can be put back into self refresh mode or power-down mode after waiting at least ^tXS period and issuing one REFRESH command (refresh period of ^tRFC). The DESELECT command must be registered on each positive clock edge during the self refresh exit interval ^tXS. ODT must be turned off during ^tXSDLL.

The use of self refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self refresh mode. Upon exit from self refresh, the device requires a minimum of one extra REFRESH command before it is put back into self refresh mode.

Figure 89: Self Refresh Entry/Exit Timing

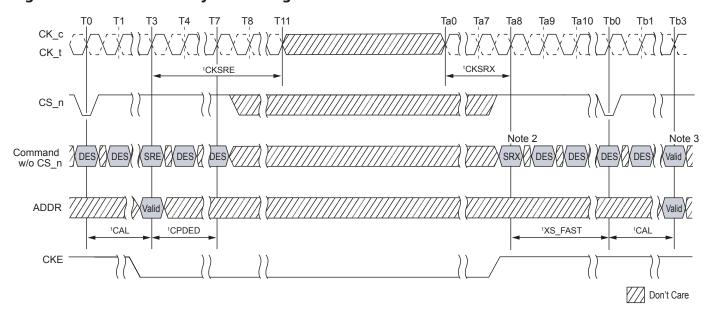


Notes:

- 1. Only MRS (limited to those described in the SELF REFRESH Operation section), ZQCS, or ZQCL commands are allowed.
- 2. Valid commands not requiring a locked DLL.
- 3. Valid commands requiring a locked DLL.



Figure 90: Self Refresh Entry/Exit Timing with CAL Mode



Notes:

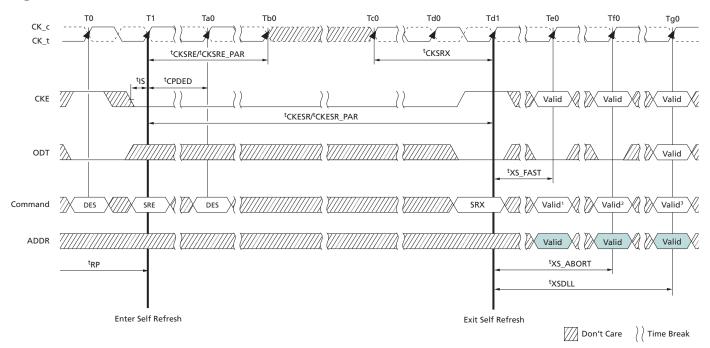
- 1. ^tCAL = 3*n*CK, ^tCPDED = 4*n*CK, ^tCKSRE/^tCKSRE_PAR = 8*n*CK, ^tCKSRX = 8*n*CK, ^tXS_FAST = ^tREFC4 (MIN) + 10ns.
- 2. CS_n = HIGH, ACT_n = "Don't Care," RAS_n/A16 = "Don't Care," CAS_n/A15 = "Don't Care," WE n/A14 = "Don't Care."
- 3. Only MRS (limited to those described in the SELF REFRESH Operations section), ZQCS, or ZQCL commands are allowed.
- 4. The figure only displays ^tXS_FAST timing, but ^tCAL must also be added to any ^tXS and ^tXSDLL associated commands during CAL mode.

Self Refresh Abort

The exit timing from self refresh exit to the first valid command not requiring a locked DLL is ^tXS. The value of ^tXS is (^tRFC+ 10ns). This delay allows any refreshes started by the device time to complete. ^tRFC continues to grow with higher density devices, so ^tXS will grow as well. An MRS bit enables the self refresh abort mode. If the bit is disabled, the controller uses ^tXS timings (location MR4, bit 9). If the bit is enabled, the device aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command not requiring a locked DLL after a delay of ^tXS_ABORT. Upon exit from self refresh, the device requires a minimum of one extra REFRESH command before it is put back into self refresh mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.



Figure 91: Self Refresh Abort



Notes:

- Only MRS (limited to those described in the SELF REFRESH Operation section), ZQCS, or ZQCL commands are allowed.
- 2. Valid commands not requiring a locked DLL with self refresh abort mode enabled in the mode register.
- 3. Valid commands requiring a locked DLL.

Self Refresh Exit with NOP Command

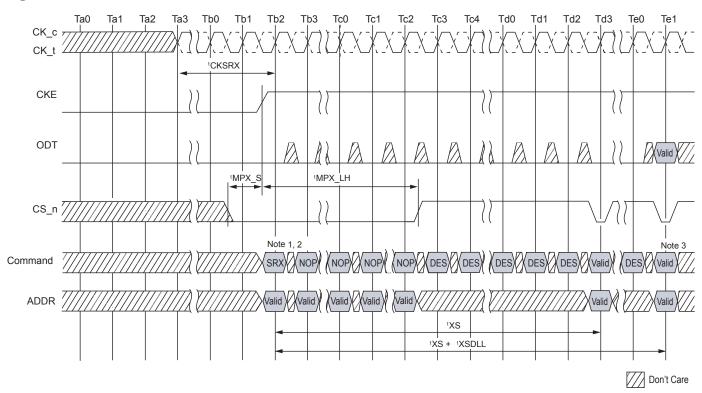
Exiting self refresh mode using the NO OPERATION command (NOP) is allowed under a specific system application. This special use of NOP allows for a common command/address bus between active DRAM devices and DRAM(s) in maximum power saving mode. Self refresh mode may exit with NOP commands provided:

- The device entered self refresh mode with CA parity, CAL, and gear-down disabled.
- tMPX S and tMPX LH are satisfied.
- NOP commands are only issued during ^tMPX_LH window.

No other command is allowed during the ^tMPX_LH window after an SELF REFRESH EXIT (SRX) command is issued.



Figure 92: Self Refresh Exit with NOP Command





Power-Down Mode

Power-down is synchronously entered when CKE is registered LOW (along with a DESE-LECT command). CKE is not allowed to go LOW when the following operations are in progress: MRS command, MPR operations, ZQCAL operations, DLL locking, or READ/WRITE operations. CKE is allowed to go LOW while any other operations, such as ROW ACTIVATION, PRECHARGE or auto precharge, or REFRESH, are in progress, but the power-down $I_{\rm DD}$ specification will not be applied until those operations are complete. The timing diagrams that follow illustrate power-down entry and exit.

For the fastest power-down exit timing, the DLL should be in a locked state when power-down is entered. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper READ operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as the controller complies with DRAM specifications.

During power-down, if all banks are closed after any in-progress commands are completed, the device will be in precharge power-down mode; if any bank is open after in-progress commands are completed, the device will be in active power-down mode.

Entering power-down deactivates the input and output buffers, excluding CK, CKE, and RESET_n. In power-down mode, DRAM ODT input buffer deactivation is based on Mode Register 5, bit 5 (MR5[5]). If it is configured to 0b, the ODT input buffer remains on and the ODT input signal must be at valid logic level. If it is configured to 1b, the ODT input buffer is deactivated and the DRAM ODT input signal may be floating and the device does not provide $R_{TT(NOM)}$ termination. Note that the device continues to provide $R_{TT(Park)}$ termination if it is enabled in MR5[8:6]. To protect internal delay on the CKE line to block the input signals, multiple DES commands are needed during the CKE switch off and on cycle(s); this timing period is defined as ^tCPDED. CKE LOW will result in deactivation of command and address receivers after ^tCPDED has expired.

Table 51: Power-Down Entry Definitions

DRAM Status	DLL	Power- Down Exit	Relevant Parameters
Active (a bank or more open)	On	Fast	^t XP to any valid command.
Precharged (all banks precharged)	On	Fast	^t XP to any valid command.

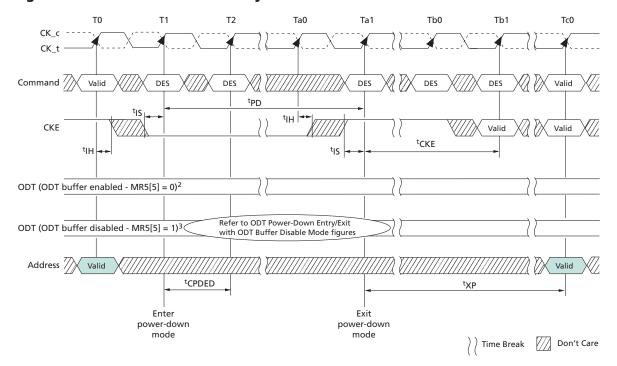
The DLL is kept enabled during precharge power-down or active power-down. In power-down mode, CKE is LOW, RESET_n is HIGH, and a stable clock signal must be maintained at the inputs of the device. ODT should be in a valid state, but all other input signals are "Don't Care." (If RESET_n goes LOW during power-down, the device will be out of power-down mode and in the reset state.) CKE LOW must be maintained until t CKE has been satisfied. Power-down duration is limited by $9 \times {}^{t}$ REFI.

The power-down state is synchronously exited when CKE is registered HIGH (along with DES command). CKE HIGH must be maintained until t CKE has been satisfied. The ODT input signal must be at a valid level when the device exits from power-down mode, independent of MR1 bit [10:8] if $R_{TT(NOM)}$ is enabled in the mode register. If $R_{TT(NOM)}$ is disabled, the ODT input signal may remain floating. A valid, executable command can



be applied with power-down exit latency, ^tXP, after CKE goes HIGH. Power-down exit latency is defined in the AC Specifications table.

Figure 93: Active Power-Down Entry and Exit

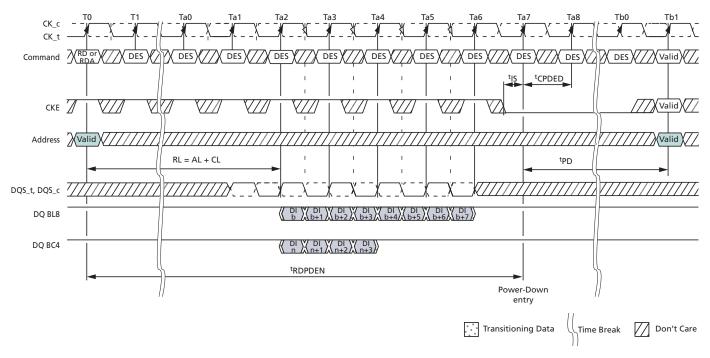


Notes:

- 1. Valid commands at T0 are ACT, DES, or PRE with one bank remaining open after completion of the PRECHARGE command.
- 2. ODT pin driven to a valid state; MR5[5] = 0 (normal setting).
- 3. ODT pin drive/float timing requirements for the ODT input buffer disable option (for additional power savings during active power-down) is described in the section for ODT Input Buffer Disable Mode for Power-Down (page 167); MR5[5] = 1.

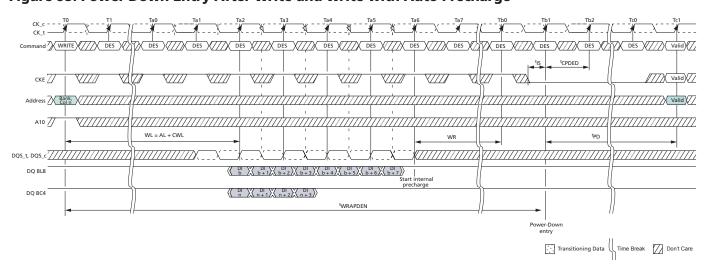


Figure 94: Power-Down Entry After Read and Read with Auto Precharge



Note: 1. DI n (or b) = data-in from column n (or b).

Figure 95: Power-Down Entry After Write and Write with Auto Precharge

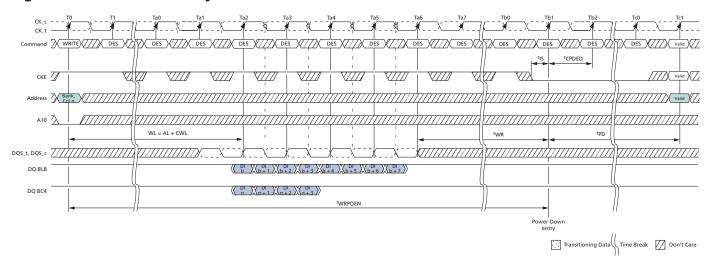


Notes: 1. DI n (or b) = data-in from column n (or b).

2. Valid commands at T0 are ACT, DES, or PRE with one bank remaining open after completion of the PRECHARGE command.



Figure 96: Power-Down Entry After Write



Note: 1. DI n (or b) = data-in from column n (or b).

Figure 97: Precharge Power-Down Entry and Exit

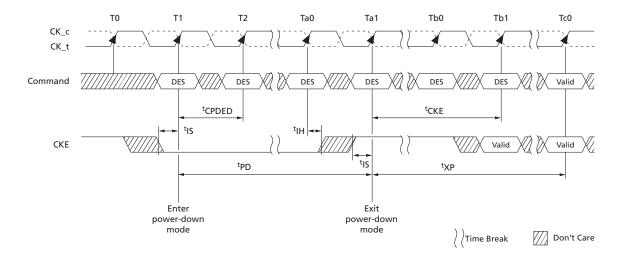




Figure 98: REFRESH Command to Power-Down Entry

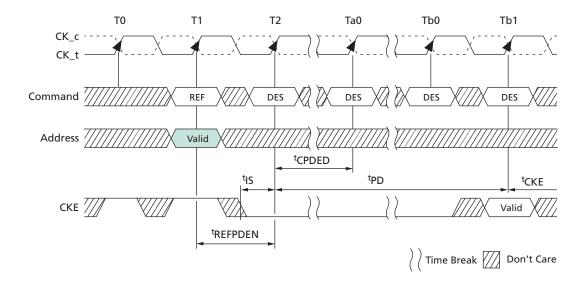


Figure 99: Active Command to Power-Down Entry

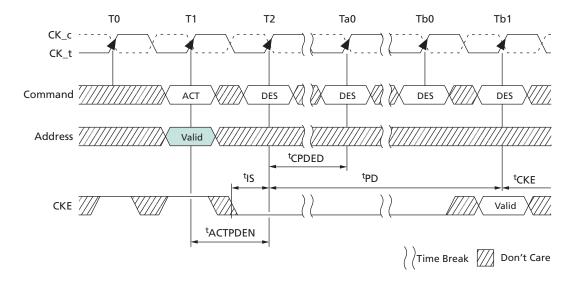




Figure 100: PRECHARGE/PRECHARGE ALL Command to Power-Down Entry

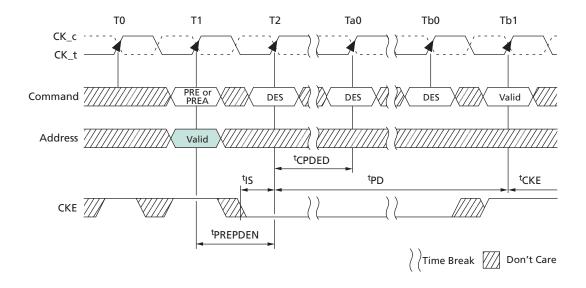
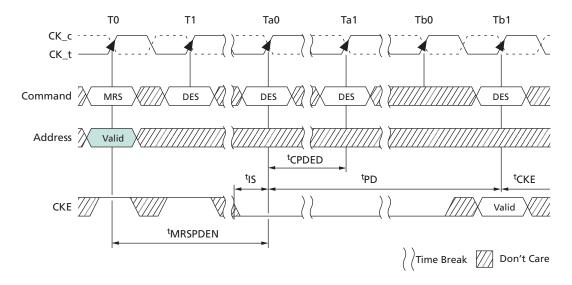


Figure 101: MRS Command to Power-Down Entry

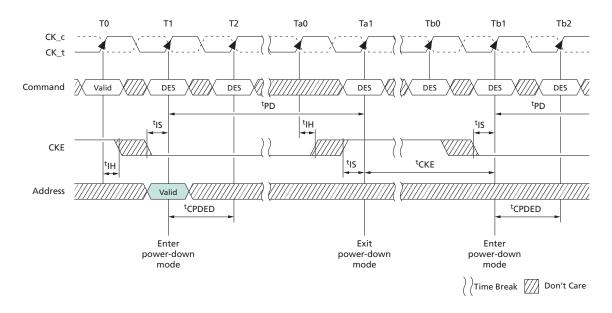


Power-Down Clarifications - Case 1

When CKE is registered LOW for power-down entry, ¹PD (MIN) must be satisfied before CKE can be registered HIGH for power-down exit. The minimum value of parameter ¹PD (MIN) is equal to the minimum value of parameter ¹CKE (MIN) as shown in the Timing Parameters by Speed Bin table. A detailed example of Case 1 follows.



Figure 102: Power-Down Entry/Exit Clarifications - Case 1



Power-Down Entry, Exit Timing with CAL

Command/Address latency is used and additional timing restrictions are required when entering power-down, as noted in the following figures.

Figure 103: Active Power-Down Entry and Exit Timing with CAL

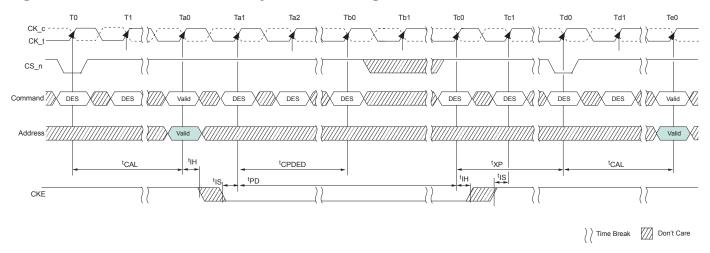
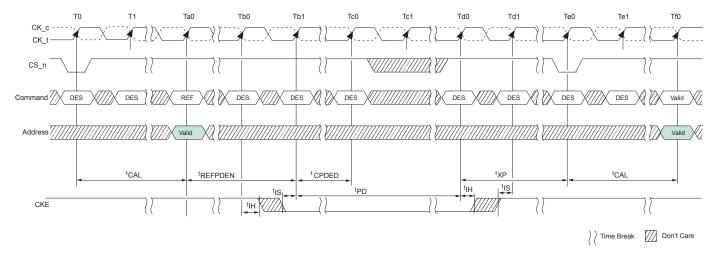




Figure 104: REFRESH Command to Power-Down Entry with CAL





ODT Input Buffer Disable Mode for Power-Down

DRAM does not provide R_{TT_NOM} termination during power-down when ODT input buffer deactivation mode is enabled in MR5 bit A5.

To account for DRAM internal delay on CKE line to disable the ODT buffer and block the sampled output, the host controller must continuously drive ODT to either low or high when entering power down (from ^tDODTLoff+1 prior to CKE low till ^tCPDED after CKE low).

The ODT signal is allowed to float after t CPDEDmin has expired. In this mode, R_{TT_NOM} termination corresponding to sampled ODT at the input when CKE is registered low (and t ANPD before that) may be either R_{TT_NOM} or R_{TT_PARK} . t ANPD is equal to (WL-1) and is counted backwards from PDE.

Figure 105: ODT Power-Down Entry with ODT Buffer Disable Mode

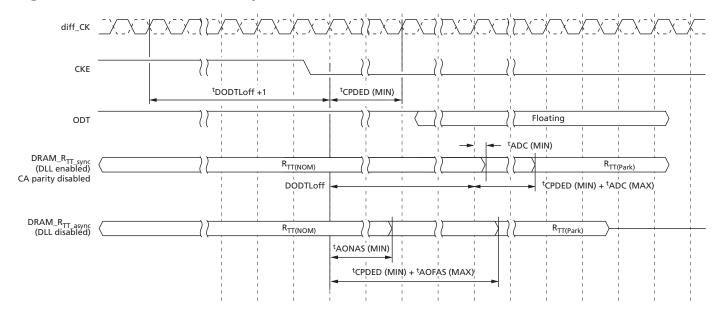
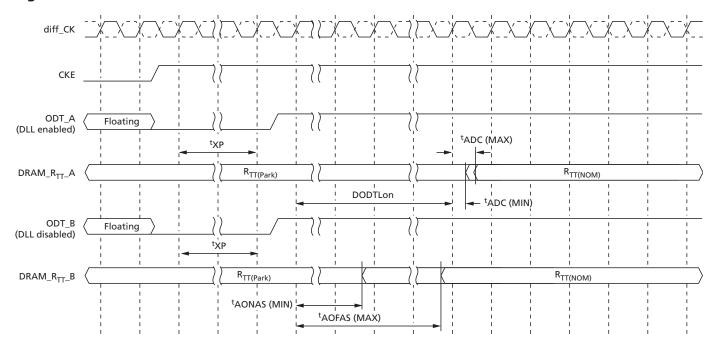




Figure 106: ODT Power-Down Exit with ODT Buffer Disable Mode



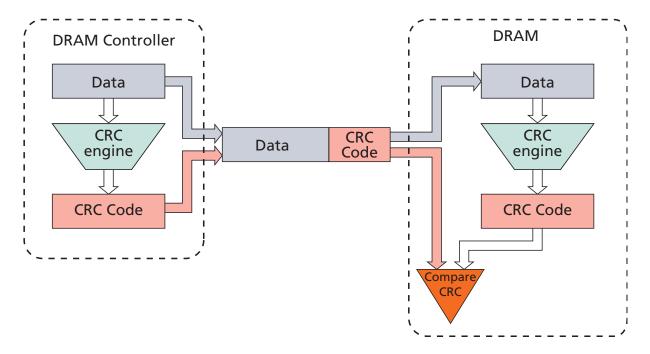


CRC Write Data Feature

CRC Write Data

The CRC write data feature takes the CRC generated data from the DRAM controller and compares it to the internally CRC generated data and determines whether the two match (no CRC error) or do not match (CRC error).

Figure 107: CRC Write Data Operation



WRITE CRC DATA Operation

A DRAM controller generates a CRC checksum using a 72-bit CRC tree and forms the write data frames, as shown in the following CRC data mapping tables for the x4, x8, and x16 configurations. A x4 device has a CRC tree with 32 input data bits used, and the remaining upper 40 bits D[71:32] being 1s. A x8 device has a CRC tree with 64 input data bits used, and the remaining upper 8 bits dependant upon whether DM_n/DBI_n is used (1s are sent when not used). A x16 device has two identical CRC trees each, one for the lower byte and one for the upper byte, with 64 input data bits used by each, and the remaining upper 8 bits on each byte dependant upon whether DM_n/DBI_n is used (1s are sent when not used). For a x8 and x16 DRAMs, the DRAM memory controller must send 1s in transfer 9 location whether or not DM_n/DBI_n is used.

The DRAM checks for an error in a received code word D[71:0] by comparing the received checksum against the computed checksum and reports errors using the ALERT_n signal if there is a mismatch. The DRAM can write data to the DRAM core without waiting for the CRC check for full writes when DM is disabled. If bad data is written to the DRAM core, the DRAM memory controller will try to overwrite the bad data with good data; this means the DRAM controller is responsible for data coherency when DM is disabled. However, in the case where both CRC and DM are enabled via



MRS (that is, persistent mode), the DRAM will not write bad data to the core when a CRC error is detected.

DBI_n and CRC Both Enabled

The DRAM computes the CRC for received written data D[71:0]. Data is not inverted back based on DBI before it is used for computing CRC. The data is inverted back based on DBI before it is written to the DRAM core.

DM n and CRC Both Enabled

When both DM and write CRC are enabled in the DRAM mode register, the DRAM calculates CRC before sending the write data into the array. If there is a CRC error, the DRAM blocks the WRITE operation and discards the data. If a CRC error is encountered from a WRITE with auto precharge (WRA), the DRAM will not block the precharge. The Nonconsecutive WRITE (BL8/BC4-OTF) with 2^tCK Preamble and Write CRC in Same or Different Bank Group and the WRITE (BL8/BC4-OTF/Fixed) with 1^tCK Preamble and Write CRC in Same or Different BankGroup figures in the WRITE Operation section show timing differences when DM is enabled.

DM_n and DBI_n Conflict During Writes with CRC Enabled

Both write DBI_n and DM_n can not be enabled at the same time; read DBI_n and DM_n can be enabled at the same time.

CRC and Write Preamble Restrictions

When write CRC is enabled:

- And 1^tCK WRITE preamble mode is enabled, a ^tCCD_S or ^tCCD_L of 4 clocks is not allowed.
- And 2^tCK WRITE preamble mode is enabled, a ^tCCD_S or ^tCCD_L of 6 clocks is not allowed.

CRC Simultaneous Operation Restrictions

When write CRC is enabled, neither MPR writes nor per-DRAM mode is allowed.

CRC Polynomial

The CRC polynomial used by DDR4 is the ATM-8 HEC, $X^8 + X^2 + X^1 + 1$.

A combinatorial logic block implementation of this 8-bit CRC for 72 bits of data includes 272 two-input XOR gates contained in eight 6-XOR-gate-deep trees.

The CRC polynomial and combinatorial logic used by DDR4 is the same as used on GDDR5.

The error coverage from the DDR4 polynomial used is shown in the following table.

Table 52: CRC Error Detection Coverage

Error Type	Detection Capability				
Random single-bit errors	100%				
Random double-bit errors	100%				



Table 52: CRC Error Detection Coverage (Continued)

Error Type	Detection Capability
Random odd count errors	100%
Random multibit UI vertical column error detection excluding DBI bits	100%

CRC Combinatorial Logic Equations

module CRC8_D72;
// polynomial: (0 1 2 8)
// data width: 72
// convention: the first serial data bit is D[71]
//initial condition all 0 implied
// "^" = XOR
function [7:0]
nextCRC8_D72;
input [71:0] Data;
input [71:0] D;
reg [7:0] CRC;
begin
D = Data;

CRC[0] =

 $\label{eq:def:Delta} D[69]^D[68]^D[67]^D[66]^D[64]^D[63]^D[60]^D[56]^D[54]^D[53]^D[52]^D[50]^D[49]^D[48]^D[45]^D[43]^D[40]^D[39]^D[35]^D[34]^D[31]^D[30]^D[28]^D[23]^D[21]^D[19]^D[18]^D[16]^D[14]^D[12]^D[8]^D[7]^D[6]^D[0];$

CRC[1] =

CRC[2] =

 $\label{eq:def:D0} D[71]^D[69]^D[68]^D[63]^D[62]^D[61]^D[60]^D[58]^D[57]^D[54]^D[50]^D[48]^D[47]^D[46]^D[44]^D[43]^D[42]^D[39]^D[37]^D[34]^D[33]^D[29]^D[28]^D[25]^D[24]^D[22]^D[17]^D[15]^D[13]^D[12]^D[10]^D[8]^D[6]^D[2]^D[1]^D[0];$

CRC[3] =

 $\label{eq:def:D0} D[70]^D[69]^D[64]^D[63]^D[62]^D[61]^D[59]^D[58]^D[55]^D[51]^D[49]^D[48]^D[47]^D[45]^D[44]^D[43]^D[38]^D[35]^D[34]^D[30]^D[29]^D[26]^D[25]^D[23]^D[18]^D[16]^D[14]^D[13]^D[11]^D[9]^D[7]^D[3]^D[2]^D[1];$

CRC[4] =

CRC[5] =

D[71]^D[66]^D[65]^D[64]^D[63]^D[61]^D[60]^D[57]^D[53]^D[51]^D[50]^D[49]^D[47]^D[46]^D[45]^D[42]^D[40]^D[37]^D[36]^D[32]^D[31]^D[28]^D[27]^D[25]^D[20]^D[18]^D[16]^D[15]^D[13]^D[11]^D[9]^D[5]^D[4]^D[3];



CRC[6] =

CRC[7] =

 $\label{eq:def:Delta} D[68]^D[65]^D[65]^D[63]^D[62]^D[59]^D[55]^D[53]^D[52]^D[51]^D[49]^D[48]^D[47]^D[44]^D[42]^D[39]^D[38]^D[34]^D[33]^D[30]^D[29]^D[27]^D[22]^D[20]^D[18]^D[17]^D[15]^D[13]^D[11]^D[6]^D[6]^D[5];$

nextCRC8 D72 = CRC;

Burst Ordering for BL8

DDR4 supports fixed WRITE burst ordering [A2:A1:A0 = 0:0:0] when write CRC is enabled in BL8 (fixed).

CRC Data Bit Mapping

Table 53: CRC Data Mapping for x4 Devices, BL8

Func-	Transfer									
tion	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	CRC4
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	CRC5
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	CRC6
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	CRC7

Table 54: CRC Data Mapping for x8 Devices, BL8

Func-					Tran	sfer				
tion	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	1
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	1
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	1
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	1
DQ4	D32	D33	D34	D35	D36	D37	D38	D39	CRC4	1
DQ5	D40	D41	D42	D43	D44	D45	D46	D47	CRC5	1
DQ6	D48	D49	D50	D51	D52	D53	D54	D55	CRC6	1
DQ7	D56	D57	D58	D59	D60	D61	D62	D63	CRC7	1
DM_n/ DBI_n	D64	D65	D66	D67	D68	D69	D70	D71	1	1

A x16 device is treated as two x8 devices; a x16 device will have two identical CRC trees implemented. CRC[7:0] covers data bits D[71:0], and CRC[15:8] covers data bits D[143:72].



Table 55: CRC Data Mapping for x16 Devices, BL8

Func-					Tran	sfer				
tion	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	1
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	1
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	1
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	1
DQ4	D32	D33	D34	D35	D36	D37	D38	D39	CRC4	1
DQ5	D40	D41	D42	D43	D44	D45	D46	D47	CRC5	1
DQ6	D48	D49	D50	D51	D52	D53	D54	D55	CRC6	1
DQ7	D56	D57	D58	D59	D60	D61	D62	D63	CRC7	1
LDM_n/	D64	D65	D66	D67	D68	D69	D70	D71	1	1
LDBI_n										
DQ8	D72	D73	D74	D75	D76	D77	D78	D79	CRC8	1
DQ9	D80	D81	D82	D83	D84	D85	D86	D87	CRC9	1
DQ10	D88	D89	D90	D91	D92	D93	D94	D95	CRC10	1
DQ11	D96	D97	D98	D99	D100	D101	D102	D103	CRC11	1
DQ12	D104	D105	D106	D107	D108	D109	D110	D111	CRC12	1
DQ13	D112	D113	D114	D115	D116	D117	D118	D119	CRC13	1
DQ14	D120	D121	D122	D123	D124	D125	D126	D127	CRC14	1
DQ15	D128	D129	D130	D131	D132	D133	D134	D135	CRC15	1
UDM_n/ UDBI_n	D136	D137	D138	D139	D140	D141	D142	D143	1	1

CRC Enabled With BC4

If CRC and BC4 are both enabled, then address bit A2 is used to transfer critical data first for BC4 writes.

CRC with BC4 Data Bit Mapping

For a x4 device, the CRC tree inputs are 16 data bits, and the inputs for the remaining bits are 1.

When A2 = 1, data bits D[7:4] are used as inputs for D[3:0], D[15:12] are used as inputs to D[11:8], and so forth, for the CRC tree.

Table 56: CRC Data Mapping for x4 Devices, BC4

	Transfer										
Function	0	1	2	3	4	5	6	7	8	9	
	A2 = 0										
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	CRC4	
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	CRC5	
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	CRC6	



Table 56: CRC Data Mapping for x4 Devices, BC4 (Continued)

	Transfer										
Function	0	1	2	3	4	5	6	7	8	9	
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	CRC7	
	A2 = 1										
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	CRC4	
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	CRC5	
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	CRC6	
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	CRC7	

For a x8 device, the CRC tree inputs are 36 data bits.

When A2 = 0, the input bits D[67:64]) are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[67:64]) are 1.

When A2 = 1, data bits D[7:4] are used as inputs for D[3:0], D[15:12] are used as inputs to D[11:8], and so forth, for the CRC tree. The input bits D[71:68]) are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[71:68]) are 1.

Table 57: CRC Data Mapping for x8 Devices, BC4

	Transfer											
Function	0	1	2	3	4	5	6	7	8	9		
A2 = 0												
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	1		
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	1		
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	1		
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	1		
DQ4	D32	D33	D34	D35	1	1	1	1	CRC4	1		
DQ5	D40	D41	D42	D43	1	1	1	1	CRC5	1		
DQ6	D48	D49	D50	D51	1	1	1	1	CRC6	1		
DQ7	D56	D57	D58	D59	1	1	1	1	CRC7	1		
DM_n/DBI_n	D64	D65	D66	D67	1	1	1	1	1	1		
				А	2 = 1							
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	1		
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	1		
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	1		
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	1		
DQ4	D36	D37	D38	D39	1	1	1	1	CRC4	1		
DQ5	D44	D45	D46	D47	1	1	1	1	CRC5	1		
DQ6	D52	D53	D54	D55	1	1	1	1	CRC6	1		
DQ7	D60	D61	D62	D63	1	1	1	1	CRC7	1		
DM_n/DBI_n	D68	D69	D70	D71	1	1	1	1	1	1		

There are two identical CRC trees for x16 devices, each have CRC tree inputs of 36 bits.



When A2 = 0, input bits D[67:64] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[67:64] are 1s. The input bits D[139:136] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[139:136] are 1s.

When A2 = 1, data bits D[7:4] are used as inputs for D[3:0], D[15:12] are used as inputs for D[11:8], and so forth, for the CRC tree. Input bits D[71:68] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[71:68] are 1s. The input bits D[143:140] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[143:140] are 1s.

Table 58: CRC Data Mapping for x16 Devices, BC4

	Transfer											
Function	0	1	2	3	4	5	6	7	8	9		
				А	2 = 0							
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	1		
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	1		
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	1		
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	1		
DQ4	D32	D33	D34	D35	1	1	1	1	CRC4	1		
DQ5	D40	D41	D42	D43	1	1	1	1	CRC5	1		
DQ6	D48	D49	D50	D51	1	1	1	1	CRC6	1		
DQ7	D56	D57	D58	D59	1	1	1	1	CRC7	1		
LDM_n/LDBI_n	D64	D65	D66	D67	1	1	1	1	1	1		
DQ8	D72	D73	D74	D75	1	1	1	1	CRC8	1		
DQ9	D80	D81	D82	D83	1	1	1	1	CRC9	1		
DQ10	D88	D89	D90	D91	1	1	1	1	CRC10	1		
DQ11	D96	D97	D98	D99	1	1	1	1	CRC11	1		
DQ12	D104	D105	D106	D107	1	1	1	1	CRC12	1		
DQ13	D112	D113	D114	D115	1	1	1	1	CRC13	1		
DQ14	D120	D121	D122	D123	1	1	1	1	CRC14	1		
DQ15	D128	D129	D130	D131	1	1	1	1	CRC15	1		
UDM_n/UDBI_n	D136	D137	D138	D139	1	1	1	1	1	1		
				А	2 = 1	•						
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	1		
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	1		
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	1		
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	1		
DQ4	D36	D37	D38	D39	1	1	1	1	CRC4	1		
DQ5	D44	D45	D46	D47	1	1	1	1	CRC5	1		
DQ6	D52	D53	D54	D55	1	1	1	1	CRC6	1		
DQ7	D60	D61	D62	D63	1	1	1	1	CRC7	1		
LDM_n/LDBI_n	D68	D69	D70	D71	1	1	1	1	1	1		



Table 58: CRC Data Mapping for x16 Devices, BC4 (Continued)

	Transfer									
Function	0	1	2	3	4	5	6	7	8	9
DQ8	D76	D77	D78	D79	1	1	1	1	CRC8	1
DQ9	D84	D85	D86	D87	1	1	1	1	CRC9	1
DQ10	D92	D93	D94	D95	1	1	1	1	CRC10	1
DQ11	D100	D101	D102	D103	1	1	1	1	CRC11	1
DQ12	D108	D109	D110	D111	1	1	1	1	CRC12	1
DQ13	D116	D117	D118	D119	1	1	1	1	CRC13	1
DQ14	D124	D125	D126	D127	1	1	1	1	CRC14	1
DQ15	D132	D133	D134	D135	1	1	1	1	CRC15	1
UDM_n/UDBI_n	D140	D141	D142	D143	1	1	1	1	1	1

CRC Equations for x8 Device in BC4 Mode with A2 = 0 and A2 = 1

The following example is of a CRC tree when x8 is used in BC4 mode (x4 and x16 CRC trees have similar differences).

CRC[0], A2=0 =

 $1^1 D[67] D[66] D[64] 1^1 D[56] 1^1 D[50] D[49] D[48] 1^1 D[43] D[40] 1^1 D[35] D[34] 1^1 1^1 D[10] D[18] D[16] 1^1 D[8] 1^1 D[9];$

CRC[0], A2=1 =

 $1^1 D[71] D[70] D[68]^1^1 D[60]^1^1^1 D[54] D[53]^D[52]^1^D[47]^D[44]^1^D[39]^D[38]^1^1^1^1^1^D[23]^D[22]^D[20]^1^1^D[12]^1^1^D[4] ;$

CRC[1], A2=0 =

 $1^{D}[66]^{D}[65]^{1}^{1}^{1}^{D}[57]^{D}[56]^{1}^{1}^{D}[51]^{D}[48]^{1}^{1}^{1}^{D}[43]^{D}[41]^{1}^{1}^{D}[34]^{D}[32]^{1}^{1}^{D}[24]^{1}^{1}^{1}^{1}^{D}[18]^{D}[17]^{D}[16]^{1}^{1}^{1}^{1}^{D}[9]^{1}^{D}[0];$

CRC[1], A2=1=

1^D[70]^D[69]^1^1^1^D[61]^D[60]^1^1^D[55]^D[52]^1^1^1^D[47]^D[45]^1^1^D[38]^D[36]^1^1^1^D[28]^1^1^1^D[22]^D[21]^D[20]^1^1^1^1^D[13]^1^D[5]^D[4];

CRC[2], A2=0 =

1^1^1^1^1^1^1^D[58]^D[57]^1^D[50]^D[48]^1^1^1^D[43]^D[42]^1^1^D[34]^D[33]^1 ^1^D[25]^D[24]^1^D[17]^1^1^1^D[10]^D[8] ^1^D[2]^D[1]^D[0];

CRC[2], A2=1 =

1^1^1^1^1^1^1^D[62]^D[61]^1^D[54]^D[52]^1^1^1^D[47]^D[46]^1^1^D[38]^D[37]^1 ^1^D[29]^D[28]^1^D[21]^1^1^1^D[14]^D12]^1^D[6]^D[5]^D[4];

CRC[3], A2=0 =

 $1^1 D[64]^1^1^1D[59]^D[58]^1^D[51]^D[49]^D[48]^1^1^1^D[43]^D[40]^1^D[35]^D[34]^1^1^D[26]^D[25]^1^D[18]^D[16]^1^1^D[11]^D[9]^1^D[3]^D[2]^D[1];$

CRC[3], A2=1 =

 $1^1 D[68]^1^1^1D[63]^D[62]^1^D[55]^D[53]^D[52]^1^1^1^D[47]^D[44]^1^D[39]^D[38]^1^1^D[30]^D[29]^1^D[22]^D[20]^1^1^D[15]^D[13]^1^D[7]^D[6]^D[5];$





CRC[4], A2=0 =

 $1^1 D[65]^D[64]^1^1^1D[59]^D[56]^1^D[50]^D[49]^D[48]^1^1^1^D[41]^1^1^D[35]^1^1^D[27]^D[26]^D[24]^D[19]^D[17]^1^1^1^D[10]^D[8]^1^D[3]^D[2];$

CRC[4], A2=1 =

 $1^{1}D[69]^{D}[68]^{1}^{1}D[63]^{D}[60]^{1}D[54]^{D}[53]^{D}[52]^{1}^{1}^{1}D[45]^{1}^{D}[39]^{1}^{1}D[30]^{D}[28]^{D}[23]^{D}[21]^{1}^{1}^{1}D[14]^{D}[12]^{1}^{D}[6];$

CRC[5], A2=0 =

 $1^{D[66]}^{D[65]}^{D[64]}^{1^{1}}^{1^{0}}^{D[57]}^{1^{0}}^{D[51]}^{D[50]}^{D[49]}^{1^{1}}^{1^{0}}^{D[42]}^{D[40]}^{1^{1}}^{D[32]}^{1^{1}}^{D[27]}^{D[25]}^{1^{0}}^{D[18]}^{D[16]}^{1^{1}}^{D[11]}^{D[9]}^{1^{1}}^{D[9]}^{D[32]}^{D[40]}^{D[4$

CRC[5], A2=1 =

 $1^{D}[70]^{D}[69]^{D}[68]^{1}^{1}^{1}^{D}[61]^{1}^{D}[55]^{D}[54]^{D}[53]^{1}^{1}^{1}^{D}[46]^{D}[44]^{1}^{D}[56]^{1}^{D}[31]^{D}[29]^{1}^{D}[22]^{D}[20]^{1}^{D}[15]^{D}[13]^{1}^{D}[7];$

CRC[6], A2=0 =

 $D[67]^{D}[66]^{D}[65]^{D}[64]^{1}^{1}^{D}[58]^{1}^{1}^{D}[51]^{D}[50]^{D}[48]^{1}^{1}^{D}[43]^{D}[41]^{1}^{1}^{D}[33]^{D}[32]^{1}^{1}^{D}[26]^{1}^{D}[19]^{D}[17]^{D}[16]^{1}^{1}^{D}[10]^{1}^{1};$

CRC[6], A2=1 =

 $D[71]^{D}[70]^{D}[69]^{D}[68]^{1}^{1}^{D}[62]^{1}^{1}^{D}[55]^{D}[54]^{D}[52]^{1}^{1}^{D}[47]^{D}[45]^{1}^{1}^{D}[37]^{D}[36]^{1}^{1}^{D}[30]^{1}^{D}[23]^{D}[21]^{D}[20]^{1}^{1}^{D}[41]^{1}^{1};$

CRC[7], A2=0 =

 $1^{D}[67]^{D}[66]^{D}[65]^{1}^{1}^{D}[59]^{1}^{1}^{1}^{D}[51]^{D}[49]^{D}[48]^{1}^{1}^{D}[42]^{1}^{1}^{D}[34]^{D}[33]^{1}^{D}[27]^{1}^{1}^{D}[18]^{D}[17]^{1}^{D}[11]^{1}^{1};$

CRC[7], A2=1 =

 $1^{D}[71]^{D}[70]^{D}[69]^{1}^{1}^{D}[63]^{1}^{1}^{D}[55]^{D}[53]^{D}[52]^{1}^{1}^{D}[46]^{1}^{D}[38]^{D}[57]^{1}^{D}[31]^{1}^{D}[22]^{D}[21]^{1}^{1}^{D}[15]^{1}^{1};$

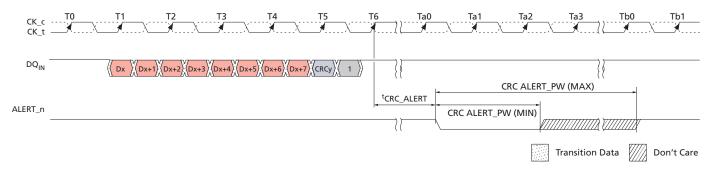
CRC Error Handling

The CRC error mechanism shares the same ALERT_n signal as CA parity for reporting write errors to the DRAM. The controller has two ways to distinguish between CRC errors and CA parity errors: 1) Read DRAM mode/MPR registers, and 2) Measure time ALERT_n is LOW. To speed up recovery for CRC errors, CRC errors are only sent back as a "short" pulse; the maximum pulse width is roughly ten clocks (unlike CA parity where ALERT_n is LOW longer than 45 clocks). The ALERT_n LOW could be longer than the maximum limit at the controller if there are multiple CRC errors as the ALERT_n signals are connected by a daisy chain bus. The latency to ALERT_n signal is defined as t CRC_ALERT in the following figure.

The DRAM will set the error status bit located at MR5[3] to a 1 upon detecting a CRC error, which will subsequently set the CRC error status flag in the MPR error log HIGH (MPR Page1, MPR3[7]). The CRC error status bit (and CRC error status flag) remains set at 1 until the DRAM controller clears the CRC error status bit using an MRS command to set MR5[3] to a 0. The DRAM controller, upon seeing an error as a pulse width, will retry the write transactions. The controller should consider the worst-case delay for ALERT_n (during initialization) and backup the transactions accordingly. The DRAM controller may also be made more intelligent and correlate the write CRC error to a specific rank or a transaction.



Figure 108: CRC Error Reporting



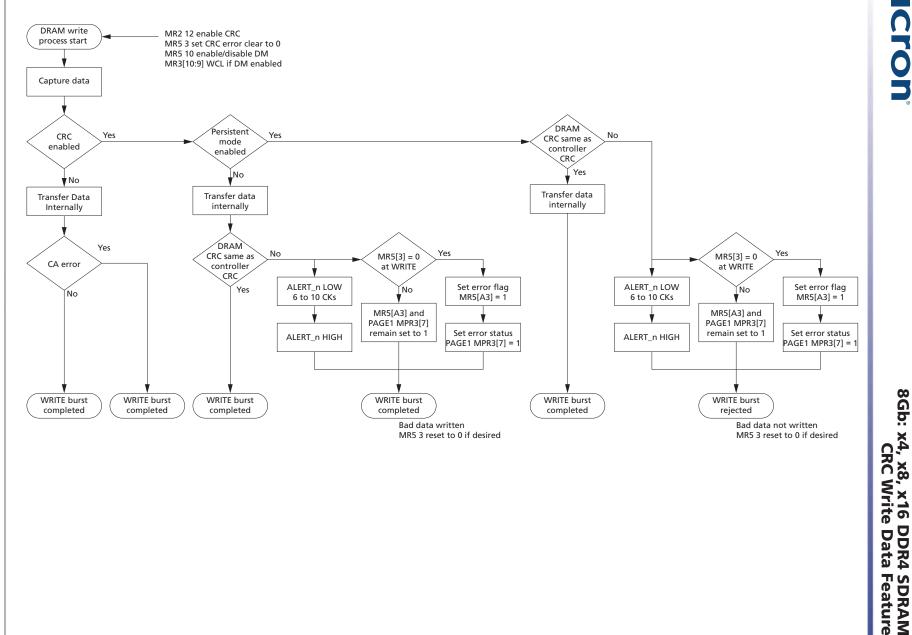
Notes

- 1. D[71:1] CRC computed by DRAM did not match CRC[7:0] at T5 and started error generating process at T6.
- 2. CRC ALERT_PW is specified from the point where the DRAM starts to drive the signal LOW to the point where the DRAM driver releases and the controller starts to pull the signal up.
- 3. Timing diagram applies to x4, x8, and x16 devices.

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CRC Write Data Flow Diagram

Figure 109: CA Parity Flow Diagram





Data Bus Inversion

The DATA BUS INVERSION (DBI) function is supported only for x8 and x16 configurations (it is not supported on x4 devices). DBI opportunistically inverts data bits, and in conjunction with the DBI_n I/O, less than half of the DQs will switch LOW for a given DQS strobe edge. The DBI function shares a common pin with the DATA MASK (DM) and TDQS functions. The DBI function applies to either or both READ and WRITE operations: Write DBI cannot be enabled at the same time the DM function is enabled, and DBI is not allowed during MPR READ operation. Valid configurations for TDQS, DM, and DBI functions are shown below.

Table 59: DBI vs. DM vs. TDQS Function Matrix

Read DBI	Write DBI	Data Mask (DM)	TDQS (x8 only)	
Enabled (or Disabled) MR5[12]=1 (or	Disabled MR5[11] = 0	Disabled MR5[10] = 0	Disabled MR1[11] = 0	
MR5[12] = 0)	Enabled MR5[11] = 1	Disabled MR5[10] = 0	Disabled MR1[11] = 0	
	Disabled MR5[11] = 0	Enabled MR5[10] = 1	Disabled MR1[11] = 0	
Disabled MR5[12] = 0	Disabled MR5[11] = 0	Disabled MR5[10] = 0	Enabled MR1[11] = 1	

DBI During a WRITE Operation

If DBI_n is sampled LOW on a given byte lane during a WRITE operation, the DRAM inverts write data received on the DQ inputs prior to writing the internal memory array. If DBI_n is sampled HIGH on a given byte lane, the DRAM leaves the data received on the DQ inputs noninverted. The write DQ frame format is shown below for x8 and x16 configurations (the x4 configuration does not support the DBI function).

Table 60: DBI Write, DQ Frame Format (x8)

	Transfer									
Function	0	1	2	3	4	5	6	7		
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7		
DM_n or DBI_n	DM0 or DBI0	DM1 or DBI1	DM2 or DBI2	DM3 or DBI3	DM4 or DBI4	DM5 or DBI5	DM6 or DBI6	DM7 or DBI7		

Table 61: DBI Write, DQ Frame Format (x16)

	Transfer, Lower (L) and Upper(U)									
Function	0	1	2	3	4	5	6	7		
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7		
LDM_n or	LDM0 or	LDM1 or	LDM2 or	LDM3 or	LDM4 or	LDM5 or	LDM6 or	LDM7 or		
LDBI_n	LDBI0	LDBI1	LDBI2	LDBI3	LDBI4	LDBI5	LDBI6	LDBI7		
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7		



Table 61: DBI Write, DQ Frame Format (x16) (Continued)

		Transfer, Lower (L) and Upper(U)						
Function	0 1 2 3 4 5 6							7
UDM_n or UDBI_n	UDM0 or UDBI0	UDM1 or UDBI1	UDM2 or UDBI2	UDM3 or UDBI3	UDM4 or UDBI4	UDM5 or UDBI5	UDM6 or UDBI6	UDM7 or UDBI7

DBI During a READ Operation

If the number of 0 data bits within a given byte lane is greater than four during a READ operation, the DRAM inverts read data on its DQ outputs and drives the DBI_n pin LOW; otherwise, the DRAM does not invert the read data and drives the DBI_n pin HIGH. The read DQ frame format is shown below for x8 and x16 configurations (the x4 configuration does not support the DBI function).

Table 62: DBI Read, DQ Frame Format (x8)

		Transfer Byte						
Function	0	1	2	3	4	5	6	7
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
DBI_n	DBI0	DBI1	DBI2	DBI3	DBI4	DBI5	DBI6	DBI7

Table 63: DBI Read, DQ Frame Format (x16)

	Transfer Byte, Lower (L) and Upper(U)							
Function	0	1	2	3	4	5	6	7
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
LDBI_n	LDBI0	LDBI1	LDBI2	LDBI3	LDBI4	LDBI5	LDBI6	LDBI7
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
UDBI_n	UDBI0	UDBI1	UDBI2	UDBI3	UDBI4	UDBI5	UDBI6	UDBI7



Data Mask

The DATA MASK (DM) function, also described as PARTIAL WRITE, is supported only for x8 and x16 configurations (it is not supported on x4 devices). The DM function shares a common pin with the DBI_n and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the WRITE DBI function is enabled. The valid configurations for the TDQS, DM, and DBI functions are shown here.

Table 64: DM vs. TDQS vs. DBI Function Matrix

Data Mask (DM)	TDQS (x8 only)	Write DBI	Read DBI
Enabled MR5[10] = 1	Disabled MR1[11] = 0	Disabled MR5[11] = 0	Enabled or Disabled MR5[12] = 1 or
Disabled MR5[10] = 0	Enabled MR1[11] = 1	Disabled MR5[11] = 0	MR5[12] = 0 Disabled MR5[12] = 0
WINS[10] = 0	Disabled MR1[11] = 0	Enabled MR5[11] = 1	Enabled or Disabled MR5[12] = 1 or
	Disabled	Disabled	MR5[12] = 0 Enabled (or Disabled)
	MR1[11] = 0	MR5[11] = 0	MR5[12] = 1 (or MR5[12] = 0)

When enabled, the DM function applies during a WRITE operation. If DM_n is sampled LOW on a given byte lane, the DRAM masks the write data received on the DQ inputs. If DM_n is sampled HIGH on a given byte lane, the DRAM does not mask the data and writes this data into the DRAM core. The DQ frame format for x8 and x16 configurations is shown below. If both CRC write and DM are enabled (via MRS), the CRC will be checked and valid prior to the DRAM writing data into the DRAM core. If a CRC error occurs while the DM feature is enabled, CRC write persistent mode will be enabled and data will not be written into the DRAM core. In the case of CRC write enabled and DM disabled (via MRS), that is, CRC write nonpersistent mode, data is written to the DRAM core even if a CRC error occurs.

Table 65: Data Mask, DQ Frame Format (x8)

	Transfer							
Function	0	1	2	3	4	5	6	7
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
DM_n or	DM0 or	DM1 or	DM2 or	DM3 or	DM4 or	DM5 or	DM6 or	DM7 or
DBI_n	DBI0	DBI1	DBI2	DBI3	DBI4	DBI5	DBI6	DBI7

Table 66: Data Mask, DQ Frame Format (x16)

		Transfer, Lower (L) and Upper (U)						
Function	0 1 2 3 4 5 6 7						7	
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7



Table 66: Data Mask, DQ Frame Format (x16) (Continued)

		Transfer, Lower (L) and Upper (U)						
Function	0	1	2	3	4	5	6	7
LDM_n or LDBI_n	LDM0 or LDBI0	LDM1 or LDBI1	LDM2 or LDBI2	LDM3 or LDBI3	LDM4 or LDBI4	LDM5 or LDBI5	LDM6 or LDBI6	LDM7 or LDBI7
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
UDM_n or UDBI_n	UDM0 or UDBI0	UDM1 or UDBI1	UDM2 or UDBI2	UDM3 or UDBI3	UDM4 or UDBI4	UDM5 or UDBI5	UDM6 or UDBI6	UDM7 or UDBI7



Programmable Preamble Modes and DQS Postambles

The device supports programmable WRITE and READ preamble modes, either the normal 1^tCK preamble mode or special 2^tCK preamble mode. The 2^tCK preamble mode places special timing constraints on many operational features as well as being supported for data rates of DDR4-2400 and faster. The WRITE preamble 1^tCK or 2^tCK mode can be selected independently from READ preamble 1^tCK or 2^tCK mode.

READ preamble training is also supported; this mode can be used by the DRAM controller to train or "read level" the DQS receivers.

There are ^tCCD restrictions under some circumstances:

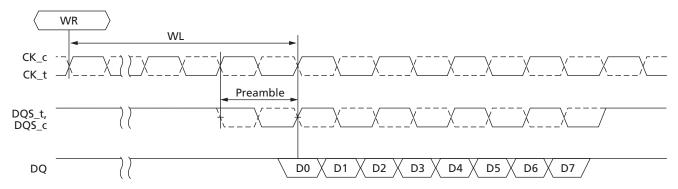
- When 2^tCK READ preamble mode is enabled, a ^tCCD_S or ^tCCD_L of 5 clocks is not allowed.
- When 2^tCK WRITE preamble mode is enabled and write CRC is *not* enabled, a ^tCCD_S or ^tCCD_L of 5 clocks is not allowed.
- When 2^tCK WRITE preamble mode is enabled and write CRC is enabled, a ^tCCD_S or ^tCCD_L of 6 clocks is not allowed.

WRITE Preamble Mode

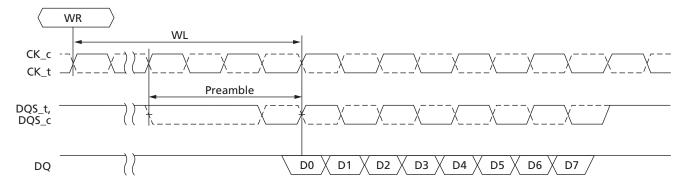
MR4[12] = 0 selects 1^tCK WRITE preamble mode while MR4[12] = 1 selects 2^tCK WRITE preamble mode. Examples are shown in the figures below.

Figure 110: 1^tCK vs. 2^tCK WRITE Preamble Mode

1tCK Mode



2^tCK Mode



8Gb: x4, x8, x16 DDR4 SDRAM Programmable Preamble Modes and DQS Postambles

CWL has special considerations when in the 2^tCK WRITE preamble mode. The CWL value selected in MR2[5:3], as seen in table below, requires at least one additional clock when the primary CWL value and 2^tCK WRITE preamble mode are used; no additional clocks are required when the alternate CWL value and 2^tCK WRITE preamble mode are used.

Table 67: CWL Selection

	CWL - Prir	nary Choice	CWL - Alter	nate Choice	
Speed Bin	1 ^t CK Preamble	2 ^t CK Preamble	1 ^t CK Preamble	2 ^t CK Preamble	
DDR4-1600	9	N/A	11	N/A	
DDR4-1866	10	N/A	12	N/A	
DDR4-2133	11	N/A	14	N/A	
DDR4-2400	12	14	16	16	
DDR4-2666	14	16	18	18	
DDR4-2933	16	18	20	20	
DDR4-3200	16	18	20	20	

Note: 1. CWL programmable requirement for MR2[5:3].

When operating in 2^tCK WRITE preamble mode, ^tWTR (command based) and ^tWR (MR0[11:9]) must be programmed to a value 1 clock greater than the ^tWTR and ^tWR setting normally required for the applicable speed bin to be JEDEC compliant; however, Micron's DDR4 DRAMs do not require these additional ^tWTR and ^tWR clocks. The CAS_n-to-CAS_n command delay to either a different bank group (^tCCD_S) or the same bank group (^tCCD_L) have minimum timing requirements that must be satisfied between WRITE commands and are stated in the Timing Parameters by Speed Bin tables.

Figure 111: 1^tCK vs. 2^tCK WRITE Preamble Mode, ^tCCD = 4

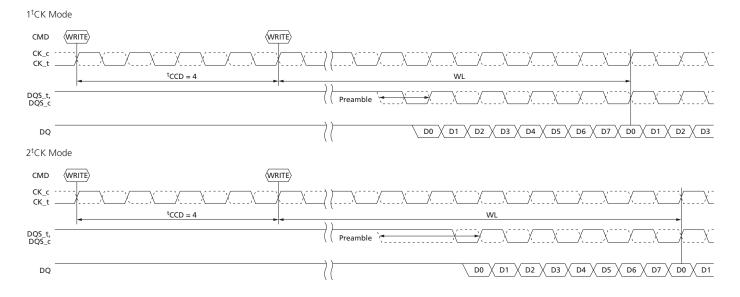
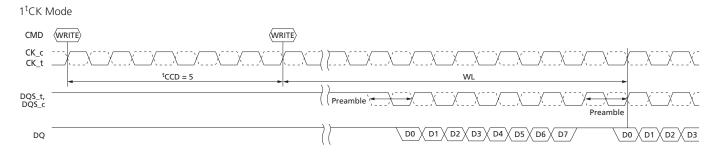




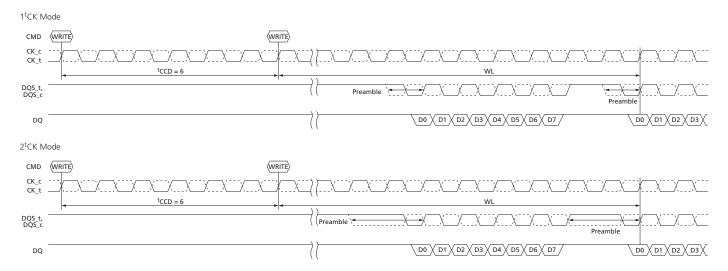
Figure 112: 1^tCK vs. 2^tCK WRITE Preamble Mode, ^tCCD = 5



 $2^{t}CK$ Mode: ${}^{t}CCD = 5$ is not allowed in $2^{t}CK$ mode.

Note: 1. ^tCCD_S and ^tCCD_L = 5 ^tCKs is not allowed when in 2^tCK WRITE preamble mode.

Figure 113: 1^tCK vs. 2 ^tCK WRITE Preamble Mode, ^tCCD = 6



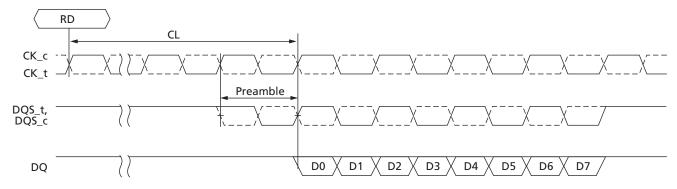


READ Preamble Mode

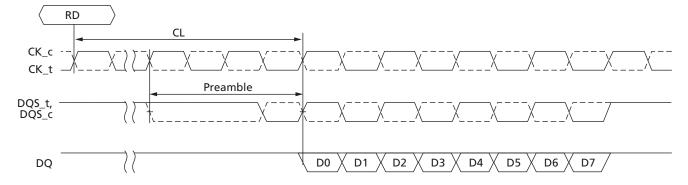
MR4[11] = 0 selects 1^tCK READ preamble mode and MR4[11] = 1 selects 2^tCK READ preamble mode. Examples are shown in the following figure.

Figure 114: 1^tCK vs. 2^tCK READ Preamble Mode

1tCK Mode



2^tCK Mode

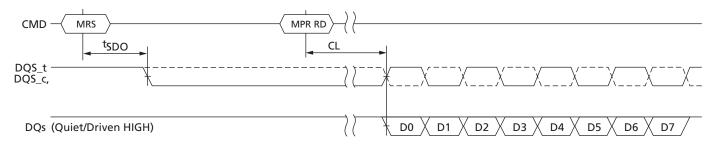


READ Preamble Training

DDR4 supports READ preamble training via MPR reads; that is, READ preamble training is allowed only when the DRAM is in the MPR access mode. The READ preamble training mode can be used by the DRAM controller to train or "read level" its DQS receivers. READ preamble training is entered via an MRS command (MR4[10] = 1 is enabled and MR4[10] = 0 is disabled). After the MRS command is issued to enable READ preamble training, the DRAM DQS signals are driven to a valid level by the time ^tSDO is satisfied. During this time, the data bus DQ signals are held quiet, that is, driven HIGH. The DQS_t signal remains driven LOW and the DQS_c signal remains driven HIGH until an MPR Page0 READ command is issued (MPR0 through MPR3 determine which pattern is used), and when CAS latency (CL) has expired, the DQS signals will toggle normally depending on the burst length setting. To exit READ preamble training mode, an MRS command must be issued, MR4[10] = 0.



Figure 115: READ Preamble Training

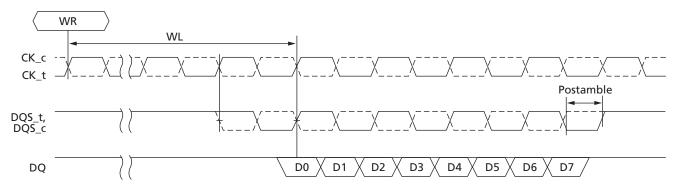


WRITE Postamble

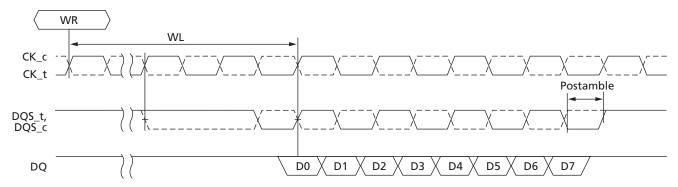
Whether the 1^tCK or 2^tCK WRITE preamble mode is selected, the WRITE postamble remains the same at ½^tCK.

Figure 116: WRITE Postamble

1^tCK Mode



2^tCK Mode



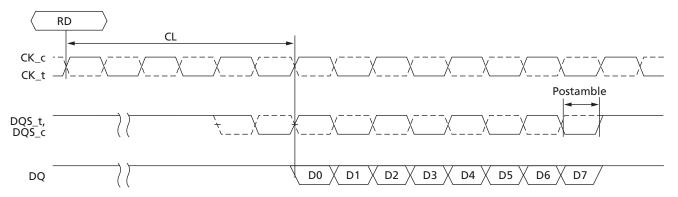
READ Postamble

Whether the 1 t CK or 2 t CK READ preamble mode is selected, the READ postamble remains the same at $\frac{1}{2}$ t CK.

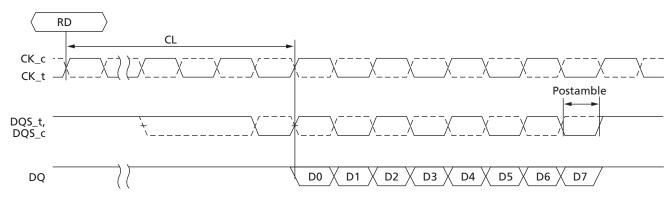


Figure 117: READ Postamble

1^tCK Mode



2^tCK Mode

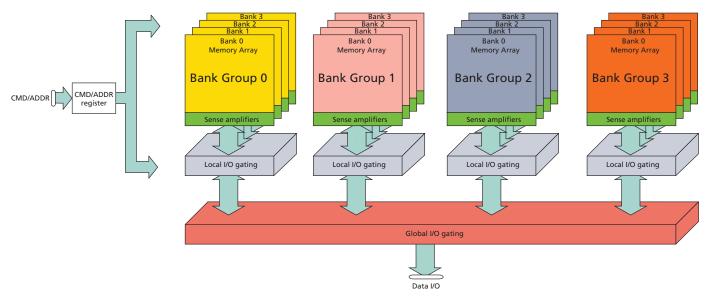




Bank Access Operation

DDR4 supports bank grouping: x4/x8 DRAMs have four bank groups (BG[1:0]), and each bank group is comprised of four subbanks (BA[1:0]); x16 DRAMs have two bank groups (BG[0]), and each bank group is comprised of four subbanks. Bank accesses to different banks' groups require less time delay between accesses than bank accesses to within the same bank's group. Bank accesses to different bank groups require ^tCCD_S (or short) delay between commands while bank accesses within the same bank group require ^tCCD_L (or long) delay between commands.

Figure 118: Bank Group x4/x8 Block Diagram



Notes: 1. Bank accesses to different bank groups require tCCD_S.

2. Bank accesses within the same bank group require ^tCCD_L.

Table 68: DDR4 Bank Group Timing Examples

Parameter	DDR4-1600	DDR4-2133	DDR4-2400	
^t CCD_S	4nCK	4nCK	4nCK	
^t CCD_L	4nCK or 6.25ns	4nCK or 5.355ns	4nCK or 5ns	
^t RRD_S (½K)	4nCK or 5ns	4 <i>n</i> CK or 3.7ns	4 <i>n</i> CK or 3.3ns	
^t RRD_L (½K)	4nCK or 6ns	4 <i>n</i> CK or 5.3ns	4nCK or 4.9ns	
tRRD_S (1K)	4nCK or 5ns	4 <i>n</i> CK or 3.7ns	4 <i>n</i> CK or 3.3ns	
^t RRD_L (1K)	4nCK or 6ns	4 <i>n</i> CK or 5.3ns	4 <i>n</i> CK or 4.9ns	
^t RRD_S (2K)	4nCK or 6ns	4 <i>n</i> CK or 5.3ns	4 <i>n</i> CK or 5.3ns	
tRRD_L (2K)	4nCK or 7.5ns	4 <i>n</i> CK or 6.4ns	4 <i>n</i> CK or 6.4ns	



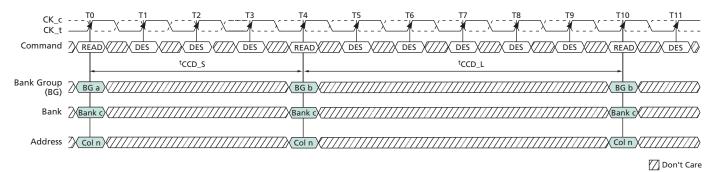
Table 68: DDR4 Bank Group Timing Examples (Continued)

	Parameter	DDR4-1600	DDR4-2133	DDR4-2400
	tWTR_S	2 <i>n</i> CK or 2.5ns	2 <i>n</i> CK or 2.5ns	2nCK or 2.5ns
ĺ	tWTR_L	4nCK or 7.5ns	4nCK or 7.5ns	4 <i>n</i> CK or 7.5ns

Notes:

- 1. Refer to Timing Tables for actual specification values, these values are shown for reference only and are not verified for accuracy.
- 2. Timings with both *n*CK and ns require both to be satisfied; that is, the larger time of the two cases must be satisfied.

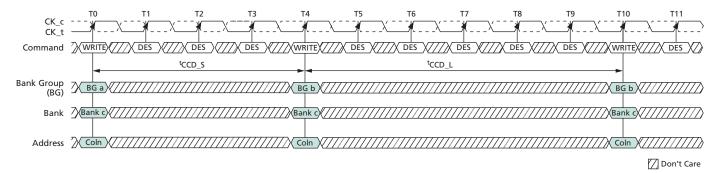
Figure 119: READ Burst tCCD_S and tCCD_L Examples



Notes:

- 1. ^tCCD_S; CAS_n-to-CAS_n delay (short). Applies to consecutive CAS_n to different bank groups (T0 to T4).
- 2. ^tCCD_L; CAS_n-to-CAS_n delay (long). Applies to consecutive CAS_n to the same bank group (T4 to T10).

Figure 120: Write Burst ^tCCD S and ^tCCD L Examples

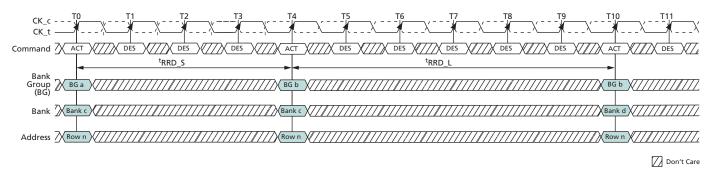


Notes: 1. ^tCCD_S; CAS_n-to-CAS_n delay (short). Applies to consecutive CAS_n to different bank groups (T0 to T4).

2. ^tCCD_L; CAS_n-to-CAS_n delay (long). Applies to consecutive CAS_n to the same bank group (T4 to T10).

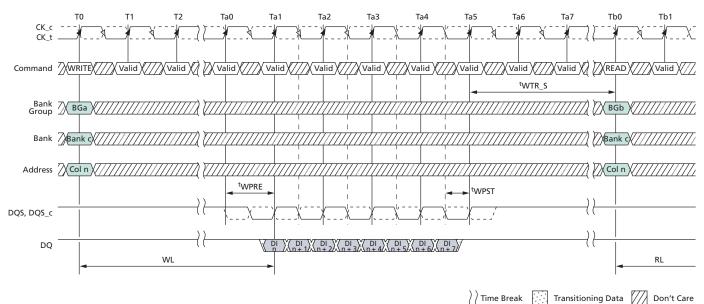


Figure 121: ^tRRD Timing



- Notes: 1. ^tRRD_S; ACTIVATE-to-ACTIVATE command period (short); applies to consecutive ACTI-VATE commands to different bank groups (T0 and T4).
 - tRRD_L; ACTIVATE-to-ACTIVATE command period (long); applies to consecutive ACTI-VATE commands to the different banks in the same bank group (T4 and T10).

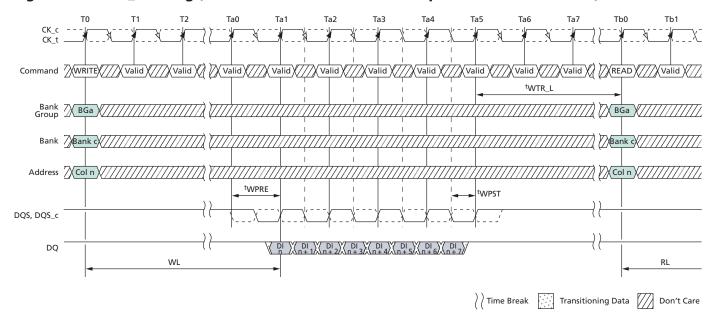
Figure 122: tWTR_S Timing (WRITE-to-READ, Different Bank Group, CRC and DM Disabled)



Note: 1. tWTR_S: delay from start of internal write transaction to internal READ command to a different bank group.



Figure 123: tWTR_L Timing (WRITE-to-READ, Same Bank Group, CRC and DM Disabled)



Note: 1. tWTR_L: delay from start of internal write transaction to internal READ command to the same bank group.



READ Operation

Read Timing Definitions

The read timings shown below are applicable in normal operation mode, that is, when the DLL is enabled and locked.

Note: ^tDQSQ = both rising/falling edges of DQS; no ^tAC defined.

Rising data strobe edge parameters:

- ^tDQSCK (MIN)/(MAX) describes the allowed range for a rising data strobe edge relative to CK.
- ^tDQSCK is the actual position of a rising strobe edge relative to CK.
- tQSH describes the DQS differential output HIGH time.
- ^tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tQSL describes the DQS differential output LOW time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.



Figure 124: Read Timing Definition

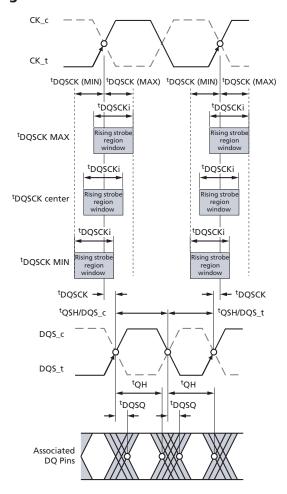


Table 69: Read-to-Write and Write-to-Read Command Intervals

Access Type	Bank Group	Timing Parameters	Note
Read-to-Write, mini-	Same	CL - CWL + RBL/2 + 1 ^t CK + ^t WPRE	1, 2
mum	Different	CL - CWL + RBL/2 + 1 ^t CK + ^t WPRE	1, 2
Write-to-Read, mini-	Same	CWL + WBL/2 + ^t WTR_L	1, 3
mum	Different	CWL + WBL/2 + ^t WTR_S	1, 3

- Notes: 1. These timings require extended calibrations times ^tZQinit and ^tZQCS.
 - 2. RBL: READ burst length associated with READ command, RBL = 8 for fixed 8 and on-thefly mode 8 and RBL = 4 for fixed BC4 and on-the-fly mode BC4.
 - 3. WBL: WRITE burst length associated with WRITE command, WBL = 8 for fixed 8 and onthe-fly mode 8 or BC4 and WBL = 4 for fixed BC4 only.

Read Timing - Clock-to-Data Strobe Relationship

The clock-to-data strobe relationship shown below is applicable in normal operation mode, that is, when the DLL is enabled and locked.



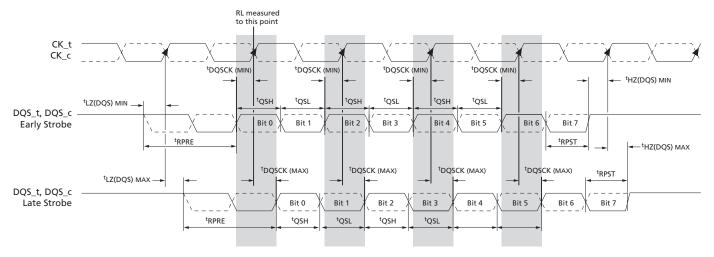
Rising data strobe edge parameters:

- ^tDQSCK (MIN)/(MAX) describes the allowed range for a rising data strobe edge relative to CK.
- ^tDQSCK is the actual position of a rising strobe edge relative to CK.
- tQSH describes the data strobe high pulse width.
- tHZ(DQS) DQS strobe going to high, nondrive level (shown in the postamble section of the figure below).

Falling data strobe edge parameters:

- tQSL describes the data strobe low pulse width.
- tLZ(DQS) DQS strobe going to low, initial drive level (shown in the preamble section of the figure below).

Figure 125: Clock-to-Data Strobe Relationship



Notes:

- 1. Within a burst, the rising strobe edge will vary within [†]DQSCKi while at the same voltage and temperature. However, when the device, voltage, and temperature variations are incorporated, the rising strobe edge variance window can shift between [†]DQSCK (MIN) and [†]DQSCK (MAX).
 - A timing of this window's right edge (latest) from rising CK_t, CK_c is limited by a device's actual ^tDQSCK (MAX). A timing of this window's left inside edge (earliest) from rising CK_t, CK_c is limited by ^tDQSCK (MIN).
- 2. Notwithstanding Note 1, a rising strobe edge with ^tDQSCK (MAX) at T(n) can not be immediately followed by a rising strobe edge with ^tDQSCK (MIN) at T(n + 1) because other timing relationships (^tQSH, ^tQSL) exist: if ^tDQSCK(n + 1) < 0: ^tDQSCK(n) < 1.0 ^tCK (^tQSH (MIN)) + ^tQSL (MIN)) | ^tDQSCK(n + 1) |.
- The DQS_t, DQS_c differential output HIGH time is defined by ^tQSH, and the DQS_t, DQS_c differential output LOW time is defined by ^tQSL.
- 4. ^tLZ(DQS) MIN and ^tHZ(DQS) MIN are not tied to ^tDQSCK (MIN) (early strobe case), and ^tLZ(DQS) MAX and ^tHZ(DQS) MAX are not tied to ^tDQSCK (MAX) (late strobe case).
- 5. The minimum pulse width of READ preamble is defined by ^tRPRE (MIN).
- 6. The maximum READ postamble is bound by ^tDQSCK (MIN) plus ^tQSH (MIN) on the left side and ^tHZDSQ (MAX) on the right side.
- 7. The minimum pulse width of READ postamble is defined by ^tRPST (MIN).



8. The maximum READ preamble is bound by ^tLZDQS (MIN) on the left side and ^tDQSCK (MAX) on the right side.

Read Timing - Data Strobe-to-Data Relationship

The data strobe-to-data relationship is shown below and is applied when the DLL is enabled and locked.

Note: ^tDQSQ: both rising/falling edges of DQS; no ^tAC defined.

Rising data strobe edge parameters:

- ^tDQSQ describes the latest valid transition of the associated DQ pins.
- ^tQH describes the earliest invalid transition of the associated DQ pins.

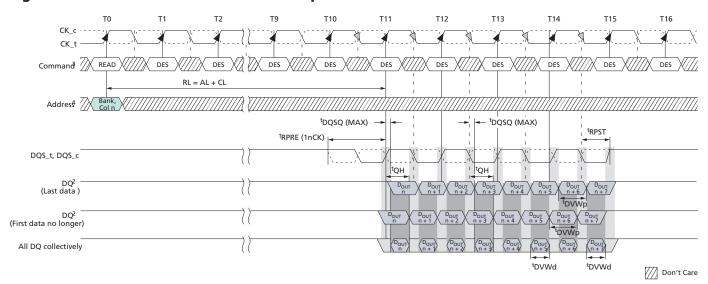
Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Data valid window parameters:

- ^tDVWd is the Data Valid Window per device per UI and is derived from [^tQH ^tDQSQ] of each UI on a given DRAM
- ^tDVWp is the Data Valid Window per pin per UI and is derived [^tQH ^tDQSQ] of each UI on a pin of a given DRAM

Figure 126: Data Strobe-to-Data Relationship



- Notes: 1. BL = 8, RL = 11 (AL = 0, CL = 1), Premable = 1^{t} CK.
 - 2. $D_{OUT}n = data-out from column n$.
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0.
 - 5. Output timings are referenced to V_{DDQ} , and DLL on for locking.
 - 6. ^tDQSQ defines the skew between DQS to data and does not define DQS to clock.



7. Early data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

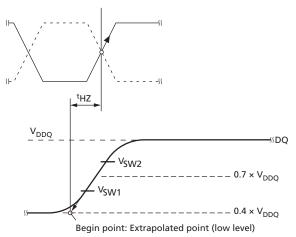
^tLZ(DQS), ^tLZ(DQ), ^tHZ(DQS), and ^tHZ(DQ) Calculations

 t HZ and t LZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving t HZ(DQS) and t HZ(DQ), or begins driving t LZ(DQS) and t LZ(DQ). The figure below shows a method to calculate the point when the device is no longer driving t HZ(DQS) and t HZ(DQ), or begins driving t LZ(DQS) and t LZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. t LZ(DQS), t LZ(DQ), t HZ(DQS), and t HZ(DQ) are defined as singled-ended parameters.

Figure 127: tLZ and tHZ Method for Calculating Transitions and Endpoints

tLZ(DQ): CK_t, CK_c rising crossing at RL

 $^{\rm t}$ HZ(DQ) with BL8: CK_t, CK_c rising crossing at RL + 4CK $^{\rm t}$ HZ(DQ) with BC4: CK_t, CK_c rising crossing at RL + 2CK



Notes

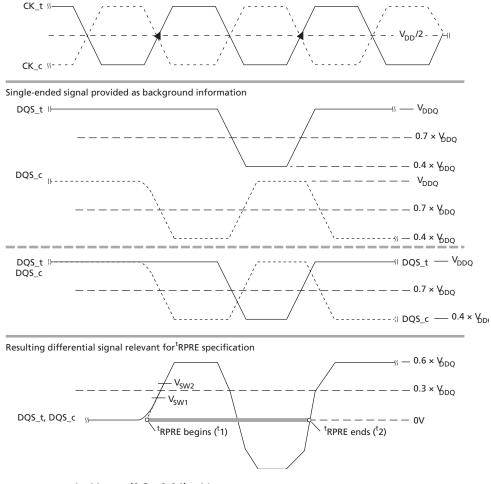
 $0.4 \times V_{DDO}$

- 1. $V_{sw1} = (0.70 0.04) \times V_{DDQ}$ for both ^tLZ and ^tHZ.
- 2. $V_{sw2} = (0.70 + 0.04) \times V_{DDQ}$ for both ^tLZ and ^tHZ.
- 3. Extrapolated point (low level) = $V_{DDQ}/(50 + 34) \times 34 = 0.4 \times V_{DDQ}$ Driver impedance = RZQ/7 = 34Ω V_{TT} test load = 50Ω to V_{DDO} .



^tRPRE Calculation

Figure 128: ^tRPRE Method for Calculating Transitions and Endpoints

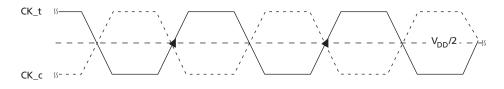


- Notes: 1. $V_{sw1} = (0.3 0.04) \times V_{DDQ}$.
 - 2. $V_{sw2} = (0.30 + 0.04) \times V_{DDQ}$.
 - 3. DQS_t and DQS_c low level = $V_{DDQ}/(50 + 34) \times 34 = 0.4 \times V_{DDQ}$ Driver impedance = RZQ/7 = 34Ω V_{TT} test load = 50Ω to V_{DDQ} .

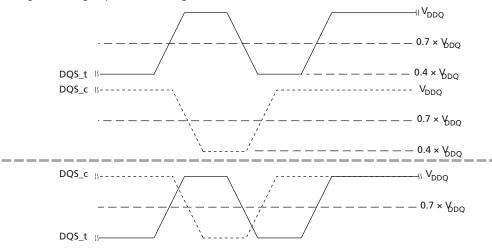


^tRPST Calculation

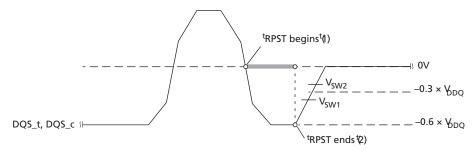
Figure 129: tRPST Method for Calculating Transitions and Endpoints



Single-ended signal provided as background information



Resulting differential signal relevant for^tRPST specification



- Notes: 1. $V_{sw1} = (-0.3 0.04) \times V_{DDQ}$.
 - 2. $V_{sw2} = (-0.30 + 0.04) \times V_{DDQ}$.
 - 3. DQS_t and DQS_c low level = $V_{DDQ}/(50 + 34) \times 34 = 0.4 \times V_{DDQ}$ Driver impedance = RZQ/7 = 34Ω V_{TT} test load = 50Ω to V_{DDQ} .



READ Burst Operation

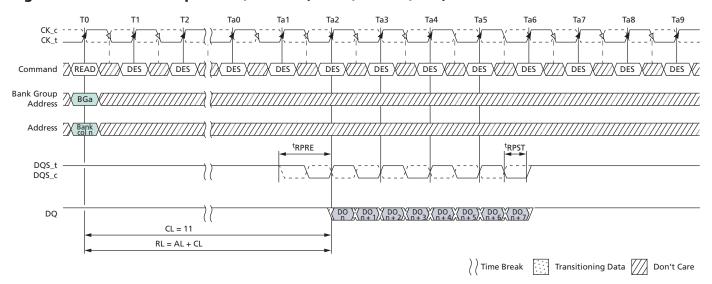
DDR4 READ commands support bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF when OTF is enabled:

- A12 = 0, BC4 (BC4 = burst chop)
- A12 = 1, BL8

READ commands can issue precharge automatically with a READ with auto precharge command (RDA), and is enabled by A10 HIGH:

- READ command with A10 = 0 (RD) performs standard read, bank remains active after READ burst.
- READ command with A10 = 1 (RDA) performs read with auto precharge, bank goes in to precharge after READ burst.

Figure 130: READ Burst Operation, RL = 11 (AL = 0, CL = 11, BL8)

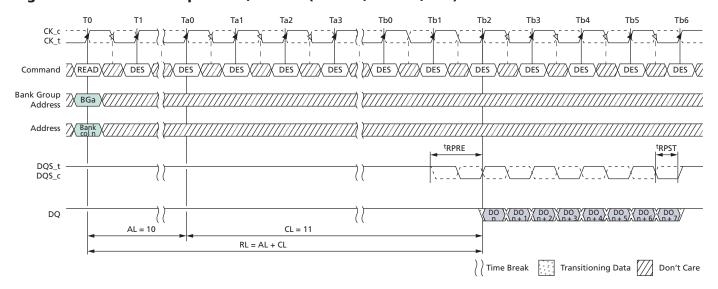


Notes

- BL8, RL = 0, AL = 0, CL = 11, Preamble = 1^tCK.
- 2. DO n = data-out from column n.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ command at T0.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.



Figure 131: READ Burst Operation, RL = 21 (AL = 10, CL = 11, BL8)

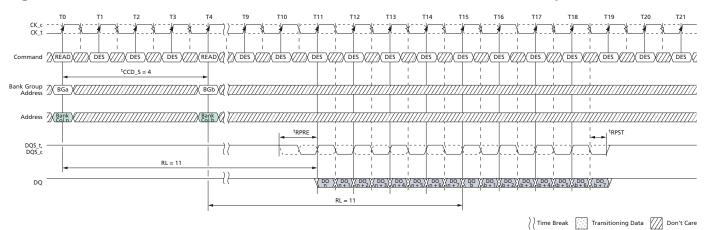


- Notes: 1. BL8, RL = 21, AL = (CL 1), CL = 11, Preamble = 1^{t} CK.
 - 2. DO n = data-out from column n.
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ command at T0.
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.



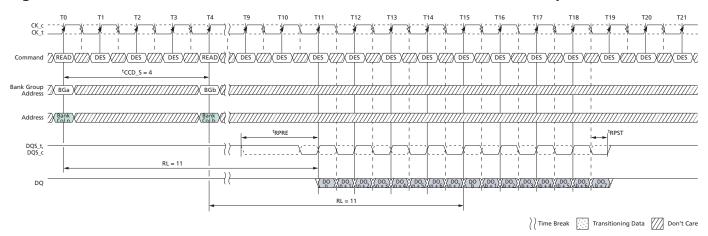
READ Operation Followed by Another READ Operation

Figure 132: Consecutive READ (BL8) with 1tCK Preamble in Different Bank Group



- 1. BL8, AL = 0, CL = 11, Preamble = 1^tCK.
- 2. DO n (or b) = data-out from column n (or column b).
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T4.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

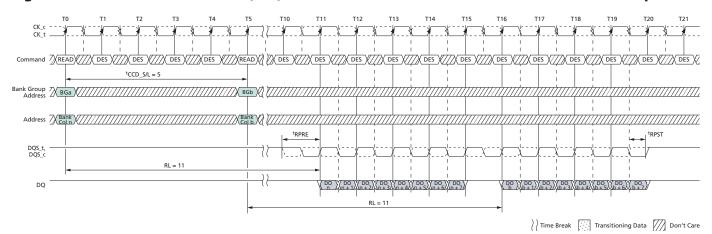
Figure 133: Consecutive READ (BL8) with 2^tCK Preamble in Different Bank Group



- Notes: 1. BL8, AL = 0, CL = 11, Preamble = $2^{t}CK$.
 - 2. DO n (or b) = data-out from column n (or column b).
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T4.
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

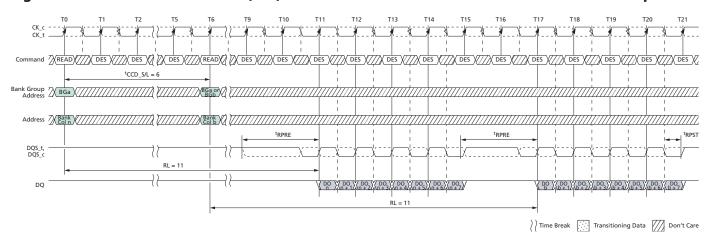


Figure 134: Nonconsecutive READ (BL8) with 1tCK Preamble in Same or Different Bank Group



- Notes: 1. BL8, AL = 0, CL = 11, Preamble = $1^{t}CK$, ${t}CCD_{S}/L = 5$.
 - 2. DO n (or b) = data-out from column n (or column b).
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T5.
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

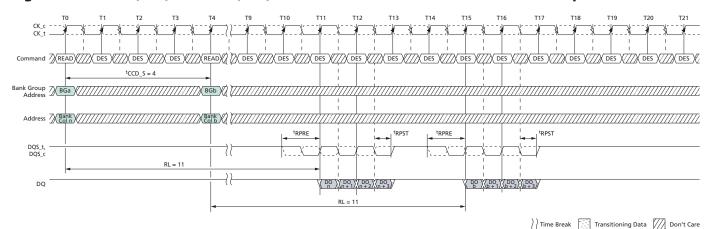
Figure 135: Nonconsecutive READ (BL8) with 2^tCK Preamble in Same or Different Bank Group



- Notes: 1. BL8, AL = 0, CL = 11, Preamble = $2^{t}CK$, ${t}CCD_{S}/L = 6$.
 - 2. DO n (or b) = data-out from column n (or column b).
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and T6.
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.
 - 6. 6 ^{t}CCD S/L = 5 isn't allowed in $2^{t}CK$ preamble mode.

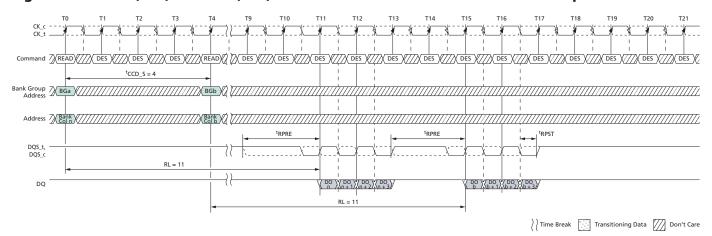


Figure 136: READ (BC4) to READ (BC4) with 1tCK Preamble in Different Bank Group



- Notes: 1. BL8, AL = 0, CL = 11, Preamble = $1^{t}CK$.
 - 2. DO n (or b) = data-out from column n (or column b).
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and T4.
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 137: READ (BC4) to READ (BC4) with 2^tCK Preamble in Different Bank Group

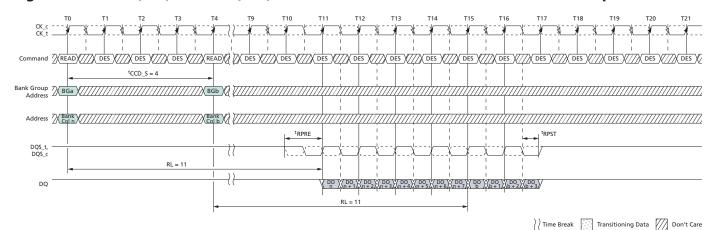


Notes: 1. BL8, AL = 0, CL = 11, Preamble = $2^{t}CK$.

- 2. DO n (or b) = data-out from column n (or column b).
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and T4.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

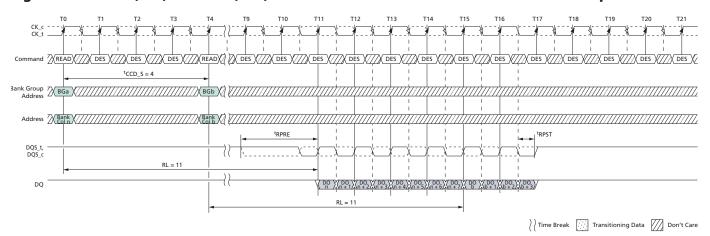


Figure 138: READ (BL8) to READ (BC4) OTF with 1tCK Preamble in Different Bank Group



- Notes: 1. BL = 8, AL = 0, CL = 11, Preamble = 1^tCK.
 - 2. DO n (or b) = data-out from column n (or column b).
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T0. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T4.
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 139: READ (BL8) to READ (BC4) OTF with 2^tCK Preamble in Different Bank Group

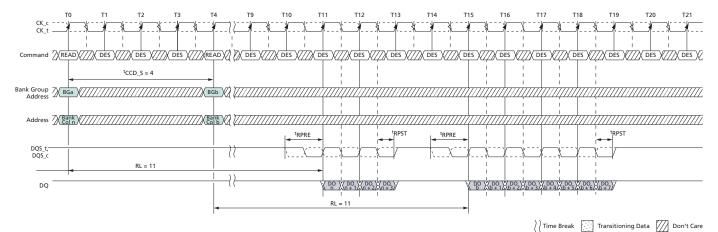


Notes: 1. BL = 8, AL = 0, CL = 11, Preamble = 2^tCK.

- 2. DO n (or b) = data-out from column n (or column b).
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T0. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T4.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

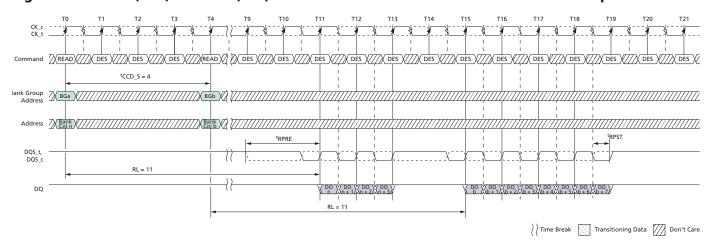


Figure 140: READ (BC4) to READ (BL8) OTF with 1^tCK Preamble in Different Bank Group



- Notes: 1. BL = 8, AL = 0, CL = 11, Preamble = 1^tCK.
 - 2. DO n (or b) = data-out from column n (or column b).
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T4.
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 141: READ (BC4) to READ (BL8) OTF with 2^tCK Preamble in Different Bank Group

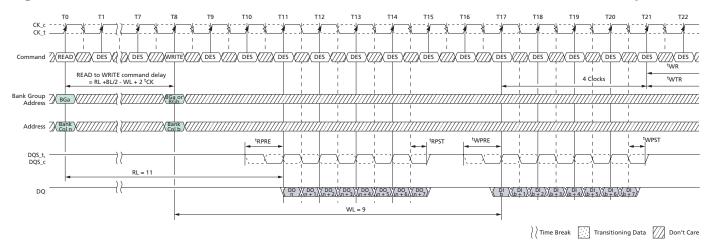


- Notes: 1. BL = 8, AL = 0, CL = 11, Preamble = 2^tCK.
 - 2. DO n (or b) = data-out from column n (or column b).
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T4.
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.



READ Operation Followed by WRITE Operation

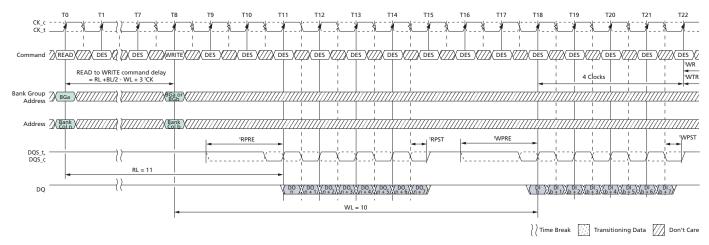
Figure 142: READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



Notes

- 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1^{t} CK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1^{t} CK.
- 2. DO n = data-out from column n; DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and WRITE commands at T8.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 143: READ (BL8) to WRITE (BL8) with 2^tCK Preamble in Same or Different Bank Group



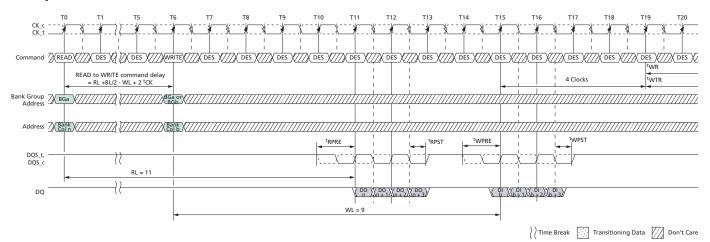
Notes:

- 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 2^{t} CK, WL = 10 (CWL = 9+1 [see Note 5], AL = 0), WRITE preamble = 2^{t} CK.
- 2. DO n = data-out from column n; DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.



- 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and WRITE commands at T8.
- 5. When operating in 2^tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting.
- 6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 144: READ (BC4) OTF to WRITE (BC4) OTF with 1^tCK Preamble in Same or Different Bank Group

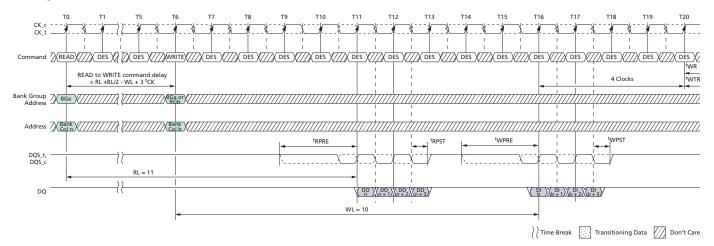


Notes

- 1. BC = 4, RL = 11 (CL = 11, AL = 0), READ preamble = 1^{t} CK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1^{t} CK.
- 2. DO n = data-out from column n; DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 (OTF) setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and WRITE commands at T6.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

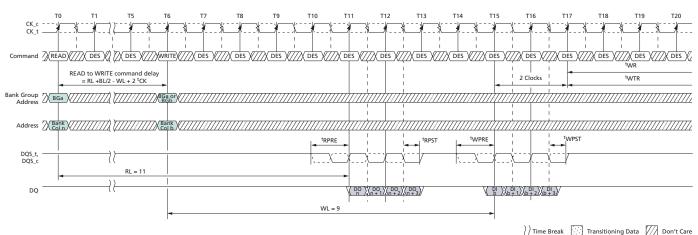


Figure 145: READ (BC4) OTF to WRITE (BC4) OTF with 2^tCK Preamble in Same or Different Bank Group



- Notes:
- 1. BC = 4, RL = 11 (CL = 11, AL = 0), READ preamble = 2^{t} CK, WL = 10 (CWL = 9 + 1 [see Note 5], AL = 0), WRITE preamble = 2^{t} CK.
- 2. DO n = data-out from column n; DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 (OTF) setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and WRITE commands at T6.
- 5. When operating in 2^tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting.
- 6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 146: READ (BC4) Fixed to WRITE (BC4) Fixed with 1^tCK Preamble in Same or Different Bank Group

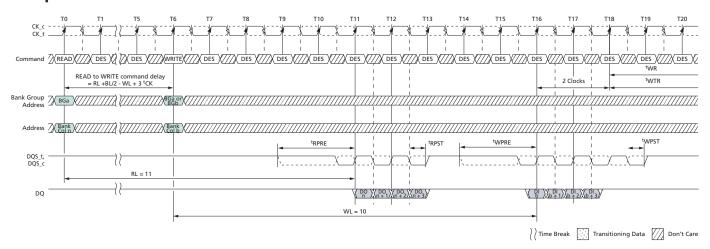


- Notes: 1. BC = 4, RL = 11 (CL = 11, AL = 0), READ preamble = 1^{t} CK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1^{t} CK.
 - 2. DO n = data-out from column n; DI b = data-in from column b.



- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 (fixed) setting activated by MR0[1:0] = 01.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 147: READ (BC4) Fixed to WRITE (BC4) Fixed with 2^tCK Preamble in Same or Different Bank Group

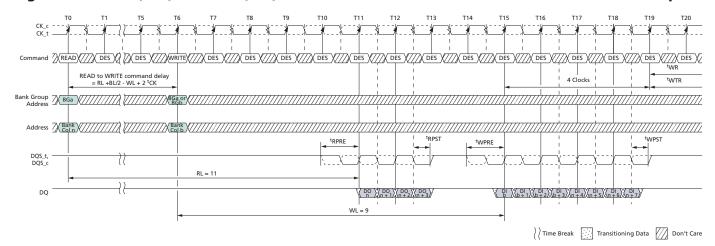


Notes:

- 1. BC = 4, RL = 11 (CL = 11, AL = 0), READ preamble = 2^{t} CK, WL = 9 (CWL = 9 + 1 [see Note 5], AL = 0), WRITE preamble = 2^{t} CK.
- 2. DO n = data-out from column n; DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 (fixed) setting activated by MR0[1:0] = 10.
- 5. When operating in 2^tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting.
- CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.



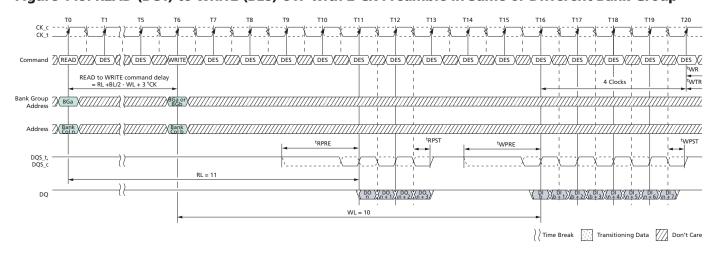
Figure 148: READ (BC4) to WRITE (BL8) OTF with 1tCK Preamble in Same or Different Bank Group



Notes:

- 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1^{t} CK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1^{t} CK.
- 2. DO n = data-out from column n; DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T6.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 149: READ (BC4) to WRITE (BL8) OTF with 2^tCK Preamble in Same or Different Bank Group



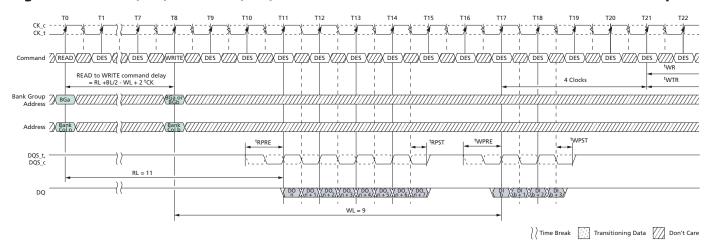
Notes

- 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 2^{t} CK, WL = 10 (CWL = 9 + 1 [see Note 5], AL = 0), WRITE preamble = 2^{t} CK.
- 2. DO n = data-out from column n; DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T6.



 CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

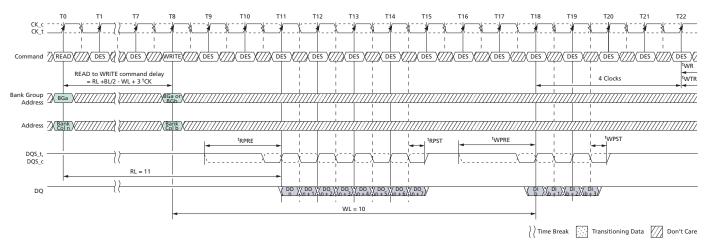
Figure 150: READ (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



Notes:

- 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = $1^{t}CK$, WL = 9 (CWL = 9, AL = 0), WRITE preamble = $1^{t}CK$.
- 2. DO n = data-out from column n; DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T0. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T8.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 151: READ (BL8) to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



votes:

- 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 2^{t} CK, WL = 10 (CWL = 9 + 1 [see Note 5], AL = 0), WRITE preamble = 2^{t} CK.
- 2. DO n = data-out from column n; DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.



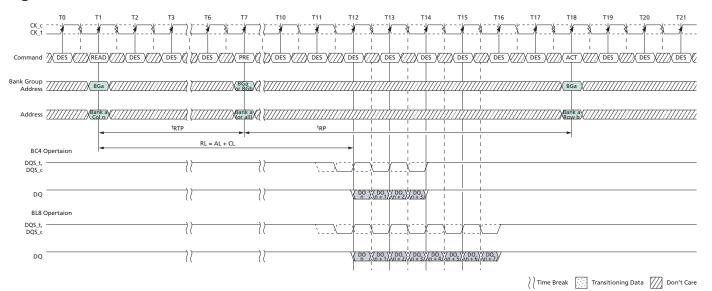
- 4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T0. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T8.
- CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ Operation Followed by PRECHARGE Operation

The minimum external READ command to PRECHARGE command spacing to the same bank is equal to AL + t RTP with t RTP being the internal READ command to PRECHARGE command delay. Note that the minimum ACT to PRE timing, t RAS, must be satisfied as well. The minimum value for the internal READ command to PRECHARGE command delay is given by t RTP (MIN) = MAX (4 × nCK, 7.5ns). A new bank ACTIVATE command may be issued to the same bank if the following two conditions are satisfied simultaneously:

- The minimum RAS precharge time (tRP [MIN]) has been satisfied from the clock at which the precharge begins.
- The minimum RAS cycle time (^tRC [MIN]) from the previous bank activation has been satisfied.

Figure 152: READ to PRECHARGE with 1tCK Preamble

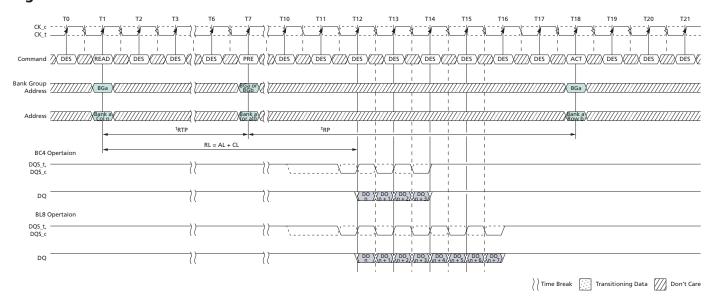


Notes

- 1. RL = 11 (CL = 11, AL = 0), Preamble = $1^{t}CK$, ${}^{t}RTP = 6$, ${}^{t}RP = 11$.
- 2. DO n = data-out from column n.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. The example assumes that ^tRAS (MIN) is satisfied at the PRECHARGE command time (T7) and that ^tRC (MIN) is satisfied at the next ACTIVATE command time (T18).
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

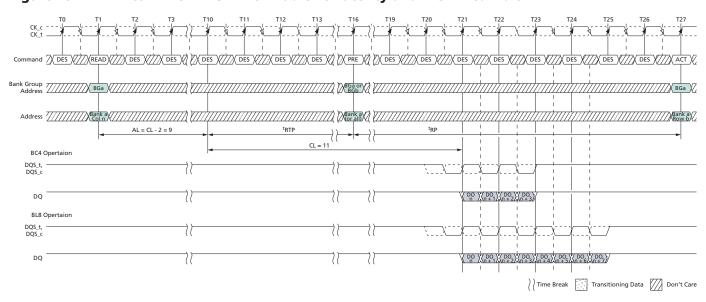


Figure 153: READ to PRECHARGE with 2tCK Preamble



- Notes: 1. RL = 11 (CL = 11, AL = 0), Preamble = $2^{t}CK$, ${}^{t}RTP = 6$, ${}^{t}RP = 11$.
 - 2. DO n = data-out from column n.
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. The example assumes that ^tRAS (MIN) is satisfied at the PRECHARGE command time (T7) and that ^tRC (MIN) is satisfied at the next ACTIVATE command time (T18).
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 154: READ to PRECHARGE with Additive Latency and 1tCK Preamble



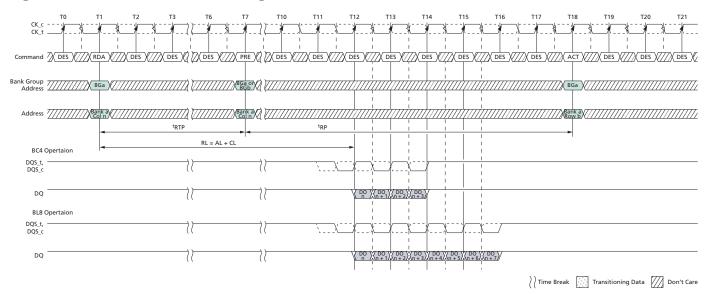
1. RL =20 (CL = 11, AL = CL - 2), Preamble = 1^{t} CK, t RTP = 6, t RP = 11.

2. DO n = data-out from column n.



- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. The example assumes that ^tRAS (MIN) is satisfied at the PRECHARGE command time (T16) and that ^tRC (MIN) is satisfied at the next ACTIVATE command time (T27).
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 155: READ with Auto Precharge and 1tCK Preamble

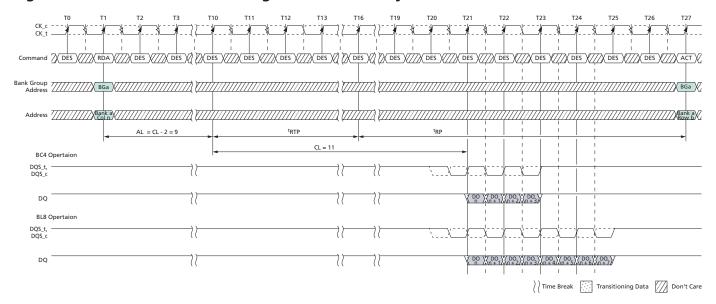


Notes:

- 1. RL = 11 (CL = 11, AL = 0), Preamble = $1^{t}CK$, ${}^{t}RTP = 6$, ${}^{t}RP = 11$.
- 2. DO n = data-out from column n.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. ${}^{t}RTP = 6$ setting activated by MR0[A11:9 = 001].
- 5. The example assumes that ^tRC (MIN) is satisfied at the next ACTIVATE command time (T18).
- 6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.



Figure 156: READ with Auto Precharge, Additive Latency, and 1^tCK Preamble

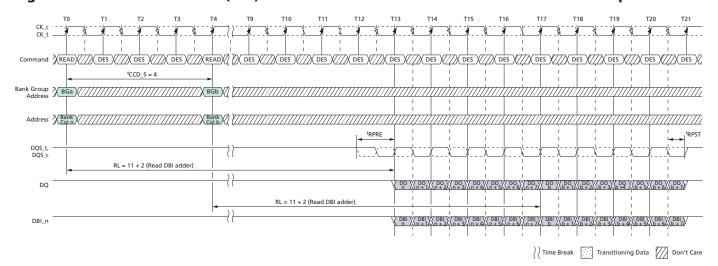


lotes:

- 1. RL = 20 (CL = 11, AL = CL 2), $Preamble = 1^{t}CK$, $^{t}RTP = 6$, $^{t}RP = 11$.
- 2. DO n = data-out from column n.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. ^tRTP = 6 setting activated by MR0[11:9] = 001.
- 5. The example assumes that ^tRC (MIN) is satisfied at the next ACTIVATE command time (T27).
- 6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

READ Operation with Read Data Bus Inversion (DBI)

Figure 157: Consecutive READ (BL8) with 1tCK Preamble and DBI in Different Bank Group



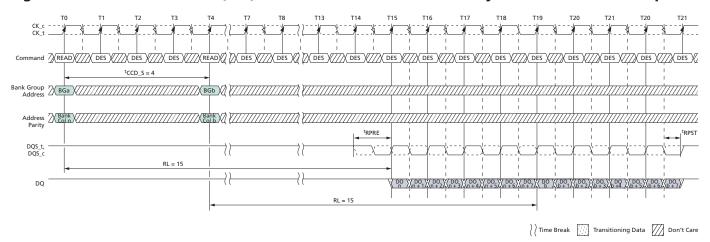
Notes: 1. BL = 8, AL = 0, CL = 11, $Preamble = 1^{\dagger}CK$, RL = 11 + 2 (Read DBI adder).



- 2. DO n (or b) = data-out from column n (or b); DBI n (or b) = data bus inversion from column n (or b).
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T4.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Enable.

READ Operation with Command/Address Parity (CA Parity)

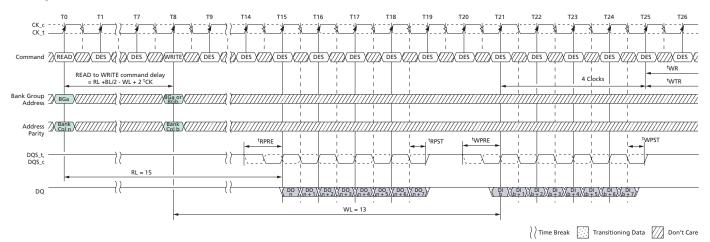
Figure 158: Consecutive READ (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



- 1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Preamble = 1^tCK.
- 2. DO n (or b) = data-out from column n (or b).
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by either MR0[A1:A0 = 00] or MR0[A1:A0 = 01] and A12 = 1 during READ commands at T0 and T4.
- 5. CA parity = Enable, CS to CA latency = Disable, Read DBI = Disable.



Figure 159: READ (BL8) to WRITE (BL8) with 1^tCK Preamble and CA Parity in Same or Different Bank Group



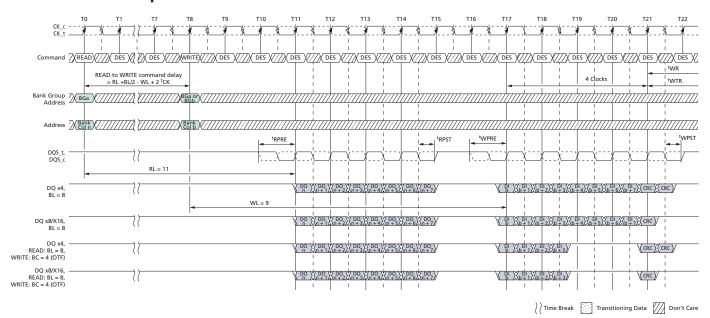
Votes:

- 1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), READ preamble = 1^{t} CK, CWL = 9, AL = 0, PL = 4, (WL = CL + AL + PL = 13), WRITE preamble = 1^{t} CK.
- 2. DO n = data-out from column n, DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and WRITE command at T8.
- 5. CA parity = Enable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.



READ Followed by WRITE with CRC Enabled

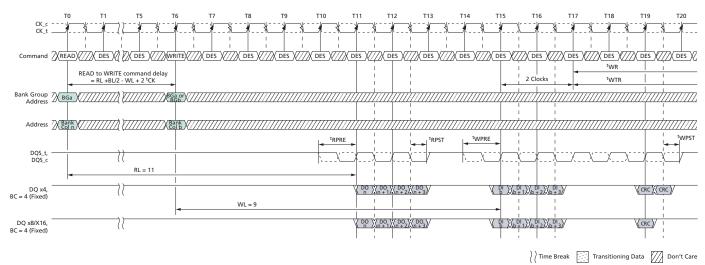
Figure 160: READ (BL8) to WRITE (BL8 or BC4: OTF) with 1^tCK Preamble and Write CRC in Same or Different Bank Group



- 1. BL = 8 (or BC = 4: OTF for Write), RL = 11 (CL = 11, AL = 0), READ preamble = 1^{t} CK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1^{t} CK.
- 2. DO n = data-out from column n, DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and WRITE commands at T8.
- 5. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T8.
- 6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.



Figure 161: READ (BC4: Fixed) to WRITE (BC4: Fixed) with 1^tCK Preamble and Write CRC in Same or Different Bank Group

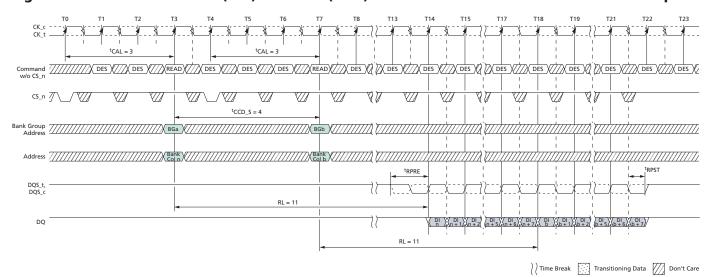


Notes:

- 1. BC = 4 (Fixed), RL = 11 (CL = 11, AL = 0), READ preamble = 1^{t} CK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1^{t} CK.
- 2. DO n = data-out from column n, DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 setting activated by MR0[1:0] = 10.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

READ Operation with Command/Address Latency (CAL) Enabled

Figure 162: Consecutive READ (BL8) with CAL (3tCK) and 1tCK Preamble in Different Bank Group

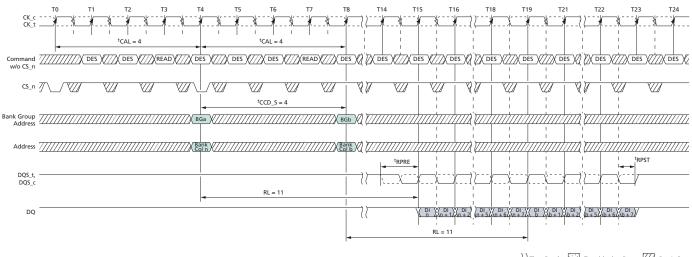


Notes: 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = $1^{t}CK$.



- 2. DI n (or b) = data-in from column n (or b).
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T3 and T7.
- 5. CA parity = Disable, CS to CA latency = Enable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
- 6. Enabling CAL mode does not impact ODT control timings. The same timing relationship relative to the command/address bus as when CAL is disabled should be maintained.

Figure 163: Consecutive READ (BL8) with CAL (4^tCK) and 1^tCK Preamble in Different Bank Group



Time Break Transitioning Data Don't Care

- Notes: 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1^{t} CK.
 - 2. DI n (or b) = data-in from column n (or b).
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T3 and T8.
 - 5. CA parity = Disable, CS to CA latency = Enable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
 - 6. Enabling CAL mode does not impact ODT control timings. The same timing relationship relative to the command/address bus as when CAL is disabled should be maintained.



WRITE Operation

Write Timing Definitions

The write timings shown in the following figures are applicable in normal operation mode, that is, when the DLL is enabled and locked.

Write Timing - Clock-to-Data Strobe Relationship

The clock-to-data strobe relationship is shown below and is applicable in normal operation mode, that is, when the DLL is enabled and locked.

Rising data strobe edge parameters:

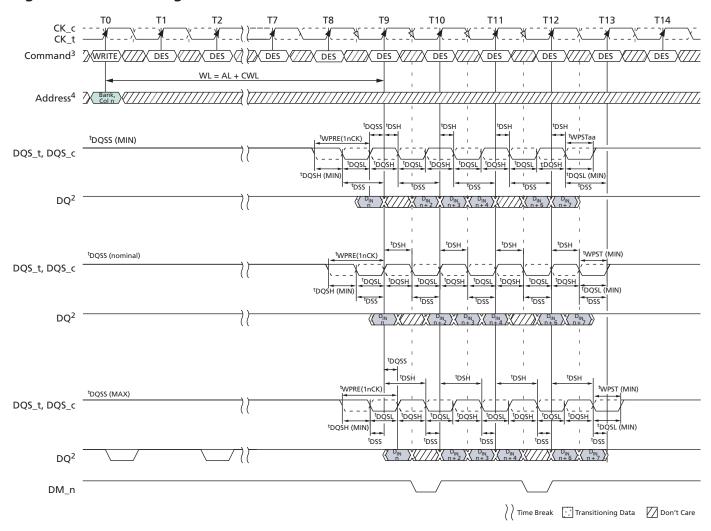
- ^tDQSS (MIN) to ^tDQSS (MAX) describes the allowed range for a rising data strobe edge relative to CK.
- ^tDQSS is the actual position of a rising strobe edge relative to CK.
- ^tDQSH describes the data strobe high pulse width.
- tWPST strobe going to HIGH, nondrive level (shown in the postamble section of the graphic below).

Falling data strobe edge parameters:

- ^tDQSL describes the data strobe low pulse width.
- tWPRE strobe going to LOW, initial drive level (shown in the preamble section of the graphic below).



Figure 164: Write Timing Definition

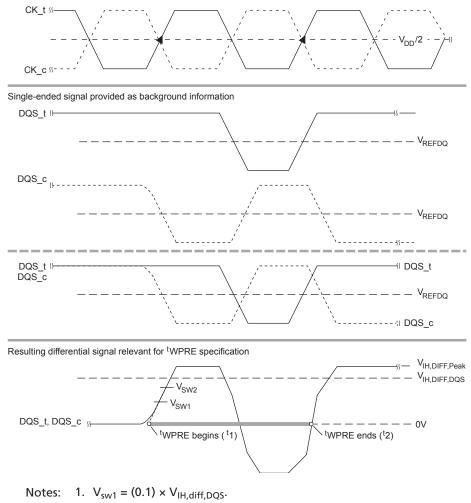


- Notes: 1. BL8, WL = 9 (AL = 0, CWL = 9).
 - 2. $D_{IN}n = data-in from column n$.
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
 - 5. ^tDQSS must be met at each rising clock edge.



^tWPRE Calculation

Figure 165: tWPRE Method for Calculating Transitions and Endpoints

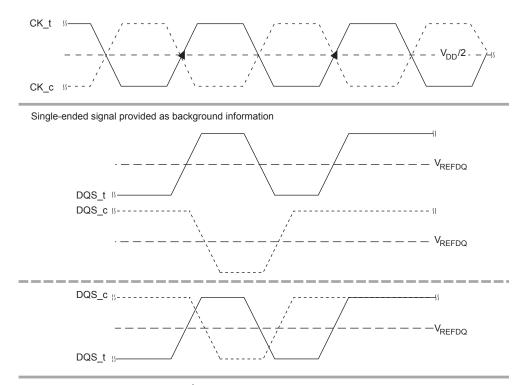


Notes: 1. $V_{sw1} = (0.1) \times V_{IH,diff,DQS}$. 2. $V_{sw2} = (0.9) \times V_{IH,diff,DQS}$.

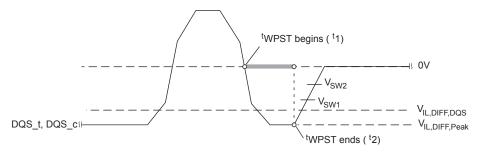


^tWPST Calculation

Figure 166: tWPST Method for Calculating Transitions and Endpoints



Resulting differential signal relevant for \$\$^tWPST\$ specification



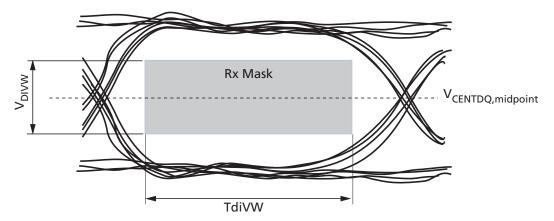
Notes: 1. $V_{sw1} = (0.9) \times V_{IL,diff,DQS}$. 2. $V_{sw2} = (0.1) \times V_{IL,diff,DQS}$.

Write Timing - Data Strobe-to-Data Relationship

The DQ input receiver uses a compliance mask (Rx) for voltage and timing as shown in the figure below. The receiver mask (Rx mask) defines the area where the input signal must not encroach in order for the DRAM input receiver to be able to successfully capture a valid input signal. The Rx mask is not the valid data-eye. TdiVW and V_{diVW} define the absolute maximum Rx mask.

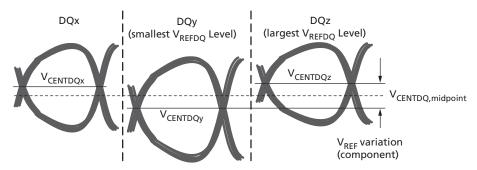


Figure 167: Rx Compliance Mask



 $V_{CENTDQ,midpoint} \ is \ defined \ as \ the \ midpoint \ between \ the \ largest \ V_{REFDQ} \ voltage \ level \ and \ the \ smallest \ V_{REFDQ} \ voltage \ level \ across \ all \ DQ \ pins \ for \ a \ given \ DRAM. Each \ DQ \ pin's \ V_{REFDQ} \ is \ defined \ by \ the \ center \ (widest \ opening) \ of \ the \ cumulative \ data \ input \ eye \ as \ depicted \ in \ the \ following \ figure. This means \ a \ DRAM's \ level \ variation \ is \ accounted \ for \ within \ the \ DRAM \ Rx \ mask. The \ DRAM \ V_{REFDQ} \ level \ will \ be \ set \ by \ the \ system \ to \ account \ for \ R_{ON} \ and \ ODT \ settings.$

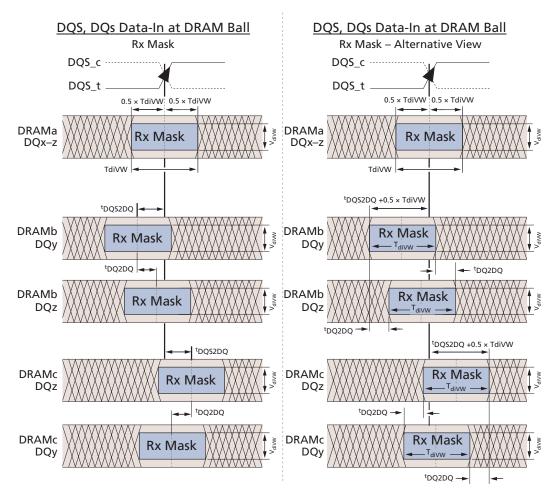
Figure 168: V_{CENT DO} V_{REFDO} Voltage Variation



The following figure shows the Rx mask requirements both from a midpoint-to-midpoint reference (left side) and from an edge-to-edge reference. The intent is not to add any new requirement or specification between the two but rather how to convert the relationship between the two methodologies. The minimum data-eye shown in the composite view is not actually obtainable due to the minimum pulse width requirement.



Figure 169: Rx Mask DQ-to-DQS Timings



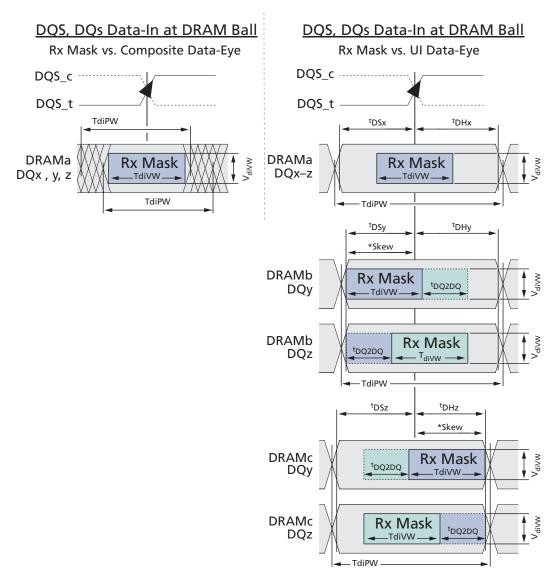
Notes:

- DQx represents an optimally centered mask. DQy represents earliest valid mask.
 - DQz represents latest valid mask.
- DRAMa represents a DRAM without any DQS/DQ skews. DRAMb represents a DRAM with early skews (negative ^tDQS2DQ). DRAMc represents a DRAM with delayed skews (positive ^tDQS2DQ).
- 3. This figure shows the skew allowed between DRAM-to-DRAM and between DQ-to-DQ for a DRAM. Signals assume data is center-aligned at DRAM latch. TdiPW is not shown; composite data-eyes shown would violate TdiPW. V_{CENTDQ,midpoint} is not shown but is assumed to be midpoint of V_{diVW}.

The previous figure shows the basic Rx mask requirements. Converting the Rx mask requirements to a classical DQ-to-DQS relationship is shown in the following figure. It should become apparent that DRAM write training is required to take full advantage of the Rx mask.



Figure 170: Rx Mask DQ-to-DQS DRAM-Based Timings



Notes: 1. DQx represents an optimally centered mask.
DQy represents earliest valid mask.
DQz represents latest valid mask.

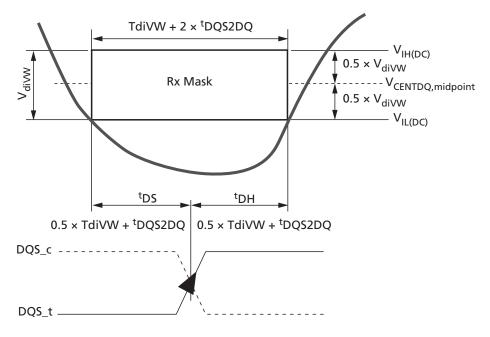
- *Skew = ^tDQS2DQ + 0.5 x TdiVW
 DRAMa represents a DRAM without any DQS/DQ skews.
 DRAMb represents a DRAM with the earliest skews (negative ^tDQS2DQ, ^tDQSy > *Skew).
 DRAMc represents a DRAM with the latest skews (positive ^tDQS2DQ, ^tDQHz > *Skew).
- tDS/tDH are traditional data-eye setup/hold edges at DC levels.
 tDS and tDH are not specified; tDH and tDS may be any value provided the pulse width and Rx mask limits are not violated.
 tDH (MIN) > TdiVW + tDS (MIN) + tDQ2DQ.

The DDR4 SDRAM's input receivers are expected to capture the input data with an Rx mask of TdiVW provided the minimum pulse width is satisfied. The DRAM controller will have to train the data input buffer to utilize the Rx mask specifications to this maxi-



mum benefit. If the DRAM controller does not train the data input buffers, then the worst case limits have to be used for the Rx mask (TdiVW + $2 \times {}^{t}DQS2DQ$), which will generally be the classical minimum (${}^{t}DS$ and ${}^{t}DH$) and is required as well.

Figure 171: Example of Data Input Requirements Without Training



WRITE Burst Operation

The following write timing diagrams are intended to help understand each write parameter's meaning and are only examples. Each parameter will be defined in detail separately. In these write timing diagrams, CK and DQS are shown aligned, and DQS and DQ are shown center-aligned for the purpose of illustration.

DDR4 WRITE command supports bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF when OTF is enabled:

- A12 = 0, BC4 (BC4 = burst chop)
- A12 = 1, BL8

WRITE commands can issue precharge automatically with a WRITE with auto precharge (WRA) command, which is enabled by A10 HIGH.

- WRITE command with A10 = 0 (WR) performs standard write, bank remains active after WRITE burst
- WRITE command with A10 = 1 (WRA) performs write with auto precharge, bank goes into precharge after WRITE burst

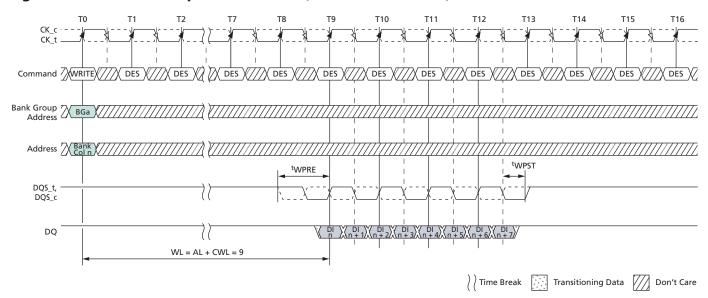
The DATA MASK (DM) function is supported for the x8 and x16 configurations only (the DM function is not supported on x4 devices). The DM function shares a common pin with the DBI_n and TDQS functions. The DM function only applies to WRITE operations and cannot be enabled at the same time the DBI function is enabled.

• If DM_n is sampled LOW on a given byte lane, the DRAM masks the write data received on the DQ inputs.



- If DM_n is sampled HIGH on a given byte lane, the DRAM does not mask the data and writes this data into the DRAM core.
- If CRC write is enabled, then DM enabled (via MRS) will be selected between write CRC nonpersistent mode (DM disabled) and write CRC persistent mode (DM enabled).

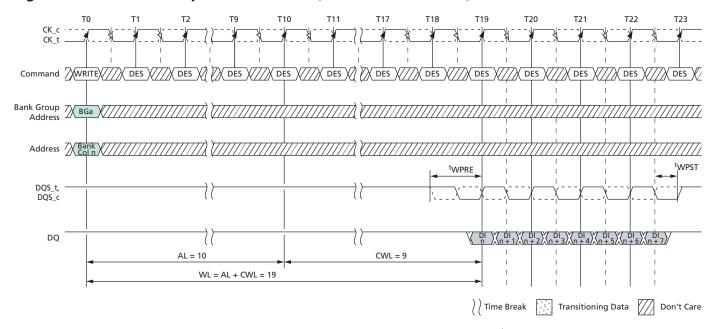
Figure 172: WRITE Burst Operation, WL = 9 (AL = 0, CWL = 9, BL8)



- Notes: 1. BL8, WL = 0, AL = 0, CWL = 9, Preamble = 1^{t} CK.
 - 2. DI n = Data-in from column n.
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
 - 5. CA parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.



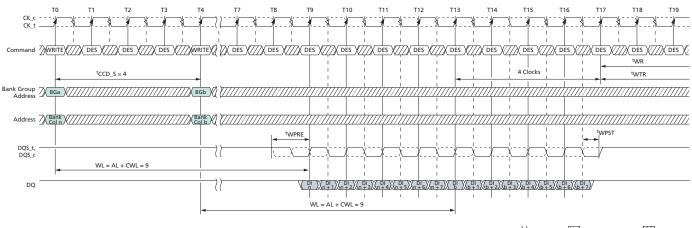
Figure 173: WRITE Burst Operation, WL = 19 (AL = 10, CWL = 9, BL8)



- Notes: 1. BL8, WL = 19, AL = 10 (CL 1), CWL = 9, Preamble = 1^{t} CK.
 - 2. DI n = data-in from column n.
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

WRITE Operation Followed by Another WRITE Operation

Figure 174: Consecutive WRITE (BL8) with 1tCK Preamble in Different Bank Group



Time Break Transitioning Data Don't Care

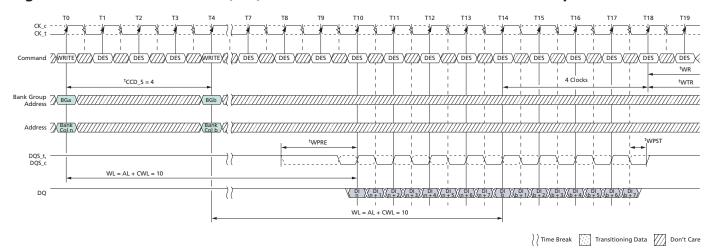
1. BL8, AL = 0, CWL = 9, Preamble = 1^tCK.

2. DI n (or b) = data-in from column n (or column b).



- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.
- 5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
- 6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

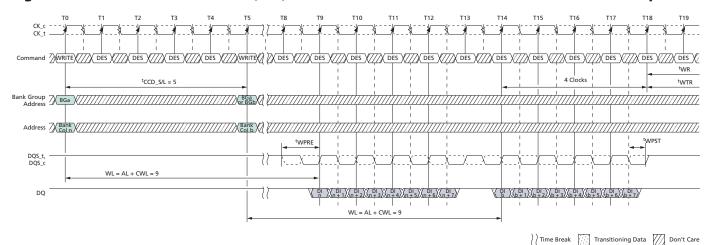
Figure 175: Consecutive WRITE (BL8) with 2^tCK Preamble in Different Bank Group



- 1. BL8, AL = 0, CWL = 9 + 1 = 10 (see Note 7), Preamble = 2^{t} CK.
- 2. DI n (or b) = data-in from column n (or column b).
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.
- 5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
- 6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.
- 7. When operating in 2^tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^tCK range, which means CWL = 9 is not allowed when operating in 2^tCK WRITE preamble mode.

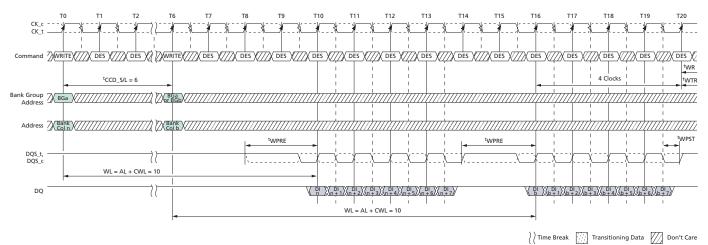


Figure 176: Nonconsecutive WRITE (BL8) with 1^tCK Preamble in Same or Different Bank Group



- Notes: 1. BL8, AL = 0, CWL = 9, Preamble = 1^{t} CK, t CCD_S/L = 5^{t} CK.
 - 2. DI n (or b) = data-in from column n (or column b).
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T5.
 - 5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
 - 6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

Figure 177: Nonconsecutive WRITE (BL8) with 2^tCK Preamble in Same or Different Bank Group

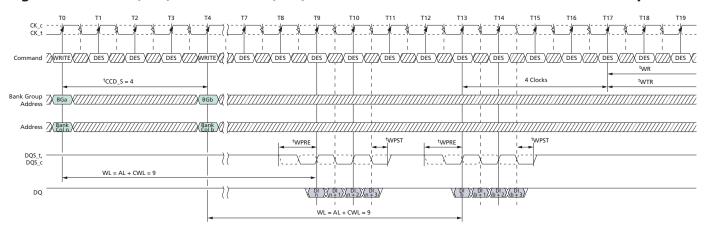


- Notes: 1. BL8, AL = 0, CWL = 9 + 1 = 10 (see Note 8), Preamble = 2^{t} CK, t CCD_S/L = 6^{t} CK.
 - 2. DI n (or b) = data-in from column n (or column b).
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T6.



- 5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
- 6. ^tCCD_S/L = 5 isn't allowed in 2^tCK preamble mode.
- 7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T20.
- 8. When operating in 2^tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^tCK range, which means CWL = 9 is not allowed when operating in 2^tCK WRITE preamble mode.

Figure 178: WRITE (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group

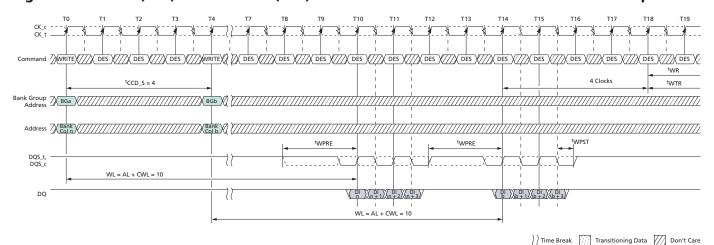


Time Break Transitioning Data Don't Care

- 1. BC4, AL = 0, CWL = 9, Preamble = 1^{t} CK.
- 2. DI n (or b) = data-in from column n (or column b).
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T4.
- 5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
- 6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.



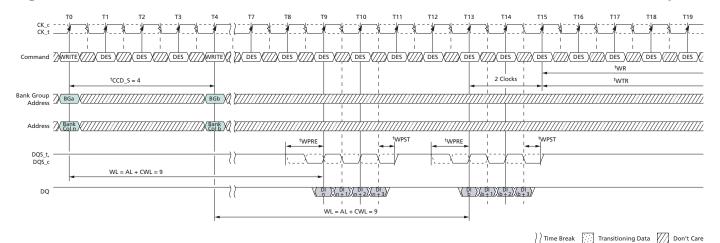
Figure 179: WRITE (BC4) OTF to WRITE (BC4) OTF with 2^tCK Preamble in Different Bank Group



Notes: 1. BC4, AL = 0, CWL = 9 + 1 = 10 (see Note 7), Preamble = 2^{t} CK.

- 2. DI n (or b) = data-in from column n (or column b).
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 setting activated by MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.
- 5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
- 6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.
- 7. When operating in 2^tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^tCK range, which means CWL = 9 is not allowed when operating in 2^tCK WRITE preamble mode.

Figure 180: WRITE (BC4) Fixed to WRITE (BC4) Fixed with 1^tCK Preamble in Different Bank Group



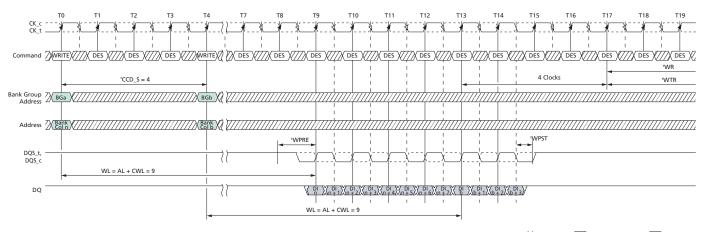
Notes: 1. BC4, AL = 0, CWL = 9, Preamble = 1^tCK.

2. DI n (or b) = data-in from column n (or column b).



- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 (fixed) setting activated by MR0[1:0] = 10.
- 5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
- 6. The write recovery time (^tWR) and write timing parameter (^tWTR) are referenced from the first rising clock edge after the last write data shown at T15.

Figure 181: WRITE (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group

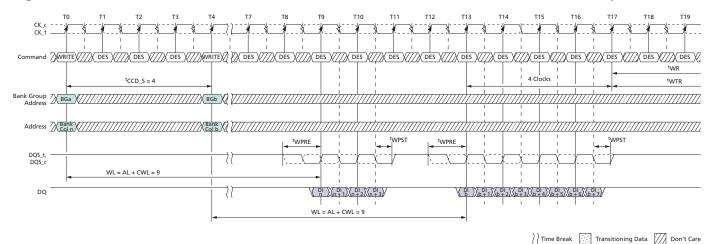


Time Break Transitioning Data Don't Care

- 1. BL = 8/BC = 4, AL = 0, CL = 9, Preamble = 1^tCK.
- 2. DI n (or b) = data-in from column n (or column b).
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during WRITE command at T0. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T4.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Disable.
- 6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.



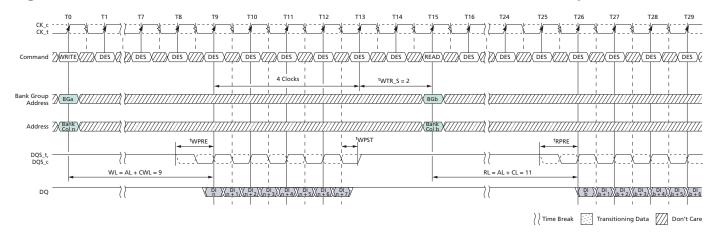
Figure 182: WRITE (BC4) OTF to WRITE (BL8) with 1^tCK Preamble in Different Bank Group



- Notes: 1. BL = 8/BC = 4, AL = 0, CL = 9, Preamble = $1^{t}CK$.
 - 2. DI n (or b) = data-in from column n (or column b).
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during WRITE command at T4.
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Disable.
 - 6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

WRITE Operation Followed by READ Operation

Figure 183: WRITE (BL8) to READ (BL8) with 1^tCK Preamble in Different Bank Group

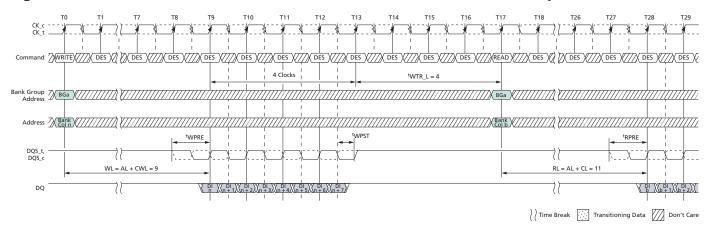


- 1. BL = 8, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1^{\dagger} CK, WRITE preamble = 1^tCK.
- 2. DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.



- 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0 and READ command at T15.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
- 6. The write timing parameter (tWTR_S) is referenced from the first rising clock edge after the last write data shown at T13.

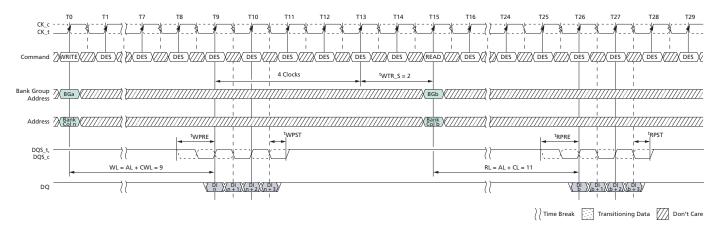
Figure 184: WRITE (BL8) to READ (BL8) with 1tCK Preamble in Same Bank Group



- 1. BL = 8, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1^{t} CK, WRITE preamble = 1^{t} CK.
- 2. DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0 and READ command at T17.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
- 6. The write timing parameter (^tWTR_L) is referenced from the first rising clock edge after the last write data shown at T13.



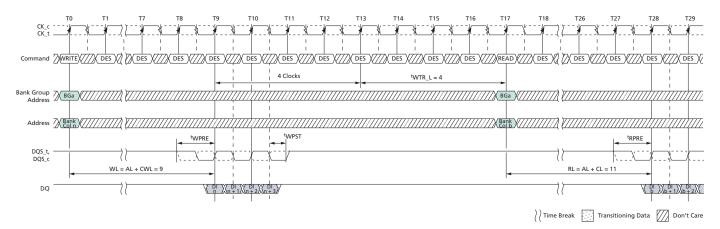
Figure 185: WRITE (BC4) OTF to READ (BC4) OTF with 1^tCK Preamble in Different Bank Group



Notes:

- 1. BC = 4, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1^{t} CK, WRITE preamble = 1^{t} CK.
- 2. DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0 and READ command at T15.
- CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
- 6. The write timing parameter (tWTR_S) is referenced from the first rising clock edge after the last write data shown at T13.

Figure 186: WRITE (BC4) OTF to READ (BC4) OTF with 1^tCK Preamble in Same Bank Group

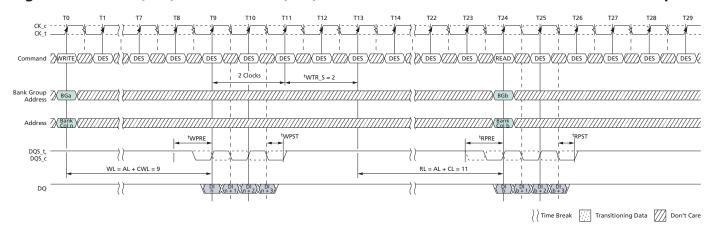


- 1. BC = 4, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1^{t} CK, WRITE preamble = 1^{t} CK.
- 2. DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0 and READ command at T17.



- CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
- 6. The write timing parameter (^tWTR_L) is referenced from the first rising clock edge after the last write data shown at T13.

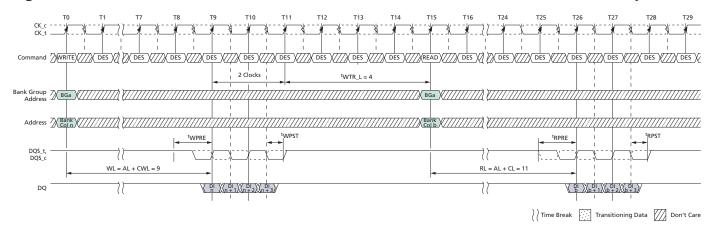
Figure 187: WRITE (BC4) Fixed to READ (BC4) Fixed with 1 tCK Preamble in Different Bank Group



Notes: 1. BC = 4, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1^{t} CK, WRITE preamble = 1^{t} CK.

- 2. DI b = data-in from column b.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 setting activated by MR0[1:0] = 10.
- CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
- 6. The write timing parameter (^tWTR_S) is referenced from the first rising clock edge after the last write data shown at T11.

Figure 188: WRITE (BC4) Fixed to READ (BC4) Fixed with 1tCK Preamble in Same Bank Group



Notes: 1. BC = 4, WL = 9 (CWL = 9, AL = 0), C L = 11, READ preamble = 1^{t} CK, WRITE preamble = 1^{t} CK.

2. DI b = data-in from column b.

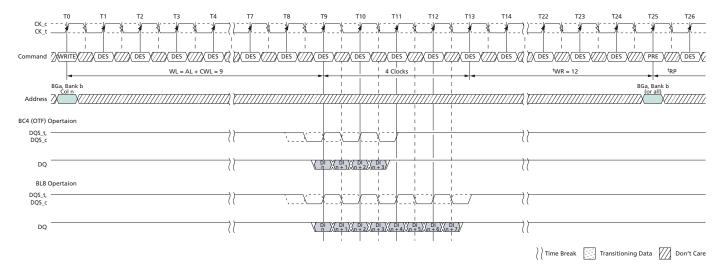


- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BC4 setting activated by MR0[1:0] = 10.
- CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
- 6. The write timing parameter (^tWTR_L) is referenced from the first rising clock edge after the last write data shown at T11.

WRITE Operation Followed by PRECHARGE Operation

The minimum external WRITE command to PRECHARGE command spacing is equal to WL (AL + CWL) plus either 4^tCK (BL8/BC4-OTF) or 2^tCK (BC4-fixed) plus ^tWR. The minimum ACT to PRE timing, ^tRAS, must be satisfied as well.

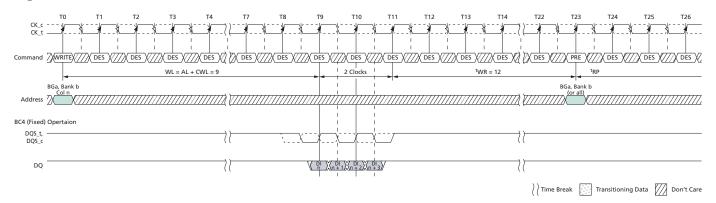
Figure 189: WRITE (BL8/BC4-OTF) to PRECHARGE with 1tCK Preamble



- 1. BL = 8 with BC4-OTF, WL = 9 (CWL = 9, AL = 0), Preamble = 1^{t} CK, t^{t} WR = 12.
- 2. DI n = data-in from column n.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times
- 4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0. BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
- 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.
- 6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T13. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

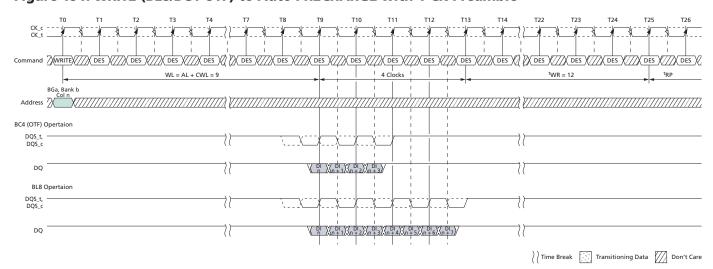






- Notes: 1. BC4 = fixed, WL = 9 (CWL = 9, AL = 0), Preamble = 1^tCK, ^tWR = 12.
 - 2. DI n = data-in from column n.
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BC4 setting activated by MR0[1:0] = 10.
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.
 - 6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

Figure 191: WRITE (BL8/BC4-OTF) to Auto PRECHARGE with 1^tCK Preamble

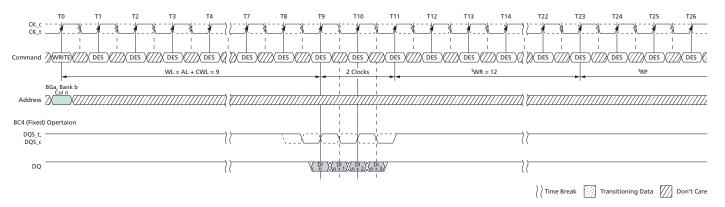


- Notes: 1. BL = 8 with BC4-OTF, WL = 9 (CWL = 9, AL = 0), Preamble = 1^{t} CK, tWR = 12.
 - 2. DI n = data-in from column n.
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0. BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE com-
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.



6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T13. ^tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

Figure 192: WRITE (BC4-Fixed) to Auto PRECHARGE with 1tCK Preamble

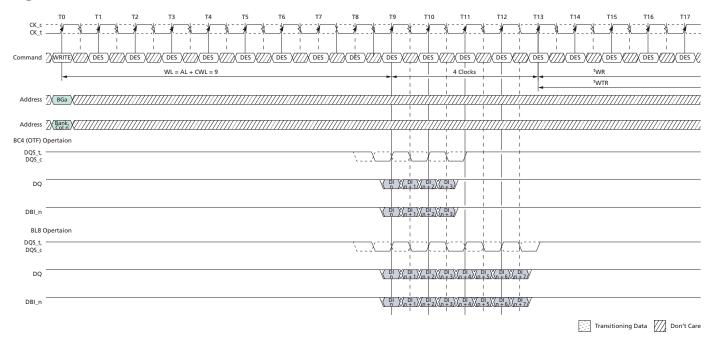


- Notes: 1. BC4 = fixed, WL = 9 (CWL = 9, AL = 0), Preamble = $1^{t}CK$, ${}^{t}WR = 12$.
 - 2. DI n = data-in from column n.
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BC4 setting activated by MR0[1:0] = 10.
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.
 - 6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.



WRITE Operation with WRITE DBI Enabled

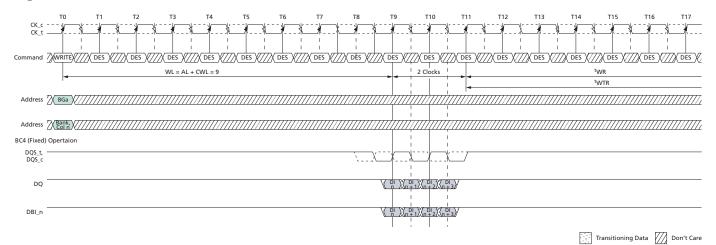
Figure 193: WRITE (BL8/BC4-OTF) with 1tCK Preamble and DBI



- 1. BL = 8 with BC4-OTF, WL = 9 (CWL = 9, AL = 0), Preamble = 1^{t} CK.
- 2. DI n = data-in from column n.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0.
 BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
- 5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Enabled, Write CRC = Disabled.
- 6. The write recovery time (tWR_DBI) is referenced from the first rising clock edge after the last write data shown at T13.



Figure 194: WRITE (BC4-Fixed) with 1tCK Preamble and DBI

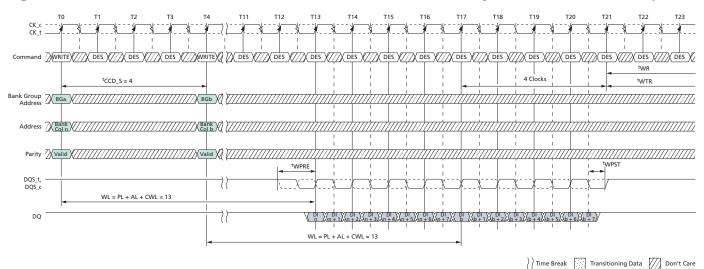


- Notes: 1. BC4 = fixed, WL = 9 (CWL = 9, AL = 0), Preamble = 1^{t} CK.
 - 2. DI n = data-in from column n.
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BC4 setting activated by MR0[1:0] = 10.
 - 5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Enabled, Write CRC = Disabled.



WRITE Operation with CA Parity Enabled

Figure 195: Consecutive Write (BL8) with 1tCK Preamble and CA Parity in Different Bank Group

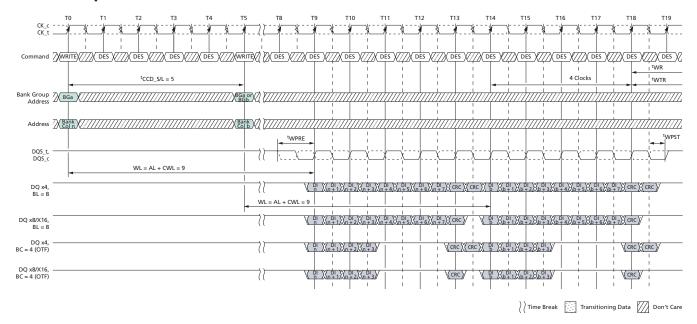


- 1. BL = 8, WL = 9 (CWL = 13, AL = 0), Preamble = 1^{t} CK.
- 2. DI n = data-in from column n.
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.
- 5. CA parity = Enable, CS to CA latency = Disable, Write DBI = Enabled, Write CRC = Disable.
- 6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.



WRITE Operation with Write CRC Enabled

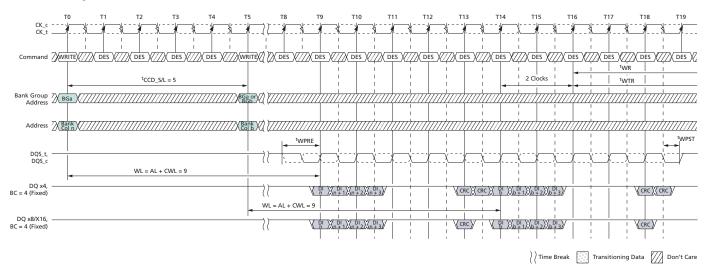
Figure 196: Consecutive WRITE (BL8/BC4-OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group



- Notes: 1. BL8/BC4-OTF, AL = 0, CWL = 9, Preamble = 1^{t} CK, t CCD_S/L = 5^{t} CK.
 - 2. DI n (or b) = data-in from column n (or column b).
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T5.
 - 5. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and
 - 6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable.
 - 7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.



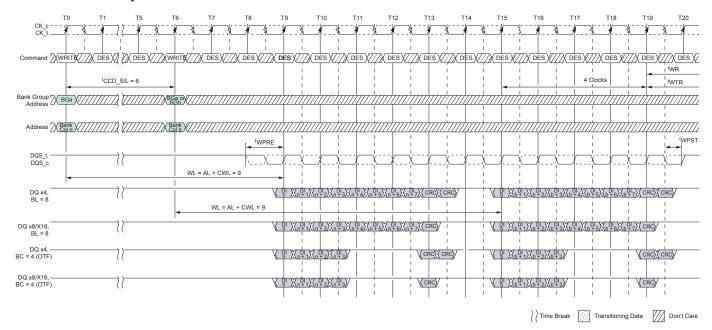
Figure 197: Consecutive WRITE (BC4-Fixed) with 1tCK Preamble and Write CRC in Same or Different **Bank Group**



- Notes: 1. BC4-fixed, AL = 0, CWL = 9, $Preamble = 1^{t}CK$, $^{t}CCD_{S}/L = 5^{t}CK$.
 - 2. DI n (or b) = data-in from column n (or column b).
 - 3. DES commands are shown for ease of illustration; other commands may be valid at
 - 4. BC4 setting activated by MR0[1:0] = 10 during WRITE commands at T0 and T5.
 - 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Disable.
 - 6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T16.



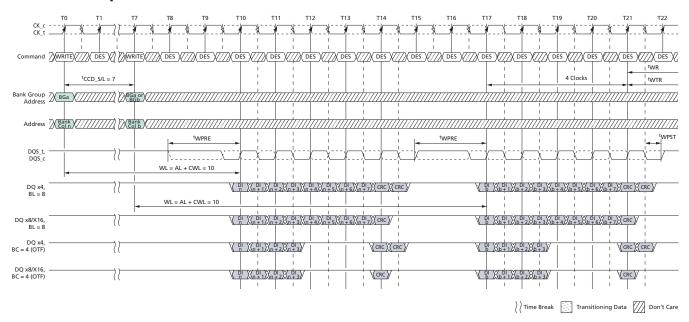
Figure 198: Nonconsecutive WRITE (BL8/BC4-OTF) with 1^tCK Preamble and Write CRC in Same or Different Bank Group



- 1. BL8/BC4-OTF, AL = 0, CWL = 9, Preamble = 1^{t} CK, t CCD_S/L = 6^{t} CK.
- 2. DI n (or b) = data-in from column n (or column b).
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T6.
- 5. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T6.
- CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Disable.
- 7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T19.



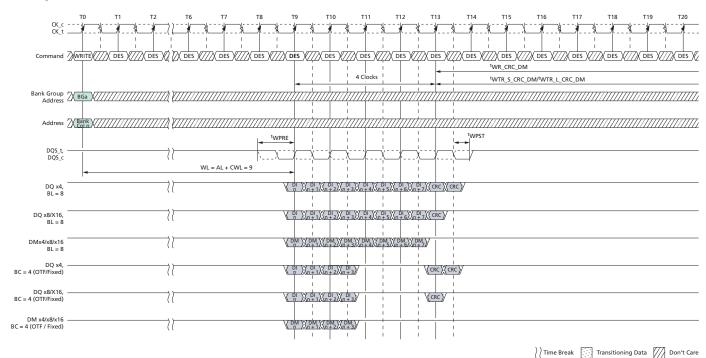
Figure 199: Nonconsecutive WRITE (BL8/BC4-OTF) with 2^tCK Preamble and Write CRC in Same or Different Bank Group



- 1. BL8/BC4-OTF, AL = 0, CWL = 9 + 1 = 10 (see Note 9), Preamble = 2^{t} CK, t CCD_S/L = 7^{t} CK (see Note 7).
- 2. DI n (or b) = data-in from column n (or column b).
- 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
- 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T7.
- 5. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T7.
- 6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Disable.
- 7. ${}^{t}CCD_{S/L} = 6{}^{t}CK$ is not allowed in $2{}^{t}CK$ preamble mode if minimum ${}^{t}CCD_{S/L}$ allowed in $1{}^{t}CK$ preamble mode would have been 6 clocks.
- 8. The write recovery time (^tWR) and write timing parameter (^tWTR) are referenced from the first rising clock edge after the last write data shown at T21.
- 9. When operating in 2^tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^tCK range. That means CWL = 9 is not allowed when operating in 2^tCK WRITE preamble mode.



Figure 200: WRITE (BL8/BC4-OTF/Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group



- Notes: 1. BL8/BC4, AL = 0, CWL = 9, Preamble = 1^{t} CK.
 - 2. DI n (or b) = data-in from column n (or column b).
 - 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 - 4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
 - 5. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during WRITE command at T0.
 - 6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Enable.
 - 7. The write recovery time (tWR_CRC_DM) and write timing parameter (tWTR_S_CRC_DM/ tWTR_L_CRC_DM) are referenced from the first rising clock edge after the last write data shown at T13.



Write Timing Violations

Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure that the device works properly. However, for certain minor violations, it is desirable that the device is guaranteed not to "hang up" and that errors are limited to that specific operation. A minor violation does not include a major timing violation (for example, when a DQS strobe misses in the ^tDQSCK window).

For the following, it will be assumed that there are no timing violations with regard to the WRITE command itself (including ODT, and so on) and that it does satisfy all timing requirements not mentioned below.

Data Setup and Hold Violations

If the data-to-strobe timing requirements (^tDS, ^tDH) are violated, for any of the strobe edges associated with a WRITE burst, then wrong data might be written to the memory location addressed with this WRITE command.

In the example, the relevant strobe edges for WRITE Burst A are associated with the clock edges: T5, T5.5, T6, T6.5, T7, T7.5, T8, and T8.5.

Subsequent reads from that location might result in unpredictable read data; however, the device will work properly otherwise.

Strobe-to-Strobe and Strobe-to-Clock Violations

If the strobe timing requirements ('DQSH, 'DQSL, 'WPRE, 'WPST) or the strobe to clock timing requirements ('DSS, 'DSH, 'DQSS) are violated, for any of the strobe edges associated with a WRITE burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data; however, the device will work properly otherwise with the following constraints:

- Both write CRC and data burst OTF are disabled; timing specifications other than ^tDQSH, ^tDQSL, ^tWPRE, ^tWPST, ^tDSS, ^tDSH, ^tDQSS are not violated.
- The offending write strobe (and preamble) arrive no earlier or later than six DQS transition edges from the WRITE latency position.
- A READ command following an offending WRITE command from any open bank is allowed.
- One or more subsequent WR or a subsequent WRA (to same bank as offending WR)
 may be issued ^tCCD_L later, but incorrect data could be written. Subsequent WR and
 WRA can be either offending or non-offending writes. Reads from these writes may
 provide incorrect data.
- One or more subsequent WR or a subsequent WRA (to a different bank group) may be issued ^tCCD_S later, but incorrect data could be written. Subsequent WR and WRA can be either offending or non-offending writes. Reads from these writes may provide incorrect data.
- After one or more precharge commands (PRE or PREA) are issued to the device after an offending WRITE command and all banks are in precharged state (idle state), a subsequent, non-offending WR or WRA to any open bank will be able to write correct data.



ZQ CALIBRATION Commands

A ZQ CALIBRATION command is used to calibrate DRAM $R_{\rm ON}$ and ODT values. The device needs a longer time to calibrate the output driver and on-die termination circuits at initialization and a relatively smaller time to perform periodic calibrations.

The ZQCL command is used to perform the initial calibration during the power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. The ZQCL command triggers the calibration engine inside the DRAM and, after calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM I/O, which is reflected as an updated output driver and ODT values.

The first ZQCL command issued after reset is allowed a timing period of ^tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after reset are allowed a timing period of ^tZQoper.

The ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter $^t ZQCS$. One ZQCS command can effectively correct a minimum of 0.5% (ZQ correction) of R_{ON} and R_{TT} impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the Output Driver and ODT Voltage and Temperature Sensitivity tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (T_{drift_rate}) and voltage (V_{drift_rate}) drift rates that the device is subjected to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQ}_{\text{correction}}}{(\text{T}_{\text{sense}} \times \text{T}_{\text{drift_rate}}) + (\text{V}_{\text{sense}} \times \text{T}_{\text{drift_rate}})}$$

Where T_{sense} = MAX($dR_{TT}dT$, $dR_{ON}dTM$) and V_{sense} = MAX($dR_{TT}dV$, $dR_{ON}dVM$) define the temperature and voltage sensitivities.

For example, if $T_{sens} = 1.5\%$ /°C, $V_{sens} = 0.15\%$ /mV, $T_{driftrate} = 1$ °C/sec and $V_{driftrate} = 15$ mV/sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128 \text{ms}$$

No other activities should be performed on the DRAM channel by the controller for the duration of ^tZQinit, ^tZQoper, or ^tZQCS. The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. After DRAM calibration is achieved, the device should disable the ZQ current consumption path to reduce power.

All banks must be precharged and ^tRP met before ZQCL or ZQCS commands are issued by the controller.

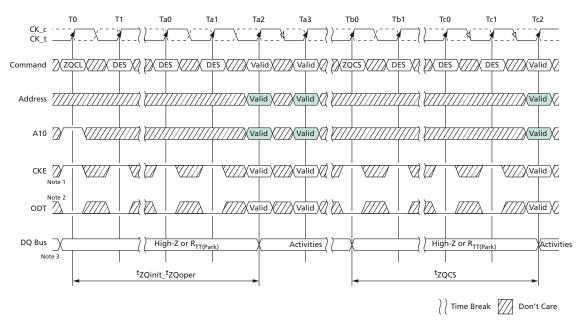
ZQ CALIBRATION commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon self refresh exit, the device will not perform an I/O cali-



bration without an explicit ZQ CALIBRATION command. The earliest possible time for a ZQ CALIBRATION command (short or long) after self refresh exit is ^tXS, ^tXS_Abort, or ^tXS_FAST depending on operation mode.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of ^tZQoper, ^tZQinit, or ^tZQCS between the devices.

Figure 201: ZQ Calibration Timing



Notes:

- 1. CKE must be continuously registered HIGH during the calibration procedure.
- 2. During ZQ calibration, the ODT signal must be held LOW and DRAM continues to provide RTT_PARK.
- 3. All devices connected to the DQ bus should be High-Z during the calibration procedure.

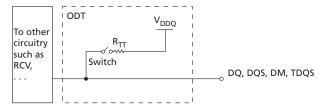


On-Die Termination

The on-die termination (ODT) feature enables the device to change termination resistance for each DQ, DQS, and DM_n/DBI_n signal for x4 and x8 configurations (and TDQS for the x8 configuration when enabled via A11 = 1 in MR1) via the ODT control pin, WRITE command, or default parking value with MR setting. For the x16 configuration, ODT is applied to each UDQ, LDQ, UDQS, LDQS, UDM_n/UDBI_n, and LDM_n/LDBI_n signal. The ODT feature is designed to improve the signal integrity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices. If DBI read mode is enabled while the DRAM is in standby, either DM mode or DBI write mode must also be enabled if $R_{\rm TT(NOM)}$ or $R_{\rm TT(Park)}$ is desired. More details about ODT control modes and ODT timing modes can be found further along in this document.

The ODT feature is turned off and not supported in self refresh mode.

Figure 202: Functional Representation of ODT



The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information. The value of R_{TT} is determined by the settings of mode register bits (see Mode Register). The ODT pin will be ignored if the mode register MR1 is programmed to disable $R_{TT(NOM)}$ [MR1[10,9,8] = 0,0,0] and in self refresh mode.

ODT Mode Register and ODT State Table

The ODT mode of the DDR4 device has four states: data termination disable, $R_{TT(NOM)}$, $R_{TT(WR)}$, and $R_{TT(Park)}$. The ODT mode is enabled if any of MR1[10:8] ($R_{TT(NOM)}$), MR2[11:9] ($R_{TT(WR)}$), or MR5[8:6] ($R_{TT(Park)}$) are non-zero. When enabled, the value of R_{TT} is determined by the settings of these bits.

R_{TT} control of each R_{TT} condition is possible with a WR or RD command and ODT pin.

- R_{TT(WR)}: The DRAM (rank) that is being written to provide termination regardless of ODT pin status (either HIGH or LOW).
- R_{TT(NOM)}: DRAM turns ON R_{TT(NOM)} if it sees ODT asserted HIGH (except when ODT is disabled by MR1).
- R_{TT(Park)}: Default parked value set via MR5 to be enabled and R_{TT(NOM)} is not turned on.
- The Termination State Table that follows shows various interactions.

The R_{TT} values have the following priority:

- Data termination disable
- R_{TT(WR)}
- R_{TT(NOM)}
- R_{TT(Park)}



Table 70: Termination State Table

Case	R _{TT(Park)}	R _{TT(NOM)} 1	R _{TT(WR)} ²	ODT Pin	ODT READS ³	ODT Stand- by ⁷	ODT WRITES
A ⁴	Disabled	Disabled	Disabled	Don't Care	Off (High-Z)	Off (High-Z)	Off (High-Z)
			Enabled	Don't Care	Off (High-Z)	Off (High-Z)	R _{TT(WR)}
B ⁵	Enabled	Disabled	Disabled	Don't Care	Off (High-Z)	R _{TT(Park)}	R _{TT(Park)}
			Enabled	Don't Care	Off (High-Z)	R _{TT(Park)}	R _{TT(WR)}
C ₆	Disabled	Enabled	Disabled	Low	Off (High-Z)	Off (High-Z)	Off (High-Z)
				High	Off (High-Z)	R _{TT(NOM)}	R _{TT(NOM)}
			Enabled	Low	Off (High-Z)	Off (High-Z)	R _{TT(WR)}
				High	Off (High-Z)	R _{TT(NOM)}	R _{TT(WR)}
D ₆	Enabled	Enabled	Disabled	Low	Off (High-Z)	R _{TT(Park)}	R _{TT(Park)}
				High	Off (High-Z)	R _{TT(NOM)}	R _{TT(NOM)}
			Enabled	Low	Off (High-Z)	R _{TT(Park)}	R _{TT(WR)}
				High	Off (High-Z)	R _{TT(NOM)}	R _{TT(WR)}

- Notes: 1. If R_{TT(NOM)} MR is disabled, power to the ODT receiver will be turned off to save power.
 - 2. If R_{TT(WR)} is enabled, R_{TT(WR)} will be activated by a WRITE command for a defined period time independent of the ODT pin and MR setting of R_{TT(Park)}/R_{TT(NOM)}. This is described in the Dynamic ODT section.
 - 3. When a READ command is executed, the DRAM termination state will be High-Z for a defined period independent of the ODT pin and MR setting of R_{TT(Park)}/R_{TT(NOM)}. This is described in the ODT During Read section.
 - 4. Case A is generally best for single-rank memories.
 - 5. Case B is generally best for dual-rank, single-slotted memories.
 - 6. Case C and Case D are generally best for multi-slotted memories.
 - 7. The ODT feature is turned off and not supported in self refresh mode.

ODT Read Disable State Table

Upon receiving a READ command, the DRAM driving data disables ODT after RL - (2 or 3) clock cycles, where $2 = 1^{t}CK$ preamble mode and $3 = 2^{t}CK$ preamble mode. ODT stays off for a duration of BL/2 + (2 or 3) + (0 or 1) clock cycles, where $2 = 1^{\text{t}}\text{CK}$ preamble mode, $3 = 2^{t}CK$ preamble mode, 0 = CRC disabled, and 1 = CRC enabled.

Table 71: Read Termination Disable Window

Pos condition	cnc.	Start ODT Disable After	Describes of ODT Disable
Preamble	CRC	Read	Duration of ODT Disable
1 ^t CK	Disabled	RL - 2	BL/2 + 2
	Enabled	RL - 2	BL/2 + 3
2 ^t CK	Disabled	RL - 3	BL/2 + 3
	Enabled	RL - 3	BL/2 + 4



Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes include the following:

- · Any bank active with CKE HIGH
- · Refresh with CKE HIGH
- · Idle mode with CKE HIGH
- Active power-down mode
- Precharge power-down mode

In synchronous ODT mode, R_{TT(NOM)} will be turned on DODTLon clock cycles after ODT is sampled HIGH by a rising clock edge and turned off DODTLoff clock cycles after ODT is registered LOW by a rising clock edge. The ODT latency is determined by the programmed values for: CAS WRITE latency (CWL), additive latency (AL), and parity latency (PL), as well as the programmed state of the preamble.

ODT Latency and Posted ODT

The ODT latencies for synchronous ODT mode are summarized in the table below. For details, refer to the latency definitions.

Table 72: ODT Latency at DDR4-1600/-1866/-2133/-2400/-2666/-3200

Applicable when write CRC is disabled

Symbol	Parameter	1 ^t CK Preamble	2 ^t CK Preamble	Unit
DODTLon	Direct ODT turn-on latency	CWL + AL + PL - 2	CWL + AL + PL - 3	^t CK
DODTLoff	Direct ODT turn-off latency	CWL + AL + PL - 2	CWL + AL + PL - 3	
RODTLoff	READ command to internal ODT turn-off latency	CL + AL + PL - 2	CL + AL + PL - 3	
RODTLon4	READ command to R _{TT(Park)} turn-on la- tency in BC4-fixed	RODTLoff + 4	RODTLoff + 5	
RODTLon8	READ command to R _{TT(Park)} turn-on la- tency in BL8/BC4-OTF	RODTLoff + 6	RODTLoff + 7	
ODTH4	ODT Assertion time, BC4 mode	4	5	
ODTH8	ODT Assertion time, BL8 mode	6	7	

Timing Parameters

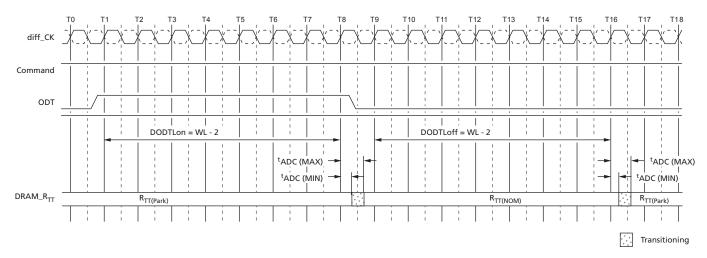
In synchronous ODT mode, the following parameters apply:

- DODTLon, DODTLoff, RODTLoff, RODTLon4, RODTLon8, and ^tADC (MIN)/(MAX).
- tADC (MIN) and tADC (MAX) are minimum and maximum R_{TT} change timing skew between different termination values. These timing parameters apply to both the synchronous ODT mode and the data termination disable mode.

When ODT is asserted, it must remain HIGH until minimum ODTH4 (BC = 4) or ODTH8 (BL = 8) is satisfied. If write CRC mode or 2^t CK preamble mode is enabled, ODTH should be adjusted to account for it. ODTHx is measured from ODT first registered HIGH to ODT first registered LOW or from the registration of a WRITE command.

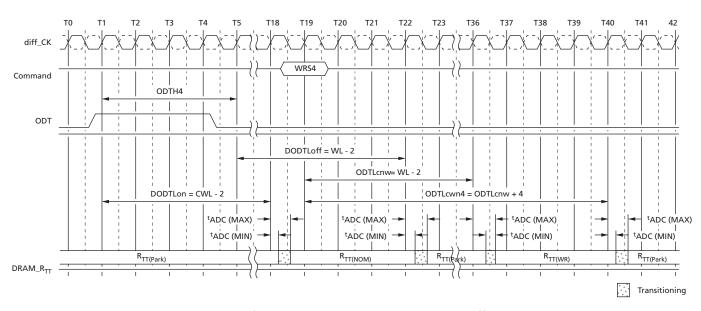


Figure 203: Synchronous ODT Timing with BL8



- Notes: 1. Example for CWL = 9, AL = 0, PL = 0; DODTLon = AL + PL + CWL 2 = 7; DODTLoff = AL + PL + CWL 2 = 7.
 - 2. ODT must be held HIGH for at least ODTH8 after assertion (T1).

Figure 204: Synchronous ODT with BC4



- Notes: 1. Example for CWL = 9, AL = 10, PL = 0; DODTLon/off = AL + PL + CWL 2 = 17; ODTcnw = AL + PL + CWL 2 = 17.
 - 2. ODT must be held HIGH for at least ODTH4 after assertion (T1).

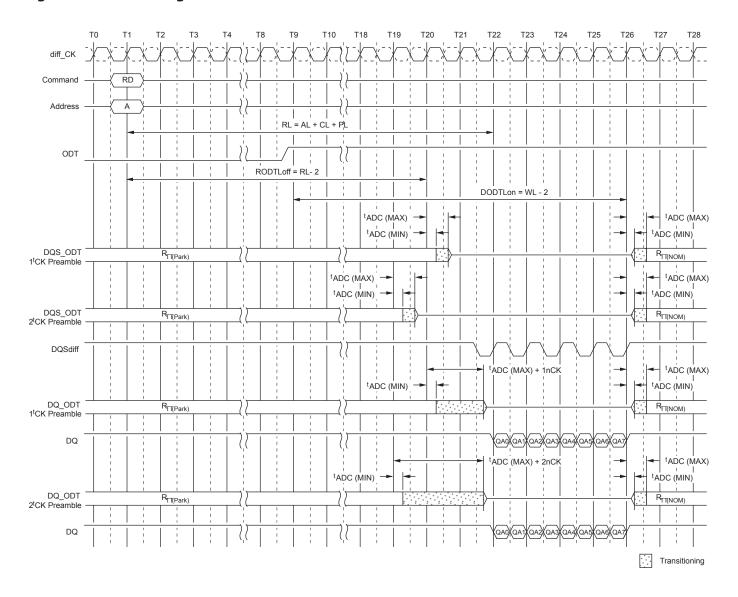


ODT During Reads

Because the DRAM cannot terminate with R_{TT} and drive with R_{ON} at the same time, R_{TT} may nominally not be enabled until the end of the postamble as shown in the example below. At cycle T26 the device turns on the termination when it stops driving, which is determined by ${}^{t}HZ$. If the DRAM stops driving early (that is, ${}^{t}HZ$ is early), then ${}^{t}ADC$ (MIN) timing may apply. If the DRAM stops driving late (that is, ${}^{t}HZ$ is late), then the DRAM complies with ${}^{t}ADC$ (MAX) timing.

Using CL = 11 as an example for the figure below: PL = 0, AL = CL - 1 = 10, RL = PL + AL + CL = 21, CWL = 9; RODTLoff = RL - 2 = 19, DODTLon = PL + AL + CWL - 2 = 17, 1^tCK preamble.

Figure 205: ODT During Reads





Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the device can be changed without issuing an MRS command. This requirement is supported by the dynamic ODT feature.

Functional Description

Dynamic ODT mode is enabled if bit A9 or A10 of MR2 is set to 1.

- Three R_{TT} values are available: R_{TT(NOM)}, R_{TT(WR)}, and R_{TT(Park)}.
- The value for R_{TT(NOM)} is preselected via bits MR1[10:8].
- The value for $R_{TT(WR)}$ is preselected via bits MR2[11:9].
- The value for R_{TT(Park)} is preselected via bits MR5[8:6].
- During operation without WRITE commands, the termination is controlled as follows:
 - Nominal termination strength R_{TT(NOM)} or R_{TT(Park)} is selected.
- R_{TT(NOM)} on/off timing is controlled via ODT pin and latencies DODTLon and DODTLoff, and R_{TT(Park)} is on when ODT is LOW.
- When a WRITE command (WR, WRA, WRS4, WRS8, WRAS4, and WRAS8) is registered, and if dynamic ODT is enabled, the termination is controlled as follows:
 - Latency ODTLcnw after the WRITE command, termination strength $R_{\rm TT(WR)}$ is selected.
 - Latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the WRITE command, termination strength R_{TT(WR)} is de-selected.

One or two clocks will be added into or subtracted from ODTLcwn8 and ODTLcwn4, depending on write CRC mode and/or 2^tCK preamble enablement.

The following table shows latencies and timing parameters relevant to the on-die termination control in dynamic ODT mode. The dynamic ODT feature is not supported in DLL-off mode. An MRS command must be used to set $R_{TT(WR)}$ to disable dynamic ODT externally (MR2[11:9] = 000).

Table 73: Dynamic ODT Latencies and Timing (1^tCK Preamble Mode and CRC Disabled)

Name and Description	Abbr.	Defined from	Defined to	1600/1866/ 2133/2400	2666	2933/3200	Unit	
ODT latency for change from R _{TT(Park)} /	ODTLc nw	Registering ex- ternal WRITE	Change R_{TT} strength from	1	ODTLcnw = WL - 2			
R _{TT(NOM)} to R _{TT(WR)}		command	$R_{TT(Park)}$ / $R_{TT(NOM)}$ to $R_{TT(WR)}$					
ODT latency for change from $R_{TT(WR)}$ to $R_{TT(Park)}/R_{TT(NOM)}$ (BC =	ODTLc wn4	Registering ex- ternal WRITE command	Change R _{TT} strength from R _{TT(WR)} to	ODTLcwn4 = 4 + ODTLcnw		.cnw	^t CK	
4)			R _{TT(Park)} / R _{TT(NOM)}					
ODT latency for change from R _{TT(WR)} to	ODTLc wn8	Registering ex- ternal WRITE	Change R _{TT} strength from	ODT	Lcwn8 = 6 + ODTL	.cnw	^t CK (AVG)	
$R_{TT(Park)}/R_{TT(NOM)}$ (BL = 8)		command	$R_{TT(NOM)}$ to $R_{TT(WR)}$					



Table 73: Dynamic ODT Latencies and Timing (1^tCK Preamble Mode and CRC Disabled) (Continued)

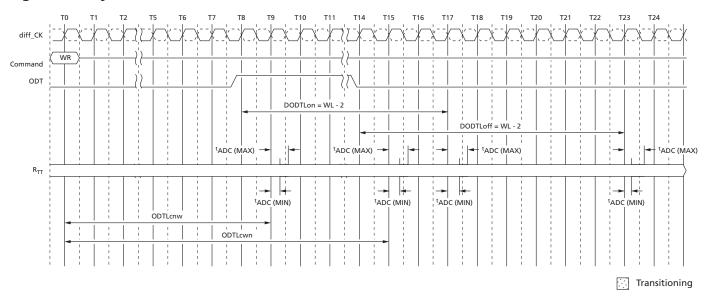
Name and Descrip-				1600/1866/			
tion	Abbr.	Defined from	Defined to	2133/2400	2666	2933/3200	Unit
R _{TT} change skew	^t ADC	ODTLcnw	R _{TT} valid	^t ADC (MIN) =	tADC (MIN) =	^t ADC (MIN) =	^t CK
		ODTLcwn		0.30	0.28	0.26	(AVG)
				^t ADC (MAX) =	$^{t}ADC (MAX) =$	^t ADC (MAX) =	
				0.70	0.72	0.74	

Table 74: Dynamic ODT Latencies and Timing with Preamble Mode and CRC Mode Matrix

	1 ^t CK Pa	rameter	2 ^t CK Pa	2 ^t CK Parameter		
Symbol	CRC Off	CRC On	CRC Off	CRC On	Unit	
ODTLcnw ¹	WL - 2	WL - 2	WL - 3	WL - 3	^t CK	
ODTLcwn4	ODTLcnw + 4	ODTLcnw + 7	ODTLcnw + 5	ODTLcnw + 8		
ODTLcwn8	ODTLcnw + 6	ODTLcnw + 7	ODTLcnw + 7	ODTLcnw + 8		

Note: 1. ODTLcnw = WL - 2 (1^tCK preamble) or WL - 3 (2^tCK preamble).

Figure 206: Dynamic ODT (1^t CK Preamble; CL = 14, CWL = 11, BL = 8, AL = 0, CRC Disabled)

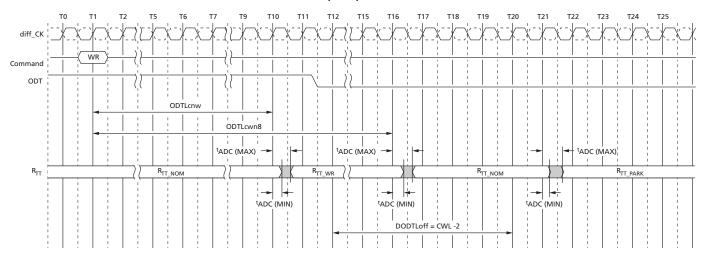


Notes: 1. ODTLcnw = WL - 2 (1^tCK preamble) or WL - 3 (2^tCK preamble).

2. If BC4, then ODTLcwn = WL + 4 if CRC disabled or WL + 5 if CRC enabled; If BL8, then ODTLcwn = WL + 6 if CRC disabled or WL + 7 if CRC enabled.



Figure 207: Dynamic ODT Overlapped with $R_{TT(NOM)}$ (CL = 14, CWL = 11, BL = 8, AL = 0, CRC Disabled)



Note: 1. Behavior with WR command issued while ODT is registered HIGH.



Asynchronous ODT Mode

Asynchronous ODT mode is selected when the DRAM runs in DLL-off mode. In asynchronous ODT timing mode, the internal ODT command is *not* delayed by either additive latency (AL) or the parity latency (PL) relative to the external ODT signal (R_{TT(NOM)}). In asynchronous ODT mode, two timing parameters apply: ^tAONAS (MIN/MAX), and ^tAOFAS (MIN/MAX).

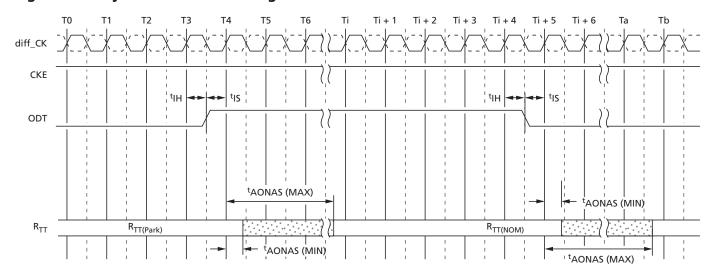
R_{TT(NOM)} Turn-on Time

- Minimum $R_{TT(NOM)}$ turn-on time (tAONAS [MIN]) is when the device termination circuit leaves $R_{TT(Park)}$ and ODT resistance begins to turn on.
- Maximum $R_{TT(NOM)}$ turn-on time (^tAONAS [MAX]) is when the ODT resistance has reached $R_{TT(NOM)}$.
- tAONAS (MIN) and tAONAS (MAX) are measured from ODT being sampled HIGH.

R_{TT(NOM)} Turn-off Time

- Minimum $R_{TT(NOM)}$ turn-off time (tAOFAS [MIN]) is when the device's termination circuit starts to leave $R_{TT(NOM)}$.
- Maximum R_{TT(NOM)} turn-off time (^tAOFAS [MAX]) is when the on-die termination has reached R_{TT(Park)}.
- tAOFAS (MIN) and tAOFAS (MAX) are measured from ODT being sampled LOW.

Figure 208: Asynchronous ODT Timings with DLL Off



Transitioning



Electrical Specifications

Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability. Although "unlimited" row accesses to the same row is allowed within the refresh period; excessive row accesses to the same row over a long term can result in degraded operation.

Table 75: Absolute Maximum Ratings

Symbol	Parameter	Min	Мах	Unit	Notes
V _{DD}	Voltage on V _{DD} pin relative to V _{SS}	-0.4	1.5	V	1
V _{DDQ}	Voltage on V _{DDQ} pin relative to V _{SS}	-0.4	1.5	V	1
V _{PP}	Voltage on V _{PP} pin relative to V _{SS}	-0.4	3.0	V	3
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.4	1.5	V	
T _{STG}	Storage temperature	-55	150	°C	2

Notes:

- 1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than $0.6 \times V_{DDQ}$. When V_{DD} and V_{DDQ} are <500mV, V_{REF} can be ≤300mV.
- 2. Storage temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to the JESD51-2 standard.
- 3. V_{PP} must be equal to or greater than V_{DD}/V_{DDO} at all times when powered.

DRAM Component Operating Temperature Range

Operating temperature, T_{OPER} , is the case surface temperature on the center/top side of the DRAM. For measurement conditions, refer to the JEDEC document JESD51-2.

Table 76: Temperature Range

Symbol	nbol Parameter		Max	Unit	Notes
T_{OPER}	Normal operating temperature range	-40	85	°C	1
	Extended temperature range (optional)	>85	105	°C	2

Notes

- 1. The normal temperature range specifies the temperatures at which all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to 85°C under all operating conditions for the commercial offering; The industrial and automotive temperature offerings allow the case temperature to go below 0°C to -40°C.
- 2. Some applications require operation of the commercial, industrial, and automotive temperature DRAMs in the extended temperature range (between 85°C and 105°C case temperature). Full specifications are supported in this range, but the following additional conditions apply:
 - Refer to tREFI and tRFC parameters table for tREFI requirements when operating above 85°C
 - If SELF REFRESH operation is required in the extended temperature range, it is mandatory to use either the manual self refresh mode with extended temperature range ca-

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pability (MR2[6] = 0 and MR2 [7] = 1) or enable the optional auto self refresh mode (MR2 [6] = 1 and MR2 [7] = 1).

Electrical Characteristics – AC and DC Operating Conditions

Supply Operating Conditions

Table 77: Recommended Supply Operating Conditions

			Rating			
Symbol	Parameter	Min	Тур	Max	Unit	Notes
V _{DD}	Supply voltage	1.14	1.2	1.26	V	1, 2, 3, 4, 5
V_{DDQ}	Supply voltage for output	1.14	1.2	1.26	V	1, 2, 6
V _{PP}	Wordline supply voltage	2.375	2.5	2.750	V	7

- Notes: 1. Under all conditions V_{DDQ} must be less than or equal to V_{DD} .
 - 2. V_{DDQ} tracks with V_{DD} . AC parameters are measured with V_{DD} and V_{DDQ} tied together.
 - 3. V_{DD} slew rate between 300mV and 80% of $V_{DD,min}$ shall be between 0.004 V/ms and 600 V/ms, 20 MHz band-limited measurement.
 - 4. V_{DD} ramp time from 300mV to V_{DD.min} shall be no longer than 200ms.
 - 5. A stable valid V_{DD} level is a set DC level (0 Hz to 250 KHz) and must be no less than $V_{DD,min}$ and no greater than $V_{DD,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is final. AC noise of ± 60 mV (greater than 250 KHz) is allowed on V_{DD} provided the noise doesn't alter V_{DD} to less than $V_{DD,min}$ or greater than $V_{DD,max}$.
 - 6. A stable valid V_{DDO} level is a set DC level (0 Hz to 250 KHz) and must be no less than V_{DDQ,min} and no greater than V_{DDQ,max}. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is final. AC noise of ±60mV (greater than 250 KHz) is allowed on V_{DDO} provided the noise doesn't alter V_{DDQ} to less than $V_{DDQ,min}$ or greater than $V_{DDQ,max}$.
 - 7. A stable valid V_{PP} level is a set DC level (0 Hz to 250 KHz) and must be no less than V_{PP,min} and no greater than V_{PP,max}. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is final. AC noise of ± 120 mV (greater than 250 KHz) is allowed on V_{PP} provided the noise doesn't alter V_{PP} to less than V_{PP.min} or greater than V_{PP.max}.

Table 78: V_{DD} Slew Rate

Symbol	Min	Max	Unit	Notes
V_{DD_sl}	0.004	600	V/ms	1, 2
V_{DD_on}	_	200	ms	3

- Notes: 1. Measurement made between 300mV and 80% V_{DD} (minimum level).
 - 2. The DC bandwidth is limited to 20 MHz.
 - 3. Maximum time to ramp V_{DD} from 300 mV to V_{DD} minimum.

Leakages

Table 79: Leakages

Condition	Symbol	Min	Max	Unit	Notes
Input leakage (excluding ZQ and TEN)	I _{IN}	-2	2	μA	1
ZQ leakage	I _{ZQ}	-50	10	μA	1
TEN leakage	I _{TEN}	-6	10	μA	1, 2
V _{REFCA} leakage	I _{VREFCA}	-2	2	μA	3
Output leakage: V _{OUT} = V _{DDQ}	I _{OZpd}	_	10	μΑ	4
Output leakage: V _{OUT} = V _{SSQ}	I _{OZpu}	-50	_	μΑ	4, 5

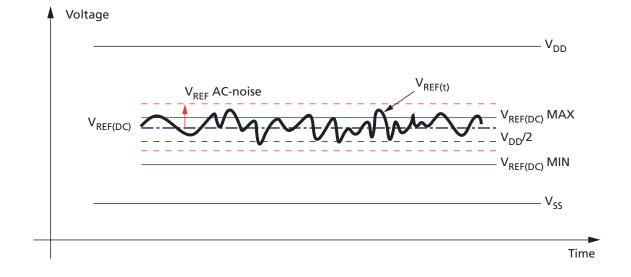
- Notes: 1. Input under test $0V < V_{IN} < 1.1V$.
 - 2. Additional leakage due to weak pull-down.
 - 3. $V_{REFCA} = V_{DD}/2$, V_{DD} at valid level after initialization.
 - 4. DQs are disabled.
 - 5. ODT is disabled with the ODT input HIGH.

V_{REFCA} Supply

 V_{REFCA} is to be supplied to the DRAM and equal to $V_{DD}/2$. The V_{REFCA} is a reference supply input and therefore does not draw biasing current.

The DC-tolerance limits and AC-noise limits for the reference voltages V_{REFCA} are illustrated in the figure below. The figure shows a valid reference voltage $V_{\text{REF}(t)}$ as a function of time (V_{REF} stands for V_{REF(DC)} is the linear average of V_{REF(t)} over a very long period of time (1 second). This average has to meet the MIN/MAX requirements. Furthermore, $V_{REF(t)}$ may temporarily deviate from $V_{REF(DC)}$ by no more than $\pm 1\%$ V_{DD} for the AC-noise limit.

Figure 209: V_{REFDO} Voltage Range





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The voltage levels for setup and hold time measurements are dependent on V_{REF} . V_{REF} is understood as V_{REF(DC)}, as defined in the above figure. This clarifies that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid HIGH or LOW level, and therefore, the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{\text{REF}(DC)}$ deviations from the optimum position within the data-eye of the input signals. This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (±1% of V_{DD}) are included in DRAM timings and their associated deratings.

V_{REFDQ} Supply and Calibration Ranges

The device internally generates its own V_{REFDO} . DRAM internal V_{REFDO} specification parameters: voltage range, step size, V_{REF} step time, V_{REF} full step time, and V_{REF} valid level are used to help provide estimated values for the internal V_{REFDO} and are not pass/fail limits. The voltage operating range specifies the minimum required range for DDR4 SDRAM devices. The minimum range is defined by V_{REFDO,min} and V_{REFDO,max}. A calibration sequence should be performed by the DRAM controller to adjust V_{REFDO} and optimize the timing and voltage margin of the DRAM data input receivers.

Table 80: V_{REFDO} Specification

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Range 1 V _{REFDQ} operating points	V _{REFDQ} R1	60%	_	92%	V_{DDQ}	1, 2
Range 2 V _{REFDQ} operating points	V _{REFDQ} R2	45%	_	77%	V_{DDQ}	1, 2
V _{REF} step size	V _{REF,step}	0.5%	0.65%	0.8%	V_{DDQ}	3
V _{REF} set tolerance	V _{REF,set_tol}	-1.625%	0%	1.625%	V_{DDQ}	4, 5, 6
		-0.15%	0%	0.15%	V_{DDQ}	4, 7, 8
V _{REF} step time	V _{REF,time}	-	_	150	ns	9, 10, 11
V _{REF} valid tolerance	V _{REF_val_tol}	-0.15%	0%	0.15%	V_{DDQ}	12

- Notes: 1. $V_{REF(DC)}$ voltage is referenced to $V_{DDQ(DC)}$. $V_{DDQ(DC)}$ is 1.2V.
 - 2. DRAM range 1 or range 2 is set by the MRS6[6]6.
 - 3. V_{REF} step size increment/decrement range. V_{REF} at DC level.
 - 4. $V_{REF,new} = V_{REF,old} \pm n \times V_{REF,step}$; n = number of steps. If increment, use "+," if decrement, use "-."
 - 5. For n >4, the minimum value of V_{REF} setting tolerance = $V_{REF,new}$ 1.625% \times V_{DDQ} . The maximum value of V_{REF} setting tolerance = $V_{REF,new}$ + 1.625% × V_{DDQ} .
 - 6. Measured by recording the MIN and MAX values of the V_{RFF} output over the range, drawing a straight line between those points, and comparing all other VRFF output settings to that line.
 - 7. For n \leq 4, the minimum value of V_{REF} setting tolerance = $V_{REF,new}$ 0.15% \times V_{DDQ} . The maximum value of V_{REF} setting tolerance = $V_{REF,new}$ + 0.15% × V_{DDQ} .
 - 8. Measured by recording the MIN and MAX values of the V_{REF} output across four consecutive steps (n = 4), drawing a straight line between those points, and comparing all V_{RFF} output settings to that line.
 - 9. Time from MRS command to increment or decrement one step size for V_{REF}.
 - 10. Time from MRS command to increment or decrement more than one step size up to the full range of V_{RFF}.
 - 11. If the V_{REF} monitor is enabled, V_{REF} must be derated by +10ns if DQ bus load is 0pF and an additional +15 ns/pF of DQ bus loading.



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Only applicable for DRAM component-level test/characterization purposes. Not applicable for normal mode of operation. V_{REF} valid qualifies the step times, which will be characterized at the component level.

V_{REFDQ} Ranges

MR6[6] selects range 1 (60% to 92.5% of V_{DDQ}) or range 2 (45% to 77.5% of V_{DDQ}), and MR6[5:0] sets the V_{REFDQ} level, as listed in the following table. The values in MR6[6:0] will update the V_{DDQ} range and level independent of MR6[7] setting. It is recommended MR6[7] be enabled when changing the settings in MR6[6:0], and it is highly recommended MR6[7] be enabled when changing the settings in MR6[6:0] multiple times during a calibration routine.

Table 81: V_{REFDQ} Range and Levels

BADCIT-01	MR6[6] 0 =	MR6[6] 1 =	MDC[F-0]	MR6[6] 0 =	MR6[6] 1 =
MR6[5:0]	Range 1	Range 2	MR6[5:0]	Range 1	Range 2
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%		11 0011 to 11 1111 are	reserved



Electrical Characteristics – AC and DC Single-Ended Input Measurement Levels

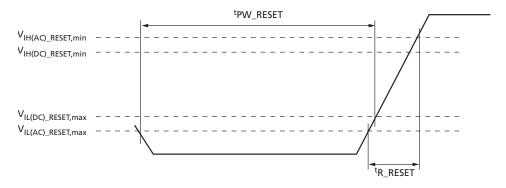
RESET_n Input Levels

Table 82: RESET n Input Levels (CMOS)

Parameter	Symbol	Min	Max	Unit	Note
AC input high voltage	V _{IH(AC)_RESET}	0.8 × V _{DD}	V _{DD}	V	1
DC input high voltage	V _{IH(DC)_RESET}	$0.7 \times V_{DD}$	V _{DD}	V	2
DC input low voltage	V _{IL(DC)_RESET}	V _{SS}	$0.3 \times V_{DD}$	V	3
AC input low voltage	V _{IL(AC)_RESET}	V _{SS}	0.2 × V _{DD}	V	4
Rising time	tR_RESET	_	1	μs	5
RESET pulse width after power-up	tPW_RESET_S	1	_	μs	6, 7
RESET pulse width during power-up	^t PW_RESET_L	200	_	μs	6

- Notes: 1. Overshoot should not exceed the V_{IN} shown in the Absolute Maximum Ratings table.
 - 2. After RESET_n is registered HIGH, the RESET_n level must be maintained above V_{IH(DC)} RESET, otherwise operation will be uncertain until it is reset by asserting RESET_n signal LOW.
 - 3. After RESET_n is registered LOW, the RESET_n level must be maintained below V_{IL(DC) RE-} SET during ^tPW_RESET, otherwise the DRAM may not be reset.
 - 4. Undershoot should not exceed the V_{IN} shown in the Absolute Maximum Ratings table.
 - 5. Slope reversal (ring-back) during this level transition from LOW to HIGH should be mitigated as much as possible.
 - 6. RESET is destructive to data contents.
 - 7. See RESET Procedure at Power Stable Condition figure.

Figure 210: RESET_n Input Slew Rate Definition



Command/Address Input Levels

Table 83: Command and Address Input Levels: DDR4-1600 Through DDR4-2400

Parameter	Symbol	Min	Max	Unit	Note
AC input high voltage	V _{IH(AC)}	V _{REF} + 100	V _{DD} 5	mV	1, 2, 3
DC input high voltage	V _{IH(DC)}	V _{REF} + 75	V_{DD}	mV	1, 2

Table 83: Command and Address Input Levels: DDR4-1600 Through DDR4-2400 (Continued)

Parameter	Symbol	Min	Max	Unit	Note
DC input low voltage	$V_{IL(DC)}$	V _{SS}	V _{REF} - 75	mV	1, 2
AC input low voltage	V _{IL(AC)}	V _{SS} 5	V _{REF} - 100	mV	1, 2, 3
Reference voltage for CMD/ADDR inputs	V _{REFFCA(DC)}	0.49 × V _{DD}	0.51 × V _{DD}	V	4

- Notes: 1. For input except RESET_n. $V_{REF} = V_{REFCA(DC)}$.
 - 2. $V_{REF} = V_{REFCA(DC)}$.
 - 3. Input signal must meet V_{IL}/V_{IH(AC)} to meet ^tIS timings and V_{IL}/V_{IH(DC)} to meet ^tIH timings.
 - 4. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REFCA(DC)}$ by more than $\pm 1\%$ V_{DD} (for reference: approximately ± 12 mV).
 - 5. Refer to "Overshoot and Undershoot Specifications."

Table 84: Command and Address Input Levels: DDR4-2666

Parameter	Symbol	Min	Max	Unit	Note
AC input high voltage	V _{IH(AC)}	V _{REF} + 90	V _{DD} 5	mV	1, 2, 3
DC input high voltage	V _{IH(DC)}	V _{REF} + 65	V_{DD}	mV	1, 2
DC input low voltage	V _{IL(DC)}	V _{SS}	V _{REF} - 65	mV	1, 2
AC input low voltage	V _{IL(AC)}	V _{SS} 5	V _{REF} - 90	mV	1, 2, 3
Reference voltage for CMD/ADDR inputs	V _{REFFCA(DC)}	0.49 × V _{DD}	0.51 × V _{DD}	V	4

- Notes: 1. For input except RESET_n. $V_{REF} = V_{REFCA(DC)}$.
 - 2. $V_{REF} = V_{REFCA(DC)}$.
 - 3. Input signal must meet V_{IL}/V_{IH(AC)} to meet ^tIS timings and V_{IL}/V_{IH(DC)} to meet ^tIH timings.
 - 4. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REFCA(DC)} by more than ±1% V_{DD} (for reference: approximately ±12mV).
 - 5. Refer to "Overshoot and Undershoot Specifications."

Table 85: Command and Address Input Levels: DDR4-2933 and DDR4-3200

Parameter	Symbol	Min	Max	Unit	Note
AC input high voltage	V _{IH(AC)}	V _{REF} + 90	V _{DD} 5	mV	1, 2, 3
DC input high voltage	V _{IH(DC)}	V _{REF} + 65	V_{DD}	mV	1, 2
DC input low voltage	V _{IL(DC)}	V _{SS}	V _{REF} - 65	mV	1, 2
AC input low voltage	V _{IL(AC)}	V _{SS} 5	V _{REF} - 90	mV	1, 2, 3
Reference voltage for CMD/ADDR inputs	V _{REFFCA(DC)}	0.49 × V _{DD}	0.51 × V _{DD}	V	4

- Notes: 1. For input except RESET_n. $V_{REF} = V_{REFCA(DC)}$.
 - 2. $V_{REF} = V_{REFCA(DC)}$.
 - 3. Input signal must meet $V_{IL}/V_{IH(AC)}$ to meet ^tIS timings and $V_{IL}/V_{IH(DC)}$ to meet ^tIH timings.
 - 4. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REFCA(DC)}$ by more than ±1% V_{DD} (for reference: approximately ±12mV).
 - 5. Refer to "Overshoot and Undershoot Specifications."

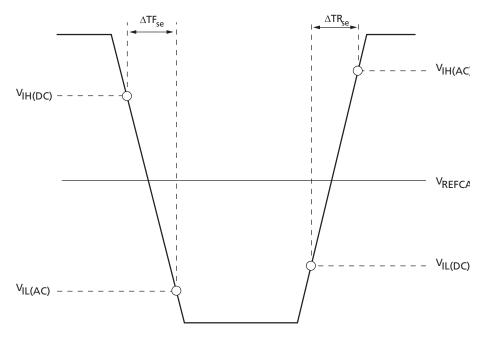
Table 86: Single-Ended Input Slew Rates

Parameter	Symbol	Min	Мах	Unit	Note
Single-ended input slew rate – CA	SR _{CA}	1.0	7.0	V/ns	1, 2, 3, 4

Notes: 1. For input except RESET_n.

- 2. $V_{REF} = V_{REFCA(DC)}$.
- 3. ${}^{t}IS/{}^{t}IH$ timings assume $SR_{CA} = 1V/ns$.
- 4. Measured between $V_{IH(AC)}$ and $V_{IL(AC)}$ for falling edges and between $V_{IL(AC)}$ and $V_{IH(AC)}$ for rising edges

Figure 211: Single-Ended Input Slew Rate Definition



Command, Control, and Address Setup, Hold, and Derating

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached $V_{\rm IH(AC)}/V_{\rm IL(AC)}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach $V_{\rm IH(AC)}/V_{\rm IL(AC)}.$ For slew rates that fall between the values listed in derating tables, the derating values may be obtained by linear interpolation.

Setup (${}^{t}IS$) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{IH(AC)min}$ that does not ring back below $V_{IH(DC)min}$. Setup (${}^{t}IS$) nominal slew rate for a falling signal is defined as the slew



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rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{IL(AC)max}$ that does not ring back above $V_{IL(DC)max}. \\$

 $Hold \ (^{t}IH) \ nominal \ slew \ rate \ for \ a \ rising \ signal \ is \ defined \ as \ the \ slew \ rate \ between \ the \ last \ crossing \ of \ V_{IL(DC)max} \ and \ the \ first \ crossing \ of \ V_{IH(AC)min} \ that \ does \ not \ ring \ back \ below \ V_{IH(DC)min}. \ Hold \ (^{t}IH) \ nominal \ slew \ rate \ for \ a \ falling \ signal \ is \ defined \ as \ the \ slew \ rate \ between \ the \ last \ crossing \ of \ V_{IL(AC)min} \ that \ does \ not \ ring \ back \ above \ V_{IL(DC)max}.$

Table 87: Command and Address Setup and Hold Values Referenced - AC/DC-Based

Symbol	1600	1866	2133	2400	2666	2933	3200	Unit	Reference
^t IS(base, AC100)	115	100	80	62	_	_	_	ps	$V_{IH(AC)}/V_{IL(AC)}$
^t IH(base, DC75)	140	125	105	87	-	_	_	ps	$V_{IH(DC)}/V_{IL(DC)}$
^t IS(base, AC90)	_	_	_	_	55	48	40	ps	V _{IH(AC)} /V _{IL(AC)}
^t IH(base, DC65)	-	_	-	-	80	73	65	ps	V _{IH(DC)} /V _{IL(DC)}
tIS/tIH(Vref)	215	200	180	162	145	138	130	ps	$V_{IH(DC)}/V_{IL(DC)}$

Table 88: Derating Values for tIS/tIH - AC100DC75-Based

	$\Delta^{ m t}$ IS with AC100 Threshold, $\Delta^{ m t}$ IH with DC75 Threshold Derating (ps) – AC/DC-Based															
CMD/						CK,	CK# E	iffere	ntial S	lew Ra	ite					
ADDR	10.0	V/ns	8.0 V/ns		6.0 V/ns		4.0	4.0 V/ns		V/ns	2.0 V/ns		1.5 V/ns		1.0 V/ns	
Slew Rate V/ns	Δ ^t IS	Δ ^t IH	Δ ^t IS	Δ ^t IH	Δ ^t IS	Δ ^t IH	Δ ^t IS	Δ ^t IH	Δ ^t IS	Δ ^t IH	Δ ^t IH	Δ ^t IH	Δ ^t IS	Δ ^t IH	Δ ^t IS	Δ ^t IH
7.0	76	54	76	55	77	56	79	58	82	60	86	64	94	73	111	89
6.0	73	53	74	53	75	54	77	56	79	58	83	63	92	71	108	88
5.0	70	50	71	51	72	52	74	54	76	56	80	60	88	68	105	85
4.0	65	46	66	47	67	48	69	50	71	52	75	56	83	65	100	81
3.0	57	40	57	41	58	42	60	44	63	46	67	50	75	58	92	75
2.0	40	28	41	28	42	29	44	31	46	33	50	38	58	46	75	63
1.5	23	15	24	16	25	17	27	19	29	21	33	25	42	33	58	50
1.0	-10	-10	-9	-9	-8	-8	-6	-6	-4	-4	0	0	8	8	25	25
0.9	-17	-14	-16	-14	-15	-13	-13	-10	-11	-8	-7	-4	1	4	18	21
0.8	-26	-19	-25	-19	-24	-18	-22	-16	-20	-14	-16	-9	-7	-1	9	16
0.7	-37	-26	-36	-25	-35	-24	-33	-22	-31	-20	-27	-16	-18	-8	-2	9
0.6	-52	-35	-51	-34	-50	-33	-48	-31	-46	-29	-42	-25	-33	-17	-17	0
0.5	-73	-48	-72	-47	-71	-46	-69	-44	-67	-42	-63	-38	-54	-29	-38	-13
0.4	-104	-66	-103	-66	-102	-65	-100	-63	-98	-60	-94	-56	-85	-48	-69	-31

Table 89: Derating Values for ^tIS/^tIH - AC90/DC65-Based

	$\Delta^{ m t}$ IS with AC90 Threshold, $\Delta^{ m t}$ IH with DC65 Threshold Derating (ps) – AC/DC-Based															
CMD/		CK, CK# Differential Slew Rate														
ADDR	10.0	V/ns	8.0	8.0 V/ns 6		V/ns	4.0	4.0 V/ns		V/ns	2.0 V/ns		1.5 V/ns		1.0	V/ns
Slew Rate V/ns	Δ ^t IS	Δ ^t IH	Δ ^t IS	Δ ^t IH	Δ ^t IS	Δ ^t IH	Δ ^t IS	Δ ^t IH	Δ ^t IS	Δ ^t IH	Δ ^t IH	Δ ^t IH	Δ ^t IS	Δ ^t IH	Δ ^t IS	Δ ^t IH
7.0	68	47	69	47	70	48	72	50	73	52	77	56	85	63	100	78
6.0	66	45	67	46	68	47	69	49	71	50	75	54	83	62	98	77
5.0	63	43	64	44	65	45	66	46	68	48	72	52	80	60	95	75
4.0	59	40	59	40	60	41	62	43	64	45	68	49	75	56	90	71
3.0	51	34	52	35	53	36	54	38	56	40	60	43	68	51	83	66
2.0	36	24	37	24	38	25	39	27	41	29	45	33	53	40	68	55
1.5	21	13	22	13	23	14	24	16	26	18	30	22	38	29	53	44
1.0	-9	-9	-8	-8	-8	-8	-6	-6	-4	-4	0	0	8	8	23	23
0.9	-15	-13	-15	-12	-14	-11	-12	-9	-10	-7	-6	-4	1	4	16	19
0.8	-23	-17	-23	-17	-22	-16	-20	-14	-18	-12	-14	-8	-7	-1	8	14
0.7	-34	-23	-33	-22	-32	-21	-30	-20	-28	-18	-25	-14	-17	-6	-2	9
0.6	-47	-31	-47	-30	-46	-29	-44	-27	-42	-25	-38	-22	-31	-14	-16	1
0.5	-67	-42	-66	-41	-65	-40	-63	-38	-61	-36	-58	-33	-50	-25	-35	-10
0.4	-95	-58	-95	-57	-94	-56	-92	-54	-90	-53	-86	-49	-79	-41	-64	-26

Data Receiver Input Requirements

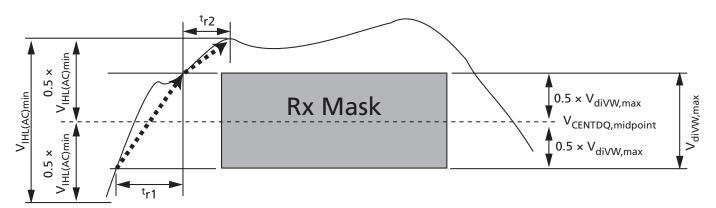
The following parameters apply to the data receiver Rx MASK operation detailed in the Write Timing section, Data Strobe-to-Data Relationship.

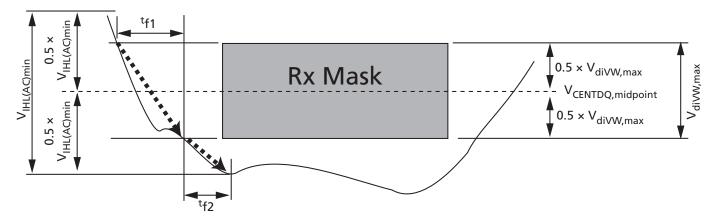
The rising edge slew rates are defined by srr1 and srr2. The slew rate measurement points for a rising edge are shown in the figure below. A LOW-to-HIGH transition time, tr1, is measured from $0.5 \times V_{diVW,max}$ below $V_{CENTDQ,midpoint}$ to the last transition through $0.5 \times V_{diVW,max}$ above $V_{CENTDQ,midpoint}$; tr2 is measured from the last transition through $0.5 \times V_{diVW,max}$ above $V_{CENTDQ,midpoint}$ to the first transition through the $0.5 \times V_{IHL(AC)min}$ above $V_{CENTDQ,midpoint}$.

The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in the figure below. A HIGH-to-LOW transition time, tf1, is measured from $0.5 \times V_{diVW,max}$ above $V_{CENTDQ,midpoint}$ to the last transition through $0.5 \times V_{diVW,max}$ below $V_{CENTDQ,midpoint}$; tf2 is measured from the last transition through $0.5 \times V_{diVW,max}$ below $V_{CENTDQ,midpoint}$ to the first transition through the $0.5 \times V_{IHL(AC)min}$ below $V_{CENTDQ,midpoint}$.



Figure 212: DQ Slew Rate Definitions





- Notes: 1. Rising edge slew rate equation $srr1 = V_{diVW,max}/({}^tr1)$.
 - 2. Rising edge slew rate equation srr2 = $(V_{IHL(AC)min} V_{diVW,max})/(2 \times {}^{t}r2)$.
 - 3. Falling edge slew rate equation $srf1 = V_{diVW,max}/({}^tf1)$.
 - 4. Falling edge slew rate equation srf2 = $(V_{IHL(AC)min} V_{diVW,max})/(2 \times {}^tf2)$.

Table 90: DQ Input Receiver Specifications

Note 1 applies to the entire table

		DDR4-1600, 1866, 2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200			Not
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	es
V _{IN} Rx mask input peak-to-peak	V _{diVW}	-	136	_	130	-	120	_	115	_	110	mV	2, 3
DQ Rx input tim- ing window	TdiVW	-	0.2	_	0.2	_	0.22	-	0.23	-	0.23	UI	2, 3
DQ AC input swing peak-to- peak	V _{IHL(AC)}	186	_	160	_	150	_	145	_	140	_	mV	4, 5

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Table 90: DQ Input Receiver Specifications (Continued)

Note 1 applies to the entire table

rtote i applies to til			4400										
			-1600, 2133	DDP/	-2400	DDP/	-2666	DDP/	-2933	DDP4	-3200		
					1		1		1		I		Not
Parameter	Symbol	Min	Max	Min	Мах	Min	Max	Min	Max	Min	Мах	Unit	es
DQ input pulse width	TdiPW	0.58	-	0.58	_	0.58	_	0.58	_	0.58	_	UI	6
DQS-to-DQ Rx mask offset	^t DQS2D Q	-0.17	0.17	-0.17	0.17	-0.19	0.19	-0.22	0.22	-0.22	0.22	UI	7
DQ-to-DQ Rx mask offset	^t DQ2DQ	-	0.1	-	0.1	-	0.105	-	0.115	_	0.125	UI	8
Input slew rate over V _{diVW} if ^t CK ≥ 0.937ns	srr1, srf1	1	9	1	9	1	9	1	9	1	9	V/ns	9
Input slew rate over V _{diVW} if 0.937ns > ^t CK ≥ 0.625ns	srr1, srf1	-	-	1.25	9	1.25	9	1.25	9	1.25	9	V/ns	9
Rising input slew rate over 1/2 V _{IHL(AC)}	srr2	0.2 × srr1	9	0.2 × srr1	9	0.2 × srr1	9	0.2 × srr1	9	0.2 × srr1	9	V/ns	10
Falling input slew rate over 1/2 V _{IHL(AC)}	srf2	0.2 × srf1	9	0.2 × srf1	9	0.2 × srf1	9	0.2 × srf1	9	0.2 × srf1	9	V/ns	10

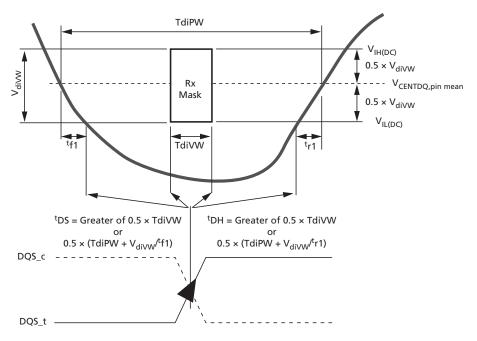
- Notes: 1. All Rx mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdiVW (MIN), V_{diVW.max}, and minimum slew rate limits, then either TdiVW (MIN) or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.
 - 2. Data Rx mask voltage and timing total input valid window where V_{diVW} is centered around V_{CENTDQ,midpoint} after V_{REFDQ} training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER $=1^{e-16}$ when the Rx mask is not violated.
 - 3. Defined over the DQ internal V_{REF} range 1.
 - 4. Overshoot and undershoot specifications apply.
 - 5. DQ input pulse signal swing into the receiver must meet or exceed VIHI (AC)min. VIHI (AC)min is to be achieved on an UI basis when a rising and falling edge occur in the same UI (a valid TdiPW).
 - 6. DQ minimum input pulse width defined at the V_{CENTDO.midpoint}.
 - 7. DQS-to-DQ Rx mask offset is skew between DQS and DQ within a nibble (x4) or word (x8, x16 [for x16, the upper and lower bytes are treated as separate x8s]) at the SDRAM balls over process, voltage, and temperature.
 - 8. DQ-to-DQ Rx mask offset is skew between DQs within a nibble (x4) or word (x8, x16) at the SDRAM balls for a given component over process, voltage, and temperature.
 - 9. Input slew rate over V_{diVW} mask centered at V_{CENTDQ,midpoint}. Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7V/ns of each other.
 - 10. Input slew rate between V_{diVW} mask edge and $V_{IHL(AC)min}$ points.

The following figure shows the Rx mask relationship to the input timing specifications relative to system ^tDS and ^tDH. The classical definition for ^tDS/^tDH required a DQ rising

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and falling edges to not violate ^tDS and ^tDH relative to the DQS strobe at any time; however, with the Rx mask ^tDS and ^tDH can shift relative to the DQS strobe provided the input pulse width specification is satisfied and the Rx mask is not violated.

Figure 213: Rx Mask Relative to ^tDS/^tDH



The following figure and table show an example of the worst case Rx mask required if the DQS and DQ pins do not have DRAM controller to DRAM write DQ training. The figure and table show that without DRAM write DQ training, the Rx mask would increase from 0.2UI to essentially 0.54UI. This would also be the minimum ^tDS and ^tDH required as well.

Figure 214: Rx Mask Without Write Training

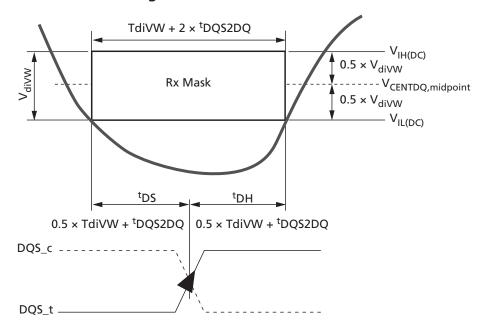


Table 91: Rx Mask and ^tDS/^tDH without Write Training

DDR4	V _{IHL(AC)} (mV)	TdiPW (UI)	V _{diVW} (mV)	TdiVW (UI)	^t DQS2DQ (UI)	^t DQ2DQ (UI)	Rx Mask with Write Train (ps)	^t DS + ^t DH (ps)
1600	186	0.58	136	0.2	±0.17	0.1	125	338
1866	186	0.58	136	0.2	±0.17	0.1	107.1	289
2133	186	0.58	136	0.2	±0.17	0.1	94	253
2400	160	0.58	130	0.2	±0.17	0.1	83.3	225
2666	150	0.58	120	0.22	±0.19	0.105	82.5	225
2933	145	0.58	115	0.23	±0.22	0.115	78.4	228
3200	140	0.58	110	0.23	±0.22	0.125	71.8	209

Note: 1. $V_{IHL(AC)}$, V_{diVW} , and $V_{ILH(DC)}$ referenced to $V_{CENTDQ,midpoint}$.

Connectivity Test (CT) Mode Input Levels

Table 92: TEN Input Levels (CMOS)

Parameter	Symbol	Min	Мах	Unit	Note
TEN AC input high voltage	V _{IH(AC)_TEN}	0.8 × V _{DD}	V_{DD}	V	1
TEN DC input high voltage	V _{IH(DC)_TEN}	0.7 × V _{DD}	V_{DD}	V	
TEN DC input low voltage	V _{IL(DC)_TEN}	V _{SS}	$0.3 \times V_{DD}$	V	
TEN AC input low voltage	V _{IL(AC)_TEN}	V _{SS}	$0.2 \times V_{DD}$	V	2
TEN falling time	tF_TEN	_	1 0	ns	

Table 92: TEN Input Levels (CMOS) (Continued)

Parameter	Symbol	Min	Мах	Unit	Note
TEN rising time	^t R_TEN	_	1 0	ns	

Notes: 1. Overshoot should not exceed the V_{IN} values in the Absolute Maximum Ratings table.

2. Undershoot should not exceed the V_{IN} values in the Absolute Maximum Ratings table.

Figure 215: TEN Input Slew Rate Definition

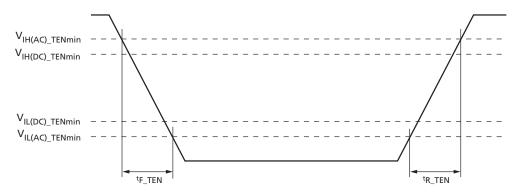


Table 93: CT Type-A Input Levels

Parameter	Symbol	Min	Max	Unit	Note
CTipA AC input high voltage	V _{IH(AC)}	V _{REF} + 200	V _{DD1} ¹	V	2, 3
CTipA DC input high voltage	V _{IH(DC)}	V _{REF} + 150	V_{DD}	V	2, 3
CTipA DC input low voltage	V _{IL(DC)}	V _{SS}	V _{REF} - 150	V	2, 3
CTipA AC input low voltage	V _{IL(AC)}	V _{SS1} ¹	V _{REF} - 200	V	2, 3
CTipA falling time	tF_CTipA	_	5	ns	2
CTipA rising time	^t R_CTipA	_	5	ns	2

Notes: 1. Refer to Overshoot and Undershoot Specifications.

- 2. CT Type-A inputs: CS_n, BG[1:0], BA[1:0], A[9:0], A10/AP, A11, A12/BC_n, A13, WE_n/A14, CAS_n/A15, RAS_n/A16, A17, CKE, ACT_n, ODT, CLK_t, CLK_C, PAR.
- 3. $V_{REFCA} = 0.5 \times V_{DD}$.

Figure 216: CT Type-A Input Slew Rate Definition

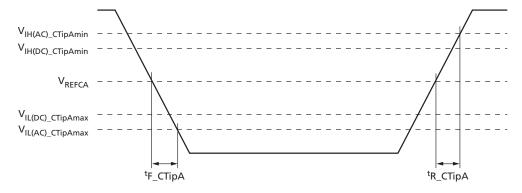


Table 94: CT Type-B Input Levels

Parameter	Symbol	Min	Мах	Unit	Note
CTipB AC input high voltage	V _{IH(AC)}	V _{REF} + 300	V _{DD1} ¹	V	2, 3
CTipB DC input high voltage	V _{IH(DC)}	V _{REF} + 200	V_{DD}	V	2, 3
CTipB DC input low voltage	V _{IL(DC)}	V _{SS}	V _{REF} - 200	V	2, 3
CTipB AC input low voltage	V _{IL(AC)}	V _{SS1} ¹	V _{REF} - 300	V	2, 3
CTipB falling time	^t F_CTipB	_	5	ns	2
CTipB rising time	^t R_CTipB	_	5	ns	2

- Notes: 1. Refer to Overshoot and Undershoot Specifications.
 - 2. CT Type-B inputs: DML_n/DBIL_n, DMU_n/DBIU_n and DM_n/DBI_n.
 - 3. V_{REFDQ} should be $0.5 \times V_{DD}$

Figure 217: CT Type-B Input Slew Rate Definition

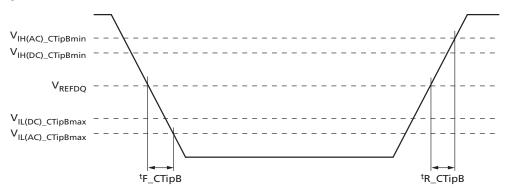


Table 95: CT Type-C Input Levels (CMOS)

Parameter	Symbol	Min	Max	Unit	Note
CTipC AC input high voltage	V _{IH(AC)_CTipC}	0.8 × V _{DD}	V_{DD}^{1}	V	2
CTipC DC input high voltage	V _{IH(DC)_CTipC}	0.7 × V _{DD}	V_{DD}	V	2
CTipC DC input low voltage	V _{IL(DC)_CTipC}	V _{SS}	0.3 × V _{DD}	V	2
CTipC AC input low voltage	V _{IL(AC)_CTipC}	V _{SS} ¹	0.2 × V _{DD}	V	2
CTipC falling time	tF_CTipC	_	1 0	ns	2
CTipC rising time	^t R_CTipC	_	1 0	ns	2

Notes: 1. Refer to Overshoot and Undershoot Specifications.

2. CT Type-C inputs: Alert_n.

Figure 218: CT Type-C Input Slew Rate Definition

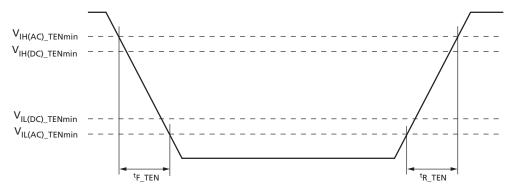


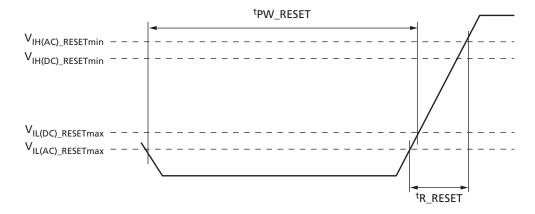
Table 96: CT Type-D Input Levels

Parameter	Symbol	Min	Max	Unit	Note
CTipD AC input high voltage	V _{IH(AC)_CTipD}	0.8 × V _{DD}	V_{DD}	V	4
CTipD DC input high voltage	V _{IH(DC)_CTipD}	$0.7 \times V_{DD}$	V_{DD}	V	2
CTipD DC input low voltage	V _{IL(DC)_CTipD}	V _{SS}	0.3 × V _{DD}	V	1
CTipD AC input low voltage	V _{IL(AC)_CTipD}	V _{SS}	0.2 × V _{DD}	V	5
Rising time	^t R_RESET	_	1	μs	3
RESET pulse width - after power-up	tPW_RESET_S	1	_	μs	
RESET pulse width - during power-up	^t PW_RESET_L	200	_	μs	

Notes:

- 1. After RESET_n is registered LOW, the RESET_n level must be maintained below $V_{IL(DC)_RE-SET}$ during tPW_RESET , otherwise, the DRAM may not be reset.
- 2. After RESET_n is registered HIGH, the RESET_n level must be maintained above V_{IH(DC)_RESET}, otherwise, operation will be uncertain until it is reset by asserting RESET_n signal LOW.
- 3. Slope reversal (ring-back) during this level transition from LOW to HIGH should be mitigated as much as possible.
- 4. Overshoot should not exceed the V_{IN} values in the Absolute Maximum Ratings table.
- 5. Undershoot should not exceed the V_{IN} values in the Absolute Maximum Ratings table.
- 6. CT Type-D inputs: RESET_n; same requirements as in normal mode.

Figure 219: CT Type-D Input Slew Rate Definition

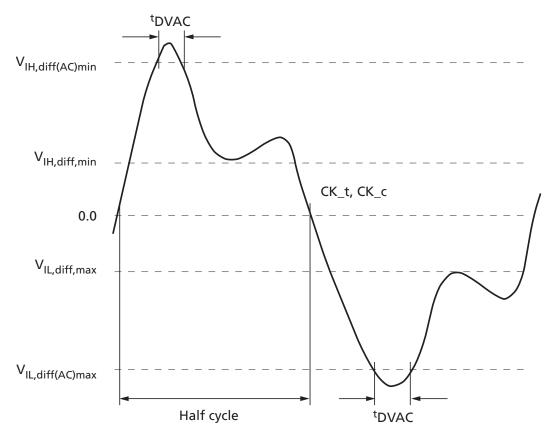




Electrical Characteristics – AC and DC Differential Input Measurement Levels

Differential Inputs

Figure 220: Differential AC Swing and "Time Exceeding AC-Level" ^tDVAC



Notes: 1. Differential signal rising edge from V_{IL,diff,max} to V_{IH,diff(AC)min} must be monotonic slope.

2. Differential signal falling edge from $_{IH,diff,min}$ to $V_{IL,diff(AC)max}$ must be monotonic slope.

Table 97: Differential Input Swing Requirements for CK_t, CK_c

	Sym-		DDR4-1600 / 1866 / 2133		DDR4-2400 / 2666 DDR4-		l-2933 DDR4-3200		-3200		Note
Parameter	bol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	S
Differential input high	V_{IHdiff}	150	Note 3	135	Note 3	125	Note 3	110	Note 3	mV	1
Differential input low	V _{ILdiff}	Note 3	-150	Note 3	-135	Note 3	-125	Note 3	-110	mV	1
Differential input high (AC)	V _{IH-} diff(AC)	2 × (V _{IH(AC)} - V _{REF})	Note 3	2 × (V _{IH(AC)} - V _{REF})	Note 3	2 × (V _{IH(AC)} - V _{REF})	Note 3	2 × (V _{IH(AC)} - V _{REF})	Note 3	V	2

Table 97: Differential Input Swing Requirements for CK_t, CK_c (Continued)

	Sym-		·1600 / / 2133		-2400 / 666	DDR4	-2933	DDR4	-3200		Note
Parameter	bol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	S
Differential input low (AC)	V _{IL} -	Note 3	2 × (V _{IL(AC)} - V _{REF})	Note 3	2 × (V _{IL(AC)} - V _{REF})	Note 3	2 × (V _{IL(AC)} - V _{REF})	Note 3	2 × (V _{IL(AC)} - V _{REF})	V	2

- Notes: 1. Used to define a differential signal slew-rate.
 - 2. For CK_t, CK_c use V_{IH(AC)} and V_{IL(AC)} of ADD/CMD and V_{REFCA}.
 - 3. These values are not defined; however, the differential signals (CK_t, CK_c) need to be within the respective limits, $V_{IH(DC)max}$ and $V_{IL(DC)min}$ for single-ended signals as well as the limitations for overshoot and undershoot.

Table 98: Minimum Time AC Time ^tDVAC for CK

	^t DVAC (ps) at V _{IH,0}	diff(AC) to V _{IL,diff(AC)}
Slew Rate (V/ns)	200mV	TBDmV
>4.0	120	TBD
4.0	115	TBD
3.0	110	TBD
2.0	105	TBD
1.9	100	TBD
1.6	95	TBD
1.4	90	TBD
1.2	85	TBD
1.0	80	TBD
<1.0	80	TBD

Note: 1. Below V_{IL(AC)}.

Single-Ended Requirements for CK Differential Signals

Each individual component of a differential signal (CK_t, CK_c) has to comply with certain requirements for single-ended signals. CK_t and CK_c have to reach approximately $V_{SEHmin}/V_{SEL,max}$, which are approximately equal to the AC levels $V_{IH(AC)}$ and $V_{IL(AC)}$ for ADD/CMD signals in every half-cycle. The applicable AC levels for ADD/CMD might differ per speed-bin, and so on. For example, if a value other than 100mV is used for ADD/CMD V_{IH(AC)} and V_{IL(AC)} signals, then these AC levels also apply for the singleended signals CK_t and CK_c.

While ADD/CMD signal requirements are with respect to V_{REFCA} , the single-ended components of differential signals have a requirement with respect to V_{DD}/2; this is nominally the same. The transition of single-ended signals through the AC levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V_{SEL,max}/V_{SEH,min} has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Figure 221: Single-Ended Requirements for CK

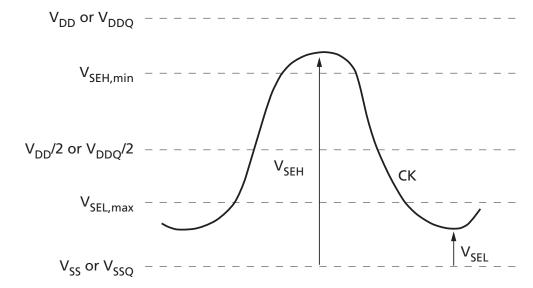


Table 99: Single-Ended Requirements for CK

		DDR4-1600 / 1866 / 2133		DDR4-2400 / 2666		DDR4-2933 / 3200			
Parameter	Symbol	Min	Max			Min	Max	Unit	Notes
Single-ended high level for CK_t, CK_c	V _{SEH}	V _{DD} /2 + 0.100	Note 3	V _{DD} /2 + 0.095	Note 3	V _{DD} /2 + 0.085	Note 3	V	1, 2
Single-ended low level for CK_t, CK_c	V _{SEL}	Note 3	V _{DD} /2 - 0.100	Note 3	V _{DD} /2 - 0.095	Note 3	V _{DD} /2 - 0.085	V	1, 2

- Notes: 1. For CK_t, CK_c use V_{IH(AC)} and V_{IL(AC)} of ADD/CMD and V_{REFCA}.
 - 2. ADDR/CMD V_{IH(AC)} and V_{IL(AC)} based on V_{REFCA}.
 - 3. These values are not defined; however, the differential signal (CK_t, CK_c) need to be within the respective limits, $V_{IH(DC)max}$ and $V_{IL(DC)min}$ for single-ended signals as well as the limitations for overshoot and undershoot.

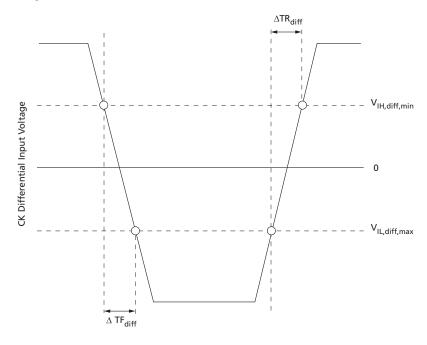
Slew Rate Definitions for CK Differential Input Signals

Table 100: CK Differential Input Slew Rate Definition

	Measured		
Description	From	То	Defined by
Differential input slew rate for rising edge	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$ V_{IH,diff,min} - V_{IL,diff,max} /\Delta TR_{diff}$
Differential input slew rate for falling edge	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$V_{IH,diff,min}$ - $V_{IL,diff,max}$

Note: 1. The differential signal CK_t, CK_c must be monotonic between these thresholds.

Figure 222: Differential Input Slew Rate Definition for CK_t, CK_c



CK Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signal CK_t, CK_c must meet the requirements shown below. The differential input cross point voltage $V_{\rm IX(CK)}$ is measured from the actual cross point of true and complement signals to the midlevel between $V_{\rm DD}$ and $V_{\rm SS}$.

Figure 223: V_{IX(CK)} Definition

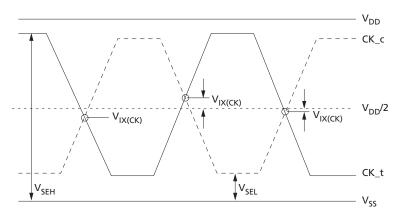




Table 101: Cross Point Voltage For CK Differential Input Signals at DDR4-1600 through DDR4-2400

			DDR4-1600, 1866, 2133, 2400			
Parameter	Sym	Input Level	Min	Max		
Differential input cross point volt- age relative to V _{DD} /2 for CK_t, CK_c	(,	$V_{SEH} > V_{DD}/2 + 145 \text{mV}$	N/A	120mV		
		$V_{DD}/2 + 100 \text{mV} \le V_{SEH} \le V_{DD}/2 + 145 \text{mV}$	N/A	(V _{SEH} - V _{DD} /2) - 25mV		
		$V_{DD}/2 - 145 \text{mV} \le V_{SEL} \le V_{DD}/2 - 100 \text{mV}$	$-(V_{DD}/2 - V_{SEL}) + 25mV$	N/A		
		V _{SEL} < V _{DD} /2 - 145mV	-120mV	N/A		

Table 102: Cross Point Voltage For CK Differential Input Signals at DDR4-2666 through DDR4-3200

			DDR4-2666, 2933, 3200		
Parameter	Sym	Input Level	Min	Max	
Differential input	-	$V_{SEH} > V_{DD}/2 + 145 \text{mV}$	N/A	110mV	
cross point volt-		$V_{DD}/2 + 90 \text{mV} \le V_{SEH} \le V_{DD}/2 + 145 \text{mV}$	N/A	(V _{SEH} - V _{DD} /2) - 30mV	
age relative to V _{DD} /2 for CK_t,		$V_{DD}/2 - 145 \text{mV} \le V_{SEL} \le V_{DD}/2 - 90 \text{mV}$	$-(V_{DD}/2 - V_{SEL}) + 30mV$	N/A	
CK_c		$V_{SEL} < V_{DD}/2 - 145 mV$	-110mV	N/A	

DQS Differential Input Signal Definition and Swing Requirements

Figure 224: Differential Input Signal Definition for DQS_t, DQS_c

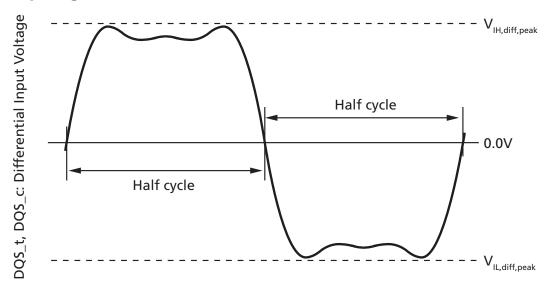


Table 103: DDR4-1600 through DDR4-2400 Differential Input Swing Requirements for DQS_t, DQS_c

			00, 1866, 33	DDR4-2400				
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes	
Peak differential input high voltage	V _{IH,diff,peak}	186	V_{DDQ}	160	V_{DDQ}	mV	1,2	

Table 103: DDR4-1600 through DDR4-2400 Differential Input Swing Requirements for DQS_t, DQS_c (Continued)

		DDR4-16 21	00, 1866, 33	DDR4-2400				
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes	
Peak differential input low voltage	$V_{IL,diff,peak}$	V _{SSQ}	-186	V _{SSQ}	-160	mV	1,2	

Notes:

- 1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
- 2. Minimum value point is used to determine differential signal slew-rate.

Table 104: DDR4-2633 through DDR4-3200 Differential Input Swing Requirements for DQS_t, DQS_c

	DDR4-2666		DDR4-2933		DDR4-3200				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Peak differential input high voltage	$V_{IH,diff,peak}$	150	V_{DDQ}	145	V_{DDQ}	140	V_{DDQ}	mV	1,2
Peak differential input low voltage	$V_{IL,diff,peak}$	V _{SSQ}	-150	V _{SSQ}	-145	V _{SSQ}	-140	mV	1,2

Notes:

- 1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
- 2. Minimum value point is used to determine differential signal slew-rate.

The peak voltage of the DQS signals are calculated using the following equations:

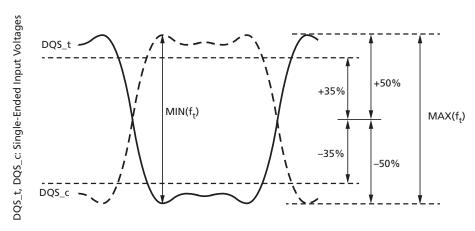
 $V_{IH,dif,Peak}$ voltage = MAX(f_t)

 $V_{IL,dif,Peak}$ voltage = MIN(f_t)

 $(f_t) = DQS_t, DQS_c.$

The MAX(f(t)) or MIN(f(t)) used to determine the midpoint from which to reference the ±35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all UIs.

Figure 225: DQS_t, DQS_c Input Peak Voltage Calculation and Range of Exempt non-Monotonic Signaling



8Gb: x4, x8, x16 DDR4 SDRAM Electrical Characteristics – AC and DC Differential Input Measurement Levels

DQS Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS_t, DQS_c) must meet $V_{IX_DQS_ratio}$ in the table below. The differential input cross point voltage V_{IX_DQS} ($V_{IX_DQS_FR}$ and $V_{IX_DQS_RF}$) is measured from the actual cross point of DQS_t, DQS_c relative to the V_{DOS_mid} of the DQS_t and DQS_c signals.

 $V_{DQS,mid}$ is the midpoint of the minimum levels achieved by the transitioning DQS_t and DQS_c signals, and noted by $V_{DQS_trans}.V_{DQS_trans}$ is the difference between the lowest horizontal tangent above $V_{DQS,mid}$ of the transitioning DQS signals and the highest horizontal tangent below $V_{DQS,mid}$ of the transitioning DQS signals. A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within $\pm 35\%$ of the midpoint of either $V_{IH,DIFEPeak}$ voltage (DQS_t rising) or $V_{IL,DIFEPeak}$ voltage (DQS_c rising), as shown in the figure below

A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in the figure below), and a ring-back's horizontal tangent is derived from its positive slope to zero slope transition (point B in the figure below) and is not a valid horizontal tangent; a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in the figure below), and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in the figure below) and is not a valid horizontal tangent.

Figure 226: VIXDQS Definition

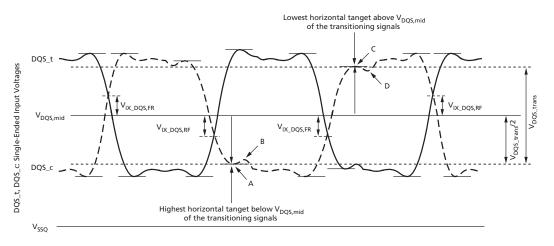


Table 105: Cross Point Voltage For Differential Input Signals DQS

		DDR4-1600, 18 2666, 29			
Parameter	Symbol	Min	Max	Unit	Notes
DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings	$V_{IX_DQS,ratio}$	-	25	%	1, 2

Table 105: Cross Point Voltage For Differential Input Signals DQS (Continued)

		DDR4-1600, 18 2666, 29			
Parameter	Symbol	Min	Max	Unit	Notes
V _{DQS,mid} to V _{cent(midpoint)} offset	V_{DQS,mid_to_Vcent}	_	Note 3	mV	2

Notes

- V_{IX_DQS,ratio} is DQS V_{IX} crossing (V_{IX_DQS,FR} or V_{IX_DQS,RF}) divided by V_{DQS_trans}. V_{DQS_trans} is the difference between the lowest horizontal tangent above V_{DQS,mid} of the transitioning DQS signals and the highest horizontal tangent below V_{DQS,mid} of the transitioning DQS signals.
- 2. $V_{DQS,mid}$ will be similar to the V_{REFDQ} internal setting value ($V_{cent(midpoint)}$ offset) obtained during V_{REF} Training if the DQS and DQs drivers and paths are matched.
- 3. The maximum limit shall not exceed the smaller of V_{IH.diff,DOS} minimum limit or 50mV.

Slew Rate Definitions for DQS Differential Input Signals

Table 106: DQS Differential Input Slew Rate Definition

	Meas	sured	
Description	From	То	Defined by
Differential input slew rate for rising edge	V _{IL,diff,DQS}	V _{IH,diff,DQS}	$ V_{IH,diff,DQS} - V_{IL,diff,DQS} /\Delta TR_{diff}$
Differential input slew rate for falling edge	V _{IH,diff,DQS}	V _{IL,diff,DQS}	$ V_{IHdiffDQS} - V_{IL,diff,DQS} /\Delta TF_{diff}$

Note: 1. The differential signal DQS_t, DQS_c must be monotonic between these thresholds.

Figure 227: Differential Input Slew Rate and Input Level Definition for DQS_t, DQS_c

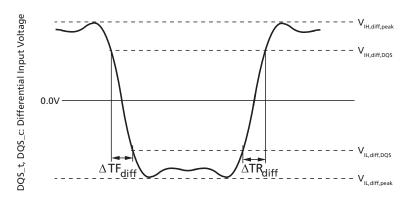


Table 107: DDR4-1600 through DDR4-2400 Differential Input Slew Rate and Input Levels for DQS_t, DQS_c

		DDR4-1600, 1866, 2133		DDR4	-2400		
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Peak differential input high voltage	$V_{IH,diff,peak}$	186	V_{DDQ}	160	V_{DDQ}	mV	1
Differential input high voltage	$V_{IH,diff,DQS}$	136	_	130	_	mV	2, 3
Differential input low voltage	$V_{IL,diff,DQS}$	_	-136	_	-130	mV	2, 3

8Gb: x4, x8, x16 DDR4 SDRAM Electrical Characteristics – AC and DC Differential Input Measurement Levels

Table 107: DDR4-1600 through DDR4-2400 Differential Input Slew Rate and Input Levels for DQS_t, DQS c (Continued)

		DDR4-1600,	DDR4	-2400			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Peak differential input low voltage	$V_{IL,diff,peak}$	V _{SSQ}	-186	V _{SSQ}	-160	mV	1
DQS differential input slew rate	SRIdiff	3.0	18	3.0	18	V/ns	4, 5

- Notes: 1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
 - 2. Differential signal rising edge from $V_{IL,diff,DQS}$ to $V_{IH,diff,DQS}$ must be monotonic slope.
 - 3. Differential signal falling edge from $V_{IH,diff,DQS}$ to $V_{IL,diff,DQS}$ must be monotonic slope.
 - 4. Differential input slew rate for rising edge from $V_{IL.diff,DQS}$ to $V_{IH,diff,DQS}$ is defined by | $V_{IL,diff,min} - V_{IH,diff,max} / \Delta TR_{diff}$
 - 5. Differential input slew rate for falling edge from $V_{IH,diff,DQS}$ to $V_{IL,diff,DQS}$ is defined by | $V_{IL,diff,min} - V_{IH,diff,max} / \Delta TF_{diff}$

Table 108: DDR4-2666 through DDR4-3200 Differential Input Slew Rate and Input Levels for DQS t, DQS c

		DDR4-2666 DDR4-2933		DDR4	-3200				
Parameter	Symbol	Min	Мах	Min	Max	Min	Max	Unit	Notes
Peak differential input high voltage	$V_{IH,diff,peak}$	150	V_{DDQ}	145	V_{DDQ}	140	V _{DDQ}	mV	1
Differential input high voltage	$V_{IH,diff,DQS}$	130	_	115	_	110	_	mV	2, 3
Differential input low voltage	$V_{IL,diff,DQS}$	-	-130	_	-115	-	-110	mV	2, 3
Peak differential input low voltage	V _{IL,diff,peak}	V _{SSQ}	-150	V _{SSQ}	-145	V _{SSQ}	-140	mV	1
DQS differential input slew rate	SRIdiff	2.5	18	2.5	18	2.5	18	V/ns	4, 5

- 1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
- 2. Differential signal rising edge from $V_{IL,diff,DQS}$ to $V_{IH,diff,DQS}$ must be monotonic slope.
- 3. Differential signal falling edge from $V_{IH,diff,DQS}$ to $V_{IL,diff,DQS}$ must be monotonic slope.
- 4. Differential input slew rate for rising edge from $V_{IL,diff,DQS}$ to $V_{IH,diff,DQS}$ is defined by | $V_{IL,diff,min} - V_{IH,diff,max} / \Delta TR_{diff}$
- 5. Differential input slew rate for falling edge from $V_{IH,diff,DQS}$ to $V_{IL,diff,DQS}$ is defined by | $V_{IL,diff,min} - V_{IH,diff,max} / \Delta TF_{diff}$



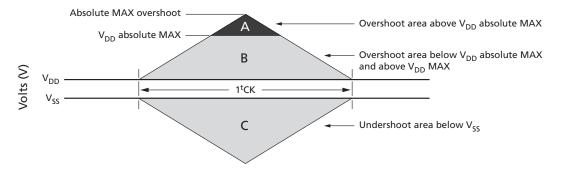
Electrical Characteristics – Overshoot and Undershoot Specifications

Address, Command, and Control Overshoot and Undershoot Specifications

Table 109: ADDR, CMD, CNTL Overshoot and Undershoot/Specifications

	DDR4-							
Description	1600	1866	2133	2400	2666	2933	3200	Unit
Address and control pins (A[17:0], BG[1:0], BA[1:0], CS_n, RAS_n, CAS_n, WE_n, CKE, ODT, C2-0)								
Area A: Maximum peak amplitude above V _{DD} absolute MAX	0.06	0.06	0.06	0.06	0.06	0.06	0.06	V
Area B: Amplitude allowed between V_{DD} and V_{DD} absolute MAX	0.24	0.24	0.24	0.24	0.24	0.24	0.24	V
Area C: Maximum peak amplitude allowed for undershoot below V _{SS}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	V
Area A maximum overshoot area per 1 ^t CK	0.0083	0.0071	0.0062	0.0055	0.0055	0.0055	0.0055	V/ns
Area B maximum overshoot area per 1 ^t CK	0.2550	0.2185	0.1914	0.1699	0.1699	0.1699	0.1699	V/ns
Area C maximum undershoot area per 1 ^t CK	0.2644	0.2265	0.1984	0.1762	0.1762	0.1762	0.1762	V/ns

Figure 228: ADDR, CMD, CNTL Overshoot and Undershoot Definition



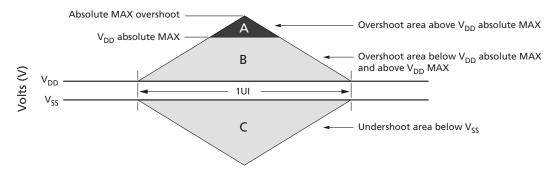


Clock Overshoot and Undershoot Specifications

Table 110: CK Overshoot and Undershoot/ Specifications

	DDR4-							
Description	1600	1866	2133	2400	2666	2933	3200	Unit
CLK_t, CLK_n								
Area A: Maximum peak amplitude above V _{DD} absolute MAX	0.06	0.06	0.06	0.06	0.06	0.06	0.06	V
Area B: Amplitude allowed between V_{DD} and V_{DD} absolute MAX	0.24	0.24	0.24	0.24	0.24	0.24	0.24	V
Area C: Maximum peak amplitude allowed for undershoot below V_{SS}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	V
Area A maximum overshoot area per 1UI	0.0038	0.0032	0.0028	0.0025	0.0025	0.0025	0.0025	V/ns
Area B maximum overshoot area per 1UI	0.1125	0.0964	0.0844	0.0750	0.0750	0.0750	0.0750	V/ns
Area C maximum undershoot area per 1UI	0.1144	0.0980	0.0858	0.0762	0.0762	0.0762	0.0762	V/ns

Figure 229: CK Overshoot and Undershoot Definition



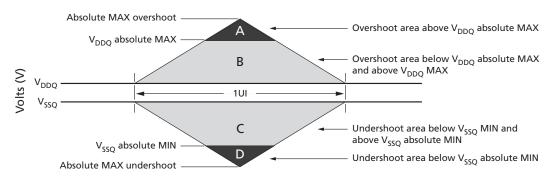


Data, Strobe, and Mask Overshoot and Undershoot Specifications

Table 111: Data, Strobe, and Mask Overshoot and Undershoot/ Specifications

Description	DDR4- 1600	DDR4- 1866	DDR4- 2133	DDR4- 2400	DDR4- 2666	DDR4- 2933	DDR4- 3200	Unit	
DQS_t, DQS_n, LDQS_t, LDQS_n, UDQS_t, UDQS_n, DQ[0:15], DM/DBI, UDM/UDBI, LDM/LDBI,									
Area A: Maximum peak amplitude above V _{DDQ} absolute MAX	0.16	0.16	0.16	0.16	0.16	0.16	0.16	V	
Area B: Amplitude allowed between V_{DDQ} and V_{DDQ} absolute MAX	0.24	0.24	0.24	0.24	0.24	0.24	0.24	V	
Area C: Maximum peak amplitude allowed for undershoot below V _{SSQ}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	V	
Area D: Maximum peak amplitude below V _{SSQ} absolute MIN	0.10	0.10	0.10	0.10	0.10	0.10	0.10	V	
Area A maximum overshoot area per 1UI	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	0.0100	V/ns	
Area B maximum overshoot area per 1UI	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	0.0700	V/ns	
Area C maximum undershoot area per 1UI	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	0.0700	V/ns	
Area D maximum undershoot area per 1UI	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	0.0100	V/ns	

Figure 230: Data, Strobe, and Mask Overshoot and Undershoot Definition



Electrical Characteristics – AC and DC Output Measurement Levels Single-Ended Outputs

Table 112: Single-Ended Output Levels

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
DC output high measurement level (for IV curve linearity)	V _{OH(DC)}	1.1 × V _{DDQ}	V
DC output mid measurement level (for IV curve linearity)	V _{OM(DC)}	$0.8 \times V_{DDQ}$	V
DC output low measurement level (for IV curve linearity)	V _{OL(DC)}	0.5 × V _{DDQ}	V
AC output high measurement level (for output slew rate)	V _{OH(AC)}	$(0.7 + 0.15) \times V_{DDQ}$	V

Table 112: Single-Ended Output Levels (Continued)

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
AC output low measurement level (for output slew rate)	V _{OL(AC)}	(0.7 - 0.15) × V _{DDQ}	V

Note: 1. The swing of $\pm 0.15 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $R_{ZQ}/7$ and an effective test load of 50Ω to $V_{TT} = V_{DDO}$.

Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals.

Table 113: Single-Ended Output Slew Rate Definition

	Meas	sured	
Description	From	То	Defined by
Single-ended output slew rate for rising edge	V _{OL(AC)}	V _{OH(AC)}	$[V_{OH(AC)} - V_{OL(AC)}]/\Delta TR_{se}$
Single-ended output slew rate for falling edge	V _{OH(AC)}	V _{OL(AC)}	$[V_{OH(AC)} - V_{OL(AC)}]/\Delta TF_{se}$

Figure 231: Single-ended Output Slew Rate Definition

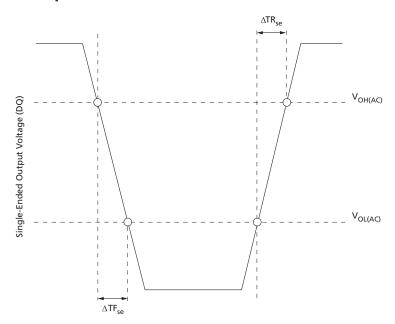


Table 114: Single-Ended Output Slew Rate

For $R_{ON} = R_{ZO}/7$

		DDR4-1600/ 1866 / 2133 / 2400			DDR4-2666		DDR4-2933 / 3200	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Single-ended output slew rate	SRQ _{se}	4	9	4	9	4	9	V/ns

- Notes: 1. SR = slew rate; Q = query output; se = single-ended signals.
 - 2. In two cases a maximum slew rate of 12V/ns applies for a single DQ signal within a byte lane:
 - Case 1 is defined for a single DQ signal within a byte lane that is switching into a certain direction (either from HIGH-to-LOW or LOW-to-HIGH) while all remaining DQ signals in the same byte lane are static (they stay at either HIGH or LOW).
 - Case 2 is defined for a single DQ signal within a byte lane that is switching into a certain direction (either from HIGH-to-LOW or LOW-to-HIGH) while all remaining DQ signals in the same byte lane are switching into the opposite direction (from LOW-to-HIGH or HIGH-to-LOW, respectively). For the remaining DQ signal switching into the opposite direction, the standard maximum limit of 9 V/ns applies.

Differential Outputs

Table 115: Differential Output Levels

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
AC differential output high measurement level (for output slew rate)	$V_{OH,diff(AC)}$	0.3 × V _{DDQ}	V
AC differential output low measurement level (for output slew rate)	$V_{OL,diff(AC)}$	−0.3 × V _{DDQ}	V

Note: 1. The swing of $\pm 0.3 \times V_{DDO}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of R_{ZO}/7 and an effective test load of 50Ω to $V_{TT} = V_{DDO}$ at each differential output.

Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL.diff(AC)} and V_{OL.diff(AC)} for differential signals.

Table 116: Differential Output Slew Rate Definition

	Measured		
Description	From	То	Defined by
Differential output slew rate for rising edge	V _{OL,diff(AC)}	V _{OH,diff(AC)}	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}]/\Delta TR_{diff}$
Differential output slew rate for falling edge	V _{OH,diff(AC)}	V _{OL,diff(AC)}	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}]/\Delta TF_{diff}$

Figure 232: Differential Output Slew Rate Definition

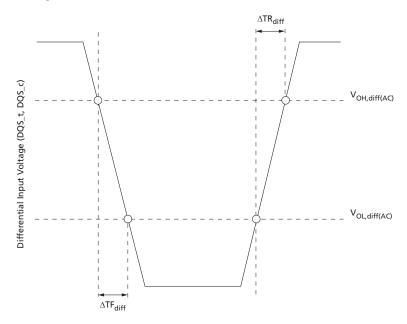


Table 117: Differential Output Slew Rate

For $R_{ON} = R_{7O}/7$

101 NOW 112Q 7		DDR4-1600 / 1866 / 2133 / 2400		DDR4-2666		DDR4-2933 / 3200		
Parameter	Symbol	Min	Мах	Min	Max	Min	Max	Unit
Differential output slew rate	SRQ _{diff}	8	18	8	18	8	18	V/ns

Note: 1. SR = slew rate; Q = query output; diff = differential signals.

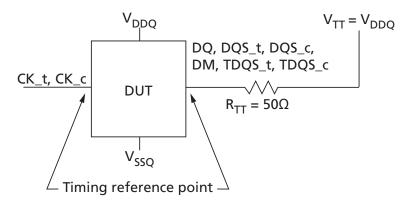
Reference Load for AC Timing and Output Slew Rate

The effective reference load of 50Ω to V_{TT} = V_{DDQ} and driver impedance of $R_{ZQ}/7$ for each output was used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

 R_{ON} nominal of DQ, DQS_t and DQS_c drivers uses 34 ohms to specify the relevant AC timing parameter values of the device. The maximum DC high level of output signal = $1.0 \times V_{DDQ}$, the minimum DC low level of output signal = { 34 /(34 + 50) } $\times V_{DDQ}$ = 0.4 \times V_{DDQ} .

The nominal reference level of an output signal can be approximated by the following: The center of maximum DC high and minimum DC low = { (1 + 0.4) / 2 } × V_{DDQ} = 0.7 × V_{DDQ} . The actual reference level of output signal might vary with driver R_{ON} and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye.

Figure 233: Reference Load For AC Timing and Output Slew Rate



Connectivity Test Mode Output Levels

Table 118: Connectivity Test Mode Output Levels

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
DC output high measurement level (for IV curve linearity)	V _{OH(DC)}	1.1 × V _{DDQ}	V
DC output mid measurement level (for IV curve linearity)	V _{OM(DC)}	$0.8 \times V_{DDQ}$	V
DC output low measurement level (for IV curve linearity)	V _{OL(DC)}	$0.5 \times V_{DDQ}$	V
DC output below measurement level (for IV curve linearity)	V _{OB(DC)}	$0.2 \times V_{DDQ}$	V
AC output high measurement level (for output slew rate)	V _{OH(AC)}	$V_{TT} + (0.1 \times V_{DDQ})$	V
AC output low measurement level (for output slew rate)	V _{OL(AC)}	V_{TT} - $(0.1 \times V_{DDQ})$	V

Note: 1. Driver impedance of $R_{ZQ}/7$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$.

Figure 234: Connectivity Test Mode Reference Test Load

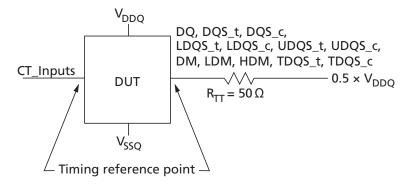


Figure 235: Connectivity Test Mode Output Slew Rate Definition

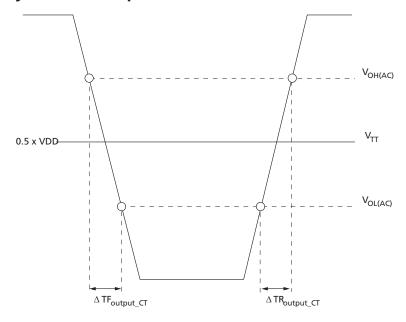


Table 119: Connectivity Test Mode Output Slew Rate

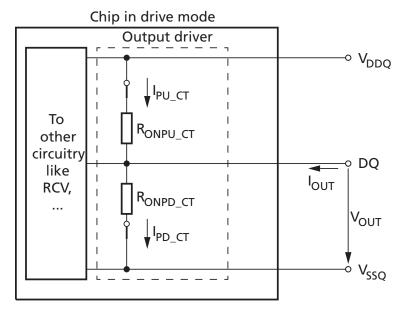
		DDR4-1600 / 1866 / 2133 / 2400		DDR4	-2666	DDR4- 32	·2933 / 00	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Output signal falling time	TF_output_CT	-	10	_	10	-	10	ns/V
Output signal rising time	TR_output_CT	_	10	_	10	_	10	ns/V

Electrical Characteristics – AC and DC Output Driver Characteristics

Connectivity Test Mode Output Driver Electrical Characteristics

The DDR4 driver supports special values during connectivity test mode. These $R_{\rm ON}$ values are referenced in this section. A functional representation of the output buffer is shown in the figure below.

Figure 236: Output Driver During Connectivity Test Mode



The output driver impedance, R_{ON} , is determined by the value of the external reference resistor R_{ZQ} as follows: $R_{ON} = R_{ZQ}/7$. This targets 34Ω with nominal $R_{ZQ} = 240\Omega$; however, connectivity test mode uses uncalibrated drivers and only a maximum target is defined. Mismatch between pull up and pull down is undefined.

The individual pull-up and pull-down resistors (R_{ONPu_CT} and R_{ONPd_CT}) are defined as follows:

 R_{ONPu_CT} when R_{ONPd_CT} is off:

$$\mathsf{R}_{\mathsf{ONPU_CT}} \, = \, \frac{\mathsf{V}_{\mathsf{DDQ}} \cdot \mathsf{V}_{\mathsf{OUT}}}{\left|\mathsf{I}_{\mathsf{OUT}}\right|}$$

R_{ONPD} CT when R_{ONPU} CT is off:

$$R_{ONPD_CT} = \frac{V_{OUT}}{|I_{OUT}|}$$

Table 120: Output Driver Electrical Characteristics During Connectivity Test Mode

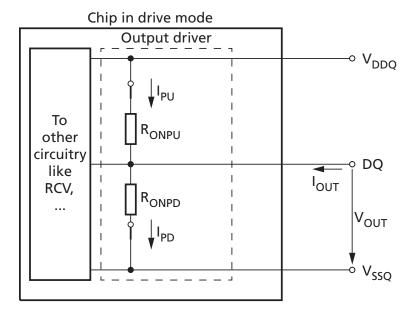
Assumes $R_{ZO} = 240\Omega$; ZQ calibration not required

R _{ON,nom_CT}	Resistor	V _{OUT}	Min	Nom	Max	Unit
		$V_{OB(DC)} = 0.2 \times V_{DDQ}$	N/A	N/A	1.9	R _{ZQ} /7
	D	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	N/A	N/A	2.0	R _{ZQ} /7
	R _{ONPD_CT}	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	N/A	N/A	2.2	R _{ZQ} /7
34Ω		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	N/A	N/A	2.5	R _{ZQ} /7
3412	R _{ONPU_CT}	$V_{OB(DC)} = 0.2 \times V_{DDQ}$	N/A	N/A	1.9	R _{ZQ} /7
		$V_{OL(DC)} = 0.5 \times V_{DDQ}$	N/A	N/A	2.0	R _{ZQ} /7
		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	N/A	N/A	2.2	R _{ZQ} /7
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	N/A	N/A	2.5	R _{ZQ} /7

Output Driver Electrical Characteristics

The DDR4 driver supports two R_{ON} values. These R_{ON} values are referred to as strong mode (low R_{ON} : 34 Ω) and weak mode (high R_{ON} : 48 Ω). A functional representation of the output buffer is shown in the figure below.

Figure 237: Output Driver: Definition of Voltages and Currents



The output driver impedance, R_{ON} , is determined by the value of the external reference resistor R_{ZQ} as follows: $R_{ON(34)} = R_{ZQ}/7$, or $R_{ON(48)} = R_{ZQ}/5$. This provides either a nominal $34.3\Omega \pm 10\%$ or $48\Omega \pm 10\%$ with nominal $R_{ZQ} = 240\Omega$.

The individual pull-up and pull-down resistors (R_{ONPu} and R_{ONPd}) are defined as follows:

R_{ONPu} when R_{ONPd} is off:

$$R_{ONPU} = \frac{V_{DDQ} - V_{OUT}}{\left|I_{OUT}\right|}$$

R_{ONPD} when R_{ONPU} is off:

$$R_{ONPD} = \frac{V_{OUT}}{\left|I_{OUT}\right|}$$

Table 121: Strong Mode (34 Ω) Output Driver Electrical Characteristics

Assumes $R_{ZO} = 240\Omega$; Entire operating temperature range after proper ZQ calibration

R _{ON,nom}	Resistor	V _{OUT}	Min	Nom	Max	Unit	Notes
		$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.73	1.00	1.10	R _{ZQ} /7	1, 2, 3
	R _{ON34PD}	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.83	1.00	1.10	R _{ZQ} /7	1, 2, 3
34Ω		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.83	1.00	1.25	R _{ZQ} /7	1, 2, 3
3412		$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.90	1.00	1.25	R _{ZQ} /7	1, 2, 3
	R _{ON34PU}	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.90	1.00	1.10	R _{ZQ} /7	1, 2, 3
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.80	1.00	1.10	R _{ZQ} /7	1, 2, 3
	n pull-up and pull- MM _{PUPD}	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	10	_	23	%	1, 2, 3, 4, 6, 7
Mismatch between DQ to DQ within byte variation pull-up, MM _{PUdd}		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	_	-	10	%	1, 2, 3, 4, 5
Mismatch between DQ to DQ within byte variation pull-down, MM _{PDdd}		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	-	_	10	%	1, 2, 3, 4, 6, 7

Notes:

- 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
- 2. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.
- 3. Micron recommends calibrating pull-down and pull-up output driver impedances at 0.8 \times V_{DDQ}. Other calibration schemes may be used to achieve the linearity specification shown above; for example, calibration at 0.5 \times V_{DDO} and 1.1 V_{DDO}.
- 4. DQ-to-DQ mismatch within byte variation for a given component including DQS_t and DQS_c (characterized).
- 5. Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD}: Measure both R_{ONPD} and R_{ONPD} at $0.8 \times V_{DDQ}$ separately; $R_{ON,nom}$ is the nominal R_{ON} value:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ON,nom}} \times 100$$

6. R_{ON} variance range ratio to R_{ON} nominal value in a given component, including DQS_t and DQS_c:

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$$MM_{PUDD} = \frac{R_{ONPU,max} - R_{ONPU,min}}{R_{ON,nom}} \times 100$$

$$MM_{PDDD} = \frac{R_{ONPD,max} - R_{ONPD,min}}{R_{ON,nom}} \times 100$$

- 7. The lower and upper bytes of a x16 are each treated on a per byte basis.
- 8. The minimum values are derated by 9% when the device operates between -40° C and 0° C (T_{c}).

Table 122: Weak Mode (48Ω) Output Driver Electrical Characteristics

Assumes $R_{ZO} = 240\Omega$; Entire operating temperature range after proper ZQ calibration

R _{ON,nom}	Resistor	V _{OUT}	Min	Nom	Max	Unit	Notes
48Ω	R _{ON48PD}	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.73	1.00	1.10	R _{ZQ} /5	1, 2, 3
		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.83	1.00	1.10	R _{ZQ} /5	1, 2, 3
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.83	1.00	1.25	R _{ZQ} /5	1, 2, 3
	R _{ON48PU}	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.90	1.00	1.25	R _{ZQ} /5	1, 2, 3
		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.90	1.00	1.10	R _{ZQ} /5	1, 2, 3
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.80	1.00	1.10	R _{ZQ} /5	1, 2, 3
	een pull-up and n, MM _{PUPD}	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	10	_	23	%	1, 2, 3, 4, 6, 7
Mismatch between DQ to DQ within byte variation pull-up, MM _{PUdd}		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	_	-	10	%	1, 2, 3, 4, 5
Mismatch between DQ to DQ within byte variation pull-down, MM _{PDdd}		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	_	_	10	%	1, 2, 3, 4, 6, 7

Notes.

- 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
- 2. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.
- 3. Micron recommends calibrating pull-down and pull-up output driver impedances at 0.8 \times V_{DDQ}. Other calibration schemes may be used to achieve the linearity specification shown above; for example, calibration at 0.5 \times V_{DDO} and 1.1 V_{DDO}.
- 4. DQ-to-DQ mismatch within byte variation for a given component including DQS_t and DQS_c (characterized).
- 5. Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD}: Measure both R_{ONPU} and R_{ONPD} at $0.8 \times V_{DDQ}$ separately; R_{ON,nom} is the nominal R_{ON} value:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ON,nom}} \times 100$$

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 R_{ON} variance range ratio to R_{ON} nominal value in a given component, including DQS_t and DQS_c:

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$$MM_{PUDD} = \frac{R_{ONPU,max} - R_{ONPU,min}}{R_{ON,nom}} \times 100$$

$$MM_{PDDD} = \frac{R_{ONPD,max} - R_{ONPD,min}}{R_{ON,nom}} \times 100$$

- 7. The lower and upper bytes of a x16 are each treated on a per byte basis.
- 8. The minimum values are derated by 9% when the device operates between -40° C and 0° C (T_{c}).

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the equations and tables below.

 $\Delta T = T - T(@calibration); \Delta V = V_{DDO} - V_{DDO}(@calibration); V_{DD} = V_{DDO}$

Table 123: Output Driver Sensitivity Definitions

Symbol	Min	Мах	Unit
R _{ONPU} @ V _{OH(DC)}	0.6 - $dR_{ON}dTH \times \Delta T $ - $dR_{ON}dVH \times \Delta V $	$1.1 _ dR_{ON}dTH \times \Delta T + dR_{ON}dVH \times \Delta V $	R _{ZQ} /6
R _{ON} @ V _{OM(DC)}	$0.9 - dR_{ON}dTM \times \Delta T - dR_{ON}dVM \times \Delta V $	$1.1 + dR_{ON}dTM \times \Delta T + dR_{ON}dVM \times \Delta V $	R _{ZQ} /6
R _{ONPD} @ V _{OL(DC)}	$0.6 - dR_{ON}dTL \times \Delta T - dR_{ON}dVL \times \Delta V $	$1.1 + dR_{ON}dTL \times \Delta T + dR_{ON}dVL \times \Delta V $	R _{ZQ} /6

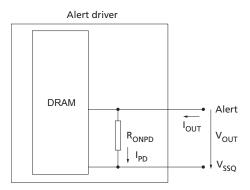
Table 124: Output Driver Voltage and Temperature Sensitivity

	Voltage and Ten		
Symbol	Min	Max	Unit
dR _{ON} dTM	0	1.5	%/°C
dR _{ON} dVM	0	0.15	%/mV
dR _{ON} dTL	0	1.5	%/°C
dR _{ON} dVL	0	0.15	%/mV
dR _{ON} dTH	0	1.5	%/°C
dR _{ON} dVM	0	0.15	%/mV

Alert Driver

A functional representation of the alert output buffer is shown in the figure below. Output driver impedance, $R_{\rm ON}$, is defined as follows.

Figure 238: Alert Driver



R_{ONPD} when R_{ONPU} is off:

$$R_{ONPD} = \frac{V_{OUT}}{\left|I_{OUT}\right|}$$

Table 125: Alert Driver Voltage

R _{ON,nom}	Register	V _{OUT}	Min	Nom	Мах	Unit
N/A	R _{ONPD}	$V_{OL(DC)} = 0.1 \times V_{DDQ}$	0.3	N/A	1.2	R _{ZQ} /7
		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.4	N/A	1.2	R _{ZQ} /7
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.4	N/A	1.4	R _{ZQ} /7

Note: 1. V_{DDO} voltage is at $V_{DDO(DC)}$.

Electrical Characteristics – On-Die Termination Characteristics

ODT Levels and I-V Characteristics

On-die termination (ODT) effective resistance settings are defined and can be selected by any or all of the following options:

- MR1[10:8] ($R_{\rm TT(NOM)}$): Disable, 240 ohms, 120 ohms, 80 ohms, 60 ohms, 48 ohms, 40 ohms, and 34 ohms.
- MR2[11:9] (R_{TT(WR)}): Disable, 240 ohms, 120 ohms, and 80 ohms.
- MR5[8:6] $(R_{TT(Park)})$: Disable, 240 ohms, 120 ohms, 80 ohms, 60 ohms, 48 ohms, 40 ohms, and 34 ohms.

ODT is applied to the following inputs:

- x4: DQ, DM_n, DQS_t, and DQS_c inputs.
- x8: DQ, DM_n, DQS_t, DQS_c, TDQS_t, and TDQS_c inputs.
- x16: DQ, LDM_n, UDM_n, LDQS_t, LDQS_c, UDQS_t, and UDQS_c inputs.

A functional representation of ODT is shown in the figure below.

Figure 239: ODT Definition of Voltages and Currents

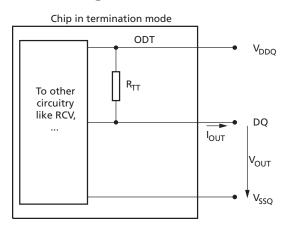


Table 126: ODT DC Characteristics

R _{TT}	V _{OUT}	Min	Nom	Max	Unit	Notes
240 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	R _{ZQ}	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	R _{ZQ}	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	R _{ZQ}	1, 2, 3
120 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	R _{ZQ} /2	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	R _{ZQ} /2	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	R _{ZQ} /2	1, 2, 3
80 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	R _{ZQ} /3	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	R _{ZQ} /3	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	R _{ZQ} /3	1, 2, 3
60 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	R _{ZQ} /4	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	R _{ZQ} /4	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	R _{ZQ} /4	1, 2, 3
48 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	R _{ZQ} /5	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	R _{ZQ} /5	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	R _{ZQ} /5	1, 2, 3
40 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	R _{ZQ} /6	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	R _{ZQ} /6	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	R _{ZQ} /6	1, 2, 3
34 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	R _{ZQ} /7	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	R _{ZQ} /7	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	R _{ZQ} /7	1, 2, 3
DQ-to-DQ mismatch within byte	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0	_	10	%	1, 2, 4, 5, 6

Notes: 1. The tolerance limits are specified after calibration to 240 ohm ±1% resistor with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see ODT Temperature and Voltage Sensitivity.

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- 2. Micron recommends calibrating pull-up ODT resistors at $0.8 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity specification shown here.
- 3. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and $V_{SSQ} = V_{SS}$.
- 4. The DQ-to-DQ mismatch within byte variation for a given component including DQS_t and DQS_c.
- 5. R_{TT} variance range ratio to R_{TT} nominal value in a given component, including DQS_t and DQS_c.

$$DQ-to-DQ mismatch = \frac{R_{TT(MAX)} - R_{TT(MIN)}}{R_{TT(NOM)}} \times 100$$

- 6. DQ-to-DQ mismatch for a x16 device is treated as two separate bytes.
- 7. For IT, AT, and UT devices, the minimum values are derated by 9% when the device operates between –40°C and 0°C (TC).

ODT Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the following equations and tables.

$$\Delta T = T - T(@ \text{ calibration}); \Delta V = V_{DDO} - V_{DDO}(@ \text{ calibration}); V_{DD} = V_{DDO}$$

Table 127: ODT Sensitivity Definitions

Parameter	Min	Мах	Unit
R _{TT} @	$0.9 - dR_{TT}dT \times \Delta T - dR_{TT}dV \times \Delta V $	1.6 + $dR_{TT}dTH \times \Delta T + dR_{TT}dVH \times \Delta V $	R _{ZQ} /n

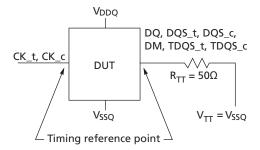
Table 128: ODT Voltage and Temperature Sensitivity

Parameter	Min	Мах	Unit	
dR _{TT} dT	0	1.5	%/°C	
dR _{TT} dV	0	0.15	%/mV	

ODT Timing Definitions

The reference load for ODT timings is different than the reference load used for timing measurements.

Figure 240: ODT Timing Reference Load



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ODT Timing Definitions

Definitions for ^tADC, ^tAONAS, and ^tAOFAS are provided in the Table 129 (page 307) and shown in Figure 241 (page 308) and Figure 243 (page 309). Measurement reference settings are provided in the subsequent Table 130 (page 307).

The ^tADC for the dynamic ODT case and read disable ODT cases are represented by ^tADC of Direct ODT Control case.

Table 129: ODT Timing Definitions

Parameter	Begin Point Definition	End Point Definition	Figure
^t ADC	Rising edge of CK_t, CK_c defined by the end point of DODTLoff	Extrapolated point at V _{RTT,nom}	Figure 241 (page 308)
	Rising edge of CK_t, CK_c defined by the end point of DODTLon	Extrapolated point at V _{SSQ}	Figure 241 (page 308)
	Rising edge of CK_t, CK_c defined by the end point of ODTLcnw	Extrapolated point at V _{RTT,nom}	Figure 242 (page 308)
	Rising edge of CK_t, CK_c defined by the end point of ODTLcwn4 or ODTLcwn8	Extrapolated point at V _{SSQ}	Figure 242 (page 308)
^t AONAS	Rising edge of CK_t, CK_c with ODT being first registered HIGH	Extrapolated point at V _{SSQ}	Figure 243 (page 309)
^t AOFAS	Rising edge of CK_t, CK_c with ODT being first registered LOW	Extrapolated point at V _{RTT,nom}	Figure 243 (page 309)

Table 130: Reference Settings for ODT Timing Measurements

Measure						
Parameter	R _{TT(Park)}	R _{TT(NOM)}	R _{TT(WR)}	VSW1	VSW2	Note
^t ADC	Disable	$R_{ZQ}/7 (34\Omega)$	_	0.20V	0.40V	1, 2, 4
	_	$R_{ZQ}/7 (34\Omega)$	High-Z	0.20V	0.40V	1, 3, 5
^t AONAS	Disable	$R_{ZQ}/7 (34\Omega)$	_	0.20V	0.40V	1, 2, 6
^t AOFAS	Disable	$R_{ZQ}/7 (34\Omega)$	_	0.20V	0.40V	1, 2, 6

- Notes: 1. MR settings are as follows: MR1 has A10 = 1, A9 = 1, A8 = 1 for $R_{TT(NOM)}$ setting; MR5 has A8 = 0, A7 = 0, A6 = 0 for $R_{TT(Park)}$ setting; and MR2 has A11 = 0, A10 = 1, A9 = 1 for R_{TT(WR)} setting.
 - 2. ODT state change is controlled by ODT pin.
 - 3. ODT state change is controlled by a WRITE command.
 - 4. Refer to Figure 241 (page 308).
 - 5. Refer to Figure 242 (page 308).
 - 6. Refer to Figure 243 (page 309).

Figure 241: ^tADC Definition with Direct ODT Control

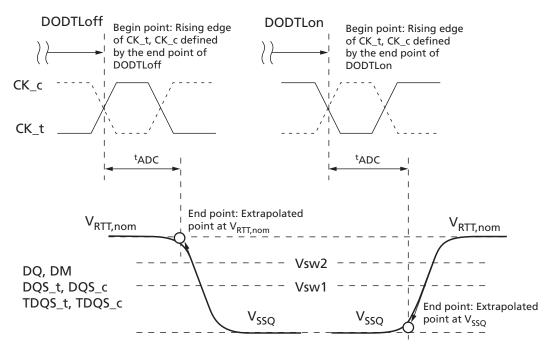


Figure 242: ^tADC Definition with Dynamic ODT Control

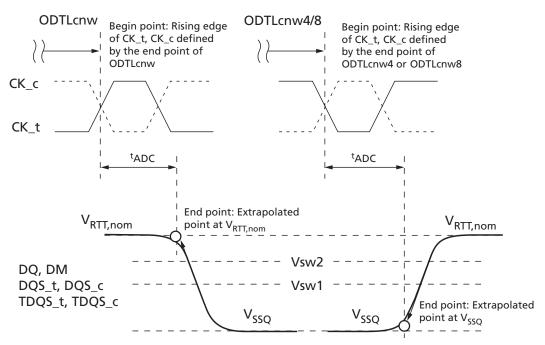
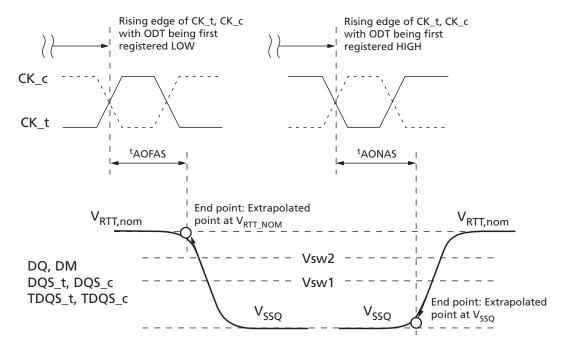


Figure 243: ^tAOFAS and ^tAONAS Definitions





DRAM Package Electrical Specifications

Table 131: DRAM Package Electrical Specifications for x4 and x8 Devices

				66/2133/ /2666	29	33	32	.00		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Input/	Zpkg	Z _{IO}	45	85	48	85	48	85	ohm	1, 2, 4
output	Package delay	Td _{IO}	14	42	14	40	14	40	ps	1, 3, 4
	Lpkg	L _{IO}	_	3.3	_	3.3	_	3.3	nH	10
	Cpkg	C _{IO}	_	0.78	_	0.78	_	0.78	pF	11
DQS_t,	Zpkg	Z _{IO DQS}	45	85	48	85	48	85	ohm	1, 2
DQS_c	Package delay	Td _{IO DQS}	14	42	14	40	14	40	ps	1, 3
	Delta Zpkg	DZ _{IO DQS}	_	10	_	10	_	10	ohm	1, 2, 6
	Delta delay	DTd _{IO DQS}	_	5	_	5	-	5	ps	1, 3, 6
	Lpkg	L _{IO DQS}	_	3.3	_	3.3	-	3.3	nH	10
	Cpkg	C _{IO DQS}	_	0.78	_	0.78	_	0.78	pF	11
Input CTRL	Zpkg	Z _{I CTRL}	50	90	50	90	50	90	ohm	1, 2, 8
pins	Package delay	Td _{I CTRL}	14	42	14	40	14	40	ps	1, 3, 8
	Lpkg	L _{I CTRL}	_	3.4	_	3.4	_	3.4	nH	10
	Cpkg	C _{I CTRL}	_	0.7	_	0.7	_	0.7	pF	11
Input CMD	Zpkg	Z _{I ADD CMD}	50	90	50	90	50	90	ohm	1, 2, 7
ADD pins	Package delay	Td _{I ADD CMD}	14	45	14	40	14	40	ps	1, 3, 7
	Lpkg	L _{I ADD CMD}	_	3.6	_	3.6	_	3.6	nH	10
	Cpkg	C _{I ADD CMD}	_	0.74	_	0.74	_	0.74	pF	11
CK_t, CK_c	Zpkg	Z _{CK}	50	90	50	90	50	90	ohm	1, 2
	Package delay	Td _{CK}	14	42	14	42	14	42	ps	1, 3
	Delta Zpkg	DZ _{DCK}	_	10	_	10	_	10	ohm	1, 2, 5
	Delta delay	DTd _{DCK}	_	5	_	5	_	5	ps	1, 3, 5
	Lpkg	L _{I CLK}	_	3.4	_	3.4	_	3.4	nH	10
	Cpkg	C _{I CLK}	_	0.7	_	0.7	_	0.7	pF	11
ZQ Zpkg		Z _{O ZQ}	_	100	_	100	_	100	ohm	1, 2
ZQ delay		Td _{O ZQ}	20	90	20	90	20	90	ps	1, 3
ALERT Zpkg		Z _{O ALERT}	40	100	40	100	40	100	ohm	1, 2
ALERT delay	'	Td _{O ALERT}	20	55	20	55	20	55	ps	1, 3

- Notes: 1. This parameter is not subject to a production test; it is verified by design and characterization and are provided for reference; system signal simulations should not use these values but use the Micron package model. The package parasitic (L and C) are validated using package only samples. The capacitance is measured with V_{DD}, V_{DDO}, V_{SS}, and V_{SSO} shorted with all other signal pins floating. The inductance is measured with V_{DD}, V_{DDO}, V_{SS}, and V_{SSO} shorted and all other signal pins shorted at the die, not pin, side.
 - 2. Package-only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where: Zpkg (total per pin) = SQRT (Lpkg/Cpkg).



- 3. Package-only delay (Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where: Tdpkg (total per pin) = SQRT (Lpkg × Cpkg).
- 4. Z_{IO} and Td_{IO} apply to DQ, DM, TDQS_t and TDQS_c.
- 5. Absolute value of ZCK_t, ZCK_c for impedance (Z) or absolute value of TdCK_t, TdCK_c for delay (Td).
- Absolute value of ZIO (DQS_t), ZIO (DQS_c) for impedance (Z) or absolute value of TdIO (DQS_t), TdIO (DQS_c) for delay (Td).
- 7. Z_{I ADD CMD} and Td_{I ADD CMD} apply to A[17:0], BA[1:0], BG[1:0], RAS_n CAS_n, WE_n, ACT_n, and PAR.
- 8. Z_{I CTRL} and Td_{I CTRL} apply to ODT, CS_n, and CKE.
- 9. Package implementations will meet specification if the Zpkg and package delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.
- 10. It is assumed that Lpkg can be approximated as Lpkg = $Z_0 \times Td$.
- 11. It is assumed that Cpkg can be approximated as Cpkg = Td/Z_O .

Table 132: DRAM Package Electrical Specifications for x16 Devices

				66/2133/ /2666	29	33	32	.00		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Input/	Zpkg	Z _{IO}	45	85	45	85	45	85	ohm	1, 2, 4
output	Package delay	Td _{IO}	14	45	14	45	14	45	ps	1, 3, 4
	Lpkg	L _{IO}	_	3.4	_	3.4	_	3.4	nH	11
	Cpkg	C _{IO}	_	0.82	_	0.82	_	0.82	pF	11
LDQS_t/	Zpkg	Z _{IO DQS}	45	85	45	85	45	85	ohm	1, 2
LDQS_c/	Package delay	Td _{IO DQS}	14	45	14	45	14	45	ps	1, 3
UDQS_t/ UDQS_c	Lpkg	L _{IO DQS}	-	3.4	_	3.4	_	3.4	nH	11
0003_0	Cpkg	C _{IO DQS}	-	0.82	_	0.82	_	0.82	pF	11
LDQS_t/	Delta Zpkg	DZ _{IO DQS}	-	10.5	_	10.5	_	10.5	ohm	1, 2, 6
LDQS_c, UDQS_t/ UDQS_c,	Delta delay	DTd _{IO DQS}	_	5	_	5	_	5	ps	1, 3, 6
Input CTRL	Zpkg	Z _{I CTRL}	50	90	50	90	50	90	ohm	1, 2, 8
pins	Package delay	Td _{I CTRL}	14	42	14	42	14	42	ps	1, 3, 8
	Lpkg	L _{I CTRL}	-	3.4	-	3.4	_	3.4	nH	11
	Cpkg	C _{I CTRL}	-	0.7	_	0.7	_	0.7	pF	11
Input CMD	Zpkg	Z _{I ADD CMD}	50	90	50	90	50	90	ohm	1, 2, 7
ADD pins	Package delay	Td _{I ADD CMD}	14	52	14	52	14	52	ps	1, 3, 7
	Lpkg	L _{I ADD CMD}	-	3.9	_	3.9	_	3.9	nH	11
	Cpkg	C _{I ADD CMD}	-	0.86	_	0.86	_	0.86	pF	11
CK_t, CK_c	Zpkg	Z _{CK}	50	90	50	90	50	90	ohm	1, 2
	Package delay	Td _{CK}	14	42	14	42	14	42	ps	1, 3
	Delta Zpkg	DZ _{DCK}	_	10.5	_	10.5	_	10.5	ohm	1, 2, 5
	Delta delay	DTd _{DCK}	-	5	_	5	-	5	ps	1, 3, 5



Table 132: DRAM Package Electrical Specifications for x16 Devices (Continued)

			1600/18 2400	66/2133/ /2666	29	33	32	00		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Input CLK	Lpkg	L _{I CLK}	_	3.4	_	3.4	_	3.4	nH	11
	Cpkg	C _{I CLK}	-	0.7	_	0.7	_	0.7	pF	11
ZQ Zpkg		Z _{O ZQ}	_	100	_	100	_	100	ohm	1, 2
ZQ delay		Td _{O ZQ}	20	90	20	90	20	90	ps	1, 3
ALERT Zpkg		Z _{O ALERT}	40	100	40	100	40	100	ohm	1, 2
ALERT delay	1	Td _{O ALERT}	20	55	20	55	20	55	ps	1, 3

- Notes: 1. This parameter is not subject to a production test; it is verified by design and characterization and are provided for reference; system signal simulations should not use these values but use the Micron package model. The package parasitic (L and C) are validated using package only samples. The capacitance is measured with V_{DD} , V_{DDQ} , V_{SS} , and V_{SSQ} shorted with all other signal pins floating. The inductance is measured with VDD, VDDO, V_{SS}, and V_{SSO} shorted and all other signal pins shorted at the die, not pin, side.
 - 2. Package-only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where: Zpkg (total per pin) = SQRT (Lpkg/Cpkg).
 - 3. Package-only delay (Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where: Tdpkg (total per pin) = SQRT (Lpkg × Cpkg).
 - 4. Z_{IO} and Td_{IO} apply to DQ, DM, TDQS_t and TDQS_c.
 - 5. Absolute value of ZCK_t, ZCK_c for impedance (Z) or absolute value of TdCK_t, TdCK_c for delay (Td).
 - 6. Absolute value of ZIO (DQS_t), ZIO (DQS_c) for impedance (Z) or absolute value of TdIO (DQS_t), TdIO (DQS_c) for delay (Td).
 - 7. $Z_{IADD\ CMD}$ and $Td_{IADD\ CMD}$ apply to A[17:0], BA[1:0], BG[1:0], RAS_n CAS_n, WE_n, ACT_n, and PAR.
 - 8. $Z_{I \ CTRL}$ and $Td_{I \ CTRL}$ apply to ODT, CS_n, and CKE.
 - 9. Package implementations will meet specification if the Zpkg and package delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.
 - 10. It is assumed that Lpkg can be approximated as Lpkg = $Z_O \times Td$.
 - 11. It is assumed that Cpkg can be approximated as Cpkg = Td/Z_O .



Table 133: Pad Input/Output Capacitance

			-1600, 2133		-2400, 66	DDR4	-2933	DDR4	-3200		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Input/output capacitance: DQ, DM, DQS_t, DQS_c, TDQS_t, TDQS_c	C _{IO}	0.55	1.4	0.55	1.15	0.55	1.00	0.55	1.00	pF	1, 2, 3
Input capacitance: CK_t and CK_c	C _{CK}	0.2	0.8	0.2	0.7	0.2	0.7	0.15	0.7	pF	2, 3
Input capacitance delta: CK_t and CK_c	C _{DCK}	-	0.05	-	0.05	-	0.05	-	0.05	pF	2, 3, 6
Input/output capacitance del- ta: DQS_t and DQS_c	C _{DDQS}	-	0.05	-	0.05	-	0.05	-	0.05	pF	2, 3, 5
Input capacitance: CTRL, ADD, CMD input-only pins	C _I	0.2	0.8	0.2	0.7	0.2	0.6	0.15	0.55	pF	2, 3, 4
Input capacitance delta: All CTRL input-only pins	C _{DI_CTRL}	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	2, 3, 8, 9
Input capacitance delta: All ADD/CMD input-only pins	C _{DI_ADD_CM}	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1, 2, 10, 11
Input/output capacitance del- ta: DQ, DM, DQS_t, DQS_c, TDQS_t, TDQS_c	C _{DIO}	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1, 2, 3, 4
Input/output capacitance: ALERT pin	C _{ALERT}	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	pF	2, 3
Input/output capacitance: ZQ pin	C _{ZQ}	-	2.3	-	2.3	-	2.3	-	2.3	pF	2, 3, 12
Input/output capacitance: TEN pin	C _{TEN}	0.2	2.3	0.2	2.3	0.2	2.3	0.15	2.3	рF	2, 3, 13

- Notes: 1. Although the DM, TDQS_t, and TDQS_c pins have different functions, the loading matches DQ and DQS.
 - 2. This parameter is not subject to a production test; it is verified by design and characterization and are provided for reference; system signal simulations should not use these values but use the Micron package model. The capacitance, if and when, is measured according to the JEP147 specification, "Procedure for Measuring Input Capacitance Using a Vector Network Analyzer (VNA)," with V_{DD} , V_{DDQ} , V_{SS} , and V_{SSQ} applied and all other pins floating (except the pin under test, CKE, RESET_n and ODT, as necessary). V_{DD} = $V_{DDO} = 1.2V$, $V_{BIAS} = V_{DD}/2$ and on-die termination off. Measured data is rounded using industry standard half-rounded up methodology to the nearest hundredth of the MSB.
 - 3. This parameter applies to monolithic die, obtained by de-embedding the package L and
 - 4. $C_{DIO} = C_{IO}(DQ, DM) 0.5 \times (C_{IO}(DQS_t) + C_{IO}(DQS_c))$.
 - 5. Absolute value of C_{IO} (DQS_t), C_{IO} (DQS_c)
 - 6. Absolute value of CCK_t, CCK_c
 - 7. C_I applies to ODT, CS_n, CKE, A[17:0], BA[1:0], BG[1:0], RAS_n, CAS_n, ACT_n, PAR and
 - 8. C_{DI CTRI} applies to ODT, CS_n, and CKE.



- 9. $C_{DI_CTRL} = C_I(CTRL) 0.5 \times (C_I(CLK_t) + C_I(CLK_c)).$
- 10. C_{DI_ADD_CMD} applies to A[17:0], BA1:0], BG[1:0], RAS_n, CAS_n, ACT_n, PAR and WE_n.
- 11. $C_{DI_ADD_CMD} = C_I(ADD_CMD) 0.5 \times (C_I(CLK_t) + C_I(CLK_c)).$
- 12. Maximum external load capacitance on ZQ pin: 5pF.
- 13. Only applicable if TEN pin does not have an internal pull-up.

Thermal Characteristics

Table 134: Thermal Characteristics

Parameter/	Condition		Value	Units	Symbol	Notes
	ase temperatur	re:	0 to +85	°C	T _C	1, 2, 3
Commercial			0 to +95	°C	T _C	1, 2, 3, 4
Operating case temperature:			-40 to +85	°C	T _C	1, 2, 3
Industrial			-40 to +95	°C	T _C	1, 2, 3, 4
Operating case temperature:		-40 to +85	°C	T _C	1, 2, 3	
Automotive		-40 to +105	°C	T _C	1, 2, 3, 4	
	78-ball	Junction-to-case (TOP)	3.1	°C/W	ΘJC	5
REV A	"PM"	Junction-to-board	10.6	°C/W	ΘЈВ	
NEV A	96-ball	Junction-to-case (TOP)	3.0	°C/W	ΘJC	5
	"HA"	Junction-to-board	9.9	°C/W	ΘЈВ	
	78-ball	Junction-to-case (TOP)	3.5	°C/W	ΘJC	5
REV B	"WE"	Junction-to-board	21	°C/W	ΘЈВ	
NEV D	96-ball "JY"	Junction-to-case (TOP)	4.1	°C/W	ΘJC	5
		Junction-to-board	16.2	°C/W	ΘJB	
	, , , , , , , , , , , , , , , , , , , ,	Junction-to-case (TOP)	3.2	°C/W	ΘJC	5
REV D	"WE"	Junction-to-board	20.2	°C/W	ΘЈВ	
KEVD	96-ball "LY"	Junction-to-case (TOP)	TBD	°C/W	ΘJC	5
	90-Dali Li	Junction-to-board	TBD	°C/W	ΘJB	
	78-ball "SA"	Junction-to-case (TOP)	4.9	°C/W	ΘJC	5
REV E	76-ball 3A	Junction-to-board	14.2	°C/W	ΘJB	
KEVE	96-ball "LY"	Junction-to-case (TOP)	4.8	°C/W	ΘJC	5
	90-Dali Li	Junction-to-board	15.2	°C/W	ΘJB	
	78-ball	Junction-to-case (TOP)	2.8	°C/W	ΘJC	5
REV G	"WE"	Junction-to-board	13.1	°C/W	ΘJB	
KLVG	N/A	Junction-to-case (TOP)	N/A	°C/W	ΘJC	5
	IN/A	Junction-to-board	N/A	°C/W	ΘJB	
	78-ball "SA"	Junction-to-case (TOP)	4.4	°C/W	ΘJC	5
REV H	70-Dali 3A	Junction-to-board	13.2	°C/W	ΘJB	
I\LV II	96-ball "LY"	Junction-to-case (TOP)	3.4	°C/W	ΘJC	5
	Jo-Dali Li	Junction-to-board	14.7	°C/W	ΘJB	

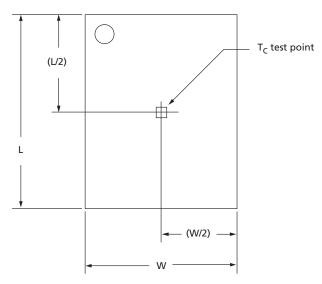


Table 134: Thermal Characteristics (Continued)

Parameter/0	Condition		Value	Units	Symbol	Notes
	78-ball "SA"	Junction-to-case (TOP)	6.0	°C/W	ΘJC	5
REV J	78-ball "SA"	Junction-to-board	17.9	°C/W	ΘЈВ	
VEA 1	96-ball "TB"	Junction-to-case (TOP)	5.9	°C/W	ΘJC	5
	90-Dall ID	Junction-to-board	17.4	°C/W	ΘJB	

- Notes: 1. MAX operating case temperature. T_C is measured in the center of the package.
 - 2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_C during operation.
 - 3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
 - 4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate.
 - 5. The thermal resistance data is based off of a typical number.

Figure 244: Thermal Measurement Point



Current Specifications – Measurement Conditions

I_{DD}, I_{PP}, and I_{DDO} Measurement Conditions

 I_{DD} , I_{PP} , and I_{DDO} measurement conditions, such as test load and patterns, are defined in this section.

- $\bullet \ \ I_{DD} \ currents \ (I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2P}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, I_{DD5R}, I_{DD5R}$ I_{DD6N} , I_{DD6E} , I_{DD6R} , I_{DD6A} , I_{DD7} , and I_{DD8}) are measured as time-averaged currents with all V_{DD} balls of the device under test grouped together.
- I_{PP} currents are I_{PP3N} for standby cases (I_{DD2N}, I_{DD2NT}, I_{DD2P}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD8}), $I_{PP0} \ for \ active \ cases \ (I_{DD0},I_{DD1},I_{DD4R},I_{DD4W}), \ I_{PP5R} \ for \ the \ distributed \ refresh \ case$ (I_{DD5R}), I_{PP6x} for self refresh cases (I_{DD6N}, I_{DD6E}, I_{DD6R}, I_{DD6A}) and I_{PP7} for the operating



8Gb: x4, x8, x16 DDR4 SDRAM Current Specifications – Measurement Conditions

bank interleave read case (I_{DD7}). These have the same definitions as the I_{DD} currents referenced but are measured on the V_{PP} supply.

- I_{DDQ} currents are measured as time-averaged currents with V_{DDQ} balls of the device under test grouped together. Micron does not specify I_{DDQ} currents.
- I_{PP} and I_{DDQ} currents are not included in I_{DD} currents, I_{DD} and I_{DDQ} currents are not included in I_{PP} currents, and I_{DD} and I_{PP} currents are not included in I_{DDQ} currents.

Note: I_{DDQ} values cannot be directly used to calculate the I/O power of the device. They can be used to support correlation of simulated I/O power to actual I/O power. In DRAM module application, I_{DDQ} cannot be measured separately because V_{DD} and V_{DDQ} are using a merged-power layer in the module PCB.

The following definitions apply for I_{DD} , I_{PP} and I_{DDO} measurements.

- "0" and "LOW" are defined as $V_{IN} \le V_{IL(AC)max}$
- "1" and "HIGH" are defined as V_{IN} ≥V_{IH(AC)min}
- "Midlevel" is defined as inputs $V_{REF} = V_{DD}/2$
- Timings used for I_{DD}, I_{PP} and I_{DDQ} measurement-loop patterns are provided in the Current Test Definition and Patterns section.
- Basic I_{DD}, I_{PP}, and I_{DDQ} measurement conditions are described in the Current Test Definition and Patterns section.
- Detailed I_{DD}, I_{PP}, and I_{DDQ} measurement-loop patterns are described in the Current Test Definition and Patterns section.
- Current measurements are done after properly initializing the device. This includes, but is not limited to, setting:

 $R_{ON} = R_{ZO}/7$ (34 ohm in MR1);

Qoff = 0B (output buffer enabled in MR1);

 $R_{TT(NOM)} = R_{ZO}/6$ (40 ohm in MR1);

 $R_{TT(WR)} = R_{ZO}/2$ (120 ohm in MR2);

 $R_{TT(Park)} = disabled;$

TDQS feature disabled in MR1; CRC disabled in MR2; CA parity feature disabled in MR3; Gear-down mode disabled in MR3; Read/Write DBI disabled in MR5; DM disabled in MR5

- Define D = {CS_n, RAS_n, CAS_n, WE_n}: = {HIGH, LOW, LOW, LOW}; apply BG/BA changes when directed.
- Define D_n = {CS_n, RAS_n, CAS_n, WE_n}: = {HIGH, HIGH, HIGH, HIGH}; apply invert of BG/BA changes when directed above.

Note: The measurement-loop patterns must be executed at least once before actual current measurements can be taken.



Figure 245: Measurement Setup and Test Load for I_{DDx} , I_{PPx} , and I_{DDQx}

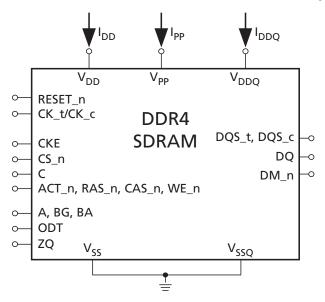
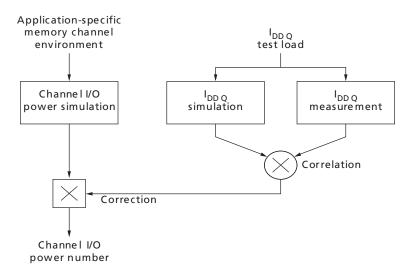


Figure 246: Correlation: Simulated Channel I/O Power to Actual Channel I/O Power



Note: 1. Supported by I_{DDO} measurement.

IDD Definitions

Table 135: Basic I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions

Symbol	Description
I _{DD0}	Operating One Bank Active-Precharge Current (AL = 0)
	CKE: HIGH; External clock: On; ^t CK, nRC, nRAS, CL: see the previous table; BL: 8; ¹ AL: 0; CS_n: HIGH between
	ACT and PRE; Command, address, bank group address, bank address inputs: partially toggling according to the
	next table; Data I/O: V _{DDQ} ; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2,
	2, (see the I _{DD0} Measurement-Loop Pattern table); Output buffer and R _{TT} : enabled in mode registers; ² ODT
	signal: stable at 0; Pattern details: see the I _{DD0} Measurement-Loop Pattern table



Table 135: Basic I_{DD} , I_{PP} , and I_{DDQ} Measurement Conditions (Continued)

Symbol	Description
I _{PPO}	Operating One Bank Active-Precharge I _{PP} Current (AL = 0) Same conditions as I _{DD0} above
I _{DD1}	Operating One Bank Active-Read-Precharge Current (AL = 0) CKE: HIGH; External clock: on; t CK, n RC, n RAS, n RCD, CL: see the previous table; BL: 8; 1,5 AL: 0; CS_n: HIGH between ACT, RD, and PRE; Command, address, bank group address, bank address inputs, Data I/O: partially toggling according to the I_{DD1} Measurement-Loop Pattern table; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, (see the following table); Output buffer and R_{TT} : enabled in mode registers; ODT Signal: stable at 0; Pattern details: see the I_{DD1} Measurement-Loop Pattern table
I _{DD2N}	Precharge Standby Current (AL = 0) CKE: HIGH; External clock: On; t CK, CL: see the previous table; BL: 8; 1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table; Data I/O: V_{DDQ} ; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT} : enabled in mode registers; ODT signal: stable at 0; Pattern details: see the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table
I _{DD2NT}	Precharge Standby ODT Current CKE: HIGH; External clock: on; ^t CK, CL: see the previous table; BL: 8; ¹ AL: 0; CS_n: stable at 1; Command, address, bank gropup address, bank address inputs: partially toggling according to the I _{DD2NT} Measurement-Loop Pattern table; Data I/O: V _{SSQ} ; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R _{TT} : enabled in mode registers; ² ODT signal: toggling according to the I _{DD2NT} Measurement-Loop Pattern table; Pattern details: see the I _{DD2NT} Measurement-Loop Pattern table
I _{DD2P}	Precharge Power-Down Current CKE: LOW; External clock: on; ^t CK, CL: see the previous table; BL: 8; ¹ AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: V _{DDQ} ; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R _{TT} : Enabled in mode registers; ² ODT signal: stable at 0
I _{DD2Q}	Precharge Quiet Standby Current CKE: HIGH; External clock: on; ^t CK, CL: see the previous table; BL: 8; ¹ AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: V _{DDQ} ; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R _{TT} : Enabled in mode registers; ² ODT signal: stable at 0
I _{DD3N}	Active Standby Current (AL = 0) CKE: HIGH; External clock: on; t CK, CL: see the previous table; BL: 8; 1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table; Data I/O: V_{DDQ} ; DM_n: stable at 1; Bank activity: all banks open; Output buffer and R_{TT} : Enabled in mode registers; 2 ODT signal: stable at 0; Pattern details: see the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table
I _{PP3N}	Active Standby I _{PP3N} Current (AL = 0) Same conditions as I _{DD3N} above
I _{DD3P}	Active Power-Down Current (AL = 0) CKE: LOW; External clock: on; t CK, CL: see the previous table; BL: 8; t AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 1; Data I/O: t CDDQ; DM_n: stable at 1; Bank activity: all banks open; Output buffer and t RT: Enabled in mode registers; t 2 ODT signal: stable at 0



Table 135: Basic I_{DD} , I_{PP} , and I_{DDQ} Measurement Conditions (Continued)

Symbol	Description
I _{DD4R}	Operating Burst Read Current (AL = 0) CKE: HIGH; External clock: on; t CK, CL: see the previous table; BL: 8; 15 AL: 0; CS_n: HIGH between RD; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD4R} Measurement-Loop Pattern table; Data I/O: seamless read data burst with different data between one burst and the next one according to the I_{DD4R} Measurement-Loop Pattern table; DM_n: stable at 1; Bank activity: all banks open, RD commands cycling through banks: 0, 0, 1, 1, 2, 2, (see the I_{DD4R} Measurement-Loop Pattern table); Output buffer and I_{TT} : Enabled in mode registers; ODT signal: stable at 0; Pattern details: see the I_{DD4R} Measurement-Loop Pattern table
I _{DD4W}	Operating Burst Write Current (AL = 0) CKE: HIGH; External clock: on; t CK, CL: see the previous table; BL: 8; AL: 0; CS_n: HIGH between WR; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD4W} Measurement-Loop Pattern table; Data I/O: seamless write data burst with different data between one burst and the next one according to the I_{DD4W} Measurement-Loop Pattern table; DM: stable at 0; Bank activity: all banks open, WR commands cycling through banks: 0, 0, 1, 1, 2, 2, (see I_{DD4W} Measurement-Loop Pattern table); Output buffer and R_{TT} : enabled in mode registers (see note2); ODT signal: stable at HIGH; Pattern details: see the I_{DD4W} Measurement-Loop Pattern table
I _{DD5R}	Distributed Refresh Current (1X REF) CKE: HIGH; External clock: on; ^t CK, CL, nREFI: see the previous table; BL: 8; ¹ AL: 0; CS_n: HIGH between REF; Command, address, bank group address, bank address inputs: partially toggling according to the I _{DDSR} Measurement-Loop Pattern table; Data I/O: V _{DDQ} ; DM_n: stable at 1; Bank activity: REF command every nREFI (see the I _{DDSR} Measurement-Loop Pattern table); Output buffer and R _{TT} : enabled in mode registers ² ; ODT signal: stable at 0; Pattern details: see the I _{DDSR} Measurement-Loop Pattern table
I _{PP5R}	Distributed Refresh Current (1X REF) Same conditions as I _{DDSR} above
I _{DD6N}	Self Refresh Current: Normal Temperature Range T _C : 0–85°C; Auto self refresh (ASR): disabled; ³ Self refresh temperature range (SRT): normal; ⁴ CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the table above; BL: 8; ¹ AL: 0; CS_n, command, address, bank group address, bank address, data I/O: V _{DDQ} ; DM_n: stable at 1; Bank activity: SELF REFRESH operation; Output buffer and R _{TT} : enabled in mode registers; ² ODT signal: midlevel
I _{DD6E}	Self Refresh Current: Extended Temperature Range ⁴ T _C : 0–95°C; Auto self refresh (ASR): disabled ⁴ ; Self refresh temperature range (SRT): extended; CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the previous table; BL: 8; AL: 0; CS_n, command, address, group bank address, bank address, data I/O: V _{DDQ} ; DM_n: stable at 1; Bank activity: EXTENDED TEMPERATURE SELF REFRESH operation; Output buffer and R _{TT} : enabled in mode registers; ODT signal: midlevel
I _{PP6x}	Self Refresh I _{PP} Current Same conditions as I _{DD6E} above
I _{DD6R}	Self Refresh Current: Reduced Temperature Range T _C : 0–45°C; Auto self refresh (ASR): disabled; Self refresh temperature range (SRT): reduced; ⁴ CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the previous table; BL: 8; ¹ AL: 0; CS_n, command, address, bank group address, bank address, data I/O: V _{DDQ} ; DM_n: stable at 1; Bank activity: EXTENDED TEMPERATURE SELF REFRESH operation; Output buffer and R _{TT} : enabled in mode registers; ² ODT signal: midlevel

8Gb: x4, x8, x16 DDR4 SDRAM Current Specifications – Measurement Conditions

Table 135: Basic I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions (Continued)

Symbol	Description
I _{DD7}	Operating Bank Interleave Read Current CKE: HIGH; External clock: on; [†] CK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see the previous table; BL: 8; ¹⁵ AL: CL - 1; CS_n: HIGH between ACT and RDA; Command, address, group bank address, bank address inputs: partially toggling according to the I _{DD7} Measurement-Loop Pattern table; Data I/O: read data bursts with different data between one burst and the next one according to the I _{DD7} Measurement-Loop Pattern table; DM: stable at 1; Bank activity: two times interleaved cycling through banks (0, 1,7) with different addressing, see the I _{DD7} Measurement-Loop Pattern table; Output buffer and R _{TT} : enabled in mode registers; ² ODT signal: stable at 0; Pattern details: see the I _{DD7} Measurement-Loop Pattern table
I _{PP7}	Operating Bank Interleave Read I_{PP} Current Same conditions as I _{DD7} above
I _{DD8}	Maximum Power Down Current Place DRAM in MPSM then CKE: HIGH; External clock: on; ^t CK, CL: see the previous table; BL: 8; ¹ AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: V _{DDQ} ; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R _{TT} : Enabled in mode registers; ² ODT signal: stable at 0

Notes:

- 1. Burst length: BL8 fixed by MRS: set MR0[1:0] 00.
- 2. Output buffer enable: set MR1[12] 0 (output buffer enabled); set MR1[2:1] 00 ($R_{ON} = R_{ZQ}/7$); $R_{TT(NOM)}$ enable: set MR1[10:8] 011 ($R_{ZQ}/6$); $R_{TT(WR)}$ enable: set MR2[11:9] 001 ($R_{ZO}/2$), and $R_{TT(Park)}$ enable: set MR5[8:6] 000 (disabled).
- 3. Auto self refresh (ASR): set MR2[6] 0 to disable or MR2[6] 1 to enable feature.
- 4. Self refresh temperature range (SRT): set MR2[7] 0 for normal or MR2[7] 1 for extended temperature range.
- 5. READ burst type: Nibble sequential, set MR0[3] 0.
- 6. In the dual-rank DDP case, note the following IDD measurement considerations:
 - For all IDD measurements except IDD6, the unselected rank should be in an IDD2P condition.
 - For all IPP measurements except IPP6, the unselected rank should be in an IDD3N condition.
 - For all IDD6/IPP6 measurements, both ranks should be in the same IDD6 condition.



Current Specifications – Patterns and Test Conditions

Current Test Definitions and Patterns

Table 136: I_{DD0} and I_{PP0} Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Cycle	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ООТ	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³
		0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	_
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	_
			3, 4	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	_
					Repeat pattern 14 until nRAS - 1; truncate if necessary														
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	_
					Repeat pattern 14 until nRC - 1; truncate if necessary														
		1	1 × <i>n</i> RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 1 instead															
		2	2 × <i>n</i> RC	Repeat sub-loop 0, use $BG[1:0] = 0$, use $BA[1:0] = 2$ instead															
	٦.	3	3 × <i>n</i> RC	Repeat sub-loop 0, use $BG[1:0] = 1$, use $BA[1:0] = 3$ instead															
ling	Hig	4	4 × <i>n</i> RC	Repeat sub-loop 0, use $BG[1:0] = 0$, use $BA[1:0] = 1$ instead															
Toggling	Static High	5	5 × <i>n</i> RC		Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 2 instead														
-	St	6	6 × <i>n</i> RC	Repeat sub-loop 0, use $BG[1:0] = 0$, use $BA[1:0] = 3$ instead															
		7	7 × <i>n</i> RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	8 × <i>n</i> RC				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 2	, use	BA[1:	0] = 0) inst	ead ⁴	
		9	9 × <i>n</i> RC				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 3	, use	BA[1:	0] = 1	1 inste	ead ⁴	
		10	10 × <i>n</i> RC				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 2	, use	BA[1:	0] = 2	2 inste	ead ⁴	
		11	11 × <i>n</i> RC				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 3	, use	BA[1:	0] = 3	3 inste	ead ⁴	
		12	12 × <i>n</i> RC				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 2	, use	BA[1:	0] = 1	1 inste	ead ⁴	
		13	13 × <i>n</i> RC				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 3	, use	BA[1:	0] = 2	2 inste	ead ⁴	
		14	14 × <i>n</i> RC				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 2	, use	BA[1:	0] = 3	3 inste	ead ⁴	
		15	15 × <i>n</i> RC				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 3	, use	BA[1:	0] = 0) inst	ead ⁴	

- Notes: 1. DQS_t, DQS_c are V_{DDQ}.
 - 2. BG1 is a "Don't Care" for x16 devices.
 - 3. DQ signals are V_{DDQ} .
 - 4. For x4 and x8 only.



Table 137: I_{DD1} Measurement – Loop Pattern¹

CK_c, CK_t,	CKE	Sub-Loop	Cycle	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	DDT	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³
		0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	_
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	_
			3, 4	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	_
						Rep	peat	patte	ern 1.	4 u	ntil <i>n</i>	RCD	- AL	- 1; t	runca	ate if	nece	essar	y
			nRCD - AL	RD	RD $\begin{vmatrix} 0 & 1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 &$												D0 = 00, D1 =		
					Repe	at pa	atter	n 1	4 unt	il <i>n</i> R	AS -	1; tru	ıncat	e if n	eces	sary			D2 = FF, D3 =
			<i>n</i> RAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	00,
					Repeat pattern 14 until nRC - 1; truncate if necessary D4 = FF, D5 = 00, D5 = 00, D7 = FF														
		1	1 × <i>n</i> RC + 0	ACT	0	0	0	1	1	0	1	1	0	0	0	0	0	0	-
			1 × nRC + 1,	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1 × <i>n</i> RC + 3,	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
					Rep	eat p	atter	n <i>n</i> R	C + 1	4 u	ıntil '	1 × n	RC +	nRA:	5 - 1;	trun	cate	if ne	cessary
ng	Static High		1 × <i>n</i> RC + <i>n</i> RCD - AL	RD	0	1	1	0	1	0	1	1	0	0	0	0	0	0	D0 = FF, D1 = 00,
Toggling	Fi F	Repeat pattern 14 until $nRAS - 1$; truncate if necessary $D2 = 00$													D2 = 00, D3 =				
7	Sta		1 × <i>n</i> RC + <i>n</i> RAS	PRE	0	1	0	1	0	0	1	1	0	0	0	0	0	0	FF, D4 = 00, D5 = FF,
				Repe	D DC												D5 = FF, D7 = 00		
		2	2 × <i>n</i> RC			Re	epea	t sub	-loop	0, u	se BG	i[1:0]	= 0,	use l	3A[1:	= [0:	2 ins	tead	
		3	3 × <i>n</i> RC			Re	epea	t sub	-loop	0, u	se BG	[1:0]	= 1,	use l	3A[1:	= [0:	3 inst	tead	
		4	4 × <i>n</i> RC			Re	epea	t sub	-loop	0, u	se BG	[1:0]	= 0,	use l	3A[1:	= [0	1 ins	tead	
		5	5 × <i>n</i> RC			Re	epea ⁻	t sub	-loop	0, u	se BG	[1:0]	= 1,	use I	3A[1:	= [0	2 ins	tead	
		6	6 × <i>n</i> RC				•		-loop										
		7	7 × <i>n</i> RC						-loop										
		8	9 × <i>n</i> RC						loop										
		9	10 × <i>n</i> RC						loop										
		10	11 × nRC				•		loop										
		11	12 × nRC						loop										
		12	13 × nRC						loop										
		13	14 × nRC						loop										
		14	15 × nRC				•		loop										
		15	16 × <i>n</i> RC			ĸe	peat	sub-	loop	u, us	e 80	[1:0]	= 3,	use E	A[I:	υ] = (J INST	еаат	

Notes: 1. DQS_t, DQS_c are V_{DDQ} when not toggling.



8Gb: x4, x8, x16 DDR4 SDRAM Current Specifications – Patterns and Test Conditions

- 2. BG1 is a "Don't Care" for x16 devices.
- 3. DQ signals are V_{DDQ} except when burst sequence drives each DQ signal by a READ com-
- 4. For x4 and x8 only.

Table 138: I_{DD2N}, I_{DD3N}, and I_{PP3P} Measurement - Loop Pattern¹

CK_c, CK_t,	CKE	Sub-Loop	Cycle	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³
		0	0	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	_
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	_
			2	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	_
			3	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	_
		1	4–7	Repeat sub-loop 0, use $BG[1:0] = 1$, use $BA[1:0] = 1$ instead															
		2	8–11	Repeat sub-loop 0, use $BG[1:0] = 0$, use $BA[1:0] = 2$ instead															
		3	12–15	Repeat sub-loop 0, use $BG[1:0] = 1$, use $BA[1:0] = 3$ instead															
		4	16–19	Repeat sub-loop 0, use $BG[1:0] = 0$, use $BA[1:0] = 1$ instead															
ng	High	5	20–23	Repeat sub-loop 0, use $BG[1:0] = 1$, use $BA[1:0] = 2$ instead															
Toggling	i 고	6	24–27	Repeat sub-loop 0, use $BG[1:0] = 0$, use $BA[1:0] = 3$ instead															
P	Static	7	28–31		Repeat sub-loop 0, use $BG[1:0] = 1$, use $BA[1:0] = 0$ instead														
		8	32–35	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead ⁴															
		9	36–39				Rep	eat su	ıb-loo	ор 0,	use B	G[1:0)] = 3	, use	BA[1:	0] = 1	inste	ead ⁴	
		10	40–43				Rep	eat su	ıb-loo	op 0,	use B	G[1:0)] = 2	, use	BA[1:	0] = 2	2 inste	ead ⁴	
		11	44–47				Rep	eat su	ıb-loo	ор 0,	use B	G[1:0)] = 3	, use	BA[1:	0] = 3	3 inste	ead ⁴	
		12	48–51				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 2	, use	BA[1:	0] = 1	inste	ead ⁴	
		13	52–55				Rep	eat su	ıb-loo	р 0,	use B	G[1:0)] = 3,	, use	BA[1:	0] = 2	2 inste	ead ⁴	
		14	56–59				Rep	eat su	ıb-lo	ор 0,	use B	G[1:0)] = 2	, use	BA[1:	0] = 3	3 inste	ead ⁴	
		15	60–63				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 3,	, use	BA[1:	0] = 0) inste	ead ⁴	

- Notes: 1. DQS_t, DQS_c are V_{DDQ}.
 - 2. BG1 is a "Don't Care" for x16 devices.
 - 3. DQ signals are V_{DDQ} .
 - 4. For x4 and x8 only.

Table 139: IDD2NT Measurement - Loop Pattern¹

CK_c, CK_t,	CKE	Sub-Loop	Cycle	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ОБТ	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³
		0	0	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	_
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	_
			2	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	_
			3	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	_
		1	4–7	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 1 instead															
		2	8–11	Repeat sub-loop 0 with ODT = 0, use $BG[1:0] = 0$, use $BA[1:0] = 2$ instead															
		3	12–15	Repeat sub-loop 0 with ODT = 1, use $BG[1:0] = 1$, use $BA[1:0] = 3$ instead															
		4	16–19		Repeat sub-loop 0 with ODT = 0, use $BG[1:0] = 0$, use $BA[1:0] = 1$ instead														
ng	High	5	20–23	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 2 instead															
Toggling	ic H	6	24–27		Repeat sub-loop 0 with ODT = 0, use $BG[1:0] = 0$, use $BA[1:0] = 3$ instead														
Tog	Static	7	28–31		Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 0 instead														
		8	32–35		Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 2, use BA[1:0] = 0 instead ⁴														
		9	36–39		F	Repea	t sub	-loop	0 wi	th O)T = 1	1, use	BG[1	:0] =	3, us	e BA[1:0] =	= 1 in:	stead ⁴
		10	40–43		F	Repea	t sub	-loop	0 wi	th O) = TC), use	BG[1	:0] =	2, us	e BA[1:0] =	= 2 in:	stead ⁴
		11	44–47		F	Repea	t sub	-loop	0 wi	th O)T = 1	1, use	BG[1	:0] =	3, us	e BA[1:0] =	= 3 in:	stead ⁴
		12	48–51		F	Repea	t sub	-loop	0 wi	th O[) = TC), use	BG[1	:0] =	2, us	e BA[1:0] =	= 1 in:	stead ⁴
		13	52–55		F	Repea	t sub	-loop	0 wi	th O[DT = 1	1, use	BG[1	:0] =	3, us	e BA[1:0] =	= 2 in:	stead ⁴
		14	56–59		F	Repea	t sub	-loop	0 wi	th O[) = TC), use	BG[1	:0] =	2, us	e BA[1:0] =	= 3 in:	stead ⁴
		15	60–63		F	Repea	t sub	-loop	0 wi	th O[DT = 1	1, use	BG[1	:0] =	3, us	e BA[1:0] =	= 0 in:	stead ⁴

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- Notes: 1. DQS_t, DQS_c are V_{SSQ}.
 - 2. BG1 is a "Don't Care" for x16 devices.
 - 3. DQ signals are V_{SSQ}.
 - 4. For x4 and x8 only.



Table 140: I_{DD4R} Measurement – Loop Pattern¹

CK_c, CK_t,	CKE	Sub-Loop	Cycle	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ОБТ	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³
		0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	D0 = 00, D1 =
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	FF, D2 = FF, D3 =
			2, 3	D_n,	1	1	1	1	1	0	3	3	0	0	0	7	F	0	00,
				D_n															D4 = FF, D5 =
																			00,
																			D5 = 00, D7 = FF
		1	4	RD	0	1	1	0	1	0	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	D2 = 00, D3 =
			6, 7	D_n,	1	1	1	1	1	0	3	3	0	0	0	7	F	0	FF D4 = 00, D5 =
				D_n															FF
	도																		D5 = FF, D7 = 00
Toggling	Static High	2	8–11														2 inst		
Jogo	atic	3	12–15							•							3 inst		
	₹	4	16–19														1 inst		
		5	20–23														2 inst		
		6	24–27														3 inst		
		7	28–31														0 inst		
		8	32–35) inst		
		9	36–39														linst		
		10	40–43														2 inst		
		11	44–47														3 inst		
		12	48–51														linst		
		13	52–55														2 inst		
		14	56–59														3 inst		
		15	60–63				кере	at sul	0-loo	p 1, ι	ise B	[1:0]د] = 3,	use I	3A[1:	υ] = () inst	ead ⁴	

- Notes: 1. DQS_t, DQS_c are V_{DDQ} when not toggling.
 - 2. BG1 is a "Don't Care" for x16 devices.
 - 3. Burst sequence driven on each DQ signal by a READ command. Outside burst operation, DQ signals are V_{DDQ}.
 - 4. For x4 and x8 only.

Table 141: I_{DD4W} Measurement – Loop Pattern¹

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Com- mand	CS_n	ACT_n	RAS_n/A1 6	CAS_n/A1 5	WE_n/A14	ОБТ	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,1 1]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³
		0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF,
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	D2 = FF, D3 = 00, D4 = FF, D5 = 00,
			2, 3	D_n, D_n	1	1	1	1	0	1	3	3	0	0	0	7	F	0	D5 = 00, D7 = FF
		1	4	WR	0	1	1	0	0	1	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	D2 = 00, D3 = FF
			6, 7	D_n, D_n	1	1	1	1	0	1	3	3	0	0	0	7	F	0	D4 = 00, D5 = FF D5 = FF, D7 = 00
		2	8–11				Rep	eat s	ub-lo	op 0,	use E	G[1:0	0] = 0), use	BA[1	:0] =	2 inst	ead	
	ے	3	12–15				Rep	eat s	ub-lo	op 1,	use E	3G[1:0	0] = 1	l, use	BA[1	:0] =	3 inst	ead	
Toggling	Static High	4	16–19				Rep	eat s	ub-lo	op 0,	use E	3G[1:0) = C), use	BA[1	:0] =	1 inst	ead	
ogg	atic	5	20–23				Rep	eat s	ub-lo	op 1,	use E	3G[1:0	0] = 1	l, use	BA[1	:0] = 2	2 inst	ead	
ĭ	Ste	6	24–27				Rep	eat s	ub-lo	op 0,	use E	3G[1:0	0] = 0), use	BA[1	:0] = [3 inst	ead	
		7	28–31				Rep	eat s	ub-lo	op 1,	use E	3G[1:0	0] = 1	l, use	BA[1	:0] =	0 inst	ead	
		8	32–35				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 2	, use E	BA[1:	0] = 0) inste	ead ⁴	
		9	36–39				Rep	eat su	ıb-lo	op 1,	use B	G[1:0)] = 3	, use E	3A[1:	0] = 1	linste	ead ⁴	
		10	40–43				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 2	, use E	3A[1:	0] = 2	2 inste	ead ⁴	
		11	44–47				Rep	eat su	ıb-lo	op 1,	use B	G[1:0)] = 3	, use E	3A[1:	0] = 3	3 inste	ead ⁴	
		12	48–51				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 2	, use E	BA[1:	0] = 1	l inste	ead ⁴	
		13	52–55				Rep	eat su	ıb-lo	op 1,	use B	G[1:0)] = 3	, use E	3A[1:	0] = 2	2 inste	ead ⁴	
		14	56–59				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 2	, use E	3A[1:	0] = 3	3 inste	ead ⁴	
		15	60–63				Rep	eat su	ıb-lo	op 1,	use B	G[1:0] = 3	, use I	BA[1:	0] = 0) inste	ead ⁴	

Notes: 1. DQS_t, DQS_c are V_{DDQ} when not toggling.

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- 2. BG1 is a "Don't Care" for x16 devices.
- 3. Burst sequence driven on each DQ signal by WRITE command. Outside burst operation, DQ signals are V_{DDQ}.
- 4. For x4 and x8 only.

Table 142: I_{DD4Wc} Measurement - Loop Pattern¹

CK_c, CK_t,	CKE	Sub-Loop	Cycle	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ООТ	BG[1:0] ³	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴
		0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF,
			1, 2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	D2 = FF, D3 = 00, D4 = FF, D5 = 00,
			3, 4	D_n, D_n	1	1	1	1	0	1	3	3	0	0	0	7	F	0	D8 = CRC
		1	5	WR	0	1	1	0	0	1	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00,
			6, 7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	D2 = 00, D3 = FF, D4 = 00, D5 = FF,
			8, 9	D_n, D_n	1	1	1	1	0	1	3	3	0	0	0	7	F	0	D5 = FF, D7 = 00 D8 = CRC
		2	10–14				Rep	eat s	ub-lo	op 0,	use E	G[1:0	0] = 0	, use	BA[1	:0] =	2 inst	ead	
	4	3	15–19				Rep	eat s	ub-lo	op 1,	use E	3G[1:0	0] = 1	, use	BA[1	:0] = [3 inst	ead	
Toggling	Static High	4	20–24				Rep	eat s	ub-lo	op 0,	use E	3G[1:0	0] = 0	, use	BA[1	:0] =	1 inst	ead	
ogg	atic	5	25–29				Rep	eat s	ub-lo	op 1,	use E	3G[1:0	0] = 1	, use	BA[1	:0] = [2 inst	ead	
-	St	6	30–34				Rep	eat s	ub-lo	op 0,	use E	3G[1:0	0] = 0	, use	BA[1	:0] = [3 inst	ead	
		7	35–39				Rep	eat s	ub-lo	op 1,	use E	3G[1:0	0] = 1	, use	BA[1	:0] =	0 inst	ead	
		8	40–44				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 2	, use	BA[1:	0] = 0) inst	ead ⁴	
		9	45–49				Rep	eat su	ıb-lo	op 1,	use B	G[1:0)] = 3	, use	BA[1:	0] = 1	linst	ead ⁴	
		10	50–54				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 2	, use	BA[1:	0] = 2	2 inste	ead ⁴	
		11	55–59				Rep	eat su	ıb-lo	р 1,	use B	G[1:0)] = 3	, use	BA[1:	0] = 3	3 inste	ead ⁴	
		12	60–64				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 2	, use	BA[1:	0] = 1	l inste	ead ⁴	
		13	65–69				Rep	eat su	ıb-lo	op 1,	use B	G[1:0)] = 3	, use	BA[1:	0] = 2	2 inste	ead ⁴	
		14	70–74				Rep	eat su	ıb-lo	op 0,	use B	G[1:0)] = 2	, use	BA[1:	0] = 3	3 inste	ead ⁴	
		15	75–79				Rep	eat su	ıb-lo	op 1,	use B	G[1:0)] = 3	, use	BA[1:	0] = 0) inst	ead ⁴	

- Notes: 1. Pattern provided for reference only.
 - 2. DQS_t, DQS_c are V_{DDO} when not toggling.
 - 3. BG1 is a "Don't Care" for x16 devices.
 - 4. Burst sequence driven on each DQ signal by WRITE command. Outside burst operation, DQ signals are V_{DDQ} .
 - 5. For x4 and x8 only.

Table 143: I_{DD5R} Measurement – Loop Pattern¹

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³
		0	0	REF	0	1	0	0	1	0	0	0	0	0	0	0	0	0	_
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	_
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	_
			3	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	_
			4	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	_
			5–8				Repe	at pa	ttern	14	, use	BG[1	:0] =	1, use	BA[1:0] =	: 1 ins	stead	
			9–12			Repeat pattern 14, use BG[1:0] = 1, use BA[1:0] = 1 instead Repeat pattern 14, use BG[1:0] = 0, use BA[1:0] = 2 instead Repeat pattern 14, use BG[1:0] = 1, use BA[1:0] = 3 instead													
			13–16			· ·													
			17–20			Repeat pattern 14, use BG[1:0] = 1, use BA[1:0] = 3 instead Repeat pattern 14, use BG[1:0] = 0, use BA[1:0] = 1 instead													
0	l de		21–24				Repe	at pa	ttern	14	, use	BG[1	:0] =	1, use	BA[1:0] =	2 in	stead	
Toggling	Static High		25–28				Repe	at pa	ttern	14	, use	BG[1	:0] =	0, use	BA[1:0] =	3 ins	stead	
log	tatic		29–32				Repe	at pa	ttern	14	, use	BG[1	:0] =	1, use	BA[1:0] =	0 ins	stead	
'	Ş		33–36				Repe	at pa	ttern	14,	use	BG[1:	0] = 2	2, use	BA[l:0] =	0 ins	tead ⁴	l .
			37–40				Repe	at pa	ttern	14,	use	BG[1:	0] = 3	3, use	BA[l:0] =	1 ins	tead ⁴	l .
			41–44				Repe	at pa	ttern	14,	use	BG[1:	0] = 2	2, use	BA[l:0] =	2 ins	tead ⁴	Į.
			45–48				Repe	at pa	ttern	14,	use	BG[1:	0] = 3	3, use	BA[l:0] =	3 ins	tead ⁴	l .
			49–52				Repe	at pa	ttern	14,	use	BG[1:	0] = 2	2, use	BA[l:0] =	1 ins	tead ⁴	Į.
			53–56				Repe	at pa	ttern	14,	use	BG[1:	0] = 3	3, use	BA[l:0] =	2 ins	tead ⁴	Į.
			57–60				Repe	at pa	ttern	14,	use	BG[1:	0] = 2	2, use	BA[l:0] =	3 ins	tead ⁴	1
			61–64				Repe	at pa	ttern	14,	use	BG[1:	0] = 3	3, use	BA[l:0] =	0 ins	tead ⁴	
		2	65 <i>n</i> REFI -						Repe	at su	b-loo	p 1; t	runc	ate if	nece	ssary			

- Notes: 1. DQS_t, DQS_c are V_{DDQ}.
 - 2. BG1 is a "Don't Care" for x16 devices.
 - 3. DQ signals are V_{DDQ} .
 - 4. For x4 and x8 only.



Table 144: I_{DD7} Measurement – Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Cycle	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	DDT	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ³
		0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	_
			1	RDA	0	1	1	0	1	0	0	0	0	0	1	0	0	0	
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	_
			3	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	_
					Rep	oeat _l	oatte	rn 2	.3 un	til <i>n</i> R	RD -	1, if <i>i</i>	nRRD	> 4.	Trund	ate i	f nec	essary	/
		1	<i>n</i> RRD	ACT	0	0	0	0	0	0	1	1	0	0	0	0	0	0	_
			nRRD+1	RDA	0	1	1	0	1	0	1	1	0	0	1	0	0	0	
					Repe	at pa	ttern	23	unti	2 × 1	าRRD	- 1, i	f <i>n</i> RR	D > 4	1. Tru	ncate	if ne	ecessa	ary
		2	2 × nRRD			Re	peat	sub-l	oop 0	, use	BG[1	:0] =	0, us	e BA[1:0] =	= 2 in	steac	l	
		3	3 × nRRD			Re	peat	sub-l	oop 1	, use	BG[1	:0] =	1, us	e BA[1:0] =	= 3 in	steac	1	
		4	4 × nRRD	Re	peat	patte	ern 2.	3 ur	ntil <i>n</i> l	AW ·	- 1, if	nFA\	N > 4	× <i>n</i> F	RRD.	Trunc	ate if	nece	ssary
		5	<i>n</i> FAW			Re	peat	sub-l	oop 0	, use	BG[1	:0] =	0, us	e BA[1:0] =	= 1 in	steac	l	
		6	<i>n</i> FAW + <i>n</i> RRD			Re	peat	sub-l	oop 1	, use	BG[1	:0] =	1, us	e BA[1:0] =	= 2 in	steac	l	
		7	$nFAW + 2 \times nRRD$			Re	peat	sub-l	oop 0	, use	BG[1	:0] =	0, us	e BA[[1:0] =	= 3 in	steac	l	
0	д	8	$nFAW + 3 \times nRRD$			Re	peat	sub-l	oop 1	, use	BG[1	:0] =	1, us	e BA[[1:0] =	= 0 in	steac	l	
gli	ij	9	$nFAW + 4 \times nRRD$							Re	peat	sub-l	oop 4						
Toggling	Static High	10	2 × nFAW			Re	peat	sub-l	oop 0	, use	BG[1	:0] =	2, us	e BA[[1:0] =	= 0 in	steac	l	
'	ν	11	$2 \times nFAW + nRRD$			Re	peat	sub-l	oop 1	, use	BG[1	:0] =	3, us	e BA[1:0] =	= 1 in	steac	l	
		12	2 × <i>n</i> FAW + 2 × <i>n</i> RRD			Re	peat	sub-le	oop 0	, use	BG[1	:0] =	2, us	e BA[[1:0] =	= 2 in	steac	l	
		13	2 × <i>n</i> FAW + 3 × <i>n</i> RRD			Re	peat	sub-l	oop 1	, use	BG[1	:0] =	3, us	e BA[[1:0] =	= 3 in	steac	I	
		14	2 × nFAW + 4 × nRRD							Re	peat	sub-l	oop 4	ļ					
		15	3 × nFAW			Re	peat	sub-l	oop 0	, use	BG[1	:0] =	2, us	e BA[1:0] =	= 1 in	steac	l	
		16	3 × nFAW + nRRD			Re	peat	sub-l	oop 1	, use	BG[1	:0] =	3, us	e BA[1:0] =	= 2 in	steac	l	
		17	3 × <i>n</i> FAW + 2 × <i>n</i> RRD			Re	peat	sub-l	oop 0	, use	BG[1	:0] =	2, us	e BA[[1:0] =	= 3 in	steac	I	
		18	3 × <i>n</i> FAW + 3 × <i>n</i> RRD			Re	peat	sub-l	oop 1	, use	BG[1	:0] =	3, us	e BA[[1:0] =	= 0 in	steac	I	
		19	3 × nFAW + 4 × nRRD							Re	peat	sub-l	oop 4	ļ					
		20	4 × <i>n</i> FAW	F	Repea	at pat	tern	23	until	nRC -	- 1, if	nRC	> 4 ×	nFA\	N. Tru	uncat	e if n	ecess	ary

- Notes: 1. DQS_t, DQS_c are V_{DDQ}.
 - 2. BG1 is a "Don't Care" for x16 devices.
 - 3. DQ signals are V_{DDQ} except when burst sequence drives each DQ signal by a READ command.



4. For x4 and x8 only.

IDD Specifications

Table 145: Timings used for I_{DD} , I_{PP} , and I_{DDQ} Measurement – Loop Patterns

		DD	R4-1	600	DD	R4-1	866	DD	R4-2	133	DD	R4-24	400	DD	R4-2	666	DD	R4-29	933	DD	R4-32	200	
Syml	bol	10-10-10	11-11-11	12-12-12	12-12-12	13-13-13	14-14-14	14-14-14	15-15-15	16-16-16	16-16-16	17-17-17	18-18-18	18-18-18	19-19-19	20-20-20	20-20-20	21-21-21	22-22-22	20-20-20	22-22-22	24-24-24	Uni t
^t Ck	(1.25			1.071			0.937			0.833			0.75			0.682			0.625		ns
CL		10	11	12	12	13	14	14	15	16	16	17	18	18	19	20	20	21	22	20	22	24	CK
CW	'L	9	11	11	10	12	12	11	14	14	16	16	16	18	18	18	14	18	18	16	20	20	СК
nRC	.D	10	11	12	12	13	14	14	15	16	16	17	18	18	19	20	19	20	21	20	22	24	СК
nRo	С	38	39	40	44	45	46	50	51	52	55	56	57	61	62	63	66	67	68	72	74	76	CK
nRI	Р	10	11	12	12	13	14	14	15	16	16	17	18	18	19	20	19	20	21	20	22	24	CK
nRA	۱S		28			32			36			39			43			47			52		CK
<i>n</i> FA	x4 ¹		16			16			16			16			16			16			16		CK
W	х8		20			22			23			26			28			31			34		CK
	x1 6		28			28			32			36			40			44			48		CK
nRRD	х4		4			4			4			4			4			4			4		CK
_S	х8		4			4			4			4			4			4			4		CK
	x1 6		5			6			6			7			8			8			9		CK
nRRD	х4		5			5			6			6			7			8			8		CK
_L	х8		5			5			6			6			7			8			8		CK
	x1 6		6			6			7			8			9			10			11		CK
nCCD)_S		4			4			4			4			4			4			4		CK
nCCD)_L		5			5			6			6			7			8			8		CK
nWTF	R_S		2			3			3			3			4			4			4		CK
nWTF	R_L		6			7			8			9			10			11			12		CK
nRE	FI		6,240)	,	7,283	3	1	8,325			9,364		1	10,400)	•	11,43	7	1	12,480)	CK
nRFC 2	2Gb		128			150			171			193			214			235			256		CK
nRFC 4			208			243			278			313			347			382			416		CK
nRFC 8	8Gb		280			327			374			421			467			514			560		CK
<i>n</i> RF 16G			280			327			374			421			467			514			560		CK

Note: 1. 1KB based x4 use same numbers of clocks for *n*FAW as the x8.



Current Specifications – Limits

Table 146: I_{DD} , I_{PP} , and I_{DDQ} Current Limits; Die Rev. A (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	Unit
I _{DD0} : One bank ACTIVATE-to-PRE-	x4, x8	55	60	65	TBD	mA
CHARGE current	x16	85	90	95	TBD	mA
IPPO: One bank ACTIVATE-to-PRECHARGE	x4, x8	3	3	3	TBD	mA
I _{PP} current	x16	4	4	4	TBD	mA
I _{DD1} : One bank ACTIVATE-to-READ-to-	x4, x8	70	75	80	TBD	mA
PRECHARGE current	x16	105	110	115	TBD	mA
I _{DD2N} : Precharge standby current	x4, x8	45	50	55	TBD	mA
	x16	65	70	75	TBD	mA
I _{DD2NT} : Precharge standby ODT current	x4, x8	55	60	65	TBD	mA
	x16	75	80	90	TBD	mA
I _{DD2P} : Precharge power-down current	x4, x8	25	30	35	TBD	mA
	x16	45	50	55	TBD	mA
I _{DD2Q} : Precharge quiet standby current	x4, x8	45	45	50	TBD	mA
	x16	65	65	70	TBD	mA
I _{DD3N} : Active standby current	x4, x8	55	55	60	TBD	mA
	x16	75	75	85	TBD	mA
I _{PP3N} : Active standby I _{PP} current	ALL	3	3	3	TBD	mA
I _{DD3P} : Active power-down current	x4, x8	35	40	40	TBD	mA
	x16	55	60	65	TBD	mA
I _{DD4R} : Burst read current	x4	135	145	160	TBD	mA
	x8	150	150	175	TBD	mA
	x16	210	230	250	TBD	mA
I _{DD4W} : Burst write current	x4	135	145	160	TBD	mA
	x8	150	160	175	TBD	mA
	x16	210	230	250	TBD	mA
I _{DD5R} : Distributed refresh current (1X	x4, x8	64	64	68	TBD	mA
REF)	x16	84	84	94	TBD	mA
I_{PPSR} : Distributed refresh I _{PP} current (1X REF)	ALL	5	5	5	TBD	mA
I _{DD6N} : Self refresh current; 0–85°C ¹	ALL	30	30	30	TBD	mA
I _{DD6E} : Self refresh current; 0–95°C ^{2,4}	x4, x8	35	35	35	TBD	mA
	x16	50	50	50		mA
I _{DD6R} : Self refresh current; 0–45C ^{3,4}	ALL	25	25	25	TBD	mA
I _{DD6A} : Auto self refresh current (25°C) ⁴	ALL	20	20	20	TBD	mA
I _{DD6A} : Auto self refresh current (45°C) ⁴	ALL	25	25	25	TBD	mA
I _{DD6A} : Auto self refresh current (75°C) ⁴	x4, x8	35	35	35	TBD	mA
	x16	50	50	50	TBD	mA



Table 146: I_{DD} , I_{PP} , and I_{DDO} Current Limits; Die Rev. A (0° \leq T_C \leq 85°C) (Continued)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	Unit
I _{PP6x} : Auto self refresh I _{PP} current; 0– 95°C ²⁵	ALL	5	5	5		mA
I _{DD7} : Bank interleave read current	x4	250	255	265	TBD	mA
	x8	200	205	215	TBD	mA
	x16	265	270	280	TBD	mA
I _{PP7} : Bank interleave read I _{PP} current	x4	25	25	25	TBD	mA
	x8	15	15	15	TBD	
	x16	20	20	20	TBD	mA
I _{DD8} : Maximum power-down current	ALL	20	20	20	TBD	mA

- Notes: 1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0-85°C).
 - 2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
 - 3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0-45°C).
 - 4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
 - 5. When additive latency is enabled for I_{DD0}, current changes by approximately 0%.
 - 6. When additive latency is enabled for I_{DD1}, current changes by approximately +5%(x4/x8), +4%(x16).
 - 7. When additive latency is enabled for I_{DD2N}, current changes by approximately +0%.
 - 8. When DLL is disabled for I_{DD2N}, current changes by approximately –23%.
 - 9. When CAL is enabled for I_{DD2N}, current changes by approximately –25%.
 - 10. When gear-down is enabled for I_{DD2N} , current changes by approximately 0%.
 - 11. When CA parity is enabled for I_{DD2N} , current changes by approximately +7%.
 - 12. When additive latency is enabled for IDD3N, current changes by approximately +1%.
 - 13. When additive latency is enabled for IDD4R, current changes by approximately +5%.
 - 14. When read DBI is enabled for I_{DD4R}, current changes by approximately 0%.
 - 15. When additive latency is enabled for I_{DD4W}, current changes by approximately +3%(x4/ x8), +4%(x16).
 - 16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
 - 17. When write CRC is enabled for I_{DD4W} , current changes by approximately +10%(x4/x8), +10%(x16).
 - 18. When CA parity is enabled for I_{DD4W} , current changes by approximately +12% (x8), +12% (x16).
 - 19. When 2X REF is enabled for I_{DD5R}, current changes by approximately –14%.
 - 20. When 4X REF is enabled for IDD5R, current changes by approximately –33%.
 - 21. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
 - 22. I_{PP3N} test and limit is applicable for all I_{DD2x} , I_{DD3x} , I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
 - 23. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
 - 24. The I_{DD} values must be derated (increased) when operated outside of the range $0^{\circ}C \leq T_{C}$ ≤ 85°C:

When $T_C < 0$ °C: I_{DD2P} , and I_{DD3P} must be derated by 6%; I_{DD4R} and I_{DD4W} must be derated by 4%; I_{DD6}, I_{DD6ET}, and I_{DD7} must be derated by 11%.



When $T_C > 85^{\circ}\text{C}$: I_{DD0} , I_{DD2N} , I_{DD2NT} , I_{DD2Q} , I_{DD3N} , I_{DD3P} , I_{DD4R} , I_{DD4W} , and I_{DD5R} must be derated by 3%; I_{DD2P} must be derated by 40%. These values are verified by design and characterization, and may not be subject to production test.

25. I_{PP6x} is applicable to $I_{DD6N},\,I_{DD6E},\,I_{DD6R}$ and I_{DD6A} conditions.

Table 147: I_{DD} , I_{PP} , and I_{DDQ} Current Limits; Die Rev. B (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I _{DD0} : One bank ACTIVATE-to-	x4	40	43	46	49	52	mA
PRECHARGE current	x8	45	48	51	54	57	mA
	x16	75	80	85	90	95	mA
IPPO: One bank ACTIVATE-to-	x4, x8	3	3	3	3	3	mA
PRECHARGE I _{PP} current	x16	4	4	4	4	4	mA
I _{DD1} : One bank ACTIVATE-to-	x4	52	55	58	61	64	mA
READ-to- PRECHARGE cur-	x8	57	60	63	66	69	mA
rent	x16	95	100	105	110	115	mA
I _{DD2N} : Precharge standby current	ALL	33	34	35	36	37	mA
I _{DD2NT} : Precharge standby	x4, x8	45	50	50	55	60	mA
ODT current	x16	67	75	75	78	81	mA
I _{DD2P} : Precharge power- down current	ALL	25	25	25	25	25	mA
I_{DD2Q} : Precharge quiet stand- by current	ALL	30	30	30	30	30	mA
I _{DD3N} : Active standby current	x4	35	38	41	44	47	mA
	x8	40	43	46	49	52	mA
	x16	44	47	50	53	56	mA
I_{PP3N} : Active standby I _{PP} current	ALL	3	3	3	3	3	mA
I _{DD3P} : Active power-down	x4	30	32	34	36	38	mA
current	x8	35	37	39	41	43	mA
	x16	39	41	43	45	47	mA
I _{DD4R} : Burst read current	x4	100	110	121	132	143	mA
	x8	125	135	146	157	168	mA
	x16	225	243	263	283	302	mA
I _{DD4W} : Burst write current	x4	95	103	112	121	130	mA
	x8	115	123	132	141	150	mA
	x16	213	228	244	261	278	mA
I _{DD5R} : Distributed refresh	x4, x8	50	53	56	59	62	mA
current (1X REF)	x16	56	59	61	64	67	mA
I_{PP5R} : Distributed refresh I _{PP} current (1X REF)	ALL	5	5	5	5	5	mA
I_{DD6N} : Self refresh current; 0–85°C ¹	ALL	30	30	30	30	30	mA



Table 147: I_{DD} , I_{PP} , and I_{DDO} Current Limits; Die Rev. B (0° \leq T_C \leq 85°C) (Continued)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD6E} : Self refresh current; 0–95°C ^{2,4}	ALL	35	35	35	35	35	mA
I_{DD6R} : Self refresh current; 0–45C ^{3,4}	ALL	20	20	20	20	20	mA
I _{DD6A} : Auto self refresh current (25°C) ⁴	ALL	8.6	8.6	8.6	8.6	8.6	mA
I _{DD6A} : Auto self refresh current (45°C) ⁴	ALL	20	20	20	20	20	mA
I _{DD6A} : Auto self refresh current (75°C) ⁴	ALL	30	30	30	30	30	mA
I _{PP6x} : Auto self refresh I _{PP} current; 0–95°C ²⁵	ALL	5	5	5	5	5	mA
I _{DD7} : Bank interleave read	x4	175	185	200	215	230	mA
current	x8	170	175	180	185	190	mA
	x16	239	249	259	269	279	mA
IPP7: Bank interleave read IPP	x4	16	17	18	19	20	mA
current	x8	15	15	15	15	15	mA
	x16	20	20	20	20	20	mA
I _{DD8} : Maximum power-down current	ALL	25	25	25	25	25	mA

- Notes: 1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
 - 2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0-95°C).
 - 3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0–45°C).
 - 4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
 - 5. When additive latency is enabled for I_{DD0}, current changes by approximately 0%.
 - 6. When additive latency is enabled for IDD1, current changes by approximately +5%(x4/x8), +4%(x16).
 - 7. When additive latency is enabled for I_{DD2N}, current changes by approximately 0%.
 - 8. When DLL is disabled for I_{DD2N} , current changes by approximately –23%.
 - 9. When CAL is enabled for I_{DD2N}, current changes by approximately –25%.
 - 10. When gear-down is enabled for I_{DD2N} , current changes by approximately 0%.
 - 11. When CA parity is enabled for I_{DD2N} , current changes by approximately +7%.
 - 12. When additive latency is enabled for I_{DD3N}, current changes by approximately +1%.
 - 13. When additive latency is enabled for I_{DD4R}, current changes by approximately +5%.
 - 14. When read DBI is enabled for I_{DD4R}, current changes by approximately 0%.
 - 15. When additive latency is enabled for I_{DD4W}, current changes by approximately +3%(x4/ x8), +4%(x16).
 - 16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
 - 17. When write CRC is enabled for I_{DD4W}, current changes by approximately +10%(x4/x8), +10%(x16).



- When CA parity is enabled for I_{DD4W}, current changes by approximately +12% (x8), +12% (x16).
- 19. When 2X REF is enabled for I_{DD5R}, current changes by approximately –14%.
- 20. When 4X REF is enabled for I_{DD5R}, current changes by approximately –33%.
- 21. I_{PPO} test and limit is applicable for I_{DDO} and I_{DD1} conditions.
- 22. I_{PP3N} test and limit is applicable for all I_{DD2x} , I_{DD3x} , I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PPS} for the noted I_{DD} tests.
- 23. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
- 24. The I_{DD} values must be derated (increased) when operated outside of the range $0^{\circ}C \le T_{C} \le 85^{\circ}C$:

When $T_C < 0$ °C: I_{DD2P} , and I_{DD3P} must be derated by 6%; I_{DD4R} and I_{DD4W} must be derated by 4%; I_{DD6} , I_{DD6ET} , and I_{DD7} must be derated by 11%.

When $T_C > 85^{\circ}\text{C}$: I_{DD0} , I_{DD1} , I_{DD2N} , I_{DD2NT} , I_{DD2Q} , I_{DD3N} , I_{DD3P} , I_{DD4R} , I_{DD4W} , and I_{DD5R} must be derated by 3%; I_{DD2P} must be derated by 40%. These values are verified by design and characterization, and may not be subject to production test.

25. I_{PP6x} is applicable to I_{DD6N} , I_{DD6E} , I_{DD6R} and I_{DD6A} conditions.

Table 148: I_{DD} , I_{PP} , and I_{DDQ} Current Limits; Die Rev. D (0° \leq T_C \leq 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
IDDO: One bank ACTIVATE-to-	x4	40	43	46	49	52	mA
PRECHARGE current	x8	45	48	51	54	57	mA
	x16	75	80	85	90	95	mA
IPPO: One bank ACTIVATE-to-	x4, x8	3	3	3	3	3	mA
PRECHARGE I _{PP} current	x16	4	4	4	4	4	mA
IDD1: One bank ACTIVATE-to-	x4	52	55	58	61	64	mA
READ-to- PRECHARGE cur-	x8	57	60	63	66	69	mA
rent	x16	95	100	105	110	115	mA
I _{DD2N} : Precharge standby current	ALL	33	34	35	36	37	mA
I _{DD2NT} : Precharge standby	x4, x8	45	50	50	55	60	mA
ODT current	x16	67	75	75	78	81	mA
I _{DD2P} : Precharge power- down current	ALL	25	25	25	25	25	mA
I_{DD2Q}: Precharge quiet stand- by current	ALL	30	30	30	30	30	mA
I _{DD3N} : Active standby current	x4	40	43	46	49	52	mA
	x8	45	48	51	54	56	mA
	x16	49	52	55	58	61	mA
I_{PP3N} : Active standby I_{PP} current	ALL	3	3	3	3	3	mA
I _{DD3P} : Active power-down	x4	30	32	34	36	38	mA
current	x8	35	37	39	41	43	mA
	x16	39	41	43	45	47	mA



Table 148: I_{DD} , I_{PP} , and I_{DDQ} Current Limits; Die Rev. D (0° \leq T_C \leq 85°C) (Continued)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I _{DD4R} : Burst read current	x4	100	110	121	132	143	mA
	x8	125	135	146	157	168	mA
	x16	225	243	263	283	302	mA
I _{DD4W} : Burst write current	x4	105	113	122	130	140	mA
	x8	125	132	142	150	160	mA
	x16	225	240	255	270	290	mA
I _{DD5R} : Distributed refresh	x4, x8	56	58	61	64	66	mA
current (1X REF)	x16	61	64	67	69	72	mA
I_{PP5R} : Distributed refresh I _{PP} current (1X REF)	ALL	5	5	5	5	5	mA
I_{DD6N} : Self refresh current; 0–85°C ¹	ALL	31	31	31	31	31	mA
I_{DD6E} : Self refresh current; 0–95°C ^{2,4}	ALL	36	36	36	36	36	mA
I_{DD6R}: Self refresh current; 0–45C ^{3,4}	ALL	21	21	21	21	21	mA
I _{DD6A} : Auto self refresh current (25°C) ⁴	ALL	8.6	8.6	8.6	8.6	8.6	mA
I _{DD6A} : Auto self refresh current (45°C) ⁴	ALL	21	21	21	21	21	mA
I_{DD6A} : Auto self refresh current (75°C) ⁴	ALL	31	31	31	31	31	mA
I _{PP6x} : Auto self refresh I _{PP} current; 0–95°C ²⁵	ALL	5	5	5	5	5	mA
I _{DD7} : Bank interleave read	x4	175	185	200	215	230	mA
current	x8	170	175	180	185	190	mA
	x16	239	249	259	269	279	mA
I _{PP7} : Bank interleave read I _{PP}	x4	16	17	18	19	20	mA
current	x8	15	15	15	15	15	mA
	x16	20	20	20	20	20	mA
I _{DD8} : Maximum power-down current	ALL	25	25	25	25	25	mA

- Notes: 1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0-85°C).
 - 2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0-95°C).
 - 3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0-45°C).
 - 4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
 - 5. When additive latency is enabled for I_{DD0}, current changes by approximately 0%.



- 6. When additive latency is enabled for I_{DD1} , current changes by approximately +5%(x4/x8), +4%(x16).
- 7. When additive latency is enabled for I_{DD2N}, current changes by approximately 0%.
- 8. When DLL is disabled for I_{DD2N} , current changes by approximately -23%.
- 9. When CAL is enabled for I_{DD2N} , current changes by approximately -25%.
- 10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
- 11. When CA parity is enabled for I_{DD2N}, current changes by approximately +7%.
- 12. When additive latency is enabled for IDD3N, current changes by approximately +1%.
- 13. When additive latency is enabled for I_{DD4R} , current changes by approximately +5%.
- 14. When read DBI is enabled for I_{DD4R}, current changes by approximately 0%.
- 15. When additive latency is enabled for I_{DD4W} , current changes by approximately +3%(x4/x8), +4%(x16).
- 16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
- 17. When write CRC is enabled for I_{DD4W}, current changes by approximately +10%(x4/x8), +10%(x16).
- When CA parity is enabled for I_{DD4W}, current changes by approximately +12% (x8), +12% (x16).
- 19. When 2X REF is enabled for I_{DD5R}, current changes by approximately –14%.
- 20. When 4X REF is enabled for IDD5R, current changes by approximately -33%.
- 21. IPPO test and limit is applicable for IDDO and IDD1 conditions.
- 22. I_{PP3N} test and limit is applicable for all I_{DD2x} , I_{DD3x} , I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PPS} for the noted I_{DD} tests.
- 23. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
- 24. The I_{DD} values must be derated (increased) when operated outside of the range $0^{\circ}C \le T_C \le 85^{\circ}C$:

When $T_C < 0^{\circ}C$: I_{DD2P} , and I_{DD3P} must be derated by +6%; I_{DD4R} and I_{DD4W} must be derated by +4%; I_{DD6} , I_{DD6ET} , and I_{DD7} must be derated by +11%.

When $T_C > 85^{\circ}C$: I_{DD0} , I_{DD1} , I_{DD2N} , I_{DD2NT} , I_{DD2Q} , I_{DD3N} , I_{DD3P} , I_{DD4R} , and I_{DD4W} must be derated by +3%; I_{DD2P} must be derated by +40%; and I_{DD5R} and I_{PP5R} must be derated by +40%. These values are verified by design and characterization, and may not be subject to production test.

25. I_{PP6x} is applicable to I_{DD6N} , I_{DD6E} , I_{DD6R} and I_{DD6A} conditions.

Table 149: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. E (-40° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I _{DD0} : One bank ACTIVATE-to-	x4	37	39	41	43	45	mA
PRECHARGE current	x8	39	41	43	45	47	mA
	x16	46	48	50	52	54	mA
IPPO: One bank ACTIVATE-to-	x4, x8	3	3	3	3	3	mA
PRECHARGE I _{PP} current	x16	4	4	4	4	4	mA
I _{DD1} : One bank ACTIVATE-to-	x4	50	52	54	56	58	mA
READ-to- PRECHARGE cur-	x8	55	57	59	61	63	mA
rent	x16	72	74	76	78	80	mA
I _{DD2N} : Precharge standby current	ALL	29	30	31	32	33	mA
I _{DD2NT} : Precharge standby	x4, x8	36	38	40	42	44	mA
ODT current	x16	43	46	49	52	55	mA



Table 149: I_{DD} , I_{PP} , and I_{DDQ} Current Limits; Die Rev. E (-40° \leq T_C \leq 85°C) (Continued)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I _{DD2P} : Precharge power- down current	ALL	22	22	22	22	22	mA
I _{DD2Q} : Precharge quiet stand- by current	ALL	26	26	26	26	26	mA
I _{DD3N} : Active standby current	x4	34	36	38	40	42	mA
	x8	35	37	39	41	43	mA
	x16	36	38	40	42	44	mA
I_{PP3N} : Active standby I _{PP} current	ALL	3	3	3	3	3	mA
I _{DD3P} : Active power-down	x4	28	29	30	31	32	mA
current	x8	29	30	31	32	33	mA
	x16	30	31	32	33	34	mA
I _{DD4R} : Burst read current	x4	110	120	131	142	153	mA
	x8	135	145	156	167	178	mA
	x16	235	253	273	293	312	mA
I _{DD4W} : Burst write current	x4	96	105	114	123	132	mA
	x8	114	123	132	141	150	mA
	x16	182	199	216	233	250	mA
I _{DD5R} : Distributed refresh current (1X REF)	ALL	46	47	48	49	50	mA
I_{PP5R} : Distributed refresh I _{PP} current (1X REF)	ALL	5	5	5	5	5	mA
I_{DD6N} : Self refresh current; -40–85°C ¹	ALL	34	34	34	34	34	mA
I_{DD6E} : Self refresh current; -40–95°C ^{2,4}	ALL	58	58	58	58	58	mA
I_{DD6R} : Self refresh current; -40–45°C ^{3,4}	ALL	21	21	21	21	21	mA
I _{DD6A} : Auto self refresh current (25°C) ⁴	ALL	8.6	8.6	8.6	8.6	8.6	mA
I _{DD6A} : Auto self refresh current (45°C) ⁴	ALL	21	21	21	21	21	mA
I_{DD6A} : Auto self refresh current (75°C) ⁴	ALL	31	31	31	31	31	mA
I _{DD6A} : Auto self refresh current (95°C) ⁴	ALL	58	58	58	58	58	mA
I _{PP6x} : Auto self refresh I _{PP} current; -40–95°C ²⁶	ALL	5	5	5	5	5	mA
I _{DD7} : Bank interleave read	x4	175	185	200	215	230	mA
current	х8	170	175	180	185	190	mA
	x16	234	243	252	261	270	mA



Table 149: I_{DD}, I_{PP}, and I_{DDO} Current Limits; Die Rev. E (-40° ≤ T_C ≤ 85°C) (Continued)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
IPP7: Bank interleave read IPP	x4	14	14	14	14	14	mA
current	x8	13	13	13	13	13	mA
	x16	18	18	18	18	18	mA
I _{DD8} : Maximum power-down current	ALL	18	18	18	18	18	mA

- 1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (-40–85°C).
- 2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (-40–95°C).
- 3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation ($-40-45^{\circ}$ C).
- 4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
- 5. When additive latency is enabled for IDDO, current changes by approximately +1%.
- When additive latency is enabled for I_{DD1}, current changes by approximately +8%(x4/x8), +7%(x16).
- 7. When additive latency is enabled for I_{DD2N}, current changes by approximately +1%.
- 8. When DLL is disabled for I_{DD2N}, current changes by approximately –6%.
- 9. When CAL is enabled for I_{DD2N}, current changes by approximately –30%.
- 10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
- 11. When CA parity is enabled for IDD2N, current changes by approximately +10%.
- 12. When additive latency is enabled for I_{DD3N} , current changes by approximately +1%.
- 13. When additive latency is enabled for IDD4R, current changes by approximately +4%.
- 14. When read DBI is enabled for IDD4R, current changes by approximately -14%.
- 15. When additive latency is enabled for I_{DD4W} , current changes by approximately +3%(x4/x8), +4%(x16).
- 16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
- 17. When write CRC is enabled for I_{DD4W}, current changes by approximately -5%.
- 18. When CA parity is enabled for I_{DD4W} , current changes by approximately +12%.
- 19. When 2X REF is enabled for I_{DD5R}, current changes by approximately +0%.
- 20. When 4X REF is enabled for I_{DD5R}, current changes by approximately +0%.
- 21. When 2X REF is enabled for IPPSR, current changes by approximately +0%.
- 22. When 4X REF is enabled for IPPSR, current changes by approximately +0%.
- 23. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
- 24. I_{PP3N} test and limit is applicable for all I_{DD2x} , I_{DD3x} , I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PPS} for the noted I_{DD} tests.
- 25. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
- 26. The I_{DD} values must be derated (increased) when operating between 85°C < $T_C \le 95$ °C: I_{DD0} , I_{DD1} , I_{DD2NT} , I_{DD2Q} , I_{DD3N} , I_{DD3P} , I_{DD4R} , and I_{DD4W} must be derated by +3%; I_{DD2P} must be derated by +10%; and I_{DD5R} and I_{PP5R} must be derated by +43%; All I_{PP} currents except I_{PP6x} and I_{PP5R} must be derated by +0%. These values are verified by design and characterization, and may not be subject to production test.
- 27. I_{PP6x} is applicable to I_{DD6N} , I_{DD6E} , I_{DD6R} and I_{DD6A} conditions.



Table 150: I_{DD} , I_{PP} , and I_{DDQ} Current Limits; Die Rev. E (-40° \leq T_C \leq 105°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I _{DD0} : One bank ACTIVATE-to-	x8	43	45	47	49	51	mA
PRECHARGE current	x16	50	52	54	56	58	mA
IPPO: One bank ACTIVATE-to-	x8	3	3	3	3	3	mA
PRECHARGE I _{PP} current	x16	4	4	4	4	4	mA
I _{DD1} : One bank ACTIVATE-to-	x8	59	61	63	65	67	mA
READ-to- PRECHARGE cur- rent	x16	77	79	81	83	85	mA
I _{DD2N} : Precharge standby current	ALL	32	33	34	35	36	mA
I _{DD2NT} : Precharge standby	x8	40	42	44	46	48	mA
ODT current	x16	47	49	53	56	59	mA
I _{DD2P} : Precharge power- down current	ALL	26	26	26	26	26	mA
I_{DD2Q} : Precharge quiet stand- by current	ALL	29	29	29	29	29	mA
I _{DD3N} : Active standby current	x8	39	41	43	45	47	mA
	x16	40	42	44	46	48	mA
I _{PP3N} : Active standby I _{PP} current	ALL	3	3	3	3	3	mA
I _{DD3P} : Active power-down	x8	33	34	35	36	37	mA
current	x16	34	35	36	37	38	mA
I _{DD4R} : Burst read current	x8	145	155	166	178	189	mA
	x16	247	265	292	306	326	mA
I _{DD4W} : Burst write current	x8	123	132	141	151	160	mA
	x16	193	210	228	245	263	mA
I _{DD5R} : Distributed refresh current (1X REF)	ALL	96	97	98	99	100	mA
I_{PP5R} : Distributed refresh I _{PP} current (1X REF)	ALL	5	5	5	5	5	mA
I_{DD6N} : Self refresh current; -40–85°C ¹	ALL	34	34	34	34	34	mA
I_{DD6E} : Self refresh current; -40–105°C ^{2,4}	ALL	95	95	95	95	95	mA
I_{DD6R} : Self refresh current; -40–45°C ^{3,4}	ALL	21	21	21	21	21	mA
I _{DD6A} : Auto self refresh current (25°C) ⁴	ALL	8.6	8.6	8.6	8.6	8.6	mA
I_{DD6A} : Auto self refresh current (45°C) ⁴	ALL	21	21	21	21	21	mA
I_{DD6A} : Auto self refresh current (75°C) ⁴	ALL	31	31	31	31	31	mA



Table 150: I_{DD}, I_{PP}, and I_{DDO} Current Limits; Die Rev. E (-40° ≤ T_C ≤ 105°C) (Continued)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I _{DD6A} : Auto self refresh current (105°C) ⁴	ALL	95	95	95	95	95	mA
I_{PP6x} : Auto self refresh I _{PP} current; -40–105°C ²⁶	ALL	6	6	6	6	6	mA
I _{DD7} : Bank interleave read	x8	175	180	185	190	195	mA
current	x16	239	248	257	266	275	mA
IPP7: Bank interleave read IPP	x8	13	13	13	13	13	mA
current	x16	18	18	18	18	18	mA
I _{DD8} : Maximum power-down current	ALL	20	20	20	20	20	mA

- 1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (-40–85°C).
- 2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation $(-40-105^{\circ}\text{C})$.
- 3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (-40–45°C).
- 4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
- 5. When additive latency is enabled for I_{DD0} , current changes by approximately +1%.
- 6. When additive latency is enabled for I_{DD1}, current changes by approximately +8%(x4/x8), +7%(x16).
- 7. When additive latency is enabled for I_{DD2N}, current changes by approximately +1%.
- 8. When DLL is disabled for I_{DD2N} , current changes by approximately -6%.
- 9. When CAL is enabled for I_{DD2N}, current changes by approximately –30%.
- 10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
- 11. When CA parity is enabled for IDD2N, current changes by approximately +10%.
- 12. When additive latency is enabled for I_{DD3N}, current changes by approximately +1%.
- 13. When additive latency is enabled for I_{DD4R}, current changes by approximately +4%.
- 14. When read DBI is enabled for I_{DD4R}, current changes by approximately -14%.
- 15. When additive latency is enabled for I_{DD4W} , current changes by approximately +3%(x4/x8), +4%(x16).
- 16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
- 17. When write CRC is enabled for I_{DD4W}, current changes by approximately -5%.
- 18. When CA parity is enabled for I_{DD4W}, current changes by approximately +12%.
- 19. When 2X REF is enabled for IDD5R, current changes by approximately +0%.
- 20. When 4X REF is enabled for I_{DD5R}, current changes by approximately +0%.
- 21. When 2X REF is enabled for IPPSR, current changes by approximately +0%.
- 22. When 4X REF is enabled for IPPSR, current changes by approximately +0%.
- 23. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
- 24. I_{PP3N} test and limit is applicable for all I_{DD2x} , I_{DD3x} , I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PPS} for the noted I_{DD} tests.
- 25. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
- 26. I_{PP6x} is applicable to I_{DD6N} , I_{DD6E} , I_{DD6R} and I_{DD6A} conditions.



Table 151: I_{DD} , I_{PP} , and I_{DDQ} Current Limits; Die Rev. G (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I _{DD0} : One bank ACTIVATE-to-	x4	40	43	46	49	52	mA
PRECHARGE current	x8	45	48	51	54	57	mA
	x16	75	80	85	90	95	mA
IPPO: One bank ACTIVATE-to-	x4, x8	3	3	3	3	3	mA
PRECHARGE I _{PP} current	x16	4	4	4	4	4	mA
I _{DD1} : One bank ACTIVATE-to-	x4	52	55	58	61	64	mA
READ-to- PRECHARGE cur-	x8	57	60	63	66	69	mA
rent	x16	95	100	105	110	115	mA
I_{DD2N} : Precharge standby current	ALL	33	34	35	36	37	mA
I _{DD2NT} : Precharge standby	x4, x8	45	50	50	55	60	mA
ODT current	x16	67	75	75	78	81	mA
I_{DD2P} : Precharge powerdown current	ALL	25	25	25	25	25	mA
I DD2Q: Precharge quiet stand- by current	ALL	30	30	30	30	30	mA
I _{DD3N} : Active standby current	x4	40	43	46	49	52	mA
	x8	45	48	51	54	56	mA
	x16	49	52	55	58	61	mA
I_{PP3N} : Active standby I_{PP} current	ALL	3	3	3	3	3	mA
I _{DD3P} : Active power-down	x4	30	32	34	36	38	mA
current	x8	35	37	39	41	43	mA
	x16	39	41	43	45	47	mA
I _{DD4R} : Burst read current	x4	100	110	121	132	143	mA
	x8	125	135	146	157	168	mA
	x16	225	243	263	283	302	mA
I _{DD4W} : Burst write current	x4	100	108	117	126	135	mA
	x8	120	128	137	146	155	mA
	x16	218	233	249	266	283	mA
I _{DD5R} : Distributed refresh	x4, x8	56	58	61	64	66	mA
current (1X REF)	x16	61	64	67	69	72	mA
I _{PP5R} : Distributed refresh I _{PP} current (1X REF)	ALL	5	5	5	5	5	mA
I_{DD6N} : Self refresh current; 0–85°C ¹	ALL	31	31	31	31	31	mA
I_{DD6E} : Self refresh current; 0–95°C ^{2,4}	ALL	36	36	36	36	36	mA
I_{DD6R}: Self refresh current; 0–45C ^{3,4}	ALL	21	21	21	21	21	mA



Table 151: I_{DD} , I_{PP} , and I_{DDO} Current Limits; Die Rev. G (0° \leq T_C \leq 85°C) (Continued)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I _{DD6A} : Auto self refresh current (25°C) ⁴	ALL	8.6	8.6	8.6	8.6	8.6	mA
I _{DD6A} : Auto self refresh current (45°C) ⁴	ALL	21	21	21	21	21	mA
I _{DD6A} : Auto self refresh current (75°C) ⁴	ALL	31	31	31	31	31	mA
I _{PP6x} : Auto self refresh I _{PP} current; 0–95°C ²⁵	ALL	5	5	5	5	5	mA
I _{DD7} : Bank interleave read	x4	175	185	200	215	230	mA
current	x8	170	175	180	185	190	mA
	x16	239	249	259	269	279	mA
IPP7: Bank interleave read IPP	x4	16	17	18	19	20	mA
current	x8	15	15	15	15	15	mA
	x16	20	20	20	20	20	mA
I _{DD8} : Maximum power-down current	ALL	25	25	25	25	25	mA

- Notes: 1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0-85°C).
 - 2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0-95°C).
 - 3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0-45°C).
 - 4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
 - 5. When additive latency is enabled for I_{DD0}, current changes by approximately 0%.
 - 6. When additive latency is enabled for I_{DD1}, current changes by approximately +5%(x4/x8), +4%(x16)
 - 7. When additive latency is enabled for I_{DD2N} , current changes by approximately 0%.
 - 8. When DLL is disabled for I_{DD2N}, current changes by approximately –23%.
 - 9. When CAL is enabled for I_{DD2N}, current changes by approximately –25%.
 - 10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
 - 11. When CA parity is enabled for I_{DD2N}, current changes by approximately +7%.
 - 12. When additive latency is enabled for I_{DD3N}, current changes by approximately +1%.
 - 13. When additive latency is enabled for I_{DD4R}, current changes by approximately +5%.
 - 14. When read DBI is enabled for I_{DD4R}, current changes by approximately 0%.
 - 15. When additive latency is enabled for I_{DD4W}, current changes by approximately +3%(x4/ x8), +4%(x16).
 - 16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
 - 17. When write CRC is enabled for I_{DD4W}, current changes by approximately +10%(x4/x8), +10%(x16).
 - 18. When CA parity is enabled for I_{DD4W}, current changes by approximately +12% (x8), +12% (x16).
 - 19. When 2X REF is enabled for I_{DD5R}, current changes by approximately –14%.
 - 20. When 4X REF is enabled for IDD5R, current changes by approximately –33%.



- 21. IPPO test and limit is applicable for IDDO and IDD1 conditions.
- 22. I_{PP3N} test and limit is applicable for all I_{DD2x} , I_{DD3x} , I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PPS} for the noted I_{DD} tests.
- 23. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
- 24. The I_{DD} values must be derated (increased) when operated outside of the range 0°C \leq T_C \leq 85°C:

When $T_C < 0$ °C: I_{DD2P} , and I_{DD3P} must be derated by 6%; I_{DD4R} and I_{DD4W} must be derated by 4%; I_{DD6} , I_{DD6ET} , and I_{DD7} must be derated by 11%.

When $T_C > 85^{\circ}\text{C}$: I_{DD0} , I_{DD2N} , I_{DD2NT} , I_{DD2Q} , I_{DD3N} , I_{DD3P} , I_{DD4R} , I_{DD4W} , and I_{DD5R} must be derated by 3%; I_{DD2P} must be derated by 40%. These values are verified by design and characterization, and may not be subject to production test.

25. I_{PP6x} is applicable to I_{DD6N} , I_{DD6E} , I_{DD6R} and I_{DD6A} conditions.

Table 152: I_{DD} , I_{PP} , and I_{DDQ} Current Limits; Die Rev. H (0° \leq T_C \leq 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
IDDO: One bank ACTIVATE-to-	x4	55	55	57	60	na	mA
PRECHARGE current	x8	55	55	60	61	na	mA
	x16	75	75	80	83	na	mA
IPPO: One bank ACTIVATE-to-	x4, x8	3	3	3	3	na	mA
PRECHARGE I _{PP} current	x16	5	5	5	5	na	mA
I _{DD1} : One bank ACTIVATE-to-	x4	68	68	71	75	na	mA
READ-to- PRECHARGE cur-	x8	68	68	73	75	na	mA
rent	x16	100	100	107	111	na	mA
I _{DD2N} : Precharge standby current	ALL	39	39	42	43	na	mA
I _{DD2NT} : Precharge standby	x4, x8	43	43	48	50	na	mA
ODT current	x16	47	47	50	54	na	mA
I _{DD2P} : Precharge power- down current	ALL	27	27	27	27	na	mA
I_{DD2Q} : Precharge quiet stand- by current	ALL	34	34	36	36	na	mA
I _{DD3N} : Active standby current	x4	46	47	49	52	na	mA
	x8	46	47	49	52	na	mA
	x16	46	47	50	53	na	mA
I_{PP3N} : Active standby I _{PP} current	ALL	4.5	4.5	4.5	4.5	na	mA
I _{DD3P} : Active power-down	x4	34	34	34	37	na	mA
current	x8	36	36	39	40	na	mA
	x16	37	37	40	42	na	mA
I _{DD4R} : Burst read current	x4	135	135	157	173	na	mA
	x8	147	147	174	188	na	mA
	x16	259	259	312	341	na	mA



Table 152: I_{DD} , I_{PP} , and I_{DDQ} Current Limits; Die Rev. H (0° \leq T_C \leq 85°C) (Continued)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I _{DD4W} : Burst write current	x4	163	163	192	210	na	mA
	x8	181	181	217	234	na	mA
	x16	298	298	359	392	na	mA
I _{DD5R} : Distributed refresh	x4	49	49	51	53	na	mA
current (1X REF)	x8	49	49	51	53	na	mA
	x16	49	49	52	54	na	mA
I_{PP5R} : Distributed refresh I _{PP} current (1X REF)	ALL	5.5	5.5	5.5	5.5	na	mA
I_{DD6N} : Self refresh current; 0–85°C ¹	ALL	36	36	36	36	na	mA
IDD6E: Self refresh current; 0-	x4, x8	48	48	49	49	na	mA
95°C ^{2,4}	x16	50	50	50	51	na	mA
I_{DD6R}: Self refresh current; 0–45C ^{3,4}	ALL	26	26	26	26	na	mA
I _{DD6A} : Auto self refresh current (25°C) ⁴	ALL	15	15	15	15	na	mA
I _{DD6A} : Auto self refresh current (45°C) ⁴	ALL	26	26	26	26	na	mA
I _{DD6A} : Auto self refresh current (75°C) ⁴	ALL	36	36	36	36	na	mA
I _{PP6x} : Auto self refresh I _{PP} current; 0–95°C ²⁵	ALL	5	5	5	5	na	mA
I _{DD7} : Bank interleave read	x4	278	278	388	369	na	mA
current	x8	228	228	240	244	na	mA
	x16	311	311	321	331	na	mA
IPP7: Bank interleave read IPP	x4	21	21	26	28	na	mA
current	x8	16	16	16	16	na	mA
	x16	22	22	22	22	na	mA
I _{DD8} : Maximum power-down current	ALL	21	21	21	21	na	mA

- Notes: 1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0-85°C).
 - 2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
 - 3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0-45°C).
 - 4. I_{DD6E} , I_{DD6R} , I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
 - 5. When additive latency is enabled for I_{DD0}, current changes by approximately 0%.
 - 6. When additive latency is enabled for I_{DD1}, current changes by approximately +5%(x4/x8), +4%(x16).
 - 7. When additive latency is enabled for I_{DD2N}, current changes by approximately 0%.



- 8. When DLL is disabled for I_{DD2N}, current changes by approximately –5%.
- 9. When CAL is enabled for I_{DD2N}, current changes by approximately –25%.
- 10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
- 11. When CA parity is enabled for I_{DD2N}, current changes by approximately +7%.
- 12. When additive latency is enabled for IDD3N, current changes by approximately +1%.
- 13. When additive latency is enabled for I_{DD4R} , current changes by approximately +5%.
- 14. When read DBI is enabled for I_{DD4R}, current changes by approximately 0%.
- 15. When additive latency is enabled for I_{DD4W} , current changes by approximately +3%(x4/x8), +4%(x16).
- 16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
- 17. When write CRC is enabled for I_{DD4W}, current changes by approximately +10%(x4/x8), +10%(x16).
- 18. When CA parity is enabled for I_{DD4W}, current changes by approximately +12% (x8), +12% (x16).
- 19. When 2X REF is enabled for I_{DD5R}, current changes by approximately –14%.
- 20. When 4X REF is enabled for I_{DD5R}, current changes by approximately –33%.
- 21. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
- I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PPS} for the noted I_{DD} tests.
- 23. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
- 24. The I_{DD} values must be derated (increased) when operated outside of the range 0°C \leq T_C \leq 85°C:

When $T_C < 0$ °C: I_{DD2P} , and I_{DD3P} must be derated by 6%; I_{DD4R} and I_{DD4W} must be derated by 4%; I_{DD6} , I_{DD6ET} , and I_{DD7} must be derated by 11%.

When $T_C > 85^{\circ}\text{C}$: I_{DD0} , I_{DD1} , I_{DD2N} , I_{DD2NT} , I_{DD2Q} , I_{DD3N} , I_{DD3P} , I_{DD4R} , I_{DD4W} , and I_{DD5R} must be derated by 3%; I_{DD2P} must be derated by 40%. These values are verified by design and characterization, and may not be subject to production test.

25. I_{PP6x} is applicable to I_{DD6N}, I_{DD6E}, I_{DD6R} and I_{DD6A} conditions.

Table 153: I_{DD}, I_{PP}, and I_{DDO} Current Limits; Die Rev. J (-40° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I _{DD0} : One bank ACTIVATE-to-	x4	35	37	39	41	43	mA
PRECHARGE current	x8	37	39	41	43	44	mA
	x16	44	46	48	50	52	mA
IPPO: One bank ACTIVATE-to-	x4, x8	3	3	3	3	3	mA
PRECHARGE I _{PP} current	x16	4	4	4	4	4	mA
I _{DD1} : One bank ACTIVATE-to-	x4	48	50	51	53	55	mA
READ-to- PRECHARGE cur-	x8	52	54	56	58	60	mA
rent	x16	68	70	72	74	76	mA
I _{DD2N} : Precharge standby current	ALL	28	29	30	30	31	mA
I _{DD2NT} : Precharge standby	x4, x8	34	36	38	40	42	mA
ODT current	x16	41	44	47	50	53	mA
I _{DD2P} : Precharge power- down current	ALL	22	22	22	22	22	mA



Table 153: I_{DD} , I_{PP} , and I_{DDQ} Current Limits; Die Rev. J (-40° \leq T_C \leq 85°C) (Continued)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I _{DD2Q} : Precharge quiet stand- by current	ALL	26	26	26	26	26	mA
I _{DD3N} : Active standby current	x4	34	36	38	40	42	mA
	x8	35	37	39	41	43	mA
	x16	36	38	40	42	44	mA
I_{PP3N} : Active standby I _{PP} current	ALL	3	3	3	3	3	mA
I _{DD3P} : Active power-down	x4	28	29	30	31	32	mA
current	x8	29	30	31	32	33	mA
	x16	30	31	32	33	34	mA
I _{DD4R} : Burst read current	x4	105	114	125	135	145	mA
	x8	128	138	148	158	169	mA
	x16	223	240	260	278	296	mA
I _{DD4W} : Burst write current	x4	91	100	108	117	126	mA
	x8	108	116	125	134	142	mA
	x16	173	189	205	221	238	mA
I _{DD5R} : Distributed refresh current (1X REF)	ALL	44	45	45	46	47	mA
I_{PP5R} : Distributed refresh I _{PP} current (1X REF)	ALL	5	5	5	5	5	mA
I _{DD6N} : Self refresh current; -40–85°C ¹	ALL	32	32	32	32	32	mA
I _{DD6E} : Self refresh current; -40–95°C ^{2,4}	ALL	55	55	55	55	55	mA
I _{DD6R} : Self refresh current; -40–45°C ^{3,4}	ALL	20	20	20	20	20	mA
I _{DD6A} : Auto self refresh current (25°C) ⁴	ALL	8.2	8.2	8.2	8.2	8.2	mA
I _{DD6A} : Auto self refresh current (45°C) ⁴	ALL	20	20	20	20	20	mA
I _{DD6A} : Auto self refresh current (75°C) ⁴	ALL	30	30	30	30	30	mA
I _{DD6A} : Auto self refresh current (95°C) ⁴	ALL	55	55	55	55	55	mA
I _{PP6x} : Auto self refresh I _{PP} current; -40–95°C ²⁷	ALL	5	5	5	5	5	mA
I _{DD7} : Bank interleave read	x4	166	176	190	205	219	mA
current	x8	161	166	171	175	180	mA
	x16	222	231	240	248	257	mA



Table 153: I_{DD}, I_{PP}, and I_{DDO} Current Limits; Die Rev. J (-40° ≤ T_C ≤ 85°C) (Continued)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I _{PP7} : Bank interleave read I _{PP}	x4	11	11	11	11	11	mA
current	x8	10	10	10	10	13	mA
	x16	15	15	15	15	15	mA
I _{DD8} : Maximum power-down current	ALL	18	18	18	18	18	mA

- 1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (-40–85°C).
- 2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (-40–95°C).
- 3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (-40–45°C).
- 4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
- 5. When additive latency is enabled for IDDO, current changes by approximately +1%.
- 6. When additive latency is enabled for I_{DD1} , current changes by approximately +8%(x4/x8), +7%(x16).
- 7. When additive latency is enabled for I_{DD2N}, current changes by approximately +1%.
- 8. When DLL is disabled for I_{DD2N}, current changes by approximately –6%.
- 9. When CAL is enabled for I_{DD2N}, current changes by approximately –20%.
- 10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
- 11. When CA parity is enabled for IDD2N, current changes by approximately +13%.
- 12. When additive latency is enabled for I_{DD3N}, current changes by approximately +2%.
- When additive latency is enabled for I_{DD4R}, current changes by approximately +4(x4/x8), +3%(x16).
- 14. When read DBI is enabled for I_{DD4R} , current changes by approximately -14%(x4/x8), -20%(x16).
- 15. When additive latency is enabled for I_{DD4W} , current changes by approximately +4%(x4/x8), +3%(x16).
- 16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
- 17. When write CRC is enabled for I_{DD4W}, current changes by approximately -5%.
- 18. When CA parity is enabled for I_{DD4W} , current changes by approximately +12%.
- 19. When 2X REF is enabled for I_{DD5R}, current changes by approximately +0%.
- 20. When 4X REF is enabled for I_{DD5R}, current changes by approximately +0%.
- 21. When 2X REF is enabled for IPPSR, current changes by approximately +0%.
- 22. When 4X REF is enabled for IPPSR, current changes by approximately +0%.
- 23. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
- 24. I_{PP3N} test and limit is applicable for all I_{DD2x} , I_{DD3x} , I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PPS} for the noted I_{DD} tests.
- 25. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
- 26. The I_{DD} values must be derated (increased) when operating between 85°C < $T_C \le 95$ °C: I_{DD0} , I_{DD1} , I_{DD2N} , I_{DD2NT} , I_{DD2Q} , I_{DD3N} , I_{DD3P} , I_{DD4R} , and I_{DD4W} , must be derated by +3%; I_{DD2P} must be derated by +13%; I_{DD5R} and I_{PP5R} must be derated by +43%; All I_{PP} currents except I_{PP6x} and I_{PP5R} must be derated by +0%. These values are verified by design and characterization, and may not be subject to production test.
- 27. I_{PP6x} is applicable to I_{DD6N} , I_{DD6E} , I_{DD6R} and I_{DD6A} conditions.



Speed Bin Tables

DDR4 DRAM timing is primarily covered by two types of tables: the Speed Bin tables in this section and the tables found in the Electrical Characteristics and AC Timing Parameters section. The timing parameter tables define the applicable timing specifications based on the speed rating. The Speed Bin tables on the following pages list the ^tAA, ^tRCD, ^tRP, ^tRAS, and ^tRC limits of a given speed mark and are applicable to the CL settings in the lower half of the table provided they are applied in the correct clock range, which is noted.

Backward Compatibility

Although the speed bin tables list the slower data rates, ^tAA, CL, and CWL, it is difficult to determine whether a faster speed bin supports all of the ^tAA, CL, and CWL combinations across all the data rates of a slower speed bin. To assist in this process, please refer to the Backward Compatibility table.

Table 154: Backward Compatibility

Note 1 applies to the entire table.

		Speed Bin Supported																
Component Speed Bin	-125	-125E	-107	-107E	-093	-093E	-083D	-083	-083E	-075D	-075	-075E	-068D	-068	-068E	-062	-062E	-062Y
-125	yes																	
-125E	yes ²	yes																
-107	yes		yes															
-107E	yes ²	yes	yes ²	yes														
-093	yes		yes		yes													
-093E	yes ²	yes	yes ²	yes	yes ²	yes												
-083D	yes		yes		yes		yes											
-083	yes		yes		yes		yes	yes										
-083E	yes ²	yes	yes ²	yes	yes ²	yes	yes ²	yes ²	yes									
-075D	yes		yes		yes		yes			yes								
-075	yes		yes		yes		yes	yes		yes	yes							
-075E	yes	yes	yes	yes	yes	yes	yes	yes		yes	yes	yes						
-068D	yes		yes		yes		yes			yes			yes					
-068	yes		yes		yes		yes	yes		yes	yes		yes	yes				
-068E	yes		yes		yes		yes	yes		yes	yes		yes	yes	yes			
-062	yes		yes		yes		yes			yes			yes			yes		
-062E	yes		yes		yes		yes	yes		yes	yes		yes	yes		yes	yes	
-062Y	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes		yes	yes	yes



8Gb: x4, x8, x16 DDR4 SDRAM Speed Bin Tables





- 1. The backward compatibility table is not meant to guarantee that any new device will be a drop in replacement for an existing part number. Customers should review the operating conditions for any device to determine its suitability for use in their design.
- 2. This condition exceeds the JEDEC requirement in order to allow additional flexibility for components. However, JEDEC SPD compliance may force modules to only support the JEDEC-defined value. Refer to the SPD documentation for further clarification.

8Gb: x4, x8, x16 DDR4 SDRAM Speed Bin Tables

Table 155: DDR4-1600 Speed Bins and Operating Conditions

Notes 1-3 apply to the entire table

DDR4-1600 Sp	eed Bin						-12	25E	-1	25	
CL-nRCD-nRP							11-1	1-11	12-1	2-12	
Parameter						Symbol	Min	Max	Min	Max	Unit
Internal READ o	command to first	data		^t AA	13.75 (13.50) ⁴	19.00 ⁶	15.00	19.00 ⁶	ns		
Internal READ o	command to first	data with read	DBI enabled	^t AA_DBI	^t AA (MIN) + 2 <i>n</i> CK	^t AA (MAX) + 2 <i>n</i> CK	^t AA (MIN) + 2 <i>n</i> CK	^t AA (MAX) + 2 <i>n</i> CK	ns		
ACTIVATE-to-in	ternal READ or V	VRITE delay time	•			^t RCD	13.75 (13.50) ⁴	-	15.00	-	ns
PRECHARGE co	mmand period			^t RP	13.75 (13.50) ⁴	-	15.00	-	ns		
ACTIVATE-to-PF	RECHARGE comm	and period				^t RAS	35	9 × ^t REFI	35	9 × ^t REFI	ns
ACTIVATE-to-A	CTIVATE or REFRI	ESH command po	eriod			tRC ⁵	^t RAS + ^t RP	_	^t RAS + ^t RP	_	ns
Data Rate Max (MT/s)	Equivalent Speed Bin	^t AAmin(ns): non-DB	READ CL: nonDBI	READ CL: DBI	WRITE CWL	Symbol	Min	Max	Min	Max	Unit
1333	-	13.50	9	11	9	tCK (AVG)	1.500	1.900 ⁶	Rese	rved	ns
	-	15.00	10	12		tCK (AVG)	1.500 ⁶	1.900 ⁶	1.500	1.900 ⁶	ns
1600	-125E	13.75	11	13	9, 11	tCK (AVG)	1.250	<1.500	Rese	rved	ns
	-125	15.00	12	14		tCK (AVG)			1.250	<1.500	ns
Supported CL so	ettings						9, 10 ⁶	, 11-12	10,	12	nCK
Supported CL so	ettings with read	l DBI					11, 12 ⁶ , 13-14		12,	nCK	
Supported CWL	_ settings						9,	11	9,	nCK	





- 1. Speed Bin table is only valid with DLL enabled.
- 2. When operating in 2^tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^tCK range.
- 3. The programmed value of CWL must be less than or equal to the programmed value of CL.
- 4. This value applies to non-native ^tCK-CL-*n*RCD-*n*RP combinations.
- 5. When calculating ^tRC in clocks, values may not be used in a combination that violate ^tRAS or ^tRP.
- 6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

8Gb: x4, x8, x16 DDR4 SDRAM Speed Bin Tables

Table 156: DDR4-1866 Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-1866 Sp	eed Bin						-10)7E	-10	07	
CL-nRCD-nRP							13-1	3-13	14-1	4-14	
Parameter						Symbol	Min	Max	Min	Max	Unit
Internal READ o	ommand to first	data	^t AA	13.92 (13.50) ⁴	19.00 ⁶	15.00	19.00 ⁶	ns			
Internal READ o	command to first	data with read D	^t AA_DBI	^t AA (MIN) + 2 <i>n</i> CK	^t AA (MAX) + 2 <i>n</i> CK	^t AA (MIN) + 2 <i>n</i> CK	^t AA (MAX) + 2 <i>n</i> CK	ns			
ACTIVATE to int	ternal READ or W	/RITE delay time				^t RCD	13.92 (13.50) ⁴	_	15.00	-	ns
PRECHARGE con	mmand period					^t RP	13.92 (13.50) ⁴	_	15.00	1	ns
ACTIVATE-to-PR	RECHARGE comm	and period				^t RAS	34	9 × ^t REFI	34	9 × ^t REFI	ns
ACTIVATE-to-AG	CTIVATE or REFRE	ESH command pe	riod			tRC ⁵	^t RAS + ^t RP	_	^t RAS + ^t RP	-	ns
Data Rate Max (MT/s)	Equivalent Speed Bin	^t AAmin: non- DBI	READ CL: nonDBI	READ CL: DBI	WRITE CWL	Symbol	Min	Max	Min	Max	Unit
1333	_	13.50	9	11	9	^t CK (AVG)	1.500	1.900 ⁶	Rese	rved	ns
	_	15.00	10	12		tCK (AVG)	1.500 ⁶	1.900 ⁶	1.500	1.900 ⁶	ns
1600	-125E	13.75	11	13	9, 11	^t CK (AVG)	1.250	<1.500	Rese	rved	ns
	-125	15.00	12	14		tCK (AVG)			1.250	<1.500	ns
1866	-107E	13.92	13	15	10, 12	tCK (AVG)	1.071	<1.250	Rese	rved	ns
	-107	15.00	14	16		tCK (AVG)			1.071	<1.250	ns
Supported CL se	ettings						9, 10 ⁶	11–14	10, 1	2, 14	nCK
Supported CL se	ettings with read	DBI					11, 12 ⁶	, 13–16	12, 1	nCK	
Supported CWL	settings						9–	12	9–	12	nCK





- 1. Speed Bin table is only valid with DLL enabled.
- 2. When operating in 2^tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^tCK range.
- 3. The programmed value of CWL must be less than or equal to the programmed value of CL.
- 4. This value applies to non-native ^tCK-CL-*n*RCD-*n*RP combinations.
- 5. When calculating ^tRC in clocks, values may not be used in a combination that violate ^tRAS or ^tRP.
- 6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

8Gb: x4, x8, x16 DDR4 SDRAM Speed Bin Tables

Table 157: DDR4-2133 Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-2133 Sp	eed Bin						-09	3E	-0		
CL-nRCD-nRP							15-1	5-15	16-1	6-16	
Parameter						Symbol	Min	Max	Min	Max	Unit
Internal READ o	ommand to first	data	^t AA	14.06 (13.50) ⁴	19.00 ⁶	15.00	19.00 ⁶	ns			
Internal READ o	ommand to first	data with read D	^t AA_DBI	^t AA (MIN) + 3 <i>n</i> CK	^t AA (MAX) + 3 <i>n</i> CK	^t AA (MIN) + 3 <i>n</i> CK	^t AA (MAX) + 3 <i>n</i> CK	ns			
ACTIVATE to int	ernal READ or W	RITE delay time				^t RCD	14.06 (13.50) ⁴	_	15.00	_	ns
PRECHARGE cor	nmand period					^t RP	14.06 (13.50) ⁴	_	15.00	_	ns
ACTIVATE-to-PR	ECHARGE comm	and period				^t RAS	33	9 × ^t REFI	33	9 × ^t REFI	ns
ACTIVATE-to-AC	CTIVATE or REFRE	SH command pe	riod			tRC ⁵	^t RAS + ^t RP	-	^t RAS + ^t RP	_	ns
Data Rate Max (MT/s)	Equivalent Speed Bin	^t AAmin (ns): non-DBI	READ CL: non-DBI	READ CL: DBI	WRITE CWL	Symbol	Min	Мах	Min	Мах	Unit
1333	_	13.50	9	11	9	^t CK (AVG)	1.500	1.900 ⁶	Rese	rved	ns
	-	15.00	10	12		^t CK (AVG)	1.500 ⁶	1.900 ⁶	1.500	1.900 ⁶	ns
1600	-125E	13.75	11	13	9,11	^t CK (AVG)	1.250	<1.500	Rese	rved	ns
	-125	15.00	12	14		^t CK (AVG)			1.250	<1.500	ns
1866	-107E	13.92	13	15	10, 12	^t CK (AVG)	1.071	<1.250	Rese	rved	ns
	-107	15.00	14	16		^t CK (AVG)			1.071	<1.250	ns
2133	-093E	14.06	15	18	11, 14	^t CK (AVG)	0.937	<1.071	Rese	rved	ns
	-093	15.00	16	19		^t CK (AVG)			0.937	<1.071	ns
Supported CL se	ettings						9, 10 ⁶ ,		10, 12,	nCK	
Supported CL se	ttings with read	DBI					11, 12 ⁶ , 13	3–16, 18-19	12, 14,	nCK	
Supported CWL	settings						9, 10, 1	I, 12, 14	9, 10, 1	1, 12, 14	nCK





- 1. Speed Bin table is only valid with DLL enabled.
- 2. When operating in 2^tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^tCK range.
- 3. The programmed value of CWL must be less than or equal to the programmed value of CL.
- 4. This value applies to non-native ^tCK-CL-*n*RCD-*n*RP combinations.
- 5. When calculating ^tRC in clocks, values may not be used in a combination that violate ^tRAS or ^tRP.
- 6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

8Gb: x4, x8, x16 DDR4 SDRAM Speed Bin Tables

Table 158: DDR4-2400 Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-2400 S	peed Bin						-0	83E	-083		-083D		
CL-nRCD-nRP	•						16-16-16		17-17-17		18-18-18		
Parameter						Symbol	Min	Max	Min	Max	Min	Max	Unit
Internal READ	command to f	irst data			^t AA	13.32	19.00 ⁶	14.16 (13.75) ⁴	19.00 ⁶	15.00	19.00 ⁶	ns	
Internal READ	command to f	^t AA_DBI	^t AA (MIN) + 3 <i>n</i> CK	^t AA (MAX) + 3 <i>n</i> CK	^t AA (MIN) + 3 <i>n</i> CK	^t AA (MAX) + 3 <i>n</i> CK	^t AA (MIN) + 3 <i>n</i> CK	^t AA (MAX) + 3 <i>n</i> CK	ns				
ACTIVATE to i	nternal READ o	r WRITE delay	time	^t RCD	13.32	_	14.16 (13.75) ⁴	-	15.00	19.00	ns		
PRECHARGE c	ommand period	b				^t RP	13.32	_	14.16 (13.75) ⁴	_	15.00	19.00	ns
ACTIVATE-to-F	PRECHARGE cor	nmand period				^t RAS	32	9 × ^t REFI	32	9 × ^t REFI	32	9 × ^t REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period							^t RAS + ^t RP	_	^t RAS + ^t RP	_	^t RAS + ^t RP	_	ns
Data Rate Max (MT/s)	Equivalent Speed Bin	^t AAmin (ns): non-DBI	READ CL: non-DBI	READ CL: DBI	WRITE CWL	Symbol	Min	Max	Min	Max	Min	Max	Unit
1333	_	13.50	9	11	9	tCK (AVG)	1.500	1.900 ⁶	Rese	erved	Reserved		ns
	_	15.00	10	12		tCK (AVG)	1.500 ⁶	1.900 ⁶	1.500	1.900 ⁶	1.500	1.900 ⁶	ns
1600	-125E	13.75	11	13	9, 11	tCK (AVG)	1.250	<1.500	1.250	<1.500	Rese	erved	ns
	-125	15.00	12	14		tCK (AVG)					1.250	<1.500	ns
1866	-107E	13.92	13	15	10, 12	tCK (AVG)	1.071	<1.250	1.071	<1.250	Rese	erved	ns
	-107	15.00	14	16		tCK (AVG)					1.071	<1.250	ns
2133	-093E	14.06	15	18	11, 14	^t CK (AVG)	0.937	<1.071	0.937	<1.071	Rese	erved	ns
	-093	15.00	16	19		^t CK (AVG)					0.937	<1.071	ns
2400	-083E	13.32	16	19	12, 16	^t CK (AVG)	0.833	<0.937	Rese	erved	Rese	erved	ns
	-083	14.16	17	20		tCK (AVG)			0.833	<0.937			ns
	-083D	15.00	18	21		tCK (AVG)					0.833	<0.937	ns
Supported CL								, 10 ⁶ , 11–18 10–18			10, 12, 14, 16, 18		nCK
Supported CL	settings with re	ead DBI					11, 12 ⁶ , 13–16, 18–21		12–16, 18–21		12, 14, 16, 19, 21		nCK
Supported CV	/L settings						9–12, 14, 16 9-12, 14, 16			14, 16	9–12,	nCK	





- 1. Speed Bin table is only valid with DLL enabled.
- 2. When operating in 2^tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^tCK range.
- 3. The programmed value of CWL must be less than or equal to the programmed value of CL.
- 4. This value applies to non-native ^tCK-CL-*n*RCD-*n*RP combinations.
- 5. When calculating ^tRC in clocks, values may not be used in a combination that violate ^tRAS or ^tRP.
- 6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

8Gb: x4, x8, x16 DDR4 SDRAM Speed Bin Tables

Table 159: DDR4-2666 Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-2666 S	peed Bin						-0	75E	-0	75	-07		
CL-nRCD-nRP							18-1	18-18-18		19-19	20-20-20		
Parameter						Symbol	Min	Мах	Min	Max	Min	Max	Unit
Internal READ	command to f		^t AA	13.50	19.00 ⁶	14.25 (13.75) ⁴	19.00 ⁶	15.00	19.00 ⁶	ns			
Internal READ	command to f	^t AA_DBI	tAA (MIN) + 3nCK	^t AA (MAX) + 3 <i>n</i> CK	^t AA (MIN) + 3 <i>n</i> CK	^t AA (MAX) + 3 <i>n</i> CK	tAA (MIN) + 3nCK	^t AA (MAX) + 3 <i>n</i> CK	ns				
ACTIVATE to i	nternal READ o	^t RCD	13.50	_	14.25 (13.75) ⁴	_	15.00	-	ns				
PRECHARGE co	ommand period	^t RP	13.50	_	14.25 (13.75) ⁴	_	15.00	_	ns				
ACTIVATE-to-F	RECHARGE cor	nmand period				^t RAS	32	9 × ^t REFI	32	9 × ^t REFI	32	9 × ^t REFI	ns
ACTIVATE-to-A	ACTIVATE or RE	FRESH comma	nd period			^t RC ⁵	^t RAS +	_	^t RAS +	_	^t RAS +	-	ns
Data Rate Max (MT/s)	Equivalent Speed Bin	^t AAmin (ns): non-DBI	READ CL: non-DBI	READ CL: DBI	WRITE	Symbol	Min	Max	Min	Max	Min	Max	Unit
1333	-	13.50	9	11	9	tCK (AVG)	1.500	1.900 ⁶	Rese	erved	Rese	erved	ns
	-	15.00	10	12] 9	tCK (AVG)	1.500	1.900	1.500	1.900 ⁶	1.500	1.900 ⁶	ns
1600	-125E	13.75	11	13	9, 11	tCK (AVG)	1.250	<1.500	1.250	<1.500	Reserved		ns
	-125	15.00	12	14	9, 11	tCK (AVG)	1.230	<1.500	1.230	<1.500	1.250	<1.500	ns
1866	-107E	13.92	13	15	10, 12	tCK (AVG)	1.071	<1.250	1.071	<1.250	Reserved		ns
	-107	15.00	14	16	10, 12	^t CK (AVG)	1.071	\1.230	1.071	<1.230	1.071	<1.250	ns
2133	-093E	14.06	15	18	11, 14	tCK (AVG)	0.937	<1.071	0.937	<1.071	Rese	erved	ns
	-093	15.00	16	19	11, 14	tCK (AVG)					0.937	<1.071	ns
2400	-083E	13.32	16	19		tCK (AVG)		erved	Rese	erved	Rese	erved	ns
	-083	14.16	17	20	12, 16	tCK (AVG)	J 0.833	<0.937	0.833	<0.937			ns
	-083D	15.00	18	21		tCK (AVG)		10.007			0.833	<0.937	ns
2666	-075E	13.50	18	21	1	tCK (AVG)	4		Rese	erved	Reserved		ns
	-075	14.25	19	22	14, 18	tCK (AVG)	0.750	<0.833	0.750	<0.833			ns
	-075D	15.00	20	23		tCK (AVG)					0.750	<0.833	ns
Supported CL	settings						9-	-20	10)-20		4, 16, 18, 20	nCK

Table 159: DDR4-2666 Speed Bins and Operating Conditions (Continued)

Notes 1-3 apply to the entire table

Notes 1-3 apply to the entire table								
DDR4-2666 Speed Bin		-07	75E	-0	75	-07	75D	
CL-nRCD-nRP		18-1	18-18	19-1	19-19	20-2	20-20	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Supported CL settings with read DBI		11–16	, 18–23	12–16	, 18–23	12, 14, 1	6, 19, 21,	nCK
						2	23	
Supported CWL settings		9–12, 1	4, 16, 18	9–12, 1	4, 16, 18	9–12, 1	4, 16, 18	nCK



8Gb: x4, x8, x16 DDR4 SDRAM Speed Bin Tables





Notes:

- 1. Speed Bin table is only valid with DLL enabled.
- 2. When operating in 2^tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^tCK range.
- 3. The programmed value of CWL must be less than or equal to the programmed value of CL.
- 4. This value applies to non-native ^tCK-CL-*n*RCD-*n*RP combinations.
- 5. When calculating ^tRC in clocks, values may not be used in a combination that violate ^tRAS or ^tRP.
- 6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

8Gb: x4, x8, x16 DDR4 SDRAM Speed Bin Tables

Table 160: DDR4-2933 Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-2933 Speed Bin							-068E -068		-00	68D			
CL-nRCD-nRF	•						20-2	20-20	21-2	21-21	22-2	22-22	
Parameter						Symbol	Min	Max	Min	Max	Min	Max	Unit
Internal READ	command to f	irst data				^t AA	13.64	19.00 ⁶	14.32 (13.75) ⁴	19.00 ⁶	15.00	19.00 ⁶	ns
Internal READ	command to f	irst data with r	ead DBI en	abled		^t AA_DBI	^t AA (MIN) + 4 <i>n</i> CK	^t AA (MAX) + 4nCK	^t AA (MIN) + 4 <i>n</i> CK	^t AA (MAX) + 4 <i>n</i> CK	tAA (MIN) + 4nCK	^t AA (MAX) + 4nCK	ns
ACTIVATE-to-i	nternal READ o	or WRITE delay	time			^t RCD	13.64	_	14.32 (13.75) ⁴	_	15.00	-	ns
PRECHARGE c	ommand perio	d				^t RP	13.64	_	14.32 (13.75) ⁴	_	15.00	_	ns
ACTIVATE-to-l	PRECHARGE co	mmand period				^t RAS	32	9 × ^t REFI	32	9 × ^t REFI	32	9 × ^t REFI	ns
ACTIVATE-to-	ACTIVATE or RE	FRESH comma	nd period			^t RC ⁵	^t RAS +	_	^t RAS +	_	^t RAS +	_	ns
Data Rate Max (MT/s)	Equivalent Speed Bin	tAAmin(ns): non-DBI	READ CL: non-DBI	READ CL: DBI	WRITE CWL	Symbol	Min	Max	Min	Max	Min	Max	Unit
1333	_	13.50	9	11	9	tCK (AVG)	Res	erved	Res	erved	Rese	erved	ns
	_	15.00	10	12	1	tCK (AVG)	1.500	1.900 ⁶	1.500	1.900 ⁶	1.500	1.900 ⁶	ns
1600	-125E	13.75	11	13	9, 11	tCK (AVG)	1.250	<1.500	1.250	<1.500	Rese	erved	ns
	-125	15.00	12	14	1	tCK (AVG)	1				1.250	<1.500	ns
1866	-107E	13.92	13	15	10, 12	tCK (AVG)	1.071	<1.250	1.071	<1.250	Rese	erved	ns
	-107	15.00	14	16		tCK (AVG)					1.071	<1.250	ns
2133	-093E	14.06	15	18	11, 14	tCK (AVG)	0.937	<1.071	0.937	<1.071	Rese	erved	ns
	-093	15.00	16	19]	tCK (AVG)]				0.937	<1.071	ns
2400	-083E	13.32	16	19	12, 16	tCK (AVG)	Res	erved	Res	erved	Rese	erved	ns
	-083	14.16	17	20		tCK (AVG)	0.833	<0.937	0.833	<0.937			ns
	083D	15.00	18	21		tCK (AVG)					0.833	<0.937	ns
2666	-075E	13.50	18	21	14, 18	tCK (AVG)	Res	erved	Res	erved	Rese	erved	ns
	-075	14.25	19	22]	tCK (AVG)	0.750	<0.833	0.750	<0.833			ns
	-075D	15.00	20	23		tCK (AVG)					0.750	<0.833	ns

Table 160: DDR4-2933 Speed Bins and Operating Conditions (Continued)

Notes 1–3 apply to the entire table

DDR4-2933 S	DDR4-2933 Speed Bin							68E	-0	68	-06	58D	
CL-nRCD-nRP)						20-2	20-20	21-2	Reserved		22-22	
Parameter						Symbol	Min	Max	Min	Max	Min	Max	Unit
2933	-068E	13.64	20	24	16, 20	tCK (AVG)	0.682	<0.750	Rese	erved	Rese	erved	ns
	-068	14.32	21	25		tCK (AVG)			0.682	<0.750			ns
	-068D	15.00	22	26		tCK (AVG)					0.682	<0.750	ns
	_	16.37	24	28		tCK (AVG)	Rese	erved	Rese	erved	Rese	erved	ns
Supported CL	settings						10	-22	10	-22	10, 12, 1	4, 16, 18,	nCK
											20	, 22	
Supported CL	settings with re	ead DBI					12–16	, 18–26	12–16	,18–23,	12, 14, 1	6, 19, 21,	nCK
									25	-26	23	, 26	
Supported CW	/L settings						9–12, 14	4, 16, 18,	9–12, 14	4, 16, 18,	9–12, 1	4, 16, 18,	nCK
							2	20	2	20	2	20	





Notes:

- 1. Speed Bin table is only valid with DLL enabled.
- 2. When operating in 2^tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^tCK range.
- 3. The programmed value of CWL must be less than or equal to the programmed value of CL.
- 4. This value applies to non-native ^tCK-CL-*n*RCD-*n*RP combinations.
- 5. When calculating ^tRC in clocks, values may not be used in a combination that violate ^tRAS or ^tRP.
- 6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Table 161: DDR4-3200 Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-3200 Speed Bin						-06	52Y ⁶	-0	62E	-0)62		
CL-nRCD-nRF	•						22-2	22-22	22-2	22-22	24-2	24-24	
Parameter						Symbol	Min	Max	Min	Max	Min	Max	Unit
Internal READ	command to f	irst data				^t AA	13.75 (13.32) ⁴	19.00 ⁶	13.75	19.00 ⁶	15.00	19.00 ⁶	ns
Internal READ	command to f	irst data with ı	ead DBI en	abled		^t AA_DBI	tAA (MIN) + 4nCK	^t AA (MAX) + 4 <i>n</i> CK	^t AA (MIN) + 4 <i>n</i> CK	^t AA (MAX) + 4nCK	^t AA (MIN) + 4 <i>n</i> CK	^t AA (MAX) + 4nCK	ns
ACTIVATE-to-	internal READ o	or WRITE delay	time			^t RCD	13.75 (13.32) ⁴	-	13.75	_	15.00	_	ns
PRECHARGE of	ommand perio	d				^t RP	13.75 (13.32) ⁴	_	13.75	_	15.00	_	ns
ACTIVATE-to-	PRECHARGE co	mmand period				^t RAS	32	9 × ^t REFI	32	9 × ^t REFI	32	9 × ^t REFI	ns
ACTIVATE-to-	ACTIVATE or RE	FRESH comma	nd period			tRC ⁵	^t RAS +	_	^t RAS +	_	^t RAS +	_	ns
Data Rate Max (MT/s)	Equivalent Speed Bin	^t AAmin (ns): non-DBI	READ CL: non-DBI	READ CL: DBI	WRITE CWL	Symbol	Min	Max	Min	Max	Min	Max	Unit
1333	-	13.50	9	11	9	^t CK (AVG)	1.500	1.900 ⁶	Res	erved	Res	erved	ns
	-	15.00	10	12		tCK (AVG)]		1.500	1.900 ⁶	1.500	1.900 ⁶	ns
1600	-125E	13.75	11	13	9, 11	^t CK (AVG)	1.250	<1.500	1.250	<1.500	Res	erved	ns
	-125	15.00	12	14		tCK (AVG)]				1.250	<1.500	ns
1866	-107E	13.92	13	15	10, 12	tCK (AVG)	1.071	<1.250	1.071	<1.250	Res	erved	ns
	-107	15.00	14	16		^t CK (AVG)					1.071	<1.250	ns
2133	-093E	14.06	15	18	11, 14	^t CK (AVG)	0.937	<1.071	0.937	<1.071	Res	erved	ns
	-093	15.00	16	19		tCK (AVG)]				0.937	<1.071	ns
2400	-083E	13.32	16	19	12, 16	^t CK (AVG)	0.833	<0.937	Res	erved	Res	erved	ns
	-083	14.16	17	20		tCK (AVG)			0.833	<0.937			ns
	-083D	15.00	18	21		^t CK (AVG)					0.833	<0.937	ns
2666	-075E	13.50	18	21	14, 18	^t CK (AVG)	0.750	<0.833	Res	erved	Res	erved	ns
	-075	14.25	19	22		^t CK (AVG)			0.750	<0.833			ns
	-075D	15.00	20	23		tCK (AVG)					0.750	<0.833	ns



8Gb: x4, x8, x16 DDR4 SDRAM Speed Bin Tables

Table 161: DDR4-3200 Speed Bins and Operating Conditions (Continued)

Notes 1–3 apply to the entire table

DDR4-3200 S	DR4-3200 Speed Bin						-06	52Y ⁶	-0	62E	-0	062	
CL-nRCD-nRF	•						22-2	22-22	22-2	22-22	24-2	24-24	
Parameter						Symbol	Min	Max	Min	Max	Min	Max	Unit
2933	-068E	13.64	20	24	16, 20	tCK (AVG)	Rese	erved	Res	erved	Res	erved	ns
	-068	14.32	21	25		tCK (AVG)	0.682	<0.750	0.682	<0.750			ns
	-068D	15.00	22	26		tCK (AVG)			0.682	<0.750	0.682	<0.750	ns
	_	16.37	24	28		tCK (AVG)					0.682	<0.750	ns
3200	-062E	13.75	22	26	16, 20	tCK (AVG)	0.625	<0.682	0.625	<0.682	Res	erved	ns
	-062	15.00	24	28		tCK (AVG)					0.625	<0.682	ns
Supported CL	settings						9–2	2, 24	10–2	22, 24	10, 12, 1	4, 16, 18,	nCK
											20, 2	22, 24	
Supported CL	settings with re	ead DBI					11–16	, 18–23,	12–16	, 18–23,	12, 14, 1	6, 19, 21,	nCK
							25-2	26, 28	25-2	26, 28	23, 2	26, 28	
Supported CV	VL settings						9–12, 1	4, 16, 18,	9–12, 1	4, 16, 18,	9–12, 1	4, 16, 18,	nCK
							2	20	:	20		20	



Notes

- 1. Speed Bin table is only valid with DLL enabled.
- 2. When operating in 2^tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^tCK range.
- 3. The programmed value of CWL must be less than or equal to the programmed value of CL.
- 4. This value applies to non-native ^tCK-CL-*n*RCD-*n*RP combinations.
- 5. When calculating ^tRC in clocks, values may not be used in a combination that violate ^tRAS or ^tRP.
- 6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Refresh Parameters By Device Density

Table 162: Refresh Parameters by Device Density

Parameter		Symbol	2Gb	4Gb	8Gb	16Gb	Unit	Notes
REF command to ACT or REF command time	^t RFC (All bank groups)	160	260	350	350	ns	
Average periodic refresh interval	^t REFI	-40°C ≤ T _C ≤ 85°C	7.8	7.8	7.8	7.8	μs	
		85°C < T _C ≤ 95°C	3.9	3.9	3.9	3.9	μs	1
		95°C < T _C ≤ 105°C	1.95	1.95	1.95	1.95	μs	1

Note: 1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if the devices support these options or requirements.

AC Electrical Characteristics and AC Timing Parameters

Table 163: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400

			DDR4	l-1600	DDR4	-1866	DDR4	-2133	DDR4	-2400		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
			C	lock Tin	ning							
Clock period average	(DLL off mode)	^t CK (AVG, DLL_OFF)	8	20	8	20	8	20	8	20	ns	
Clock period average		^t CK (AVG, DLL_ON)	1.25	1.9	1.071	1.9	0.937	1.9	0.833	1.9	ns	3 , 13
High pulse width aver	age	^t CH (AVG)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	^t CK (AVG)	
Low pulse width avera	age	^t CL (AVG)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	^t CK (AVG)	
Clock period jitter	Total	^t JITper_tot	-63	63	-54	54	-47	47	-42	42	ps	17 , 18
	Deterministic	^t JlTper_dj	-31	31	-27	27	-23	23	-21	21	ps	17
	DLL locking	^t JITper,lck	-50	50	-43	43	-38	38	-33	33	ps	
Clock absolute period		^t CK (ABS)	MIN =	tCK (AV	G) MIN +		ot MIN; Note tot MAX		K (AVG) I	MAX +	ps	
Clock absolute high policy (includes duty cycle jit		^t CH (ABS)	0.45	_	0.45	_	0.45	-	0.45	_	^t CK (AVG)	
Clock absolute low pu (includes duty cycle jit		^t CL (ABS)	0.45	_	0.45	_	0.45	-	0.45	_	^t CK (AVG)	
Cycle-to-cycle jitter	Total	^t JITcc _tot	_	125	_	107	_	94	_	83	ps	
	DLL locking	^t JITcc,lck	_	100	_	86	_	75	-	67	ps	



8Gb: x4, x8, x16 DDR4 SDRAM AC Electrical Characteristics and AC Timing Parameters

			DDR4	-1600	DDR4	-1866	DDR4	-2133	DDR4	-2400		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Cumulative error across	2 cycles	^t ERR2per	-92	92	-79	79	-69	69	-61	61	ps	
	3 cycles	^t ERR3per	-109	109	-94	94	-82	82	-73	73	ps	
	4 cycles	^t ERR4per	-121	121	-104	104	-91	91	-81	81	ps	
	5 cycles	^t ERR5per	-131	131	-112	112	-98	98	-87	87	ps	
	6 cycles	^t ERR6per	-139	139	-119	119	-104	104	-92	92	ps	
	7 cycles	^t ERR7per	-145	145	-124	124	-109	109	-97	97	ps	
	8 cycles	^t ERR8per	-151	151	-129	129	-113	113	-101	101	ps	
	9 cycles	^t ERR9per	-156	156	-134	134	-117	117	-104	104	ps	
	10 cycles	tERR10per	-160	160	-137	137	-120	120	-107	107	ps	
	11 cycles	tERR11per	-164	164	-141	141	-123	123	-110	110	ps	
	12 cycles	^t ERR12per	-168	168	-144	144	-126	126	-112	112	ps	
	n = 13, 14 49,	^t ERR <i>n</i> per		tERR <i>n</i>	per MIN =	= (1 + 0.6	8ln[<i>n</i>]) ×	tJITper_t	ot MIN		ps	
	50 cycles			^t ERR <i>n</i> p	er MAX =	= (1 + 0.6	8ln[<i>n</i>]) ×	^t JITper_t	ot MAX			
			DQ	Input T	iming						1	
Data setup time to DQS_t, DQS_c	Base (calibrated V _{REF})	^t DS					ver Speci 15 ^t CK to				_	
	Noncalibrated V _{REF}	^t PDA_S				minimun	n of 0.5U	l			UI	22
Data hold time from DQS_t, DQS_c	Base (calibrated V _{REF})	^t DH					ver Speci 15 ^t CK to				_	
	Noncalibrated V _{REF}	^t PDA_H				minimun	n of 0.5U	I			UI	22
DQ and DM minimum of for each input	data pulse width	^t DIPW	0.58	_	0.58	_	0.58	_	0.58	_	UI	
		DQ	Output	Timing	(DLL ena	abled)	•	'		'		
DQS_t, DQS_c to DQ ske	ew, per group, per	^t DQSQ	_	0.16	-	0.16	_	0.16	_	0.17	UI	
DQ output hold time fr	om DQS_t, DQS_c	^t QH	0.76	_	0.76	_	0.76	_	0.74	_	UI	
Data Valid Window per ^t DQSQ each device's ou	-	^t DVW _d	0.63		0.63		0.64		0.64		UI	
Data Valid Window per ^t QH - ^t DQSQ each device		^t DVW _p	0.66	-	0.66	-	0.69	-	0.72	-	UI	

		DDR4	-1600	DDR4	-1866	DDR4	-2133	DDR4	l-2400		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
DQ Low-Z time from CK_t, CK_c	^t LZDQ	-450	225	-390	195	-360	180	-330	175	ps	
DQ High-Z time from CK_t, CK_c	tHZDQ	_	225	_	195	_	180	_	175	ps	
		DQ Str	obe Inp	ut Timin	g						
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 1 ^t CK preamble	^t DQSS _{1ck}	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	CK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 2 ^t CK preamble	^t DQSS _{2ck}	N	A	N	A	N	İA	-0.50	0.50	CK	
DQS_t, DQS_c differential input low pulse width	^t DQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	CK	
DQS_t, DQS_c differential input high pulse width	^t DQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	CK	
DQS_t, DQS_c differential input high pulse width for 2 ^t CK preamble	^t DQSH2PRE	N	A	N	A	N	İΑ	1.46	-	CK	
DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge for 1 ^t CK preamble	^t DSS _{1ck}	0.18	_	0.18	_	0.18	_	0.18	-	CK	
DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge for 2 ^t CK preamble	^t DSS _{2ck}	N	Α	N	A	N	İΑ	0	-	CK	
DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge for 1 ^t CK preamble	^t DSH _{1ck}	0.18	_	0.18	_	0.18	_	0.18	-	CK	
DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge for 2 ^t CK preamble	^t DSH _{2ck}	N	A	N	A	N	A	0	-	CK	
DQS_t, DQS_c differential WRITE preamble for 1 ^t CK preamble	^t WPRE _{1ck}	0.9	_	0.9	_	0.9	_	0.9	_	CK	
DQS_t, DQS_c differential WRITE preamble for 2 ^t CK preamble	^t WPRE _{2ck}	N	Α	N	A	N	İΑ	1.8	-	CK	
DQS_t, DQS_c differential WRITE postamble	^t WPST	0.33	_	0.33	_	0.33	_	0.33	-	CK	
	DQS St	robe Out	tput Tim	ing (DLI	enable	d)	'	'	'	'	
DQS_t, DQS_c rising edge output access time from rising CK_t, CK_c	^t DQSCK	-225	225	-195	195	-180	180	-175	175	ps	
DQS_t, DQS_c rising edge output variance window per DRAM	^t DQSCKi	_	370	_	330	-	310	_	290	ps	
DQS_t, DQS_c differential output high time	^t QSH	0.4	_	0.4	-	0.4	-	0.4	-	CK	

			DDR4	l-1600	DDR4	-1866	DDR4	-2133	DDR4	l- 2400		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
DQS_t, DQS_c differentia	al output low	^t QSL	0.4	-	0.4	-	0.4	_	0.4	-	CK	
time												
DQS_t, DQS_c Low-Z tim	ne (RL - 1)	^t LZDQS	-450	225	-390	195	-360	180	-330	175	ps	
DQS_t, DQS_c High-Z tin	ne (RL + BL/2)	^t HZDQS	_	225	_	195	_	180	_	175	ps	
DQS_t, DQS_c differentiable for 1 ^t CK preamble	al READ pream-	^t RPRE _{1ck}	0.9	_	0.9	-	0.9	-	0.9	-	CK	20
DQS_t, DQS_c differentiable ble for 2 ^t CK preamble	al READ pream-	^t RPRE _{2ck}	N	IA	N	A	N	IA	1.8	-	CK	20
DQS_t, DQS_c differentiable	al READ postam-	^t RPST	0.33	_	0.33	_	0.33	_	0.33	_	CK	21
		Co	ommand	and Ad	dress Ti	ming	'			'		'
DLL locking time		^t DLLK	597	_	597	_	768	_	768	_	CK	2, 4
CMD, ADDR setup time	Base	^t IS	115	_	100	_	80	_	62	_	ps	
to CK_t, CK_c Base referenced to V _{IH(AC)} and V _{IL(AC)} levels	V _{REFCA}	^t IS _{VREF}	215	_	200	_	180	-	162	-	ps	
CMD, ADDR hold time	Base	^t IH	140	_	125	_	105	_	87	_	ps	
to CK_t, CK_c Base referenced to V _{IH(DC)} and V _{IL(DC)} levels	V _{REFCA}	^t IH _{VREF}	215	-	200	-	180	-	162	-	ps	
CTRL, ADDR pulse width	for each input	^t IPW	600	_	525	-	460	-	410	_	ps	
ACTIVATE to internal RE lay	AD or WRITE de-	^t RCD		!	See Sp	beed Bin	Tables fo	r ^t RCD	!		ns	
PRECHARGE command p	period	^t RP			See S	peed Bin	Tables fo	or ^t RP			ns	
ACTIVATE-to-PRECHARG	iE command peri-	^t RAS			See Sp	peed Bin	Tables fo	r ^t RAS			ns	12
ACTIVATE-to-ACTIVATE of period	or REF command	^t RC			See S	peed Bin	Tables fo	or ^t RC			ns	12
ACTIVATE-to-ACTIVATE	•	^t RRD_S	MIN =	greater	MIN =	greater	MIN =	greater	MIN =	greater	CK	1
to different bank group size	s for 1/2KB page	(1/2KB)	of 4CK	or 5ns	of 4CK	or 4.2ns	of 4CK	or 3.7ns	of 4CK	or 3.3ns		
ACTIVATE-to-ACTIVATE of to different bank group size	•	^t RRD_S (1KB)		greater Cor 5ns		greater or 4.2ns	1	greater or 3.7ns		greater or 3.3ns	CK	1

		DDR4	I-1600	DDR4	I-1866	DDR4	l-2133	DDR4	1-2400		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
ACTIVATE-to-ACTIVATE command period	tRRD_S	MIN =	greater	MIN =	greater	MIN =	greater	MIN =	greater	CK	1
to different bank groups for 2KB page	(2KB)	of 4Ck	or 6ns	of 4CK	or 5.3ns	of 4CK	or 5.3ns	of 4CK	or 5.3ns		
size											
ACTIVATE-to-ACTIVATE command period	^t RRD_L	MIN =	greater	MIN =	greater	MIN =	greater	MIN =	greater	CK	1
to same bank groups for 1/2KB page size	(1/2KB)	of 4Ck	or 6ns	of 4CK	or 5.3ns	of 4CK	or 5.3ns	of 4CK	or 4.9ns		
ACTIVATE-to-ACTIVATE command period	tRRD_L	MIN =	greater	MIN =	greater	MIN =	greater	MIN =	greater	CK	1
to same bank groups for 1KB page size	(1KB)	of 4Ck	or 6ns	of 4CK	or 5.3ns	of 4CK	or 5.3ns	of 4CK	or 4.9ns		
ACTIVATE-to-ACTIVATE command period	^t RRD_L	MIN =	greater	MIN =	greater	MIN =	greater	MIN =	greater	CK	1
to same bank groups for 2KB page size	(2KB)	of 4CK	or 7.5ns	of 4CK	or 6.4ns	of 4CK	or 6.4ns	of 4CK	or 6.4ns		
Four ACTIVATE windows for 1/2KB page	^t FAW	MIN =	greater	MIN =	greater	MIN =	greater	MIN =	greater	ns	
size	(1/2KB)	of 16CK	or 20ns	of 16Ck	or 17ns	of 16Ck	or 15ns	of 16Ck	C or 13ns		
Four ACTIVATE windows for 1KB page	^t FAW	MIN =	greater	MIN =	greater	MIN =	greater	MIN =	greater	ns	
size	(1KB)	of 20CK	or 25ns	of 20Ck	or 23ns	of 20Ck	or 21ns	of 20Ck	or 21ns		
Four ACTIVATE windows for 2KB page	^t FAW	MIN =	greater	MIN =	greater	MIN =	greater	MIN =	greater	ns	
size	(2KB)	of 28Ck	or 35ns	of 28Ck	or 30ns	of 28Ck	or 30ns	of 28Ck	C or 30ns		
WRITE recovery time	^t WR _{1ck}				MIN :	= 15ns				ns	1, 5, 9
	^t WR _{2ck}			I	MIN = 1C	K + ^t WR ₁	ck			CK	1, 5, 10
WRITE recovery time when CRC and DM	tWR_CRC_DM _{1c}	MIN = t	WR _{1ck} +	MI	$N = {}^{t}WR_{1}$	_{ck} + grea	ter of (50	K or 3.7	5ns)	CK	1, 6, 9
are both enabled	k	greater	of (4CK								
		or 3.	.75ns)								
	^t WR_CRC_DM _{2c}			MIN :	= 1CK + ^t \	WR_CRC_	DM _{1ck}			CK	1, 6, 10
	k										
Delay from start of internal WRITE trans-	tWTR_L _{1ck}			MIN =	greater	of 4CK o	r 7.5ns			CK	1, 5, 9
action to internal READ command – Same	tWTR_L _{2ck}			М	IN = 1CK	+ tWTR_I	-1ck			CK	1, 5, 10
bank group											
Delay from start of internal WRITE trans-	tWTR_L_CRC_D		N =	MIN	= tWTR_	L _{1ck} + gre	eater of (5CK or 3.	.75ns)	CK	1, 6, 9
action to internal READ command – Same	M _{1ck}		_L _{1ck} +								
bank group when CRC and DM are both		-	of (4CK								
enabled		or 3.	75ns)								
	tWTR_L_CRC_D			MIN =	1CK + ^t W	TR_L_CR	C_DM_{1ck}			CK	1, 6, 10
	M _{2ck}										

Parameter Delay from start of internal WRITE transaction to internal READ command – Different bank group Twtr_S_2ck Delay from start of internal WRITE transaction to internal READ command – Different bank group Twtr_S_2ck MIN = 1CK + twtr_S_1ck — CK MIN = 1CK + twtr_S_1ck + greater of (5CK or 3.75ns) Twtr_S_CRC_D MIN = twtr_S_1ck + greater of (5CK or 3.75ns) CK MIN = 1CK + twtr_S_1ck + greater of (5CK or 3.75ns) Twtr_S_1ck + greater of (4CK or 3.75ns) Twtr_S_CRC_D Mode Twtr_S_CRC_D Twtr	1, 5, 7, 8, 9 1, 5, 7, 8, 10 1, 6, 7, 8, 9
action to internal READ command – Different bank group twtr_S _{2ck} MIN = 1CK + twtr_S _{1ck} CK Delay from start of internal WRITE transaction to internal READ command – Different bank group when CRC and DM are both enabled twtr_S_CRC_D MIN = twtr_S _{1ck} + greater of (5CK or 3.75ns) CK MIN = twtr_S _{1ck} + greater of (5CK or 3.75ns) WTR_S _{1ck} + greater of (4CK or 3.75ns) Twtr_S_CRC_D M _{2ck} MIN = 1CK + twtr_S _{1ck} + Greater of (5CK or 3.75ns) CK MIN = twtr_S _{1ck} + Greater of (5CK or 3.75ns) CK MIN = twtr_S _{1ck} + Greater of (5CK or 3.75ns) CK MIN = 1CK + twtr_S _{1ck} + Greater of (5CK or 3.75ns)	8, 9 1, 5, 7, 8, 10 1, 6, 7, 8, 9
ferent bank group	1, 5, 7, 8, 10 1, 6, 7, 8, 9
Delay from start of internal WRITE transaction to internal READ command – Different bank group when CRC and DM are both enabled $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	8, 10 1, 6, 7, 8, 9
action to internal READ command – Different bank group when CRC and DM are both enabled	8, 9
M _{2ck}	
READ-to-PRECHARGE time tRTP MIN = greater of 4CK or 7.5 ps	1, 6, 7, 8, 10
INTERPRETARISE UNITE INTERPRETARISE UNITE	1
CAS_n-to-CAS_n command delay to dif- t CCD_S 4 - 4 - 4 - CK ferent bank group	,
CAS_n-to-CAS_n command delay to same bank group tCCD_L MIN =	14
Auto precharge write recovery + pre- charge time	8
MRS Command Timing	·
MRS command cycle time	
MRS command cycle time in PDA mode ^t MRD_PDA MIN = greater of (16nCK, 10ns) CK	1
MRS command cycle time in CAL mode	
MRS command update delay tMOD MIN = greater of (24nCK, 15ns) CK	1
MRS command update delay in PDA tMOD_PDA MIN = tMOD CK mode	,
MRS command update delay in CAL tMOD_CAL MIN = tMOD + tCAL CK mode	
MRS command to DQS drive in preamble training tr	
MPR Command Timing	
Multipurpose register recovery time ^t MPRR MIN = 1CK CK	<u></u>
Multipurpose register write recovery time	

		DDR4	l-1600	DDR4	l-1866	DDR4	l-2133	DDR4	1-2400		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
	(CRC Erro	r Repor	ting Tim	ing						'
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	^t CRC_ALERT_P W	6	10	6	10	6	10	6	10	СК	
		CA	Parity T	iming	1		-	-		1	1
Parity latency	PL	4	_	4	_	4	_	5	_	CK	
Commands uncertain to be executed during this time	^t PAR_UN- KNOWN	-	PL	_	PL	-	PL	_	PL	CK	
Delay from errant command to ALERT_n assertion	^t PAR_ALERT_O N	_	PL + 6ns	_	P L + 6ns	_	PL + 6ns	_	PL + 6ns	CK	
Pulse width of ALERT_n signal when asserted	^t PAR_ALERT_P W	48	96	56	112	64	128	72	144	CK	
Time from alert asserted until DES commands required in persistent CA parity mode	^t PAR_ALERT_RS P	-	43	-	50	-	57	-	64	CK	
			CAL Tim	ing			,				
CS_n to command address latency	^t CAL	3	_	4	_	4	_	5	_	CK	19
CS_n to command address latency in gear-down mode	^t CALg	N/A	_	N/A	_	N/A	_	N/A	_	CK	
		IV	IPSM Tir	ning							
Command path disable delay upopn MPSM entry	^t MPED			MIN = ^t N	MOD (MIN	N) + ^t CPD	ED (MIN))		CK	1
Valid clock requirement after MPSM entry	^t CKMPE			MIN = ^t N	MOD (MIN	N) + ^t CPD	ED (MIN))		CK	1
Valid clock requirement before MPSM exit	^t CKMPX	MIN = ^t CKSRX (MIN)									1
Exit MPSM to commands not requiring a locked DLL	^t XMP	^t XS (MIN)									
Exit MPSM to commands requiring a locked DLL	^t XMPDLL			MIN = t	XMP (MIN	N) + ^t XSD	LL (MIN)			CK	1
CS setup time to CKE	^t MPX_S			MIN	= tIS (MI	N) + ^t IH (MIN)			ns	
CS_n HIGH hold time to CKE rising edge	^t MPX_HH				MIN	= ^t XP				ns	

						DDR4	I-2133	DDR4	-2400			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
CS_n LOW hold time to	CKE rising edge	^t MPX_LH	12	^t XMP-1 0ns	12	^t XMP-1 0ns	12	tXMP-1 0ns	12	^t XMP-1 0ns	ns	
			Conne	ctivity Te	st Timir	ng						
TEN pin HIGH to CS_n L mode	OW – Enter CT	^t CT_Enable	200	_	200	_	200	_	200	_	ns	
CS_n LOW and valid inp	out to valid output	^t CT_Valid	_	200	_	200	_	200	_	200	ns	
CK_t, CK_c valid and CK goes HIGH	E HIGH after TEN	^t CTCKE_Valid	10	_	10	_	10	_	10	-	ns	
Calibration and V _{REFDQ} Train Timing												
ZQCL command: Long calibration time	POWER-UP and RESET operation	^t ZQinit								CK		
	Normal opera- tion	^t ZQoper	512	_	512	_	512	_	512	_	CK	
ZQCS command: Short of	alibration time	^t ZQCS	128	_	128	_	128	_	128	_	CK	
The V _{REF} increment/dec	rement step time	V_{REF_time}				MIN =	150ns					
Enter V_{REFDQ} training m write or V_{REFDQ} MRS con		^t VREFDQE				MIN =	150ns				ns	1
Exit V _{REFDQ} training mod WRITE command delay	de to the first	^t VREFDQX				MIN =	150ns				ns	1
		Initiali	zation a	nd Rese	t Timing)						
Exit reset from CKE HIG mand	H to a valid com-	^t XPR		MIN	l = great	er of 5CK	or ^t RFC	(MIN) + 1	0ns		CK	1
RESET_L pulse low after	power stable	tPW_RESET_S	_5						μs			
RESET_L pulse low at po	^t PW_RESET_L	200	_	200	_	200	_	200	_	μs		
Begin power supply ran plies stable	np to power sup-	^t VDDPR			М	IN = N/A;	MAX = 2	200			ms	
RESET_n LOW to power	supplies stable	^t RPS				MIN = 0;	MAX = ()			ns	
			Re	fresh Ti	ming							

			DDR4	l-1600	DDR4	-1866	DDR4	l-2133	DDR4	1-2400		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
REFRESH-to-ACTIVATE		^t RFC1				MIN	= 260				ns	1, 11
or REFRESH command	4Gb	^t RFC2				MIN	= 160				ns	1, 11
period (all bank		^t RFC4				MIN	= 110				ns	1, 11
groups)		^t RFC1				MIN	= 350				ns	1, 11
	8Gb	^t RFC2				MIN	= 260				ns	1, 11
		^t RFC4				MIN	= 160				ns	1, 11
		^t RFC1				MIN	= 350				ns	1, 11
	16Gb	^t RFC2				MIN	= 260				ns	1, 11
		^t RFC4	MIN = 160									1, 11
Average periodic re-	-40°C ≤ T _C ≤ 85°C	^t REFI	MIN = N/A; MAX = 7.8									11
fresh interval	85°C < T _C ≤ 95°C	^t REFI	MIN = N/A; MAX = 3.9									11
	95°C < T _C ≤ 105°C	^t REFI	MIN = N/A; MAX = 1.95									11
			Self	Refresh	Timing						1	1
Exit self refresh to com	mands not requir-											
ing a locked DLL		^t XS				$MIN = {}^{t}R$	FC + 10n	S			ns	1
Exit self refresh to coming a locked DLL in self	•	^t XS_ABORT			I	MIN = ^t RF	C4 + 10r	ıs			ns	1
Exit self refresh to ZQCI (CL, CWL, WR, RTP and	, ,	^t XS_FAST			I	MIN = ^t RF	C4 + 10r	ıs			ns	1
Exit self refresh to comi	_	^t XSDLL				MIN = ^t D	LLK (MIN)			СК	1
Minimum CKE low pulse fresh entry to self refree		^t CKESR			MIN	l = ^t CKE ((MIN) + 1	nCK			CK	1
Minimum CKE low pulse fresh entry to self refree when CA parity is enab	sh exit timing	^t CKESR_PAR	R MIN = ${}^{t}CKE$ (MIN) + 1 nCK + PL							CK	1	
Valid clocks after self re or power-down entry (F		^t CKSRE			MIN :	= greater	of (5CK,	10ns)			CK	1
Valid clock requirement entry or power-down w enabled		^t CKSRE_PAR	R MIN = greater of (5CK, 10ns) + PL								CK	1



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Table 163: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400 (Continued)

		DDR4	4-1600	DDR4	1-1866	DDR	4-2133	DDR	4-2400		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Valid clocks before self refresh exit (SRX) or power-down exit (PDX), or reset exit	^t CKSRX			MIN :	= greater	of (5CK,	, 10ns)			CK	1
		Powe	er-Down	Timing							
Exit power-down with DLL on to any valid command	^t XP			MIN	= greater	of 4CK	or 6ns			СК	1
Exit power-down with DLL on to any valid command when CA Parity is enabled.	^t XP _PAR			MIN = (ç	greater o	f 4CK or	6ns) + PL			CK	1
CKE MIN pulse width	^t CKE (MIN)			MIN	= greater	r of 3CK	or 5ns			CK	1
Command pass disable delay	^t CPDED	4	_	4	_	4	_	4	_	CK	
Power-down entry to power-down exit timing	^t PD			-	CK						
Begin power-down period prior to CKE registered HIGH	^t ANPD				CK						
Power-down entry period: ODT either synchronous or asynchronous	PDE	Great	er of ^t AN	NPD or ^t R	V time	CK					
Power-down exit period: ODT either syn- chronous or asynchronous	PDX					CK					
	Powe	r-Down	Entry N	/linimum	Timing						
ACTIVATE command to power-down entry	^t ACTPDEN	1	_	1	_	2	_	2	_	СК	
PRECHARGE/PRECHARGE ALL command to power-down entry	^t PRPDEN	1	-	1	-	2	_	2	-	CK	
REFRESH command to power-down entry	^t REFPDEN	1	_	1	_	2	_	2	_	CK	
MRS command to power-down entry	^t MRSPDEN				MIN = ^t M	IOD (MIN	1)			CK	1
READ/READ with auto precharge command to power-down entry	^t RDPDEN				CK	1					
WRITE command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN				CK	1					
WRITE command to power-down entry (BC4MRS)	^t WRPBC4DEN				CK	1					
WRITE with auto precharge command to power-down entry (BL8OTF, BL8MRS,BC4OTF)	^t WRAPDEN				CK	1					



8Gb: x4, x8, x16 DDR4 SDRAM AC Electrical Characteristics and AC Timing Parameters

		DDR4	-1600	DDR4	-1866	DDR4	-2133	DDR4	l-2400		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
WRITE with auto precharge command to power-down entry (BC4MRS)	^t WRAPBC4DEN			MI	N = WL +	2 + WR	+ 1			CK	1
		(ODT Tim	ing							
Direct ODT turn-on latency	DODTLon			WL	- 2 = CWL	. + AL + P	L - 2			CK	
Direct ODT turn-off latency	DODTLoff			WL	- 2 = CWL	_+ AL + P	²L - 2			CK	
R _{TT} dynamic change skew	^t ADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	CK	
Asynchronous R _{TT(NOM)} turn-on delay (DLL off)	^t AONAS	1	9	1	9	1	9	1	9	ns	
Asynchronous R _{TT(NOM)} turn-off delay (DLL off)	^t AOFAS	1	9	1	9	1	9	1	9	ns	
ODT HIGH time with WRITE command	ODTH8 1 ^t CK	6	_	6	-	6	_	6	_	CK	
and BL8	ODTH8 2 ^t CK	N	Α	N	İΑ	N	İΑ	7	-	1	
ODT HIGH time without WRITE command	ODTH4 1 ^t CK	4	_	4	_	4	_	4	_	CK	
or with WRITE command and BC4	ODTH4 2 ^t CK	NA		N	İΑ	N	İΑ	5	_		
		Write	Leveling	g Timing	j						
First DQS_t, DQS_c rising edge after write leveling mode is programmed	^t WLMRD	40	_	40	_	40	_	40	_	CK	
DQS_t, DQS_c delay after write leveling mode is programmed	^t WLDQSEN	25	-	25	-	25	-	25	-	CK	
Write leveling setup from rising CK_t, CK_c crossing to rising DQS_t, DQS_c crossing	^t WLS	0.13	-	0.13	-	0.13	-	0.13	-	^t CK (AVG)	
Write leveling hold from rising DQS_t, DQS_c crossing to rising CK_t, CK_c crossing	^t WLH	0.13	-	0.13	-	0.13	-	0.13	-	^t CK (AVG)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns	
Gear-Down Timing (Not Supported Below DDR4-2666)											
Exit reset from CKE HIGH to a valid MRS gear-down	^t XPR_GEAR	N/	/A	N	/A	N	/A	N	/A	CK	
CKE HIGH assert to gear-down enable time)	^t XS_GEAR	N/	/A	N.	/A	N.	/A	N/	/A	CK	
MRS command to sync pulse time	tSYNC_GEAR	N/	/A	N.	/A	N.	/A	N.	/A	CK	

		DDR4-1600		DDR4	-1866	DDR4	-2133	DDR4	-2400		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Sync pulse to first valid command	tCMD_GEAR	N/A		N.	/A	N.	/A	N.	/A	CK	
Gear-down setup time	tGEAR_setup	N/A	_	N/A	_	N/A	_	N/A	_	CK	
Gear-down hold time	^t GEAR_hold	N/A	_	N/A	_	N/A	_	N/A	_	CK	



Notes:

- Maximum limit not applicable.
- 2. Micron tDLLK values support the legacy JEDEC tDLLK specifications.
- DDR4-1600 AC timing parameters apply if DRAM operates at lower than 1600 MT/s data rate.
- 4. Data rate is greater than or equal to 1066 Mb/s.
- 5. WRITE-to-READ when CRC and DM are both not enabled.
- 6. WRITE-to-READ delay when CRC and DM are both enabled.
- 7. The start of internal write transactions is defined as follows:
 - For BL8 (fixed by MRS and on-the-fly): rising clock edge four clock cycles after WL
 - For BC4 (on-the-fly): rising clock edge four clock cycles after WL
 - For BC4 (fixed by MRS): rising clock edge two clock cycles after WL
- 8. For these parameters, the device supports ^tnPARAM [nCK] = ROUND{^tPARAM [ns]/^tCK (AVG) [ns]} according to the rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section, in clock cycles, assuming all input clock jitter specifications are satisfied.
- 9. When operating in 1^tCK WRITE preamble mode.
- 10. When operating in 2^tCK WRITE preamble mode.
- 11. When CA parity mode is selected and the DLLoff mode is used, each REF command requires an additional "PL" added to [†]RFC refresh time.
- 12. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime and/or reduction in data retention ability.
- 13. Applicable from [†]CK (AVG) MIN to [†]CK (AVG) MAX as stated in the Speed Bin tables.
- 14. JEDEC specifies a minimum of five clocks.
- 15. The maximum read postamble is bound by ^tDQSCK (MIN) plus ^tQSH (MIN) on the left side and ^tHZ(DQS) MAX on the right side.
- 16. The reference level of DQ output signal is specified with a midpoint as a widest part of output signal eye, which should be approximately $0.7 \times V_{DDQ}$ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to $V_{TT} = V_{DDQ}$.
- 17. JEDEC hasn't agreed upon the definition of the deterministic jitter; the user should focus on meeting the total limit.
- 18. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of ^tCK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below ^tCK (AVG) MIN.
- 19. The actual ^tCAL minimum is the larger of 3 clocks or 3.748ns/^tCK; the table lists the applicable clocks required at targeted speed bin.
- 20. The maximum READ preamble is bounded by ^tLZ(DQS) MIN on the left side and ^tDQSCK (MAX) on the right side. See figure in the Clock to Data Strobe Relationship section. Boundary of DQS Low-Z occurs one cycle earlier in 2^tCK toggle mode, as illustrated in the READ Preamble section.
- 21. DQ falling signal middle-point of transferring from HIGH to LOW to first rising edge of DQS differential signal cross-point.
- 22. The ^tPDA_S/^tPDA_H parameters may use the ^tDS/^tDH limits, respectively, if the signal is LOW the entire BL8.

Electrical Characteristics and AC Timing Parameters: 2666 Through 3200

			DDR4	l-2666	DDR4	-2933	DDR4	-3200	Rese	erved		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
			C	lock Tin	ning							
Clock period average	(DLL off mode)	^t CK (AVG, DLL_OFF)	8	20	8	20	8	20			ns	
Clock period average		^t CK (AVG, DLL_ON)	0.75	1.9	0.682	1.9	0.625	1.9			ns	3, 13
High pulse width aver	age	^t CH (AVG)	0.48	0.52	0.48	0.52	0.48	0.52			^t CK (AVG)	
Low pulse width average		^t CL (AVG)	0.48	0.52	0.48	0.52	0.48	0.52			^t CK (AVG)	
Clock period jitter	Total	^t JITper_tot	-38	38	-34	34	-32	32			ps	17 , 18
	Deterministic	^t JITper_dj	-19	19	-17	17	-16	16			ps	17
	DLL locking	^t JITper,lck	-30	30	-27	27	-25	25			ps	
Clock absolute period		^t CK (ABS)	MIN =	tCK (AV	G) MIN +	. •	ot MIN; N	MAX = ^t C	K (AVG)	MAX +	ps	
Clock absolute high policy (includes duty cycle jit		^t CH (ABS)	0.45	_	0.45	-	0.45	-			^t CK (AVG)	
Clock absolute low pu (includes duty cycle jit		^t CL (ABS)	0.45	_	0.45	-	0.45	-			^t CK (AVG)	
Cycle-to-cycle jitter	Total	^t JITcc _tot	_	75	-	68	_	62			ps	
	DLL locking	^t JITcc,lck	-	60	-	55	_	62			ps	



			DDR4	I-2666	DDR4	-2933	DDR4	-3200	Rese	erved		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Cumulative error across	2 cycles	^t ERR2per	-55	55	-50	50	-46	46			ps	
	3 cycles	^t ERR3per	-66	66	-60	60	-55	55			ps	
	4 cycles	^t ERR4per	-73	73	-66	66	-61	61			ps	
	5 cycles	^t ERR5per	-78	78	-71	71	-65	65			ps	
	6 cycles	^t ERR6per	-83	83	-75	75	-69	69			ps	
	7 cycles	^t ERR7per	-87	87	-79	79	-73	73			ps	
	8 cycles	^t ERR8per	-91	91	-83	83	-76	76			ps	
	9 cycles	^t ERR9per	-94	94	-85	85	-78	78			ps	
	10 cycles	tERR10per	-96	96	-88	88	-80	80			ps	
	11 cycles	^t ERR11per								ps		
	12 cycles	^t ERR12per									ps	
	n = 13, 14 49,	^t ERR <i>n</i> per		tERR <i>n</i>	'	ps						
	50 cycles			^t ERR <i>n</i> p								
			DQ	Input T	iming							
Data setup time to DQS_t, DQS_c	Base (calibrated V _{REF})	^t DS				put Recei mately 0.	•				-	
	Non-calibrated V _{REF}	^t PDA_S				minimun	n of 0.5u	i			UI	22
Data hold time from DQS_t, DQS_c	Base (calibrated V _{REF})	^t DH				put Recei mately 0.					-	
	Non-calibrated V _{REF}	^t PDA_H				minimun	n of 0.5U	I			UI	22
DQ and DM minimum d for each input		^t DIPW	0.58	_	0.58	_	0.58	_			UI	
		DQ	OQ Output Timing (DLL enabled)									
DQS_t, DQS_c to DQ ske	ew, per group, per	^t DQSQ	-	0.18	_	0.19	_	0.20			UI	
DQ output hold time from	om DQS_t, DQS_c	^t QH	0.74	_	0.72	_	0.70	_			UI	
Data Valid Window per device: ^t QH - ^t DVW _d DQSQ each device's output per UI			0.64	-	0.64	-	0.64	-			UI	
·	ata Valid Window per device, per pin: H - ^t DQSQ each device's output per UI		0.72	-	0.72	-	0.72	-			UI	

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Table 164: Electrical Characteristics and AC Timing Parameters (Continued)

		DDR4	-2666	DDR4	-2933	DDR4	-3200	Rese	rved		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
DQ Low-Z time from CK_t, CK_c	^t LZDQ	-310	170	-280	165	-250	160			ps	
DQ High-Z time from CK_t, CK_c	^t HZDQ	_	170	_	165	_	160			ps	
		DQ Str	obe Inp	ut Timin	g						
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 1 ^t CK preamble	^t DQSS _{1ck}	-0.27	0.27	-0.27	0.27	-0.27	0.27			CK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 2 ^t CK preamble	^t DQSS _{2ck}	-0.50	0.50	-0.50	0.50	-0.50	0.50			CK	
DQS_t, DQS_c differential input low pulse width	^t DQSL	0.46	0.54	0.46	0.54	0.46	0.54			CK	
DQS_t, DQS_c differential input high pulse width	^t DQSH	0.46	0.54	0.46	0.54	0.46	0.54			CK	
DQS_t, DQS_c differential input high pulse width for 2 ^t CK preamble	^t DQSH2PRE	1.46	-	1.46	-	1.46	-			CK	
DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge for 1 ^t CK preamble	^t DSS _{1ck}	0.18	_	0.18	-	0.18	_			CK	
DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge for 2 ^t CK preamble	^t DSS _{2ck}	0	_	0	-	0	_			CK	
DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge for 1 ^t CK preamble	^t DSH _{1ck}	0.18	_	0.18	-	0.18	-			CK	
DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge for 2 ^t CK preamble	^t DSH _{2ck}	0	_	0	-	0	_			CK	
DQS_t, DQS_c differential WRITE preamble for 1 ^t CK preamble	^t WPRE _{1ck}	0.9	_	0.9	-	0.9	_			CK	
DQS_t, DQS_c differential WRITE preamble for 2 ^t CK preamble	^t WPRE _{2ck}	1.8	-	1.8	-	1.8	-			CK	
DQS_t, DQS_c differential WRITE postamble	^t WPST	0.33	-	0.33	-	0.33	-			CK	
	DQS St	robe Out	tput Tim	ing (DLI	enable	d)	'				
DQS_t, DQS_c rising edge output access time from rising CK_t, CK_c	^t DQSCK	-170	170	-165	165	-160	160			ps	
DQS_t, DQS_c rising edge output variance window per DRAM	^t DQSCKi	-	270	_	265	_	260			ps	
DQS_t, DQS_c differential output high time	^t QSH	0.40	_	0.40	_	0.40	_			CK	



8Gb: x4, x8, x16 DDR4 SDRAM Electrical Characteristics and AC Timing Parameters: 2666 Through 3200

			DDR4	-2666	DDR4	-2933	DDR4	-3200	Rese	rved		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
DQS_t, DQS_c differenti time	al output low	^t QSL	0.40	_	0.40	-	0.40	-			CK	
DQS_t, DQS_c Low-Z tim	ne (RL - 1)	^t LZDQS	-310	170	-280	165	-250	160			ps	
DQS_t, DQS_c High-Z tir	ne (RL + BL/2)	^t HZDQS	_	170	_	165	_	160			ps	
DQS_t, DQS_c differenti ble for 1 ^t CK preamble	al READ pream-	^t RPRE _{1ck}	0.9	_	0.9	_	0.9	_			CK	20
DQS_t, DQS_c differenti ble for 2 ^t CK preamble	al READ pream-	^t RPRE _{2ck}	1.8	_	1.8	-	1.8	-			CK	20
DQS_t, DQS_c differenti ble	al READ postam-	^t RPST	0.33	_	0.33	-	0.33	_			CK	21
		C	Command and Address Timing									
DLL locking time		^t DLLK	854 - 940 - 1024 -					CK	2, 4			
	Base	^t IS	55	_	48	_	40	_			ps	
to CK_t, CK_c referenced to V _{IH(AC)} and _{VIL(AC)} levels	V _{REFCA}	^t IS _{VREF}	145	_	138	_	130	_			ps	
CMD, ADDR hold time	Base	^t IH	80	_	73	-	65	_			ps	
to CK_t, CK_c referenced to V _{IH(DC)} and V _{IL(DC)} levels	V _{REFCA}	^t IH _{VREF}	145	_	138	_	130	_			ps	
CTRL, ADDR pulse width	for each input	^t IPW	385	-	365	_	340	_			ps	
ACTIVATE to internal RE	AD or WRITE de-	^t RCD			See Sp	peed Bin	Tables fo	r ^t RCD			ns	
PRECHARGE command	period	^t RP			See S	peed Bin	Tables fo	or ^t RP			ns	
ACTIVATE-to-PRECHARG	E command peri-	^t RAS			See Sp	oeed Bin	Tables fo	r ^t RAS			ns	12
ACTIVATE-to-ACTIVATE period	or REF command	^t RC	See Speed Bin Tables for ^t RC							ns	12	
ACTIVATE-to-ACTIVATE to different bank group size	s for 1/2KB page	^t RRD_S (1/2KB)	of 4CK or 3.0ns of 4CK or 2.7ns of 4CK or 2.5ns						CK	1		
ACTIVATE-to-ACTIVATE to different bank group size		^t RRD_S (1KB)		greater or 3.0ns		greater or 2.7ns		greater or 2.5ns			CK	1

		DDR4	-2666	DDR4	I-2933	DDR4	1-3200	Rese	rved		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
ACTIVATE-to-ACTIVATE command period	tRRD_S	MIN =	greater	MIN =	greater		greater			CK	1
to different bank groups for 2KB page	(2KB)	of 4CK	or 5.3ns	of 4CK	or 5.3ns	of 4CK	or 5.3ns				
size											
ACTIVATE-to-ACTIVATE command period	^t RRD_L		greater	1	greater	1	greater			CK	1
to same bank groups for 1/2KB page size	(1/2KB)	of 4CK	or 4.9ns	of 4CK	or 4.9ns	of 4CK	or 4.9ns				
ACTIVATE-to-ACTIVATE command period	tRRD_L		greater	1	greater		greater			CK	1
to same bank groups for 1KB page size	(1KB)	of 4CK	or 4.9ns	of 4CK	or 4.9ns	of 4CK	or 4.9ns				
ACTIVATE-to-ACTIVATE command period	^t RRD_L		greater	1	greater		greater			CK	1
to same bank groups for 2KB page size	(2KB)	of 4CK	or 6.4ns	of 4CK	or 6.4ns	of 4CK	or 6.4ns				
Four ACTIVATE windows for 1/2KB page	^t FAW	MIN =	greater	1	greater	1	greater			ns	
size	(1/2KB)	of 16CK	or 12ns		CK or	of 16Ck	Cor 10ns				
				10.8	375ns						
Four ACTIVATE windows for 1KB page	^t FAW		greater	1	greater		greater			ns	
size	(1KB)	of 20CK	or 21ns	of 20CK	or 21ns	of 20Ck	C or 21ns				
Four ACTIVATE windows for 2KB page	^t FAW		greater	1	greater	1	greater			ns	
size	(2KB)	of 28CK	or 30ns	of 28CK	or 30ns	of 28Ck	Cor 30ns				
WRITE recovery time	^t WR _{1ck}				MIN =	= 15ns				ns	1, 5, 9
	tWR _{2ck}			1	MIN = 1CI	K + ^t WR ₁	ck			CK	1, 5, 10
WRITE recovery time when CRC and DM	tWR_CRC_DM _{1c}		MII	$N = {}^{t}WR_{1}$	_{ck} + grea	ter of (50	CK or 3.75	ins)		CK	1, 6, 9
are both enabled	k										
WRITE recovery time when CRC and DM	tWR_CRC_DM _{2c}			MIN =	= 1CK + ^t \	NR_CRC_	DM _{1ck}			CK	1, 6, 10
are both enabled	k										
Delay from start of internal WRITE trans-	tWTR_L _{1ck}			MIN =	greater	of 4CK o	r 7.5ns			CK	1, 5, 9
action to internal READ command – Same	tWTR_L _{2ck}			M	IN = 1CK	+ tWTR_	L_{1ck}			CK	1, 5, 10
bank group	*			t							
Delay from start of internal WRITE trans-	tWTR_L_CRC_D		MIN	= 'WTR_	L _{1ck} + gre	eater of (5CK or 3.	/5ns)		CK	1, 6, 9
action to internal READ command – Same bank group when CRC and DM are both	M _{1ck}										
enabled	tWTR_L_CRC_D			MIN =	1CK + ^t W	TR_L_CR	C_DM _{1ck}			CK	1, 6, 10
	M _{2ck}										
Delay from start of internal WRITE trans-	^t WTR_S _{1ck}			MIN =	greater o	of (2CK o	r 2.5ns)			CK	1, 5, 7,
action to internal READ command – Dif-	*					4	_				8, 9
ferent bank group	^t WTR_S _{2ck}			М	IN = 1CK	+ 'WTR_	S _{1ck}			CK	1, 5, 7,
											8, 10

					DDR4	-3200	Rese	rved			
Parameter	Symbol	Min	Мах	Min	Max	Min	Max	Min	Max	Unit	Notes
Delay from start of internal WRITE trans-	tWTR_S_CRC_D		MIN	= tWTR_S	i _{1ck} + gre	ater of (CK or 3.	75ns)		CK	1, 6, 7,
action to internal READ command – Dif-	M _{1ck}										8, 9
ferent bank group when CRC and DM are	tWTR_S_CRC_D			MIN = 1	CK + tW	TR_S_CRO	C_DM _{1ck}			CK	1, 6, 7,
both enabled	M _{2ck}										8, 10
READ-to-PRECHARGE time	^t RTP			MIN =	greater	of 4CK o	r 7.5ns			CK	1
CAS_n-to-CAS_n command delay to dif-	tCCD_S	4	-	4	_	4	_			CK	
ferent bank group											
CAS_n-to-CAS_n command delay to same	tCCD_L	MIN =	_	MIN =	_	MIN =	_			CK	14
bank group		greater		greater		greater					
		of 4CK		of 4CK		of 4CK					
		or 5ns		or 5ns		or 5ns					
Auto precharge write recovery + pre- charge time	^t DAL (MIN)	· · ·								CK	8
		MRS C	omman	d Timing	j						
MRS command cycle time	^t MRD	8	_	8	_	8	_			CK	
MRS command cycle time in PDA mode	^t MRD_PDA			MIN =	greater o	of (16nCK	(, 10ns)				1
MRS command cycle time in CAL mode	tMRD_CAL			Λ	/IIN = ^t M	OD + ^t CA	L			CK	
MRS command update delay	^t MOD			MIN =	greater o	of (24nCk	(, 15ns)			CK	1
MRS command update delay in PDA	tMOD_PDA				MIN =	tMOD				CK	
mode											
MRS command update delay in CAL	tMOD_CAL			N	/IIN = ^t M	OD + ^t CA	L			CK	
mode											
MRS command to DQS drive in preamble	^t SDO			ı	$MIN = {}^{t}N$	IOD + 9n:	S				
training											
		MPR C	omman	d Timing	<u> </u>						
Multipurpose register recovery time	^t MPRR				MIN =	1nCK				CK	
Multipurpose register write recovery time	^t WR_MPR	$MIN = {}^{t}MOD + AL + PL$									
		CRC Erro	r Repor	ting Tim	ing						
CRC error to ALERT_n latency	^t CRC_ALERT	3	13	3	13	3	13			ns	
CRC ALERT_n pulse width	^t CRC_ALERT_P W	6	10	6	10	6	10			CK	
		CA	Parity T	iming							
Parity latency	PL	5	_	6	_	6	_			CK	
•								-	-		



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Table 164: Electrical Characteristics and AC Timing Parameters (Continued)

	DDR4-2666 DDR4-2933 DDR4-3200 Rese			served							
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Commands uncertain to be executed during this time	^t PAR_UN- KNOWN	-	PL	-	PL	-	PL			CK	
Delay from errant command to ALERT_n assertion	^t PAR_ALERT_O N	-	PL + 6ns	_	PL + 6ns	-	PL + 6ns			CK	
Pulse width of ALERT_n signal when asserted	^t PAR_ALERT_P W	80	160	88	176	96	192			CK	
Time from alert asserted until DES commands required in persistent CA parity mode	^t PAR_ALERT_RS P	-	71	_	78	-	85			CK	
		(CAL Tim	ing					·	·	
CS_n to command address latency	^t CAL	5	_	6	_	6	_			CK	19
CS_n to command address latency in gear-down mode	^t CALg	6	-	8	-	8	_			CK	
		IV	IPSM Tin	ning							
Command path disable delay upopn MPSM entry	^t MPED			MIN = ^t N	IOD (MIN	N) + ^t CPD	ED (MIN)			CK	1
Valid clock requirement after MPSM entry	^t CKMPE			MIN = ^t N	IOD (MIN	N) + ^t CPD	ED (MIN)			CK	1
Valid clock requirement before MPSM exit	^t CKMPX			Ŋ	ЛIN = ^t CK	SRX (MII	۷)			CK	1
Exit MPSM to commands not requiring a locked DLL	^t XMP				^t XS (MIN)				CK	
Exit MPSM to commands requiring a locked DLL	^t XMPDLL			MIN = t	XMP (MIN	N) + ^t XSD	LL (MIN)			CK	1
CS setup time to CKE	^t MPX_S			MIN	= tIS (MI	N) + ^t IH (MIN)			ns	
CS_n HIGH hold time to CKE rising edge	^t MPX_HH				MIN	= ^t XP				ns	
CS_n LOW hold time to CKE rising edge	^t MPX_LH	12 ^t XMP-1 12 ^t XMP-1 12 ^t XMP-1 0ns 0ns							ns		
		Connec	ctivity Te	st Timir	ng				'	'	
TEN pin HIGH to CS_n LOW – Enter CT mode	^t CT_Enable	200	_	200	_	200	_			ns	
CS_n LOW and valid input to valid output	^t CT_Valid	-	200	_	200	_	200			ns	



8Gb: x4, x8, x16 DDR4 SDRAM Electrical Characteristics and AC Timing Parameters: 2666 Through 3200

			DDR4	-2666	DDR4	-2933	DDR4	DDR4-3200		rved		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
CK_t, CK_c valid and CK	E HIGH after TEN	^t CTCKE_Valid	10	10 - 10 - 10 -							ns	
goes HIGH												
		Calik	oration a	and V _{REF}	_{DQ} Train	Timing						
ZQCL command: Long calibration time	POWER-UP and RESET operation	^t ZQinit	1024	_	1024	_	1024	_			CK	
	Normal opera- tion	^t ZQoper	512	_	512	-	512	_			CK	
ZQCS command: Short of	alibration time	^t ZQCS	128	_	128	_	128	_			CK	
The V _{REF} increment/dec	rement step time	V_{REF_time}				MIN =	150ns					
Enter V _{REFDQ} training m write or V _{REFDQ} MRS cor		^t VREFDQE				MIN =	150ns				ns	1
Exit V _{REFDQ} training mo WRITE command delay	raining mode to the first tVREFDQX MIN = 150ns hand delay						ns	1				
		Initiali	zation a	nd Rese	t Timing	J						
Exit reset from CKE HIG mand	H to a valid com-	o a valid com- ^t XPR MIN = greater of 5CK or ^t RFC (MIN) + 10ns			CK	1						
RESET_L pulse low after	power stable	^t PW_RESET_S	1.0	_	1.0	_	1.0	_			μs	
RESET_L pulse low at po	ower-up	^t PW_RESET_L	200	_	200	_	200	_			μs	
Begin power supply ran plies stable	np to power sup-	^t VDDPR	MIN = N/A; MAX = 200				,	ms				
RESET_n LOW to power	supplies stable	^t RPS	tRPS MIN = 0; MAX = 0					ns				
			Re	fresh Ti	ming							•
REFRESH-to-ACTIVATE		^t RFC1				MIN	= 260				ns	1, 11
or REFRESH command	4Gb	^t RFC2				MIN	= 160				ns	1, 11
period (all bank groups)		^t RFC4				MIN	= 110				ns	1, 11
groups)		^t RFC1	MIN = 350						ns	1, 11		
	8Gb	^t RFC2	MIN = 260							ns	1, 11	
		^t RFC4	MIN = 160							ns	1, 11	
		^t RFC1				MIN	= 350				ns	1, 11
	16Gb	^t RFC2				MIN	= 260				ns	1, 11
		^t RFC4				MIN	= 160				ns	1, 11

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			DDR4	4-2666	DDR4	-2933	3 DDR4-3200 Rese		rved			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Average periodic re-	-40°C ≤ T _C ≤ 85°C	^t REFI			М	IN = N/A;	MAX =	7.8			μs	11
fresh interval	85°C < T _C ≤ 95°C	^t REFI		MIN = N/A; MAX = 3.9							μs	11
	95°C < T _C ≤ 105°C	^t REFI			MI	N = N/A;	MAX = 1	1.95			μs	11
			Self	Refresh	Timing							
Exit self refresh to comring a locked DLL	nands not requir-	^t XS				MIN = ^t R	FC + 10n	S			ns	1
Exit self refresh to comring a locked DLL in self	•	tXS_ABORT				MIN = ^t RF	C4 + 10r	ns			ns	1
Exit self refresh to ZQCL (CL, CWL, WR, RTP and	, .	^t XS_FAST			N	MIN = ^t RF	C4 + 10r	าร			ns	1
Exit self refresh to comr locked DLL	elf refresh to commands requiring a ^t XSDLL			^t XSDLL MIN = ^t DLLK (MIN)					CK	1		
Minimum CKE low pulse fresh entry to self refres		^t CKESR	t CKESR MIN = t CKE (MIN) + 1 n CK					CK	1			
Minimum CKE low pulse fresh entry to self refres when CA parity is enabl	sh exit timing	^t CKESR_par			MIN =	tCKE (M	IN) + 1 <i>n</i> (CK + PL			CK	1
Valid clocks after self re or power-down entry (P		^t CKSRE			MIN =	= greater	of (5CK,	, 10ns)			CK	1
Valid clock requirement entry or power-down w enabled		^t CKSRE_par	SRE_par MIN = greater of (5CK, 10ns) + PL							CK	1	
Valid clocks before self or power-down exit (PD	` '	^t CKSRX			MIN =	= greater	of (5CK,	, 10ns)			CK	1
			Pow	er-Down	Timing							
Exit power-down with I id command	-	^t XP	MIN = greater of 4CK or 6ns					CK	1			
Exit precharge power-d- zen to commands not re DLL when CA Parity is e	equiring a locked	^t XP _PAR	MIN = (greater of 4CK or 6ns) + PL					CK	1			
CKE MIN pulse width		tCKE (MIN)			MIN :	= greater	of 3CK	or 5ns			CK	1
Command pass disable of	delay	^t CPDED	4	_	4	_	4	_			CK	



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Table 164: Electrical Characteristics and AC Timing Parameters (Continued)

	DDR4-2666 DDR4-2933 DDR4-3200 Reserved					erved					
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Power-down entry to power-down exit timing	^t PD		MIN = ^t CKE (MIN); MAX = 9 × ^t REFI								
Begin power-down period prior to CKE registered HIGH	^t ANPD				WL -	· 1CK				CK	
Power-down entry period: ODT either synchronous or asynchronous	PDE	Great	ter of ^t AN	NPD or ^t R	FC - REFR	ESH com	mand to	CKE LOV	V time	CK	
Power-down exit period: ODT either synchronous or asynchronous	PDX				^t ANPD +	+ ^t XSDLL				CK	
	Powe	r-Down	Entry N	linimum	Timing						
ACTIVATE command to power-down entry	^t ACTPDEN	2	_	2	_	2	_			CK	
PRECHARGE/PRECHARGE ALL command to power-down entry	^t PRPDEN	2	_	2	_	2	_			CK	
REFRESH command to power-down entry	^t REFPDEN	2	_	2	_	2	_			CK	
MRS command to power-down entry	^t MRSPDEN				MIN = ^t M	OD (MIN)			CK	1
READ/READ with auto precharge command to power-down entry	^t RDPDEN				MIN = R	L + 4 + 1				CK	1
WRITE command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	^t WRPDEN			MIN =	WL + 4 +	- ^t WR/ ^t CK	(AVG)			CK	1
WRITE command to power-down entry (BC4MRS)	^t WRPBC4DEN			MIN =	WL + 2 +	- ^t WR/ ^t CK	(AVG)			CK	1
WRITE with auto precharge command to power-down entry (BL8OTF, BL8MRS,BC4OTF)	tWRAPDEN	MIN = WL + 4 + WR + 1								CK	1
WRITE with auto precharge command to power-down entry (BC4MRS)	^t WRAPBC4DEN	MIN = WL + 2 + WR + 1								CK	1
		(ODT Tim	ing							
Direct ODT turn-on latency	DODTLon	WL - 2 = CWL + AL + PL - 2							CK		
Direct ODT turn-off latency	DODTLoff	WL - 2 = CWL + AL + PL - 2						CK			
R _{TT} dynamic change skew	^t ADC	0.28 0.72 0.26 0.74 0.26 0.74						CK			
Asynchronous R _{TT(NOM)} turn-on delay (DLL off)	^t AONAS	1	9	1	9	1	9			ns	



8Gb: x4, x8, x16 DDR4 SDRAM Electrical Characteristics and AC Timing Parameters: 2666 Through 3200

		DDR4	-2666	DDR4	-2933	DDR4-3200		Reserved			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Asynchronous R _{TT(NOM)} turn-off delay (DLL off)	^t AOFAS	1	9	1	9	1	9			ns	
ODT HIGH time with WRITE command	ODTH8 1 ^t CK	6	_	6	_	6	_			CK	
and BL8	ODTH8 2 ^t CK	7	_	7	_	7	_				
ODT HIGH time without WRITE command	ODTH4 1 ^t CK	4	_	4	_	4	_			CK	
or with WRITE command and BC4	ODTH4 2 ^t CK	5	_	5	_	5	_				
		Write	Levelin	g Timing	J						
First DQS_t, DQS_c rising edge after write leveling mode is programmed	^t WLMRD	40	_	40	-	40	_			CK	
DQS_t, DQS_c delay after write leveling mode is programmed	^t WLDQSEN	25	_	25	-	25	_			CK	
Write leveling setup from rising CK_t, CK_c crossing to rising DQS_t, DQS_c crossing	^t WLS	0.13	-	0.13	-	0.13	-			CK	
Write leveling hold from rising DQS_t, DQS_c crossing to rising CK_t, CK_c crossing	^t WLH	0.13	-	0.13	-	0.13	-			CK	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5			ns	
Write leveling output error	tWLOE	0	2	0	2	0	2			ns	
		Gea	r-Down	Timing							
Exit reset from CKE HIGH to a valid MRS gear-down	^t XPR_GEAR	^t X	PR	^t X	PR	^t X	PR			CK	
CKE HIGH assert to gear-down enable time)	^t XS_GEAR	t)	KS	t)	KS	t)	KS			CK	
MRS command to sync pulse time	tSYNC_GEAR	tMOD	+ 4CK	tMOD	+ 4CK	tMOD	+ 4CK			CK	
Sync pulse to first valid command	tCMD_GEAR	^t M	OD	^t M	OD	^t M	OD			CK	
Gear-down setup time	tGEAR_setup	2CK	_	2CK	_	2CK	_			CK	
Gear-down hold time	^t GEAR_hold	2CK	_	2CK	_	2CK	_			CK	





8Gb: x4, x8, x16 DDR4 SDRAM Converting Time-Based Specifications to Clock-Based Requirements

Notes:

- Maximum limit not applicable.
- 2. Micron tDLLK values support the legacy JEDEC tDLLK specifications.
- DDR4-1600 AC timing parameters apply if DRAM operates at lower than 1600 MT/s data rate.
- 4. Data rate is greater than or equal to 1066 Mb/s.
- 5. WRITE-to-READ when CRC and DM are both not enabled.
- 6. WRITE-to-READ delay when CRC and DM are both enabled.
- 7. The start of internal write transactions is defined as follows:
 - For BL8 (fixed by MRS and on-the-fly): rising clock edge four clock cycles after WL
 - For BC4 (on-the-fly): rising clock edge four clock cycles after WL
 - For BC4 (fixed by MRS): rising clock edge two clock cycles after WL
- 8. For these parameters, the device supports ^tnPARAM [nCK] = ROUND{^tPARAM [ns]/^tCK (AVG) [ns]} according to the rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section, in clock cycles, assuming all input clock jitter specifications are satisfied.
- 9. When operating in 1^tCK WRITE preamble mode.
- 10. When operating in 2^tCK WRITE preamble mode.
- 11. When CA parity mode is selected and the DLLoff mode is used, each REF command requires an additional "PL" added to ^tRFC refresh time.
- 12. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime and/or reduction in data retention ability.
- 13. Applicable from [†]CK (AVG) MIN to [†]CK (AVG) MAX as stated in the Speed Bin tables.
- 14. JEDEC specifies a minimum of five clocks.
- 15. The maximum read postamble is bound by ^tDQSCK (MIN) plus ^tQSH (MIN) on the left side and ^tHZ(DQS) MAX on the right side.
- 16. The reference level of DQ output signal is specified with a midpoint as a widest part of output signal eye, which should be approximately $0.7 \times V_{DDQ}$ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to $V_{TT} = V_{DDQ}$.
- 17. JEDEC hasn't agreed upon the definition of the deterministic jitter; the user should focus on meeting the total limit.
- 18. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of ^tCK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below ^tCK (AVG) MIN.
- 19. The actual ^tCAL minimum is the larger of 3 clocks or 3.748ns/^tCK; the table lists the applicable clocks required at targeted speed bin.
- 20. The maximum READ preamble is bounded by ^tLZ(DQS) MIN on the left side and ^tDQSCK (MAX) on the right side. See figure in the Clock to Data Strobe Relationship section. Boundary of DQS Low-Z occurs one cycle earlier in 2^tCK toggle mode, as illustrated in the READ Preamble section.
- 21. DQ falling signal middle-point of transferring from HIGH to LOW to first rising edge of DQS differential signal cross-point.
- 22. The ^tPDA_S/^tPDA_H parameters may use the ^tDS/^tDH limits, respectively, if the signal is LOW the entire BL8.

Converting Time-Based Specifications to Clock-Based Requirements

Software algorithms for calculation of timing parameters are subject to potential rounding errors when converting DRAM timing requirements to system clocks; for example, a



8Gb: x4, x8, x16 DDR4 SDRAM ୪ଓb: x4, x8, x16 DDR4 SDRAM Converting Time-Based Specifications to Clock-Based Requirements

memory clock with a nominal frequency of 933.33...3MHz which yields a clock period of 1.071428571429...ns. It is unrealistic to represent all digits after the decimal point exactly and some sort of rounding needs to be done.

DDR4 SDRAM SPD-based specifications use a minimum granularity for SPD-associated timing parameters of 1ps. Clock periods such as ^tCK (AVG) MIN are defined to the nearest picosecond. For example, 1.071428571429...ns is stated as 1071ps. Parameters such as tAA MIN are specified in units of time (nanoseconds) and require mathematical computation to convert to system clocks (nCK). Rules for rounding allow optimization of device performance without violating device parameters. These SPD algorithms rely on results that are within nCK adjustment factors on device testing and specification to avoid losing performance due to rounding errors when using SPD-based parameters. Note that JEDEC also defines an nCK adjustment factor, but mandates the inverse nCK adjustment factor be used in case of conflicting results, so only the inverse nCK adjustment factor is discussed here.

Guidance converting SPD associated timing parameters to system clock requirements:

- Round the application clock period up to the nearest picosecond.
- Express the timing specification and application clock period in picoseconds; scaling a nanosecond-based parameter value by 1000 allows programmers to use integer math instead of real math by expressing timing in ps.
- Divide the picosecond-based parameter by the picoseconds based application clock period.
- Add an inverse nCK adjustment factor of 97.4%.
- Truncate down to the next lower integer value.
- $nCK = Truncate[(parameter in ps)/(application {}^{t}CK in ps) + (974/1000)].$

Guidance converting nonSPD associated timing parameters to system clock requirements:

- Divide the time base specification (in ns) and divided by the clock period (in ns).
- The resultant is set to the next higher integer number of clocks.
- $nCK = Ceiling[(parameter in ns/application {}^{t}CK in ns)].$



Options Tables

Table 165: Options - Speed Based

		Data Rate							
Function	Acronym	1600	1866	2133	2400	2666	2933	3200	
Write leveling	WL	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Temperature controlled refresh	TCR	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Low-power auto self refresh	LPASR	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Fine granularity refresh	FGR	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Multipurpose register	MR	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Data mask	DM	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Data bus inversion	DBI	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
TDQS	_	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
ZQ calibration	ZQ CAL	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
V _{REFDQ} calibration	_	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Per-DRAM addressability	Per DRAM	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Mode register readout	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Command/Address latency	CAL	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Write CRC	CRC	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
CA parity	_	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Gear-down mode	-	No	No	No	No	Yes	Yes	Yes	
Programmable preamble	_	No	No	No	Yes	Yes	Yes	Yes	
Maximum power saving mode	MPSM	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Additive latency	AL	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Connectivity test mode	СТ	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Hard post package repair mode	hPPR	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Soft post package repair mode	sPPR	Yes	Yes	Yes	Yes	Yes	Yes	Yes	



Table 166: Options - Width Based

			Width					
Function	Acronym	х4	х8	x16				
Write leveling	WL	Yes	Yes	Yes				
Temperature controlled refresh	TCR	Yes	Yes	Yes				
Low-power auto self refresh	LPASR	Yes	Yes	Yes				
Fine granularity refresh	FGR	Yes	Yes	Yes				
Multipurpose register	MR	Yes	Yes	Yes				
Data mask	DM	No	Yes	Yes				
Data bus inversion	DBI	No	Yes	Yes				
TDQS	_	No	Yes	No				
ZQ calibration	ZQ CAL	Yes	Yes	Yes				
V _{REFDQ} calibration	_	Yes	Yes	Yes				
Per-DRAM addressability	Per DRAM	Yes	Yes	Yes				
Mode regsiter readout	-	Yes	Yes	Yes				
Command/Address latency	CAL	Yes	Yes	Yes				
Write CRC	CRC	Yes	Yes	Yes				
CA parity	_	Yes	Yes	Yes				
Gear-down mode	_	Yes	Yes	Yes				
Programmable preamble	_	Yes	Yes	Yes				
Maximum power-down mode	MPSM	Yes	Yes	Yes				
Additive latency	AL	Yes	Yes	Yes				
Connectivity test mode	СТ	JEDEC optional on 8Gb and larger densities Micron supports on all densities Yes						
Hard post package repair mode	hPPR	JEDEC optional on 4Gb Micron supports on all densities						
Soft post package repair mode	sPPR	JEDEC optional on 4Gb and 8Gb Micron supports on all densities						

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.



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