73M1903
Modem Analog Front End

Simplifying System Integration™

DATA SHEET

February 2009

DESCRIPTION

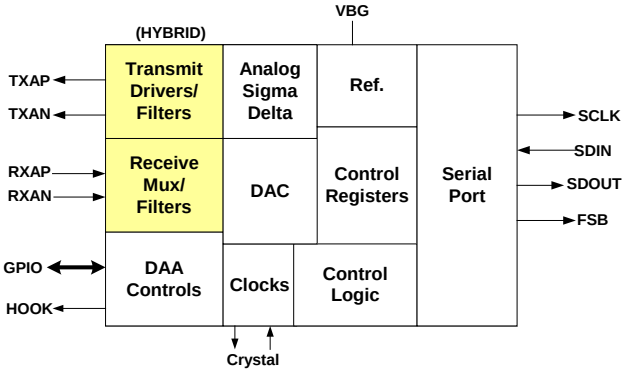
The Teridian 73M1903 Analog Front End (AFE) IC includes fully differential hybrid driver outputs, which connect to the telephone line interface through a transformer-based DAA. The receive pins are also fully differential for maximum flexibility and performance. This arrangement allows for the design of a high performance hybrid circuit to improve signal to noise performance under low receive level conditions, and compatibility with any standard transformer intended for PSTN communications applications.

The device incorporates a programmable sample rate circuit to support soft modem and DSP based implementations of all speeds up to V.92 (56 kbps). The sampling rates supported are from 7.2 kHz to 14.4 kHz by programming pre-scaler NCO and PLL NCO.

The 73M1903 device incorporates a digital host interface that is compatible with the serial ports found on most commercially available DSPs and processors and exchanges both payload and control information with the host.

Cost-saving features of the device include an input reference frequency circuit, which accepts a range of crystals from 9-27 MHz. It also accepts external reference clock values between 9-40 MHz generated by the host processor. In most applications, this eliminates the need for a dedicated crystal oscillator and reduces the bill of material (BOM).

The 73M1903 also supports two analog loop back and one digital loop back test modes.



FEATURES

- Up to 56 kbps (V.92) performance
- Programmable sample rates (7.2 - 14.4 kHz)
- Reference clock range of 9-40 MHz
- Crystal frequency range of 9-27 MHz
- Host synchronous serial interface operation
- Pin compatible with 73M2901CL/CE modems
- Low power modes
- On board line interface drivers
- Fully differential receiver and transmitter
- Drivers for transformer interface
- 3.0 V – 3.6 V operation
- 5 V tolerant I/O
- Industrial temperature range (-40 to +85 °C)
- JATE compliant transmit spectrum
- Package options:
  - 32-pin QFN
  - 20-pin TSSOP
- RoHS compliant (6/6) lead-free packages

APPLICATIONS

- Set Top Boxes
- Personal Video Recorders (PVR)
- Multifunction Peripherals (MFP)
- Fax Machines
- Internet Appliances
- Game Consoles
- Point of Sale Terminals
- Automatic Teller Machines
- Speaker Phones
- RF Modems

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1 Signal Description

The Teridian 73M1903 modem AFE IC is available in a 20-pin TSSOP or 32-pin QFN package with the same pin out. The following table describes the function of each pin. There are two pairs of power supply pins, VPA (analog) and VPD (digital). They should be separately decoupled from the supply source in order to isolate digital noise from the analog circuits internal to the chip. Failure to adequately isolate and decouple these supplies will compromise device performance.

Table 1: Inputs Selected in Regular and Alternate Multiplexer Cycles

Pin Name	**Type**	**32QFN Pin #**	**20VT Pin#**	**Description**
VND	GND	1,22	2,18	Negative Digital Ground
VNA	GND	16	13	Negative Analog Ground
VPD	PWR	2,25	3	Positive Digital Supply
VPA	PWR	10	8	Positive Analog Supply
VPPLL	PWR	20	17	Positive PLL Supply, shared with VPD
VNPLL	PWR	17	14	Negative PLL Ground
$\overline{\text{RST}}$	I	9	7	Master reset. When this pin is a logic 0 all registers are reset to their default states; Weak-pulled high- default.
OSCIN	I	19	16	Crystal oscillator input. When providing an external clock source, drive OSCIN.
OSCOUT	O	18	15	Crystal oscillator circuit output pin.
GPIO(0-7)	I/O	3, 4, 5, 6, 23, 24,30,31	N/A	Software definable digital input/output pins. Not available in the 20VT (TSSOP) package.
VREF	O	13	6	Reference voltage pin (Reflects VREF).
RXAP	I	15	12	Receive analog positive input.
RXAN	I	14	11	Receive analog negative input.
TXAP	O	12	10	Transmit analog positive output.
TXAN	O	11	9	Transmit analog negative output.
SCLK	O	8	5	Serial interface clock. With SCLK continuous selected, Frequency = 256*Fs (=2.4576 MHz for Fs=9.6 kHz)
SDOUT	O	32	1	Serial data output (or input to the host).
SDIN	I	29	20	Serial data input (or output from the host).
$\overline{\text{FS}}$	O	7	4	Frame synchronization. (Active Low)
TYPE	I	27	19	Type of frame sync. Open, weak-pulled high = early (mode1); tied low = late (mode0).
SckMode	I	28	NA	Controls the SCLK behavior after $\overline{\text{FS}}$. Open, weak-pulled high = SCLK Continuous; tied low = 32 clocks per R/W cycle. Not available in 20VT.

1.1 Serial Interface

The serial data port is a bi-directional port that can be supported by most DSPs. Although the 73M1903 is a peripheral to the DSP (host controller), the 73M1903 is the master of the serial port. It generates a serial bit clock, Sclk, from a system clock, Sysclk, which is normally an output from an on-chip PLL that can be programmed by the user. The serial bit clock is always derived by dividing the system clock by 18. The sclk rate, Fsclk, is related to the frame synchronization rate, Fs, by the relationship Fsclk = 256 x Fs or Fs = Fsclk / 256 = Fsys / 18 / 256 = Fsys / 4608, where Fsys is the frequency of Sysclk. Fs is also the rate at which both the transmit and receive data bytes are sent (received) to (by) the Host. Throughout this document two pairs of sample rate, Fs, and crystal frequency, Fxtal, will be often cited to facilitate discussions. They are:

1. $Fxtal_1$ = 27 MHz, Fs_1 = 7.2 kHz
2. $Fxtal_2$ = 18.432 MHz, Fs_2 = 8 kHz.
3. $Fxtal_3$ = 24.576 MHz, Fs_3 = 9.6 kHz – chip default.

Upon reset, until a switch to the PLL based clock, Pllclk, occurs, the system clock will be at the crystal frequency, Fxtal, and therefore the serial bit clock will be Sclk = Fsys/18 = Fxtal/18.

Examples:

1. If $Fxtal_1$ = 27.000 MHz, then sclk=1.500 MHz and Fs=sclk/256 = 5.859375 kHz.
2. If $Fxtal_2$ = 18.432 MHz, then sclk=1.024 MHz and Fs=sclk/256 = 4.00 kHz.
3. If $Fxtal_3$ = 24.576 MHz, then sclk=1.3653 MHz and Fs=sclk/256 = 5.33 kHz.

When 73M1903 is programmed through the serial port to a desired Fs and the PLL has settled out, the system clock will transition to the PLL-based clock in a glitch-less manner.

Examples:

1. If Fs_1 = 7.2 kHz, Fsys = 4608 * Fs = 33.1776 MHz and sclk = Fsys / 18 = 1.8432 MHz.
2. If Fs_2 = 8.0 kHz, Fsys = 4608 * Fs = 36.8640 MHz and sclk = Fsys / 18 = 2.048 MHz.
3. If Fs_3 = 9.6 kHz, Fsys = 4608 * Fs = 44.2368 MHz and sclk = Fsys / 18 = 2.4576 MHz.

This transition is entirely controlled by the host. Upon reset or power down of PLL and/or analog front end, the chip will automatically run off the crystal until the host forces the transition by setting a bit in a designated serial port register – location bit 7, 0Eh. The transition should be forced on or after the second Frame Synch period following the write to a designated PLL programming register (0Dh).

When reprogramming the PLL the host should first transition the system clock to the crystal before reprogramming the PLL so that any transients associated with it will not adversely impact the serial port communication.

Power saving is accomplished by disabling the analog front end by clearing bit 7 of CTRL1 (address 00h), ENFE=0.

During the normal operation, a data $\overline{FS}$ is generated by the 73M1903 at the rate of Fs. For every data $\overline{FS}$ there are 16 bits transmitted and 16 bits received. The frame synchronization ($\overline{FS}$) signal is pin programmable for type. $\overline{FS}$ can either be early or late determined by the state of the TYPE input pin. When the TYPE pin is left open, an early $\overline{FS}$ is generated in the bit clock prior to the first data bit transmitted or received. When held low, a late FS operates as a chip select; the $\overline{FS}$ signal is active for all bits that are transmitted or received. The TYPE input pin is sampled when the reset pin is active and ignored at all other times. The final state of the TYPE pin as the reset pin is de-asserted determines the frame synchronization mode used.

The bits transmitted on the SDOUT pin are defined as follows:

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RX15	RX14	RX13	RX12	RX11	RX10	RX9	RX8	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0

If the Hardware Control bit (bit 0 of register 01h) is set to zero, the 16 bits that are received on the SDIN are defined as follows:

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TX15	TX14	TX13	TX12	TX11	TX10	TX9	TX8	TX7	TX6	TX5	TX4	TX3	TX2	TX1	CTL

In this case TX0=0 is forced.

If the Hardware Control bit (bit 0 of register 01h) is set to one, the 16 bits that are received on the SDIN input are defined as follows:

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TX15	TX14	TX13	TX12	TX11	TX10	TX9	TX8	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0

Bit 15 is transmitted/received first. Bits RX15:0 are the receive code word. Bits TX15:0 are the transmit code word. If the hardware control bit is set to one, a control frame is initiated between every pair of data frames. If the hardware control bit is set to zero, CTL is used by software to request a control frame. If CTL is high, a control frame will be initiated before the next data frame. A control frame allows the controller to read or write status and control to the 73M1903.

The control word received on the SDIN pin is defined as follows:

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

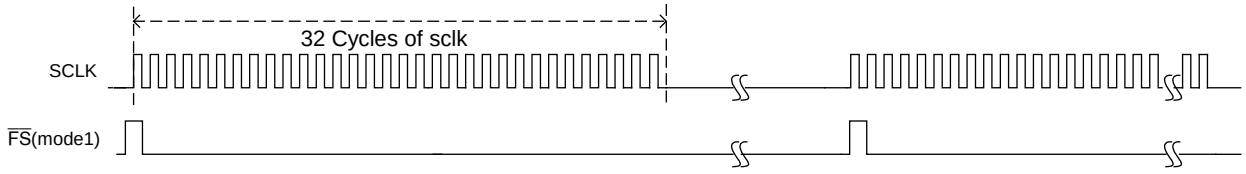
The control word transmitted on the SDOUT pin is defined as follows:

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

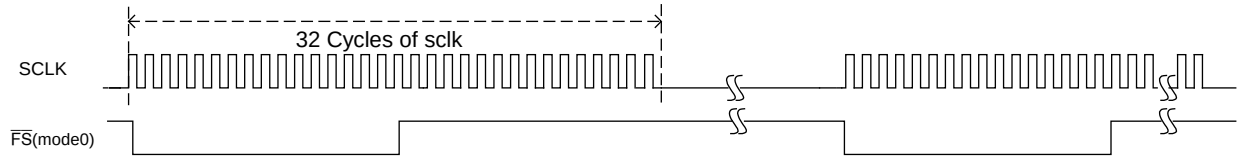
If the R/W bit is set to a 0, the data byte transmitted on the SDOUT pin is all zeros and the data received on the SDIN pin is written to the register pointed to by the received address bits; A6-A0. If the R/W bit is set to a 1, there is no write to any register and the data byte transmitted on the SDOUT pin is the data contained in the register pointed to by address bits A6-A0. Only one control frame can occur between any two data frames.

Writes to unimplemented registers are ignored. Reading an unimplemented register returns a value of 0. The position of a control data frame is controlled by the SPOS; bit 1 of register 01h. If SPOS is set to a 0 the control frames occur mid way between data frames, i.e., the time between data frames is equal. If SPOS is set to a 1, the control frame is ¼ of the way between consecutive data frames, i.e., the control frame is closer to the first data frame. This is illustrated in Figure 3.

New to the 73M1903 modem AFE IC is a feature that shuts off the serial clock (SCLK) after 32 cycles of SCLK following the frame synch (Figure 2). **This feature is unavailable in the 20 TSSOP package option**. This mode is controlled by the SckMode pin. If this pin is left open the clock will run continuously. If SckMode is low the clock will be gated on for 32 clocks for each $\overline{FS}$. The SDOUT and $\overline{FS}$ pins change values following a rising edge of SCLK. The SDIN pin is sampled on the falling edge of SCLK. Figure 4 shows the timing diagrams for the serial port.



SCLK and $\overline{FS}$ in mode 1



SCLK and $\overline{FS}$ in mode 0

Figure 1: SCLK and $\overline{FS}$ with SckMode = 0

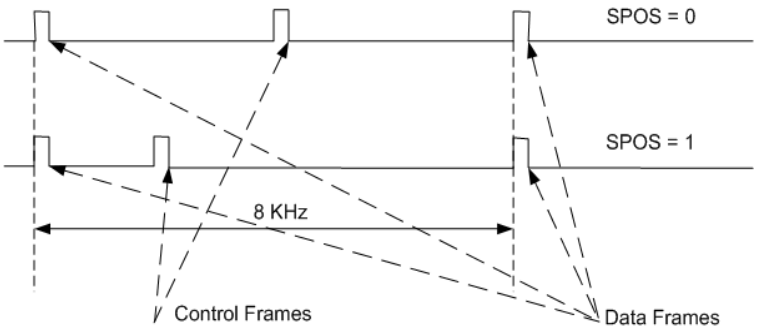


Figure 2: Control Frame Position versus SPOS

2 Control and Status Registers

Table 2 shows the memory map of addressable registers in the 73M1903. Each register and its bits are described in detail in the following sections.

Table 2: Memory Map

Address	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	08h	ENFE	Unused	TXBST1	TXBST0	TXDIS	RXG1	RXG0	RXGAIN
01	00h	TMEN	DIGLB	ANALB	INTLB	Reserved	RXPULL	SPOS	HC
02	FFh	GPIO7	GPIO 6	GPIO 5	GPIO 4	GPIO 3	GPIO 2	GPIO 1	GPIO 0
03	FFh	DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
04	00h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
05	00h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
06	10h	Rev3	Rev2	Rev1	Rev0	Unused	Reserved	Reserved	Reserved
07	00h	Unused	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
08	00h	Pseq7	Pseq6	Pseq5	Pseq4	Pseq3	Pseq2	Pseq1	Pseq0
09	0Ah	Prst2	Prst1	Prst0	Pdvsr4	Pdvsr3	Pdvsr2	Pdvsr1	Pdvsr0
0A	22h	Ichp3	Ichp2	Ichp1	Ichp0	FL	Kvco2	Kvco1	Kvco0
0B	12h	Unused	Ndvsr6	Ndvsr5	Ndvsr4	Ndvsr3	Ndvsr2	Ndvsr1	Ndvsr0
0C	00h	Nseq7	Nseq6	Nseq5	Nseq4	Nseq3	Nseq2	Nseq1	Nseq0
0D	C0h	Xtal1	Xtal0	Reserved	Reserved	Unused	Nrst2	Nrst1	Nrst0
0E	00h	Frcvco	PwdnPLL	Reserved	Unused	Unused	Unused	Unused	Unused
0E-7F		Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused

To prevent unintended operation, do not write to reserved or unused locations. These locations are for factory test or future use only and are not intended for customer programming.

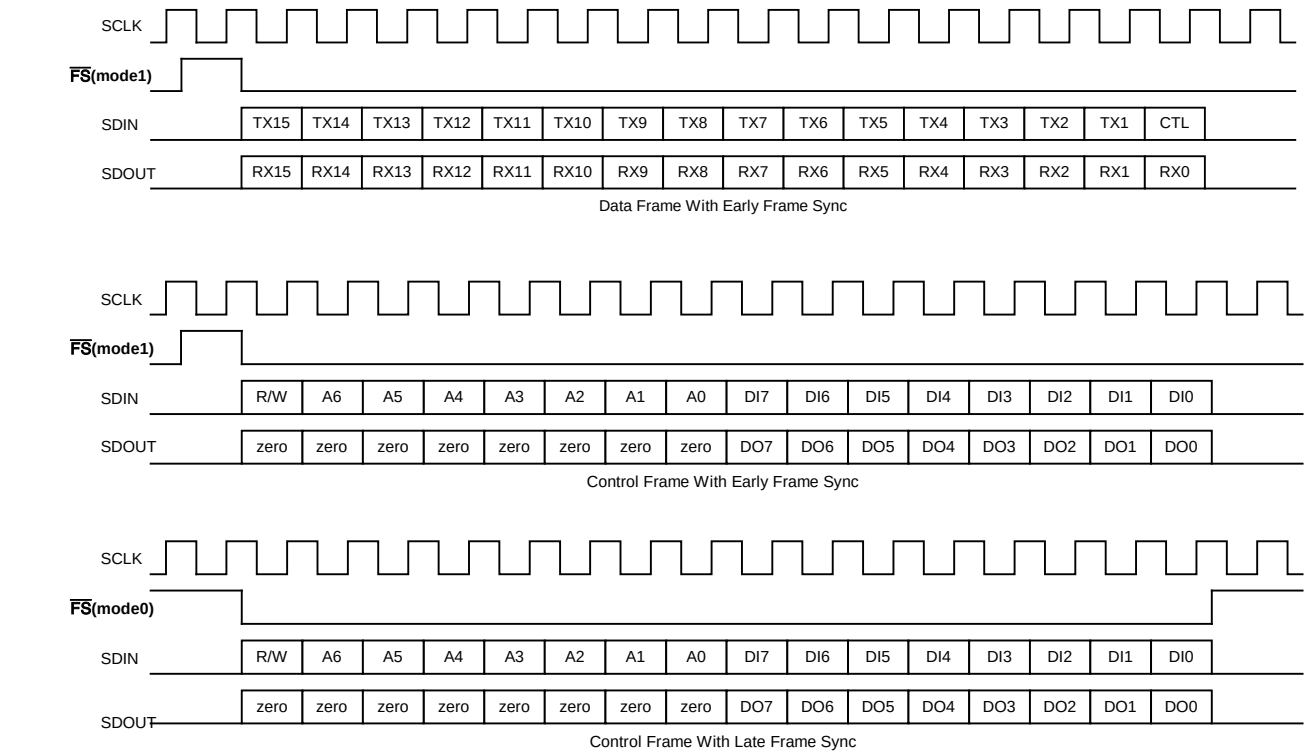


Figure 3: Serial Port Timing Diagram

2.1 GPIO

The 73M1903 modem AFE device provides 8 user defined I/O pins. Each pin is programmed separately as either an input or an output by a bit in a direction register. If the bit in the direction register is set high, the corresponding pin is an input whose value is read from the GPIO data register. If it is low, the pin will be treated as an output whose value is set by the GPIO data register.

To avoid unwanted current contention and consumption in the system from the GPIO port before the GPIO is configured after a reset, the GPIO port I/Os are initialized to a high impedance state. The input structures are protected from floating inputs, and no output levels are driven by any of the GPIO pins. The GPIO pins are configured as inputs or outputs when the host controller (or DSP) writes to the GPIO direction register. The GPIO direction and data registers are initialized to all ones (FFh) upon reset**.**

2.1.1 GPIO Data (GPIO): Address 02h

Reset State FFh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Bits in this register will be asserted on the GPIO(7:0) pins if the corresponding direction register bit is a 0. Reading this address will return data reflecting the values of pins GPIO(7:0).

2.1.2 GPIO Direction (DIR): Address 03h

Reset State FFh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0

This register is used to designate the GPIO pins as either inputs or outputs. If the register bit is low, the corresponding GPIO pin is programmed as an output. If the register bit is a 1, the corresponding pin will be treated as an input.

2.2 Analog I/O

Figure 4 shows the block diagram of the analog front end. The analog interface circuit uses differential transmit and receive signals to and from the external circuitry.

The hybrid driver in the 73M1903 IC is capable of connecting directly, but not limited to, a transformer-based Direct Access Arrangement (DAA). The hybrid driver is capable of driving the DAA's line coupling transformer, which carries an impedance on the primary side that is typically rated at 600 Ω, depending on the transformer and matching network. The hybrid drivers can also drive high impedance loads without modification. The class AB behavior of the amplifiers provides load dependent power consumption.

An on-chip band gap voltage is used to provide an internal voltage reference and bias currents for the analog receive and transmit channels. The reference derived from the bandgap, nominally 1.25 Volts, is multiplied to 1.36 Volts and output at the VREF pin. Several voltage references, nominally 1.25 Volts, are used in the analog circuits. The band gap and reference circuits are disabled after a chip reset since the ENFE bit is reset to a default state of zero. When ENFE=0, the band gap voltage and the analog bias currents are disabled. In this case all of the analog circuits are powered down and draw less than 5 µA of current.

A clock generator (CKGN) is used to create all of the non-overlapping phase clocks needed for the time sampled switched-capacitor circuits, ASDM, DAC1, and TLPF. The CKGN input is two times the analog/digital interface sample rate or 3.072 MHz clock for Fs=8 kHz.

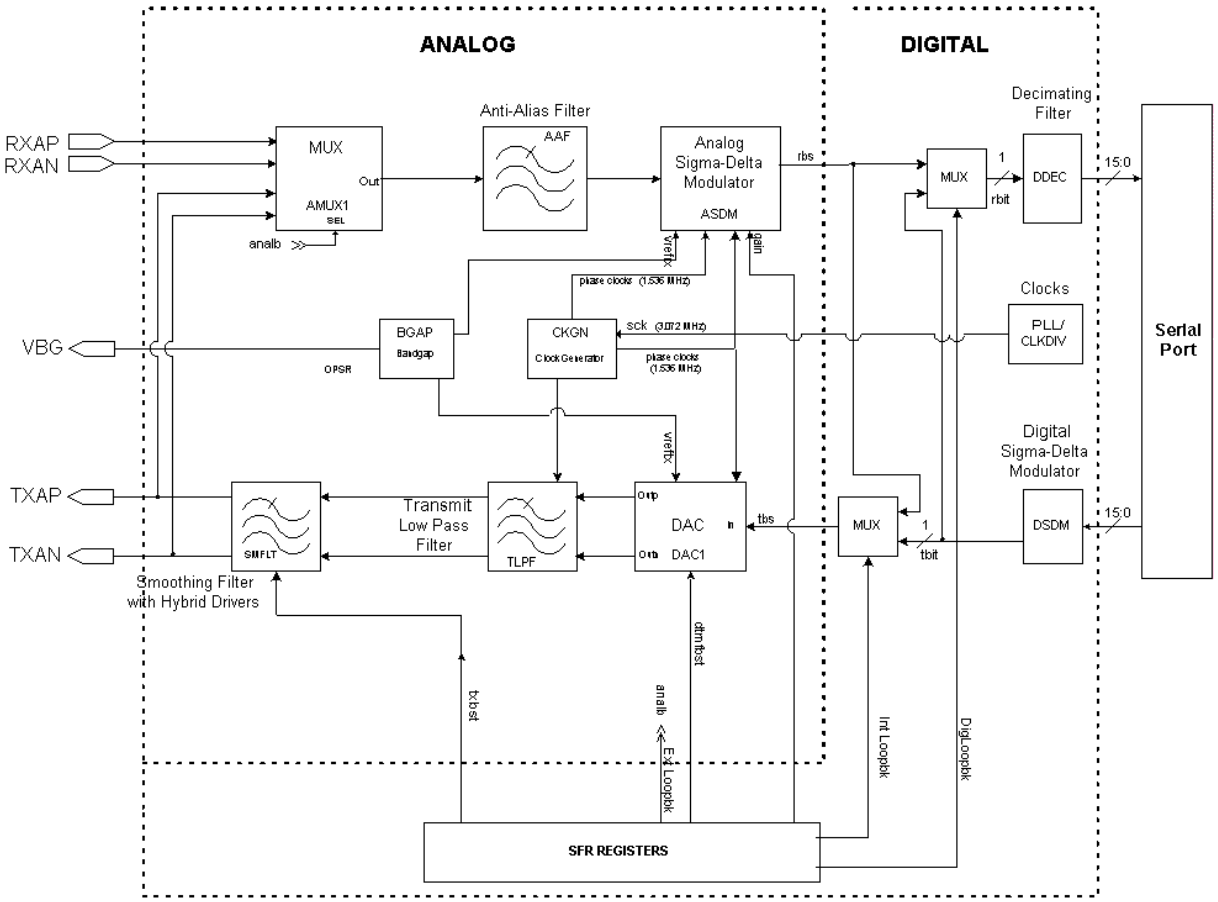


Figure 4: Analog Block Diagram

Table 3: PLL Loop Filter Settings

FL	PLLloop Filter Settings
0	R1=32 kΩ,C1=100 pF,C2=2.5 pF
1	R1=16 kΩ, C1=100 pF,C2=2.5 pF

2.2.1 Control Register (CTRL 11): Address 0Bh

Reset State 12h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Ndvsr6	Ndvsr5	Ndvsr4	Ndvsr3	Ndvsr2	Ndvsr1	Ndvsr0

Ndvsr[6:0] represents the divisor. If Nrst{2:0] =0 this register is ignored.

2.2.2 Control Register (CTRL 12): Address 0Ch

Reset State 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Nseq7	Nseq6	Nseq5	Nseq4	Nseq3	Nseq2	Nseq1	Nseq0

Nseq[7:0] represents the divisor sequence.

2.2.3 Control Register (CTRL 13): Address 0Dh

Reset State 48h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Xtal1	Xtal0	Reserved	Reserved	Unused	Nrst2	Nrst1	Nrst0

Xtal[1:0] : 00 = Xtal osc. bias current at 120 µA
01 = Xtal osc. bias current at 180 µA
10 = Xtal osc. bias current at 270 µA
11 = Xtal osc. bias current at 450 µA

If OSCIN is used as a Clock input, “00” setting should be used to save power(=167 µA at 27.648 MHz).
Nrst[3:0] represents the rate at which the NCO sequence register is reset.
The address 0Dh must be the last register to be written to when effecting a change in PLL.

2.2.4 Control Register (CTRL 14): Address 0Eh

Reset State 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Frcvco	PwdnPLL	Reserved	Unused	Unused	Unused	Unused	Unused

Frcvco = 1 forces VCO as system clock. This is reset upon $\overline{\text{RST}}$, PwdnPLL = 1 or ENFE = 0. Both PwdnPLL and ENFE are delayed coming out of digital section to keep PLL alive long enough to transition the system clock to crystal clock when Frcvco is reset by PwdnPLL or ENFE.
PwdnPll = 1 forces Power down of PLL analog section.

3 Clock Generation

3.1 Crystal Oscillator and Pre-scaler NCO

The crystal oscillator operates over wide choice of crystals (from 9 MHz to 27 MHz) and it is first input to an NCO based pre-scaler (divider) prior to being passed onto an on-chip PLL. The intent of the pre-scaler is to convert the crystal oscillator frequency, Fxtal, to a convenient frequency to be used as a reference frequency, Fref, for the PLL. The NCO pre-scaler requires a set of three numbers to be entered through the serial port (Pseq[7:0], Prst[2:0] and Pdvsr[2:0]. The PLL also requires 3 numbers as for programming; Ndvsr[6:0], Nseq[7:0], and Nrst[2:0]. The following is a brief description of the registers that control the NCOs, PLLs, and sample rates for the 73M1903 IC. The tables show some examples of the register settings for different clock and sample rates. A more detailed discussion on how these values are derived can be found in Appendix B.

3.1.1 Control Register (CTRL 8): Address 08h

Reset State 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pseq7	Pseq6	Pseq5	Pseq4	Pseq3	Pseq2	Pseq1	Pseq0

This corresponds to the sequence of divisor. If Prst{2:0] =0 this register is ignored.

3.1.2 Control Register (CTRL 9): Address 09h

Reset State 0Ah

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Prst2	Prst1	Prst0	Pdvsr4	Pdvsr3	Pdvsr2	Pdvsr1	Pdvsr0

Prst[2:0] represents the rate at which the sequence register is reset.
Pdvsr[4:0] represents the divisor.

3.1.3 Control Register (CTRL 10): Address 0Ah

Reset State 22h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ichp3	Ichp2	Ichp1	Ichp0	FL	Kvco2	Kvco1	Kvco0

Kvco2:0 represents the magnitude of Kvco associated with the VCO within PLL. This indicates the center frequency of the VCO when the control voltage is 1.6 Volts and the slope of the VCO freq versus control voltage (i.e., Kvco.). FL represents the PLL loop filter settings.

Table 4: Kvco versus Settings at Vc=1.6 V, 25 °C

Kvco2	Kvco1	Kvco0	Fvco	Kvco
0	0	0	33 MHz	38 MHz/v
0	0	1	36 MHz	38 MHz/v
0	1	0	44 MHz	40 MHz/v
0	1	1	48 MHz	40 MHz/v
1	0	0	57 MHz	63 MHz/v
1	0	1	61 MHz	63 MHz/v
1	1	0	69 MHz	69 MHz/v
1	1	1	73 MHz	69 MHz/v

Table 5: PLL Power Down

Addr. 00h bit 7 ENFE	Addr. 0Eh bit 6 PwdnPLL	PLL
0	X	PLL Power Off
1	0	PLL Power On
1	1	PLL Power Off

Table 6: Examples of NCO Settings

	Fs (kHz)	Nnco1 Dnco1	PsDiv	PsSeq(7:0)	PsRst =Dnco1 -1	Nnco2 Dnco2	PllDiv	PllSeq(7:0)	PllRst =Dnco2 -1	Fvco (Mhz)	PPM
Fxtal(Mhz)=27.0	7.2	8/125	15	11011010	7	5/96	19	XXX10000	4	33.177600	0
	8.0	8/125	15	11011010	7	3/64	21	XXXXX100	2	36.864000	0
	2.4*8/7*3 =8.22857142858	8/169	21	10000000	7	3/89	29	XXXXX110	2	37.917160*	-3
	8.4	8/125	15	11011010	7	5/112	22	XXX10100	4	38.707200	0
	9.0	8/125	15	11011010	7	1/24	24	XXXXXXXX	0	41.472000	0
	9.6	8/125	15	11011010	7	5/128	25	XXX11010	4	44.236800	0
	2.4*10/7*3 =10.2857142857	8/125	15	11011010	7	7/192	27	X1010110	6	47.396571	0
	2.4*8/7*4 =10.9714285714	7/50	7	X1000000	6	8/107	13	10100100	7	50.557500*	23
	11.2*	7/52	7	X1010100	6	5/71	14	XXX10000	4	51.611538*	38
	12.0	8/125	15	11011010	7	1/32	32	XXXXXXXX	0	55.296000	0
	12.8*	8/65	8	10000000	7	4/71	17	XXXX1110	3	58.984615*	38
	2.4*10/7*4 =13.7142857143	7/80	11	X1010100	6	4/107	26	XXXX1110	3	63.196875*	23
	14.4	8/125	15	11011010	7	5/192	38	XXX10100	4	66.355200	0
Fxtal(Mhz)=24.576	7.2	1/10	10	XXXXXXXX	0	2/27	13	XXXXXX10	1	33.177600	0
	8.0	1/10	10	XXXXXXXX	0	1/15	15	XXXXXXXX	0	36.864000	0
	2.4*8/7*3 =8.22857142858	4/35	8	XXXX1110	3	2/27	13	XXXXXX10	1	37.917257…	0
	8.4	1/10	10	XXXXXXXX	0	4/63	15	XXXX1110	3	38.707200	0
	9.0	1/10	10	XXXXXXXX	0	8/135	16	11111110	7	41.472000	0
	9.6	1/10	10	XXXXXXXX	0	1/18	18	XXXXXXXX	0	44.236800	0
	2.4*10/7*3 =10.2857142857	3/28	9	XXXXX100	2	1/18	18	XXXXXXXX	0	47.3965714..	0
	2.4*8/7*4 =10.9714285714	4/35	8	XXXX1110	3	1/18	18	XXXXXXXX	0	50.5563429..	0
	11.2	1/10	10	XXXXXXXX	0	1/21	21	XXXXXXXX	0	51.609600	0
	12	1/10	10	XXXXXXXX	0	2/45	22	XXXXXX10	1	55.296000	0
	12.8	1/10	10	XXXXXXXX	0	1/24	24	XXXXXXXX	0	58.982400	0
	2.4*10/7*4 =13.7142857143	1/7	7	XXXXXXXX	0	1/18	18	XXXXXXXX	0	63.19542…	0
	14.4	1/10	10	XXXXXXXX	0	1/27	27	XXXXXXXX	0	66.355200	0
Fxtal(Mhz)=9.216	7.2	1/4	4	XXXXXXXX	0	5/72	14	XXX10100	4	33.177600	0
	8.0	1/4	4	XXXXXXXX	0	1/16	16	XXXXXXXX	0	36.864000	0
	8.4	1/4	4	XXXXXXXX	0	5/84	16	XXX11110	4	38.707200	0
	9.0	1/4	4	XXXXXXXX	0	1/18	18	XXXXXXXX	0	41.472000	0
	9.6	1/4	4	XXXXXXXX	0	5/96	19	XXX10000	4	44.236800	0
	2.4*8/7*4 =10.9714285714	2/7	6	XXXXXX10	4	5/96	19	XXX10000	4	50.556343	0
	11.2	1/4	4	XXXXXXXX	0	5/112	22	XXX10100	4	51.609600	0
	12	1/4	4	XXXXXXXX	0	1/24	24	XXXXXXXX	0	55.296000	0

	Fs (kHz)	Nnco1 Dnco1	PsDiv	PsSeq(7:0)	PsRst =Dnco1 -1	Nnco2 Dnco2	PllDiv	PllSeq(7:0)	PllRst =Dnco2 -1	Fvco (Mhz)	PPM
	12.8	1/4	4	XXXXXXXX	0	5/128	25	XXX11010	4	58.982400	0
	14.4	1/8	8	XXXXXXXX	0	5/288	57	XXX11010	4	66.355200	0
Fxtal(Mhz)=24.000	7.2	8/125	15	11011010	7	5/108	21	XXX11010	4	33.1776	0
	8.0	2/25	12	XXXXXX10	1	5/96	19	XXX10000	4	36.864	0
	2.4*8/7*3 =8.22857142858	4/73	18	XXXX1000	3	6/173	28	XX111110	5	37.91781*	15
	8.4	8/125	15	11011010	7	5/126	25	XXX10000	4	38.7072	0
	9.0	4/25	6	XXXX1000	3	5/54	10	XXX11110	4	41.472	0
	9.6	8/125	15	11011010	7	5/144	28	XXX11110	4	44.2368	0
	2.4*10/7*3 =10.2857142857	8/125	15	11011010	7	7/216	30	X1111110	6	47.39657	0
	2.4*8/7*4 =10.9714285714	6/59	9	XX111110	5	7/145	20	X1110110	6	50.5569*	12
	11.2	8/125	15	11011010	7	5/168	33	XXX11010	4	51.6096	0
	12.0	4/25	6	XXXX1000	3	5/72	14	XXX10100	4	55.296	0
	12.8	8/125	15	11011010	7	5/192	38	XXX10100	4	58.9824	0
	2.4*10/7*4 =13.7142857143	5/61	12	XXX10000	4	8/257	32	10000000	7	63.19672*	21
	14.4	7/73	10	X1010100	6	6/173	28	XX111110	5	66.35616*	15
Fxtal(Mhz)= 25.35	7.2	8/163	20	10010010	7	3/80	26	110	2	33.177914*	10

Table 7: Clock Generation Register Settings for Fxtal = 27 MHz

Reg Address Fs (kHz)	8h	9h	Ah	Bh	Ch	Dh *	Ichp (µA)	Kvco [2:0]
7.2	DA	EF	20	13	10	C4	8	0
8.0	DA	EF	31	15	04	C2	10	1
2.4*8/7*3 =8.22857142858	80	F5	41	1D	06	C2	12	1
8.4	DA	EF	31	16	14	C4	10	1
9.0	DA	EF	31	18	XX	C0	10	1
9.6	DA	EF	32	19	1A	C4	10	2
2.4*10/7*3 =10.2857142857	DA	EF	43	1B	54	C6	12	3
2.4*8/7*4 =10.9714285714*	40	C7	23	0D	A4	C7	8	3
11.2*	54	C7	23	0E	10	C4	8	3
12.0	DA	EF	24	20	XX	C0	8	4
12.8*	80	E8	15	11	0E	C3	6	5
2.4*10/7*4 =13.7142857143	54	CB	26	1A	0E	C3	8	6
14.4	DA	EF	46	26	14	C4	12	6

Table 8: Clock Generation Register Settings for Fxtal = 24.576 MHz

Reg Address Fs (kHz)	8h	9h	Ah	Bh	Ch	Dh*	Ichp (µA)	Kvco [2:0]
7.2	XX	0A	10	0D	02	C1	6	0
8.0	XX	0A	11	0F	XX	C0	6	1
2.4*8/7*3 =8.22857142858	0E	68	11	0D	02	C1	6	1
8.4	XX	0A	21	0F	0E	C3	8	1
9.0	XX	0A	21	10	FE	C7	8	1
9.6	XX	0A	22	12	XX	C0	8	2
2.4*10/7*3 =10.2857142857	04	49	23	12	XX	C0	8	3
2.4*8/7*4 =10.9714285714	0E	68	23	12	XX	C0	8	3
11.2	XX	0A	23	15	XX	C0	8	3
12	XX	0A	14	16	02	C1	6	4
12.8	XX	0A	15	18	XX	C0	6	5
2.4*10/7*4 =13.7142857143	XX	07	16	12	XX	C0	6	6
14.4	XX	0A	26	1B	XX	C0	8	6

Table 9: Clock Generation Register Settings for Fxtal = 9.216 MHz

Reg Address Fs (kHz)	8h	9h	Ah	Bh	Ch	Dh*	Ichp (µA)	Kvco [2:0]
7.2	XX	04	20	0E	14	C4	8	0
8.0	XX	04	31	10	XX	C0	10	1
8.4	XX	04	31	10	1E	C4	10	1
9.0	XX	04	31	12	XX	C0	10	1
9.6	XX	04	32	13	10	C4	10	2
2.4*8/7*4 =10.9714285714	02	23	33	13	10	C4	10	3
11.2	XX	04	33	16	14	C4	10	3
12	XX	04	24	18	XX	C0	8	4
12.8	XX	04	35	19	1A	C4	10	5
14.4	XX	08	66	39	1A	C4	16	6

Table 10: Clock Generation Register Settings for Fxtal = 24.000 MHz

Reg Address Fs (kHz)	8h	9h	Ah	Bh	Ch	Dh*	Ichp (µA)	Kvco [2:0]
7.2	DA	EF	30	15	1A	C4	10	0
8.0	02	2C	31	13	10	C4	10	1
2.4*8/7*3 =8.22857142858	08	72	41	1C	3E	C5	12	1
8.4	DA	EF	41	19	10	C4	12	1
9.0	08	66	11	0A	1E	C4	6	1
9.6	DA	EF	42	1C	1E	C4	12	2
2.4*10/7*3 =10.2857142857	DA	EF	43	1E	7E	C6	12	3
2.4*8/7*4 =10.9714285714	3E	A9	33	14	76	C6	10	3
11.2	DA	EF	53	21	1A	C4	14	3
12	08	66	14	0E	14	C4	6	4
12.8	DA	EF	45	26	14	C4	12	5
2.4*10/7*4 =13.7142857143	10	8C	46	20	80	C7	12	6
14.4	54	CA	46	1C	3E	C5	12	6

Table 11: Clock Generation Register Settings for Fxtal = 25.35 MHz

Reg Address FS (KHz)	8h	9h	Ah	Bh	Ch	Dh*	Ichp (µA)	Kvco [2:0]
7.2	92	F4	50	1A	06	C2	14	0

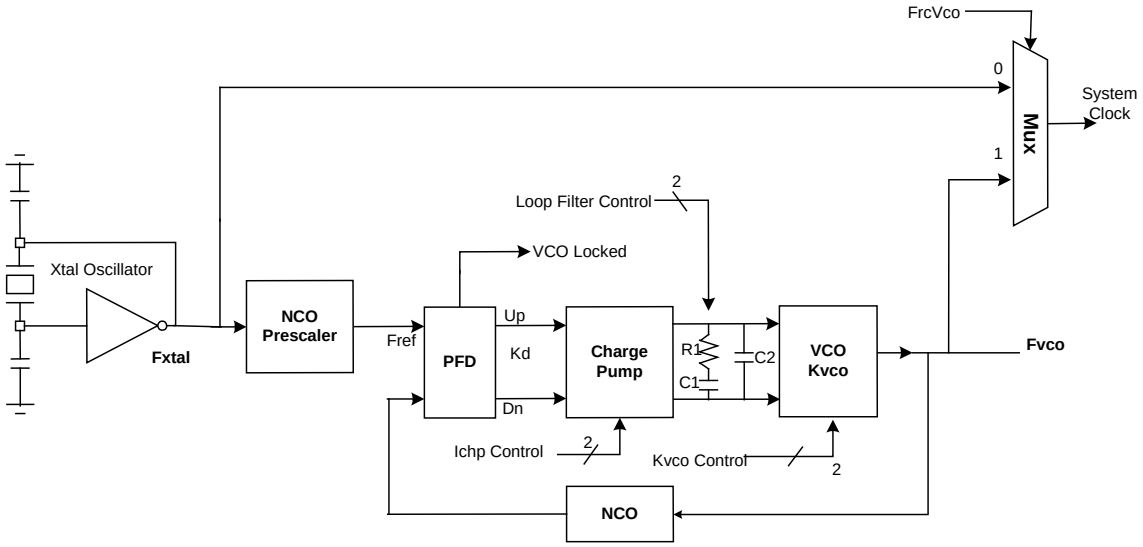


Figure 5: Clock Generation

4 Modem Receiver

A differential receive signal applied at the RXAP and RXAN pins or the output signal at TXAP and TXAN pass through a multiplexer, which selects the inputs to the ADC. In normal mode, RXAP/RXAN are selected. In analog loopback mode, TXAP/TXAN are selected. The DC bias for the RXAP/RXAN inputs is supplied from TXAP/TXAN through the external DAA in normal conditions. (See Appendix A) It can be supplied internally, in the absence of the external DAA, by setting RXPULL bit in Control Register 2. The output of the multiplexer goes into a second-order continuous time, Sallen-Key, low-pass filter (AAF) with a 3 dB point at approximately 40 kHz. The filtered output signal is the input to an analog sigma-delta modulator (ASDM), clocked at an over sampling frequency of 1.536 MHz for Fs = 8 kHz, which converts the analog signal to a serial bit stream with a pulse density that is proportional to the amplitude of the analog input signal.

There are three gain control bits for the receive path. The RXGAIN bit in control register one results in a +20 dB gain of the receive signal when set to a "1". This 20 dB of gain compensates for the loss through the DAA while on hook. It is used for Caller ID reception. This gain is realized in the front end of ASDM. The other gain bits in control register 1, RXG1:0, compensate for differences in loss through the receive path.

Table 12: Receive Gain

RXG1	RXG0	Receive Gain Setting
0	0	6 dB
0	1	9 dB
1	0	12 dB
1	1	0 dB

The output of ASDM is a serial bit stream that feeds three digital $sinc^3$ filters. Each filter has a $[\sin(x)/x]^3$ frequency response and provides a 16 bit sample every 288 clock cycles. The filters are synchronized so that there is one sample available after every 96 analog samples or at a rate of 16 kHz for Fs=8 kHz. The output of the $sinc^3$ filter is a 17 bit, two's compliment number representing the amplitude of the input signal. The $sinc^3$ filter, by virtue of holding action (for 96 sample period), introduces a droop in the passband that is later corrected for by a 48 tap FIR filter that follows. The maximum digital word that can be output from the filter is 0d800h. The minimum word is 12800h.

The output of the $sinc^3$ filter is input to another 48 tap digital FIR filter that provides an amplitude correction in the passband to the output of the $sinc^3$ filter as well as rejecting noise above Fs/2 or 4 kHz for Fs=8 kHz. The output of this filter is then decimated by a factor of 2; so, the final output is 16 bit, two's compliment samples at a rate of 8 kHz.

Figure 6 and Figure 7 depict the $sinc^3$ filter's frequency response of ASDM along with the 48 tap digital FIR response that compensates for it and the resulting overall response of the receiver.

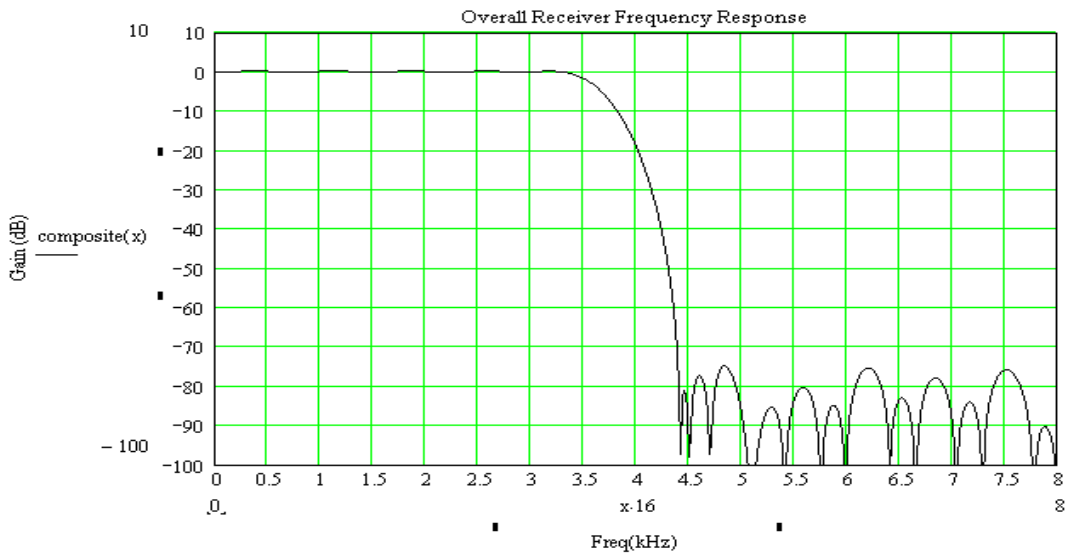


Figure 6: Overall Receiver Frequency Response

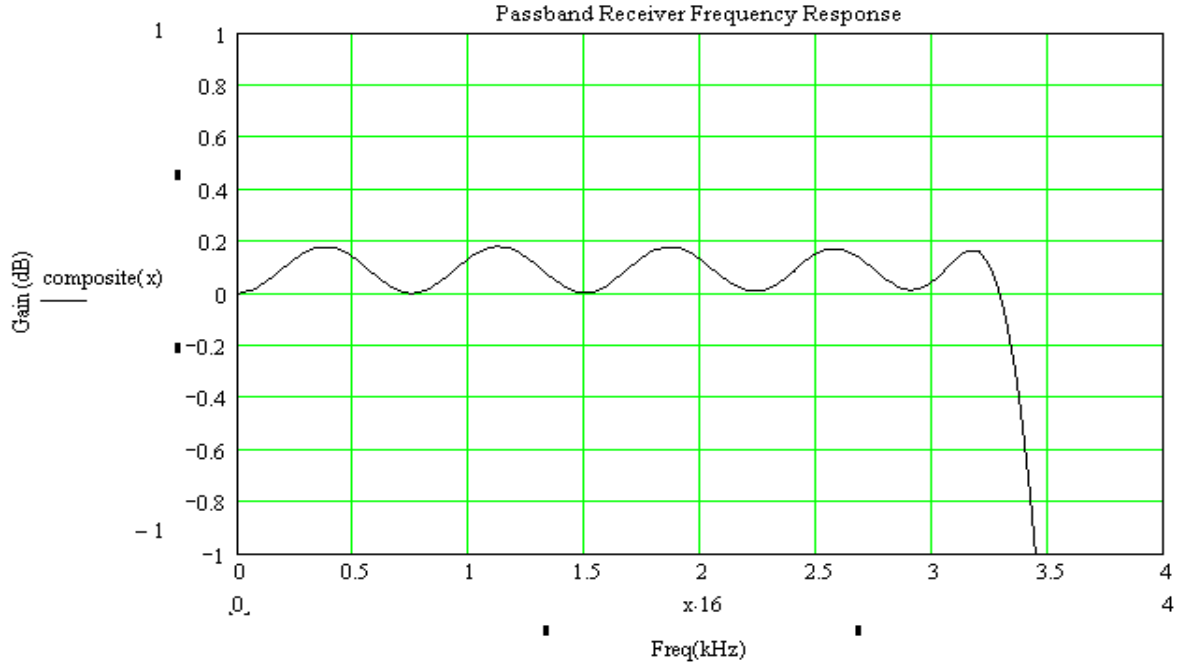


Figure 7: Rx Passband Response

It is important to keep in mind that the receive signal should not exceed 1.16 Vpk-diff for proper performance for Rxg=11 (0 dB). In particular, if the input level exceeds a value such that one's density of RBS exceeds 99.5%, $sinc^3$ filter output will exceed the maximum input range of the decimation filter and consequently the data will be corrupted. Also for stability reasons, the receive signal should not exceed 1.16 Vpk differentially. This value is set at around 65% of the full receive signal of 1.791 Vpkdiff at RXAP/RXAN pins that "would" corresponds to ASDM putting out all ones.

Figure 8 and Figure 9 show the spectrum of 1 kHz tone received at RXAP/RXAN of 1.16 Vpk-diff and 0.5 kHz and 1.0 kHz tones of 0.6 Vpk-diff each, respectively for Fs=8 kHz. Note the effect of FIR suppressing the noise above 4 kHz but at the same time enhancing (in order to compensate for the passband droop of $sinc^3$ filter) it near the passband edge of 4 kHz.

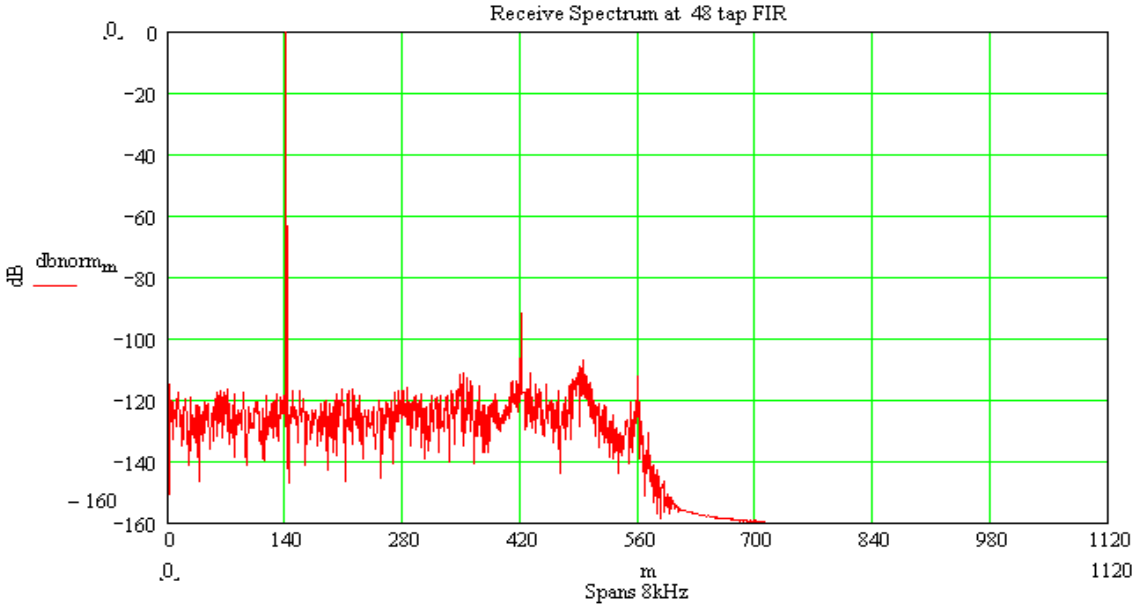


Figure 8: RXD Spectrum of 1 kHz Tone

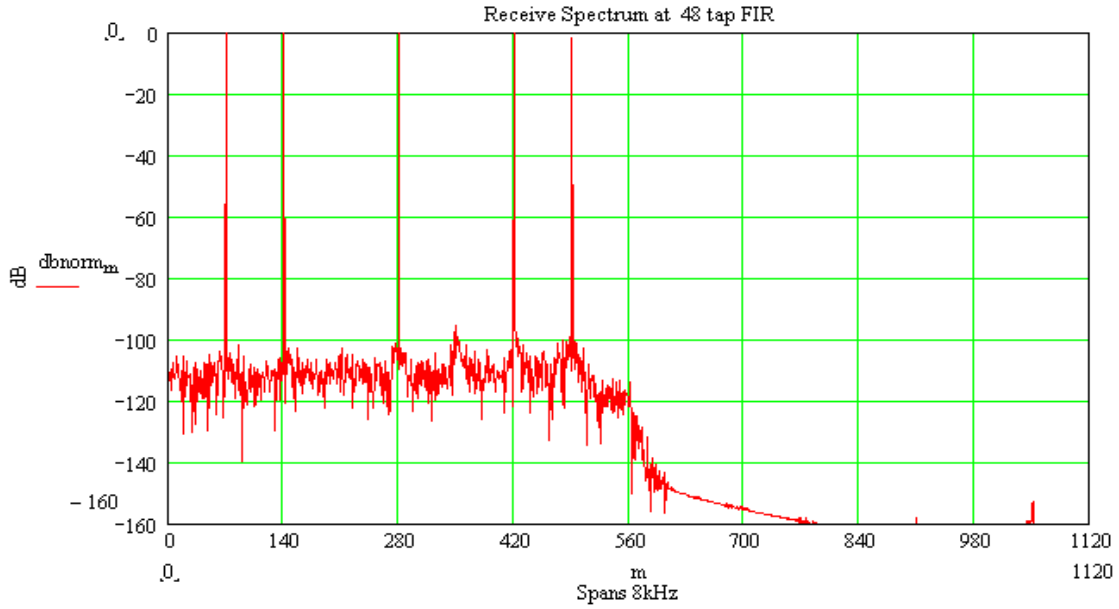


Figure 9: RXD Spectrum of 0.5 kHz, 1 kHz, 2 kHz, 3 kHz and 3.5 kHz Tones of Equal Amplitudes

5 Modem Transmitter

The modem transmitter begins with an 48 tap Transmit Interpolation Filter (TIF) that takes in the 16-bit, two's compliment numbers (TXD) at SDIN pin at Fs=8 kHz rate. It up-samples (interpolates) the data to 16 kHz rate rejecting the images at multiples of 8 kHz that exist in the original TXD data stream and outputs 16-bit, two's compliment numbers to a digital sigma-delta modulator. The gain of the interpolation filter is 0.640625 (–3.8679 dB) at DC.

The digital sigma-delta modulator (DSDM) takes 16-bit, two's compliment numbers as input and generates a 1's bit stream which feeds into a D to A converter (DAC1). The gain through DSDM is 1.0. DSDM takes 16-bit, two's compliment numbers as input and generates a 1's bit stream that feeds into a D to A converter (DAC1).

DAC1 consists of a 5-tap FIR filter and a first order switched capacitor low pass filter both operating at 1.536 MHz. It possesses nulls at multiples of 384 kHz to allow decimation by the succeeding filter.

DAC1's differential output is fed to a 3rd-order switched-capacitor low pass filter (TLPF). The output of TLPF drives a continuous time smoothing filter. The sampling nature of the transmitter leads to an additional filter response that affects the in-band signals. The response is in the form of sin(x)/x and can be expressed as 20*log [(sin(PI*f/fs))/(PI*f/fs)] where f = signal frequency and fs = sample frequency = 16 kHz. Figure 10 shows the frequency response of the transmit path from TXD to TXAP/TXAN for a dc to 4 kHz in-band signal including the effect of this sampling process plus those of DAC1, TLPF and SMFLT. It is important to note that as TXD is sampled at 8 kHz, it be band-limited to 4 kHz.

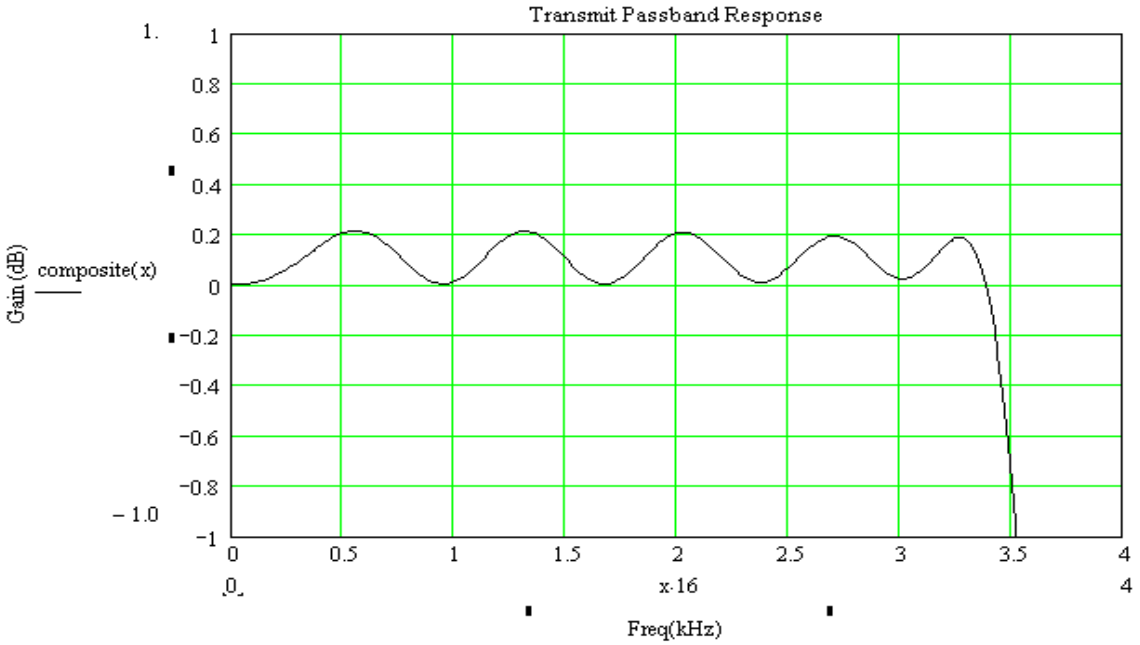


Figure 10: Frequency Response of TX Path for DC to 4 kHz in Band Signal

5.1 Transmit Levels

The 16-bit transmit code word written by the DSP to the Digital Sigma-Delta Modulator (DSDM) (via TIF) has a linear relationship with the analog output signal. So, decreasing a code word by a factor of 0.5 will result in a 0.5 (-6 dB) gain change in the analog output signal.

The following formula describes the relationship between the transmit code word and the output level at the transmit pins (TXAP/TXAN):

Vout (V) = 2 * code/32,767 * DSDMgain * dacGAIN * VREF * TLPFgain * SMFLTgain * FreqFctr

Vout is the differential peak voltage at the TXAP and TXAN pins.

Code is the 16-bit, two's compliment transmit code word written out by the DSP to the DSDM (via TIF). The code word falls within a range of ± 32,767. For a sinusoidal waveform, the peak code word should be used in the formula to obtain the peak output voltage.

DSDMgain is the scaling factor used on the transmit code word to reduce the possibility of saturating the modulator. This value is set to 0.640625(–3.555821 dB) at dc in the 48 tap transmit interpolation filter (TIF) that precedes DSDM.

dacGAIN is the gain of the DAC. The value *dacGAIN* is calculated based on capacitor values inside DAC1 and *dacGAIN*=8/9=0.8889. The number 32,767 refers to the code word that generates an 82% "1's" pulse density at the output of the DSDM. As one can see from the formula, the D to A conversion is dependent on the level of *VREF*. Also when TXBST1 bit is set, *VREF* is increased from 1.36 V to 1.586 V to allow higher transmit level or 16.6% increase in gain. This bit is intended for enhancing the DTMF transmit level and should not be used in data mode.

TLPFgain is the gain of TLPF and nominally equals to 0.00 dB or 1.0.

SMFLTgain is the gain of SMFLT and nominally equal to 1.445 or 3.2 dB.
When TXBST0 bit is set, the gain is further increased by 1.65 dB (1.21) for the total of 4.85 dB. This is to accommodate greater hybrid insertion loss encountered in some applications.

FreqFctr shows dependency of the entire transmit path on frequency. See Figure 10.
With the transmit code word of +/- 32,767, the nominal differential swing at the transmit pins at dc is:

Vout (V) = 2 * code/32,767 * DSDMgain * dacGAIN * VREF * TLPFgain * SMFLTgain * FreqFctr
= 2 * 32,767/32767 * 0.6640625 * 0.8889 * 1.36 * 1.0 * 1.4454 * 1.0 = 2.31Vpk diff.

When TXBST1 bit is set, Vout (V) = 1.166 * 2.31= 2.693 Vpk diff.

When TXBST0 bit is set, Vout (V) = 1.21 * 2.31= 2.795 Vpk diff, if not limited by power supply or internal reference.

When both TXBST1 and TXBST0 are set to 1, Vout (V) = 1.166 * 1.21 * 2.31 = 3.259 Vpk diff.

5.2 Transmit Power - dBm

To calculate the analog output power, the peak voltage must be calculated and the peak to rms ratio (crest factor) must be known. The following formula can be used to calculate the output power, in dBm referenced to 600 Ω.

Pout (dBm) = 10 * log [(Vout (V) / cf)^2 / (0.001 * 600)]

The following example demonstrates the calculation of the analog output power given a 1.2 kHz FSK tone (sine wave) with a peak code word value of 11,878 sent out by the DSP.

The differential output voltage at TXAP-TXAN will be:

With FreqFctr = 1.02, (See Figure 10)
Vout (V) = 2 * (11,878/32,767) * 0.6640625 * 0.8889 * 1.36 * 1.0 * 1.4454 * 1.02 = 0.841 V_{pk}.

The output signal power will be:
Pout (dBm) = 10 * log [(0.841 / 1.41)^2 / (0.001 * 600)] = - 2.29 dBm**.**

Table 13: Peak to RMS Ratios for Various Modulation Types

Transmit Type	Crest Factor	Max Line Level
V.90	4.0	-12 dBm
QAM	2.31	-9 dBm
DPSK	1.81	-9 dBm
FSK	1.41	-9 dBm
DTMF	1.99	-5.7 dBm

5.3 Control Register (CTRL1): Address 00h

Reset State 08h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ENFE	Unused	TXBST1	TXBST0	TXDIS	RXG1	RXG0	RXGAIN

ENFE 1 = Enable the digital filters and analog front end.
0 = Disable the analog blocks shut off the clocks to the digital and analog receive/transmit circuits.

TXBST1 1 = Add a gain of **1.335 dB (16.6%)** to the transmitter; also the common mode voltage of the transmit path is increased to 1.375 V. This is intended for enhancing DTMF transmit power only and should not be used in data mode.
0 = No gain is added

TXBST0 1 = A gain of **1.65 dB (21%)** is added to the transmitter
0 = The gain of the transmitter is nominal

TXDIS 1 = Tri-state the TXAP and TXAN pins, provides a bias of VBG into 80 kΩ for each output pin

RXG1:0 These bits control the receive gain as shown in Table 12.

RXGAIN 1 = Increase the gain of the receiver by 20 dB.

5.4 Control Register (CTRL2): Address 01h

Reset State 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMEN	DIGLB	ANALB	INTLB	CkoutEn	RXPULL	SPOS	HC

TMEN 1 = Enable test modes.

DIGLB 1 = Tie the serial bit stream from the digital transmit filter output to the digital receive filter input. DIGITAL LOOPBACK

ANALB 1 = Tie the analog output of the transmitter to the analog input of the receiver. ANALOG LOOPBACK

INTLB 1 = Tie the digital serial bit stream from the analog receiver output to the analog transmitter input. INTERNAL LOOPBACK

CkoutEn 1 = Enable the CLKOUT output; 0 = CLKOUT tri-stated. For test purposes only; do not use in normal operation.

RXPULL 1 = Pulls DC Bias to RXAP/RXAN pins, through 100 kΩ each, to VREF, to be used in testing Rx path.
0 = No DC Bias to RXAP/RXAN pins.

SPOS 1 = Control frames occur after one quarter of the time between data frames has elapsed.
0 = Control frames occur half way between data frames.

HC 1 = $\overline{FS}$ is under hardware control, bit 0 of data frames on SDIN is bit 0 of the transmit word and control frames happen automatically after every data frame.
0 = $\overline{FS}$ is under software control, bit 0 of data frames on SDIN is a control frame request bit and control frames happen only on request.

5.5 Revision Register: Address 06h

Reset State 30h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rev3	Rev2	Rev1	Rev0	Unused	Reserved	Reserved	Reserved

Bits 7-4 contain the revision level of the 73M1903 device. The rest of this register is for chip development purposes only and is not intended for customer use. Do not write to shaded locations.

6 Test Modes

There are two loop back test modes that affect the configuration of the analog front end. The internal loop back mode connects the serial bit stream generated by the analog receiver to the input of the analog transmitter. This loop back mode is similar to a remote analog loop back mode and can be used to evaluate the operation of the analog circuits. When using this loop back mode, the TXAN/TXAP pins should not be externally coupled to the RXAP/RXAN pins. Set bit 4 (INTLB) in register 1h (CTRL2) to enter this loop back mode.

The second loop back test mode is the external loop back mode, or local analog loop back mode. In this mode, the analog transmitter outputs are fed back into the input of the analog receiver. Set bit 5 (ANALB) in register 1h (CTRL2) to enter this loop back mode. In this mode, TBS must be kept to below a value that corresponds to less than 1.16 V/2.31 V x -6 dB = 25% of the full scale code of +/- 32768 at TXD in order to ensure that the receiver is not overdriven beyond the maximum of 1.16 Vpkpk diff for Rxg=11(0 dB) setting. See Table 18 for the maximum allowed transmit levels. Check the transmitted data against received data via serial interface. This tests the functionality of essentially all blocks, both digital and analog, of the chip.

There is a third loopback mode that bypasses the analog circuits entirely. Digital loop back forces the transmitter digital serial bit stream (from DSDM) to be routed into the digital receiver's $sinc^3$ filters. Set bit 6 (DIGLB) in register 1h (CTRL2) to enter this loop back mode.

7 Power Saving Modes

The 73M1903 has only one power conservation mode. When the ENFE, bit 7 in register 0h, is zero the clocks to the filters and the analog are turned off. The transmit pins output a nominal 80 kΩ impedance. The clock to the serial port is running and the GPIO and other registers can be read or updated.

8 Electrical Specifications

8.1 Absolute Maximum Ratings

Operation above maximum rating may permanently damage the device.

Parameter	Rating
Supply Voltage	-0.5 V to +4.0 V
Pin Input Voltage (except OSCIN)	-0.5 V to 6.0 V
Pin Input Voltage (OSCIN)	-0.5 V to VDD + 0.5 V

8.2 Recommended Operating Conditions

Parameter	Rating
Supply Voltage (VDD) with respect to VSS	3.0 V to 3.6 V
Oscillator Frequency	24.576 MHz ±100ppm
Operating Temperature	-40 C to +85 °C

8.3 Digital Specifications

8.3.1 DC Characteristics

Parameter	Symbol	Conditions	Min	Nom	Max	Unit
Input Low Voltage	VIL		-0.5		0.2 * VDD	V
Input High Voltage (Except OSCIN)	VIH1		0.7 VDD		5.5	V
Input High Voltage OSCIN	VIH2		0.7 VDD		VDD + 5.5	V
Output Low Voltage (Except OSCOUT, $\overline{FS}$, SCLK, SDOUT)	VOL	IOL = 4 mA			0.45	V
Output Low Voltage OSCOUT	VOLOSC	IOL = 3.0 mA			0.7	V
Output Low Voltage FS,SCLK,SDOUT	VOL	IOL = 1 mA			0.45	V
Output High Voltage (Except OSCOUT, $\overline{FS}$, SCLK, SDOUT)	VOH	IOH = -4 mA	VDD - 0.45			V
Output High Voltage OSCOUT	VOHOSC	IOH = -3.0 mA	VDD - 0.9			V
Output High Voltage $\overline{FS}$, SCLK, SDOUT	VOH	IOH = -1 mA	VDD - 0.45			V
Input Low Leakage Current (Except OSCIN)	IIL1	VSS < Vin < VIL1			1	µA
Input High Leakage Current (Except OSCIN)	IIH1	VIH1 < Vin < 5.5			1	µA
Input Low Leakage Current OSCIN	IIL2	VSS < Vin < VIL2	1		30	µA
Input High Leakage Current OSCIN	IIH2	VIH2 < Vin <VDD	1		30	µA

IDD current at 3.0V – 3.6V Nominal at 3.3V						
IDD Total current	IDD	Fs=8 kHz, Xtal=27 MHz		9	12.0	mA
IDD Total current	IDD	Fs=11.2 kHz, Xtal=27 MHz		10.3	13.4	mA
IDD Total current	IDD	Fs=14.4 kHz, Xtal=27 MHz		11.8	14.5	mA
IDD Total current ENFE=0	IDD			2	2.5	mA

8.3.2 AC Timing

Table 14: Serial I/F Timing

Parameter	Min	Nom	Max	Unit
SCLK Period (Tsclk) (Fs=8 kHz)	–	1/2.048 MHz	–	ns
SCLK to $\overline{FS}$ Delay (td1) – mode1	–	–	20	ns
SCLK to $\overline{FS}$ Delay (td2) – mode1	–	–	20	ns
SCLK to SDOUT Delay (td3) (With 10pf load)	–	–	20	ns
Setup Time SDIN to SCLK (tsu)	15	–	–	ns
Hold Time SDIN to SCLK (th)	10	–	–	ns
SCLK to $\overline{FS}$ Delay (td4) – mode0	–	–	20	ns
SCLK to $\overline{FS}$ Delay (td5) – mode0	–	–	20	ns

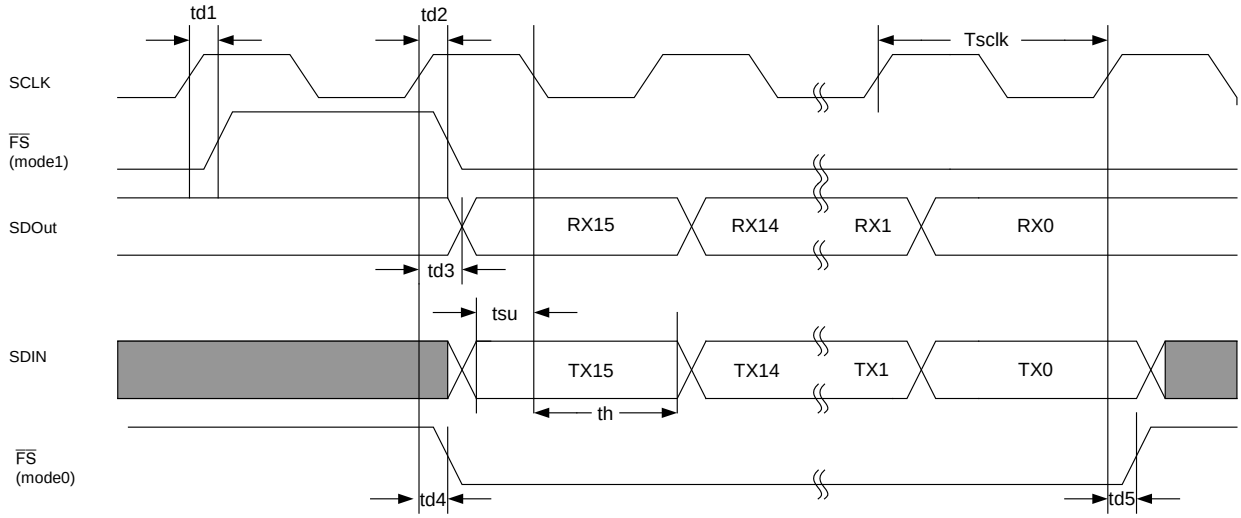


Figure 11: Serial Port Data Timing

8.4 Analog Specifications

8.4.1 DC Specifications

VREF should be connected to an external bypass capacitor with a minimum value of 0.1 µF. This pin is not intended for any other external use.

Table 15: Reference Voltage Specifications

Parameter	Test Condition	Min	Nom	Max	Units
VREF	VDD= 3.0 V - 3.6 V.		1.36		V
VREF Noise	300Hz-3.3 kHz		-86	-80	dBm_{600}
VREF PSRR	300Hz-30 kHz	40*			dB

8.4.2 AC Specifications

Table 16 shows the maximum transmit levels that the output drivers can deliver before distortion through the DAA starts to become significant. The loss though the DAA transmit path is assumed to be 7 dB. The signals presented at TXAP and TXAN are symmetrical. The transmit levels can be increased by setting either TXBST0 (+1.5 dB) or/and TXBST1 (+0.83 dB) for the combined total gain of 2.33 dB. These can be used where higher-level DTMF tones are required.

Table 16: Maximum Transmit Levels

Transmit Type	Maximum Different Line Level (dBm0)	Maximum Single-Ended Level at TXA Pins (dBm)	Peak to rms Ratio	Single-Ended rms Voltage at TXA Pins (V)	Single-Ended Peak Voltage at TXA Pins (v)
VPA=2.7 V to 3.6 V. All rms and peak voltages are relative to VREF.					
V.90	-12.0	-11.0	4	0.2175	0.87
QAM	-7.3	-6.3	2.31	0.377	0.87
DPSK	-5.1	-4.1	1.81	0.481	0.87
FSK	-3.0	-2.0	1.41	0.616	0.87
DTMF (high tone)	-7.8	-6.8	1.41	0.354	0.500
DTMF (low tone)	-9.8	-8.8	1.41	0.283	0.400

8.5 Performance

8.5.1 Receiver

Table 17: Receiver Performance Specifications

Parameter	Test Conditions	Min	Nom	Max	Units
Input Impedance	Measured at RXAP/N relative to VREF RXPULL=HI		230		kΩ
	Measured at RXAP/N relative to VREF RXPULL=LO	1.0			MΩ
Receive Gain Boost	Rxgain = 1; 1 kHz; RXAP/N=0.116 $V_{pk-diff}$ Gain Measured relative to Rxgain=0 RXGAIN=1 for Fs=8 kHz RXGAIN =1 for Fs=12 kHz RXGAIN =1 for Fs=14.4 kHz	 17.0 16.2 15.7	 18.5 17.4 17.2	 20.0 18.7 18.7	 dB dB dB
Total Harmonic Distortion (THD)	THD = 2nd and 3rd harmonic. RXGAIN =1	64	70		
RXG Gain	Gain Measured relative to RXG[1:0]=11 (0 dB) @1 kHz RXG[1:0]=00 RXG[1:0]=01 RXG[1:0]=10	 5.8 8.8 11.8	 6 9 12	 6.2 9.2 12.2	 dB dB dB
Passband Gain	Input 1.16 $V_{pk-diff}$ at RXA. Measure gain at 0.5 kHz, and 2 kHz. Normalized to 1 kHz. Gain at 0.5 kHz Gain at 1 kHz (Normalized) Gain at 2.0 kHz	 -0.29 **-0.067**	 -0.042 0.000 0.183	 0.21 0.43	 dB dB dB
Input offset	Short RXAP to RXAN. Measure input voltage relative to VREF	-30	0	30	mV
Sigma-Delta ADC Modulation gain	Normalized to VBG=1.25 V. Includes the effect of AAF(-0.4 dB) with Bits 1, 0 of CTRL2 register (01h) = 00.		41		µV/bit
Maximum Analog Signal Level at RXAP/RXAN	Peak voltage measured differentially across RXAP/RXAN.			1.16	$V_{pk-diff}$
Total Harmonic Distortion (THD)	1 kHz 1.16 $V_{pk-diff}$ at RXA with Rxg=11 THD = 2nd and 3rd harmonic.	80	85		dB
Noise	Transmit V.22bis low band; FFT run on ADC samples. Noise in 0 to 4 kHz band		-85	-80	dBm
Crosstalk	0 dBm 1000Hz sine wave at TXAP; FFT on Rx ADC samples, 1st four harmonics Reflected back to receiver inputs.		-100		dB

Note: RXG[1:0] and RXGAIN are assumed to have settings of '0' unless they are specified otherwise.

8.5.2 Transmitter

Table 18: Transmitter Performance Specifications

Parameter	Test Condition	Min	Nom	Max	Units
DAC gain (Transmit Path Gain)	Code word of ± 32,767 @1 kHz; TXBST0=0; TXBST1=0		70		µv/bit
DC offset –Differential Mode	Across TXAP and TXAN for DAC input = 0	-100		100	mV
DC offset -Common Mode	Average of TXAP and TXAN for DAC input = 0; relative to VREF	-80		80	mV
TXBST0 Gain	Code word of ± 32,767 @1 kHz; relative to TXBST0=0; TXBST1=0		1.65		dB
TXBST1 Gain	Code word of ± 32,767 @1 kHz; relative to TXBST0=0; TXBST1=0		1.335		dB
Total Harmonic Distortion (THD)	Code word of ± 32,767 @1 kHz; relative to TXBST0=0;TXBST1=0 THD = 2nd and 3rd harmonic.	-75	-85		dB
	Code word of ± (32,767*0.8) @1 kHz; relative to TXBST0=0;TXBST1=0 THD = 2nd and 3rd harmonic.	-80	-85		dB
1200 Ω Resistor across TNAN/TXAP	Code word of ± (32,767*0.9) @1 kHz; relative to TXBST0=1;TXBST1=1 THD = 2nd and 3rd harmonic.	-60	-70		dB
	Code word of ± 32,767 @1 kHz; relative to TXBST0=1;TXBST1=1 THD = 2nd and 3rd harmonic		-70		
Intermod Distortion	At output (TXAP-TXAN): DTMF 1.0 kHz, 1.2 kHz sine waves, summed 2.0 V_{pk} (-2 dBm tone summed with 0 dBm tone) Refer to TBR 21 specifications for description of complete requirements.		70		dB below low tone
Idle Channel Noise	200 Hz - 4.0 kHz		110		µV
PSRR	-30 dBm signal at VPA 300 Hz – 30kHz			40	dB
Passband Ripple	300 Hz - 3.2kHz	-0.125		0.125	dB
Transmit Gain Flatness	Code word of ± 32,767 @1 kHz. Measure gain at 0.5 kHz, and 2 kHz relative to 1 kHz.				
	Gain at 0.5 kHz		0.17		dB
	Gain at 1 kHz (Normalized)		0		dB
	Gain at 2.0 kHz		0.193		dB
	Gain at 3.3 kHz		-0.12		dB

Parameter	Test Condition	Min	Nom	Max	Units
TXAP/N Output Impedance Differentially (TXDIS=1)	TXDIS=1 Measure impedance differentially between TXAP and TXAN.		160		kΩ
TXAP/N Common Output Offset (TXDIS=1)	TXDIS=1 Short TXAP and TXAN. Measure the voltage respect to Vbg.	-20	0	20	mV

Note: TXBST0 and DTMFBS are assumed to have setting 0's unless they are specified otherwise.

9 Pinouts

9.1 32-Pin QFN Pinout

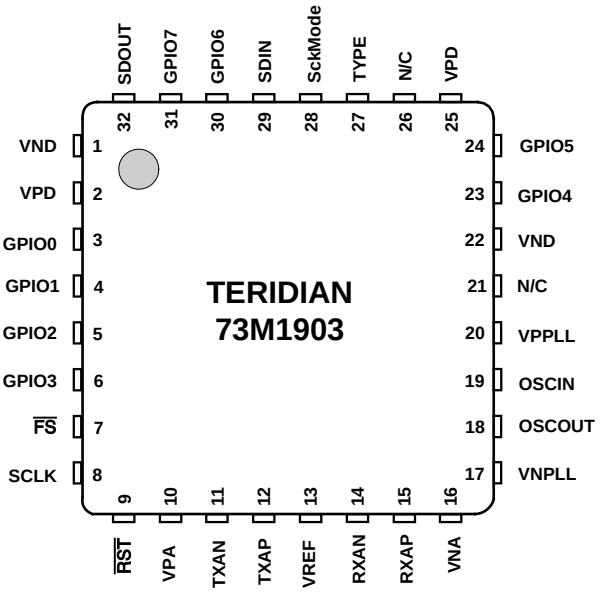


Figure 12: 32-Pin QFN Pinout

Table 19: 32-Pin QFN Pin Definitions

Pin	Name	Pin	Name
1	VND	17	VNPLL
2	VPD	18	OSCOUT
3	GPIO0	19	OSCIN
4	GPIO1	20	VPPLL
5	GPIO2	21	CLKOUT
6	GPIO3	22	VND
7	$\overline{FS}$	23	GPIO4
8	SCLK	24	GPIO5
9	$\overline{RST}$	25	VPD
10	VPA	26	N/C
11	TXAN	27	TYPE
12	TXAP	28	SckMode
13	VREF	29	SDIN
14	RXAN	30	GPIO6
15	RXAP	31	GPIO7
16	VNA	32	SDOUT

9.2 20-Pin TSSOP Pinout

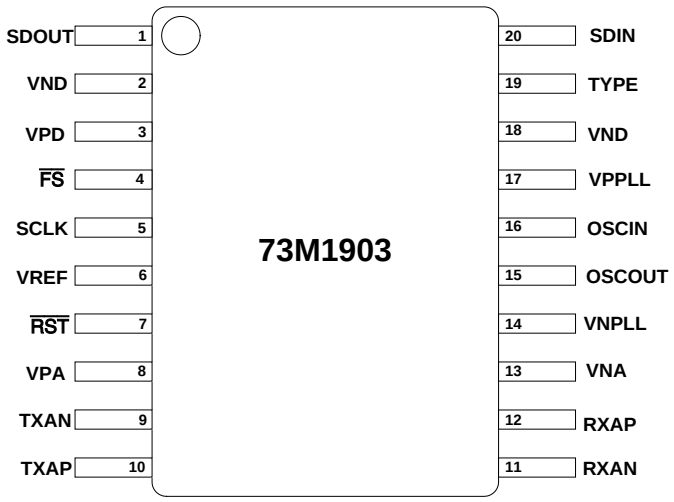


Figure 13: 20-Pin TSSOP Pinout

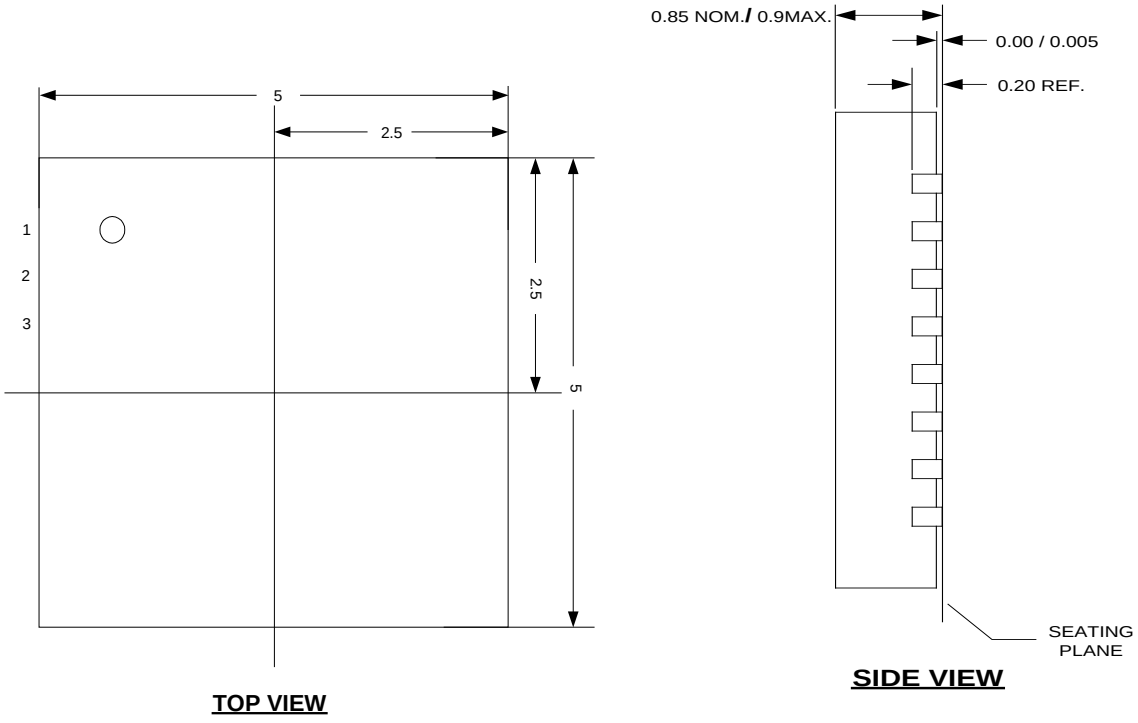
Table 20: 20-Pin TSSOP Pin Definitions

Pin	Name	Pin	Name
1	SDOUT	11	RXAN
2	VND	12	RXAP
3	VPD	13	VNA
4	$\overline{FS}$	14	VNPLL
5	SCLK	15	OSCOUT
6	VREF	16	OSCIN
7	$\overline{RST}$	17	VPPLL
8	VPA	18	VND
9	TXAN	19	TYPE
10	TXAP	20	SDIN

10 Mechanical Specifications

10.1 32-Pin QFN Mechanical Drawings

Dimensions in mm.



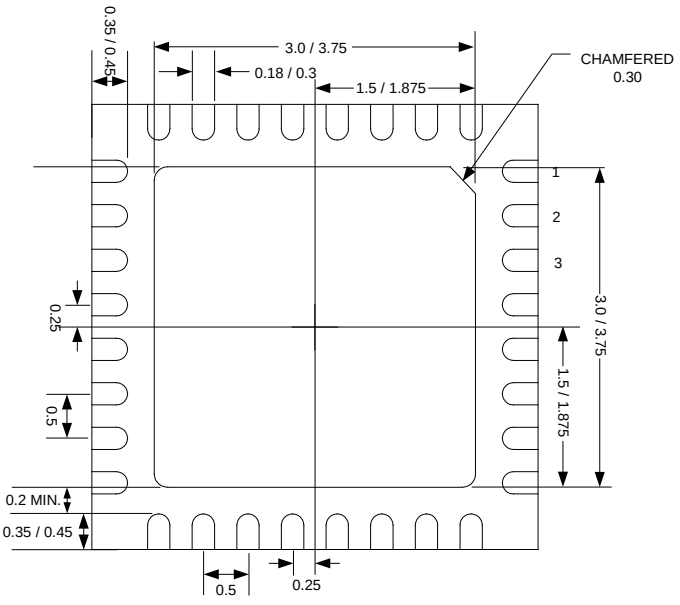
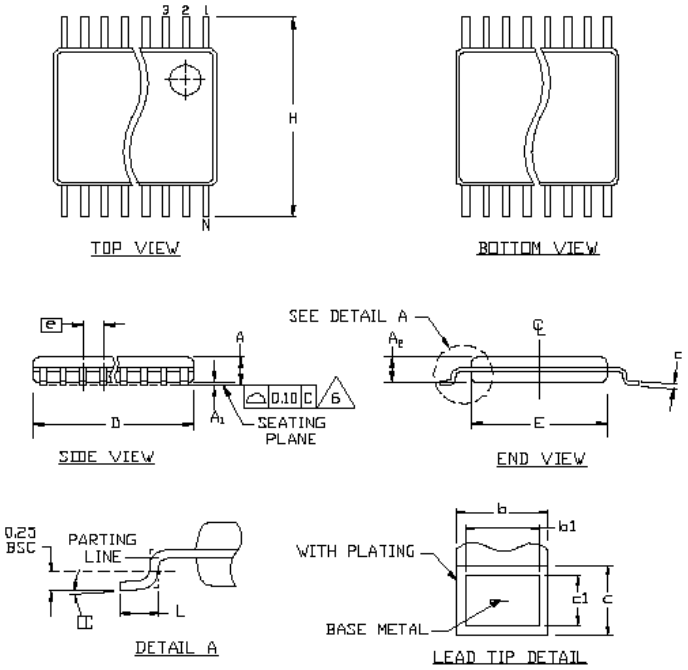


Figure 14: 32-Pin QFN Mechanical Specifications

10.2 20-Pin TSSOP Mechanical Drawings

Dimensions in mm.



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_e	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

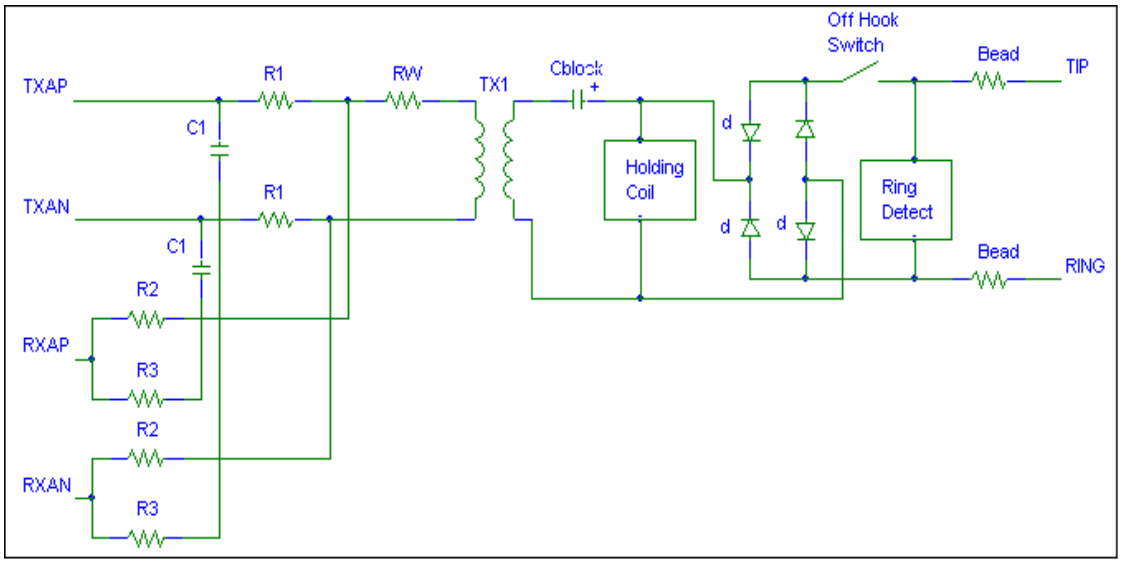
JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

Figure 15: 20-Pin TSSOP Mechanical Specifications

11 Ordering Information

Part Description	Order Number	Package Mark
73M1903 32-Lead QFN Lead Free	73M1903-IM/F	73M1903-M
73M1903 32-Lead QFN, Tape and Reel, Lead Free	73M1903-IMR/F	73M1903-M
73M1903 20-Lead TSSOP Lead Free	73M1903-IVT/F	73M190IVT
73M1903 20-Lead TSSOP, Tape and Reel, Lead Free	73M1903-IVTR/F	73M190IVT

Appendix A – 73M1903 DAA Resistor Calculation Guide



The following procedure can be used to approximate the component values for the DAA. The optimal values will be somewhat different due to the effects of the reactive components in the DAA (this is a DC approximation). Simulations with the reactive components accurately modeled will yield optimal values. The procedures for calculating the component values in the DAA are as follows. First set up R1. The DAA should be designed to reflect 600 Ω when looking in at TIP/RING. If the transformer is 1 to 1, the holding coil and ring detect circuit are high impedance, Cblock is a high value so in the frequency band of interest it is negligible, the sum of R2 and R3 is much greater than R1, and the output impedance of the drivers driving TXAP/TXAN are low then:

$$Rin = 2 \cdot R1 + RW + Rohswitch + 2 \cdot Rbead$$

RW is the sum of the winding resistance of both sides of the transformer. Measure each side of the transformer with an Ohmmeter and sum them.

Rohswitch is the on resistance of the Off Hook Switch. Mechanical Relay switches can be ignored, but Solid State Relays sometimes have an appreciable on resistance.

Rbead is the DC resistance of whatever series RF blocking devices may be in the design.

For Rin equal to 600 Ω:

$$R1 = \frac{600 - RW - Rohswitch - 2 \cdot Rbead}{2}$$

To maximize THL (Trans-Hybrid Loss), or to minimize the amount of transmit signal that shows up back on the Receive pins. The RXAP/RXAN pins get their DC bias from the TXAP/TXAN pins. By capacitively coupling the R3 resistors with the C1 caps, the DC offset can be minimized from the TXAP/TXAN to the RXAP/RXAN because the DC offset will be divided by the ratio of the R1 resistors to the winding resistance on the one side of the transformer.

Next make the sum of R2 + R3 much higher than 600 Ω. Make sure they are lower than the input impedance of the RXAP/RXAN pins; otherwise they can move the frequency response of the input filter. So let R2 + R3 = 100K.

$$R3 = \frac{100\ K}{1 + \frac{Rwtot + 600}{1200}}$$

where

$$Rwtot = RW + Rohswitch + 2 \cdot Rbead$$
$$R2 = 100\ K - R3$$

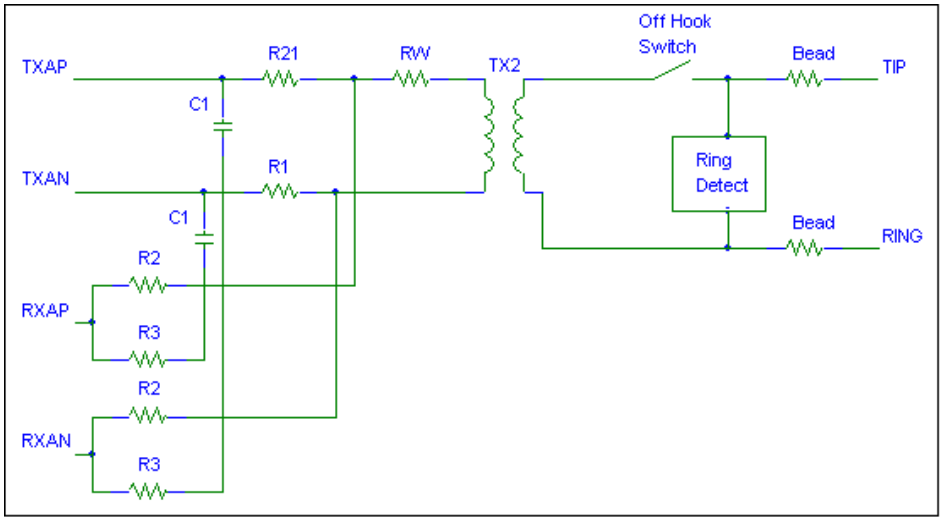
Use 1% resistors for R1, R2, and R3
To select the value for C1, make the zero at around 10Hz.

$$\frac{1}{2 \cdot \pi \cdot 100\ K \cdot C1} = 10$$
$$C1 = \frac{1}{2 \cdot \pi \cdot 100\ K \cdot 10}$$
$$C1 = 0.15\ uF$$

The blocking cap Cblock should also have the same frequency response, but due to the low impedance, its value will be much higher, usually requiring a polarized cap. A blocking cap may also be needed on the modem side of the transformer if the DC offset current of the transmit pins will exceed the current rating of the transformer.

$$Cblock = \frac{1}{2 \cdot \pi \cdot 600 \cdot 10}$$
$$Cblock = 27\ uF$$

If you are using a Wet transformer design, as in the following figure:



The only difference is that the blocking capacitor, Cblock, it is removed. All other equations still hold true.

Trans-Hybrid Loss (THL)

Trans-Hybrid Loss is by definition the loss of transmit signal from Tip/Ring to the receive inputs on the modem IC. This definition is only valid when driving a specific phone line impedance. In reality, phone line impedances are never perfect, so this definition isn't of much help. Instead, as an alternate definition that helps in analysis for this modem design, THL is the loss from the transmit pins to the receive pins. In this definition the worst-case THL from the transmit pins to the Receive pins is 10.8 dB. An insertion loss of 7 dB is assumed accounting for losses due to switch, bridge and transformer.

Appendix B – Crystal Oscillator

The crystal oscillator is designed to operate over wide choice of crystals (from 9 MHz to 27 MHz). The crystal oscillator output is input to an NCO based pre-scaler (divider) prior to being passed onto an on-chip PLL. The intent of the pre-scaler is to convert the crystal oscillator frequency, Fxtal, to a convenient frequency to be used as a reference frequency, Fref, for the PLL. A set of three numbers– Pdvsr (5 bit), Prst (3 bit) and Pseq (8 bit) must be entered through the serial port as follows:

Pdvsr = Integer [Fref/Fxtal];
Prst = Denominator of the ratio (Fref/Fxtal) minus 1 when it is expressed as a ratio of two smallest integers = Nnco1/Dnco1;
Pseq = Divide Sequence

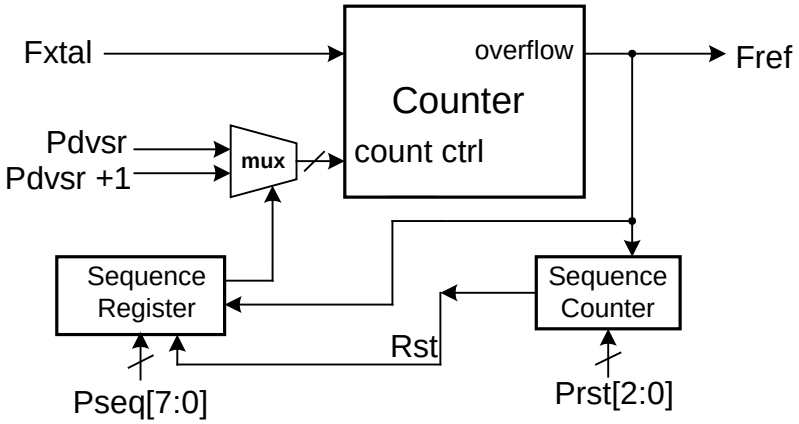


Figure 16: NCO Block Diagram

Please note that in all cases, pre-scaler should be designed such that pre-scaler output frequency, Fref, is in the range of 2 ~ 4 MHz.

In the first example below, the exact divide ratio required is Fxtal/Fref = 15.625 =125/8. If a divide sequence of {÷16,÷16,÷15,÷16,÷16,÷15,÷16,÷15} is repeated, the effective divide ratio would be exactly 15.625. Consequently, Pdvsr of 15, the length of the repeating pattern, Prst = 8 –1 =7, and the pattern, {1,1,0,1,1,0,1,0}, where 0 means Pdvsr, or ÷15, and 1 means Pdvsr +1, or ÷16 must be entered as below.

Example 1:

Fxtal = 27 MHz, Fref = 1.728 MHz.
Pdvsr = Integer [Fxtal/Fref] = 15 =0Fh
Prst[2:0] = 8 – 1 = 7 from Fxtal/Fref = 15.625 =125/8;
Pseq = ÷16,÷16,÷15,÷16,÷16,÷15,÷16,÷15 => {1,1,0,1,1,0,1,0} =DAh.

In the second example, Fxtal/Fref =4.0. This is a constant divide by 4. Thus Pdvsr is 4, Prst = 1 –1 =0 and Pseq = {x,x,x,x,x,x,x,x).

Example 2:

Fxtal = 18.432 MHz, Fref = 2.304 MHz.
Pdvsr = Integer [Fxtal/Fref] = 8 = 8h;
Prst[2:0] = 1- 1 = 0 from Fref/Fxtal = 18.432/2.304 = 8/1;
Pseq = {x,x,x,x,x,x,x,x} = xxh

Example 3:

Fxtal = 24.576 MHz, fref = 2.4576 MHz.
Pdvsr = Integer [Fxtal/Fref] = 10 = Ah;
Prst[2:0] = 1- 1 = 0 from Fref/Fxtal = 24.576/2.4576 = 10/1;
Pseq = {x,x,x,x,x,x,x,x} = xxh

It is also important to note that when Fxtal/Fref is an integer the output of the pre-scaler is a straight frequency divider (example 2). As such there will be no jitter generated at Fref. However if Fxtal/Fref is a fractional number, Fref, at the output of the pre-scaler NCO would be exact only in an average sense (example 1) and there will be a certain amount of fixed pattern (repeating) jitter associated with Fref which can be filtered out by the PLL that follows by appropriately programming the PLL. It is important to note, however, that the fixed pattern jitter does not degrade the performance of the sigma delta modulators so long as its frequency is >> 4 kHz.

PLL

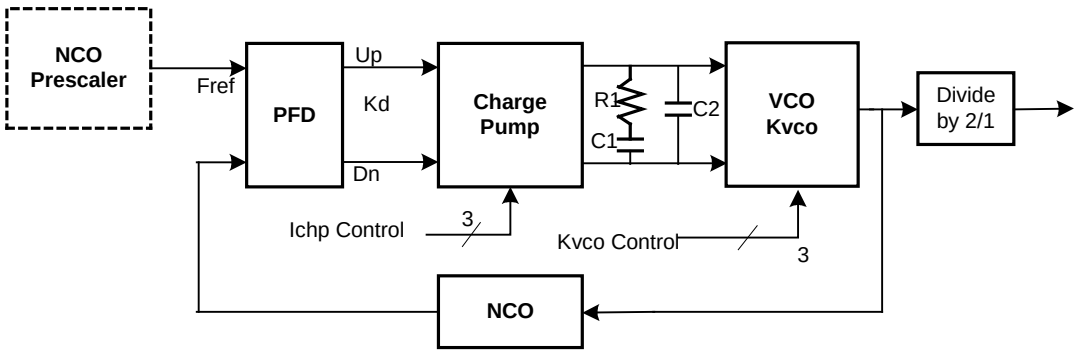


Figure 17: PLL Block Diagram

1903B has a built in PLL circuit to allow an operation over wide range of Fs. It is of a conventional design with the exception of an NCO based feedback divider. See Figure 17. The architecture of the 73m1903 dictates that the PLL output frequency, Fvco, be related to the sampling rate, fs, by fvco = 2 x 2304 x fs. The nco must function as a divider whose divide ratio equals Fref/Fvco.

Just as in the NCO pre-scaler, a set of three numbers– Ndvsr (7 bits), Nrst (3 bit) and Nseq (8 bits) must be entered through a serial port to effect this divide:

Ndvsr = Integer [Fref/Fxtal] ;
Nrst = denominator of the ratio (Fvco/Fref), Dnco1, minus 1, when it is expressed as a ratio of two smallest integers = Nnco1/Dnco1;
Nseq = Divide Sequence

Example 1:

Fs = 7.2 kHz or Fvco = 2 x 2304 x 7.2 kHz =33.1776 MHz, Fref = 1.728 MHz.
Ndvsr = Integer [Fvco/Fref] = 19
Nrst = 5 – 1 = 4 from Fvco/Fref = 19.2 = 96/5;
Nseq = ÷19, ÷19, ÷19, ÷19, ÷20 => {0,0,0,0,1} =xxx00001 = 01h.

Example 2:

Fs = 8.0 kHz or Fvco = 2 x 2304 x 8 kHz =36.864 MHz, Fref = 2.304 MHz.
Ndvsr = Integer [Fvco/Fref] = 16 = 10h;
Nrst= 1-1 = 0 from Fvco/Fref = 16/1;
Nseq = {x,x,x,x,x,x,x,x} = xxh.

Example 3:

Fs = 9.6 kHz or Fvco = 2 x 2304 x 9.6 kHz =44.2368 MHz, Fref = 2.4576 MHz.
Ndvsr = Integer [Fvco/Fref] = 18 = 16h;
Nrst= 1-1 = 0 from Fvco/Fref = 18/1;
Nseq = {x,x,x,x,x,x,x,x} = xxh.

It is important to note that in general the NCO based feedback divider will generate a fixed jitter pattern whose frequency components are at Fref/Accreset2 and its integer multiples. The overall jitter frequency will be a nonlinear combination of jitters from both pre-scaler and PLL NCO. The fundamental frequency component of this jitter is at Fref/Prst/Nrst. The PLL parameters should be selected to remove this jitter.

Three separate controls are provided to fine tune the PLL as shown in the following sections.

To ensure quick settling of PLL, a feature was designed into the 73m1903 where Ichp is kept at a higher value until lokdet becomes active or Frcvco bit is set to 1, whichever occurs first. Thus PLL is guaranteed to have the settling time of less than one frame synch period after a new set of NCO parameters had been written to the appropriate registers. The serial port register writes for a particular sample rate should be done in sequence starting from register 08h ending in register 0dh. 0dh register should be the last one to be written to. This will be followed by a write to the next register in sequence (0eh) to force the transition of Sysclk from Xtal to Pllclk.

Upon the system reset, the system clock is reset to Fxtal/9. The system clock will remain at Fxtal/9 until the host forces the transition, but no sooner the second frame synch period after the write to 0dh. When this happens, the system clock will transition to pllclk without any glitches through a specially designed deglitch mux.

Examples of NCO Settings

Example 1:

Crystal Frequency = 24.576 MHz; Desired Sampling Rate, Fs = 13.714 kHz(=2.4 kHz x 10/7 x 4)

Step 1. First compute the required VCO frequency, Fvco, corresponding to
Fs = 2.4 kHz x 10/7 x 4 = 13.714 kHz, or
Fvco = 2 x 2304 x Fs = 2 x 2304 x 2.4 kHz x 10/7 x 4 = 63.19543 MHz.

Step 2. Express the required VCO frequency divided by the Crystal Frequency as a ratio of two integers. This is initially given by:

$$Fvco / Fxtal = \frac{2 \bullet 2304 \bullet 2.4\text{kHz} \bullet 10/7 \bullet 4}{24.576MHz}.$$

After a few rounds of simplification this ratio reduces to:

$$Fvco / Fxtal = \frac{18}{7} = \left(\frac{1}{7}\right) \bullet \left(\frac{18}{1}\right)$$

$$= \frac{\frac{\text{Nnco1}}{\text{Dnco1}}}{\frac{\text{Nnco2}}{\text{Dnco2}}} = \frac{\frac{1}{7}}{\frac{1}{18}}$$

where Nnco1 and Nnco2 must be < or equal to 8.

The ratio, Nnco1/Dnco1 = 1/7, is used to form a divide ratio for the NCO in prescaler and Nnco2/Dnco2 = 1/18 for the NCO in the PLL.

Prescaler NCO: From Nnco1/Dnco1 = 1/7,
Pdvsr = Integer [Dnco1/Nnco1] = 7;
Prst[2:0] = Nnco1 – 1 = 0; this means NO fractional divide. It always does ÷7. Thus Pseq becomes "don't care" and is ignored.
Pseq = {x,x,x,x,x,x,x,x} = xxh.

PLL NCO: From Nnco2/Dnco2 = 1/18,
Ndvsr = Integer [Dnco2/Nnco2] = 18;
Nrst[2:0] = Nnco2 – 1 = 0; this means NO fractional divide. It always does ÷18. Thus Pseq becomes "don't care" and is ignored.
Nseq = {x,x,x,x,x,x,x,x} = xxh.

Example 2:

Crystal Frequency = 24.576 MHz; Desired Sampling Rate, Fs = 10.971 kHz=2.4 kHz x 8/7 x4

Step 1. First compute the required VCO frequency, Fvco, corresponding to
Fs = 2.4 kHz x 8/7 x 4 =10.971 kHz.
Fvco = 2 x 2304 x Fs = 2 x 2304 x 2.4 kHz x 8/7 x 4 = 50.55634 MHz.

Step 2. Express the required VCO frequency divided by the Crystal Frequency as a ratio of two integers. This is initially given by:

$$Fvco / Fxtal = \frac{2 \bullet 2304 \bullet 2.4\text{kHz} \bullet 8/7 \bullet 4}{24.576MHz}.$$

After a few rounds of simplification this ratio reduces to:

$$Fvco / Fxtal = \left(\frac{4}{35}\right) \bullet \left(\frac{18}{1}\right)$$

$$= \frac{\frac{\text{Nnco1}}{\text{Dnco1}}}{\frac{\text{Nnco2}}{\text{Dnco2}}} = \frac{\frac{4}{35}}{\frac{1}{18}}$$

, where Nnco1 and Nnco2 must be < or equal to 8.

The ratio, Nnco1/Dnco1 = 4/35, is used to form a divide ratio for the NCO in pre-scaler and Nnco2/Dnco2 =1/18 for the NCO in the PLL.

Pre-scaler NCO: From Nnco1/Dnco1 = 4/35,
Pdvsr = Integer [Dnco1/Nnco1] = 8;
Prst[2:0] = Nnco1 – 1 = 3;
Dnco1/Nnco1 = 35/4 = 8.75 suggests a divide sequence of {÷9,÷9,÷9,÷8}, or
Pseq = {x,x,x,x,1,1,1,0} = xDh.

PLL NCO: From Nnco2/Dnco2 = 1/18,
Ndvsr = Integer [Dnco2/Nnco2] = 18;
Nrst[2:0] = Nnco2 – 1 = 0; this means NO fractional divide. It always does ÷18. Thus Pseq becomes "don't care".
Nseq = {x,x,x,x,x,x,x,x} = xxh.

Example 3:

Crystal Frequency = 27 MHz; Desired Sampling Rate, Fs = 7.2 kHz

Step 1. First compute the required VCO frequency, Fvco, corresponding to
Fs = 2.4 kHz x 3 = 7.2 kHz.
Fvco = 2 x 2304 x Fs = 2 x 2304 x 2.4 kHz x 3 = 33.1776 MHz.

Step 2. Express the required VCO frequency divided by the Crystal Frequency as a ratio of two integers. This is initially given by:

$$Fvco / Fxtal = \frac{2 \bullet 2304 \bullet 2.4\text{kHz} \bullet 3}{27MHz}.$$

After a few rounds of simplification this reduces to:

$$Fvco / Fxtal = \left(\frac{8}{125}\right) \bullet \left(\frac{96}{5}\right)$$

$$= \frac{\frac{Nnco1}{Dnco1}}{\frac{Nnco2}{Dnco2}} = \frac{\frac{8}{125}}{\frac{5}{96}}$$

The two ratios are not unique and many other possibilities exist. But for this particular application, they are found to be the best set of choices within the constraints of Prst and Nrst allowed. (Nnco1, Nnco2 must be less than or equal to 8.)

The ratio, Nnco1/Dnco1 = 8/125, is used to form a divide ratio for the NCO in prescaler and Nnco2/Dnco2 =5/96 for the NCO in the PLL.

Pre-scaler NCO: From Nnco1/Dnco1 = 8/125,
Pdvsr = Integer [Dnco1/Nnco1] = 15;
Prst[2:0] = Nnco1 – 1 = 7;
Dnco1/Nnco1 = 125/8 = 15.625 suggests a divide sequence of {÷16,÷16,÷15,÷16,÷16,÷15,÷16,÷15}, or
Pseq = {1,1,0,1,1,0,1,0} = DAh.
PLL NCO: From Nnco2/Dnco2 = 5/96,
Ndvsr = Integer [Dnco2/Nnco2] = 19;
Nrst[2:0] = Nnco2 – 1 = 4;
Dnco2/Nnco2 = 19.2 suggests a divide sequence of {÷19, ÷19, ÷19, ÷19, ÷20}, or
Nseq = {x,x,x,0,0,0,0,1} = x1h.

Revision History

Rev. #	Date	Comments
1.0	4/16/2004	First publication.
1.1	12/13/2004	Minor modification for format.
1.2	7/15/2005	Company logo change and minor modification for format.
1.3	9/14/2006	Corrected QFN pin-out drawing.
1.4	9/14/2006	Corrected QFN pin-out drawing.
1.5	5/23/2007	Added 20-VT package information.
1.6	12/14/2007	Changed 32-QFN from punched to SAWN. Removed the leaded package option.
1.7	1/17/2008	Changed the bottom view package dimension for 32-QFN package.
2.0	2/23/2009	Removed all references to the 32-pin TQFP package. Formatted to the new corporate standard.

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Teridian Semiconductor Corp., 6440 Oak Canyon, Suite 100, Irvine, CA 92618
TEL (714) 508-8800, FAX (714) 508-8877, http://www.teridian.com

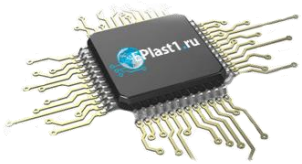
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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.