19-4541; Rev 1; 7/09

Quad-Channel, I²C-Margining IDACs with Three Channels of Power-Supply Tracking

General Description

The DS4426 contains four I²C-adjustable current DACs capable of sinking or sourcing current. External resistors set the full-scale range of each output. Each DAC output has 127 sink and 127 source steps that are programmed by the I²C interface. Power-supply tracking functionality is provided for three channels using dedicated control inputs. Once power-supply tracking is accomplished, the current outputs default to zero. Two address pins allow up to four DS4426 devices to exist on the same I²C bus.

Applications

Power-Supply Adjustment

Power-Supply Margining

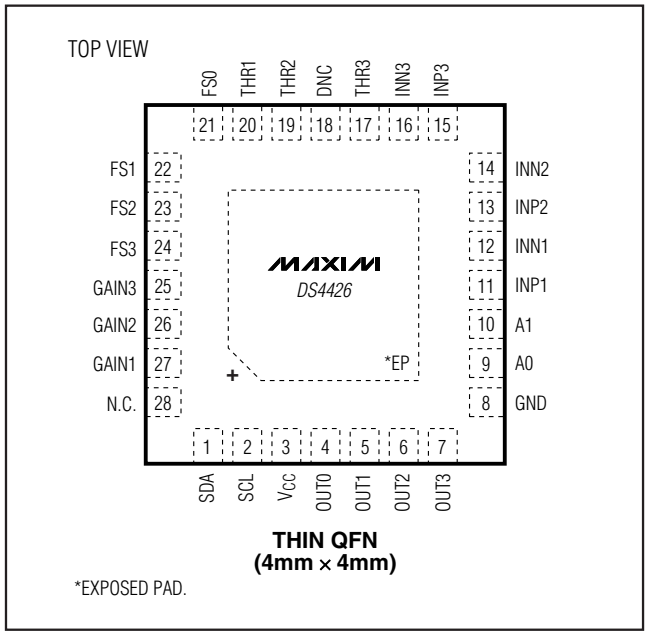
Power-Supply Tracking

Adjustable Current Sink or Source

Features

- **Four Current DACs**
  - **50µA to 200µA Adjustable Full-Scale Range**
  - **127 Settings Each for Sink and Source**
- **Power-Supply Tracking**
  - **Power-Supply Sequencing**
  - **Ramp-Up and Ramp-Down Tracking Control**
  - **Ratiometric Tracking Support**
- **+2.7V to +5.5V Operation**
- **I²C-Compatible Serial Interface**
- **Two Address Input Pins Allow Up to Four Devices on Same I²C Bus**
- **Lead-Free, 28-Pin TQFN Package (4mm x 4mm) with Exposed Pad**
- **Industrial Temperature Range: -40°C to +85°C**

Pin Configuration



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS4426T+	-40°C to +85°C	28 TQFN-EP*
DS4426T+T&R	-40°C to +85°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

Functional Diagram appears at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Quad-Channel, I²C-Margining IDACs with Three Channels of Power-Supply Tracking

ABSOLUTE MAXIMUM RATINGS

Voltage Range on SDA, SCL Relative to GND .....-0.5V to +6.0V
Voltage Range on V_{CC} Relative to GND .....-0.5V to +6.0V
Voltage Range on A0, A1, FS[3:0], GAIN[3:1], INN[3:1], INP[3:1], THR[3:1], and OUT[3:0] Relative to GND .....-0.5V to (V_{CC} + 0.5V)*

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

**Not to exceed +6.0V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.7		5.5	V
Input Logic 1 (SDA, SCL, A0, A1)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SDA, SCL, A0, A1)	V_{IL}		-0.3		0.3 x V_{CC}	V
Full-Scale Resistor Values	$R_{FS[3:0]}$	(Note 2)	40		160	kΩ

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	V_{CC} = +5.5V (Note 3)			0.9	mA
Input Leakage Current (SDA, SCL)	I_{IL}	V_{CC} = +5.5V	-1		+1	µA
RFS Voltage	V_{RFS}	T_A = +25°C	0.940	0.990	1.040	V
Reference Voltage	V_{REF}			1.24		V
Temperature Coefficient				±100		ppm/°C
Output Leakage Current (SDA)	I_L		-1		+1	µA
Output-Current Low (SDA)	I_{OL}	V_{OL} = +0.4V	3			mA
		V_{OL} = +0.6V	6			
I/O Capacitance	$C_{I/O}$				10	pF

DAC OUTPUT CURRENT CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Variation Due to Power-Supply Change		DC source, V_{OUT} measured at +1.2V		0.33		%/V
		DC sink, V_{OUT} measured at +1.2V		0.33		
Output Current Variation Due to Output-Voltage Change		DC source, V_{CC} = +3.6V		0.15		%/V
		DC sink, V_{CC} = +3.6V		0.30		

DAC OUTPUT CURRENT CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage for Sinking Current	$V_{OUT:SINK}$	(Note 4)	0.5		3.5	V
Output Voltage for Sourcing Current	$V_{OUT:SOURCE}$	(Note 4)	0		V_{CC} - 0.75	V
Full-Scale Sink Output Current	$I_{OUT:SINK}$	(Note 4)	50		200	µA
Full-Scale Source Output Current	$I_{OUT:SOURCE}$	(Note 4)	-200		-50	µA
Output-Current Full-Scale Accuracy	$I_{OUT:FS}$	T_A = +25°C			±5	%
Output-Current Temperature Coefficient	$I_{OUT:TC}$	(Note 5)		±130		ppm/°C
Output-Current Power-Supply Rejection Ratio				0.33		%/V
Output-Leakage Current at Zero Current Setting	I_{ZERO}		-1		+1	µA
Output-Current Differential Linearity	DNL	(Note 6)			0.5	LSB
Output-Current Integral Linearity	INL	(Note 7)			1	LSB

I²C ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C. Timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$. See Figure 6.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 8)	0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
START Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 9)	20 + 0.1C_B		300	ns
SDA and SCL Fall Time	t_F	(Note 9)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 9)			400	pF

Quad-Channel, I²C-Margining IDACs with Three Channels of Power-Supply Tracking

POWER-SUPPLY TRACKING CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, see Figure 5.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Divider Ratio	R_{DIV}	R_A/R_B and R_C/R_D	0.5		1	
Output Load	R_L	$R_L = (R_F \times R_E)/(R_F+R_E)$	1		20	kΩ
Feedback Resistor Ratio	R_F/R_B		0.5		4.5	
Gain Resistor	R_G		0.8		10	kΩ
Gain Setting Ratio	R_L/R_G		1.4		5	
Power-Supply Tracking Gain	G_{VI}	R_L/R_G = 2, R_L = 5kΩ, V_{CC} = +3.6V, T_A = +25°C		2.4		mA/V
		R_L/R_G = 5, R_L = 5kΩ, V_{CC} = +3.6V, T_A = +25°C	3.8	6.2	10	
Power-Supply Tracking Input Bias Current	I_B				1	µA
Power-Supply Tracking Input Voltage	V_{IN}	INP[3:1] and INN[3:1]	0		V_{CC} - 1.4	V
Unity Gain Bandwidth	GBW	R_L/R_G = 1.4; R_L = 5kΩ		12		MHz
Output Voltage While Tracking	$V_{OUT:TRK}$	Switch closed, V_{CC} = +3.0V, measured at OUT[3:1], R_L = 5kΩ	0		1.5	V
Output Current While Tracking	$I_{OUT:TRK}$	R_L/R_G = 1.4, R_G = 1kΩ, V_{CC} = +3.0V, V_{FB} = +0.8V			1	mA
Tracking Accuracy					±600	mV
Output Leakage	I_{BC}	Switch open			0.5	µA
Comparator Input Bias Current	I_{OFF}				1	µA
Comparator Input Offset	V_{OS}			±5		mV
Switch Delay	t_{DC}			5		µs
Comparator Hysteresis	V_{HYS}			12.5		mV

Note 1: All voltages are referenced to GND. Current entering the IC is specified positive, and current exiting the IC is negative.

Note 2: Input resistors ($R_{FS[3:0]}$) must be between the specified values to ensure the device meets its accuracy and linearity specifications.

Note 3: Supply current specified with all outputs set to zero current setting and with all inputs at V_{CC} or GND. SDA and SCL are connected to V_{CC}. Excludes current through R_{FS} resistors (I_{RFS}). Total current including I_{RFS} is I_{CC} + (2 x I_{RFS}).

Note 4: The output-voltage full-scale ranges must be satisfied to ensure the device meets its accuracy and linearity specifications. Only applies to current DAC operation, not power-supply tracking operation.

Note 5: Temperature drift excludes drift caused by external resistors.

Note 6: Differential linearity is defined as the difference between the expected incremental current increase with respect to position and the actual increase. The expected incremental increase is the full-scale range divided by 127.

Note 7: Integral linearity is defined as the difference between the expected value as a function of the setting and the actual value. The expected value is a straight line between the zero and the full-scale values proportional to the setting.

Note 8: Timing shown is for fast-mode operation (400kHz). This device is also backward-compatible with I²C standard-mode timing.

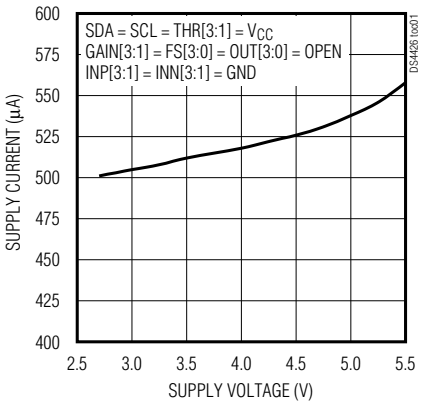
Note 9: C_B—Total capacitance of one bus line in pF.

Quad-Channel, I²C-Margining IDACs with Three Channels of Power-Supply Tracking

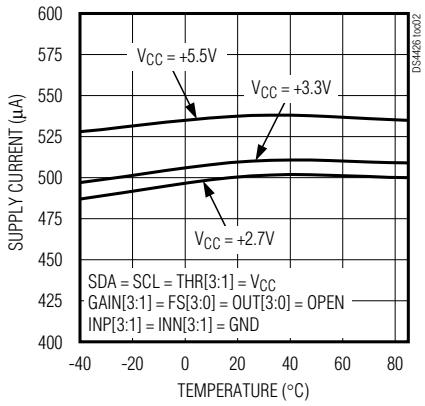
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

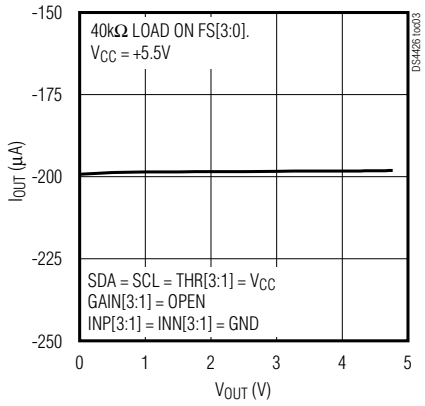
SUPPLY CURRENT vs. SUPPLY VOLTAGE



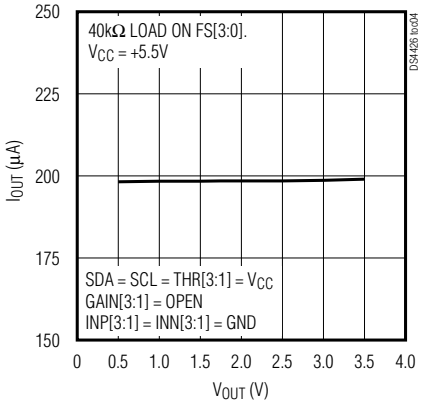
SUPPLY CURRENT vs. TEMPERATURE



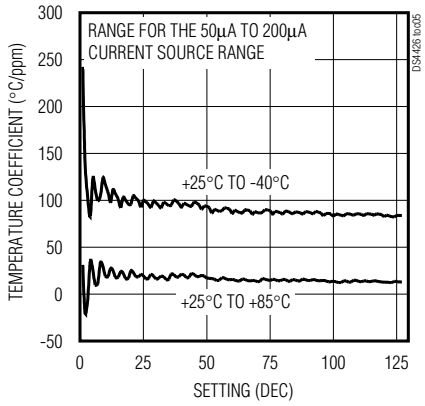
VOLTCO (SOURCE)



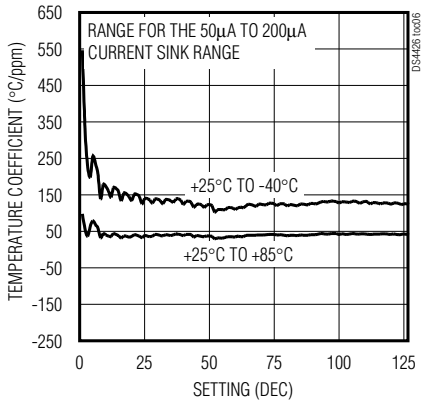
VOLTCO (SINK)



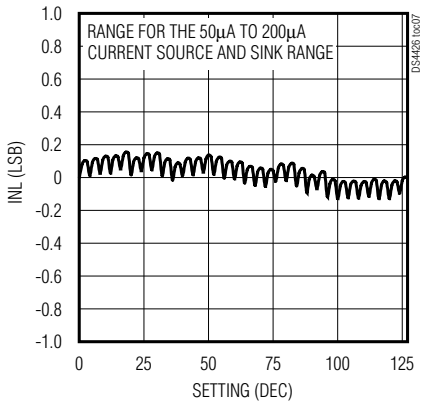
TEMPERATURE COEFFICIENT vs. SETTING (SOURCE)



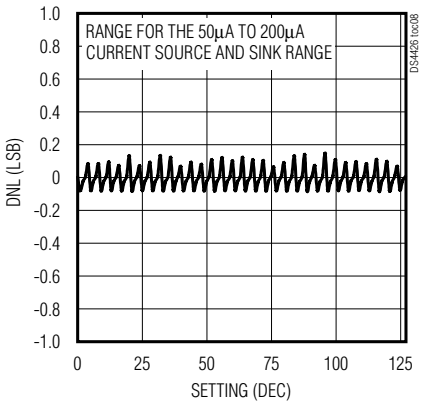
TEMPERATURE COEFFICIENT vs. SETTING (SINK)



INTEGRAL LINEARITY



DIFFERENTIAL LINEARITY



Quad-Channel, I²C-Margining IDACs with Three Channels of Power-Supply Tracking

Pin Description

PIN	NAME	FUNCTION
1	SDA	Serial Data Input/Output. I²C data pin.
2	SCL	Serial Clock Input. I²C clock input.
3	V_{CC}	Voltage Supply
4	OUT0	Current DAC Output
5, 6, 7	OUT1, OUT2, OUT3	Current DAC and Tracking Control Output
8	GND	Ground
9	A0	I²C Address Input 0
10	A1	I²C Address Input 1
11, 13, 15	INP1, INP2, INP3	Power-Supply Tracking Positive Input
12, 14, 16	INN1, INN2, INN3	Power-Supply Tracking Negative Input
17, 19, 20	THR3, THR2, THR1	Threshold Input. Comparator input used to set threshold for tracking enable/disable based on $V_{REF}/2$.
18	DNC	Do Not Connect
21–24	FS0, FS1, FS2, FS3	Full-Scale Calibration Input. A resistor-to-ground on this input determines full-scale output current on the associated output.
25, 26, 27	GAIN3, GAIN2, GAIN1	Gain Adjustment Pin. Connect a resistor between this pin and V_{CC}.
28	N.C.	No Connection
—	EP	Exposed Pad. No connection.

Detailed Description

The DS4426 contains four I²C-adjustable current sources that are each capable of sinking and sourcing current. Three of the current outputs (OUT[3:1]) also have power-supply tracking circuitry that allows additional current to be sourced during power-up.

Adjustable Current DACs

Each output (OUT[3:0]) has 127 sink and 127 source settings that are programmed through the I²C interface. The full-scale current ranges (and corresponding step sizes) of the outputs are determined by external resistors connected to the corresponding FS pins (see Figure 1). The formula to determine the external resistor values (R_{FS}) for each output is given by:

$$R_{FS} = \frac{V_{RFS}}{16 \times I_{FS}} \times 127$$

where I_{FS} is the desired full-scale current value, V_{RFS} is the R_{FS} voltage (see the *DC Electrical Characteristics* table), and R_{FS} is the external resistor value.

To calculate the output-current value (I_{OUT}) based on the corresponding DAC value (see Table 2 for corresponding memory addresses), use the following equation:

$$I_{OUT} = \frac{DACValue(dec)}{127} \times I_{FS}$$

On power-up, the DS4426 current DAC outputs are set to zero current. This is done to prevent the device from sinking or sourcing an incorrect current before the system host controller has a chance to modify its setting. Note, however, that if power-supply tracking is enabled (see the *Power-Supply Tracking Circuit* section), then the DS4426 can still source current at power-up.

When used in adjustable power-supply applications (see Figure 8), the DS4426 does not affect the initial power-up voltage of the supply because it defaults to providing zero output current on power-up unless power-supply tracking is enabled. As it sources or sinks current into the feedback voltage node, it changes the amount of output voltage required by the regulator to reach its steady-state operating point.

Quad-Channel, I²C-Margining IDACs with Three Channels of Power-Supply Tracking

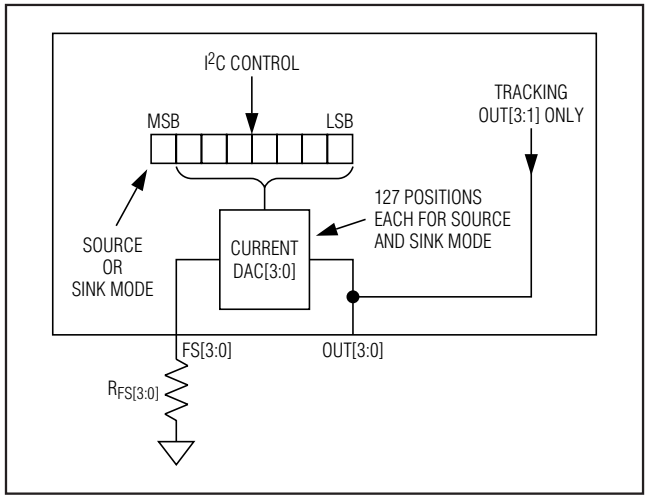


Figure 1. Current DAC Detail

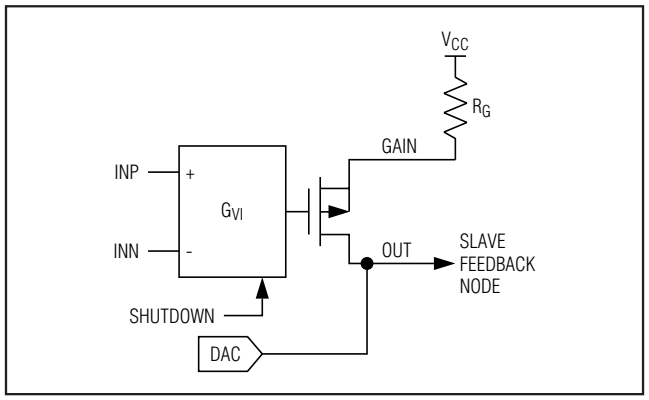


Figure 2. Gain Stage

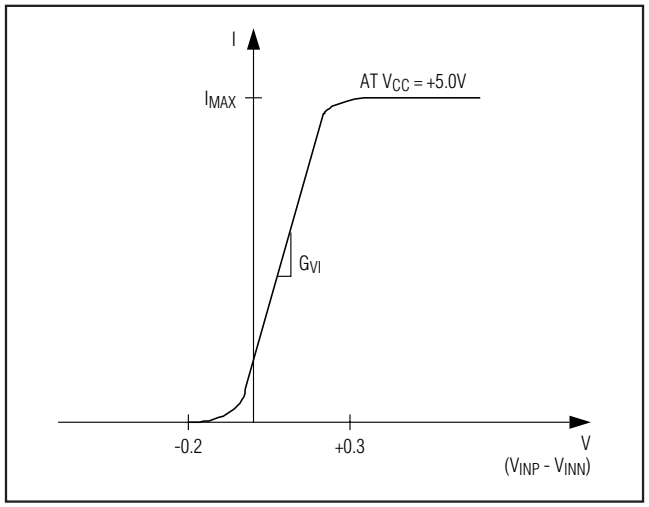


Figure 3. INP and INN Differential Inputs

Using the external resistors $R_{FS[3:0]}$ to set the output-current range, the DS4426 provides some flexibility for adjusting the impedances of the feedback network or the range over which the power supply can be controlled or margined.

As a source for biasing instrumentation or other circuits, the DS4426 provides a simple and inexpensive current source with an I²C interface for control. The adjustable, full-scale range allows the application to get the most out of its 7-bit sink or source resolution.

Power-Supply Tracking Circuit

By making use of the power-supply tracking circuitry, the DS4426 has the ability to source current on power-up. This current is additive with the current DAC source/sink currents and is determined by the value of the gain resistor, R_G, and the supply voltage, V_{CC}. This current is controlled by the voltages presented to the corresponding INP and INN pins, and the voltages presented to the corresponding threshold (THR) pins.

Maximum Source Current

The maximum current the DS4426 can source at power-up using the power-supply tracking circuitry depends on the value of the supply voltage, V_{CC}, and the gain resistor, R_G, connected from the corresponding GAIN pin to V_{CC}. The maximum current (I_{MAX}) that can be sourced to the corresponding OUT pin can be estimated using the following equation:

$$I_{MAX} \cong \frac{(V_{CC} - V_{OUT})}{R_G}$$

The power-supply tracking circuit can be estimated with Figure 2.

Inputs for Power-Supply Tracking: INP and INN

Each pair of power-supply tracking inputs, INP and INN, determines if and how much of the I_{MAX} current is sourced when the power-supply tracking circuit is enabled. When the difference between the voltage presented to INP (V_{INP}) and INN (V_{INN}) is more than approximately +0.3V, then the maximum source current, as determined by the value I_{MAX}, is sourced into the OUT pin connection. When the difference between V_{INP} and V_{INN} is less than approximately -0.2V, then no current is sourced into the corresponding OUT pin. The change in current from no current to I_{MAX} can be estimated by the power-supply tracking gain, G_{VI} (see the *Power-Supply Tracking Characteristics* table).

Figure 3 shows the typical current behavior of the power-supply tracking circuit with respect to the voltage difference seen at the INP and INN inputs.

Quad-Channel, I²C-Margining IDACs with Three Channels of Power-Supply Tracking

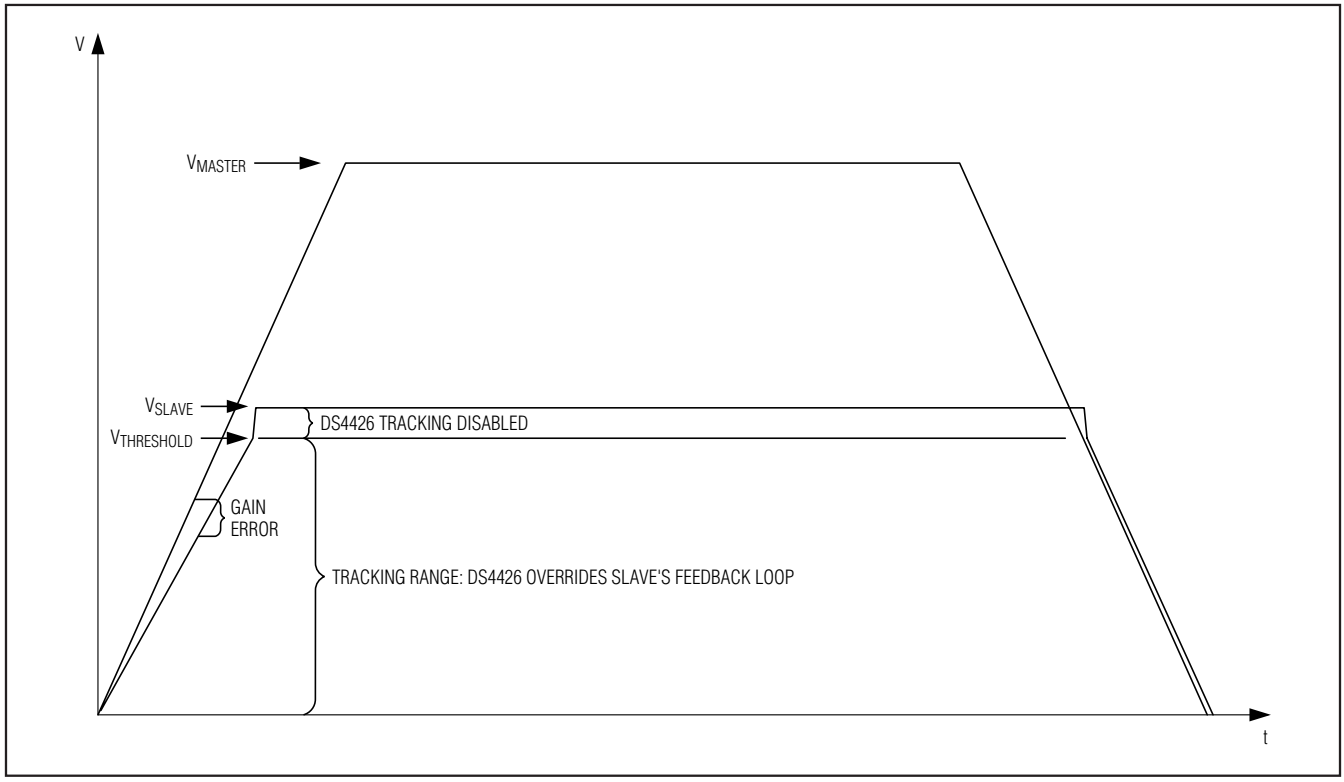


Figure 4. Enabling Power-Supply Tracking Using the THR Input

THR Inputs for Enabling Power-Supply Tracking

Comparators are used to individually enable/disable power-supply tracking based on the voltage presented to the corresponding THR pin relative to a fixed internal reference ($V_{REF}/2$ = +0.62V). Figure 4 shows a typical startup and shutdown plot based on the voltage presented to the THR pin. Tracking can be disabled by connecting the corresponding THR pin to a voltage greater than $V_{REF}/2$. Below this threshold, the tracking circuit is active.

Power-Supply Tracking in DC-DC Power Applications

The DS4426 provides several options for power-supply tracking control of DC-DC power supplies. In many cases, it is desirable to prevent certain DC-DC supplies from exceeding the voltage of other supplies. This is often the case with the voltages applied to a digital core and I/O. Each DS4426 supports one master with three slave DC-DCs. See Figure 5 for more information.

Loop Bandwidth Consideration

Power-supply tracking is used to override each slave DC-DC's feedback loop during power-up and power-down. Power-supply tracking is capable of slewing at a much faster rate than most DC-DC converters. Care must be exercised when selecting the loop bandwidth of the master DC-DC, slave DC-DC, and power-supply tracking control loop such that oscillations and overshoot are minimized.

While the slave DC-DC supplies are tracking the master DC-DC supply, there are three time constants of concern:

1) Master BW. The master DC-DC control loop bandwidth, power-up ramp rate, and power-down ramp rate.
2) Slave BW. The slave DC-DC supplies control loop bandwidths.
3) Tracking BW. The DS4426 tracking circuit bandwidth.

To ensure stable operation and minimize peaking, the bandwidths should follow the following rule:

Master BW and Slave BW < (Tracking BW/10)

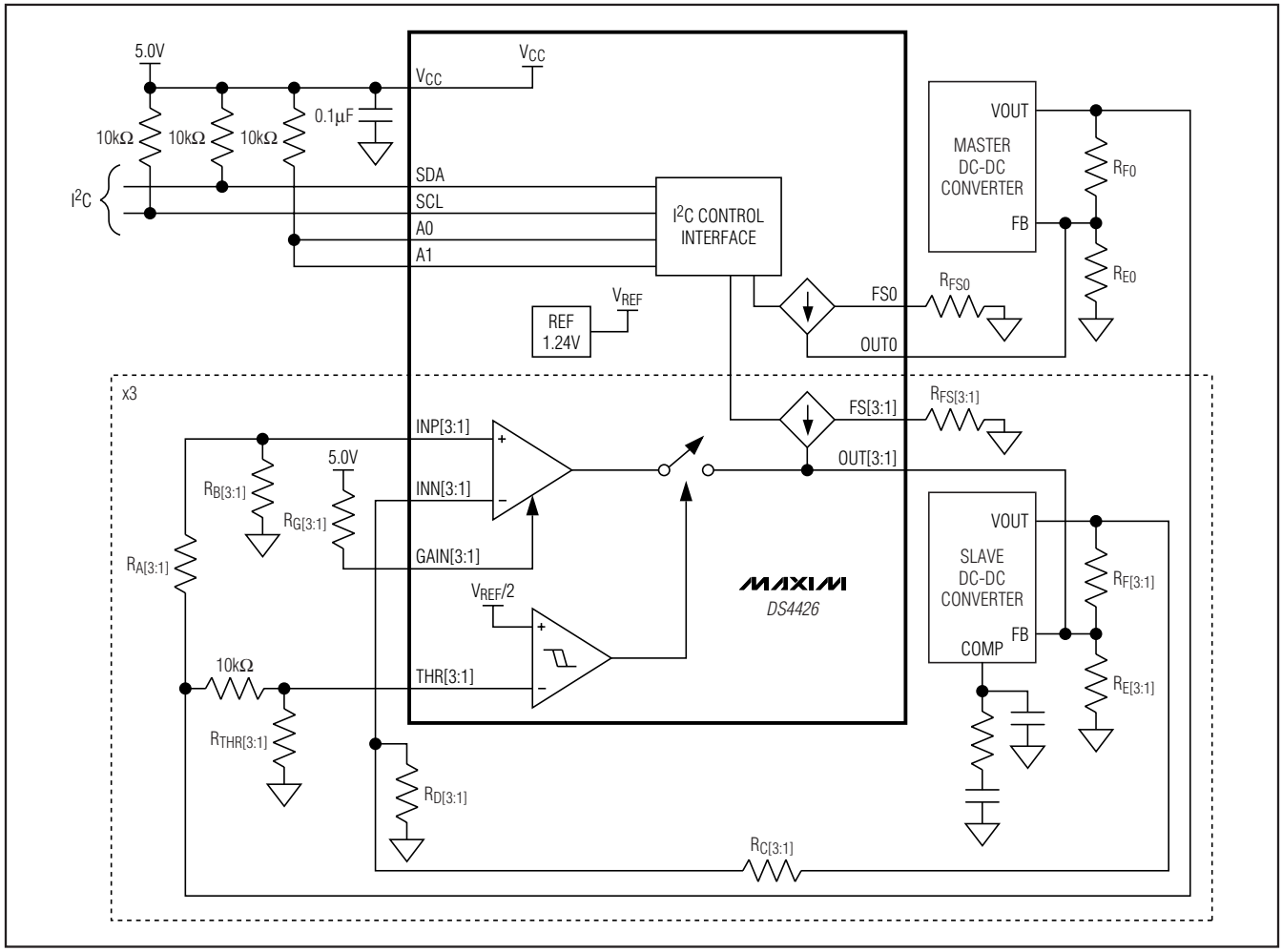


Figure 5. Typical DC-DC Power-Supply Tracking Application

Ratiometric Tracking

The DS4426 can maintain a defined ratio between a slave voltage and the master voltage where:

$$K_{SM} = V_{SLAVE}/V_{MASTER}.$$

In Figure 5, this ratio is given by the following:

$$K_{SM} = [R_{B[3:1]}/(R_{A[3:1]} + R_{B[3:1]})]/[R_{D[3:1]}/(R_{C[3:1]} + R_{D[3:1]})].$$

Nonratiometric tracking is the special case where $K_{SM} = 1$.

Power-Supply Tracking Loop Gain Stability

Slave DC-DC output tracking is controlled by the DS4426 sourcing current into the slave DC-DC's feedback loop. This changes the stability of the loop during tracking. The amount of gain used can be adjusted by changing the ratio of R_L/R_G. If oscillations occur, increasing R_G reduces gain and increases the system's phase margin. If the slave DC-DC has a compensation pin, the RC network connected to this pin can also be adjusted to improve phase margin. This pin is often labeled COMP or ITH. A larger compensation time constant (increased R and/or increased C) often increases the stability of the system during tracking; however, this also modifies the DC-DC's transient response. In order to prevent modification of the slave DC-DC's transient response after power-supply tracking is complete, R_G should first be modified before adjusting the compensation network. The higher the gain, the less the gain error. Reducing the gain increases the gain error during tracking. See Figure 4 for more information.

Quad-Channel, I²C-Margining IDACs with Three Channels of Power-Supply Tracking

Table 1. Slave Addresses

A1	A0	SLAVE ADDRESS (HEX)
GND	GND	90h
GND	V_{CC}	92h
V_{CC}	GND	94h
V_{CC}	V_{CC}	96h

Inputs for Tracking in DC-DC Power Applications

When enabling/disabling the power-supply tracking, a resistor-divider connected to the THR input sets the disable threshold (see $V_{THRESHOLD}$ in Figure 4). The top of the resistor-divider must be connected to the master DC-DC voltage for correct operation. Below this threshold, the tracking circuit is active.

Power-Supply Sequencing

The DS4426 can be used to perform power-supply sequencing. This is a subset of power-supply tracking with modifications to the external resistor network. The basic concept is that the DS4426 sources maximum current into the slave power supply's feedback node until a voltage in the system has risen above a specific voltage level. By sourcing the maximum current into the feedback node, the power supply's output is held off. Maximum sourcing current is achieved with two steps:

1) Apply the maximum allowed input voltage across INP and INN. Connect INP to V_{CC} - 1.4V using a voltage-divider to ground. Connect INN to ground.
2) Set the gain to the maximum allowed (R_L/R_G = 5).

The slave power supply is allowed to turn on once the voltage on THR is greater than $V_{REF}/2$. Use a resistor-divider connected to the rising system voltage to scale the trip point to $V_{REF}/2$.

I²C Slave Address

The DS4426 responds to one of four I²C slave addresses determined by the state of the input on the two address inputs. The two input states are connected to V_{CC} or connected to ground.

Table 2. Memory Addresses

MEMORY ADDRESS (HEX)	CURRENT SOURCE
F8h	OUT0
F9h	OUT1
FAh	OUT2
FBh	OUT3

Memory Organization

The DS4426's current sources are controlled by writing to memory addresses listed in Table 2.

The format of each of the output control registers is given by:

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
S	D_6	D_5	D_4	D_3	D_2	D_1	D_0

where:

BIT	NAME	DESCRIPTION	POWER-ON DEFAULT
S	Sign Bit	Determines if DAC sources or sinks current. For sink, S = 0. For source, S = 1.	0b
Dx	Data	7-bit data word controlling DAC output. Setting 0000000b outputs zero current regardless of the state of the sign bit.	0000000b

For example:

R_{FS0} = 80kΩ and register 0xF8h is written to a value of 0xAAh. Use the following formula to calculate the output current:

$$I_{FS} = (1.0V/80k\Omega) \times (127/16) = 99.22\mu A$$

The MSB of the output register is 1, so the output is sourcing the value corresponding to position 2Ah (42 decimal). The magnitude of the output current is equal to the following:

$$99.22\mu A \times (42/127) = 32.8125\mu A$$

I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers:

I²C Slave Address: The slave address of the DS4426 is determined by the state of the A0 and A1 pins (see Table 1).

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states. When the bus is idle it often initiates a low-power mode for slave devices.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 3 for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 3 for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 6 for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL, plus the setup-and-hold time requirements (Figure 6). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time (Figure 6) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse, and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An Acknowledgement (ACK) or Not Acknowledge (NACK) is always the ninth bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the ninth bit. A device performs a NACK by transmitting a 1 during the ninth bit. Timing for the ACK and NACK is identical to all other bit writes (Figure 6). An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit-write definition, and the acknowledgement is read using the bit-read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit-read definition, and the master transmits an ACK using the bit-write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit. The DS4426's slave address is determined by the state of the A0 and A1 pins (see Table 1). When the R/$\overline{W}$ bit is 0 (such as in 90h), the master is indicating it will write data to the slave. If R/$\overline{W}$ = 1 (91h in this case), the master is indicating it wants to read from the slave. If an incorrect slave address is written, the DS4426 assumes the master is communicating with another I²C device and ignores the communication until the next START condition is sent.

Memory Address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

Quad-Channel, I²C-Margining IDACs with Three Channels of Power-Supply Tracking

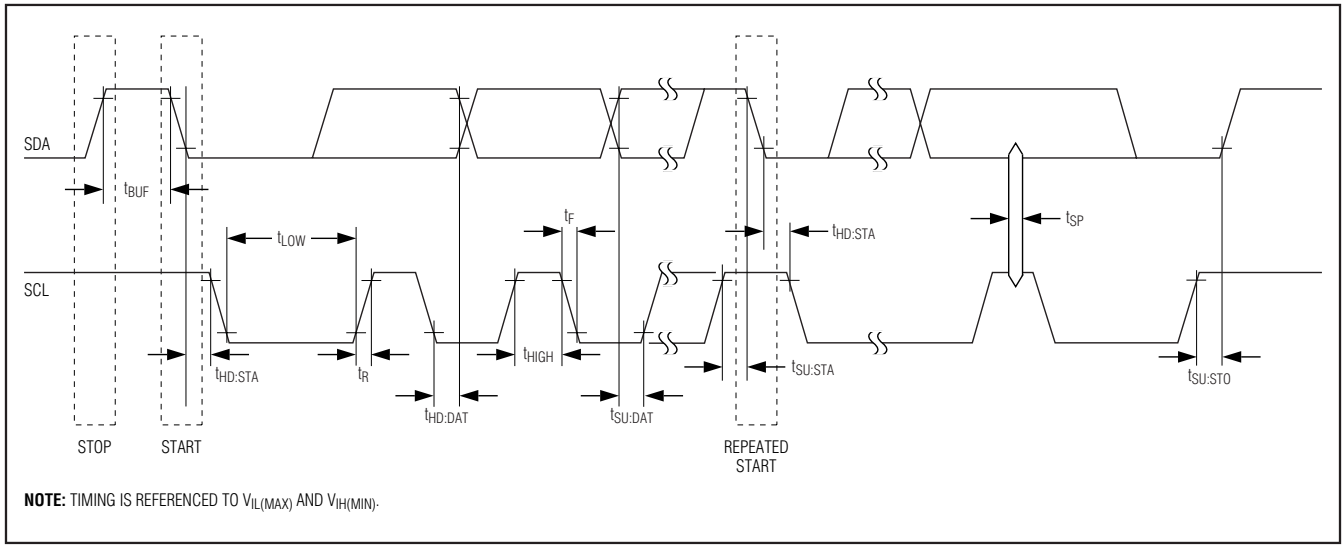


Figure 6. I²C Timing Diagram

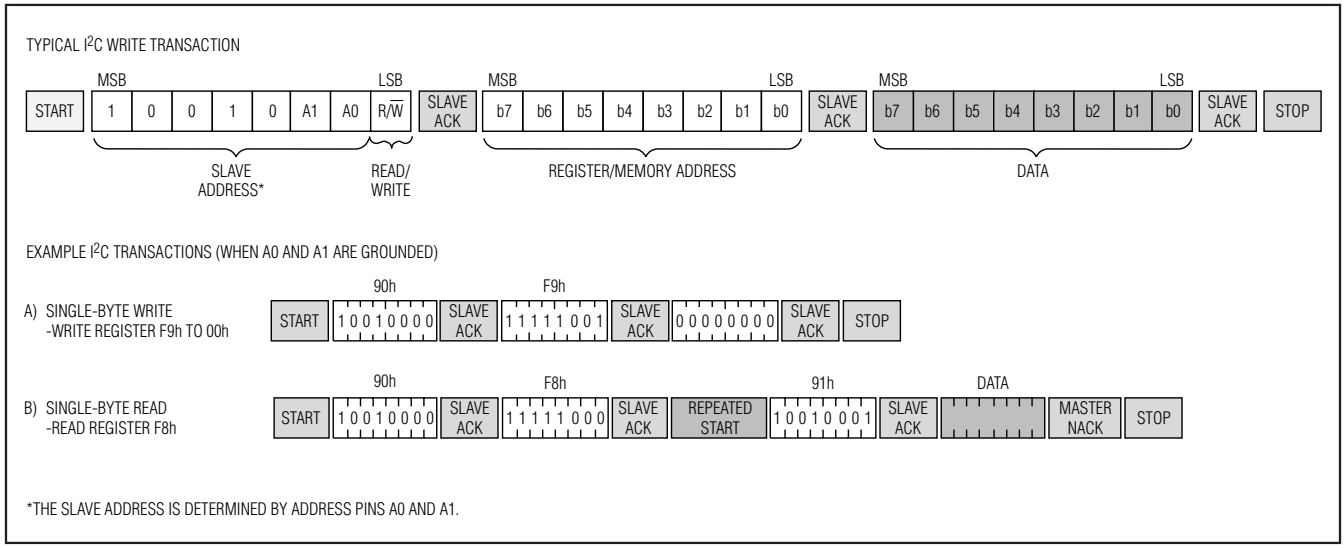


Figure 7. I²C Communication Examples

I²C Communication

Writing to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember that the master must read the slave's acknowledgement during all byte-write operations.

Reading from a Slave: To read from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition.

Applications Information

Example Calculations for an Adjustable Power Supply

In this example, the circuit shown in Figure 8 is used to margin a +2.0V supply by ±20%. The margined power supply has a DC-DC converter output voltage, V_{OUT}, of +2.0V and a DC-DC converter feedback voltage, V_{FB}, of +0.8V. To determine the relationship of R_{0A} and R_{0B}, start with the equation:

$$V_{FB} = \frac{R_{0B}}{R_{0A} + R_{0B}} \times V_{OUT}$$

Substituting V_{FB} = +0.8V and V_{OUT} = +2.0V, the relationship between R_{0A} and R_{0B} is determined to be:

$$R_{0A} = 1.5 \times R_{0B}$$

I_{OUT0} is chosen to be 100µA (midrange source/sink current for the DS4426). Summing the currents into the feedback node, we have the following:

$$I_{OUT0} = I_{R0B} - I_{R0A}$$

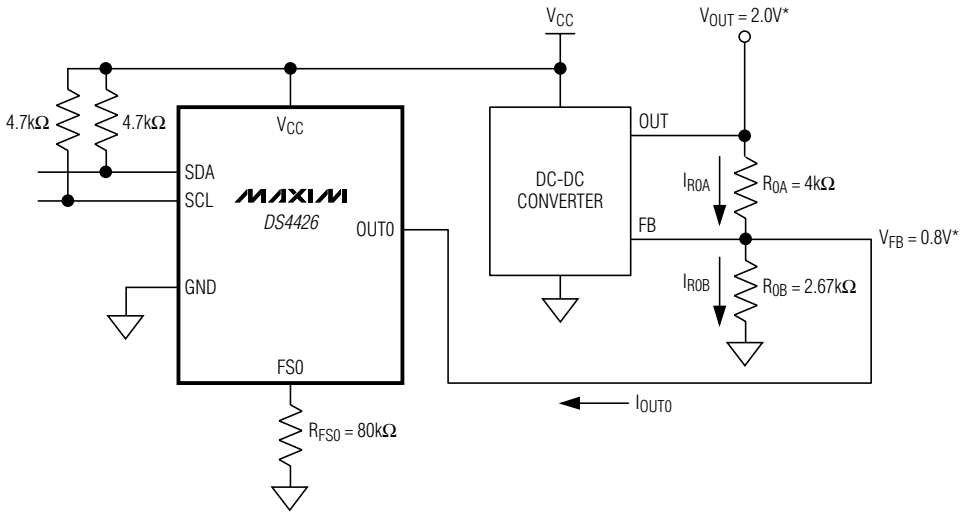
where:

$$I_{R0B} = \frac{V_{FB}}{R_{0B}}$$

and

$$I_{R0A} = \frac{V_{OUT} - V_{FB}}{R_{0A}}$$

To create a ±20% margin in the supply voltage, the value of V_{OUT} is set to +2.4V. With these values in place, R_{0B} is calculated to be 2.67kΩ, and R_{0A} is

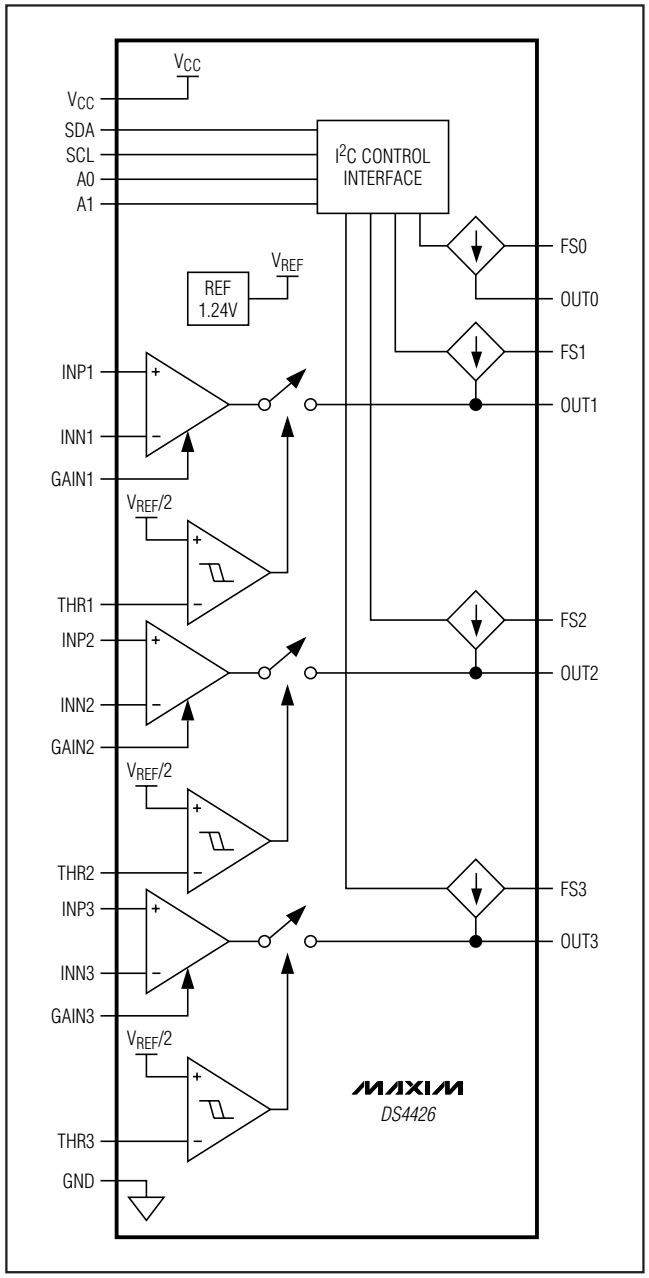


*V_{OUT} AND V_{FB} VALUES ARE DETERMINED BY THE DC-DC CONVERTER AND SHOULD NOT BE CONFUSED WITH V_{OUT} AND V_{REF} OF THE DS4426.

Figure 8. Example Typical Application Circuit

Quad-Channel, I²C-Margining IDACs with Three Channels of Power-Supply Tracking

Functional Diagram



calculated to be 4.00kΩ. The current DAC in this configuration allows the output voltage to be moved linearly from +1.6V to +2.4V using 127 settings. This corresponds to a resolution of 6.3mV/step.

VCC Decoupling

To achieve the best results when using the DS4426, decouple the power supply with a 0.01µF (or 0.1µF) capacitor. Use a high-quality, ceramic, surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance. Ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TQFN	T2844+1	**21-0139**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/08	Initial release.	—
1	7/09	Added OUT[3:0] to the *Absolute Maximum Ratings* for the following condition: Voltage Range on A0, A1, FS[3:0], GAIN[3:1], INN[3:1], INP[3:1], and THR[3:1].	2

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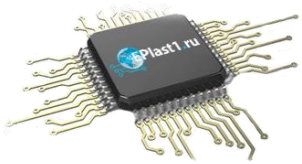

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