Low-Power Sub-1-GHz Fractional-N UHF Device Family for Automotive

1 Introduction

1.1 Features

- Qualification in Accordance With AEC-Q100 Grade 1
- Extended Temperature Range Up To 125°C
- Radio-Frequency (RF) Performance
  - High Sensitivity (–114 dBm at 1.2 kBaud, 315 MHz, 1% Packet Error Rate)
  - Low Current Consumption (15.5 mA in Receive, 1.2 kBaud, 315 MHz)
- Programmable Output Power up to +10 dBm for All Supported Frequencies
- Excellent Receiver Selectivity and Blocking Performance
- Programmable Data Rate From 1.2 kBaud to 250 kBaud
- Frequency Bands: 310 MHz to 348 MHz, 420 MHz to 450 MHz, and 779 MHz to 928 MHz
- Analog Features
  - 2-FSK, GFSK, and MSK Supported, as Well as OOK and Flexible ASK Shaping
  - Suitable for Frequency-Hopping Systems Due to a Fast Settling Frequency Synthesizer: 90-µs Settling Time
  - Automatic Frequency Compensation (AFC) Can Align Frequency Synthesizer to Received Center Frequency
  - Integrated Analog Temperature Sensor
- Digital Features
  - Flexible Support for Packet-Oriented Systems: On-Chip Support for Sync Word Detection, Address Check, Flexible Packet Length, and Automatic CRC Handling
  - Efficient SPI Interface: All Registers Can Be Programmed With One Burst Transfer
  - Digital RSSI Output
  - Programmable Channel Filter Bandwidth
  - Programmable Carrier Sense (CS) Indicator
  - Programmable Preamble Quality Indicator (PQI) for Improved Protection Against False Sync Word Detection in Random Noise
  - Support for Automatic Clear Channel Assessment (CCA) Before Transmitting (for Listen-Before-Talk Systems)
  - Support for Per-Package Link Quality Indication (LQI)
  - Optional Automatic Whitening and Dewhitening of Data
- Low-Power Features
  - Fast Startup Time: 240 µs From Sleep to Receive (RX) or Transmit (TX) Mode
  - Wake-On-Radio Functionality for Automatic Low-Power RX Polling
  - Separate 64-Byte RX and TX Data FIFOs (Enables Burst Mode Data Transmission)
- General
  - Few External Components: Completely On-Chip Frequency Synthesizer, No External Filters or RF Switch Needed
  - Green Package: RoHS Compliant and No Antimony or Bromine
  - Small Size QFN 5-mm×5-mm 32-Pin Package
  - Suited for Systems Compliant With EN 300 220 (Europe) and FCC CFR Part 15 (US)
  - Support for Asynchronous and Synchronous Serial Receive/Transmit Mode for Backward Compatibility With Existing Radio Communication Protocols
  - Designed for Automotive Applications

1.2 Applications

- Ultra-Low-Power Wireless Applications in the 315/433/868/915-MHz ISM/SRD Bands
- Remote Keyless Entry Systems
- Passive Entry/Passive Start Systems
- Vehicle Service Links
- Garage Door Opener
- TPMS Systems

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1.3 Advantages

- Relay Attack Prevention Through Fast Channel Hopping
- Lowest System Cost Through Highest Integration Level
- Only One Crystal Needed For Key-Fob Designs
- Integrated Protocol Handling, Wake-On-Radio, Clock Output Relax Microcontroller Requirements

1.4 Family Members

All family members are pin-to-pin and software compatible.

UHF Transceivers	CC1101IRHBRG4Q1 (–40°C to 85°C)
	CC1101TRHBRG4Q1 (–40°C to 105°C)
	CC1101QRHBRG4Q1 (–40°C to 125°C)
UHF Receivers	CC1131IRHBRG4Q1 (–40°C to 85°C)
	CC1131TRHBRG4Q1 (–40°C to 105°C)
	CC1131QRHBRG4Q1 (–40°C to 125°C)
UHF Transmitters	CC1151IRHBRG4Q1 (–40°C to 85°C)
	CC1151TRHBRG4Q1 (–40°C to 105°C)
	CC1151QRHBRG4Q1 (–40°C to 125°C)

1.5 Description

The CC11x1-Q1 device family is designed for very low-power wireless applications. The circuits are mainly intended for the Industrial, Scientific and Medical (ISM) and Short Range Device (SRD) frequency bands at 315 MHz, 433 MHz, 868 MHz, and 915 MHz, but can easily be programmed for operation at other frequencies in the 310-MHz to 348-MHz, 420-MHz to 450-MHz, and 779-MHz to 928-MHz bands.

The devices integrate a highly configurable baseband modem. The modem supports various modulation formats and has a configurable data rate up to 250 kBaud. CC11x1-Q1 family provides extensive hardware support for packet handling, data buffering, burst transmissions, clear channel assessment, link quality indication, and wake-on-radio. The main operating parameters and the 64-byte transmit/receive FIFOs can be controlled via an SPI interface. In a typical system, the devices are used together with a microcontroller and a few additional passive components.

WARNING

This product shall not be used in any of the following products or systems without prior express written permission from Texas Instruments:

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Please contact lpw-medical-approval@list.ti.com if your application might fall within a category described above.

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1.6 Abbreviations

The following abbreviations are used in this data manual.

ACP	Adjacent Channel Power	MSK	Minimum Shift Keying
ADC	Analog-to-Digital Converter	N/A	Not Applicable
AFC	Automatic Frequency Compensation	NRZ	Non Return to Zero (Coding)
AGC	Automatic Gain Control	OOK	On-Off Keying
AMR	Automatic Meter Reading	PA	Power Amplifier
ASK	Amplitude Shift Keying	PCB	Printed Circuit Board
BER	Bit Error Rate	PD	Power Down
BT	Bandwidth-Time Product	PER	Packet Error Rate
CCA	Clear Channel Assessment	PLL	Phase-Locked Loop
CFR	Code of Federal Regulations	POR	Power-On Reset
CRC	Cyclic Redundancy Check	PQI	Preamble Quality Indicator
CS	Carrier Sense	PQT	Preamble Quality Threshold
CW	Continuous Wave (Unmodulated Carrier)	PTAT	Proportional To Absolute Temperature
DC	Direct Current	QLP	Quad Leadless Package
DVGA	Digital Variable Gain Amplifier	QPSK	Quadrature Phase Shift Keying
ESR	Equivalent Series Resistance	RC	Resistor Capacitor
FCC	Federal Communications Commission	RF	Radio Frequency
FEC	Forward Error Correction	RSSI	Received Signal Strength Indicator
FIFO	First In, First Out	RX	Receive, Receive Mode
FHSS	Frequency Hopping Spread Spectrum	SAW	Surface Acoustic Wave
2-FSK	Binary Frequency Shift Keying	SMD	Surface Mount Device
GFSK	Gaussian shaped Frequency Shift Keying	SNR	Signal-to-Noise Ratio
IF	Intermediate Frequency	SPI	Serial Peripheral Interface
I/Q	In-Phase/Quadrature	SRD	Short Range Devices
ISM	Industrial, Scientific, Medical	TBD	To Be Defined
LC	Inductor-Capacitor	T/R	Transmit/Receive
LNA	Low Noise Amplifier	TX	Transmit, Transmit Mode
LO	Local Oscillator	UHF	Ultra-High Frequency
LSB	Least-Significant Bit	VCO	Voltage Controlled Oscillator
LQI	Link Quality Indicator	WOR	Wake on Radio, Low power polling
MCU	Microcontroller Unit	XOSC	Crystal Oscillator
MSB	Most-Significant Bit	XTAL	Crystal

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2 Electrical Specifications

2.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage(2)		–0.3 V to 3.9 V
	Voltage on any digital pin		–0.3 V to (V_{DD} + 0.3 V)(3)
	Voltage on the pins RF_P, RF_N, DCOUPL1 and DCOUPL2		–0.3 V to 2 V
	Voltage ramp-up rate		120 kV/µs
	Input RF level		10 dBm
T_{stg}	Storage temperature range		–50°C to 150°C
T_{solder}	Solder reflow temperature(4)		260°C
ESD	Electrostatic discharge rating(5)	Human-Body Model (HBM)(6)	±750 V
		Charged-Device Model (CDM)(7)	±200 V
		Machine Model (MM)(8)	±100 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All supply pins must have the same voltage.
(3) Maximum voltage is 3.9 V.
(4) Measured according to IPC/JEDEC J-STD-020C
(5) High-sensitivity UHF devices must be handled with special care to avoid ESD damage. TI is not responsible for damage to this device caused by external ESD conditions. The following electrostatic discharge (ESD) precautions are recommended:
- Protective outer garments
- Handling in ESD-safeguarded work area
- Transporting in ESD-shielded containers
- Frequent monitoring and testing of all ESD-protection equipment

(6) Measured according to JEDEC STD 22, Method A114
(7) Measured according to JEDEC STD 22, C101C
(8) Measured according to JEDEC STD 22, Method A115A

2.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{DD}	Supply voltage		1.8	3.6	V
T_A	Operating free-air temperature	I temperature suffix	–40	85	°C
		T temperature suffix	–40	105	
		Q temperature suffix	–40	125	

2.3 General Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency range	T_A = –40°C to 105°C, V_{DD} = 1.8 V to 3.3 V	310		348	MHz
		420		450	
		779		928	
Data rate(1)	The data rate step size is determined by the reference frequency – see *Data Rate Programming*	1.2		250	kBaud
	Shaped MSK (also known as differential offset QPSK)		26 to 250		
Device weight			0.0715		g

(1) Optional Manchester encoding halves the data rate.

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2.4 Current Consumption

V_{DD} = 1.8 V to 3.3 V, f_{REF} = 26 MHz, All voltages refer to GND (unless otherwise noted). Typical values at T_A = 25°C, V_{DD} = 3 V. All measurement results obtained using the reference designs.

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Current consumption in power-down modes	Voltage regulator to digital part off, register values retained, RC oscillator off, all GDO pins programmed to 0X2F (SLEEP state)	–40°C to 105°C		0.7	5	µA
		125°C		1.9		
	Voltage regulator to digital part off, register values retained, low-power RC oscillator running (SLEEP state with WOR enabled)	–40°C to 105°C		2	6	
		125°C		2.5		
	Voltage regulator to digital part off, register values retained, XOSC running (SLEEP state with MCSM0.OSC_FORCE_ON set)	–40°C to 105°C		370	490	
		125°C		400		
	Voltage regulator to digital part on, all other modules in power down (XOFF state)	–40°C to 105°C		160	300	
		125°C		190		
	Only voltage regulator to digital part and crystal oscillator running (IDLE state)	–40°C to 105°C		1.8	2.5	mA
		125°C		1.9		
	Only the frequency synthesizer running (after going from IDLE until reaching RX or TX states, and frequency calibration states)	–40°C to 105°C		9	10.5	
		125°C		9.1		
Current consumption, 315 MHz	Transmit mode(1), 10-dBm output power, Continuous wave	–40°C to 105°C		29.5	32.9	mA
		125°C		28.9		
	Transmit mode(1), 0-dBm output power, Continuous wave	–40°C to 105°C		14.6	16.5	
		125°C		14.3		
	Transmit mode(1), –5-dBm output power, Continuous wave	–40°C to 105°C		12.2	14	
		125°C		12.1		
	Receive mode(2), 1.2 kbps, input 20 dB above sensitivity limit	–40°C to 105°C		17.5	21	
		125°C		18.3		
	Receive mode(2), 38.4 kbps, input 20 dB above sensitivity limit	–40°C to 105°C		17.5	21	
		125°C		18.4		
	Receive mode(2), 38.4 kbps, input 20 dB above sensitivity limit, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1)	–40°C to 105°C		15.5	17	
		125°C		16.5		
	Receive mode(2), 250 kbps, input 30 dB above sensitivity limit	–40°C to 105°C		17.8	21.5	
		125°C		18.4		
Current consumption, 433 MHz	Transmit mode(1), 10-dBm output power	–40°C to 105°C		30.5	33	mA
		125°C		30		
	Transmit mode(1), 0-dBm output power	–40°C to 105°C		15.4	17.5	
		125°C		15.1		
	Transmit mode(1), –5-dBm output power	–40°C to 105°C		13.1	14.9	
		125°C		13		
	Receive mode(2), 1.2 kbps, input 20 dB above sensitivity limit	–40°C to 105°C		18.6	22	
		125°C		19.2		
	Receive mode(2), 38.4 kbps, input 20 dB above sensitivity limit	–40°C to 105°C		18.6	22.2	
		125°C		19.3		
	Receive mode(2), 38.4 kbps, input 20 dB above sensitivity limit, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1)	–40°C to 105°C		16.5	18	
		125°C		17		
	Receive mode(2), 250 kbps, input 30 dB above sensitivity limit	–40°C to 105°C		18.6	22.2	
		125°C		19.3		

(1) Transmit parameters valid for CC1101 and CC1151 only
(2) Receive parameters valid for CC1101 and CC1131 only

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Current Consumption *(continued)*

V_{DD} = 1.8 V to 3.3 V, f_{REF} = 26 MHz, All voltages refer to GND (unless otherwise noted). Typical values at T_A = 25°C, V_{DD} = 3 V. All measurement results obtained using the reference designs.

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Current consumption, 868 MHz	Transmit mode(1), 10-dBm output power	–40°C to 105°C		35.5	39	mA
		125°C		33.9		
	Transmit mode(1), 0-dBm output power	–40°C to 105°C		16.4	18.5	
		125°C		16.2		
	Transmit mode(1), –5-dBm output power	–40°C to 105°C		15	17.5	
		125°C		16		
	Receive mode(2), 1.2 kbps, input 20 dB above sensitivity limit	–40°C to 105°C		18.5	21.5	
		125°C		19		
	Receive mode(2), 38.4 kbps, input 20 dB above sensitivity limit	–40°C to 105°C		18.4	21.5	
		125°C		19		
	Receive mode(2), 38.4 kbps, input 20 dB above sensitivity limit, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1)	–40°C to 105°C		16	18	
		125°C		16.5		
	Receive mode(2), 250 kbps, input 30 dB above sensitivity limit	–40°C to 105°C		18.5	22	
		125°C		19.1		
Current consumption, 915 MHz	Transmit mode(1), 10-dBm output power	–40°C to 105°C		34	41	mA
		125°C		32		
	Transmit mode(1), 0-dBm output power	–40°C to 105°C		16	18	
		125°C		15.8		
	Transmit mode(1), –5-dBm output power	–40°C to 105°C		14.5	16.5	
		125°C		15.5		
	Receive mode(2), 1.2 kbps, input 20 dB above sensitivity limit	–40°C to 105°C		18.2	21.5	
		125°C		18.8		
	Receive mode(2), 38.4 kbps, input 20 dB above sensitivity limit	–40°C to 105°C		18.3	21.5	
		125°C		18.8		
	Receive mode(2), 38.4 kbps, input 20 dB above sensitivity limit, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1)	–40°C to 105°C		16	18	
		125°C		16.5		
	Receive mode(2), 250 kbps, input 30 dB above sensitivity limit	–40°C to 105°C		18.3	21.5	
		125°C		18.8		

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2.5 RF Receive Section Characteristics

V_{DD} = 1.8 V to 3.3 V, Forward error correction disabled, All voltages refer to GND (unless otherwise noted). Typical values at T_A = 25°C, V_{DD} = 3 V. Receive parameters valid for CC1101 and CC1131 only.

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Digital channel RX filter input bandwidth	User programmable, depend on reference frequency, f_{REF} = 26 MHz			58 to 812		kHz
Receiver sensitivity, 315 MHz	1.2 kBaud / 2-FSK, 1% packet error rate, TX deviation 5.2 kHz, 58-kHz RX bandwidth, high-sensitivity mode (MDMCFG2.DEM_DCFILT_OFF = 0)	–40°C to 105°C		–114		dBm
		125°C		–113		
	1.2 kBaud / 2-FSK, 1% packet error rate, TX deviation 5.2 kHz, 58-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1)	–40°C to 105°C		–109		
		125°C		–105		
	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, high-sensitivity mode (MDMCFG2.DEM_DCFILT_OFF = 0)	–40°C to 105°C	–98	–105		
		125°C		–101		
	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1)	–40°C to 105°C	–96	–103		
		125°C		–100		
	1.2 kBaud / ASK, 1% packet error rate, 58-kHz RX bandwidth, high-sensitivity mode(MDMCFG2.DEM_DCFILT_OFF = 0)	–40°C to 105°C		–108		
Receiver sensitivity, 433 MHz	1.2 kBaud / 2-FSK, 1% packet error rate, TX deviation 5.2 kHz, 58-kHz RX bandwidth, high-sensitivity mode (MDMCFG2.DEM_DCFILT_OFF = 0)	–40°C to 105°C		–114		dBm
		125°C		–113		
	1.2 kBaud / 2-FSK, 1% packet error rate, TX deviation 5.2 kHz, 58-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1)	–40°C to 105°C		–109		
		125°C		–105		
	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, high-sensitivity mode (MDMCFG2.DEM_DCFILT_OFF = 0)	–40°C to 105°C	–100	–107		
		125°C		–102		
	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1)	–40°C to 105°C	–98	–104		
		125°C		–101		
	1.2 kBaud / ASK, 1% packet error rate, 58-kHz RX bandwidth, high-sensitivity mode. (MDMCFG2.DEM_DCFILT_OFF = 0)	–40°C to 105°C		–109		
Receiver sensitivity, 868 MHz	1.2 kBaud / 2-FSK, 1% packet error rate, TX deviation 5.2 kHz, 58-kHz RX bandwidth, high-sensitivity mode (MDMCFG2.DEM_DCFILT_OFF = 0)	–40°C to 105°C		–111		dBm
		125°C		–109		
	1.2 kBaud / 2-FSK, 1% packet error rate, TX deviation 5.2 kHz, 58-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1)	–40°C to 105°C		–107		
		125°C		–102		
	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, high-sensitivity mode (MDMCFG2.DEM_DCFILT_OFF = 0)	–40°C to 105°C	–100	–106		
		125°C		–101		
	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1)	–40°C to 105°C	–96	–103		
		125°C		–99		
	250 kBaud / 2-FSK, 1% packet error rate, TX deviation 127 kHz, 540-kHz RX bandwidth, high-sensitivity mode (MDMCFG2.DEM_DCFILT_OFF = 0)	–40°C to 105°C	–90	–98		
		125°C		–95		
	1.2 kBaud / ASK, 1% packet error rate, 58-kHz RX bandwidth, high-sensitivity mode. (MDMCFG2.DEM_DCFILT_OFF = 0)	–40°C to 105°C		–108		

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RF Receive Section Characteristics *(continued)*

V_{DD} = 1.8 V to 3.3 V, Forward error correction disabled, All voltages refer to GND (unless otherwise noted). Typical values at T_A = 25°C, V_{DD} = 3 V. Receive parameters valid for CC1101 and CC1131 only.

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Receiver sensitivity, 915 MHz	1.2 kBaud / 2-FSK, 1% packet error rate, TX deviation 5.2 kHz, 58-kHz RX bandwidth, high-sensitivity mode (MDMCFG2.DEM_DCFILT_OFF = 0)	–40°C to 105°C		–111		dBm
		125°C		–109		
	1.2 kBaud / 2-FSK, 1% packet error rate, TX deviation 5.2 kHz, 58-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1)	–40°C to 105°C		–107		
		125°C		–102		
	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, high-sensitivity mode (MDMCFG2.DEM_DCFILT_OFF = 0)	–40°C to 105°C	–100	–107		
		125°C		–102		
	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1)	–40°C to 105°C	–97	–103		
		125°C		–100		
	250 kBaud / 2-FSK, 1% packet error rate, TX deviation 127 kHz, 540-kHz RX bandwidth, high-sensitivity mode (MDMCFG2.DEM_DCFILT_OFF = 0)	–40°C to 105°C		–98		
		125°C		–93		
Receiver adjacent channel rejection, 315 MHz/433 MHz	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1), Channel spacing 200 kHz, Desired channel 3 dB above sensitivity level, Signal level at ±200 kHz	–40°C to 105°C		–56		dB
		125°C		–52		
Receiver alternate channel rejection, 315 MHz/433 MHz	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1), Channel spacing 200 kHz, Desired channel 3 dB above sensitivity level, Signal level at ±400 kHz	–40°C to 105°C		–55		dB
		125°C		–50		
Receiver blocking ±2 MHz, 315 MHz/433 MHz	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1), Channel spacing 200 kHz, Desired channel 3 dB above sensitivity level, Signal level at ±2 MHz	–40°C to 105°C		–46		dBm
		125°C		–41		
Receiver blocking ±10 MHz, 315 MHz/433 MHz	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1), Desired channel 3 dB above sensitivity level, Signal level at ±10 MHz	–40°C to 105°C		–40		dBm
		125°C		–33		
Receiver image channel rejection, 315 MHz/433 MHz	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1), Channel spacing 200 kHz, Desired channel 3 dB above sensitivity level, Signal level at f_{Signal} – 608 kHz	–40°C to 105°C		–65		dB
		125°C		–61		
Receiver adjacent channel rejection, 868 MHz/915 MHz	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1), Channel spacing 200 kHz, Desired channel 3 dB above sensitivity level, Signal level at ±200 kHz	–40°C to 105°C		–64		dB
		125°C		–61		
Receiver alternate channel rejection, 868 MHz/915 MHz	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1), Channel spacing 200 kHz, Desired channel 3 dB above sensitivity level, Signal level at ±400 kHz	–40°C to 105°C		–58		dB
		125°C		–54		
Receiver blocking, 868 MHz ± 2 MHz	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1), Wanted signal 3 dB above sensitivity limit, level of unmodulated signal at ±2 MHz is recorded	–40°C to 105°C		–44		dBm
		125°C		–40		
Receiver blocking, 868 MHz ± 10 MHz	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1), Wanted signal 3 dB above sensitivity limit, Level of unmodulated signal at ±10 MHz is recorded	–40°C to 105°C		–38		dBm
		125°C		–33		

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RF Receive Section Characteristics *(continued)*

V_{DD} = 1.8 V to 3.3 V, Forward error correction disabled, All voltages refer to GND (unless otherwise noted). Typical values at T_A = 25°C, V_{DD} = 3 V. Receive parameters valid for CC1101 and CC1131 only.

PARAMETER	TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
Receiver image channel rejection, 868 MHz/915 MHz	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1), Channel spacing 200 kHz, Desired channel 3 dB above sensitivity level, Signal level at f_{Signal} – 608 kHz		–40°C to 105°C		–60		dB
			125°C		–55		
Receiver spurious emission	38.4 kBaud / 2-FSK, 1% packet error rate, TX deviation 19 kHz, 100-kHz RX bandwidth, low-current mode (MDMCFG2.DEM_DCFILT_OFF = 1)	25 MHz to 1 GHz	–40°C to 105°C		–57		dBm
		> 1 GHz	–40°C to 105°C		–47		

2.6 Selectivity

Figure 2-1 to Figure 2-3 show the typical selectivity performance (adjacent and alternate rejection).

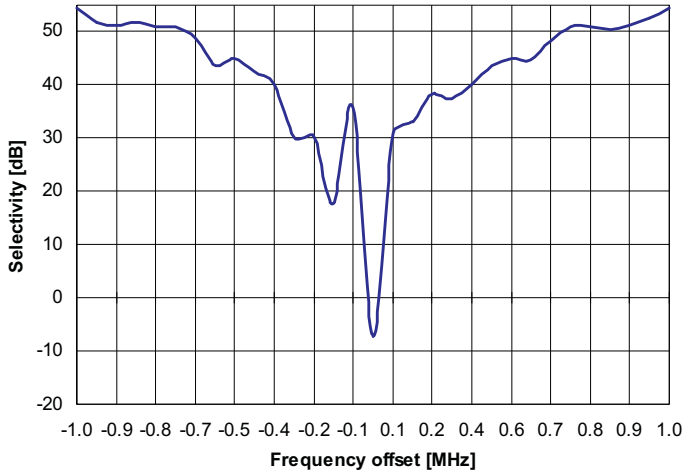

Figure 2-1. Typical Selectivity at 1.2-kBaud Data Rate, 868.3 MHz, GFSK, 5.2-kHz Deviation, IF Frequency 152.3 kHz, Digital Channel Filter Bandwidth 58 kHz

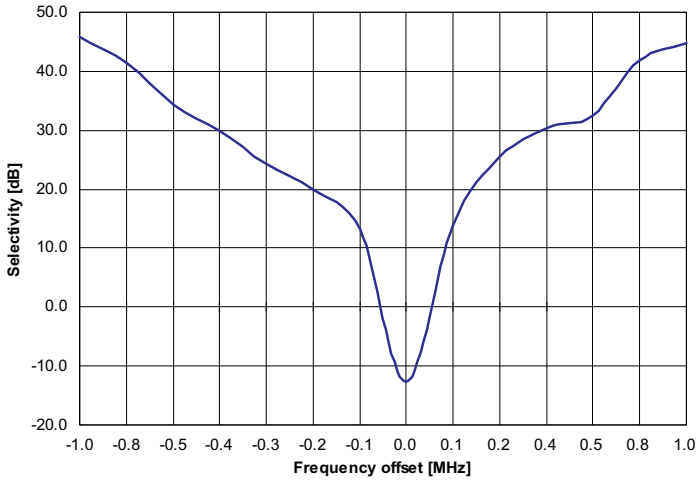

Figure 2-2. Typical Selectivity at 38.4-kBaud Data Rate, 868 MHz, GFSK, 20-kHz Deviation, IF Frequency 152.3 kHz, Digital Channel Filter Bandwidth 100 kHz

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Selectivity *(continued)*

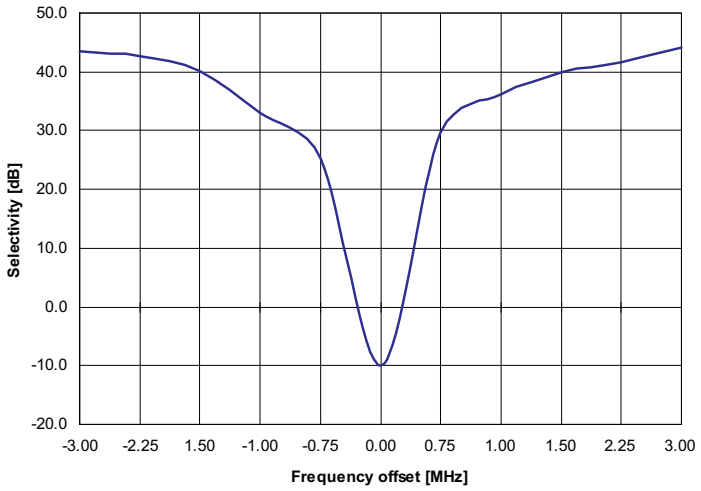

Figure 2-3. Typical Selectivity at 250-kBaud Data Rate, 868 MHz, GFSK, IF Frequency 304 kHz, Digital Channel Filter Bandwidth 540 kHz

2.7 RSSI Section Characteristics(1)

V_{DD} = 1.8 V to 3.3 V, All voltages refer to GND (unless otherwise noted). Typical values at T_A = 25°C, V_{DD} = 3 V. Receive parameters valid for CC1101 and CC1131 only.

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
RSSI accuracy, 310 MHz	RX mode, 100-kHz RX bandwidth, Reference signal CW , –90-dBm power level. Read RSSI status register and calculate measured RSSI level.	–40°C to 105°C		–90		dBm
		125°C				
	RX mode, 100-kHz RX bandwidth, Reference signal CW , –20-dBm power level. Read RSSI status register and calculate measured RSSI level.	–40°C to 105°C		–20		
		125°C				
RSSI accuracy, 928 MHz	RX mode, 100-kHz RX bandwidth, Reference signal CW , –90-dBm power level. Read RSSI status register and calculate measured RSSI level.	–40°C to 105°C	–97	–89	–82	dBm
		125°C		–91		
	RX mode, 100-kHz RX bandwidth, Reference signal CW , –55-dBm power level. Read RSSI status register and calculate measured RSSI level.	–40°C to 105°C	–62	–54	–45	
		125°C		–56		
	RX mode, 100-kHz RX bandwidth, Reference signal CW , –20-dBm power level. Read RSSI status register and calculate measured RSSI level.	–40°C to 105°C	–27	–19	–10	
		125°C		–21		

(1) RSSI tolerances can be compensated by an offset correction for each device.

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2.8 RF Transmit Section Characteristics

V_{DD} = 1.8 V to 3.3 V, All voltages refer to GND (unless otherwise noted). Typical values at T_A = 25°C, V_{DD} = 3 V. Transmit parameters valid for CC1101 and CC1151 only.

PARAMETER	TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
Differential load impedance	Load impedance as seen from the RF port RF_N and RF_P towards the antenna. For matching follow the reference design.	315 MHz	–40°C to 105°C		122 + j31		Ω
		433 MHz			116 + j41		
		868 MHz/ 915 MHz			87 + j43		
TX output power, 315 MHz	38.4 kBaud / GFSK, TX deviation 19 kHz, Output power setting: 10 dBm CW, Delivered into a 50-Ω load, including matching network as outlined		–40°C to 105°C	9	11	12.5	dBm
			125°C		10		
	38.4 kBaud / GFSK, TX deviation 19 kHz, Output power setting: 0 dBm CW, Delivered into a 50-Ω load, including matching network as outlined		–40°C to 105°C	–3	–0.5	2.5	
			125°C		–1.5		
	38.4 kBaud / GFSK, TX deviation 19 kHz, Output power setting: –5 dBm CW, Delivered into a 50-Ω load, including matching network as outlined		–40°C to 105°C	–8.5	–5.7	–2.5	
			125°C		–6.7		
TX output power, 433 MHz	38.4 kBaud / GFSK, TX deviation 19 kHz, Output power setting: 10 dBm CW, Delivered into a 50-Ω load, including matching network as outlined		–40°C to 105°C	9	10.8	12	dBm
			125°C		10.3		
	38.4 kBaud / GFSK, TX deviation 19 kHz, Output power setting: 0 dBm CW, Delivered into a 50-Ω load, including matching network as outlined		–40°C to 105°C	–4.5	–0.2	4	
			125°C		–1.1		
	38.4 kBaud / GFSK, TX deviation 19 kHz, Output power setting: –5 dBm CW, Delivered into a 50-Ω load, including matching network as outlined		–40°C to 105°C	–8	–5.3	–2.5	
			125°C		–6.2		
TX output power, 868 MHz	38.4 kBaud / GFSK, TX deviation 19 kHz, Output power setting: 10 dBm CW, Delivered into a 50-Ω load, including matching network as outlined		–40°C to 105°C	8	10.4	12	dBm
			125°C		9.7		
	38.4 kBaud / GFSK, TX deviation 19 kHz, Output power setting: 0 dBm CW, Delivered into a 50-Ω load, including matching network as outlined		–40°C to 105°C	–4	–0.5	3.5	
			125°C		–1.9		
	38.4 kBaud / GFSK, TX deviation 19 kHz, Output power setting: –5 dBm CW, Delivered into a 50-Ω load, including matching network as outlined		–40°C to 105°C	–9	–5	–2.5	
			125°C		–7		
TX output power, 915 MHz	38.4 kBaud / GFSK, TX deviation 19 kHz, Output power setting: 10 dBm CW, Delivered into a 50-Ω load, including matching network as outlined		–40°C to 105°C	7.5	9.6	12	dBm
			125°C		9.4		
	38.4 kBaud / GFSK, TX deviation 19 kHz, Output power setting: 0 dBm CW, Delivered into a 50-Ω load, including matching network as outlined		–40°C to 105°C	–4	–0.3	4	
			125°C		–0.9		
	38.4 kBaud / GFSK, TX deviation 19 kHz, Output power setting: –5 dBm CW, Delivered into a 50-Ω load, including matching network as outlined		–40°C to 105°C	–8	–5	–1.5	
			125°C		–5.6		
Second-order harmonics, 315 MHz	Conducted measurement on reference design with CW and maximum output-power settings Note: PA output matching impacts harmonics level		–40°C to 105°C		–50		dBm
			125°C		–53		
Third-order harmonics, 315 MHz	Conducted measurement on reference design with CW and maximum output-power settings Note: PA output matching impacts harmonics level		–40°C to 105°C		–32		dBm
			125°C		–40		

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RF Transmit Section Characteristics *(continued)*

V_{DD} = 1.8 V to 3.3 V, All voltages refer to GND (unless otherwise noted). Typical values at T_A = 25°C, V_{DD} = 3 V. Transmit parameters valid for CC1101 and CC1151 only.

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Second-order harmonics, 433 MHz	Conducted measurement on reference design with CW and maximum output power settings Note: PA output matching impacts harmonics level	–40°C to 105°C		–40		dBm
		125°C		–41		
Third-order harmonics, 433 MHz	Conducted measurement on reference design with CW and maximum output power settings Note: PA output matching impacts harmonics level	–40°C to 105°C		–26		dBm
		125°C		–27		
Second-order harmonics, 868 MHz	Conducted measurement on reference design with CW and maximum output power settings Note: PA output matching impacts harmonics level	–40°C to 105°C		–48		dBm
		125°C		–44		
Third-order harmonics, 868 MHz	Conducted measurement on reference design with CW and maximum output power settings Note: PA output matching impacts harmonics level	–40°C to 105°C		–45		dBm
		125°C		–45		
Second-order harmonics, 915 MHz	Conducted measurement on reference design with CW and maximum output power settings Note: PA output matching impacts harmonics level	–40°C to 105°C		–50		dBm
		125°C		–53		
Third-order harmonics, 915 MHz	Conducted measurement on reference design with CW and maximum output power settings Note: PA output matching impacts harmonics level	–40°C to 105°C		–45		dBm
		125°C		–46		

2.9 Crystal Oscillator Characteristics

V_{DD} = 1.8 V to 3.3 V, T_A = –40°C to 105°C, without forward error correction (unless otherwise noted). All voltages refer to GND. Typical values at T_A = 25°C, V_{DD} = 3 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference frequency	Depending on the UHF operating frequency a 26-MHz or 27-MHz crystal should be used.		26 to 27		MHz
Tolerances	The acceptable crystal tolerance depend on the system requirements e.g., RX/TX bandwidth, channel spacing, clock synchronization between RX/TX units		±20		ppm
ESR			100		Ω
Start-up time	Measured on the reference design. Parameter depends on the crystal that is used. Time does not include POR of the device		150		µs
Load capacitors	Simulated over operating conditions		10 to 20		pF

2.10 Low-Power RC Oscillator Characteristics

V_{DD} = 1.8 V to 3.3 V, T_A = –40°C to 105°C, without forward error correction (unless otherwise noted). All voltages refer to GND. Typical values at T_A = 25°C, V_{DD} = 3 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Nominal, calibrated frequency	After calibration: $f_{RC} = f_{REF}/750$, f_{REF} = 26 MHz	34	34.666	35	kHz
Frequency accuracy after calibration			±0.3		%
Calibration time	Time to calibrate RC oscillator, Calibration is continuously done in the background as long as the crystal oscillator is running		2		ms

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2.11 Frequency Synthesizer Characteristics

V_{DD} = 1.8 V to 3.3 V, f_{REF} = 26 MHz, without forward error correction (unless otherwise noted). All voltages refer to GND. Typical values at T_A = 25°C, V_{DD} = 3 V.

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Synthesizer frequency resolution	26-MHz or 27-MHz f_{REF}, Frequency resolution is equal for all frequency bands	–40°C to 105°C		$f_{REF}/2_{16}$		Hz
Phase noise at 50-kHz offset	Single sideband noise power in dBc/Hz measured at nominal supply over all frequency bands at maximum power setting	–40°C to 105°C		–80		dBc/Hz
Phase noise at 100-kHz offset	Single sideband noise power in dBc/Hz measured at nominal supply over all frequency bands at maximum power setting	–40°C to 105°C		–85		dBc/Hz
Phase noise at 200-kHz offset	Single sideband noise power in dBc/Hz measured at nominal supply over all frequency bands at maximum power setting	–40°C to 105°C		–92		dBc/Hz
Phase noise at 500-kHz offset	Single sideband noise power in dBc/Hz measured at nominal supply over all frequency bands at maximum power setting	–40°C to 105°C		–100		dBc/Hz
Phase noise at 1-MHz offset	Single sideband noise power in dBc/Hz measured at nominal supply over all frequency bands at maximum power setting	–40°C to 105°C		–100		dBc/Hz
Synthesizer turn-on time / hop time	Time from IDLE state crystal oscillator running until arriving the RX, FSTXON, or TX state, RC oscillator calibration disabled	–40°C to 105°C		110		µs
Synthesizer turn-on time	Time from IDLE state crystal oscillator running until arriving the RX, FSTXON, or TX state, with synthesizer calibration	–40°C to 105°C		850		µs
Synthesizer RX/TX settling time	Time to switch from RX to TX	–40°C to 105°C		10		µs
Synthesizer TX/RX settling time	Time to switch from TX to RX	–40°C to 105°C		25		µs
Synthesizer calibration time	Manual triggered calibration before entering or after leaving the RX/TX state	–40°C to 105°C		18739		f_{REF} cycles

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2.12 Analog Temperature Sensor Characteristics

V_{DD} = 1.8 V to 3.3 V, T_A = –40°C to 105°C, without forward error correction (unless otherwise noted). All voltages refer to GND. Typical values at T_A = 25°C, V_{DD} = 3 V. Note that it is necessary to write 0xBF to the PTEST register to use the analog temperature sensor in the IDLE state.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	T_A = –40°C	0.60	0.70	0.80	V
	T_A = 0°C		0.775		
	T_A = 25°C		0.815		
	T_A = 70°C		0.880		
	T_A = 85°C		0.912		
	T_A = 105°C	0.88	0.96	1.07	
	T_A = 125°C		0.968		
Temperature coefficient	Fitted from T_A = –20°C to 80°C		1.6		mV/ C
Error in calculated temperature, calibrated	From T_A = –20°C to 80°C when using 2.44 mV/°C, after 1-point calibration at 25°C temperature		±2		°C

2.13 Digital Input/Output DC Characteristics

V_{DD} = 1.8 V to 3.3 V, T_A = –40°C to 105°C, without forward error correction (unless otherwise noted). All voltages refer to GND. Typical values at T_A = 25°C, V_{DD} = 3 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage	Logic 0	0		0.7	V
	Logic 1	V_{DD} – 0.7		V_{DD}	
Output voltage	Logic 0	0		0.5	V
	Logic 1	V_{DD} – 0.3		V_{DD}	
Input current	Logic 0, Input equals 0 V		–50		nA
	Logic 1, Input equals VDD		50		

2.14 Power-On Reset Characteristics(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-up ramp-up time	From 0 V to 3 V		1		ms

(1) When the power supply complies with the requirements shown here, proper power-on-reset functionality is assured. Otherwise, the chip should be assumed to have unknown state until it transmits an SRES strobe over the SPI interface. See *Power-On Startup Sequence* for further details.

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2.15 SPI Interface Timing

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency			6	MHz
t_{ch}	Clock high time	80			ns
t_{cl}	Clock low time	80			ns
t_{sd}	Setup time, data (negative SCLK edge) to positive edge on SCLK (1)	80			ns
t_{hd}	Hold time, data after positive edge on SCLK	50			ns
t_{ns}	Negative edge on SCLK to $\overline{CS}$ high	50			ns

(1) t_{sd} applies between address and data bytes, and between data bytes.

2.16 Typical State Transition Timing

PARAMETER	XOSC PERIODS	26-MHz CRYSTAL
IDLE to RX, no calibration	2298	88.4 µs
IDLE to RX, with calibration	~21037	809 µs
IDLE to TX/FSTXON, no calibration	2298	88.4 µs
IDLE to TX/FSTXON, with calibration	~21037	809 µs
TX to RX switch	560	21.5 µs
RX to TX switch	250	9.6 µs
RX or TX to IDLE, no calibration	2	0.1 µs
RX or TX to IDLE, with calibration	~18739	721 µs
Manual calibration	~18739	721 µs

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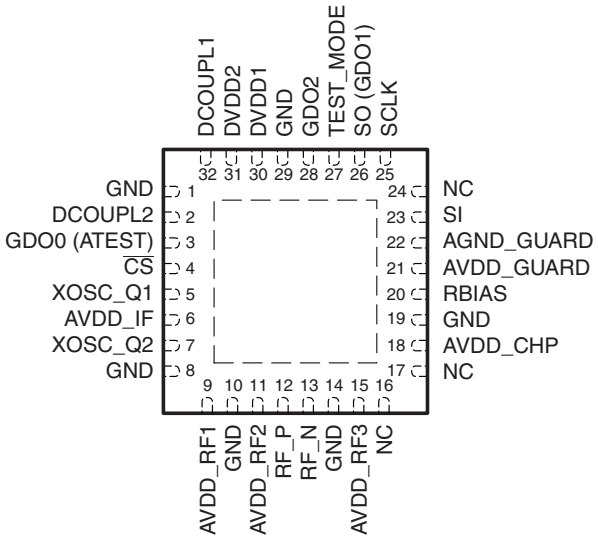
3 Detailed Description

3.1 Terminal Assignments

RHB PACKAGE
(TOP VIEW)



NC – No internal connection

Table 3-1. Terminal Functions

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
1	GND	Ground (Analog)	Analog ground connection
2	DCOUPL2	Power Input (Digital)	1.6-V to 2-V digital power supply input for decoupling
3	GDO0 (ATEST)	Digital I/O	Digital output pin for general use: • Test signals • FIFO status signals • Clear Channel Indicator • Clock output, down-divided from XOSC • Serial output RX data • Serial input TX data Also used as analog test I/O for prototype and production testing.
4	$\overline{CS}$	Digital Input	Serial configuration interface, chip select
5	XOSC_Q1	Analog I/O	Crystal oscillator pin 1, or external clock input
6	AVDD_IF	Power (Analog)	1.8-V to 3.6-V analog power supply connection
7	XOSC_Q2	Analog I/O	Crystal oscillator pin 2
8	GND	Ground (Analog)	Analog ground connection
9	AVDD_RF1	Power (Analog)	1.8-V to 3.6-V analog power supply connection
10	GND	Ground (Analog)	Analog ground connection
11	AVDD_RF2	Power (Analog)	1.8-V to 3.6-V analog power supply connection
12	RF_P	RF I/O	Positive RF input signal to LNA in receive mode. Positive RF output signal from PA in transmit mode
13	RF_N	RF I/O	Negative RF input signal to LNA in receive mode. Negative RF output signal from PA in transmit mode
14	GND	Ground (Analog)	Analog ground connection
15	AVDD_RF3	Power (Analog)	1.8-V to 3.6-V analog power supply connection
16	NC		Not connected
17	NC		Not connected
18	AVDD_CHP	Power (Analog)	1.8-V to 3.6-V analog power supply connection
19	GND	Ground (Analog)	Analog ground connection
20	RBIAS	Analog I/O	External precision bias resistor for reference current
21	AVDD_GUARD	Power (Digital)	Power supply connection for digital noise isolation
22	AGND_GUARD	Ground (Digital)	Ground connection for digital noise isolation
23	SI	Digital Input	Serial configuration interface, data input
24	NC		Not connected
25	SCLK	Digital Input	Serial configuration interface, clock input
26	SO (GDO1)	Digital Output	Serial configuration interface, data output. Optional general output pin when $\overline{CS}$ is high.
27	TEST_MODE	Digital Input	GND enables and NC disables on-chip data scrambling. Internal pullup resistor.
28	GDO2	Digital Output	Digital output pin for general use: • Test signals • FIFO status signals • Clear channel indicator • Clock output, down-divided from XOSC • Serial output RX data
29	GND	Ground (Analog)	Analog ground connection
30	DVDD1	Power (Digital)	1.8-V to 3.6-V digital power supply for digital I/Os and for digital core voltage regulator
31	DVDD2		
32	DCOUPL1	Output regulator digital core	1.6-V to 1.8-V digital power supply output for digital core / decoupling. NOTE: This pin is intended to supply only the CC11x1-Q1 chip. It cannot be used to provide supply voltage to other devices.

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3.2 Block Diagram

A simplified block diagram of CC11x1-Q1 is shown in Figure 3-1. The CC11x1-Q1 devices feature a low intermediate frequency (IF) receiver. The received radio frequency (RF) signal is amplified by the low-noise amplifier (LNA) and down-converted in a quadrature (I and Q) to the IF. At IF, the I/Q signals are digitized by the analog-to-digital converters (ADCs). Automatic gain control (AGC), fine channel filtering, and demodulation bit/packet synchronization is performed digitally.

The transmitter part of CC11x1-Q1 is based on direct synthesis of the RF frequency. The frequency synthesizer includes a completely on-chip LC voltage-controlled oscillator (VCO) and a 90° phase shifter for generating the I and Q signals, and it is also used for the down-conversion mixers in receive mode. A crystal must be connected to XOSC_Q1 and XOSC_Q2. The crystal oscillator generates the reference frequency for the synthesizer as well as the clocks for the ADC and the digital part.

A 4-wire SPI serial interface is used for the register configuration and data buffer access. The digital base band modem includes support for channel configuration, packet handling, Forward Error Correction and data buffering.

In the CC1131-Q1 devices, the TX path is not available. In the CC1151-Q1 devices, the RX path is not available.

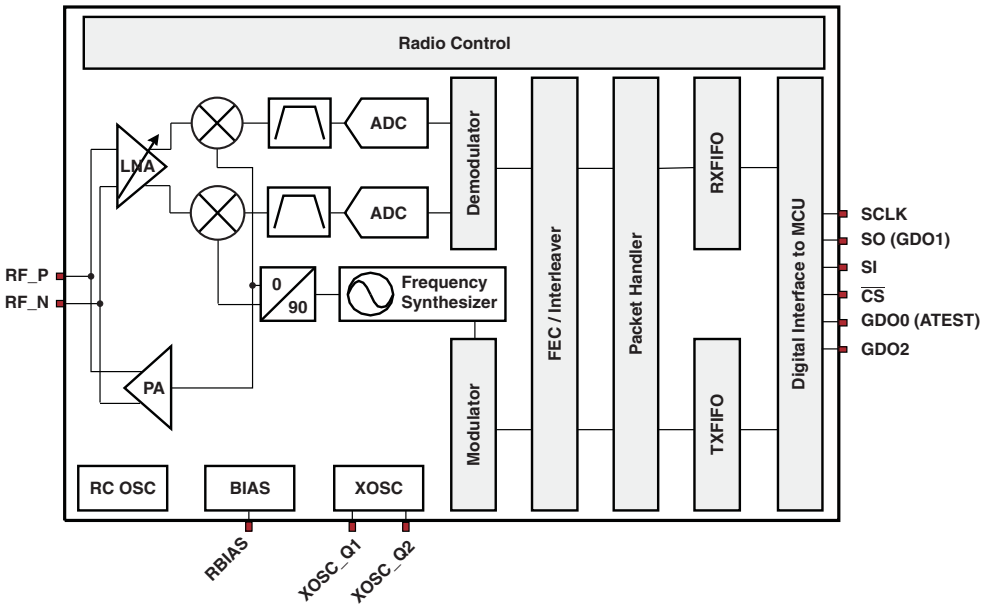

Figure 3-1. Simplified Block Diagram

CC11x1-Q1 features a low intermediate frequency (IF) receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the IF. At IF, the I/Q signals are digitized by the ADCs. Automatic gain control (AGC), fine channel filtering and demodulation bit/packet synchronization are performed digitally.

The transmitter part of CC11x1-Q1 is based on direct synthesis of the RF frequency. The frequency synthesizer includes a completely on-chip LC VCO and a 90° phase shifter for generating the I and Q LO signals to the down-conversion mixers in receive mode.

A crystal is to be connected to XOSC_Q1 and XOSC_Q2. The crystal oscillator generates the reference frequency for the synthesizer, as well as clocks for the ADC and the digital part.

A 4-wire SPI serial interface is used for configuration and data buffer access.

The digital baseband includes support for channel configuration, packet handling, and data buffering.

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3.3 Application Circuit

Only a few external components are required for using the CC11x1-Q1. The recommended application circuits are shown in Figure 3-2 and Figure 3-3. Typical values for the external components are given in Table 3-2.

Bias Resistor

The bias resistor R171 is used to set an accurate bias current.

Balun and RF Matching

The components between the RF_N/RF_P pins and the point where the two signals are joined together (C131, C122, L121, and L131 for the 315/433-MHz reference design [5], or L101, L111, C111, L121, C131, C122, and L131 for the 868/915-MHz reference design [6]) form a balun that converts the differential RF signal on CC11x1-Q1 to a single-ended RF signal. C125 is needed for dc blocking. Together with an appropriate LC network, the balun components also transform the impedance to match a 50-Ω antenna or cable. Suggested values for 315 MHz, 433 MHz, and 868/915 MHz are listed in Table 3-2.

Crystal

The reference oscillator uses an external 26-MHz or 27-MHz crystal with two loading capacitors (C81 and C101). See Section 3.22 for details.

Additional Filtering

Additional external components (e.g., an RF SAW filter) may be used to improve the performance in specific applications.

Power Supply Decoupling

The power supply must be properly decoupled close to the supply pins. A short and proper GND connection is also essential for the functionality of the device.

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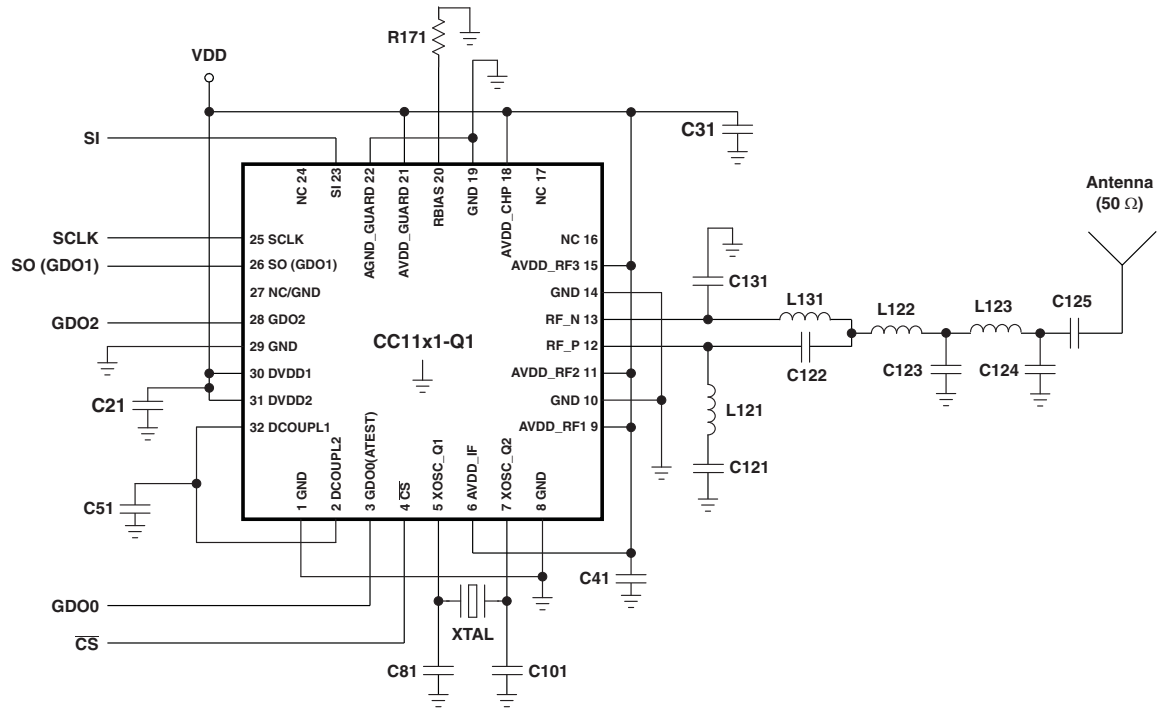
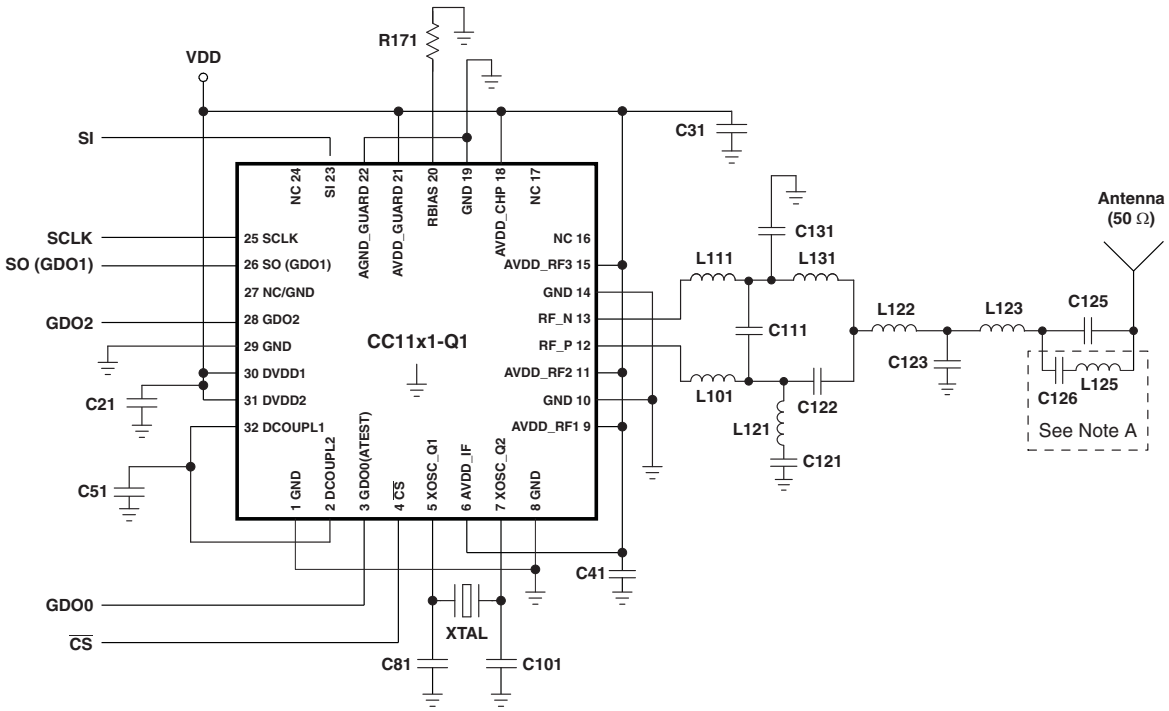


Figure 3-2. Typical Application Circuit for 315 MHz/433 MHz



A. C126 and L125 may be added to build an optional filter to reduce emission at 699 MHz.

Figure 3-3. Typical Application Circuit for 868 MHz/915 MHz

Table 3-2. Bill of Materials for the Application Circuit

COMPONENT	VALUE AT 315 MHz	VALUE AT 433 MHz	VALUE AT 868 MHz	VALUE AT 915 MHz
C21	100 nF ± 10%, 0402 X5R			
C31	100 nF ± 10%, 0402 X5R			
C41	100 nF ± 10%, 0402 X5R			
C51	100 nF ± 10%, 0402 X5R			
C81	27 pF ± 5%, 0402 NP0			
C101	27 pF ± 5%, 0402 NP0			
C111	—	—	1 pF ± 0.25 pF, 0402 NP0	1 pF ± 0.25 pF, 0402 NP0
C121	220 pF ± 5%, 0402 NP0	220 pF ± 5%, 0402 NP0	100 pF ± 5%, 0402 NP0	100 pF ± 5%, 0402 NP0
C122	6.8 pF ± 0.5 pF, 0402 NP0	3.9 pF ± 0.25 pF, 0402 NP0	1.5 pF ± 0.25 pF, 0402 NP0	1.5 pF ± 0.25 pF, 0402 NP0
C123	12 pF ± 5%, 0402 NP0	8.2 pF ± 0.5 pF, 0402 NP0	3.3 pF ± 0.25 pF, 0402 NP0	3.3 pF ± 0.25 pF, 0402 NP0
C124	6.8 pF ± 0.5 pF, 0402 NP0	5.6 pF ± 0.5 pF, 0402 NP0	—	—
C125	220 pF ± 5%, 0402 NP0	220 pF ± 5%, 0402 NP0	100 pF ± 5%, 0402 NP0	100 pF ± 5%, 0402 NP0
C126	—	—	47 pF ± 5%, 0402 NP0	—
C131	6.8 pF ± 0.5 pF, 0402 NP0	3.9 pF ± 0.25 pF, 0402 NP0	1.5 pF ± 0.25 pF, 0402 NP0	1.5 pF ± 0.25 pF, 0402 NP0
L101	—	—	12 nH ± 5%, 0402 / muRata LQW15A	12 nH ± 5%, 0402 / muRata LQW15A
L111	—	—	12 nH ± 5%, 0402 / muRata LQW14A	12 nH ± 5%, 0402 / muRata LQW15A
L121	33 nH ± 5%, 0402 / muRata LQW15A	27 nH ± 5%, 0402 / muRata LQW15A	18 nH ± 5%, 0402 / muRata LQW15A	18 nH ± 5%, 0402 / muRata LQW15A
L122	18 nH ± 5%, 0402 / muRata LQW15A	22 nH ± 5%, 0402 / muRata LQW15A	12 nH ± 5%, 0402 / muRata LQW14A	12 nH ± 5%, 0402 / muRata LQW14A
L123	33 nH ± 5%, 0402 / muRata LQW15A	27 nH ± 5%, 0402 / muRata LQW15A	12 nH ± 5%, 0402 / muRata LQW15A	12 nH ± 5%, 0402 / muRata LQW15A
L125	—	—	3.3 nH ± 5%, 0402 / muRata LQW15A	—
L131	33 nH ± 5%, 0402 / muRata LQW15A	27 nH ± 5%, 0402 / muRata LQW15A	18 nH ± 5%, 0402 / muRata LQW15A	18 nH ± 5%, 0402 / muRata LQW15A
R171	56 kΩ ± 1%, 0402			
XTAL	26 MHz	27 MHz	27 MHz	26 MHz

3.4 Configuration Overview

CC11x1-Q1 can be configured to achieve optimum performance for many different applications. Configuration is done using the SPI interface. The following key parameters can be programmed:

- Power-down / power-up mode
- Crystal oscillator power up / power down
- Receive / transmit mode
- RF channel selection
- Data rate
- Modulation format
- RX channel filter bandwidth
- RF output power
- Data buffering with separate 64-byte receive and transmit FIFOs
- Packet radio hardware support
- Forward error correction (FEC) with interleaving
- Data whitening
- Wake-on-radio (WOR)

Details of each configuration register are in Section 4.

Figure 3-4 shows a simplified state diagram that explains the main CC11x1-Q1 states, together with typical usage and current consumption. For detailed information on controlling the CC11x1-Q1 state machine, and a complete state diagram, see Section 3.15.

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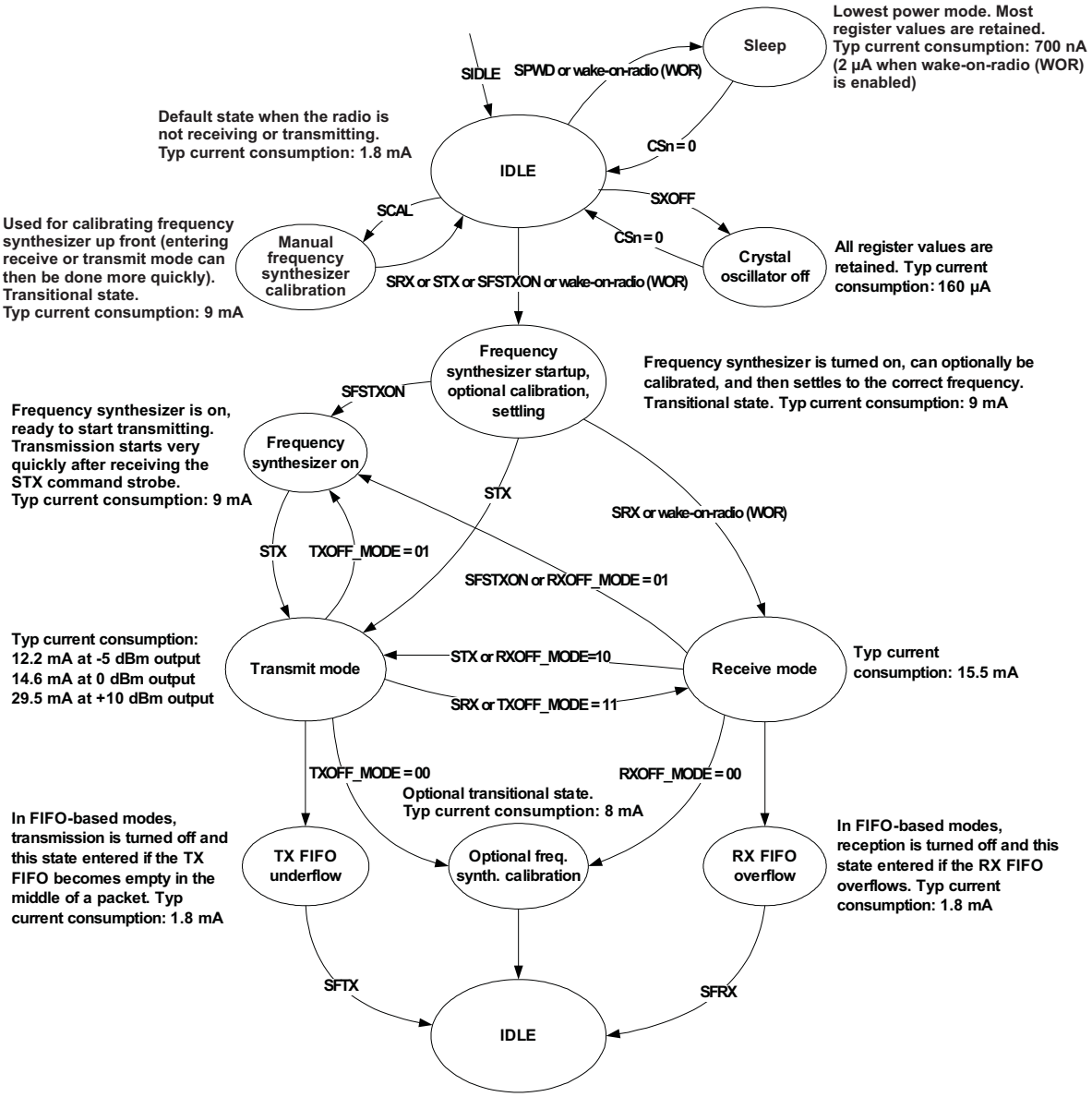

Figure 3-4. Simplified State Diagram, With Typical Current Consumption at 1.2-kBaud Data Rate and MDMCFG2.DEM_DCFILT_OFF = 1 (Current Optimized), Frequency Band = 315 MHz

3.5 Configuration Software

CC11x1-Q1 can be configured using the SmartRF® Studio software. The SmartRF Studio software is highly recommended for obtaining optimum register settings and for evaluating performance and functionality. A screenshot of the SmartRF Studio user interface for CC11x1-Q1 is shown in Figure 3-5.

After chip reset, all the registers have default values as shown in Section 4. The optimum register setting might differ from the default value. Therefore, after a reset, all registers that are different from the default value need to be programmed through the SPI interface. For the CC11x1-Q1 device, the settings of the CC1101 are valid.

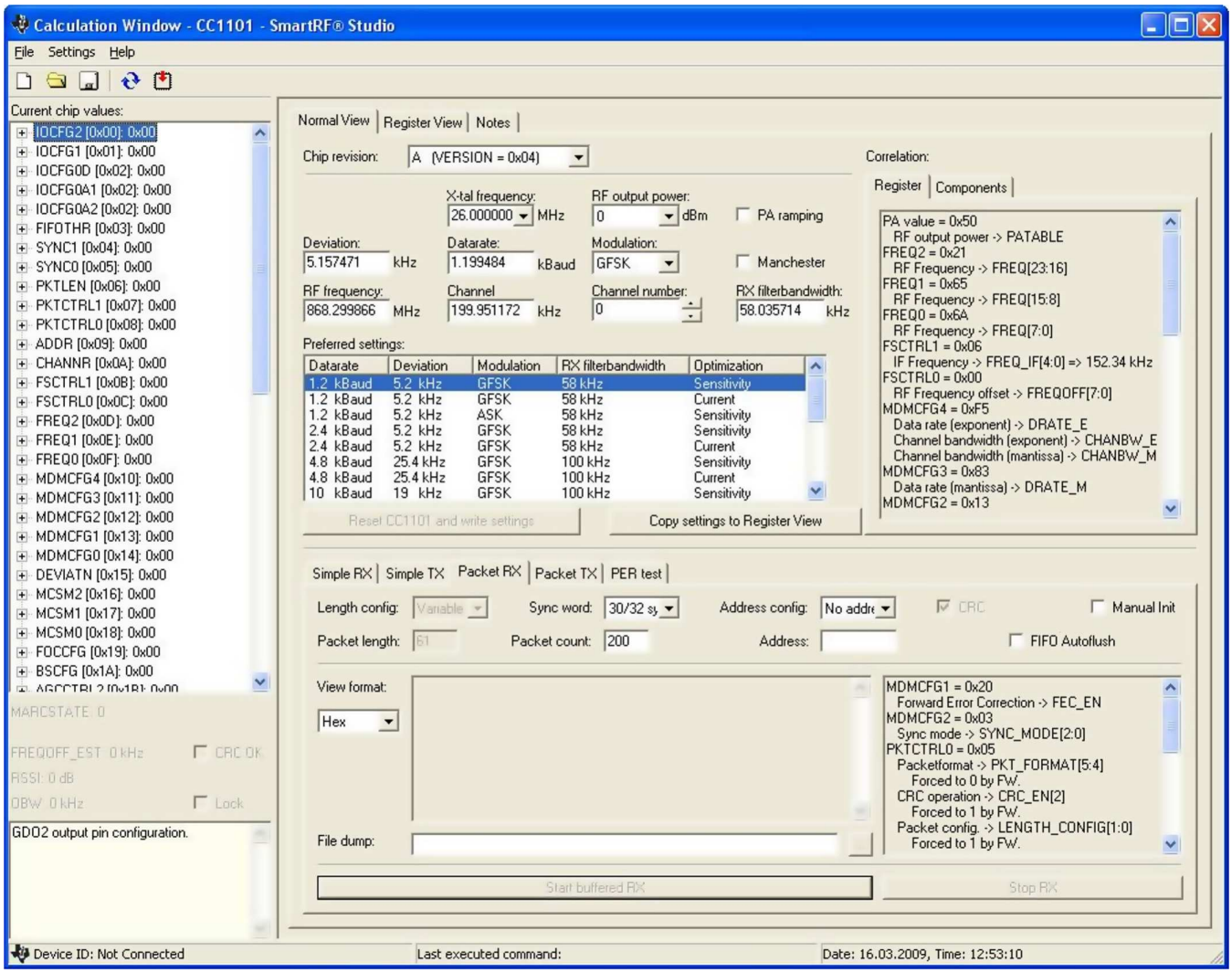

Figure 3-5. SmartRF Studio User Interface

3.6 4-Wire Serial Configuration and Data Interface

CC11x1-Q1 is configured via a simple 4-wire SPI-compatible interface (SI, SO, SCLK, and $\overline{CS}$) where CC11x1-Q1 is the slave. This interface is also used to read and write buffered data. All transfers on the SPI interface are done most significant bit first.

All transactions on the SPI interface start with a header byte containing a R/$\overline{W}$ bit, a burst access bit (B), and a 6-bit address (A_5 to A_0).

The $\overline{CS}$ pin must be kept low during transfers on the SPI bus. If $\overline{CS}$ goes high during the transfer of a header byte or during read/write from/to a register, the transfer is canceled. The timing for the address and data transfer on the SPI interface is shown in Figure 3-6 with reference to Section 2.15.

When $\overline{CS}$ is pulled low, the MCU must wait until CC11x1-Q1 SO pin goes low before starting to transfer the header byte. This indicates that the crystal is running. Unless the chip was in the SLEEP or XOFF states, the SO pin goes low immediately after taking $\overline{CS}$ low.

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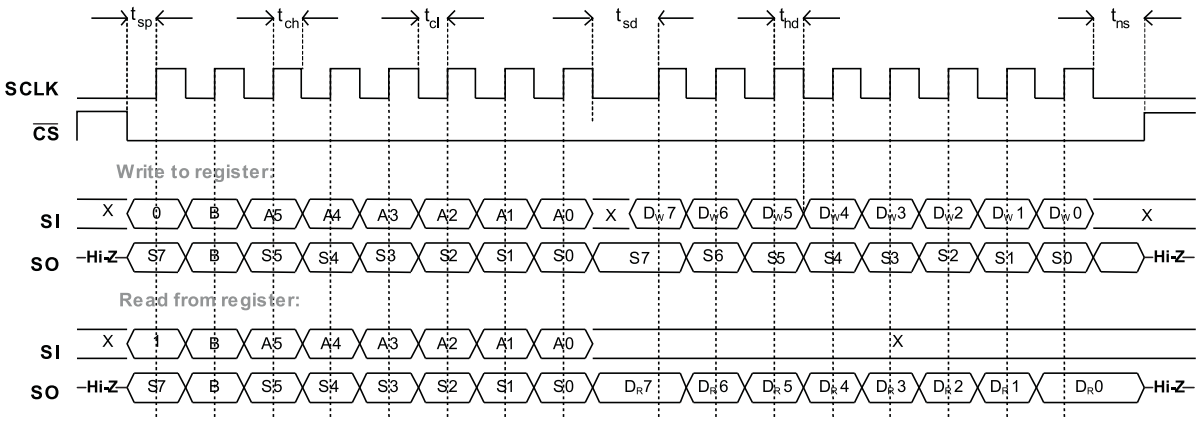

Note: See Section 2.15 for SPI interface timing specifications.

Figure 3-6. Configuration Registers Write and Read Operations

3.6.1 Chip Status Byte

When the header byte, data byte, or command strobe is sent on the SPI interface, the chip status byte is sent by the CC11x1-Q1 on the SO pin. The status byte contains key status signals, useful for the MCU. The first bit, s7, is the CHIP_RDYn signal. This signal must go low before the first positive edge of SCLK. The CHIP_RDYn signal indicates that the crystal is running.

The STATE value comprises bits 6, 5, and 4. This value reflects the state of the chip. The XOSC and power to the digital core is on in the IDLE state, but all other modules are in power down. The frequency and channel configuration should be updated only when the chip is in this state. The RX state is active when the chip is in receive mode. Likewise, TX is active when the chip is transmitting.

The last four bits (3:0) in the status byte contain FIFO_BYTES_AVAILABLE. For read operations (the R/$\overline{W}$ bit in the header byte is set to 1), the FIFO_BYTES_AVAILABLE field contains the number of bytes available for reading from the RX FIFO. For write operations (the R/$\overline{W}$ bit in the header byte is set to 0), the FIFO_BYTES_AVAILABLE field contains the number of bytes that can be written to the TX FIFO. When FIFO_BYTES_AVAILABLE = 15, 15 or more bytes are available/free.

Table 3-3 gives a status byte summary.

Table 3-3. Status Byte Summary

BITS	NAME	DESCRIPTION		
7	CHIP_RDYn	Stays high until power and crystal have stabilized. Should always be low when using the SPI interface.		
06:04	STATE[2:0]	Indicates the current main state machine mode		
		Value	**State**	**Description**
		0	IDLE	IDLE state (Also reported for some transitional states instead of SETTLING or CALIBRATE)
		1	RX	Receive mode
		10	TX	Transmit mode
		11	FSTXON	Fast TX ready
		100	CALIBRATE	Frequency synthesizer calibration is running
		101	SETTLING	PLL is settling
		110	RXFIFO_OVERFLOW	RX FIFO has overflowed. Read out any useful data, then flush the FIFO with SFRX.
		111	TXFIFO_UNDERFLOW	TX FIFO has underflowed. Acknowledge with SFTX.
03:00	FIFO_BYTES_AVAILABLE[3:0]	The number of bytes available in the RX FIFO or free bytes in the TX FIFO		

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3.6.2 Register Access

The configuration registers on the CC11x1-Q1 are located on SPI addresses from 0x00 to 0x2E. Table 4-2 lists all configuration registers. SmartRF Studio should be used to generate optimum register settings. The detailed description of each register is found in Section 4.2. All configuration registers can be both written to and read. The R/$\overline{W}$ bit controls if the register should be written to or read. When writing to registers, the status byte is sent on the SO pin each time a header byte or data byte is transmitted on the SI pin. When reading from registers, the status byte is sent on the SO pin each time a header byte is transmitted on the SI pin.

Registers with consecutive addresses can be accessed efficiently by setting the burst bit (B) in the header byte. The address bits (A5 to A0) set the start address in an internal address counter. This counter is incremented by one each new byte (every 8 clock pulses). The burst access is either a read or a write access and must be terminated by setting $\overline{CS}$ high.

For register addresses in the range 0x30 to 0x3D, the burst bit is used to select between status registers, burst bit is one, and command strobes, burst bit is zero (see 10.4 below). Because of this, burst access is not available for status registers and they must be accessed one at a time. The status registers can only be read.

3.6.3 SPI Read

When reading register fields over the SPI interface while the register fields are updated by the radio hardware (e.g., MARCSTATE or TXBYTES), there is a small, but finite, probability that a single read from the register is being corrupt. As an example, the probability of any single read from TXBYTES being corrupt, assuming the maximum data rate is used, is approximately 80 ppm. See the CC1101 errata notes (SWRZ020) for more details.

3.6.4 Command Strobes

Command strobes may be viewed as single byte instructions to CC11x1-Q1. By addressing a command strobe register, internal sequences are started. These commands are used to disable the crystal oscillator, enable receive mode, enable wake-on-radio etc. The 13 command strobes are listed in Table 4-1.

The command strobe registers are accessed by transferring a single header byte (no data is being transferred). That is, only the R/$\overline{W}$ bit, the burst access bit (set to 0), and the six address bits (in the range 0x30 through 0x3D) are written. The R/$\overline{W}$ bit can be either one or zero and determines how the FIFO_BYTES_AVAILABLE field in the status byte should be interpreted.

When writing command strobes, the status byte is sent on the SO pin.

A command strobe may be followed by any other SPI access without pulling $\overline{CS}$ high. However, if an SRES strobe is being issued, wait for SO to go low again before the next header byte is issued, as shown in Figure 3-7. The command strobes are executed immediately, with the exception of the SPWD and the SXOFF strobes that are executed when $\overline{CS}$ goes high.

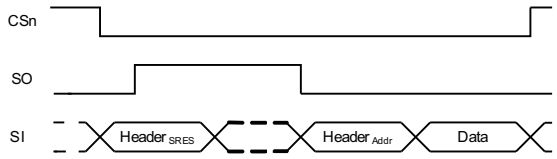

Figure 3-7. SRES Command Strobe

3.6.5 FIFO Access

The 64-byte TX FIFO and the 64-byte RX FIFO are accessed through the 0x3F address. When the R/$\overline{W}$ bit is zero, the TX FIFO is accessed, and the RX FIFO is accessed when the R/$\overline{W}$ bit is one.

The TX FIFO is write-only, while the RX FIFO is read-only.

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The burst bit is used to determine if the FIFO access is a single byte access or a burst access. The single byte access method expects a header byte with the burst bit set to zero and one data byte. After the data byte a new header byte is expected; hence, $\overline{CS}$ can remain low. The burst access method expects one header byte and then consecutive data bytes until terminating the access by setting $\overline{CS}$ high.

The following header bytes access the FIFOs:

- 0x3F: Single byte access to TX FIFO
- 0x7F: Burst access to TX FIFO
- 0xBF: Single byte access to RX FIFO
- 0xFF: Burst access to RX FIFO

When writing to the TX FIFO, the status byte (see Section 3.6.1) is output for each new data byte on SO, as shown in Figure 3-6. This status byte can be used to detect TX FIFO underflow while writing data to the TX FIFO. Note that the status byte contains the number of bytes free before writing the byte in progress to the TX FIFO. When the last byte that fits in the TX FIFO is transmitted on SI, the status byte received concurrently on SO indicates that one byte is free in the TX FIFO.

The TX FIFO may be flushed by issuing a SFTX command strobe. Similarly, a SFRX command strobe flushes the RX FIFO. A SFTX or SFRX command strobe can only be issued in the IDLE, TXFIFO_UNDERFLOW, or RXFIFO_OVERFLOW states. Both FIFOs are flushed when going to the SLEEP state.

Figure 3-8 gives a brief overview of different register access types possible.

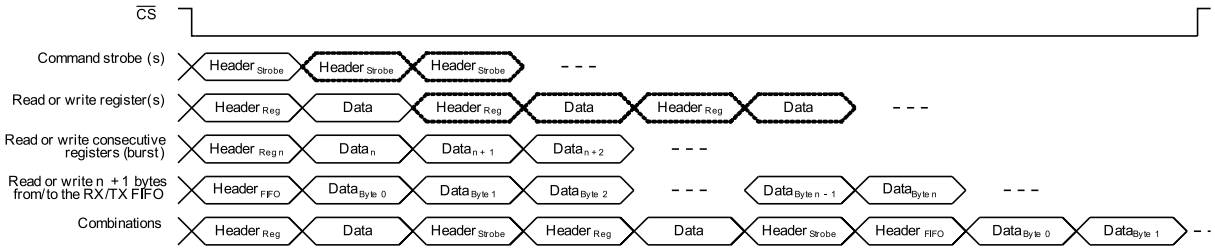

Figure 3-8. Register Access Types

3.6.6 PATABLE Access

The 0x3E address is used to access the PATABLE, which is used for selecting PA power control settings. The SPI expects up to eight data bytes after receiving the address. By programming the PATABLE, controlled PA power ramp-up and ramp-down can be achieved, as well as ASK modulation shaping for reduced bandwidth. See SmartRF Studio for recommended shaping / PA ramping sequences.

See Section 3.20 for details on output power programming.

The PATABLE is an 8-byte table that defines the PA control settings to use for each of the eight PA power values (selected by the 3-bit value FREND0.PA_POWER). The table is written and read from the lowest setting (0) to the highest (7), one byte at a time. An index counter is used to control the access to the table. This counter is incremented each time a byte is read or written to the table, and set to the lowest index when $\overline{CS}$ is high. When the highest value is reached the counter restarts at zero.

The access to the PATABLE is either single byte or burst access depending on the burst bit. When using burst access the index counter counts up; when reaching 7 the counter restarts at 0. The R/$\overline{W}$ bit controls whether the access is a read or a write access.

If one byte is written to the PATABLE and this value is to be read out then $\overline{CS}$ must be set high before the read access to set the index counter back to zero.

Note that the content of the PATABLE is lost when entering the SLEEP state, except for the first byte (index 0).

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3.7 Microcontroller Interface and Pin Configuration

In a typical system, CC11x1-Q1 interfaces to a microcontroller. This microcontroller must be able to:

- Program CC11x1-Q1 into different modes
- Read and write buffered data
- Read back status information via the 4-wire SPI-bus configuration interface (SI, SO, SCLK and $\overline{CS}$).

3.7.1 Configuration Interface

The microcontroller uses four I/O pins for the SPI configuration interface (SI, SO, SCLK and $\overline{CS}$). The SPI is described in Section 3.6.

3.7.2 General Control and Status Pins

The CC11x1-Q1 has two dedicated configurable pins (GDO0 and GDO2) and one shared pin (GDO1) that can output internal status information useful for control software. These pins can be used to generate interrupts on the MCU. See Section 3.25 for more details on the signals that can be programmed. GDO1 is shared with the SO pin in the SPI interface. The default setting for GDO1/SO is 3-state output. By selecting any other of the programming options, the GDO1/SO pin becomes a generic pin. When $\overline{CS}$ is low, the pin functions as a normal SO pin.

In the synchronous and asynchronous serial modes, the GDO0 pin is used as a serial TX data input pin while in transmit mode.

The GDO0 pin can also be used for an on-chip analog temperature sensor. By measuring the voltage on the GDO0 pin with an external ADC, the temperature can be calculated. Specifications for the temperature sensor are found in Section 2.12.

With default PTEST register setting (0x7F) the temperature sensor output is available only when the frequency synthesizer is enabled (e.g., the MANCAL, FSTXON, RX, and TX states). It is necessary to write 0xBF to the PTEST register to use the analog temperature sensor in the IDLE state. Before leaving the IDLE state, the PTEST register should be restored to its default value (0x7F).

3.7.3 Optional Radio-Control Feature

The CC11x1-Q1 has an optional way of controlling the radio by reusing SI, SCLK, and $\overline{CS}$ from the SPI interface. This allows simple three-pin control of the major states of the radio: SLEEP, IDLE, RX, and TX.

This optional functionality is enabled with the MCSM0.PIN_CTRL_EN configuration bit.

State changes are commanded as follows: When $\overline{CS}$ is high, the SI and SCLK is set to the desired state according to Table 3-4. When $\overline{CS}$ goes low, the state of SI and SCLK is latched and a command strobe is generated internally according to the pin configuration. It is only possible to change state with this functionality. That means that, for instance, RX is not restarted if SI and SCLK are set to RX and $\overline{CS}$ toggles. When $\overline{CS}$ is low, the SI and SCLK has normal SPI functionality.

All pin control command strobes are executed immediately, except the SPWD strobe, which is delayed until $\overline{CS}$ goes high.

Table 3-4. Optional Pin Control Coding

$\overline{CS}$	SCLK	SI	FUNCTION
1	X	X	Chip unaffected by SCLK/SI
↓	0	0	Generates SPWD strobe
↓	0	1	Generates STX strobe
↓	1	0	Generates SIDLE strobe
↓	1	1	Generates SRX strobe
0	SPI mode	SPI mode	SPI mode (wakes up into IDLE if in SLEEP/XOFF)

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3.8 Data Rate Programming

The data rate used when transmitting, or the data rate expected in receive is programmed by the MDMCFG3.DRATE_M and the MDMCFG4.DRATE_E configuration registers. The data rate is given by the formula below. As the formula shows, the programmed data rate depends on the crystal frequency.

$$R_{DATA} = \frac{(256+DRATE_M) \times 2^{DRATE_E}}{2^{28}} \times f_{XOSC} \quad (1)$$

The following approach can be used to find suitable values for a given data rate:

$$DRATE_E = \left\lfloor \log_2 \left(\frac{R_{DATA} \times 2^{20}}{f_{XOSC}} \right) \right\rfloor$$

$$DRATE_M = \frac{R_{DATA} \times 2^{28}}{f_{XOSC} \times 2^{DRATE_E}} - 256 \quad (2)$$

If DRATE_M is rounded to the nearest integer and becomes 256, increment DRATE_E and use DRATE_M = 0.

The data rate can be set from 1.2 kBaud to 500 kBaud with the minimum step size shown in Table 3-5.

Table 3-5. Data Rate Step Size

DATA RATE (kBaud)			DATA RATE STEP SIZE (kBaud)
MINIMUM	TYPICAL	MAXIMUM	
0.8	1.2 / 2.4	3.17	0.0062
3.17	4.8	6.35	0.0124
6.35	9.6	12.7	0.0248
12.7	19.6	25.4	0.0496
25.4	38.4	50.8	0.0992
50.8	76.8	101.6	0.1984
101.6	153.6	203.1	0.3967
203.1	250	406.3	0.7935

3.9 Receiver Channel Filter Bandwidth

To meet different channel width requirements, the receiver channel filter is programmable. The MDMCFG4.CHANBW_E and MDMCFG4.CHANBW_M configuration registers control the receiver channel filter bandwidth, which scales with the crystal oscillator frequency. Equation 3 gives the relation between the register settings and the channel filter bandwidth:

$$BW_{channel} = \frac{f_{XOSC}}{8 \times (4 + CHANBW_M) \times 2^{CHANBW_E}} \quad (3)$$

The CC11x1-Q1 supports the channel filter bandwidths shown in Table 3-6.

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Table 3-6. Channel Filter Bandwidths (kHz) (Assuming a 26-MHz Crystal)

MDMCFG4. CHANBW_M	MDMCFG4.CHANBW_E			
	00	01	10	11
00	812	406	203	102
01	650	325	162	81
10	541	270	135	68
11	464	232	116	58

For best performance, the channel filter bandwidth should be selected so that the signal bandwidth occupies at most 80% of the channel filter bandwidth. The channel center tolerance due to crystal accuracy should also be subtracted from the signal bandwidth, as shown in the following example.

With the channel filter bandwidth set to 500 kHz, the signal should stay within 80% of 500 kHz, which is 400 kHz. Assuming 915-MHz frequency and ±20-ppm frequency uncertainty for both the transmitting device and the receiving device, the total frequency uncertainty is ±40 ppm of 915 MHz, which is ±37 kHz. If the whole transmitted signal bandwidth is to be received within 400 kHz, the transmitted signal bandwidth should be maximum 400 kHz – (2 × 37 kHz), which is 326 kHz.

3.10 Demodulator, Symbol Synchronizer, and Data Decision

CC11x1-Q1 contains an advanced and highly configurable demodulator. Channel filtering and frequency offset compensation are performed digitally. To generate the RSSI level (see Section 3.13.3 for more information) the signal level in the channel is estimated. Data filtering is also included for enhanced performance.

3.10.1 Frequency Offset Compensation

When using 2-FSK, GFSK, or MSK modulation, the demodulator compensates for the offset between the transmitter and receiver frequency, within certain limits, by estimating the center of the received data. This value is available in the FREQEST status register. Writing the value from FREQEST into FSCTRL0.FREQOFF the frequency synthesizer is automatically adjusted according to the estimated frequency offset.

The tracking range of the algorithm is selectable as fractions of the channel bandwidth with the FOCCFG.FOC_LIMIT configuration register.

If the FOCCFG.FOC_BS_CS_GATE bit is set, the offset compensator freezes until carrier sense asserts. This may be useful when the radio is in RX for long periods with no traffic, because the algorithm may drift to the boundaries when trying to track noise.

The tracking loop has two gain factors, which affect the settling time and noise sensitivity of the algorithm. FOCCFG.FOC_PRE_K sets the gain before the sync word is detected, and FOCCFG.FOC_POST_K selects the gain after the sync word has been found.

NOTE

Frequency offset compensation is not supported for ASK or OOK modulation.

3.10.2 Bit Synchronization

The bit synchronization algorithm extracts the clock from the incoming symbols. The algorithm requires that the expected data rate is programmed as described in Section 3.8. Resynchronization is performed continuously to adjust for error in the incoming symbol rate.

3.10.3 Byte Synchronization

Byte synchronization is achieved by a continuous sync word search. The sync word is a 16-bit configurable field (can be repeated to get a 32 bit) that is automatically inserted at the start of the packet

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by the modulator in transmit mode. The demodulator uses this field to find the byte boundaries in the stream of bits. The sync word also functions as a system identifier, because only packets with the correct predefined sync word are received if the sync word detection in RX is enabled in register MDMCFG2 (see Section 3.13.1). The sync word detector correlates against the user-configured 16- or 32-bit sync word. The correlation threshold can be set to 15/16, 16/16, or 30/32 bits match. The sync word can be further qualified using the preamble quality indicator mechanism described below and/or a carrier sense condition. The sync word is configured through the SYNC1 and SYNC0 registers.

To make false detections of sync words less likely, a mechanism called preamble quality indication (PQI) can be used to qualify the sync word. A threshold value for the preamble quality must be exceeded in order for a detected sync word to be accepted. See Section 3.13.2 for more details.

3.11 Packet Handling Hardware Support

The CC11x1-Q1 has built-in hardware support for packet oriented radio protocols.

In transmit mode, the packet handler can be configured to add the following elements to the packet stored in the TX FIFO:

- A programmable number of preamble bytes
- A two byte synchronization (sync) word. Can be duplicated to give a 4-byte sync word (recommended). It is not possible to insert only preamble or insert only a sync word.
- A CRC checksum computed over the data field.

The recommended setting is 4-byte preamble and 4-byte sync word, except for 500 kBaud data rate where the recommended preamble length is 8 bytes.

In addition, the following can be implemented on the data field and the optional 2-byte CRC checksum:

- Whitening of the data with a PN9 sequence.
- Forward error correction by the use of interleaving and coding of the data (convolutional coding)

In receive mode, the packet handling support deconstructs the data packet by implementing the following (if enabled):

- Preamble detection
- Sync word detection
- CRC computation and CRC check
- One byte address check
- Packet length check (length byte checked against a programmable maximum length)
- Dewhitening
- Deinterleaving and decoding

Optionally, two status bytes (see Table 3-7 and Table 3-8) with RSSI value, Link Quality Indication, and CRC status can be appended in the RX FIFO.

Table 3-7. Received Packet Status Byte 1 (First Byte Appended After Data)

BIT	FIELD NAME	DESCRIPTION
7:0	RSSI	RSSI value

Table 3-8. Received Packet Status Byte 2 (Second Byte Appended After Data)

BIT	FIELD NAME	DESCRIPTION
7	CRC_OK	1: CRC for received data OK (or CRC disabled) 0: CRC error in received data
6:0	LQI	Indicating the link quality

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NOTE

Register fields that control the packet handling features should be altered only when CC11x1-Q1 is in the IDLE state.

3.11.1 Data Whitening

From a radio perspective, the ideal over-the-air data are random and dc free. This results in the smoothest power distribution over the occupied bandwidth. This also gives the regulation loops in the receiver uniform operation conditions (no data dependencies).

Real-world data often contain long sequences of zeros and ones. Performance can then be improved by whitening the data before transmitting, and dewhitening the data in the receiver. With CC11x1-Q1, this can be done automatically by setting PKTCTRL0.WHITE_DATA = 1. All data, except the preamble and the sync word, are then XORed with a 9-bit pseudo-random (PN9) sequence before being transmitted, as shown in Figure 3-9. At the receiver end, the data are XORed with the same pseudo-random sequence. This way, the whitening is reversed, and the original data appear in the receiver. The PN9 sequence is initialized to all ones.

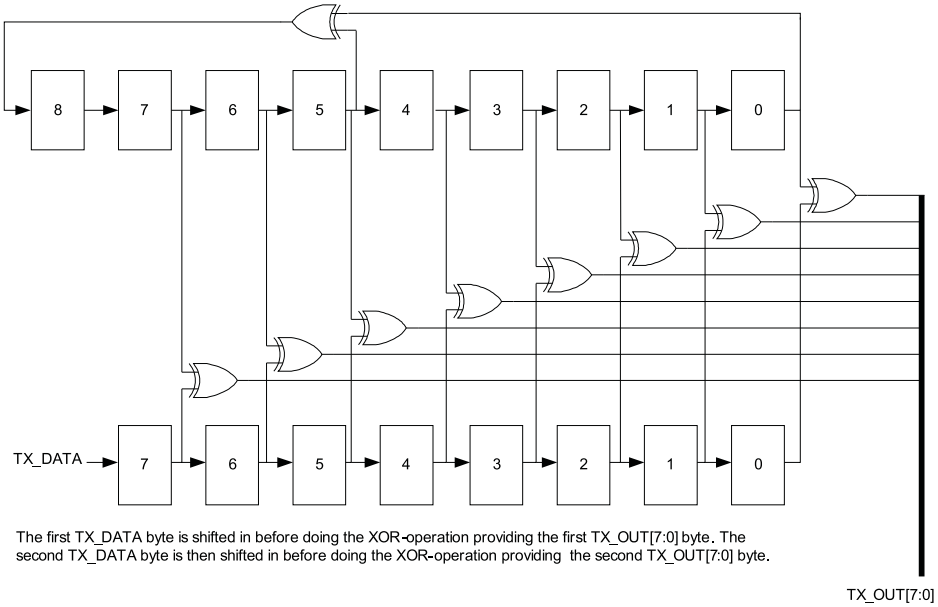

Figure 3-9. Data Whitening in TX Mode

3.11.2 Packet Format

The format of the data packet can be configured and consists of the following items (see Figure 3-10):

- Preamble
- Synchronization word
- Optional length byte
- Optional address byte
- Payload
- Optional 2-byte CRC

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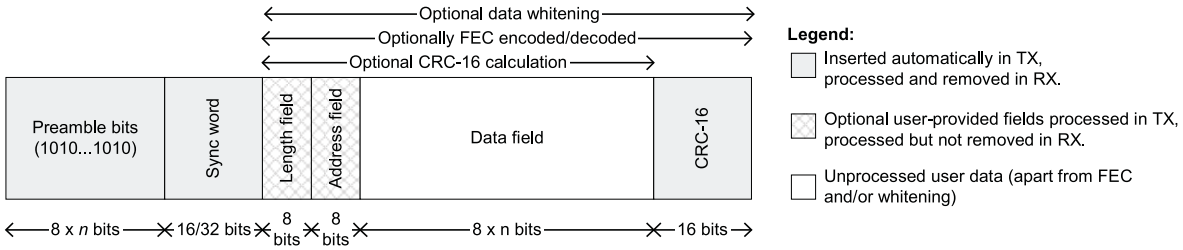

Figure 3-10. Packet Format

The preamble pattern is an alternating sequence of ones and zeros (10101010…). The minimum length of the preamble is programmable. When enabling TX, the modulator starts transmitting the preamble. When the programmed number of preamble bytes has been transmitted, the modulator sends the sync word and then data from the TX FIFO if data is available. If the TX FIFO is empty, the modulator continues to send preamble bytes until the first byte is written to the TX FIFO. The modulator then sends the sync word and then the data bytes. The number of preamble bytes is programmed with the MDMCFG1.NUM_PREAMBLE value.

The synchronization word is a two-byte value set in the SYNC1 and SYNC0 registers. The sync word provides byte synchronization of the incoming packet. A one-byte synch word can be emulated by setting the SYNC1 value to the preamble pattern. It is also possible to emulate a 32-bit sync word by using MDMCFG2.SYNC_MODE set to 3 or 7. The sync word is then repeated twice.

CC11x1-Q1 supports both constant packet length protocols and variable length protocols. Variable or fixed packet length mode can be used for packets up to 255 bytes. For longer packets, infinite packet length mode must be used.

Fixed packet length mode is selected by setting PKTCTRL0.LENGTH_CONFIG = 0. The desired packet length is set by the PKTLEN register.

In variable packet length mode, PKTCTRL0.LENGTH_CONFIG = 1, the packet length is configured by the first byte after the sync word. The packet length is defined as the payload data, excluding the length byte and the optional CRC. The PKTLEN register is used to set the maximum packet length allowed in RX. Any packet received with a length byte with a value greater than PKTLEN is discarded.

With PKTCTRL0.LENGTH_CONFIG = 2, the packet length is set to infinite, and transmission and reception continues until turned off manually. As described in the next section, this can be used to support packet formats with different length configuration than natively supported by CC11x1-Q1. One should make sure that TX mode is not turned off during the transmission of the first half of any byte. Refer to the errata notes for more details.

NOTE

The minimum packet length supported (excluding the optional length byte and CRC) is one byte of payload data.

3.11.2.1 Arbitrary Length Field Configuration

The packet length register, PKTLEN, can be reprogrammed during receive and transmit. In combination with fixed packet length mode (PKTCTRL0.LENGTH_CONFIG = 0) this opens the possibility to have a different length field configuration than supported for variable length packets (in variable packet length mode the length byte is the first byte after the sync word). At the start of reception, the packet length is set to a large value. The MCU reads out enough bytes to interpret the length field in the packet. Then the PKTLEN value is set according to this value. The end of packet occurs when the byte counter in the packet handler is equal to the PKTLEN register. Thus, the MCU must be able to program the correct length, before the internal counter reaches the packet length.

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3.11.2.2 Packet Length Greater Than 255

Also the packet automation control register, PKTCTRL0, can be reprogrammed during TX and RX. This opens the possibility to transmit and receive packets that are longer than 256 bytes and still be able to use the packet handling hardware support. At the start of the packet, the infinite packet length mode (PKTCTRL0.LENGTH_CONFIG = 2) must be active. On the TX side, the PKTLEN register is set to mod(length, 256). On the RX side the MCU reads out enough bytes to interpret the length field in the packet and sets the PKTLEN register to mod(length, 256). When less than 256 bytes remain of the packet, the MCU disables infinite packet length mode and activates fixed packet length mode. When the internal byte counter reaches the PKTLEN value, the transmission or reception ends (the radio enters the state determined by TXOFF_MODE or RXOFF_MODE). Automatic CRC appending/checking can also be used (by setting PKTCTRL0.CRC_EN = 1).

When for example a 600-byte packet is to be transmitted, the MCU should do the following (see also Figure 3-11).

1. Set PKTCTRL0.LENGTH_CONFIG = 2.
2. Preprogram the PKTLEN register to mod(600, 256) = 88.
3. Transmit at least 345 bytes (600 – 255), for example by filling the 64-byte TX FIFO six times (384 bytes transmitted).
4. Set PKTCTRL0.LENGTH_CONFIG = 0.
5. The transmission ends when the packet counter reaches 88. A total of 600 bytes are transmitted.

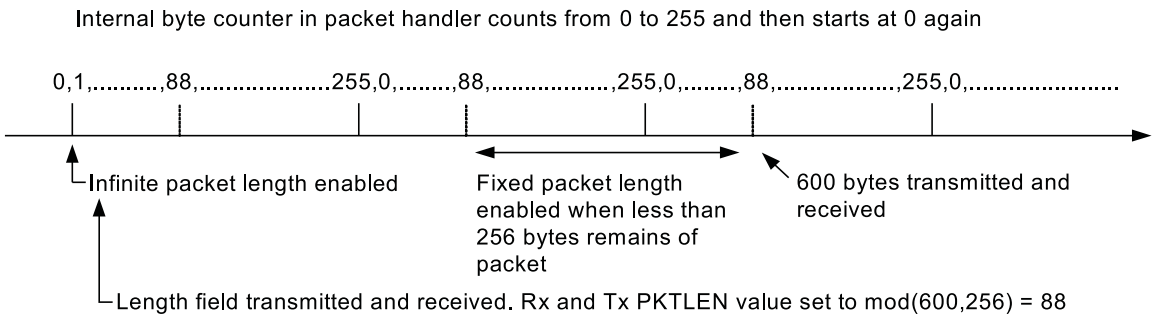

Figure 3-11. Packet Length Greater Than 255

3.11.3 Packet Filtering in Receive Mode

CC11x1-Q1 supports three different types of packet filtering: address filtering, maximum length filtering, and CRC filtering.

3.11.3.1 Address Filtering

Setting PKTCTRL1.ADR_CHK to any other value than zero enables the packet address filter. The packet handler engine compares the destination address byte in the packet with the programmed node address in the ADDR register and the 0x00 broadcast address when PKTCTRL1.ADR_CHK = 10 or both 0x00 and 0xFF broadcast addresses when PKTCTRL1.ADR_CHK = 11. If the received address matches a valid address, the packet is received and written into the RX FIFO. If the address match fails, the packet is discarded and receive mode restarted (regardless of the MCSM1.RXOFF_MODE setting).

If the received address matches a valid address when using infinite packet length mode and address filtering is enabled, 0xFF is written into the RX FIFO followed by the address byte and then the payload data.

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3.11.3.2 Maximum Length Filtering

In variable packet length mode, PKTCTRL0.LENGTH_CONFIG = 1, the PKTLEN.PACKET_LENGTH register value is used to set the maximum allowed packet length. If the received length byte has a larger value than this, the packet is discarded and receive mode restarted (regardless of the MCSM1.RXOFF_MODE setting).

3.11.3.3 CRC Filtering

The filtering of a packet when CRC check fails is enabled by setting PKTCTRL1.CRC_AUTOFLUSH = 1. The CRC auto flush function flushes the entire RX FIFO if the CRC check fails. After auto flushing the RX FIFO, the next state depends on the MCSM1.RXOFF_MODE setting.

When using the auto flush function, the maximum packet length is 63 bytes in variable packet length mode and 64 bytes in fixed packet length mode. Note that the maximum allowed packet length is reduced by two bytes when PKTCTRL1.APPEND_STATUS is enabled, to make room in the RX FIFO for the two status bytes appended at the end of the packet. Because the entire RX FIFO is flushed when the CRC check fails, the previously received packet must be read out of the FIFO before receiving the current packet. The MCU must not read from the current packet until the CRC has been checked as OK.

3.11.4 Packet Handling in Transmit Mode

The payload that is to be transmitted must be written into the TX FIFO. The first byte written must be the length byte when variable packet length is enabled. The length byte has a value equal to the payload of the packet (including the optional address byte). If address recognition is enabled on the receiver, the second byte written to the TX FIFO must be the address byte. If fixed packet length is enabled, then the first byte written to the TX FIFO should be the address (if the receiver uses address recognition).

The modulator first sends the programmed number of preamble bytes. If data is available in the TX FIFO, the modulator sends the two-byte (optionally four-byte) sync word and then the payload in the TX FIFO. If CRC is enabled, the checksum is calculated over all the data pulled from the TX FIFO and the result is sent as two extra bytes following the payload data. If the TX FIFO runs empty before the complete packet has been transmitted, the radio enters TXFIFO_UNDERFLOW state. The only way to exit this state is by issuing an SFTX strobe. Writing to the TX FIFO after it has underflowed does not restart TX mode.

If whitening is enabled, everything following the sync words is whitened. This is done before the optional FEC/Interleaver stage. Whitening is enabled by setting PKTCTRL0.WHITE_DATA = 1.

If FEC/Interleaving is enabled, everything following the sync words is scrambled by the interleaver and FEC encoded before being modulated. FEC is enabled by setting MDMCFG1.FEC_EN = 1.

3.11.5 Packet Handling in Receive Mode

In receive mode, the demodulator and packet handler searches for a valid preamble and the sync word. When found, the demodulator has obtained both bit and byte synchronism and receives the first payload byte.

If FEC/Interleaving is enabled, the FEC decoder starts to decode the first payload byte. The interleaver descrambles the bits before any other processing is done to the data.

If whitening is enabled, the data is dewhitened at this stage.

When variable packet length mode is enabled, the first byte is the length byte. The packet handler stores this value as the packet length and receives the number of bytes indicated by the length byte. If fixed packet length mode is used, the packet handler accepts the programmed number of bytes.

Next, the packet handler optionally checks the address and only continues the reception if the address matches. If automatic CRC check is enabled, the packet handler computes CRC and matches it with the appended CRC checksum.

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At the end of the payload, the packet handler optionally writes two extra packet status bytes (see Table 3-7 and Table 3-8) that contain CRC status, link quality indication, and RSSI value.

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3.11.6 Packet Handling in Firmware

When implementing a packet oriented radio protocol in firmware, the MCU needs to know when a packet has been received/transmitted. Additionally, for packets longer than 64 bytes the RX FIFO needs to be read while in RX and the TX FIFO needs to be refilled while in TX. This means that the MCU needs to know the number of bytes that can be read from or written to the RX FIFO and TX FIFO respectively. There are two possible solutions to get the necessary status information:

Interrupt Driven Solution

In both RX and TX one can use one of the GDO pins to give an interrupt when a sync word has been received/transmitted and/or when a complete packet has been received/transmitted (IOCFGx.GDOx_CFG = 0x06). In addition, there are two configurations for the IOCFGx.GDOx_CFG register that are associated with the RX FIFO (IOCFGx.GDOx_CFG = 0x00 and IOCFGx.GDOx_CFG = 0x01) and two that are associated with the TX FIFO (IOCFGx.GDOx_CFG = 0x02 and IOCFGx.GDOx_CFG = 0x03) that can be used as interrupt sources to provide information on how many bytes are in the RX FIFO and TX FIFO respectively (see Table 3-17).

SPI Polling

The PKTSTATUS register can be polled at a given rate to get information about the current GDO2 and GDO0 values respectively. The RXBYTES and TXBYTES registers can be polled at a given rate to get information about the number of bytes in the RX FIFO and TX FIFO respectively. Alternatively, the number of bytes in the RX FIFO and TX FIFO can be read from the chip status byte returned on the MISO line each time a header byte, data byte, or command strobe is sent on the SPI bus.

An interrupt-driven solution should be used, as high-rate SPI polling reduces the RX sensitivity. Furthermore, as explained in Section 3.6.3 and the errata notes, when using SPI polling, there is a small, but finite, probability that a single read from registers PKTSTATUS , RXBYTES, and TXBYTES is corrupt. The same is the case when reading the chip status byte.

See the TI web site for software examples.

3.12 Modulation Formats

CC11x1-Q1 supports amplitude, frequency, and phase shift modulation formats. The desired modulation format is set in the MDMCFG2.MOD_FORMAT register.

Optionally, the data stream can be Manchester coded by the modulator and decoded by the demodulator. This option is enabled by setting MDMCFG2.MANCHESTER_EN = 1. Manchester encoding is not supported at the same time as using the FEC/Interleaver option.

3.12.1 Frequency Shift Keying

CC11x1-Q1 can use Gaussian shaped 2-FSK (GFSK). The 2-FSK signal is then shaped by a Gaussian filter with BT = 1, producing a GFSK modulated signal. This spectrum-shaping feature improves adjacent channel power (ACP) and occupied bandwidth.

In 'true' 2-FSK systems with abrupt frequency shifting, the spectrum is inherently broad. By making the frequency shift 'softer', the spectrum can be made significantly narrower. Thus, higher data rates can be transmitted in the same bandwidth using GFSK.

When FSK/GFSK modulation is used, the DEVIATN register specifies the expected frequency deviation of incoming signals in RX and should be the same as the TX deviation for demodulation to be performed reliably and robustly.

The frequency deviation is programmed with the DEVIATION_M and DEVIATION_E values in the DEVIATN register. The value has an exponent/mantissa form, and the resultant deviation is given by:

$$f_{dev} = \frac{f_{xosc}}{2^{17}} \times (8 + \text{DEVIATION_M}) \times 2^{\text{DEVIATION_E}} \quad (4)$$

The symbol encoding is shown in Table 3-9.

Table 3-9. Symbol Encoding for 2-FSK/GFSK Modulation

FORMAT	SYMBOL	CODING
2-FSK/GFSK	0	– Deviation
	1	+ Deviation

3.12.2 Minimum Shift Keying

When using MSK [identical to offset QPSK with half-sine shaping (data coding may differ)], the complete transmission (preamble, sync word, and payload) is MSK modulated. Phase shifts are performed with a constant transition time. The fraction of a symbol period used to change the phase can be modified with the DEVIATN.DEVIATION_M setting. This is equivalent to changing the shaping of the symbol. The MSK modulation format implemented in CC11x1-Q1 inverts the sync word and data compared to, e.g., signal generators.

3.12.3 Amplitude Modulation

CC11x1-Q1 supports two different forms of amplitude modulation: On-Off Keying (OOK) and Amplitude Shift Keying (ASK).

OOK modulation simply turns on or off the PA to modulate 1 and 0 respectively.

The ASK variant supported by the CC11x1-Q1 allows programming of the modulation depth (the difference between 1 and 0), and shaping of the pulse amplitude. Pulse shaping produces a more bandwidth constrained output spectrum.

3.13 Received Signal Qualifiers and Link Quality Information

CC11x1-Q1 has several qualifiers that can be used to increase the likelihood that a valid sync word is detected.

3.13.1 Sync Word Qualifier

If sync word detection in RX is enabled in register MDMCFG2, the CC11x1-Q1 does not start filling the RX FIFO and performing the packet filtering described in Section 3.11.3.3 before a valid sync word has been detected. The sync word qualifier mode is set by MDMCFG2.SYNC_MODE and is summarized in Table 3-10. Carrier sense is described in Section 3.13.4.

Table 3-10. Sync Word Qualifier Mode

MDMCFG2.SYNC_MODE	SYNC WORD QUALIFIER MODE
000	No preamble/sync
001	15/16 sync word bits detected
010	16/16 sync word bits detected
011	30/32 sync word bits detected
100	No preamble/sync, carrier sense above threshold
101	15/16 + carrier sense above threshold
110	16/16 + carrier sense above threshold
111	30/32 + carrier sense above threshold

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3.13.2 Preamble Quality Threshold (PQT)

The preamble quality threshold (PQT) sync-word qualifier adds the requirement that the received sync word must be preceded with a preamble with a quality above the programmed threshold.

Another use of the preamble quality threshold is as a qualifier for the optional RX termination timer. See Section 3.15.7 for details.

The preamble quality estimator increases an internal counter by one each time a bit is received that is different from the previous bit, and decreases the counter by 8 each time a bit is received that is the same as the last bit. The threshold is configured with the register field PKTCTRL1.PQT. A threshold of 4 × PQT for this counter is used to gate sync word detection. By setting the value to zero, the preamble quality qualifier of the synch word is disabled.

A preamble quality reached signal can be observed on one of the GDO pins by setting IOCFGx.GDOx_CFG = 8. It is also possible to determine if preamble quality is reached by checking the PQT_REACHED bit in the PKTSTATUS register. This signal/bit asserts when the received signal exceeds the PQT.

3.13.3 RSSI

The RSSI value is an estimate of the signal power level in the chosen channel. This value is based on the current gain setting in the RX chain and the measured signal level in the channel.

In RX mode, the RSSI value can be read continuously from the RSSI status register until the demodulator detects a sync word (when sync word detection is enabled). At that point the RSSI readout value is frozen until the next time the chip enters the RX state. The RSSI value is in dBm with ½-dB resolution. The RSSI update rate, f_{RSSI}, depends on the receiver filter bandwidth ($BW_{channel}$ defined in Section 3.9) and AGCCTRL0.FILTER_LENGTH.

$$f_{RSSI}=\frac{2\times BW_{channel}}{8\times 2^{FILTER_LENGTH}} \quad (5)$$

If PKTCTRL1.APPEND_STATUS is enabled the last RSSI value of the packet is automatically added to the first byte appended after the payload.

The RSSI value read from the RSSI status register is a twos-complement number. The following procedure can be used to convert the RSSI reading to an absolute power level (RSSI_dBm).

1. Read the RSSI status register
2. Convert the reading from a hexadecimal number to a decimal number (RSSI_dec)
3. If RSSI_dec ≥ 128 then RSSI_dBm = (RSSI_dec – 256)/2 – RSSI_offset
4. Else if RSSI_dec < 128 then RSSI_dBm = (RSSI_dec)/2 – RSSI_offset

Table 3-11 gives typical values for the RSSI_offset. Figure 3-12 and Figure 3-13 shows typical plots of RSSI reading as a function of input power level for different data rates.

Table 3-11. Typical RSSI_offset Values

DATA RATE (kBaud)	RSSI_offset (dB), 433 MHz	RSSI_offset (dB), 868 MHz
1.2	74	74
38.4	74	74
250	74	74

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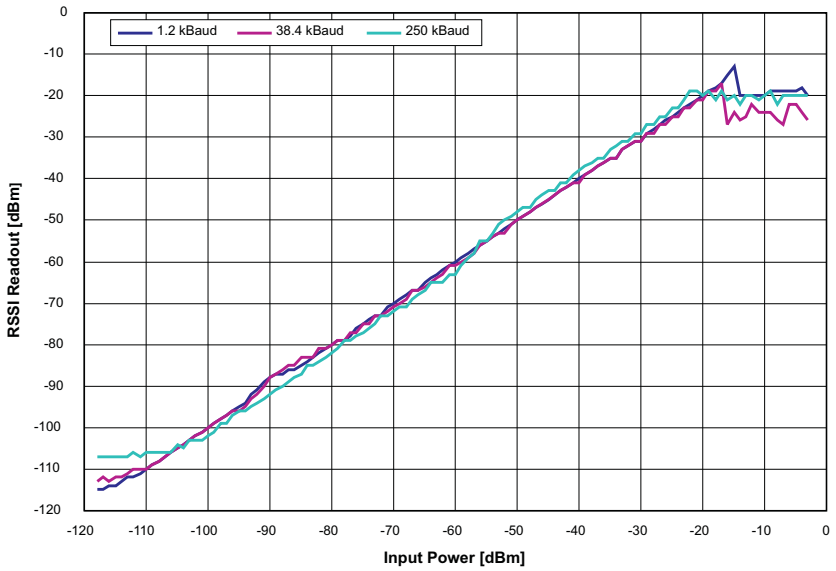

Figure 3-12. Typical RSSI Value vs Input Power Level for Different Data Rates at 433 MHz

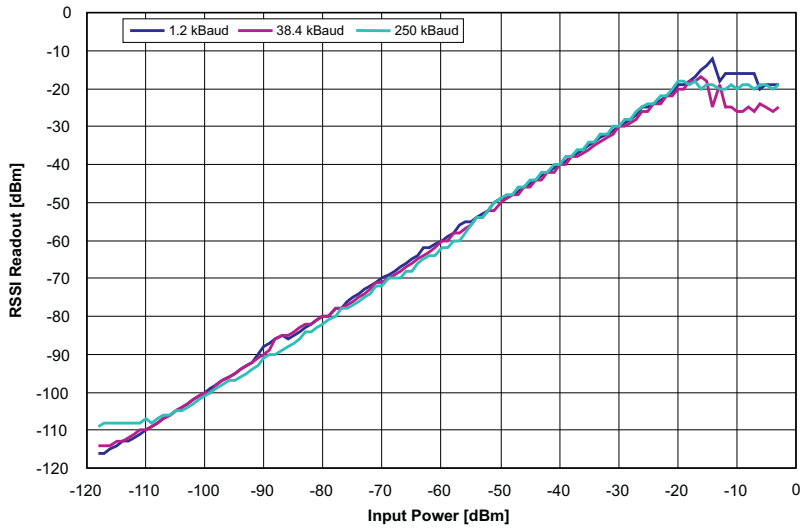

Figure 3-13. Typical RSSI Value vs Input Power Level for Different Data Rates at 868 MHz

3.13.4 Carrier Sense (CS)

Carrier sense (CS) is used as a sync word qualifier and for CCA and can be asserted based on two conditions, which can be individually adjusted:

- CS is asserted when the RSSI is above a programmable absolute threshold and deasserted when RSSI is below the same threshold (with hysteresis).
- CS is asserted when the RSSI has increased with a programmable number of dB from one RSSI sample to the next and deasserted when RSSI has decreased with the same number of dB. This setting is not dependent on the absolute signal level and is thus useful to detect signals in environments with time varying noise floor.

Carrier sense can be used as a sync word qualifier that requires the signal level to be higher than the threshold for a sync word search to be performed. The signal can also be observed on one of the GDO pins by setting IOCFGx.GDOx_CFG = 14 and in the status register bit PKTSTATUS.CS.

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Other uses of carrier sense include the TX-if-CCA function (see Section 3.13.5) and the optional fast RX termination (see Section 3.15.7).

CS can be used to avoid interference from other RF sources in the ISM bands.

3.13.4.1 CS Absolute Threshold

The absolute threshold related to the RSSI value depends on the following register fields:

- AGCCTRL2.MAX_LNA_GAIN
- AGCCTRL2.MAX_DVGA_GAIN
- AGCCTRL1.CARRIER_SENSE_ABS_THR
- AGCCTRL2.MAGN_TARGET

For a given AGCCTRL2.MAX_LNA_GAIN and AGCCTRL2.MAX_DVGA_GAIN setting the absolute threshold can be adjusted ±7 dB in steps of 1 dB using CARRIER_SENSE_ABS_THR.

The MAGN_TARGET setting is a compromise between blocker tolerance/selectivity and sensitivity. The value sets the desired signal level in the channel into the demodulator. Increasing this value reduces the headroom for blockers, and therefore close-in selectivity.

It is strongly recommended to use SmartRF Studio to generate the correct MAGN_TARGET setting.

Table 3-12 and Table 3-13 show the typical RSSI readout values at the CS threshold at 2.4 kBaud and 250 kBaud data rate respectively. The default CARRIER_SENSE_ABS_THR = 0 (0 dB) and MAGN_TARGET = 3 (33 dB) have been used.

For other data rates the user must generate similar tables to find the CS absolute threshold.

Table 3-12. Typical RSSI Value in dBm at CS Threshold With Default MAGN_TARGET at 2.4 kBaud, 868 MHz

		MAX_DVGA_GAIN[1:0]			
		00	**01**	**10**	**11**
MAX_LNA_GAIN[2:0]	**000**	–97.5	–91.5	–85.5	–79.5
	001	–94	–88	–82.5	–76
	010	–90.5	–84.5	–78.5	–72.5
	011	–88	–82.5	–76.5	–70.5
	100	–85.5	–80	–73.5	–68
	101	–84	–78	–72	–66
	110	–82	–76	–70	–64
	111	–79	–73.5	–67	–61

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Table 3-13. Typical RSSI Value in dBm at CS Threshold With Default MAGN_TARGET at 250 kBaud, 868 MHz

		MAX_DVGA_GAIN[1:0]			
		00	**01**	**10**	**11**
MAX_LNA_GAIN[2:0]	**000**	–90.5	–84.5	–78.5	–72.5
	001	–88	–82	–76	–70
	010	–84.5	–78.5	–72	–66
	011	–82.5	–76.5	–70	–64
	100	–80.5	–74.5	–68	–62
	101	–78	–72	–66	–60
	110	–76.5	–70	–64	–58
	111	–74.5	–68	–62	–56

If the threshold is set high (i.e., only strong signals are wanted) the threshold should be adjusted upwards by first reducing the MAX_LNA_GAIN value and then the MAX_DVGA_GAIN value. This reduces power consumption in the receiver front end, because the highest gain settings are avoided.

3.13.4.2 CS Relative Threshold

The relative threshold detects sudden changes in the measured signal level. This setting is not dependent on the absolute signal level and is thus useful to detect signals in environments with a time varying noise floor. The register field AGCCTRL1.CARRIER_SENSE_REL_THR is used to enable/disable relative CS, and to select threshold of 6 dB, 10 dB, or 14 dB RSSI change.

3.13.5 Clear Channel Assessment (CCA)

The Clear Channel Assessment (CCA) is used to indicate if the current channel is free or busy. The current CCA state is viewable on any of the GDO pins by setting IOCFGx.GDOx_ CFG = 0x09.

MCSM1.CCA_MODE selects the mode to use when determining CCA.

When the STX or SFSTXON command strobe is given while CC11x1-Q1 is in the RX state, the TX or FSTXON state is only entered if the clear channel requirements are fulfilled. The chip otherwise remains in RX (if the channel becomes available, the radio does not enter TX or FSTXON state before a new strobe command is sent on the SPI interface). This feature is called TX-if-CCA. Four CCA requirements can be programmed:

- Always (CCA disabled, always goes to TX)
- If RSSI is below threshold
- Unless currently receiving a packet
- Both the above (RSSI below threshold and not currently receiving a packet)

3.13.6 Link Quality Indicator (LQI)

The Link Quality Indicator (LQI) is a metric of the current quality of the received signal. If PKTCTRL1.APPEND_STATUS is enabled, the value is automatically added to the last byte appended after the payload. The value can also be read from the LQI status register. The LQI gives an estimate of how easily a received signal can be demodulated by accumulating the magnitude of the error between ideal constellations and the received signal over the 64 symbols immediately following the sync word. LQI is best used as a relative measurement of the link quality (a high value indicates a better link than a low value does), because the value is dependent on the modulation format.

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3.14 Forward Error Correction With Interleaving

3.14.1 Forward Error Correction (FEC)

CC11x1-Q1 has built in support for Forward Error Correction (FEC). To enable this option, set MDMCFG1.FEC_EN to 1. FEC is supported only in fixed packet length mode (PKTCTRL0.LENGTH_CONFIG = 0). FEC is employed on the data field and CRC word to reduce the gross bit error rate when operating near the sensitivity limit. Redundancy is added to the transmitted data in such a way that the receiver can restore the original data in the presence of some bit errors.

The use of FEC allows correct reception at a lower SNR, thus extending communication range if the receiver bandwidth remains constant. Alternatively, for a given SNR, using FEC decreases the bit error rate (BER). As the packet error rate (PER) is related to BER by:

$$PER = 1 - (1 - BER)^{packet_length} \quad (6)$$

A lower BER can be used to allow longer packets, or a higher percentage of packets of a given length, to be transmitted successfully. Finally, in realistic ISM radio environments, transient and time-varying phenomena produce occasional errors even in otherwise good reception conditions. FEC masks such errors and, combined with interleaving of the coded data, even correct relatively long periods of faulty reception (burst errors).

The FEC scheme adopted for CC11x1-Q1 is convolutional coding, in which n bits are generated based on k input bits and the m most recent input bits, forming a code stream able to withstand a certain number of bit errors between each coding state (the m-bit window).

The convolutional coder is a rate 1/2 code with a constraint length of m = 4. The coder codes one input bit and produces two output bits; hence, the effective data rate is halved. I.e., to transmit at the same effective data rate when using FEC, it is necessary to use twice as high over-the-air data rate. This requires a higher receiver bandwidth, and thus reduce sensitivity. In other words the improved reception by using FEC and the degraded sensitivity from a higher receiver bandwidth are counteracting factors.

3.14.2 Interleaving

Data received through radio channels often experiences burst errors due to interference and time-varying signal strengths. To increase the robustness to errors spanning multiple bits, interleaving is used when FEC is enabled. After deinterleaving, a continuous span of errors in the received stream become single errors spread apart.

CC11x1-Q1 employs matrix interleaving, which is illustrated in Figure 3-14. The on-chip interleaving and deinterleaving buffers are 4×4 matrices. In the transmitter, the data bits from the rate one-half convolutional coder are written into the rows of the matrix, whereas the bit sequence to be transmitted is read from the columns of the matrix. Conversely, in the receiver, the received symbols are written into the columns of the matrix, whereas the data passed onto the convolutional decoder is read from the rows of the matrix.

When FEC and interleaving is used at least one extra byte is required for trellis termination. In addition, the amount of data transmitted over the air must be a multiple of the size of the interleaver buffer (two bytes). The packet control hardware therefore automatically inserts one or two extra bytes at the end of the packet, so that the total length of the data to be interleaved is an even number. Note that these extra bytes are invisible to the user, as they are removed before the received packet enters the RX FIFO.

When FEC and interleaving are used the minimum data payload is 2 bytes.

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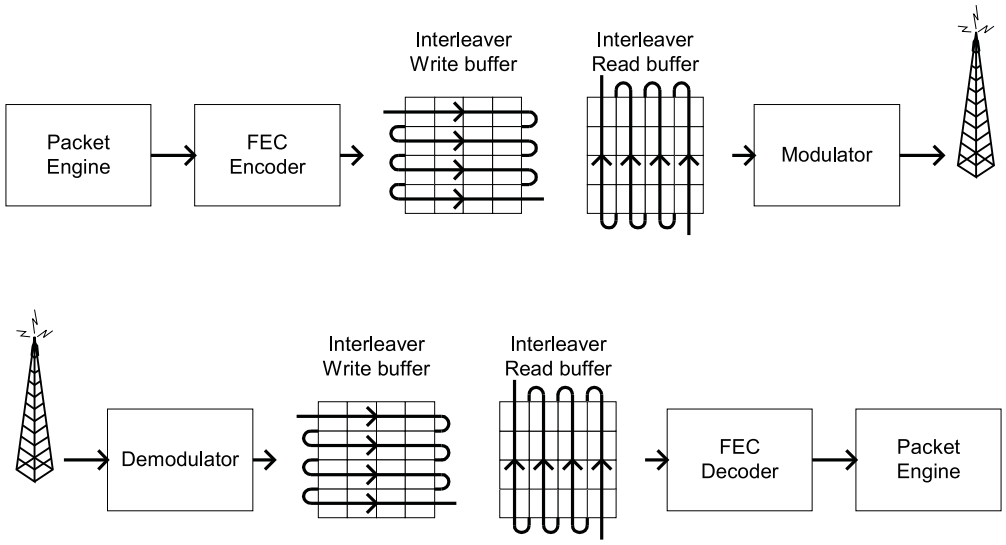

Figure 3-14. General Principle of Matrix Interleaving

3.15 Radio Control

CC11x1-Q1 has a built-in state machine that is used to switch between different operational states (modes). The change of state is done either by using command strobes or by internal events such as TX FIFO underflow.

A simplified state diagram, together with typical usage and current consumption, is shown in Figure 3-4. The complete radio control state diagram is shown in Figure 3-15. The numbers refer to the state number readable in the MARCSTATE status register. This register is primarily for test purposes.

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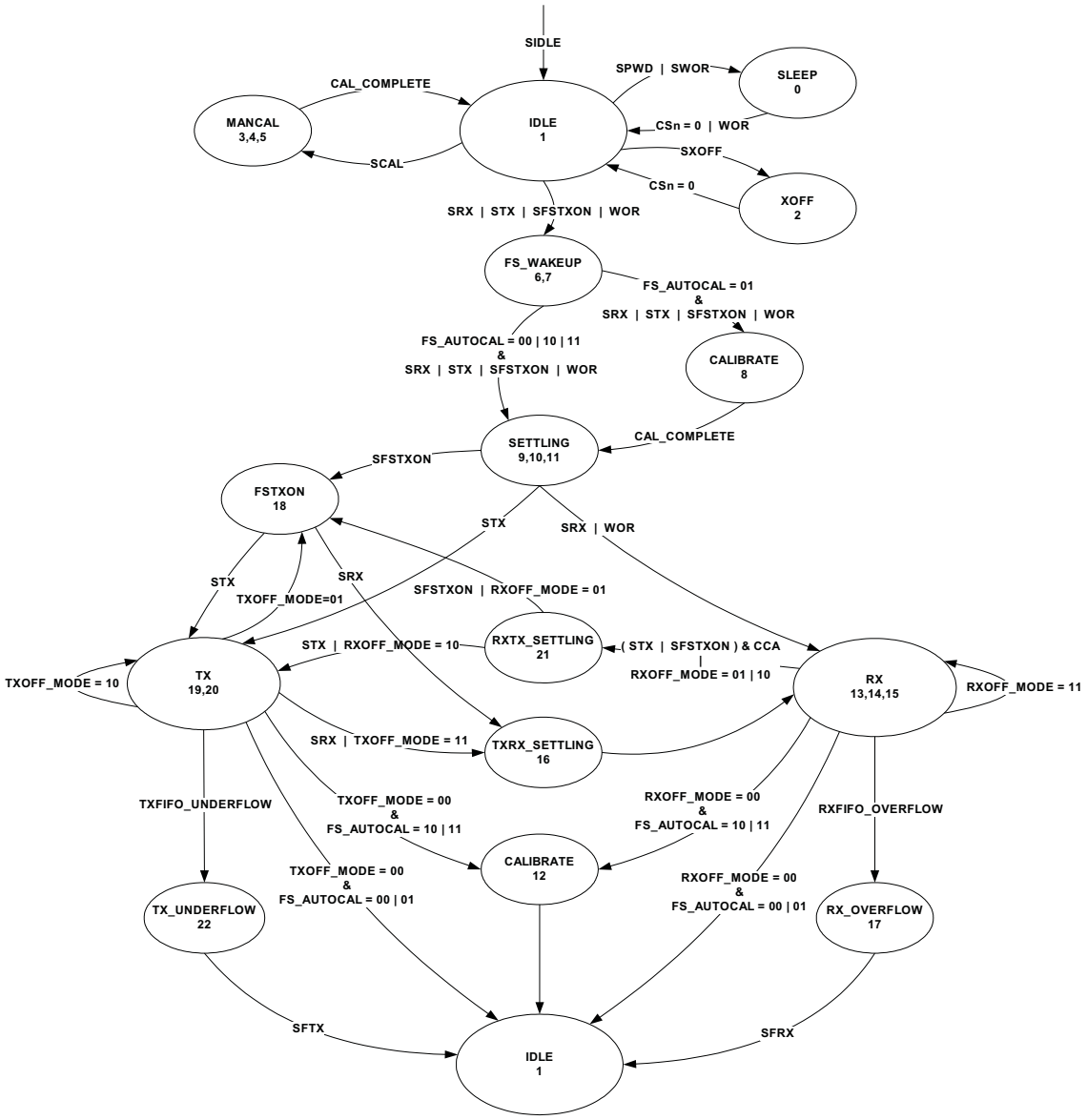

Figure 3-15. Complete Radio-Control State Diagram

3.15.1 Power-On Start-Up Sequence

When the power supply is turned on, the system must be reset. This is achieved by one of the two sequences described below, i.e. automatic power-on reset (POR) or manual reset.

After the automatic power-on reset or manual reset it is also recommended to change the signal that is output on the GDO0 pin. The default setting is to output a clock signal with a frequency of CLK_XOSC/192, but to optimize performance in TX and RX an alternative GDO setting should be selected from the settings found in Table 3-17.

3.15.1.1 Automatic POR

A power-on reset circuit is included in the CC11x1-Q1. The minimum requirements stated in Section 2.14 must be followed for the power-on reset to function properly. The internal power-up sequence is completed when CHIP_RDYn goes low. CHIP_RDYn is observed on the SO pin after $\overline{CS}$ is pulled low. See Section 3.6.1 for more details on CHIP_RDYn.

When the CC11x1-Q1 reset is completed, the chip is in the IDLE state and the crystal oscillator is running. If the chip has had sufficient time for the crystal oscillator to stabilize after the power-on-reset the SO pin goes low immediately after taking $\overline{CS}$ low. If $\overline{CS}$ is taken low before reset is completed the SO pin first goes high, indicating that the crystal oscillator is not stabilized, before going low as shown in Figure 3-16.

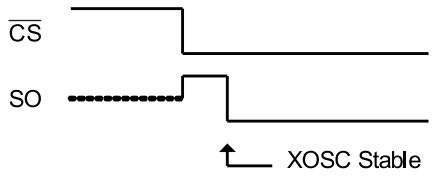

Figure 3-16. Power-On Reset

3.15.1.2 Manual Reset

The other global reset possibility on CC11x1-Q1 uses the SRES command strobe. By issuing this strobe, all internal registers and states are set to the default, IDLE state. The manual power-up sequence is as follows (see Figure 3-17):

- Set SCLK = 1 and SI = 0, to avoid potential problems with pin control mode (see Section 3.7.3).
- Strobe $\overline{CS}$ low then high.
- Hold $\overline{CS}$ high for at least 40 µs relative to pulling $\overline{CS}$ low
- Pull $\overline{CS}$ low and wait for SO to go low (CHIP_RDYn).
- Issue the SRES strobe on the SI line.
- When SO goes low again, reset is complete and the chip is in the IDLE state.

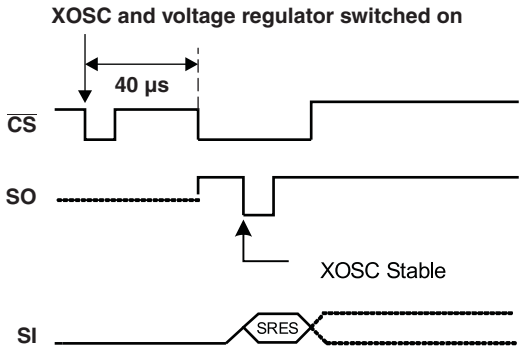

Figure 3-17. Power-On Reset With SRES

NOTE

This reset procedure is required only after the power supply is first turned on. If the user wants to reset the CC11x1-Q1 after this, it is only necessary to issue an SRES command strobe.

3.15.2 Crystal Control

The crystal oscillator (XOSC) is either automatically controlled or always on, if MCSM0.XOSC_FORCE_ON is set.

In the automatic mode, the XOSC is turned off if the SXOFF or SPWD command strobes are issued. The state machine then goes to XOFF or SLEEP, respectively. This can be done only from the IDLE state. The XOSC is turned off when $\overline{CS}$ is released (goes high). The XOSC is automatically turned on again when $\overline{CS}$ goes low. The state machine then goes to the IDLE state. The SO pin on the SPI interface must be pulled low before the SPI interface is ready to be used, as described in Section 2.9.

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If the XOSC is forced on, the crystal stays on, even in the SLEEP state.

Crystal oscillator start-up time depends on crystal ESR and load capacitances. The electrical specification for the crystal oscillator can be found in Section 2.9.

3.15.3 Voltage Regulator Control

The voltage regulator to the digital core is controlled by the radio controller. When the chip enters the SLEEP state, which is the state with the lowest current consumption, the voltage regulator is disabled. This occurs after $\overline{CS}$ is released when a SPWD command strobe has been sent on the SPI interface. The chip is now in the SLEEP state. Setting $\overline{CS}$ low again turns on the regulator and crystal oscillator and make the chip enter the IDLE state.

When wake on radio is enabled, the WOR module controls the voltage regulator as described in Section 3.15.5.

3.15.4 Active Modes

CC11x1-Q1 has two active modes: receive and transmit. These modes are activated directly by the MCU by using the SRX and STX command strobes, or automatically by Wake on Radio.

The frequency synthesizer must be calibrated regularly. CC11x1-Q1 has one manual calibration option (using the SCAL strobe), and three automatic calibration options, controlled by the MCSM0.FS_AUTOCAL setting:

- Calibrate when going from IDLE to either RX or TX (or FSTXON)
- Calibrate when going from either RX or TX to IDLE automatically
- Calibrate every fourth time when going from either RX or TX to IDLE automatically

If the radio goes from TX or RX to IDLE by issuing an SIDLE strobe, calibration is not performed. The calibration takes a constant number of XOSC cycles (see Table 3-14 for timing details).

When RX is activated, the chip remains in receive mode until a packet is successfully received or the RX termination timer expires (see Section 3.15.7).

NOTE

The probability that a false sync word is detected can be reduced by using PQT, CS, maximum sync word length, and sync word qualifier mode as described in Section 3.13.

After a packet is successfully received, the radio controller goes to the state indicated by the MCSM1.RXOFF_MODE setting. The possible destinations are:

- IDLE
- FSTXON: Frequency synthesizer on and ready at the TX frequency. Activate TX with STX .
- TX: Start sending preamble
- RX: Start search for a new packet

Similarly, when TX is active the chip remains in the TX state until the current packet has been successfully transmitted. Then the state changes as indicated by the MCSM1.TXOFF_MODE setting. The possible destinations are the same as for RX.

The MCU can manually change the state from RX to TX and vice versa by using the command strobes. If the radio controller is currently in transmit and the SRX strobe is used, the current transmission is ended and the transition to RX is done.

If the radio controller is in RX when the STX or SFSTXON command strobes are used, the TX-if-CCA function is used. If the channel is not clear, the chip remains in RX. The MCSM1.CCA_MODE setting controls the conditions for clear channel assessment (see Section 3.13.5 for details).

The SIDLE command strobe can always be used to force the radio controller to go to the IDLE state.

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3.15.5 Wake On Radio (WOR)

The optional Wake on Radio (WOR) functionality enables CC11x1-Q1 to periodically wake up from SLEEP and listen for incoming packets without MCU interaction.

When the WOR strobe command is sent on the SPI interface, the CC11x1-Q1 goes to the SLEEP state when $\overline{CS}$ is released. The RC oscillator must be enabled before the WOR strobe can be used, as it is the clock source for the WOR timer. The on-chip timer sets CC11x1-Q1 into IDLE state and then RX state. After a programmable time in RX, the chip goes back to the SLEEP state, unless a packet is received. See Figure 3-18 and Section 3.15.7 for details on how the timeout works.

Set the CC11x1-Q1 into the IDLE state to exit WOR mode.

CC11x1-Q1 can be set up to signal the MCU that a packet has been received by using the GDO pins. If a packet is received, the MCSM1.RXOFF_MODE determines the behavior at the end of the received packet. When the MCU has read the packet, it can put the chip back into SLEEP with the SWOR strobe from the IDLE state. The FIFO loses its contents in the SLEEP state.

The WOR timer has two events, Event 0 and Event 1. In the SLEEP state with WOR activated, reaching Event 0 turns on the digital regulator and starts the crystal oscillator. Event 1 follows Event 0 after a programmed timeout.

The time between two consecutive Event 0 is programmed with a mantissa value given by WOREVT1.EVENT0 and WOREVT0.EVENT0, and an exponent value set by WORCTRL.WOR_RES. The equation is:

$$t_{Event0} = \frac{750}{f_{XOSC}} \times EVENT0 \times 2^{5 \times WOR_RES} \quad (7)$$

The Event 1 timeout is programmed with WORCTRL.EVENT1. Figure 3-18 shows the timing relationship between Event 0 timeout and Event 1 timeout.

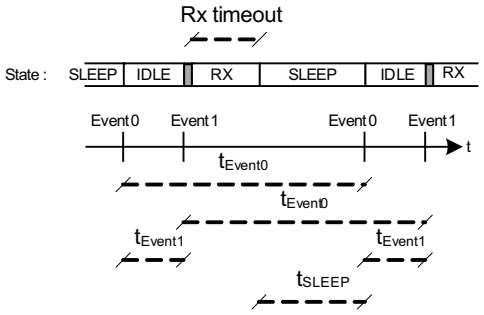

Figure 3-18. Event 0 and Event 1 Relationship

The time from the CC11x1-Q1 enters SLEEP state until the next Event0 is programmed to appear (tSLEEP in Figure 3-18) should be larger than 11.08 ms when using a 26-MHz crystal and 10.67 ms when a 27-MHz crystal is used. If t_{SLEEP} is less than 11.08 (10.67) ms, there is a chance that the consecutive Event 0 will occur (750 / f_{XOSC}) × 128 seconds too early. *CC1100/CC2500 – Wake-On-Radio* (SWRA126) explains in detail the theory of operation and the different registers involved when using WOR, as well as highlighting important aspects when using WOR mode.

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3.15.5.1 RC Oscillator and Timing

The frequency of the low-power RC oscillator used for the WOR functionality varies with temperature and supply voltage. To keep the frequency as accurate as possible, the RC oscillator is calibrated whenever possible, which is when the XOSC is running and the chip is not in the SLEEP state. When the power and XOSC is enabled, the clock used by the WOR timer is a divided XOSC clock. When the chip goes to the sleep state, the RC oscillator uses the last valid calibration result. The frequency of the RC oscillator is locked to the main crystal frequency divided by 750.

In applications where the radio wakes up very often, typically several times every second, it is possible to do the RC oscillator calibration once and then turn off calibration (WORCTRL.RC_CAL = 0) to reduce the current consumption. This requires that RC oscillator calibration values are read from registers RCCTRL0_STATUS and RCCTRL1_STATUS and written back to RCCTRL0 and RCCTRL1 respectively. If the RC oscillator calibration is turned off, it must be manually turned on again if temperature and supply voltage changes.

See *CC1100/CC2500 – Wake-On-Radio* (SWRA126) for further details.

3.15.6 Timing

The radio controller controls most of the timing in CC11x1-Q1, such as synthesizer calibration, PLL lock time, and RX/TX turnaround times. Timing from IDLE to RX and IDLE to TX is constant, dependent on the auto calibration setting. RX/TX and TX/RX turnaround times are constant. The calibration time is constant 18739 clock periods. Table 3-14 shows timing in crystal clock cycles for key state transitions.

Power on time and XOSC start-up times are variable, but within the limits stated in Section 2.9.

Note that in a frequency hopping spread spectrum or a multi-channel protocol the calibration time can be reduced from 721 µs to approximately 150 µs (see Section 3.27.2).

Table 3-14. State Transition Timing

DESCRIPTION	XOSC PERIODS	26-MHz CRYSTAL
IDLE to RX, no calibration	2298	88.4 µs
IDLE to RX, with calibration	~21037	809 µs
IDLE to TX/FSTXON, no calibration	2298	88.4 µs
IDLE to TX/FSTXON, with calibration	~21037	809 µs
TX to RX switch	560	21.5 µs
RX to TX switch	250	9.6 µs
RX or TX to IDLE, no calibration	2	0.1 µs
RX or TX to IDLE, with calibration	~18739	721 µs
Manual calibration	~18739	721 µs

3.15.7 RX Termination Timer

CC11x1-Q1 has optional functions for automatic termination of RX after a programmable time. The main use for this functionality is wake-on-radio (WOR), but it may be useful for other applications. The termination timer starts when in RX state. The timeout is programmable with the MCSM2.RX_TIME setting. When the timer expires, the radio controller checks the condition for staying in RX. If the condition is not met, RX terminates.

The programmable conditions are:

- MCSM2.RX_TIME_QUAL = 0
  Continue receive if sync word has been found
- MCSM2.RX_TIME_QUAL = 1
  Continue receive if sync word has been found or preamble quality is above threshold (PQT)

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If the system can expect the transmission to have started when enabling the receiver, the MCSM2.RX_TIME_RSSI function can be used. The radio controller then terminates RX if the first valid carrier sense sample indicates no carrier (RSSI below threshold) (see Section 3.13.4 for details on Carrier Sense).

For ASK/OOK modulation, lack of carrier sense is only considered valid after eight symbol periods. Thus, the MCSM2.RX_TIME_RSSI function can be used in ASK/OOK mode when the distance between "1" symbols is 8 or less.

If RX terminates due to no carrier sense when the MCSM2.RX_TIME_RSSI function is used, or if no sync word was found when using the MCSM2.RX_TIME timeout function, the chip goes back to IDLE if WOR is disabled and back to SLEEP if WOR is enabled. Otherwise, the MCSM1.RXOFF_MODE setting determines the state to go to when RX ends. This means that the chip does not automatically go back to SLEEP once a sync word has been received. It is therefore recommended to always wake up the microcontroller on sync word detection when using WOR mode. This can be done by selecting output signal 6 (see Table 3-17) on one of the programmable GDO output pins, and programming the microcontroller to wake up on an edge-triggered interrupt from this GDO pin.

3.16 Data FIFO

The CC11x1-Q1 contains two 64 byte FIFOs, one for received data and one for data to be transmitted. The SPI interface is used to read from the RX FIFO and write to the TX FIFO. Section 3.6 contains details on the SPI FIFO access. The FIFO controller detects overflow in the RX FIFO and underflow in the TX FIFO.

When writing to the TX FIFO, it is the responsibility of the MCU to avoid TX FIFO overflow. A TX FIFO overflow results in an error in the TX FIFO content.

Likewise, when reading the RX FIFO, the MCU must avoid reading the RX FIFO past its empty value, because an RX FIFO underflow results in an error in the data read out of the RX FIFO.

The chip status byte that is available on the SO pin while transferring the SPI header contains the fill grade of the RX FIFO if the access is a read operation and the fill grade of the TX FIFO if the access is a write operation. Section 3.6.1 contains more details on this.

The number of bytes in the RX FIFO and TX FIFO can be read from the status registers RXBYTES.NUM_RXBYTES and TXBYTES.NUM_TXBYTES respectively. If a received data byte is written to the RX FIFO at the exact same time as the last byte in the RX FIFO is read over the SPI interface, the RX FIFO pointer is not properly updated and the last read byte is duplicated. To avoid this problem one should never empty the RX FIFO before the last byte of the packet is received.

For packet lengths less than 64 bytes it is recommended to wait until the complete packet has been received before reading it out of the RX FIFO.

If the packet length is larger than 64 bytes the MCU must determine how many bytes can be read from the RX FIFO (RXBYTES.NUM_RXBYTES-1) and the following software routine can be used:

1. Read RXBYTES.NUM_RXBYTES repeatedly at a rate ensured to be at least twice that at which RF bytes are received until the same value is returned twice. Store value in n.
2. If n < # of bytes remaining in packet, read n – 1 bytes from the RX FIFO.
3. Repeat steps 1 and 2 until n = # of bytes remaining in packet.
4. Read the remaining bytes from the RX FIFO.

The 4-bit FIFOTHR.FIFO_THR setting is used to program threshold points in the FIFOs. Table 3-15 lists the 16 FIFO_THR settings and the corresponding thresholds for the RX and TX FIFOs. The threshold value is coded in opposite directions for the RX FIFO and TX FIFO. This gives equal margin to the overflow and underflow conditions when the threshold is reached.

A signal asserts when the number of bytes in the FIFO is equal to or higher than the programmed threshold. This signal can be viewed on the GDO pins (see Table 3-17).

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Figure 3-20 shows the number of bytes in both the RX FIFO and TX FIFO when the threshold signal toggles, in the case of FIFO_THR = 13. Figure 3-19 shows the signal as the respective FIFO is filled above the threshold, and then drained below.

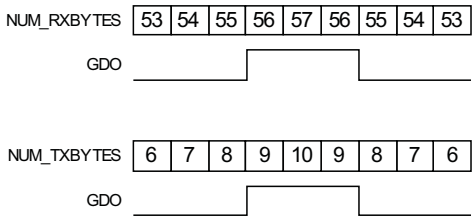

Figure 3-19. FIFO_THR = 13 vs Number of Bytes in FIFO (GDOx_CFG = 0x00 in RX and GDOx_CFG = 0x02 in TX)

Table 3-15. FIFO_THR Settings and the Corresponding FIFO Thresholds

FIFO_THR	BYTES IN TX FIFO	BYTES IN RX FIFO
0 (0000)	61	4
1 (0001)	57	8
2 (0010)	53	12
3 (0011)	49	16
4 (0100)	45	20
5 (0101)	41	24
6 (0110)	37	28
7 (0111)	33	32
8 (1000)	29	36
9 (1001)	25	40
10 (1010)	21	44
11 (1011)	17	48
12 (1100)	13	52
13 (1101)	9	56
14 (1110)	5	60
15 (1111)	1	64

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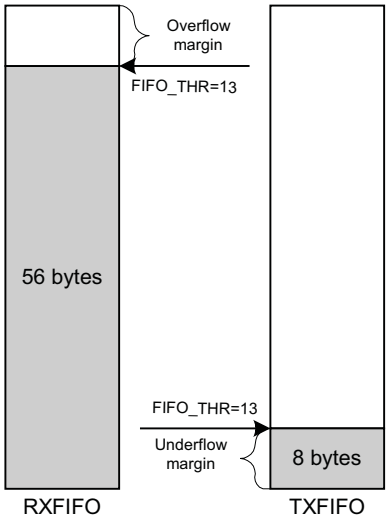

Figure 3-20. Example of FIFOs at Threshold

3.17 Frequency Programming

The frequency programming in CC11x1-Q1 is designed to minimize the programming needed in a channel-oriented system.

To set up a system with channel numbers, the desired channel spacing is programmed with the MDMCFG0.CHANSPC_M and MDMCFG1.CHANSPC_E registers. The channel spacing registers are mantissa and exponent respectively.

The base or start frequency is set by the 24-bit frequency word located in the FREQ2, FREQ1, and FREQ0 registers. This word is typically set to the center of the lowest channel frequency that is to be used.

The desired channel number is programmed with the 8-bit channel number register, CHANNR.CHAN, which is multiplied by the channel offset. The resultant carrier frequency is given by:

$$f_{carrier} = \frac{f_{XOSC}}{2^{16}} \times \left(FREQ + CHAN \times \left(\left(256 + CHANSPC_M\right) \times 2^{CHANSPC_E-2}\right)\right) \quad (8)$$

With a 26-MHz crystal the maximum channel spacing is 405 kHz. To get, for example, 1-MHz channel spacing one solution is to use 333-kHz channel spacing and select each third channel in CHANNR.CHAN.

The preferred IF frequency is programmed with the FSCTRL1.FREQ_IF register. The IF frequency is given by:

$$f_{IF} = \frac{f_{XOSC}}{2^{10}} \times FREQ_IF \quad (9)$$

NOTE

The SmartRF Studio software automatically calculates the optimum FSCTRL1.FREQ_IF register setting based on channel spacing and channel filter bandwidth.

If any frequency programming register is altered when the frequency synthesizer is running, the synthesizer may give an undesired response. Hence, the frequency programming should only be updated when the radio is in the IDLE state.

3.18 VCO

The VCO is completely integrated on-chip.

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3.18.1 VCO and PLL Self-Calibration

The VCO characteristics vary with temperature and supply voltage changes, as well as the desired operating frequency. To ensure reliable operation, CC11x1-Q1 includes frequency synthesizer self-calibration circuitry. This calibration should be done regularly, and must be performed after turning on power and before using a new frequency (or channel). The number of XOSC cycles for completing the PLL calibration is given in Table 3-14.

The calibration can be initiated automatically or manually. The synthesizer can be automatically calibrated each time the synthesizer is turned on, or each time the synthesizer is turned off automatically. This is configured with the MCSM0.FS_AUTOCAL register setting. In manual mode, the calibration is initiated when the SCAL command strobe is activated in the IDLE mode.

NOTE

The calibration values are maintained in SLEEP mode, so the calibration is still valid after waking up from SLEEP mode (unless supply voltage or temperature has changed significantly).

To check that the PLL is in lock, the user can program register IOCFGx.GDOx_CFG to 0x0A and use the lock detector output available on the GDOx pin as an interrupt for the MCU (x = 0,1, or 2). A positive transition on the GDOx pin means that the PLL is in lock. As an alternative the user can read register FSCAL1. The PLL is in lock if the register content is different from 0x3F (see also the errata notes). For more robust operation the source code could include a check so that the PLL is re-calibrated until PLL lock is achieved if the PLL does not lock the first time.

3.19 Voltage Regulators

CC11x1-Q1 contains several on-chip linear voltage regulators, which generate the supply voltage needed by low-voltage modules. These voltage regulators are invisible to the user, and can be viewed as integral parts of the various modules. The user must however make sure that the absolute maximum ratings and required pin voltages in Table 3-1 and Section 2.1 are not exceeded. The voltage regulator for the digital core requires one external decoupling capacitor.

Setting the $\overline{CS}$ pin low turns on the voltage regulator to the digital core and starts the crystal oscillator. The SO pin on the SPI interface must go low before the first positive edge of SCLK (setup time is given in Section 2.15).

If the chip is programmed to enter power-down mode, (SPWD strobe issued), the power is turned off after $\overline{CS}$ goes high. The power and crystal oscillator are turned on again when $\overline{CS}$ goes low.

The voltage regulator output should be used only for driving the CC11x1-Q1.

3.20 Output Power Programming

The RF output power level from the device has two levels of programmability, as illustrated in Figure 3-21. Firstly, the special PATABLE register can hold up to eight user selected output power settings. Secondly, the 3-bit FREND0.PA_POWER value selects the PATABLE entry to use. This two-level functionality provides flexible PA power ramp up and ramp down at the start and end of transmission, as well as ASK modulation shaping. All the PA power settings in the PATABLE from index 0 up to the FREND0.PA_POWER value are used.

The power ramping at the start and at the end of a packet can be turned off by setting FREND0.PA_POWER to zero and then program the desired output power to index 0 in the PATABLE.

If OOK modulation is used, the logic 0 and logic 1 power levels shall be programmed to index 0 and 1 respectively.

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See Design Note DN013 *Programming Output Power on CC1101* (SWRA151) for recommended PATABLE settings for various output levels and frequency bands. Using PA settings from 0x61 to 0x6F is not recommended. See Section 3.6.6 for PATABLE programming details.

See Design Note DN013 *Programming Output Power on CC1101* (SWRA151) for output power and current consumption for default PATABLE setting (0xC6). PATABLE must be programmed in burst mode to write to entries other than PATABLE[0].

NOTE

All content of the PATABLE, except for the first byte (index 0), is lost when entering the SLEEP state.

3.21 Shaping and PA Ramping

With ASK modulation, up to eight power settings are used for shaping. The modulator contains a counter that counts up when transmitting a one and down when transmitting a zero. The counter counts at a rate equal to 8 times the symbol rate. The counter saturates at FREND0.PA_POWER and 0 respectively. This counter value is used as an index for a lookup in the power table. Thus, to utilize the whole table, FREND0.PA_POWER should be 7 when ASK is active. The shaping of the ASK signal is dependent on the configuration of the PATABLE.

Figure 3-22 shows some examples of ASK shaping.

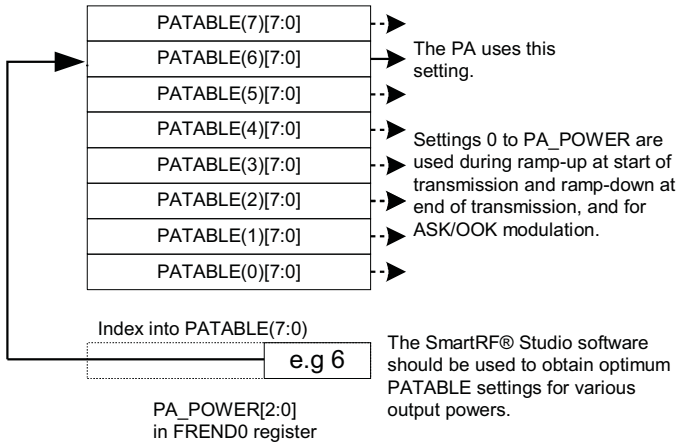

Figure 3-21. PA_POWER and PATABLE

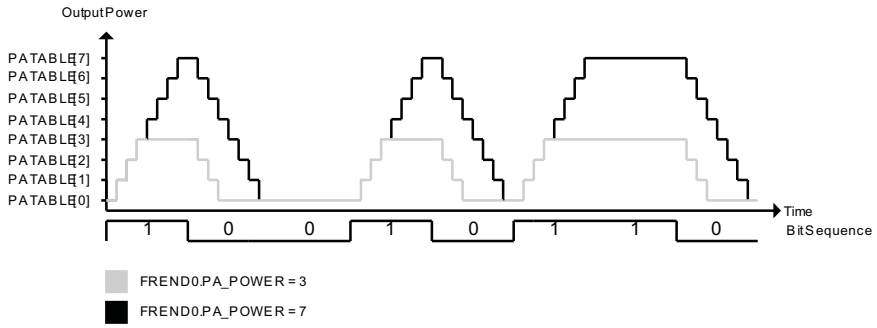

Figure 3-22. Shaping of ASK Signal

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3.22 Crystal Oscillator

A crystal in the frequency range 26-27 MHz must be connected between the XOSC_Q1 and XOSC_Q2 pins. The oscillator is designed for parallel mode operation of the crystal. In addition, loading capacitors (C81 and C101) for the crystal are required. The loading capacitor values depend on the total load capacitance, CL, specified for the crystal. The total load capacitance seen between the crystal terminals should equal CL for the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C_{81}} + \frac{1}{C_{101}}} + C_{parasitic} \quad (10)$$

The parasitic capacitance is constituted by pin input capacitance and PCB stray capacitance. Total parasitic capacitance is typically 2.5 pF.

The crystal oscillator circuit is shown in Figure 3-23. Typical component values for different values of CL are given in Table 3-16.

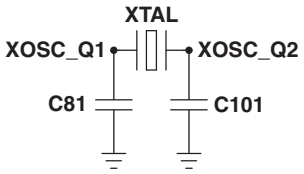

Figure 3-23. Crystal Oscillator Circuit

Table 3-16. Crystal Oscillator Component Values

Component	C_L = 10 pF	C_L = 13 pF	C_L = 16 pF
C81	15 pF	22 pF	27 pF
C101	15 pF	22 pF	27 pF

The crystal oscillator is amplitude regulated. This means that a high current is used to start up the oscillations. When the amplitude builds up, the current is reduced to what is necessary to maintain approximately 0.4-V_{pp} signal swing. This ensures a fast start-up, and keeps the drive level to a minimum. The ESR of the crystal should be within the specification to ensure a reliable start-up (see Section 2.9).

The initial tolerance, temperature drift, aging and load pulling should be carefully specified to meet the required frequency accuracy in a certain application.

3.22.1 Reference Signal

The chip can alternatively be operated with a reference signal from 26 to 27 MHz instead of a crystal. This input clock can either be a full-swing digital signal (0 V to V_{DD}) or a sine wave of maximum 1 V peak-peak amplitude. The reference signal must be connected to the XOSC_Q1 input. The sine wave must be connected to XOSC_Q1 using a serial capacitor. When using a full-swing digital signal this capacitor can be omitted. The XOSC_Q2 line must be left unconnected. C81 and C101 can be omitted when using a reference signal.

3.23 External RF Match

The balanced RF input and output of CC11x1-Q1 share two common pins and are designed for a simple, low-cost matching and balun network on the printed circuit board. The receive- and transmit switching at the CC11x1-Q1 front-end is controlled by a dedicated on-chip function, eliminating the need for an external RX/TX-switch.

A few passive external components combined with the internal RX/TX switch/termination circuitry ensures match in both RX and TX mode.

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Although CC11x1-Q1 has a balanced RF input/output, the chip can be connected to a single-ended antenna with few external low cost capacitors and inductors.

The passive matching/filtering network connected to CC11x1-Q1 should have the following differential impedance as seen from the RF-port (RF_P and RF_N) toward the antenna:

$Z_{out\ 315\ MHz} = 122 + j31\ \Omega$

$Z_{out\ 433\ MHz} = 116 + j41\ \Omega$

$Z_{out\ 868/915\ MHz} = 86.5 + j43\ \Omega$

To ensure optimal matching of the CC11x1-Q1 differential output it is recommended to follow the reference design as closely as possible. Gerber files for the reference designs are available for download from the TI web site.

3.24 PCB Layout Recommendations

The top layer should be used for signal routing, and the open areas should be filled with metallization connected to ground using several vias.

The area under the chip is used for grounding and shall be connected to the bottom ground plane with several vias. In the reference designs, five vias are placed inside the exposed die attached pad. These vias should be tented (covered with solder mask) on the component side of the PCB to avoid migration of solder through the vias during the solder reflow process.

The solder paste coverage should not be 100%. If it is, out gassing may occur during the reflow process, which may cause defects (splattering, solder balling). Using "tented" vias reduces the solder paste coverage below 100%.

Each decoupling capacitor should be placed as close as possible to the supply pin it is supposed to decouple. Each decoupling capacitor should be connected to the power line (or power plane) by separate vias. The best routing is from the power line (or power plane) to the decoupling capacitor and then to the CC11x1-Q1 supply pin. Supply power filtering is very important.

Each decoupling capacitor ground pad should be connected to the ground plane using a separate via. Direct connections between neighboring power pins increase noise coupling and should be avoided unless absolutely necessary.

The external components ideally should be as small as possible (0402 is recommended) and surface mount devices are highly recommended. Please note that components smaller than those specified may have differing characteristics.

Precaution should be used when placing the microcontroller to avoid noise interfering with the RF circuitry.

A development kit with a fully assembled evaluation module is available. It is strongly advised that this reference layout is followed closely to get the best performance. The schematic, BOM, and layout Gerber files are all available from the TI web site.

3.25 General Purpose / Test Output Control Pins

The three digital output pins GDO0, GDO1, and GDO2 are general control pins configured with IOCFG0.GDO0_CFG, IOCFG1.GDO1_CFG, and IOCFG2.GDO3_CFG respectively. Table 3-17 shows the different signals that can be monitored on the GDO pins. These signals can be used as inputs to the MCU. GDO1 is the same pin as the SO pin on the SPI interface, thus the output programmed on this pin is valid only when $\overline{CS}$ is high. The default value for GDO1 is 3-stated, which is useful when the SPI interface is shared with other devices.

The default value for GDO0 is a 135-141 kHz clock output (XOSC frequency divided by 192). Because the XOSC is turned on at power-on-reset, this can be used to clock the MCU in systems with only one crystal. When the MCU is up and running, it can change the clock frequency by writing to IOCFG0.GDO0_CFG.

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An on-chip analog temperature sensor is enabled by writing the value 128 (0x80) to the IOCFG0 register. The voltage on the GDO0 pin is then proportional to temperature. See Section 2.12 for temperature sensor specifications.

If the IOCFGx.GDOx_CFG setting is less than 0x20 and IOCFGx_GDOx_INV is 0 (1), the GDO0 and GDO2 pins are hardwired to 0 (1) and the GDO1 pin is hardwired to 1 (0) in the SLEEP state. These signals are hardwired until the CHIP_RDYn signal goes low.

If the IOCFGx.GDOx_CFG setting is 0x20 or higher, the GDO pins also work as programmed in SLEEP state. As an example, GDO1 is high impedance in all states if IOCFG1.GDO1_CFG = 0x2E.

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Table 3-17. GDOx Signal Selection (x = 0, 1, or 2)

GDOx_CFG[5:0]	DESCRIPTION
0 (0x00)	Associated to the RX FIFO: Asserts when RX FIFO is filled at or above the RX FIFO threshold. De-asserts when RX FIFO is drained below the same threshold.
1 (0x01)	Associated to the RX FIFO: Asserts when RX FIFO is filled at or above the RX FIFO threshold or the end of packet is reached. De-asserts when the RX FIFO is empty.
2 (0x02)	Associated to the TX FIFO: Asserts when the TX FIFO is filled at or above the TX FIFO threshold. De-asserts when the TX FIFO is below the same threshold.
3 (0x03)	Associated to the TX FIFO: Asserts when TX FIFO is full. De-asserts when the TX FIFO is drained below the TX FIFO threshold.
4 (0x04)	Asserts when the RX FIFO has overflowed. De-asserts when the FIFO has been flushed.
5 (0x05)	Asserts when the TX FIFO has underflowed. De-asserts when the FIFO is flushed.
6 (0x06)	Asserts when sync word has been sent / received, and de-asserts at the end of the packet. In RX, the pin de-asserts when the optional address check fails or the RX FIFO overflows. In TX, the pin de-asserts if the TX FIFO underflows.
7 (0x07)	Asserts when a packet has been received with CRC OK. De-asserts when the first byte is read from the RX FIFO.
8 (0x08)	Preamble Quality Reached. Asserts when the PQI is above the programmed PQT value.
9 (0x09)	Clear channel assessment. High when RSSI level is below threshold (dependent on the current CCA_MODE setting)
10 (0x0A)	Lock detector output. The PLL is in lock if the lock detector output has a positive transition or is constantly logic high. To check for PLL lock the lock detector output should be used as an interrupt for the MCU.
11 (0x0B)	Serial Clock. Synchronous to the data in synchronous serial mode. In RX mode, data is set up on the falling edge by CC11x1-Q1 when GDOx_INV = 0. In TX mode, data is sampled by CC11x1-Q1 on the rising edge of the serial clock when GDOx_INV = 0.
12 (0x0C)	Serial synchronous data output. Used for synchronous serial mode.
13 (0x0D)	Serial data output. Used for asynchronous serial mode.
14 (0x0E)	Carrier sense. High if RSSI level is above threshold.
15 (0x0F)	CRC_OK. The last CRC comparison matched. Cleared when entering/restarting RX mode.
16 (0x10) to 21 (0x15)	Reserved – used for test
22 (0x16)	RX_HARD_DATA[1]. Can be used together with RX_SYMBOL_TICK for alternative serial RX output.
23 (0x17)	RX_HARD_DATA[0]. Can be used together with RX_SYMBOL_TICK for alternative serial RX output.
24 (0x18) to 26 (0x1A)	Reserved – used for test
27 (0x1B)	PA_PD. Note: PA_PD has the same signal level in SLEEP and TX states. To control an external PA or RX/TX switch in applications where the SLEEP state is used, it is recommended to use GDOx_CFGx = 0x2F instead.
28 (0x1C)	LNA_PD. Note: LNA_PD has the same signal level in SLEEP and RX states. To control an external LNA or RX/TX switch in applications where the SLEEP state is used, it is recommended to use GDOx_CFGx = 0x2F instead.
29 (0x1D)	RX_SYMBOL_TICK. Can be used together with RX_HARD_DATA for alternative serial RX output.
30 (0x1E) to 35 (0x23)	Reserved – used for test
36 (0x24)	WOR_EVNT0
37 (0x25)	WOR_EVNT1
38 (0x26)	Reserved – used for test
39 (0x27)	CLK_32k
40 (0x28)	Reserved – used for test
41 (0x29)	CHIP_RDYn
42 (0x2A)	Reserved – used for test
43 (0x2B)	XOSC_STABLE
44 (0x2C)	Reserved – used for test
45 (0x2D)	GDO0_Z_EN_N. When this output is 0, GDO0 is configured as input (for serial TX data).
46 (0x2E)	High impedance (3-state)
47 (0x2F)	HW to 0 (HW1 achieved by setting GDOx_INV = 1). Can be used to control an external LNA/PA or RX/TX switch.

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Table 3-17. GDOx Signal Selection (x = 0, 1, or 2) (continued)

GDOx_CFG[5:0]	DESCRIPTION	
48 (0x30)	CLK_XOSC/1	Note: There are 3 GDO pins, but only one CLK_XOSC/n can be selected as an output at any time. If CLK_XOSC/n is to be monitored on one of the GDO pins, the other two GDO pins must be configured to values less than 0x30. The GDO0 default value is CLK_XOSC/192. To optimize RF performance, these signal should not be used while the radio is in RX or TX mode.
49 (0x31)	CLK_XOSC/1.5	
50 (0x32)	CLK_XOSC/2	
51 (0x33)	CLK_XOSC/3	
52 (0x34)	CLK_XOSC/4	
53 (0x35)	CLK_XOSC/6	
54 (0x36)	CLK_XOSC/8	
55 (0x37)	CLK_XOSC/12	
56 (0x38)	CLK_XOSC/16	
57 (0x39)	CLK_XOSC/24	
58 (0x3A)	CLK_XOSC/32	
59 (0x3B)	CLK_XOSC/48	
60 (0x3C)	CLK_XOSC/64	
61 (0x3D)	CLK_XOSC/96	
62 (0x3E)	CLK_XOSC/128	
63 (0x3F)	CLK_XOSC/192	

3.26 Asynchronous and Synchronous Serial Operation

Several features and modes of operation have been included in the CC11x1-Q1 to provide backward compatibility with previous Chipcon products and other existing RF communication systems. For new systems, it is recommended to use the built-in packet handling features, as they can give more robust communication, significantly offload the microcontroller, and simplify software development.

3.26.1 Asynchronous Operation

For backward compatibility with systems already using the asynchronous data transfer from other Chipcon products, asynchronous transfer is also included in CC11x1-Q1. When asynchronous transfer is enabled, several of the support mechanisms for the MCU that are included in CC11x1-Q1 are disabled, such as packet handling hardware, buffering in the FIFO, and so on. The asynchronous transfer mode does not allow the use of the data whitener, interleaver, and FEC, and it is not possible to use Manchester encoding.

NOTE

MSK is not supported for asynchronous transfer.

Setting PKTCTRL0.PKT_FORMAT to 3 enables asynchronous serial mode.

In TX, the GDO0 pin is used for data input (TX data). Data output can be on GDO0, GDO1, or GDO2. This is set by the IOCFG0.GDO0_CFG, IOCFG1.GDO1_CFG and IOCFG2.GDO2_CFG fields.

The CC11x1-Q1 modulator samples the level of the asynchronous input 8 times faster than the programmed data rate. The timing requirement for the asynchronous stream is that the error in the bit period must be less than one eighth of the programmed data rate.

3.26.2 Synchronous Serial Operation

Setting PKTCTRL0.PKT_FORMAT to 1 enables synchronous serial mode. In the synchronous serial

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mode, data is transferred on a two wire serial interface. The CC11x1-Q1 provides a clock that is used to set up new data on the data input line or sample data on the data output line. Data input (TX data) is the GDO0 pin. This pin is automatically configured as an input when TX is active. The data output pin can be any of the GDO pins (this is set by the IOCFG0.GDO0_CFG, IOCFG1.GDO1_CFG, and IOCFG2.GDO2_CFG fields).

Preamble and sync word insertion/detection may or may not be active, dependent on the sync mode set by the MDMCFG2.SYNC_MODE. If preamble and sync word is disabled, all other packet handler features and FEC should also be disabled. The MCU must then handle preamble and sync word insertion and detection in software. If preamble and sync word insertion/detection is left on, all packet handling features and FEC can be used. One exception is that the address filtering feature is unavailable in synchronous serial mode.

When using the packet handling features in synchronous serial mode, the CC11x1-Q1 inserts and detects the preamble and sync word and the MCU only provides/gets the data payload. This is equivalent to the recommended FIFO operation mode.

3.27 System Considerations and Guidelines

3.27.1 SRD Regulations

International regulations and national laws regulate the use of radio receivers and transmitters. Short range devices (SRDs) for license-free operation below 1 GHz are usually operated in the 433 MHz, 868 MHz, or 915 MHz frequency bands. The CC11x1-Q1 is specifically designed for such use with its 310 MHz to 348 MHz, 420 MHz to 450 MHz, and 779 MHz to 928 MHz operating ranges. The most important regulations when using the CC11x1-Q1 in the 433 MHz, 868 MHz, or 915 MHz frequency bands are EN 300 220 (Europe) and FCC CFR47 Part 15 (USA). A summary of the most important aspects of these regulations can be found in *SRD Regulations for Licence Free Transceiver Operation* (SWRA090).

NOTE

Compliance with regulations is dependent on complete system performance. It is the customer's responsibility to ensure that the system complies with regulations.

3.27.2 Frequency Hopping and Multi-Channel Systems

The 433-MHz, 868-MHz, and 915-MHz bands are shared by many systems both in industrial, office, and home environments. It is therefore recommended to use a frequency-hopping spread-spectrum (FHSS) or multi-channel protocol, because the frequency diversity makes the system more robust with respect to interference from other systems operating in the same frequency band. FHSS also combats multipath fading.

CC11x1-Q1 is highly suited for FHSS or multi-channel systems due to its agile frequency synthesizer and effective communication interface. Using the packet handling support and data buffering is also beneficial in such systems, as these features significantly offload the host controller.

Charge pump current, VCO current, and VCO capacitance array calibration data is required for each frequency when implementing frequency hopping for CC11x1-Q1. There are three ways of obtaining the calibration data from the chip:

1. Frequency hopping with calibration for each hop. The PLL calibration time is approximately 720 µs. The blanking interval between each frequency hop is then approximately 810 µs.
2. Fast frequency hopping without calibration for each hop can be done by calibrating each frequency at startup and saving the resulting FSCAL3, FSCAL2, and FSCAL1 register values in MCU memory. Between each frequency hop, the calibration process can then be replaced by writing the FSCAL3, FSCAL2, and FSCAL1 register values corresponding to the next RF frequency. The PLL turn-on time is approximately 90 µs. The blanking interval between each frequency hop is then approximately 90 µs. The VCO current calibration result available in FSCAL2 is not dependent on the RF frequency.

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Neither is the charge pump current calibration result available in FSCAL3. The same value can, therefore, be used for all frequencies.

3. Run calibration on a single frequency at startup. Next, write 0 to FSCAL3[5:4] to disable the charge-pump calibration. After writing to FSCAL3[5:4], strobe SRX (or STX) with MCSM0.FS_AUTOCAL = 1 for each new frequency hop. That is, VCO current and VCO capacitance calibration are done but not charge-pump current calibration. When charge pump current calibration is disabled, the calibration time is reduced from approximately 720 µs to approximately 150 µs. The blanking interval between each frequency hop is then approximately 240 µs.

There is a trade off between blanking time and memory space needed for storing calibration data in non-volatile memory. Solution 2 above gives the shortest blanking interval, but requires more memory space to store calibration values. Solution 3 gives approximately 570 µs smaller blanking interval than solution 1.

NOTE

The recommended settings for TEST0.VCO_SEL_CAL_EN change with frequency. Therefore, SmartRF Studio should be used to determine the correct settings for a specific frequency before doing a calibration, regardless of which calibration method is used.

It must be noted that the TESTn registers (n = 0, 1, or 2) content is not retained in SLEEP state, and thus it is necessary to rewrite these registers when returning from the SLEEP state.

3.27.3 Wideband Modulation Not Using Spread Spectrum

Digital modulation systems under FFC Part 15.247 include 2-FSK and GFSK modulation. A maximum peak output power of 1 W (+30 dBm) is allowed if the 6-dB bandwidth of the modulated signal exceeds 500 kHz. In addition, the peak power spectral density conducted to the antenna shall not be greater than 8 dBm in any 3-kHz band.

Operating at high data rates and frequency separation, the CC11x1-Q1 is suited for systems targeting compliance with digital modulation system as defined by FFC part 15.247. An external power amplifier is needed to increase the output above 10 dBm.

3.27.4 Data Burst Transmissions

The high maximum data rate of CC11x1-Q1 allows burst transmissions. A low average data rate link (e.g., 10 kBaud), can be realized using a higher over-the-air data rate. Buffering the data and transmitting in bursts at high data rate (e.g., 500 kBaud) reduces the time in active mode and, therefore, reduces the average current consumption significantly. Reducing the time in active mode reduces the likelihood of collisions with other systems in the same frequency range.

3.27.5 Continuous Transmissions

In data streaming applications, the CC11x1-Q1 allows continuous transmissions at 500-kBaud effective data rate. As the modulation is done with a closed-loop PLL, there is no limitation on the length of a transmission (open-loop modulation used in some transceivers often prevents this continuous data streaming and reduces the effective data rate).

3.27.6 Crystal Drift Compensation

The CC11x1-Q1 has a very fine frequency resolution (see Section 2.11). This feature can be used to compensate for frequency offset and drift.

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The frequency offset between an external transmitter and the receiver is measured in the CC11x1-Q1 and can be read back from the FREQEST status register as described in Section 3.10.1. The measured frequency offset can be used to calibrate the frequency using the external transmitter as the reference. That is, the received signal of the device matches the receiver's channel filter better. In the same way, the center frequency of the transmitted signal matches the external transmitter's signal.

3.27.7 Spectrum Efficient Modulation

CC11x1-Q1 also allows the use of Gaussian shaped 2-FSK (GFSK). This spectrum-shaping feature improves adjacent channel power (ACP) and occupied bandwidth. In true 2-FSK systems with abrupt frequency shifting, the spectrum is inherently broad. By making the frequency shift softer, the spectrum can be made significantly narrower. Thus, higher data rates can be transmitted in the same bandwidth using GFSK.

3.27.8 Low Cost Systems

As the CC11x1-Q1 provides 250-kBaud multi-channel performance without any external filters, a very low-cost system can be made.

A differential antenna eliminates the need for a balun, and the dc biasing can be achieved in the antenna topology, see Figure 3-2 and Figure 3-3.

A HC-49 type SMD crystal is used in the reference designs. Note that the crystal package strongly influences the price. In a size-constrained PCB design a smaller but more expensive crystal can be used.

3.27.9 Battery Operated Systems

In low-power applications, the SLEEP state with the crystal oscillator core switched off should be used when the CC11x1-Q1 is not active. The crystal oscillator core can be left running in the SLEEP state if start-up time is critical.

The WOR functionality should be used in low power applications.

3.27.10 Increasing Output Power

In some applications, it may be necessary to extend the link range. Adding an external power amplifier is the most effective way to do this.

The power amplifier should be inserted between the antenna and the balun, and two T/R switches are needed to disconnect the PA in RX mode (see Figure 3-24).

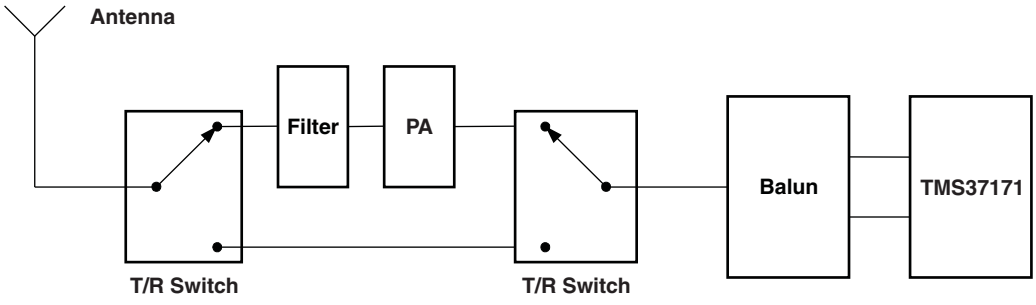

Figure 3-24. Block Diagram of CC11x1-Q1 With External Power Amplifier

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4 Configuration Registers

4.1 Overview

The configuration of CC11x1-Q1 is done by programming 8-bit registers. The optimum configuration data based on selected system parameters are most easily found by using the SmartRF Studio software. Complete descriptions of the registers are given in the following tables. After chip reset, all the registers have default values as shown in the tables. The optimum register setting might differ from the default value. After a reset, all registers that should be different from the default value, therefore, need to be programmed through the SPI interface.

There are 13 command strobe registers, listed in Table 4-1. Accessing these registers initiates the change of an internal state or mode. There are 47 normal 8-bit configuration registers, listed in Table 4-2. Many of these registers are for test purposes only and need not be written for normal operation of CC11x1-Q1.

There are also 12 status registers, listed in Table 4-3. These registers, which are read-only, contain information about the status of CC11x1-Q1.

The two FIFOs are accessed through one 8-bit register. Write operations write to the TX FIFO, while read operations read from the RX FIFO.

During the header byte transfer and while writing data to a register or the TX FIFO, a status byte is returned on the SO line. This status byte is described in Table 3-3.

Table 4-7 summarizes the SPI address space. The address to use is given by adding the base address to the left and the burst and read/write bits on the top. Note that the burst bit has different meaning for base addresses above and below 0x2F.

Table 4-1. Command Strobes

ADDRESS	STROBE NAME	DESCRIPTION
0x30	SRES	Reset chip.
0x31	SFSTXON	Enable and calibrate frequency synthesizer (if MCSM0.FS_AUTOCAL = 1). If in RX (with CCA), go to a wait state where only the synthesizer is running (for quick RX/TX turnaround).
0x32	SXOFF	Turn off crystal oscillator.
0x33	SCAL	Calibrate frequency synthesizer and turn it off. SCAL can be strobed from IDLE mode without setting manual calibration mode (MCSM0.FS_AUTOCAL = 0).
0x34	SRX	Enable RX. Perform calibration first if coming from IDLE and MCSM0.FS_AUTOCAL = 1.
0x35	STX	In IDLE state, enable TX. Perform calibration first if MCSM0.FS_AUTOCAL = 1. If in RX state and CCA is enabled, only go to TX if channel is clear.
0x36	SIDLE	Exit RX/TX, turn off frequency synthesizer, and exit WOR mode, if applicable.
0x38	SWOR	Start automatic RX polling sequence (WOR) as described in Section 3.15.5 if WORCTRL.RC_PD = 0.
0x39	SPWD	Enter power-down mode when $\overline{CS}$ goes high.
0x3A	SFRX	Flush the RX FIFO buffer. Only issue SFRX in IDLE or RXFIFO_OVERFLOW states.
0x3B	SFTX	Flush the TX FIFO buffer. Only issue SFTX in IDLE or TXFIFO_UNDERFLOW states.
0x3C	SWORRST	Reset real-time clock to Event1 value.
0x3D	SNOP	No operation. May be used to access the chip status byte.

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Table 4-2. Configuration Registers

ADDRESS	REGISTER	DESCRIPTION	PRESERVED IN SLEEP STATE?
0x00	IOCFG2	GDO2 output pin configuration	Yes
0x01	IOCFG1	GDO1 output pin configuration	Yes
0x02	IOCFG0	GDO0 output pin configuration	Yes
0x03	FIFOTHR	RX FIFO and TX FIFO thresholds	Yes
0x04	SYNC1	Sync word, high byte	Yes
0x05	SYNC0	Sync word, low byte	Yes
0x06	PKTLEN	Packet length	Yes
0x07	PKTCTRL1	Packet automation control	Yes
0x08	PKTCTRL0	Packet automation control	Yes
0x09	ADDR	Device address	Yes
0x0A	CHANNR	Channel number	Yes
0x0B	FSCTRL1	Frequency synthesizer control	Yes
0x0C	FSCTRL0	Frequency synthesizer control	Yes
0x0D	FREQ2	Frequency control word, high byte	Yes
0x0E	FREQ1	Frequency control word, middle byte	Yes
0x0F	FREQ0	Frequency control word, low byte	Yes
0x10	MDMCFG4	Modem configuration	Yes
0x11	MDMCFG3	Modem configuration	Yes
0x12	MDMCFG2	Modem configuration	Yes
0x13	MDMCFG1	Modem configuration	Yes
0x14	MDMCFG0	Modem configuration	Yes
0x15	DEVIATN	Modem deviation setting	Yes
0x16	MCSM2	Main radio control state machine configuration	Yes
0x17	MCSM1	Main radio control state machine configuration	Yes
0x18	MCSM0	Main radio control state machine configuration	Yes
0x19	FOCCFG	Frequency offset compensation configuration	Yes
0x1A	BSCFG	Bit synchronization configuration	Yes
0x1B	AGCTRL2	AGC control	Yes
0x1C	AGCTRL1	AGC control	Yes
0x1D	AGCTRL0	AGC control	Yes
0x1E	WOREVT1	High byte Event 0 timeout	Yes
0x1F	WOREVT0	Low byte Event 0 timeout	Yes
0x20	WORCTRL	Wake-on-radio control	Yes
0x21	FREND1	Front-end RX configuration	Yes
0x22	FREND0	Front-end TX configuration	Yes
0x23	FSCAL3	Frequency synthesizer calibration	Yes
0x24	FSCAL2	Frequency synthesizer calibration	Yes
0x25	FSCAL1	Frequency synthesizer calibration	Yes
0x26	FSCAL0	Frequency synthesizer calibration	Yes
0x27	RCCTRL1	RC oscillator configuration	Yes
0x28	RCCTRL0	RC oscillator configuration	Yes
0x29	FSTEST	Frequency synthesizer calibration control	No
0x2A	PTEST	Production test	No
0x2B	AGCTEST	AGC test	No
0x2C	TEST2	Various test settings	No
0x2D	TEST1	Various test settings	No
0x2E	TEST0	Various test settings	No

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Table 4-3. Status Registers

ADDRESS	REGISTER	DESCRIPTION
0x30 (0xF0)	PARTNUM	Part number
0x31 (0xF1)	VERSION	Current version number
0x32 (0xF2)	FREQEST	Frequency offset estimate
0x33 (0xF3)	LQI	Demodulator estimate for link quality
0x34 (0xF4)	RSSI	Received signal strength indication
0x35 (0xF5)	MARCSTATE	Control state machine state
0x36 (0xF6)	WORTIME1	High byte of WOR timer
0x37 (0xF7)	WORTIME0	Low byte of WOR timer
0x38 (0xF8)	PKTSTATUS	Current GDOx status and packet status
0x39 (0xF9)	VCO_VC_DAC	Current setting from PLL calibration module
0x3A (0xFA)	TXBYTES	Underflow and number of bytes in the TX FIFO
0x3B (0xFB)	RXBYTES	Overflow and number of bytes in the RX FIFO
0x3C (0xFC)	RCCTRL1_STATUS	Last RC oscillator calibration result
0x3D (0xFD)	RCCTRL0_STATUS	Last RC oscillator calibration result

Table 4-4. Status Byte Summary

BIT	FIELD NAME	DESCRIPTION		
7	CHIP_RDYn	Stays high until power and crystal have stabilized. Should always be low when using the SPI interface.		
06:04	STATE[2:0]	Indicates the current main state machine mode		
		Value	**State**	**Description**
		0	IDLE	IDLE state (Also reported for some transitional states instead of SETTLING or CALIBRATE)
		1	RX	Receive mode
		10	TX	Transmit mode
		11	FSTXON	Fast TX ready
		100	CALIBRATE	Frequency synthesizer calibration is running
		101	SETTLING	PLL is settling
		110	RXFIFO_OVERFLOW	RX FIFO has overflowed. Read out any useful data, then flush the FIFO with SFRX
		111	TXFIFO_UNDERFLOW	TX FIFO has underflowed. Acknowledge with SFTX.
03:00	FIFO_BYTES_AVAILABLE[3:0]	The number of bytes available in the RX FIFO or free bytes in the TX FIFO		

Table 4-5. Received Packet Status Byte 1 (First Byte Appended After Data)

BIT	FIELD NAME	DESCRIPTION
7:0	RSSI	RSSI value

Table 4-6. Received Packet Status Byte 2 (Second Byte Appended After Data)

BIT	FIELD NAME	DESCRIPTION
7	CRC_OK	1: CRC for received data OK (or CRC disabled) 0: CRC error in received data
6:0	LQI	Indicating the link quality

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Table 4-7. SPI Address Space

	WRITE		READ		
	SINGLE BYTE	BURST	SINGLE BYTE	BURST	
	+0x00	+0x40	+0x80	+0xC0	
0x00	IOCFG2				R/W configuration registers, burst access possible
0x01	IOCFG1				
0x02	IOCFG0				
0x03	FIFOTHR				
0x04	SYNC1				
0x05	SYNC0				
0x06	PKTLEN				
0x07	PKTCTRL1				
0x08	PKTCTRL0				
0x09	ADDR				
0x0A	CHANNR				
0x0B	FSCTRL1				
0x0C	FSCTRL0				
0x0D	FREQ2				
0x0E	FREQ1				
0x0F	FREQ0				
0x10	MDMCFG4				
0x11	MDMCFG3				
0x12	MDMCFG2				
0x13	MDMCFG1				
0x14	MDMCFG0				
0x15	DEVIATN				
0x16	MCSM2				
0x17	MCSM1				
0x18	MCSM0				
0x19	FOCCFG				
0x1A	BSCFG				
0x1B	AGCCTRL2				
0x1C	AGCCTRL1				
0x1D	AGCCTRL0				
0x1E	WOREVT1				
0x1F	WOREVT0				
0x20	WORCTRL				
0x21	FREND1				
0x22	FREND0				
0x23	FSCAL3				
0x24	FSCAL2				
0x25	FSCAL1				
0x26	FSCAL0				
0x27	RCCTRL1				
0x28	RCCTRL0				
0x29	FSTEST				
0x2A	PTEST				
0x2B	AGCTEST				
0x2C	TEST2				
0x2D	TEST1				
0x2E	TEST0				
0x2F					

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Table 4-7. SPI Address Space (continued)

	WRITE		READ		
	SINGLE BYTE	BURST	SINGLE BYTE	BURST	
	+0x00	+0x40	+0x80	+0xC0	
0x30	SRES		SRES	PARTNUM	Command Strobes, Status registers (read only) and multi byte registers
0x31	SFSTXON		SFSTXON	VERSION	
0x32	SXOFF		SXOFF	FREQEST	
0x33	SCAL		SCAL	LQI	
0x34	SRX		SRX	RSSI	
0x35	STX		STX	MARCSTATE	
0x36	SIDLE		SIDLE	WORTIME1	
0x37				WORTIME0	
0x38	SWOR		SWOR	PKTSTATUS	
0x39	SPWD		SPWD	VCO_VC_DAC	
0x3A	SFRX		SFRX	TXBYTES	
0x3B	SFTX		SFTX	RXBYTES	
0x3C	SWORRST		SWORRST	RCCTRL1_STATUS	
0x3D	SNOP		SNOP	RCCTRL0_STATUS	
0x3E	PATABLE	PATABLE	PATABLE	PATABLE	
0x3F	TX FIFO	TX FIFO	RX FIFO	RX FIFO	

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4.2 Register Details

4.2.1 Configuration Register Details – Registers With Preserved Values In Sleep State

0x00: IOCFG2 – GDO2 Output Pin Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	Reserved		R0	
6	GDO2_INV	0	R/W	Invert output; i.e., select active low (1) or active high (0)
5:0	GDO2_CFG[5:0]	41 (0x29)	R/W	Default is CHP_RDYn (see Table 3-17).

0x01: IOCFG1 – GDO1 Output Pin Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	GDO_DS	0	R/W	Set high (1) or low (0) output drive strength on the GDO pins.
6	GDO1_INV	0	R/W	Invert output; i.e., select active low (1) or active high (0)
5:0	GDO1_CFG[5:0]	46 (0x2E)	R/W	Default is 3-state (see Table 3-17).

0x02: IOCFG0 – GDO0 Output Pin Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	TEMP_SENSOR_ENABLE	0	R/W	Enable analog temperature sensor. Write 0 in all other register bits when using temperature sensor.
6	GDO0_INV	0	R/W	Invert output; i.e., select active low (1) or active high (0)
5:0	GDO0_CFG[5:0]	63 (0x3F)	R/W	Default is CLK_XOSC/192 (see Table 3-17). It is recommended to disable the clock output in initialization to optimize RF performance.

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0x03: FIFOTHR – RX FIFO and TX FIFO Thresholds

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	Reserved	0	R/W	Write 0 for compatibility with possible future extensions
6	ADC_RETENTION	0	R/W	0: TEST1 = 0x31 and TEST2 = 0x88 when waking up from SLEEP 1: TEST1 = 0x35 and TEST2 = 0x81 when waking up from SLEEP Note that the changes in the TEST registers due to the ADC_RETENTION bit setting are only seen INTERNALLY in the analog part. The values read from the TEST registers when waking up from SLEEP mode are always the reset value. The ADC_RETENTION bit should be set to 1 before going into SLEEP mode if settings with an RX filter bandwidth below 325 kHz are wanted at time of wake-up.
5:4	CLOSE_IN_RX [1:0]	0 (00)	R/W	For more details, see *Close-in Reception With CC1101* (SWRA147). Setting: 0 (00) – RX Attenuation, Typical Values: 0 dB Setting: 1 (01) – RX Attenuation, Typical Values: 6 dB Setting: 2 (10) – RX Attenuation, Typical Values: 12 dB Setting: 3 (11) – RX Attenuation, Typical Values: 18 dB
3:0	FIFO_THR[3:0]	7 (0111)	R/W	Set the threshold for the TX FIFO and RX FIFO. The threshold is exceeded when the number of bytes in the FIFO is equal to or higher than the threshold value. Setting: 0 (0000) – Bytes in TX FIFO: 61 – Bytes in RX FIFO: 4 Setting: 1 (0001) – Bytes in TX FIFO: 57 – Bytes in RX FIFO: 8 Setting: 2 (0010) – Bytes in TX FIFO: 53 – Bytes in RX FIFO: 12 Setting: 3 (0011) – Bytes in TX FIFO: 49 – Bytes in RX FIFO: 16 Setting: 4 (0100) – Bytes in TX FIFO: 45 – Bytes in RX FIFO: 20 Setting: 5 (0101) – Bytes in TX FIFO: 41 – Bytes in RX FIFO: 24 Setting: 6 (0110) – Bytes in TX FIFO: 37 – Bytes in RX FIFO: 28 Setting: 7 (0111) – Bytes in TX FIFO: 33 – Bytes in RX FIFO: 32 Setting: 8 (1000) – Bytes in TX FIFO: 29 – Bytes in RX FIFO: 36 Setting: 9 (1001) – Bytes in TX FIFO: 25 – Bytes in RX FIFO: 40 Setting: 10 (1010) – Bytes in TX FIFO: 21 – Bytes in RX FIFO: 44 Setting: 11 (1011) – Bytes in TX FIFO: 17 – Bytes in RX FIFO: 48 Setting: 12 (1100) – Bytes in TX FIFO: 13 – Bytes in RX FIFO: 52 Setting: 13 (1101) – Bytes in TX FIFO: 9 – Bytes in RX FIFO: 56 Setting: 14 (1110) – Bytes in TX FIFO: 5 – Bytes in RX FIFO: 60 Setting: 15 (1111) – Bytes in TX FIFO: 1 – Bytes in RX FIFO: 64

0x04: SYNC1 – Sync Word, High Byte

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	SYNC[15:8]	211 (0xD3)	R/W	8 MSB of 16-bit sync word

0x05: SYNC0 – Sync Word, Low Byte

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	SYNC[7:0]	145 (0x91)	R/W	8 LSB of 16-bit sync word

0x06: PKTLEN – Packet Length

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	PACKET_LENGTH	255 (0xFF)	R/W	Indicates the packet length when fixed packet length mode is enabled. If variable packet length mode is used, this value indicates the maximum packet length allowed.

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0x07: PKTCTRL1 – Packet Automation Control

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:5	PQT[2:0]	0 (0x00)	R/W	Preamble quality estimator threshold. The preamble quality estimator increases an internal counter by one each time a bit is received that is different from the previous bit, and decreases the counter by 8 each time a bit is received that is the same as the last bit. A threshold of 4 × PQT for this counter is used to gate sync-word detection. When PQT = 0 a sync word is always accepted.
4	Reserved	0	R0	
3	CRC_AUTOFLUSH	0	R/W	Enable automatic flush of RX FIFO when CRC in not OK. This requires that only one packet is in the RX FIFO and that packet length is limited to the RX FIFO size.
2	APPEND_STATUS	1	R/W	When enabled, two status bytes are appended to the payload of the packet. The status bytes contain RSSI and LQI values, as well as CRC OK.
1:0	ADR_CHK[1:0]	0 (00)	R/W	Controls address check configuration of received packages.

Setting	Address Check Configuration
0 (00)	No address check
1 (01)	Address check, no broadcast
2 (10)	Address check and 0 (0x00) broadcast
3 (11)	Address check and 0 (0x00) and 255 (0xFF) broadcast

0x08: PKTCTRL0 – Packet Automation Control

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	Reserved		R0	
6	WHITE_DATA	1	R/W	Turn data whitening on/off 0: Whitening off 1: Whitening on
5:4	PKT_FORMAT[1:0]	0 (00)	R/W	Format of RX and TX data

Setting	Packet Format
0 (00)	Normal mode, use FIFOs for RX and TX
1 (01)	Synchronous serial mode. Used for backwards compatibility. Data in on GDO0
2 (10)	Random TX mode. Sends random data using PN9 generator. Used for test. Works as normal mode, setting 0 (00), in RX.
3 (11)	Asynchronous serial mode. Data in on GDO0 and Data out on either of the GDO0 pins

3	Reserved	0	R0	
2	CRC_EN	1	R/W	Enable CRC 1: CRC calculation in TX and CRC check in RX enabled 0: CRC disabled for TX and RX
1:0	LENGTH_CONFIG[1:0]	1 (01)	R/W	Configure the packet length

Setting	Packet Length Configuration
0 (00)	Fixed packet length mode. Length configured in PKTLEN register
1 (01)	Variable packet length mode. Packet length configured by the first byte after sync word
2 (10)	Infinite packet length mode
3 (11)	Reserved

0x09: ADDR – Device Address

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	DEVICE_ADDR[7:0]	0 (0x00)	R/W	Address used for packet filtration. Optional broadcast addresses are 0 (0x00) and 255 (0xFF).

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0x0A: CHANNR – Channel Number

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	CHAN[7:0]	0 (0x00)	R/W	The 8-bit unsigned channel number, which is multiplied by the channel spacing setting and added to the base frequency.

0x0B: FSCTRL1 – Frequency Synthesizer Control

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:5	Reserved		R0	
4:0	FREQ_IF[4:0]	15 (0x0F)	R/W	The desired IF frequency to employ in RX. Subtracted from FS base frequency in RX and controls the digital complex mixer in the demodulator. $f_{IF} = (f_{XOSC}/2^{10}) \times FREQ_IF$ The default value gives an IF frequency of 381 kHz, assuming a 26-MHz crystal.

0x0C: FSCTRL0 – Frequency Synthesizer Control

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	FREQOFF[7:0]	0 (0x00)	R/W	Frequency offset added to the base frequency before being used by the frequency synthesizer (twos complement). Resolution is $f_{XTAL}/2^{14}$ (1.59 kHz to 1.65 kHz). Range is ±202 kHz to ±210 kHz, dependent on crystal frequency.

0x0D: FREQ2 – Frequency Control Word, High Byte

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:6	FREQ[23:22]	0 (00)	R	FREQ[23:22] is always 0 (the FREQ2 register is less than 36 with 26-MHz to 27-MHz crystal)
5:0	FREQ[21:16]	30 (0x1E)	R/W	FREQ[23:22] is the base frequency for the frequency synthesizer in increments of $f_{XOSC}/2^{16}$. $f_{carrier} = (f_{XOSC}/2^{16}) \times FREQ[23:0]$

0x0E: FREQ1 – Frequency Control Word, Middle Byte

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	FREQ[15:8]	196 (0xC4)	R/W	See description in FREQ2 register

0x0F: FREQ0 – Frequency Control Word, Low Byte

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	FREQ[7:0]	236 (0xEC)	R/W	See description in FREQ2 register

0x10: MDMCFG4 – Modem Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:6	CHANBW_E[1:0]	2 (0x02)	R/W	
5:4	CHANBW_M[1:0]	0 (0x00)	R/W	Sets the decimation ratio for the delta-sigma ADC input stream and thus the channel bandwidth. The default values give 203 kHz channel filter bandwidth, assuming a 26-MHz crystal.
3:0	DRATE_E[3:0]	12 (0x0C)	R/W	The exponent of the user specified symbol rate

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0x11: MDMCFG3 – Modem Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	DRATE_M[7:0]	34 (0x22)	R/W	The mantissa of the user specified symbol rate. The symbol rate is configured using an unsigned, floating-point number with 9-bit mantissa and 4-bit exponent. The 9th bit is a hidden 1. The resulting data rate is: The default values give a data rate of 115.051 kBaud (closest setting to 115.2 kBaud), assuming a 26-MHz crystal.

0x12: MDMCFG2 – Modem Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	DEM_DCFILT_OFF	0	R/W	Disable digital dc blocking filter before demodulator. 0 = Enable (better sensitivity) 1 = Disable (current optimized). Only for data rates ≤ 250 kBaud. The recommended IF frequency changes when the dc blocking is disabled. Use SmartRF Studio to calculate correct register setting.
6:4	MOD_FORMAT[2:0]	0 (000)	R/W	The modulation format of the radio signal **Setting** / **Modulation Format** 0 (000) 2-FSK 1 (001) GFSK 2 (010) Reserved 3 (011) ASK/OOK 4 (100) Reserved 5 (101) Reserved 6 (110) Reserved 7 (111) MSK ASK is supported only for output powers up to –1 dBm MSK is supported only for data rates above 26 kBaud
3	MANCHESTER_EN	0	R/W	Enables Manchester encoding/decoding. 0 = Disable 1 = Enable
2:0	SYNC_MODE[2:0]	2 (010)	R/W	Combined sync-word qualifier mode. The values 0 (000) and 4 (100) disables preamble and sync word transmission in TX and preamble and sync word detection in RX. The values 1 (001), 2 (010), 5 (101) and 6 (110) enables 16-bit sync word transmission in TX and 16-bits sync word detection in RX. Only 15 of 16 bits need to match in RX when using setting 1 (001) or 5 (101). The values 3 (011) and 7 (111) enables repeated sync word transmission in TX and 32-bits sync word detection in RX (only 30 of 32 bits need to match). **Setting** / **Sync-Word Qualifier Mode** 0 (000) No preamble/sync 1 (001) 15/16 sync word bits detected 2 (010) 16/16 sync word bits detected 3 (011) 30/32 sync word bits detected 4 (100) No preamble/sync, carrier-sense above threshold 5 (101) 15/16 + carrier-sense above threshold 6 (110) 16/16 + carrier-sense above threshold 7 (111) 30/32 + carrier-sense above threshold

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0x13: MDMCFG1– Modem Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	FEC_EN	0	R/W	Enable Forward Error Correction (FEC) with interleaving for packet payload 0 = Disable 1 = Enable (Only supported for fixed packet length mode, i.e. PKTCTRL0.LENGTH_CONFIG = 0)
6:4	NUM_PREAMBLE[2:0]	2 (010)	R/W	Sets the minimum number of preamble bytes to be transmitted
3:2	Reserved		R0	
1:0	CHANSPC_E[1:0]	2 (10)	R/W	Two bit exponent of channel spacing

Setting	Number of Preamble Bytes
0 (000)	2
1 (001)	3
2 (010)	4
3 (011)	6
4 (100)	8
5 (101)	12
6 (110)	16
7 (111)	24

0x14: MDMCFG0 – Modem Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	CHANSPC_M[7:0]	248 (0xF8)	R/W	8-bit mantissa of channel spacing. The channel spacing is multiplied by the channel number CHAN and added to the base frequency. It is unsigned and has the format: The default values give 199.951 kHz channel spacing (the closest setting to 200 kHz), assuming 26-MHz crystal frequency.

0x15: DEVIATN – Modem Deviation Setting

BIT	FIELD NAME	RESET	R/W	DESCRIPTION	
7	Reserved		R0	Reserved	
6:4	DEVIATION_E[2:0]	4 (100b)	R/W	Deviation exponent	
3	Reserved		R0	Reserved	
2:0	DEVIATION_M[2:0]	7 (111b)	R/W	Transmit	
				2-FSK/ GFSK	Specifies the nominal frequency deviation from the carrier for a 0 (–DEVIATN) and 1 (+DEVIATN) in a mantissa-exponent format, interpreted as a 4-bit value with MSB implicit 1. The resulting frequency deviation is given by: The default values give ±47.607-kHz deviation assuming 26.0-MHz crystal frequency.
				MSK	Specifies the fraction of symbol period (1/8-8/8) during which a phase change occurs (0: +90°, 1: –90°). See the SmartRF Studio software [8] for correct DEVIATN setting when using MSK.
				ASK/ OOK	This setting has no effect.
				Receive	
				2-FSK/ GFSK	Specifies the expected frequency deviation of incoming signal, and must be approximately correct for demodulation to be performed reliably and robustly.
				MSK/ ASK/ OOK	This setting has no effect.

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0x16: MCSM2 – Main Radio Control State Machine Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:5	Reserved		R0	Reserved
4	RX_TIME_RSSI	0	R/W	Direct RX termination based on RSSI measurement (carrier sense). For ASK/OOK modulation, RX times out if there is no carrier sense in the first 8 symbol periods.
3	RX_TIME_QUAL	0	R/W	When the RX_TIME timer expires, the chip checks if sync word is found when RX_TIME_QUAL = 0, or either sync word is found or PQI is set when RX_TIME_QUAL = 1.
2:0	RX_TIME[2:0]	7 (111)	R/W	Timeout for sync word search in RX for both WOR mode and normal RX operation. The timeout is relative to the programmed EVENT0 timeout. The RX timeout in µs is given by EVENT0 × C(RX_TIME, WOR_RES) × 26/X, where C is given by the following table, and X is the crystal oscillator frequency in MHz.

	WOR_RES			
Setting	**0**	**1**	**2**	**3**
0 (000)	3.6058	18.0288	32.4519	46.875
1 (001)	1.8029	9.0144	16.226	23.4375
2 (010)	0.9014	4.5072	8.113	11.7188
3 (011)	0.4507	2.2536	4.0565	5.8594
4 (100)	0.2254	1.1268	2.0282	2.9297
5 (101)	0.1127	0.5634	1.0141	1.4648
6 (110)	0.0563	0.2817	0.5071	0.7324
7 (111)	Until end of packet			

As an example, EVENT0 = 34666, WOR_RES = 0 and RX_TIME = 6 corresponds to 1.96-ms RX timeout, 1-s polling interval and 0.195% duty cycle. Note that WOR_RES should be 0 or 1 when using WOR, because using WOR_RES > 1 gives a very low duty cycle. In applications where WOR is not used all settings of WOR_RES can be used.

The duty cycle using WOR is approximated by:

	WOR_RES	
Setting	**0**	**1**
0 (000)	12.50%	1.95%
1 (001)	6.25%	9765 ppm
2 (010)	3.13%	4883 ppm
3 (011)	1.56%	2441 ppm
4 (100)	0.78%	NA
5 (101)	0.39%	NA
6 (110)	0.20%	NA
7 (111)	NA	

Note that the RC oscillator must be enabled to use setting 0-6, because the timeout counts RC oscillator periods. WOR mode does not need to be enabled.

The timeout counter resolution is limited: With RX_TIME = 0, the timeout count is given by the 13 MSBs of EVENT0, decreasing to the 7 MSBs of EVENT0 with RX_TIME = 6.

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0x17: MCSM1 – Main Radio Control State Machine Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:6	Reserved		R0	
5:4	CCA_MODE[1:0]	3 (11)	R/W	Selects CCA_MODE. Reflected in CCA signal.

Setting	Clear Channel Indication
0 (00)	Always
1 (01)	If RSSI below threshold
2 (10)	Unless currently receiving a packet
3 (11)	If RSSI below threshold unless currently receiving a packet

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
3:2	RXOFF_MODE[1:0]	0 (00)	R/W	Select what should happen when a packet has been received

Setting	Next State After Finishing Packet Reception
0 (00)	IDLE
1 (01)	FSTXON
2 (10)	TX
3 (11)	Stay in RX

It is not possible to set RXOFF_MODE to be TX or FSTXON and at the same time use CCA.

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
1:0	TXOFF_MODE[1:0]	0 (00)	R/W	Select what should happen when a packet has been sent (TX)

Setting	Next State After Finishing Packet Transmission
0 (00)	IDLE
1 (01)	FSTXON
2 (10)	Stay in TX (start sending preamble)
3 (11)	RX

0x18: MCSM0 – Main Radio Control State Machine Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:6	Reserved		R0	
5:4	FS_AUTOCAL[1:0]	0 (00)	R/W	Automatically calibrate when going to RX or TX, or back to IDLE

Setting	When To Perform Automatic Calibration
0 (00)	Never (manually calibrate using SCAL strobe)
1 (01)	When going from IDLE to RX or TX (or FSTXON)
2 (10)	When going from RX or TX back to IDLE automatically
3 (11)	Every 4th time when going from RX or TX to IDLE automatically

In some automatic wake-on-radio (WOR) applications, using setting 3 (11) can significantly reduce current consumption.

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
3:2	PO_TIMEOUT	1 (01)	R/W	Programs the number of times the six-bit ripple counter must expire after XOSC has stabilized before CHP_RDYn goes low. If XOSC is on (stable) during power-down, PO_TIMEOUT should be set so that the regulated digital supply voltage has time to stabilize before CHP_RDYn goes low (PO_TIMEOUT = 2 recommended). Typical start-up time for the voltage regulator is 50 us. If XOSC is off during power-down and the regulated digital supply voltage has sufficient time to stabilize while waiting for the crystal to be stable, PO_TIMEOUT can be set to 0. For robust operation it is recommended to use PO_TIMEOUT = 2.

Setting	Expire Count	Timeout After XOSC Start
0 (00)	1	Approximately 2.3 µs to 2.4 µs
1 (01)	16	Approximately 37 µs to 39 µs
2 (10)	64	Approximately 149 µs to 155 µs
3 (11)	256	Approximately 597 µs to 620 µs

Exact timeout depends on crystal frequency.

1	PIN_CTRL_EN	0	R/W	Enables the pin radio control option
0	XOSC_FORCE_ON	0	R/W	Force the XOSC to stay on in the SLEEP state.

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0x19: FOCCFG – Frequency Offset Compensation Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:6	Reserved		R0	
5	FOC_BS_CS_GATE	1	R/W	If set, the demodulator freezes the frequency offset compensation and clock recovery feedback loops until the CS signal goes high.
4:3	FOC_PRE_K[1:0]	2 (10)	R/W	The frequency compensation loop gain to be used before a sync word is detected. **Setting** / **Frequency Compensation Loop Gain Before Sync Word** 0 (00) – K 1 (01) – 2K 2 (10) – 3K 3 (11) – 4K
2	FOC_POST_K	1	R/W	The frequency compensation loop gain to be used after a sync word is detected. **Setting** / **Frequency Compensation Loop Gain After Sync Word** 0 – Same as FOC_PRE_K 1 – K/2
1:0	FOC_LIMIT[1:0]	2 (10)	R/W	The saturation point for the frequency offset compensation algorithm: **Setting** / **Saturation Point (Maximum Compensated Offset)** 0 (00) – ±0 (no frequency offset compensation) 1 (01) – $\pm BW_{CHAN}/8$ 2 (10) – $\pm BW_{CHAN}/4$ 3 (11) – $\pm BW_{CHAN}/2$ Frequency offset compensation is not supported for ASK/OOK. Always use FOC_LIMIT = 0 with these modulation formats.

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0x1A: BSCFG – Bit Synchronization Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:6	BS_PRE_KI[1:0]	1 (01)	R/W	The clock recovery feedback loop integral gain to be used before a sync word is detected (used to correct offsets in data rate):

Setting	Clock Recovery Loop Integral Gain Before Sync Word
0 (00)	K_I
1 (01)	$2K_I$
2 (10)	$3K_I$
3 (11)	$4K_I$

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
5:4	BS_PRE_KP[1:0]	2 (10)	R/W	The clock recovery feedback loop proportional gain to be used before a sync word is detected.

Setting	Clock Recovery Loop Proportional Gain Before Sync Word
0 (00)	K_P
1 (01)	$2K_P$
2 (10)	$3K_P$
3 (11)	$4K_P$

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
3	BS_POST_KI	1	R/W	The clock recovery feedback loop integral gain to be used after a sync word is detected.

Setting	Clock Recovery Loop Integral Gain After Sync Word
0	Same as BS_PRE_KI
1	K_I /2

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
2	BS_POST_KP	1	R/W	The clock recovery feedback loop proportional gain to be used after a sync word is detected.

Setting	Clock Recovery Loop Proportional Gain After Sync Word
0	Same as BS_PRE_KP
1	K_P

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
1:0	BS_LIMIT[1:0]	0 (00)	R/W	The saturation point for the data rate offset compensation algorithm:

Setting	Data Rate Offset Saturation (Max Data Rate Difference)
0 (00)	±0 (No data rate offset compensation performed)
1 (01)	±3.125% data rate offset
2 (10)	±6.25% data rate offset
3 (11)	±12.5% data rate offset

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0x1B: AGCCTRL2 – AGC Control

BIT	FIELD NAME	RESET	R/W	DESCRIPTION	
7:6	MAX_DVGA_GAIN[1:0]	0 (00)	R/W	Reduces the maximum allowable DVGA gain.	
				Setting	**Allowable DVGA Settings**
				0 (00)	All gain settings can be used
				1 (01)	The highest gain setting can not be used
				2 (10)	The 2 highest gain settings can not be used
				3 (11)	The 3 highest gain settings can not be used
5:3	MAX_LNA_GAIN[2:0]	0 (000)	R/W	Sets the maximum allowable LNA + LNA 2 gain relative to the maximum possible gain.	
				Setting	**Maximum Allowable LNA + LNA 2 Gain**
				0 (000)	Maximum possible LNA + LNA 2 gain
				1 (001)	Approximately 2.6 dB below maximum possible gain
				2 (010)	Approximately 6.1 dB below maximum possible gain
				3 (011)	Approximately 7.4 dB below maximum possible gain
				4 (100)	Approximately 9.2 dB below maximum possible gain
				5 (101)	Approximately 11.5 dB below maximum possible gain
				6 (110)	Approximately 14.6 dB below maximum possible gain
				7 (111)	Approximately 17.1 dB below maximum possible gain
2:0	MAGN_TARGET[2:0]	3 (011)	R/W	These bits set the target value for the averaged amplitude from the digital channel filter (1 LSB = 0 dB).	
				Setting	**Target Amplitude From Channel Filter**
				0 (000)	24 dB
				1 (001)	27 dB
				2 (010)	30 dB
				3 (011)	33 dB
				4 (100)	36 dB
				5 (101)	38 dB
				6 (110)	40 dB
				7 (111)	42 dB

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0x1C: AGCCTRL1 – AGC Control

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	Reserved		R0	
6	AGC_LNA_PRIORITY	1	R/W	Selects between two different strategies for LNA and LNA 2 gain adjustment. When 1, the LNA gain is decreased first. When 0, the LNA 2 gain is decreased to minimum before decreasing LNA gain.
5:4	CARRIER_SENSE_REL_THR[1:0]	0 (00)	R/W	Sets the relative change threshold for asserting carrier sense
				Setting / **Carrier Sense Relative Threshold**
				0 (00) – Relative carrier sense threshold disabled
				1 (01) – 6 dB increase in RSSI value
				2 (10) – 10 dB increase in RSSI value
				3 (11) – 14 dB increase in RSSI value
3:0	CARRIER_SENSE_ABS_THR[3:0]	0 (0000)	R/W	Sets the absolute RSSI threshold for asserting carrier sense. The twos-complement signed threshold is programmed in steps of 1 dB and is relative to the MAGN_TARGET setting.
				Setting / **Carrier Sense Absolute Threshold** (Equal to channel filter amplitude when AGC has not decreased gain)
				-8 (1000) – Absolute carrier sense threshold disabled
				-7 (1001) – 7 dB below MAGN_TARGET setting
				⋮ – ⋮
				-1 (1111) – 1 dB below MAGN_TARGET setting
				0 (0000) – At MAGN_TARGET setting
				1 (0001) – 1 dB above MAGN_TARGET setting
				⋮ – ⋮
				7 (0111) – 7 dB above MAGN_TARGET setting

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0x1D: AGCCTRL0 – AGC Control

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:6	HYST_LEVEL[1:0]	2 (10)	R/W	Sets the level of hysteresis on the magnitude deviation (internal AGC signal that determine gain changes).

Setting	Description
0 (00)	No hysteresis, small symmetric dead zone, high gain
1 (01)	Low hysteresis, small asymmetric dead zone, medium gain
2 (10)	Medium hysteresis, medium asymmetric dead zone, medium gain
3 (11)	Large hysteresis, large asymmetric dead zone, low gain

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
5:4	WAIT_TIME[1:0]	1 (01)	R/W	Sets the number of channel filter samples from a gain adjustment has been made until the AGC algorithm starts accumulating new samples.

Setting	Channel Filter Samples
0 (00)	8
1 (01)	16
2 (10)	24
3 (11)	32

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
3:2	AGC_FREEZE[1:0]	0 (00)	R/W	Controls when the AGC gain should be frozen.

Setting	Function
0 (00)	Normal operation. Always adjust gain when required.
1 (01)	The gain setting is frozen when a sync word has been found.
2 (10)	Manually freeze the analog gain setting and continue to adjust the digital gain.
3 (11)	Manually freezes both the analog and the digital gain setting. Used for manually overriding the gain.

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
1:0	FILTER_LENGTH[1:0]	1 (01)	R/W	Sets the averaging length for the amplitude from the channel filter. Sets the OOK/ASK decision boundary for OOK/ASK reception.

Setting	Channel Filter Samples	OOK Decision
0 (00)	8	4 dB
1 (01)	16	8 dB
2 (10)	32	12 dB
3 (11)	64	16 dB

0x1E: WOREVT1 – High Byte Event0 Timeout

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	EVENT0[15:8]	135 (0x87)	R/W	High byte of EVENT0 timeout register

0x1F: WOREVT0 – Low Byte Event0 Timeout

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	EVENT0[7:0]	107 (0x6B)	R/W	Low byte of EVENT0 timeout register. The default EVENT0 value gives 1-s timeout, assuming a 26-MHz crystal.

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0x20: WORCTRL – Wake On Radio Control

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	RC_PD	1	R/W	Power down signal to RC oscillator. When written to 0, automatic initial calibration is performed
6:4	EVENT1[2:0]	7 (111)	R/W	Timeout setting from register block. Decoded to Event 1 timeout. RC oscillator clock frequency equals f_{XOSC}/750, which is 34.7 to 36 kHz, depending on crystal frequency. The following table lists the number of clock periods after Event 0 before Event 1 times out.
3	RC_CAL	1	R/W	Enables (1) or disables (0) the RC oscillator calibration.
2	Reserved		R0	
1:0	WOR_RES	0 (00)	R/W	Controls the Event 0 resolution as well as maximum timeout of the WOR module and maximum timeout under normal RX operation::

Setting	t_{Event1}
0 (000)	4 (0.111 to 0.115 ms)
1 (001)	6 (0.167 to 0.173 ms)
2 (010)	8 (0.222 to 0.230 ms)
3 (011)	12 (0.333 to 0.346 ms)
4 (100)	16 (0.444 to 0.462 ms)
5 (101)	24 (0.667 to 0.692 ms)
6 (110)	32 (0.889 to 0.923 ms)
7 (111)	48 (1.333 to 1.385 ms)

Setting	Resolution (1 LSB)	Maximum Timeout
0 (00)	1 period (28 to 29 µs)	1.8 to 1.9 seconds
1 (01)	25 periods (0.89 to 0.92 ms)	58 to 61 seconds
2 (10)	210 periods (28 to 30 ms)	31 to 32 minutes
3 (11)	215 periods (0.91 to 0.94 s)	16.5 to 17.2 hours

NOTE
WOR_RES should be 0 or 1 when using WOR, because WOR_RES > 1 results in a very low duty cycle.

In normal RX operation all settings of WOR_RES can be used.

0x21: FREND1 – Front End RX Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:6	LNA_CURRENT[1:0]	1 (01)	R/W	Adjusts front-end LNA PTAT current output
5:4	LNA2MIX_CURRENT[1:0]	1 (01)	R/W	Adjusts front-end PTAT outputs
3:2	LODIV_BUF_CURRENT_RX[1:0]	1 (01)	R/W	Adjusts current in RX LO buffer (LO input to mixer)
1:0	MIX_CURRENT[1:0]	2 (10)	R/W	Adjusts current in mixer

0x22: FREND0 – Front End TX Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:6	Reserved		R0	
5:4	LODIV_BUF_CURRENT_TX[1:0]	1 (0x01)	R/W	Adjusts current TX LO buffer (input to PA). The value to use in this field is given by the SmartRF Studio software.
3	Reserved		R0	
2:0	PA_POWER[2:0]	0 (0x00)	R/W	Selects PA power setting. This value is an index to the PATABLE, which can be programmed with up to 8 different PA settings. In OOK/ASK mode, this selects the PATABLE index to use when transmitting a 1. PATABLE index zero is used in OOK/ASK when transmitting a 0. The PATABLE settings from index 0 to the PA_POWER value are used for ASK TX shaping, and for power ramp-up/ramp-down at the start/end of transmission in all TX modulation formats.

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0x23: FSCAL3 – Frequency Synthesizer Calibration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:6	FSCAL3[7:6]	2 (0x02)	R/W	Frequency synthesizer calibration configuration. The value to write in this field before calibration is given by the SmartRF Studio software.
5:4	CHP_CURR_CAL_EN[1:0]	2 (0x02)	R/W	Enable charge pump calibration stage when 1
3:0	FSCAL3[3:0]	9 (1001)	R/W	Frequency synthesizer calibration result register. Digital bit vector defining the charge pump output current, on an exponential scale: $I_{OUT} = I_0 \times 2^{FSCAL3[3:0]/4}$ Fast frequency hopping without calibration for each hop can be done by calibrating earlier for each frequency and saving the resulting FSCAL3, FSCAL2, and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2, and FSCAL1 register values corresponding to the next RF frequency.

0x24: FSCAL2 – Frequency Synthesizer Calibration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:6	Reserved		R0	
5	VCO_CORE_H_EN	0	R/W	Choose high (1) / low (0) VCO
4:0	FSCAL2[4:0]	10 (0x0A)	R/W	Frequency synthesizer calibration result register. VCO current calibration result and override value. Fast frequency hopping without calibration for each hop can be done by calibrating earlier for each frequency and saving the resulting FSCAL3, FSCAL2, and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2, and FSCAL1 register values corresponding to the next RF frequency.

0x25: FSCAL1 – Frequency Synthesizer Calibration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:6	Reserved		R0	
5:0	FSCAL1[5:0]	32 (0x20)	R/W	Frequency synthesizer calibration result register. Capacitor array setting for VCO coarse tuning. Fast frequency hopping without calibration for each hop can be done by calibrating earlier for each frequency and saving the resulting FSCAL3, FSCAL2, and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2, and FSCAL1 register values corresponding to the next RF frequency.

0x26: FSCAL0 – Frequency Synthesizer Calibration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	Reserved		R0	
6:0	FSCAL0[6:0]	13 (0x0D)	R/W	Frequency synthesizer calibration control. The value to use in this register is given by the SmartRF Studio software.

0x27: RCCTRL1 – RC Oscillator Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	Reserved		R0	
6:0	FSCAL0[6:0]	65 (0x41)	R/W	RC oscillator configuration

0x28: RCCTRL0 – RC Oscillator Configuration

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	Reserved		R0	
6:0	RCCTRL0[6:0]	0 (0x00)	R/W	RC oscillator configuration

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4.2.2 Configuration Register Details – Registers that Lose Programming in SLEEP State

0x29: FSTEST – Frequency Synthesizer Calibration Control

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	FSTEST[7:0]	89 (0x59)	R/W	For test only. Do not write to this register.

0x2A: PTEST – Production Test

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	PTEST[7:0]	127 (0x7F)	R/W	Writing 0xBF to this register makes the on-chip temperature sensor available in the IDLE state. The default 0x7F value should then be written back before leaving the IDLE state. Other use of this register is for test only.

0x2B: AGCTEST – AGC Test

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	AGCTEST[7:0]	63 (0x3F)	R/W	For test only. Do not write to this register.

0x2C: TEST2 – Various Test Settings

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	TEST2[7:0]	136 (0x88)	R/W	The value to use in this register is given by the SmartRF Studio software. This register is forced to 0x88 or 0x81 when it wakes up from SLEEP mode, depending on the configuration of FIFOTHR. ADC_RETENTION.

0x2D: TEST1 – Various Test Settings

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	TEST1[7:0]	49 (0x31)	R/W	The value to use in this register is given by the SmartRF Studio software. This register is forced to 0x31 or 0x35 when it wakes up from SLEEP mode, depending on the configuration of FIFOTHR. ADC_RETENTION.

0x2E: TEST0 – Various Test Settings

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:2	TEST0[7:2]	2 (0x02)	R/W	The value to use in this register is given by the SmartRF Studio software.
1	VCO_SEL_CAL_EN	1	R/W	Enable VCO selection calibration stage when 1
0	TEST0[0]	1	R/W	The value to use in this register is given by the SmartRF Studio software.

4.2.3 Status Register Details

0x30 (0xF0): PARTNUM – Chip ID

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	PARTNUM[7:0]	0 (0x00)	R	Chip part number

0x31 (0xF1): VERSION – Chip ID

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	VERSION[7:0]	4 (0x04)	R	Chip version number

0x32 (0xF2): FREQEST – Frequency Offset Estimate From Demodulator

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	FREQOFF_EST		R	The estimated frequency offset (twos complement) of the carrier. Resolution is $f_{XTAL}/2^{14}$ (1.59 to 1.65 kHz). Range is ±202 kHz to ±210 kHz, dependent on XTAL frequency. Frequency offset compensation is only supported for 2-FSK, GFSK, and MSK modulation. This register reads 0 when using ASK or OOK modulation.

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0x33 (0xF3): LQI – Demodulator Estimate for Link Quality

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	CRC OK		R	The last CRC comparison matched. Cleared when entering/restarting RX mode.
6:0	LQI_EST[6:0]		R	The Link Quality Indicator estimates how easily a received signal can be demodulated. Calculated over the 64 symbols following the sync word.

0x34 (0xF4): RSSI – Received Signal Strength Indication

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	RSSI		R	Received signal strength indicator

0x35 (0xF5): MARCSTATE – Main Radio Control State Machine State

BIT	FIELD NAME	RESET	R/W	DESCRIPTION		
7:5	Reserved		R0			
4:0	MARC_STATE[4:0]		R	Main radio control FSM state		
				Value	**State Name**	**State** (see Figure 3-15)
				0 (0x00)	SLEEP	SLEEP
				1 (0x01)	IDLE	IDLE
				2 (0x02)	XOFF	XOFF
				3 (0x03)	VCOON_MC	MANCAL
				4 (0x04)	REGON_MC	MANCAL
				5 (0x05)	MANCAL	MANCAL
				6 (0x06)	VCOON	FS_WAKEUP
				7 (0x07)	REGON	FS_WAKEUP
				8 (0x08)	STARTCAL	CALIBRATE
				9 (0x09)	BWBOOST	SETTLING
				10 (0x0A)	FS_LOCK	SETTLING
				11 (0x0B)	IFADCON	SETTLING
				12 (0x0C)	ENDCAL	CALIBRATE
				13 (0x0D)	RX	RX
				14 (0x0E)	RX_END	RX
				15 (0x0F)	RX_RST	RX
				16 (0x10)	TXRX_SWITCH	TXRX_SETTLING
				17 (0x11)	RXFIFO_OVERFLOW	RXFIFO_OVERFLOW
				18 (0x12)	FSTXON	FSTXON
				19 (0x13)	TX	TX
				20 (0x14)	TX_END	TX
				21 (0x15)	RXTX_SWITCH	RXTX_SETTLING
				22 (0x16)	TXFIFO_UNDERFLOW	TXFIFO_UNDERFLOW
				Note: It is not possible to read back the SLEEP or XOFF state numbers because setting $\overline{CS}$ low makes the chip enter the IDLE mode from the SLEEP or XOFF states.		

0x36 (0xF6): WORTIME1 – High Byte of WOR Time

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	TIME[15:8]		R	High byte of timer value in WOR module

0x37 (0xF7): WORTIME0 – Low Byte of WOR Time

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	TIME[7:0]		R	Low byte of timer value in WOR module

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0x38 (0xF8): PKTSTATUS – Current GDOx Status and Packet Status

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	CRC_OK		R	The last CRC comparison matched. Cleared when entering/restarting RX mode.
6	CS		R	Carrier sense
5	PQT_REACHED		R	Preamble Quality reached
4	CCA		R	Channel is clear
3	SFD		R	Sync word found. Asserted when sync word has been sent / received, and de-asserted at the end of the packet. In RX, this bit de-asserts when the optional address check fails or the radio enters RX_OVERFLOW state. In TX this bit de-asserts if the radio enters TX_UNDERFLOW state.
2	GDO2		R	Current GDO2 value. Note: the reading gives the non-inverted value irrespective of what IOCFG2.GDO2_INV is programmed to. It is not recommended to check for PLL lock by reading PKTSTATUS[2] with GDO2_CFG = 0x0A.
1	Reserved		R0	
0	GDO0		R	Current GDO0 value. Note: Gives the noninverted value, regardless of the IOCFG0.GDO0_INV setting. It is not recommended to check for PLL lock by reading PKTSTATUS[0] with GDO0_CFG = 0x0A.

0x39 (0xF9): VCO_VC_DAC – Current Setting from PLL Calibration Module

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7:0	VCO_VC_DAC[7:0]		R	Status register for test only

0x3A (0xFA): TXBYTES – Underflow and Number of Bytes

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	TXFIFO_UNDERFLOW		R	
6:0	NUM_TXBYTES		R	Number of bytes in TX FIFO

0x3B (0xFB): RXBYTES – Overflow and Number of Bytes

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	RXFIFO_OVERFLOW		R	
6:0	NUM_RXBYTES		R	Number of bytes in RX FIFO

0x3C (0xFC): RCCTRL1_STATUS – Last RC Oscillator Calibration Result

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	Reserved		R0	
6:0	RCCTRL1_STATUS[6:0]		R	Contains the value from the last run of the RC oscillator calibration routine. For usage description, see *CC1100/CC2500 – Wake-On-Radio* (SWRA126).

0x3D (0xFD): RCCTRL0_STATUS – Last RC Oscillator Calibration Result

BIT	FIELD NAME	RESET	R/W	DESCRIPTION
7	Reserved		R0	
6:0	RCCTRL0_STATUS[6:0]		R	Contains the value from the last run of the RC oscillator calibration routine. For usage description, see *CC1100/CC2500 – Wake-On-Radio* (SWRA126).

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5 Package and Shipping Information

5.1 Package Thermal Properties

Table 5-1. Thermal Properties of QFN-32 Package

THERMAL RESISTANCE	
Air velocity (m/s)	0
$R_{\theta JA}$ (K/W)	40.4

5.2 Soldering Information

The recommendations for lead-free reflow in IPC/JEDEC J-STD-020C should be followed.

5.3 Carrier Tape and Reel Specifications

Carrier tape and reel is in accordance with EIA Specification 481.

Table 5-2. Carrier Tape and Reel Specification

PACKAGE	TAPE WIDTH	COMPONENT PITCH	HOLE PITCH	REEL DIAMETER	UNITS PER REEL
QFN-32	12 mm	8 mm	4 mm	13 inches	3000

5.4 Ordering Information

Table 5-3. Ordering Information

TI PART NUMBER	DESCRIPTION	MINIMUM ORDER QUANTITY (MOQ)
CC1101IRHBRG4Q1	CC1101-Q1 Transceiver, QFN-32 (RHB), RoHS Pb-free, –40°C to 85°C	3000 (tape and reel)
CC1101TRHBRG4Q1	CC1101-Q1 Transceiver, QFN-32 (RHB), RoHS Pb-free, –40°C to 105°C	3000 (tape and reel)
CC1101QRHBRG4Q1	CC1101-Q1 Transceiver, QFN-32 (RHB), RoHS Pb-free, –40°C to 125°C	3000 (tape and reel)
CC1131IRHBRG4Q1	CC1131-Q1 Receiver, QFN-32 (RHB), RoHS Pb-free, –40°C to 85°C	3000 (tape and reel)
CC1131TRHBRG4Q1	CC1131-Q1 Receiver, QFN-32 (RHB), RoHS Pb-free, –40°C to 105°C	3000 (tape and reel)
CC1131QRHBRG4Q1	CC1131-Q1 Receiver, QFN-32 (RHB), RoHS Pb-free, –40°C to 125°C	3000 (tape and reel)
CC1151IRHBRG4Q1	CC1151-Q1 Transmitter, QFN-32 (RHB), RoHS Pb-free, –40°C to 85°C	3000 (tape and reel)
CC1151TRHBRG4Q1	CC1151-Q1 Transmitter, QFN-32 (RHB), RoHS Pb-free, –40°C to 105°C	3000 (tape and reel)
CC1151QRHBRG4Q1	CC1151-Q1 Transmitter, QFN-32 (RHB), RoHS Pb-free, –40°C to 125°C	3000 (tape and reel)

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6 References

[1] DN009 Upgrade from CC1100 to CC1101 (SWRA145)

[2] CC1101EM 315–433 MHz Reference Design (SWRR046)

[3] CC1101EM 868–915 MHz Reference Design (SWRR045)

[4] CC1101 Errata Notes (SWRZ020)

[5] AN001 SRD Regulations for Licence Free Transceiver Operation (SWRA090)

[6] AN050 Using the CC1101 in the European 868 MHz SRD Band (SWRA146)

[7] AN047 CC1100/CC2500 – Wake-On-Radio (SWRA126)

[8] SmartRF® Studio (SWRC046)

[9] CC1100 CC2500 Examples Libraries (SWRC021)

[10] CC1100/CC1150DK, CC1101DK, and CC2500/CC2550DK Examples and Libraries User Manual (SWRU109)

[11] DN010 Close-in Reception with CC1101 (SWRA147)

[12] DN017 CC11xx 868/915 MHz RF Matching (SWRA168)

[13] DN015 Permanent Frequency Offset Compensation (SWRA159)

[14] DN006 CC11xx Settings for FCC 15.247 Solutions (SWRA123)

[15] DN505 RSSI Interpretation and Timing (SWRA114)

[16] AN058 Antenna Selection Guide (SWRA161)

[17] AN067 Wireless MBUS Implementation with CC1101 and MSP430 (SWRA234)

[18] DN013 Programming Output Power on CC1101 (SWRA168)

[19] DN022 CC11xx OOK/ASK register settings (SWRA215)

[20] DN005 CC11xx Sensitivity versus Frequency Offset and Crystal Accuracy (SWRA122)

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

REVISION	COMMENTS
SWRS076	Initial Product Preview release
SWRS076A	Changed first TYP value for "Current consumption in power-down modes" in Section 2.4 from 1.1 µA to 0.7 µA. Changed unit for rejection parameters in Section 2.5 from dBm to dB. Updated current consumption values in Figure 3-4.
SWRS076B	Change all instances of "387 MHz to 464 MHz" to "420 MHz to 450 MHz".

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
CC1101IRHBRG4Q1	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CC1101QRHBRG4Q1	ACTIVE	QFN	RHB	32	3000	TBD	Call TI	Call TI	
CC1101TRHBRG4Q1	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CC1131IRHBRG4Q1	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CC1131QRHBRG4Q1	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CC1131TRHBRG4Q1	ACTIVE	QFN	RHB	32	3000	TBD	Call TI	Call TI	
CC1151IRHBRG4Q1	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CC1151QRHBRG4Q1	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CC1151TRHBRG4Q1	ACTIVE	QFN	RHB	32	3000	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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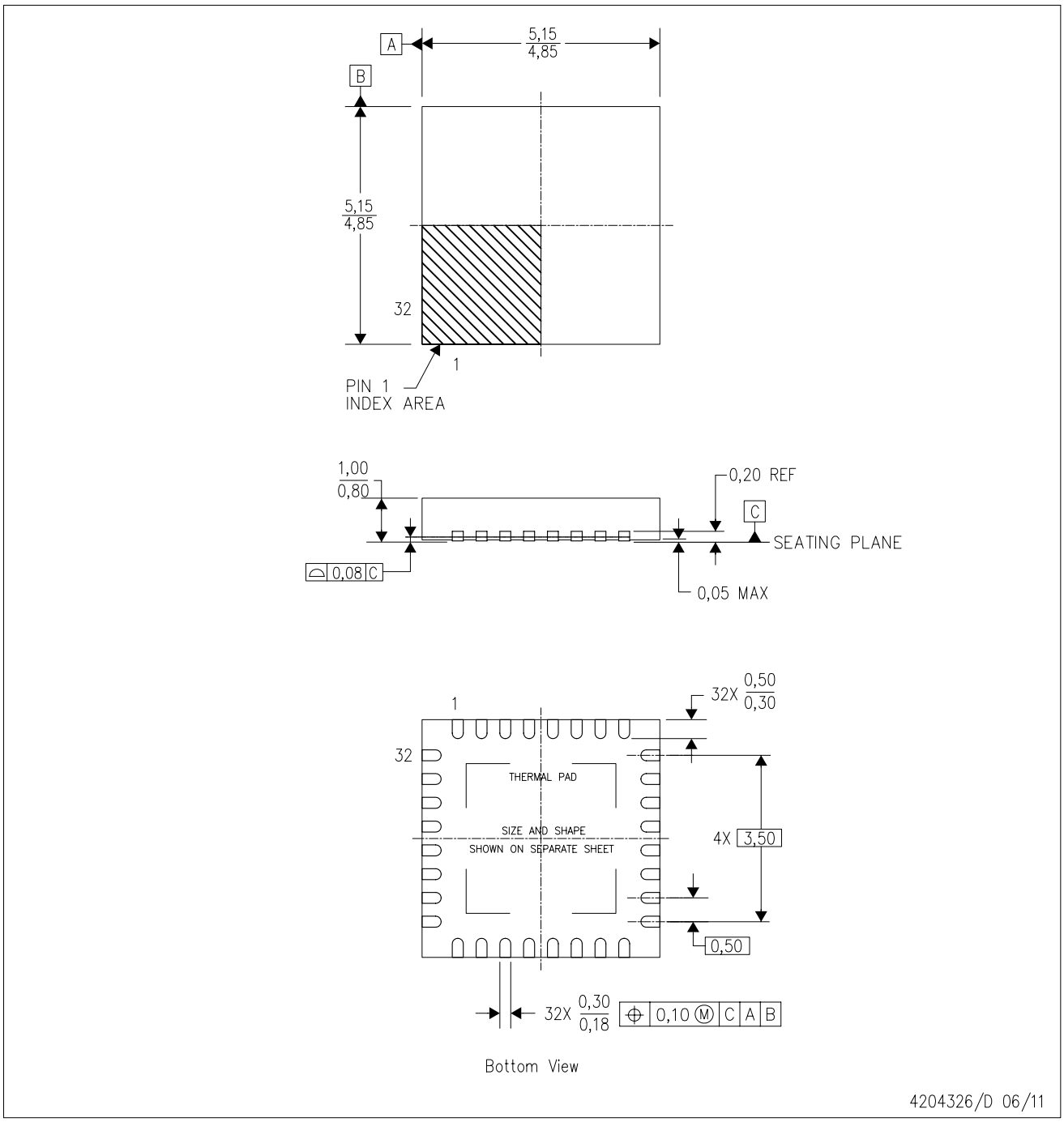
OTHER QUALIFIED VERSIONS OF CC1101-Q1 :

- Catalog: CC1101

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

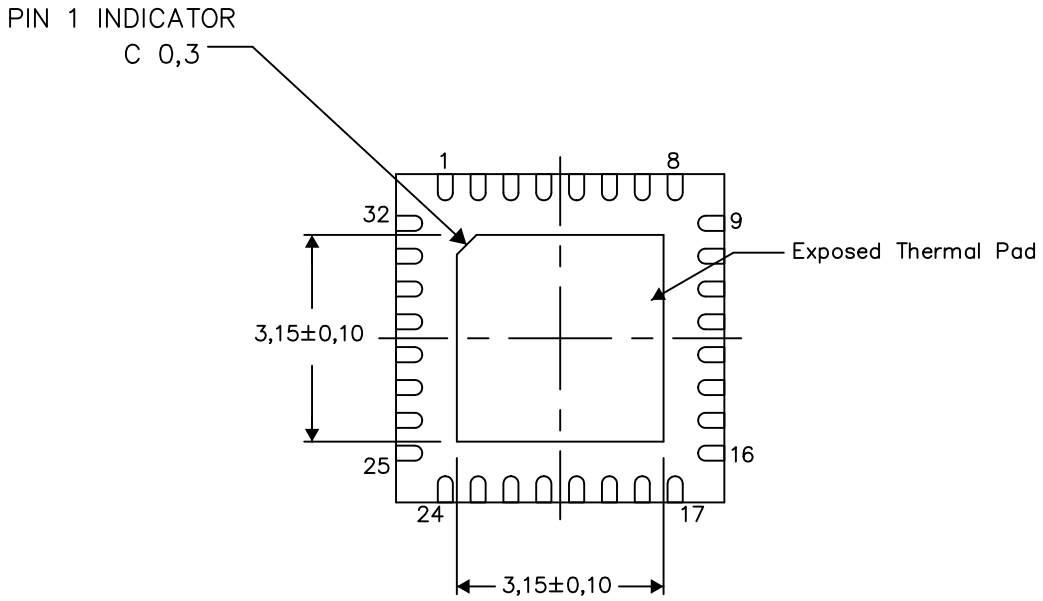
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



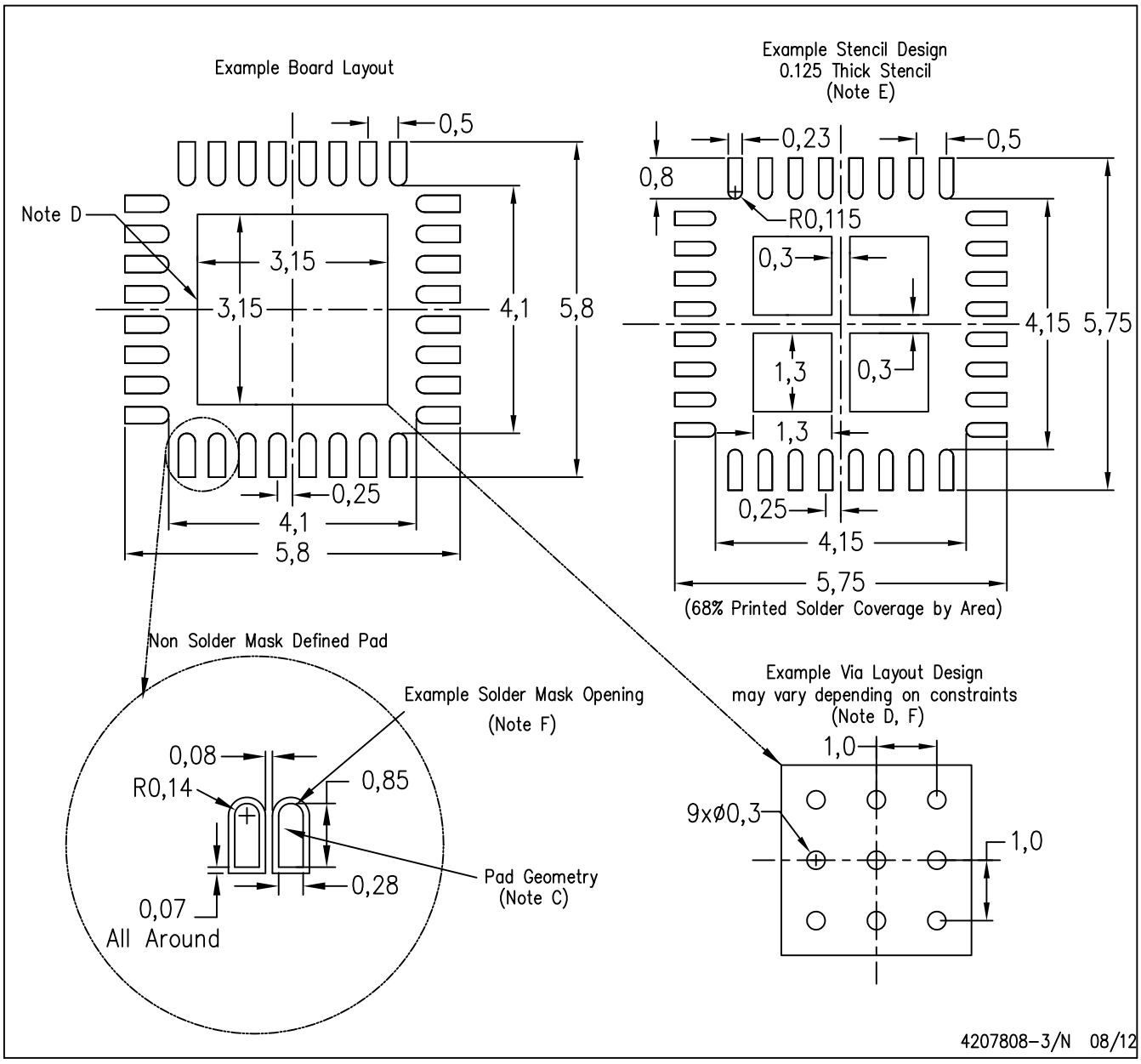
Bottom View

Exposed Thermal Pad Dimensions

4206356–3/W 09/12

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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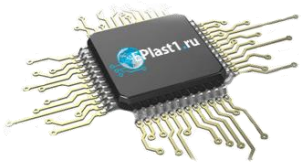

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