

2.5 V or 3.3 V, 200 MHz, 1:18 Clock Distribution Buffer

Features

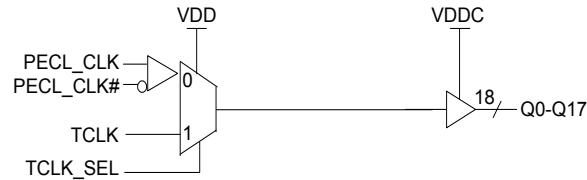
- 200 MHz clock support
- LVPECL or LVCMOS/LVTTL clock input
- LVCMOS/LVTTL compatible inputs
- 18 clock outputs: drive up to 36 clock lines
- 60 ps typical output-to-output skew
- Dual or single supply operation:
 - 3.3 V core and 3.3 V outputs
 - 3.3 V core and 2.5 V outputs
 - 2.5 V core and 2.5 V outputs
- Pin compatible with MPC940L, MPC9109
- Available in Commercial and Industrial temperature
- 32-pin TQFP package

Functional Description

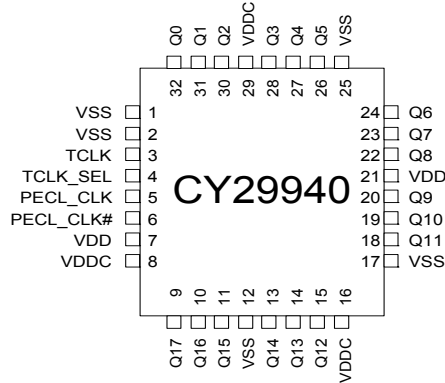
The CY29940 is a low-voltage 200 MHz clock distribution buffer with the capability to select either a differential LVPECL or a LVCMOS/LVTTL compatible input clock. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The eighteen outputs are 2.5 V or 3.3 V LVCMOS/LVTTL compatible and can drive 50 Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:36. Low output-to-output skews make the CY29940 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

For a complete list of related documentation, [click here](#).

Block Diagram



Pin Configuration



Pin Description

Pin	Name	PWR	I/O [1]	Description
5	PECL_CLK		I, PU	PECL input clock
6	PECL_CLK#		I, PD	PECL input clock
3	TCLK		I, PD	External reference/test clock input
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q(17:0)	VDDC	O	Clock outputs
4	TCLK_SEL		I, PD	Clock Select Input. When LOW, PECL clock is selected and when HIGH TCLK is selected.
8, 16, 29	VDDC			3.3 V or 2.5 V power supply for output clock buffers
7, 21	VDD			3.3 V or 2.5 V power supply
1, 2, 12, 17, 25	VSS			Common ground

Note

1. PD = Internal Pull-Down, PU = Internal Pull-up

Maximum Ratings

Exceeding the maximum ratings^[2] may impair the useful life of the device. User guidelines are not tested.

Maximum input voltage relative to V_{SS}	$V_{SS} - 0.3$ V
Maximum input voltage relative to V_{DD}	$V_{DD} + 0.3$ V
Storage temperature	-65 °C to +150 °C
Operating temperature	-40 °C to +85 °C
Maximum ESD protection	2 kV

Maximum power supply 5.5 V

Maximum input current ± 20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters

$V_{DD} = 3.3$ V $\pm 5\%$ or 2.5 V $\pm 5\%$, $V_{DDC} = 3.3$ V $\pm 5\%$ or 2.5 V $\pm 5\%$, $T_A = -40$ °C to +85 °C

Parameter ^[2]	Description	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low voltage		V_{SS}	-	0.8	V
V_{IH}	Input high voltage		2.0	-	V_{DD}	V
I_{IL}	Input low current ^[3]		-	-	-200	μ A
I_{IH}	Input high current ^[3]		-	-	200	μ A
V_{PP}	Peak-to-peak input voltage PECL_CLK		500	-	1000	mV
V_{CMR}	Common mode range ^[4] PECL_CLK	$V_{DD} = 3.3$ V	$V_{DD} - 1.4$	-	$V_{DD} - 0.6$	V
		$V_{DD} = 2.5$ V	$V_{DD} - 1.0$	-	$V_{DD} - 0.6$	V
V_{OL}	Output low voltage ^[5, 6, 7]	$I_{OL} = 20$ mA	-	-	0.5	V
V_{OH}	Output high voltage ^[5, 6, 7]	$I_{OH} = -20$ mA, $V_{DDC} = 3.3$ V	2.4	-	-	V
		$I_{OH} = -20$ mA, $V_{DDC} = 2.5$ V	1.8	-	-	V
I_{DDQ}	Quiescent supply current		-	5	7	mA
I_{DD}	Dynamic supply current	$V_{DD} = 3.3$ V, Outputs at 150 MHz, $C_L = 15$ pF	-	285	-	mA
		$V_{DD} = 3.3$ V, Outputs at 200 MHz, $C_L = 15$ pF	-	335	-	
		$V_{DD} = 2.5$ V, Outputs at 150 MHz, $C_L = 15$ pF	-	200	-	
		$V_{DD} = 2.5$ V, Outputs at 200 MHz, $C_L = 15$ pF	-	240	-	
Z_{out}	Output impedance	$V_{DD} = 3.3$ V	8	12	16	Ω
		$V_{DD} = 2.5$ V	10	15	20	
C_{in}	Input capacitance		-	4	-	pF

Thermal Resistance

Parameter ^[8]	Description	Test Conditions	32-pin TQFP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	67	°C/W
θ_{JC}	Thermal resistance (junction to case)		28	°C/W

Notes

- Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.
- Inputs have pull-up/pull-down resistors that effect input current.
- The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the VCMR range and the input lies within the VPP specification. Driving series or parallel terminated 50 Ω (or 50 Ω to $V_{DD}/2$) transmission lines
- Outputs driving 50 Ω transmission lines.
- See Figure 1 on page 5 and Figure 2 on page 5.
- 50% input duty cycle.
- These parameters are guaranteed by design and are not tested.

AC Parameters^[9]
 $V_{DD} = 3.3\text{ V} \pm 5\%$ or $2.5\text{ V} \pm 5\%$, $V_{DDC} = 3.3\text{ V} \pm 5\%$ or $2.5\text{ V} \pm 5\%$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$

Parameter	Description	Conditions	Min	Typ	Max	Unit	
F_{max}	Input frequency		–	–	200	MHz	
t_{PD}	PECL_CLK to Q Delay ^[10, 11, 12] $\leq 150\text{ MHz}$	$V_{DD} = 3.3\text{ V}, 85\text{ }^\circ\text{C}$	t_{PHL}	2.0	–	3.2	ns
			t_{PLH}	2.1	–	3.4	
		$V_{DD} = 3.3\text{ V}, 70\text{ }^\circ\text{C}$	t_{PHL}	1.9	–	3.1	
			t_{PLH}	2.0	–	3.2	
		$V_{DD} = 2.5\text{ V}, 85\text{ }^\circ\text{C}$	t_{PHL}	2.5	–	5.2	
			t_{PLH}	2.6	–	5	
		$V_{DD} = 2.5\text{ V}, 70\text{ }^\circ\text{C}$	t_{PHL}	2.5	–	5	
			t_{PLH}	2.6	–	5	
t_{PD}	LVCMOS to Q Delay ^[10, 11, 12] $\leq 150\text{ MHz}$	$V_{DD} = 3.3\text{ V}, 85\text{ }^\circ\text{C}$	t_{PHL}	1.9	–	3	ns
			t_{PLH}	2.0	–	3.2	
		$V_{DD} = 3.3\text{ V}, 70\text{ }^\circ\text{C}$	t_{PHL}	1.8	–	2.9	
			t_{PLH}	1.8	–	3.1	
		$V_{DD} = 2.5\text{ V}, 85\text{ }^\circ\text{C}$	t_{PHL}	2.5	–	4	
			t_{PLH}	2.5	–	4	
		$V_{DD} = 2.5\text{ V}, 70\text{ }^\circ\text{C}$	t_{PHL}	2.3	–	3.8	
			t_{PLH}	2.3	–	3.8	
t_J	Total jitter	$V_{DD} = 3.3\text{ V @ }150\text{ MHz}$	–	–	10	ps	
F_{outDC}	Output duty cycle ^[10, 11, 13]	$F_{CLK} < 134\text{ MHz}$	–	–	55	%	
		$F_{CLK} > 134\text{ MHz}$	–	–	60		
T_{skew}	Output-to-output skew ^[10, 11]	$V_{DD} = 3.3\text{ V}$	–	60	150	ps	
		$V_{DD} = 2.5\text{ V}$	–	–	200		
$T_{skew(pp)}$	Part-to-part skew ^[14]	PECL, $V_{DDC} = 3.3\text{ V}$	–	–	1.4	ns	
		PECL, $V_{DDC} = 2.5\text{ V}$	–	–	2.2		
$T_{skew(pp)}$	Part-to-part skew ^[14]	TCLK, $V_{DDC} = 3.3\text{ V}$	–	–	1.2	ns	
		TCLK, $V_{DDC} = 2.5\text{ V}$	–	–	1.7		
$T_{skew(pp)}$	Part-to-part skew ^[15]	PECL_CLK	–	–	850	ps	
		TCLK	–	–	750		
t_R/t_F	Output clocks rise/fall time ^[10, 11]	0.7 V to 2.0 V, $V_{DDC} = 3.3\text{ V}$	0.3	–	1.1	ns	
		0.5 V to 1.8 V, $V_{DDC} = 2.5\text{ V}$	0.3	–	1.2		

Notes

9. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
10. Outputs driving $50\ \Omega$ transmission lines.
11. See [Figure 1 on page 5](#) and [Figure 2 on page 5](#).
12. Parameters tested @ 150 MHz.
13. 50% input duty cycle.
14. Across temperature and voltage ranges, includes output skew.
15. For a specific temperature and voltage, includes output skew.

Figure 1. LVCMOS_CLK CY29940 Test Reference for $V_{CC} = 3.3\text{ V}$ and $V_{CC} = 2.5\text{ V}$

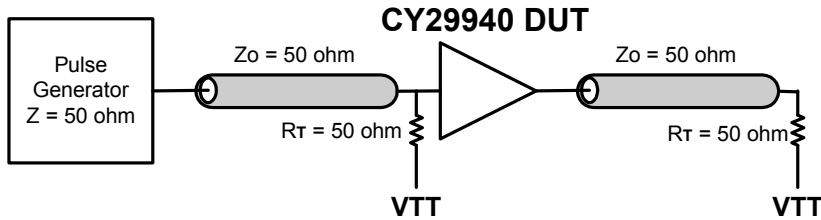


Figure 2. PECL_CLK CY29940 Test Reference for $V_{CC} = 3.3\text{ V}$ and $V_{CC} = 2.5\text{ V}$

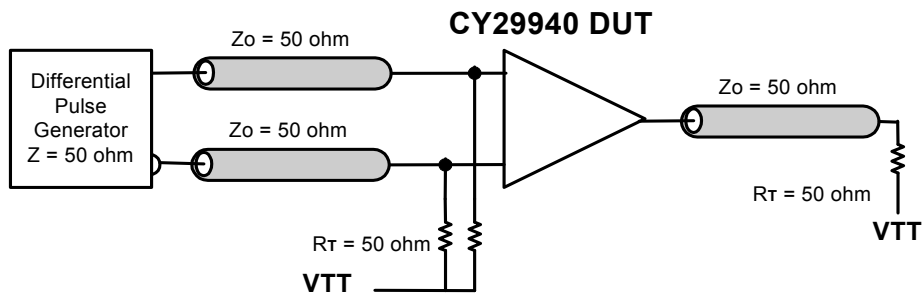


Figure 3. Propagation Delay (TPD) Test Reference

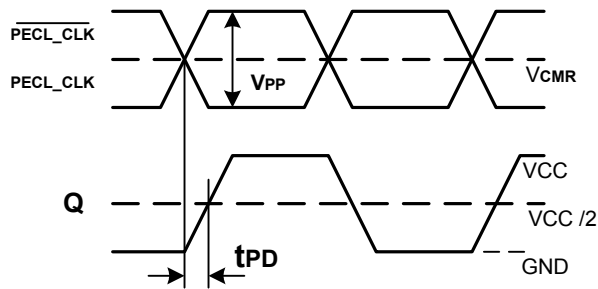


Figure 4. LVCMOS Propagation Delay (TPD) Test Reference

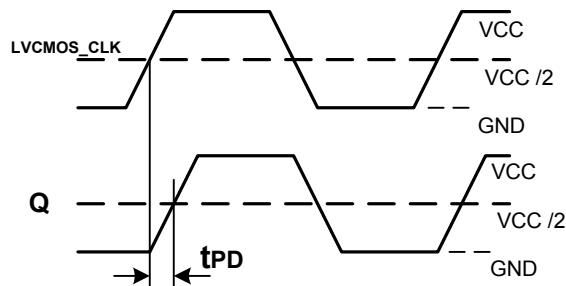


Figure 5. Output Duty Cycle (FoutDC)

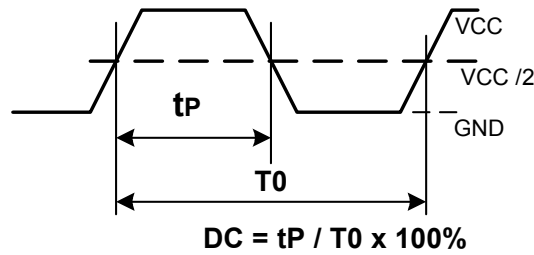
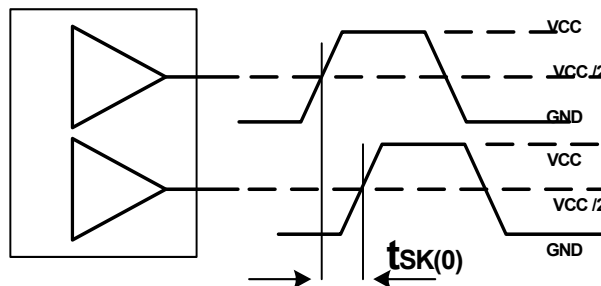


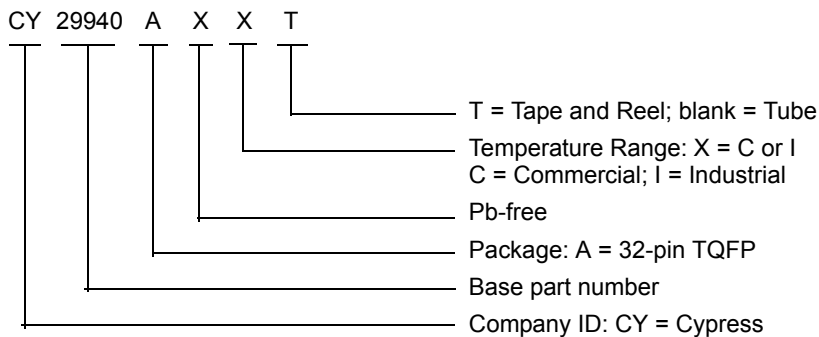
Figure 6. Output-to-Output Skew tsk(0)



Ordering Information

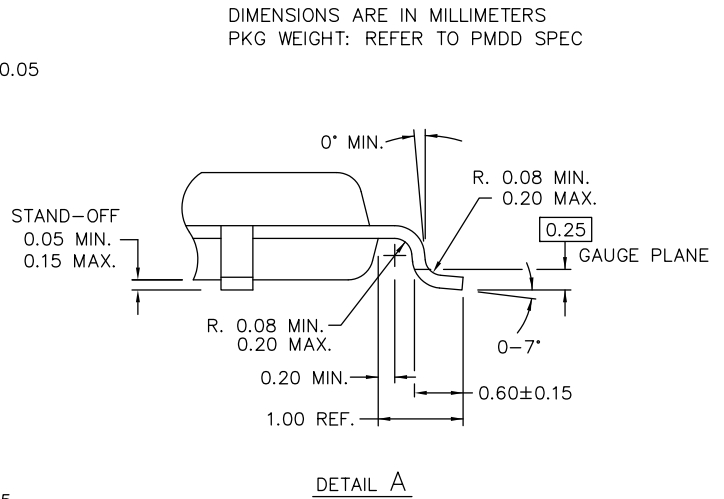
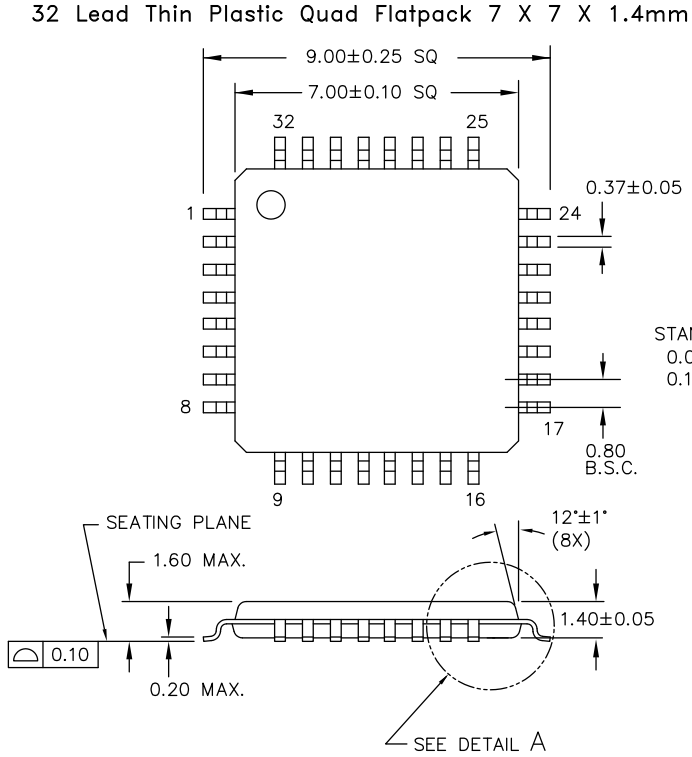
Part Number	Package Type	Production Flow
Pb-free		
CY29940AXI	32-pin TQFP	Industrial, -40 °C to +85 °C
CY29940AXIT	32-pin TQFP – Tape and Reel	Industrial, -40 °C to +85 °C
CY29940AXC	32-pin TQFP	Commercial, 0 °C to 70 °C
CY29940AXCT	32-pin TQFP – Tape and Reel	Commercial, 0 °C to 70 °C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 7. 32-pin TQFP 7 × 7 × 1.4 mm A32.14



51-85088 *E

Acronyms

Acronym	Description
ESD	electrostatic discharge
I/O	input/output
TQFP	thin quad flat package
LVC MOS	low voltage complementary metal oxide semiconductor
LVPECL	low-voltage positive emitter-coupled logic
LVTTTL	low-voltage transistor-transistor logic
TQFP	thin quad flat pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kV	kilo Volts
MHz	Mega Hertz
μA	micro Amperes
mA	milli Amperes
mm	milli meter
mV	milli Volts
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
ps	pico seconds
V	Volts
W	Watts

Document History Page

Document Title: CY29940, 2.5 V or 3.3 V, 200 MHz, 1:18 Clock Distribution Buffer				
Document Number: 38-07283				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	111094	02/01/02	BRK	New data sheet
*A	116776	08/15/02	HWT	Incorporate results of final characterization using corporate methods, added output impedance on page 3 and added output duty cycle on page 4. Updated Ordering Information : Add commercial temperature range part numbers.
*B	122875	12/21/02	RBI	Add power up requirements to maximum rating information
*C	448379	See ECN	RGL	Add typical value for output-to-output skew Updated Ordering Information : Added Lead-free devices.
*D	2899304	03/25/10	BASH / KVM	Updated Ordering Information : Removed inactive parts. Updated Package Drawing and Dimensions .
*E	3254185	05/11/2011	CXQ	Added Ordering Code Definitions . Added Acronyms and Units of Measure . Updated to new template.
*F	3548252	03/12/2012	PURU	Changed LQFP to TQFP throughout document.
*G	4586288	12/03/2014	PURU	Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end. Updated Package Drawing and Dimensions : Updated Figure 7 (spec 51-85088 – Changed revision from *D to *E).
*H	4787038	06/04/2015	TAVA	Updated to new template. Completing Sunset Review.
*I	5258862	05/04/2016	PSR	Added Thermal Resistance . Updated to new template. Completing Sunset Review.
*J	5973872	11/22/2017	AESATMP8	Updated logo and Copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM [®] Cortex [®] Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC[®] Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2002-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.