

# Freescale Semiconductor Addendum

Document Number: QFN\_Addendum

Rev. 0, 07/2014

# Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.





Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D



## **Freescale Semiconductor**

Data Sheet: Technical Data

An Energy Efficient Solution by Freescale

Document Number: MC9S08QB8 Rev. 3, 3/2009





16-Pin TSSOP Case 948F



24 QFN Case 1982-01

## MC9S08QB8 Series

Covers: MC9S08QB8 and MC9S08QB4

#### Features

- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 20 MHz CPU at 3.6 V to 1.8 V across temperature range of -40 °C to 85 °C
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- · On-Chip Memory
  - Up to 8 KB flash memory read/program/erase over full operating voltage and temperature
  - Up to 512 bytes random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- · Power-Saving Modes
  - Two very low power stop modes
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
  - Low power run
  - Low power wait
  - 6 μs typical wakeup time from stop3 mode
  - Typical stop current of 250 nA at 3 V, 25 °C
- Clock Source Options
  - Oscillator (XOSC) Very low-power, loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1 MHz to 10 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash block protection

Development Support

28 SOIC

Case 751F

- Single-wire background debug interface
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- Peripherals
  - ADC 8-channel, 12-bit resolution; 2.5 μs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V.
  - **ACMP** Analog comparator with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; output can be tied internally to TPM input capture; operation in stop3
  - **TPM** One 1-channel timer/pulse-width modulator (TPM) module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel; ACMP output can be tied internally to input capture
  - MTIM 8-bit modulo timer module with optional prescaler
  - **RTC** (Real-time counter) 8-bit modulo counter with binary or decimal based prescaler; external clock source for precise time base, time-of-day, calendar or task scheduling functions; free running on-chip low power oscillator (1 kHz) for cyclic wakeup without external components; runs in all MCU modes
  - **SCI** Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wakeup on active edge
  - **KBI** 8-pin keyboard interrupt with selectable edge and level detection modes
- Input/Output
  - 22 GPIOs and one input-only and one output-only pin.
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins except PTA5.
- Package Options
  - 28-pin SOIC, 24-pin QFN, 16-pin TSSOP

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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## **Revision History**

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
1	10/22/2008	Initial public released.
2	12/17/2008	Completed all the TBDs in Table 8.
3	3/6/2009	Corrected the 24-pin QFN package information. Changed $V_{DDAD}$ and $V_{SSAD}$ to $V_{DDA}$ and $V_{SSA}$ separatedly. In Table 7, updated the $II_{In}I$ , $II_{OZ}I$ and added $II_{OZTOT}I$ . In Table 11, updated the DCO output frequency range-trimmed, and updated some of the symbols.

## **Related Documentation**

Find the most current versions of all documents at: http://www.freescale.com

#### Reference Manual (MC9S08QB8RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.



#### **MCU Block Diagram** 1

The block diagram shows the structure of the MC9S08QB8 MCU.

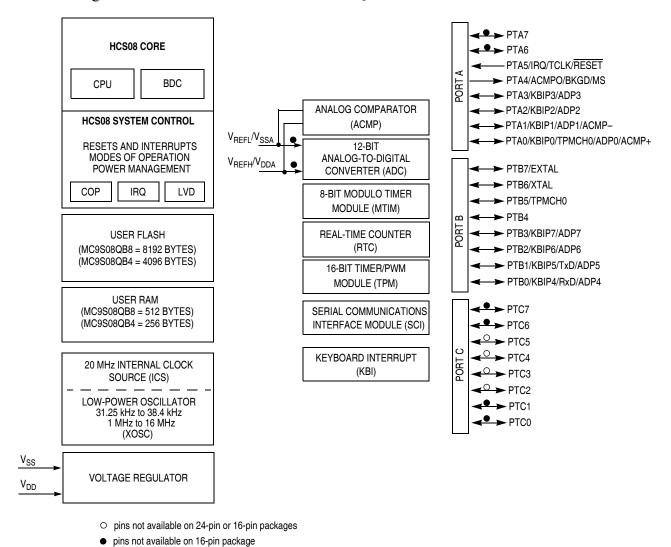


Figure 1. MC9S08QB8 Series Block Diagram

 $^{1}$   $\,$  V  $_{\rm DDA}$  /V  $_{\rm REFH}$  and V  $_{\rm SSA}$  /V  $_{\rm REFL}$  are double bonded to V  $_{\rm DD}$  and V  $_{\rm SS}$  respectively in 16-pin package.

MC9S08QB8 Series MCU Data Sheet, Rev. 3 Freescale Semiconductor 3



## **Pin Assignments**

## 2 Pin Assignments

This chapter shows the pin assignments for the MC9S08QB8 series devices.

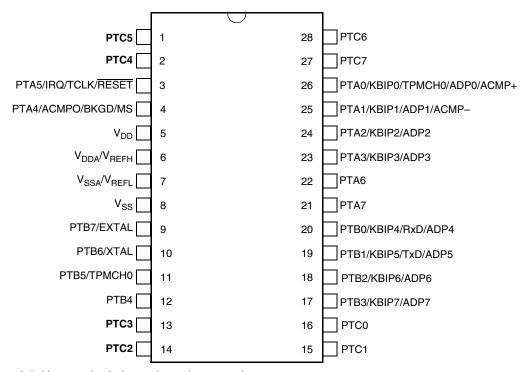
Table 1. Pin Availability by Package Pin-Count

Pir	n Num	ber		< Lowes	t <b>Priority</b>	> Highest	
28	24	16	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	_		PTC5				
2	_	_	PTC4				
3	23	1	PTA5	IRQ	TCLK	RESET	
4	24	2	PTA4	ACMPO	BKGD	MS	
5	1	3					$V_{DD}$
6	2	1					$V_{\rm DDA}/V_{\rm REFH}$
7	3	l					V <sub>SSA</sub> /V <sub>REFL</sub>
8	4	4					$V_{SS}$
9	5	5	PTB7				EXTAL
10	6	6	PTB6				XTAL
11	7	7	PTB5	TPMCH0 <sup>1</sup>			
12	8	8	PTB4				
13	_	-	PTC3				
14	_	-	PTC2				
15	9	l	PTC1				
16	10		PTC0				
17	11	9	PTB3	KBIP7		ADP7	
18	12	10	PTB2	KBIP6		ADP6	
19	13	11	PTB1	KBIP5	TxD	ADP5	
20	14	12	PTB0	KBIP4	RxD	ADP4	
21	15	_	PTA7				
22	16		PTA6				
23	17	13	PTA3	KBIP3		ADP3	
24	18	14	PTA2	KBIP2		ADP2	
25	19	15	PTA1	KBIP1		ADP1 <sup>2</sup>	ACMP-2
26	20	16	PTA0	KBIP0	TPMCH0	ADP0 <sup>2</sup>	ACMP+ <sup>2</sup>
27	21	_	PTC7				
28	22		PTC6				

<sup>&</sup>lt;sup>1</sup> TPMCH0 pin can be repositioned using at PTB5 TPMCH0PS in SOPT2, default reset location is PTA0.

 $<sup>^{2}\,\,</sup>$  If ADC and ACMP are enabled, both modules will have access to the pin.



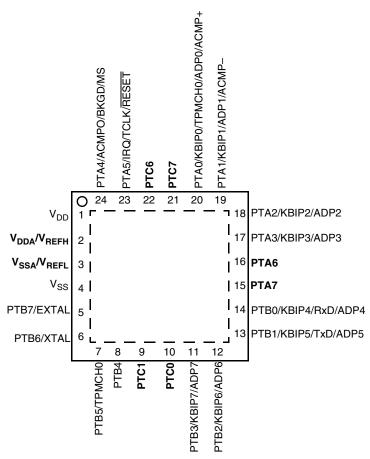


Pins shown in bold type are lost in the next lower pin count package.

Figure 2. MC9S08QB8 Series in 28-Pin SOIC Package



#### **Pin Assignments**



Pins shown in bold type are lost in the next lower pin count package.

Figure 3. MC9S08QB8 Series in 24-Pin QFN Packages

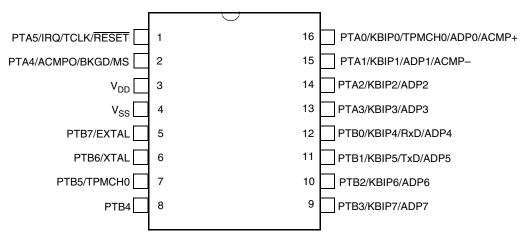


Figure 4. MC9S08QB8 Series in 16-Pin TSSOP Package



## 3.1 Introduction

This chapter contains electrical and timing specifications for the MC9S08QB8 series of microcontrollers available at the time of publication.

## 3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table 2. Parameter Classifications** 

Р	Those parameters are guaranteed during production testing on each individual device.
С	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
Т	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

#### NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

## 3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either  $V_{SS}$  or  $V_{DD}$ ) or the programmable pull-up resistor associated with the pin is enabled.

**Table 3. Absolute Maximum Ratings** 

Rating	Symbol	Value	Unit
Supply voltage	$V_{DD}$	-0.3 to 3.8	V
Maximum current into V <sub>DD</sub>	I <sub>DD</sub>	120	mA
Digital input voltage	V <sub>In</sub>	$-0.3$ to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) <sup>1, 2, 3</sup>	I <sub>D</sub>	±25	mA
Storage temperature range	T <sub>stg</sub>	-55 to 150	°C

Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V<sub>DD</sub>) and negative (V<sub>SS</sub>) clamp voltages, then use the larger of the two resistance values.

## 3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take  $P_{I/O}$  into account in power calculations, determine the difference between actual pin voltage and  $V_{SS}$  or  $V_{DD}$  and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and  $V_{SS}$  or  $V_{DD}$  will be very small.

**Table 4. Thermal Characteristics** 

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T <sub>A</sub>	T <sub>L</sub> to T <sub>H</sub> -40 to 85	°C
Maximum junction temperature	T <sub>JM</sub>	95	°C
Thermal resistance 28-pin SOIC		70	°C/W
Thermal resistance 24-pin QFN	$\theta_{\sf JA}$	92	°C/W
Thermal resistance 16-pin TSSOP		129	°C/W

The average chip-junction temperature  $(T_I)$  in  ${}^{\circ}C$  can be obtained from:

$$T_{J} = T_{A} + (P_{D} \times \theta_{JA})$$
 Eqn. 1

where:

 $<sup>^2~</sup>$  All functional non-supply pins, except for PTA5 are internally clamped to  $\rm V_{SS}$  and  $\rm V_{DD}$ 

Power supply must maintain regulation within operating V<sub>DD</sub> range during instantaneous and operating maximum current conditions. If positive injection current (V<sub>In</sub> > V<sub>DD</sub>) is greater than I<sub>DD</sub>, the injection current may flow out of V<sub>DD</sub> and could result in external power supply going out of regulation. Ensure external V<sub>DD</sub> load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).



 $T_A = Ambient temperature, °C$ 

 $\theta_{IA}$  = Package thermal resistance, junction-to-ambient, °C/W

 $P_{\rm D} = P_{\rm int} + P_{\rm I/O}$ 

 $P_{int} = I_{DD} \times V_{DD}$ , Watts — chip internal power

 $P_{I/O}$  = Power dissipation on input and output pins — user determined

For most applications,  $P_{I/O} \ll P_{int}$  and can be neglected. An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is:

$$P_D = K \div (T_A + 273^{\circ}C)$$
 Eqn. 2

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273^{\circ}C) + \theta_{JA} \times (P_D)^2$$
 Eqn. 3

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving Equation 1 and Equation 2 iteratively for any value of  $T_A$ .

## 3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Model	Description	Symbol	Value	Unit
	Series resistance	R1	1500	Ω
Human Body	Storage capacitance	С	100	pF
,	Number of pulses per pin	_	1500 100 1 3 0	
	Series resistance	R1	0	Ω
Machine	Storage capacitance	С	200	pF
	Number of pulses per pin	_	3	
Lotab up	Minimum input voltage limit		-2.5	V
Latch-up	Maximum input voltage limit		7.5	V

Table 5. ESD and Latch-up Test Conditions



**Table 6. ESD and Latch-Up Protection Characteristics** 

No.	Rating <sup>1</sup>	Symbol	Min	Max	Unit
1	Human body model (HBM)	$V_{HBM}$	±2000	_	V
2	Charge device model (CDM)	V <sub>CDM</sub>	±500	_	V
3	Latch-up current at T <sub>A</sub> = 85°C	I <sub>LAT</sub>	±100	_	mA

Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

## 3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

**Table 7. DC Characteristics** 

Num	С	C	Characteristic	Symbol	ymbol Condition		Typical <sup>1</sup>	Max	Unit	
1	Р	Operating Vol	tage	$V_{DD}$	_	1.8	_	3.6	V	
	С		All I/O pins, low-drive strength		$V_{DD} > 1.8 \text{ V},$ $I_{Load} = -2 \text{ mA}$	V <sub>DD</sub> - 0.5	_	_		
2	Р	Output high voltage	All I/O pins,	V <sub>OH</sub>	$V_{DD} > 2.7 \text{ V},$ $I_{Load} = -10 \text{ mA}$	V <sub>DD</sub> - 0.5	_	_	٧	
	С		high-drive strength		$V_{DD} > 1.8V$ , $I_{Load} = -2 \text{ mA}$	V <sub>DD</sub> - 0.5	_	_		
3	D	Output high current	Max total I <sub>OH</sub> for all ports	I <sub>OHT</sub>	V <sub>OUT</sub> < V <sub>DD</sub>	0	_	-80	mA	
	С		All I/O pins, low-drive strength		$V_{DD} > 1.8 \text{ V},$ $I_{Load} = 0.6 \text{ mA}$	_	_	0.5		
4	Р	Output low voltage	All I/O pins,	V <sub>OL</sub>	V <sub>OL</sub>	$V_{DD} > 2.7 \text{ V},$ $I_{Load} = 10 \text{ mA}$	_	_	0.5	٧
	С		high-drive strength		$V_{DD} > 1.8 \text{ V},$ $I_{Load} = 3 \text{ mA}$	_	_	0.5		
5	D	Output low current	Max total I <sub>OL</sub> for all ports	I <sub>OLT</sub>	V <sub>OUT</sub> > V <sub>SS</sub>	0	_	80	mA	
6	Р	Input high	all digital inputs	V <sub>IH</sub>	V <sub>DD</sub> > 2.7 V	0.70 x V <sub>DD</sub>	_	_		
	С	voltage	an digital inputs	V IH	V <sub>DD</sub> > 1.8 V	0.85 x V <sub>DD</sub>	_	_	v	
7	Р	Input low	all digital inputs	V <sub>IL</sub>	V <sub>DD</sub> > 2.7 V	_	_	0.35 x V <sub>DD</sub>	<b>'</b>	
'	С	voltage	an digital inputs	VIL.	V <sub>DD</sub> > 1.8 V	_	_	0.30 x V <sub>DD</sub>		
8	С	Input hysteresis	all digital inputs	V <sub>hys</sub>	_	0.06 x V <sub>DD</sub>	_	_	mV	
9	Р	Input leakage current	all input only pins (Per pin)	II <sub>In</sub> I	$V_{In} = V_{DD}$ or $V_{SS}$	_	_	200	nA	
10	Р	Hi-Z (off-state) leakage current	all input/output (per pin)	ll <sub>OZ</sub> l	$V_{In} = V_{DD}$ or $V_{SS}$	_	_	200	nA	

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#### **Table 7. DC Characteristics (continued)**

Num	С	(	Characteristic	Symbol	Condition	Min	Typical <sup>1</sup>	Max	Unit
10	С	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	II <sub>OZTOT</sub> I	$V_{In} = V_{DD}$ or $V_{SS}$	_	_	2	μА
11	Р	Pullup, Pulldown resistors	all digital inputs except PTA5/IRQ/TCLK/RESET, when enabled	n <sub>PU,</sub>	_	17.5	_	52.5	kΩ
12	С	Pullup, Pulldown resistors	PTA5/IRQ/TCLK/RESET, when enabled <sup>2</sup>	R <sub>PU,</sub> R <sub>PD</sub>	_	17.5	_	52.5	kΩ
	D	DC injection Single pin limit  Current 3, 4,  Total MCU limit, includes sum of all stressed pins			-0.2	_	0.2	mA	
13			· ·	I <sub>IC</sub>	$V_{IN} < V_{SS}, V_{IN} > V_{DD}$	<b>–</b> 5	_	5	mA
14	С	Input Capacit	ance, all pins	C <sub>In</sub>	_	_	_	8	pF
15	С	RAM retentio	n voltage	$V_{RAM}$	_	_	0.6	1.0	V
16	С	POR re-arm	voltage <sup>6</sup>	$V_{POR}$	_	0.9	1.4	2.0	V
17	D	POR re-arm	time	t <sub>POR</sub>	_	10	_	_	μS
18	Р	Low-voltage detection threshold		V <sub>LVD</sub>	V <sub>DD</sub> falling V <sub>DD</sub> rising	1.80 1.88	1.84 1.92	1.88 1.96	V
19	Р	Low-voltage warning threshold		$V_{LVW}$	V <sub>DD</sub> falling V <sub>DD</sub> rising	2.08	2.14	2.26	V
20	С	Low-voltage inhibit reset/recover hysteresis		V <sub>hys</sub>	_	_	80	_	mV
21	Р	Bandgap Volt	tage Reference <sup>7</sup>	$V_{BG}$	_	1.15	1.17	1.18	V

<sup>1</sup> Typical values are measured at 25 °C. Characterized, not tested

<sup>&</sup>lt;sup>2</sup> The specified resistor value is the actual value internal to the device. The pullup or pulldown value may appear lower when measured externally on the pin.

 $<sup>^3</sup>$  All functional non-supply pins, except for PTA5 are internally clamped to  $V_{SS}$  and  $V_{DD}$ .

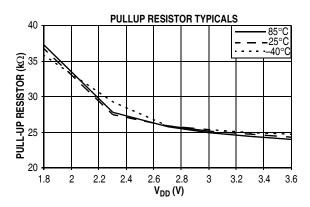
<sup>&</sup>lt;sup>4</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

Power supply must maintain regulation within operating V<sub>DD</sub> range during instantaneous and operating maximum current conditions. If the positive injection current (V<sub>In</sub> > V<sub>DD</sub>) is greater than I<sub>DD</sub>, the injection current may flow out of V<sub>DD</sub> and could result in external power supply going out of regulation. Ensure that external V<sub>DD</sub> load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

<sup>&</sup>lt;sup>6</sup> Maximum is highest voltage that POR is guaranteed.

<sup>&</sup>lt;sup>7</sup> Factory trimmed at  $V_{DD} = 3.0 \text{ V}$ , Temp = 25 °C





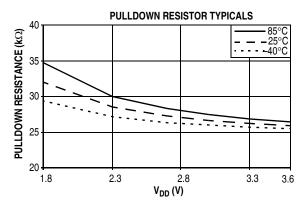
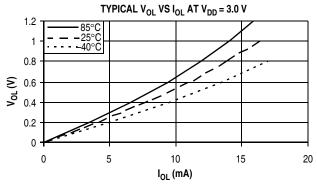


Figure 5. Pullup and Pulldown Typical Resistor Values ( $V_{DD} = 3.0 \text{ V}$ )



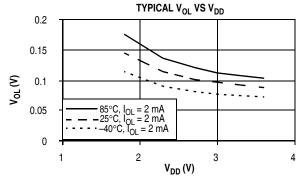
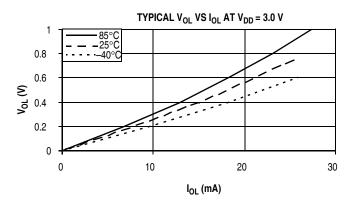


Figure 6. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)



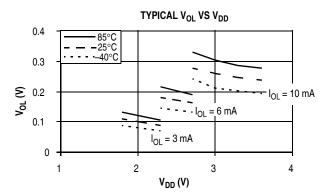


Figure 7. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

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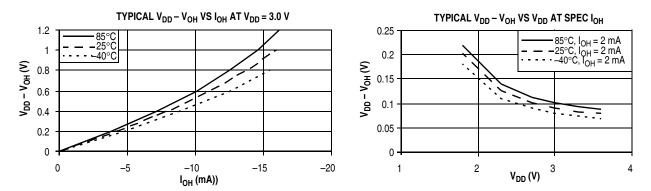


Figure 8. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

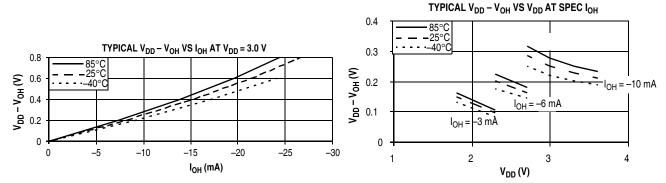


Figure 9. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

## 3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.



**Table 8. Supply Current Characteristics** 

Num	С	Parameter	Symbol	Bus Freq	V <sub>DD</sub> (V)	Typical <sup>1</sup>	Max	Unit	Temp (°C)		
1	Р	Run supply current	RI <sub>DD</sub>	10 MHz	_	5.60	6	mA	–40 to 85°C		
'	Т	FEI mode, all modules on	ı ııDD	1 MHz	3	0.80	_	1117	-40 to 65 C		
2	Т	Run supply current	RI <sub>DD</sub>	10 MHz		3.60	_	mA	–40 to 85°C		
	Т	FEI mode, all modules off	טטיי י	1 MHz	3	0.75	1	ША	- <del>1</del> 0 to 05 O		
3	Т	Run supply current LPRS=0, all modules off	RI <sub>DD</sub>	16 kHz FBILP	3	165		μA	–40 to 85°C		
3	Т		NIDD	16 kHz FBELP	3	105	_	μΑ	-40 to 65 C		
4	Т	Run supply current LPRS=1, all modules off	RI <sub>DD</sub>	16 kHz FBELP	3	7.3	_	μА	–40 to 85°C		
5	Т	Wait mode supply current	WI <sub>DD</sub>	10 MHz	3	570	_	μΑ	–40 to 85°C		
3	Т	FEI mode, all modules off	VVIDD	1 MHz		290	_	μΑ	-40 to 65 C		
6	Т	Wait mode supply current LPRS = 1, all mods off	WI <sub>DD</sub>	16 kHz FBELP	3	1	_	μА	-40 to 85°C		
	Р		631	_	3		0.2	0.25	0.65		–40 to 25°C
	С			_		0.5	0.8		70°C		
7	Р	Stop2 mode supply current		_		1	2	μΑ	85°C		
,	С	Stop2 mode supply current	S2I <sub>DD</sub>	1		0.2	0.5	μΑ	–40 to 25°C		
	С			1	2	0.3	0.6		70°C		
	С			1		0.7	1.6		85°C		
	Р					0.45	0.80		–40 to 25°C		
	С	Stop3 mode supply current			3	1	1.8		70°C		
8	Р		S3I <sub>DD</sub>			3	5.8	μА	85°C		
	С	no clocks active	DD. DD	_			0.3	0.6	μ	–40 to 25°C	
	С			_	2	0.8	1.5		70°C		
	С		-	_		2.5	5.0		85°C		

Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

## **Table 9. Stop Mode Adders**

Num	C Parameter	Condition			Units			
Italii		i arameter	Condition	<b>-40</b> °C	<b>25</b> °C	<b>70</b> °C	<b>85</b> °C	Omis
1	T	LPO	_	50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN <sup>1</sup>	_	63	70	77	81	μА

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**Table 9. Stop Mode Adders (continued)** 

Num	_	C Parameter	Condition			Units		
IVUIII		raiametei	Condition	<b>-40</b> °C	<b>25</b> °C	<b>70</b> °C	<b>85</b> °C	Office
4	Т	RTC	Does not include clock source current	50	75	100	150	nA
5	T	LVD <sup>1</sup>	LVDSE = 1	90	100	110	115	μΑ
6	T	ACMP <sup>1</sup>	Not using the bandgap (BGBE = 0)	18	20	22	23	μΑ
7	Т	ADC <sup>1</sup>	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	106	114	120	μΑ

<sup>&</sup>lt;sup>1</sup> Not available in stop2 mode.

## 3.8 External Oscillator (XOSC) Characteristics

Reference Figure 10 and Figure 11 for crystal or resonator circuits.

Table 10. XOSCVLP and ICS Specifications (Temperature Range = −40 to 85°C Ambient)

Num	С	Characteristic	Symbol	Min	Typ <sup>1</sup>	Max	Unit
1	С	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	f <sub>lo</sub> f <sub>hi</sub> f <sub>hi</sub>	32 1 1		38.4 16 8	kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C <sub>1,</sub> C <sub>2</sub>		See No		
3	D	Feedback resistor Low range, low power (RANGE = 0, HGO = 0) <sup>2</sup> Low range, high gain (RANGE = 0, HGO = 1) High range (RANGE = 1, HGO = X)	R <sub>F</sub>		— 10 1		МΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0) <sup>2</sup> Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R <sub>S</sub>				kΩ
5	С	Crystal start-up time <sup>4</sup> Low range, low power Low range, high gain High range, low power High range, high gain	t CSTL t CSTH	_ _ _ _	600 400 5 15	_ _ _ _	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f <sub>extal</sub>	0.03125 0	_ _	20 20	MHz



- <sup>1</sup> Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.
- <sup>2</sup> Load capacitors (C<sub>1</sub> C<sub>2</sub>), feedback resistor (R<sub>F</sub>) and series resistor (R<sub>S</sub>) are incorporated internally when RANGE = HGO = 0.
- <sup>3</sup> See crystal or resonator manufacturer's recommendation.
- <sup>4</sup> Proper PC board layout procedures must be followed to achieve specifications.

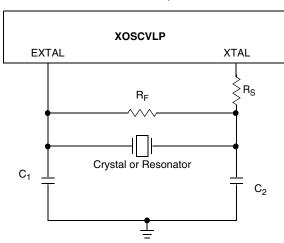


Figure 10. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

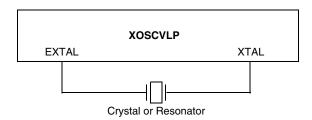


Figure 11. Typical Crystal or Resonator Circuit: Low Range/Low Power

## 3.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = -40 to 85°C Ambient)

Num	С	Charac	Symbol	Min.	Typical <sup>1</sup>	Max.	Unit	
1	Р	Average internal reference freq at V <sub>DD</sub> = 3.6 V and temperature	f <sub>int_t</sub>		32.768		kHz	
2	Р	Internal reference frequency —	user trimmed	f <sub>int_ut</sub>	31.25	_	39.06	kHz
3	Т	Internal reference start-up time		t <sub>IRST</sub>	_	60	100	μS
4		DCO output frequency range — trimmed <sup>2</sup>	Low range (DRS = 00)	f <sub>dco_t</sub>	16	_	20	MHz
5	Р	DCO output frequency <sup>2</sup> Reference = 32768 Hz and DM	CO output frequency <sup>2</sup> eference = 32768 Hz and DMX32 = 1			19.92	_	MHz
6		Resolution of trimmed DCO out and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$		±0.1	±0.2	%f <sub>dco</sub>



Table 11	ICS Fraguency	Specifications	/Tomporature Dan	ao - 40 to 85	°C Ambiant)	(continued)
Table 11	. ICS Frequency	Specifications	(Temperature Ran	ae = -4u to 85	C Ambienti	(continuea)

Num	С	Characteristic	Symbol	Min.	Typical <sup>1</sup>	Max.	Unit
7	С	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	_	± 0.2	± 0.4	%f <sub>dco</sub>
8	С	Total deviation of DCO output from trimmed frequency <sup>3</sup> Over full voltage and temperature range Over fixed voltage and temperature range of 0 to 70 °C	Δf <sub>dco_t</sub>	_	-1.0 to 0.5 ±0.5	± 2 ± 1	%f <sub>dco</sub>
10	С	FLL acquisition time <sup>4</sup>	t <sub>Acquire</sub>	_	_	1	ms
11	С	Long term jitter of DCO output clock (averaged over 2-ms interval) <sup>5</sup>	C <sub>Jitter</sub>	_	0.02	0.2	%f <sub>dco</sub>

Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f<sub>Bus</sub>. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V<sub>DD</sub> and V<sub>SS</sub> and variation in crystal oscillator frequency increase the C<sub>Jitter</sub> percentage for a given interval.

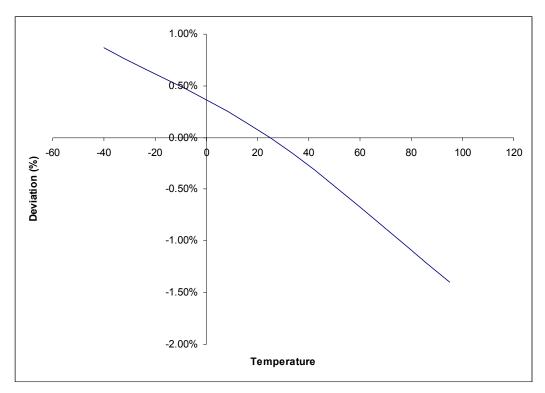


Figure 12. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

<sup>&</sup>lt;sup>2</sup> The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

<sup>&</sup>lt;sup>3</sup> This parameter is characterized and not tested on each device.

This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.



## 3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

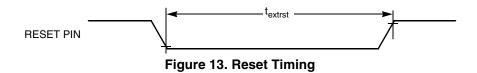
## 3.10.1 Control Timing

**Table 12. Control Timing** 

Num	С	Rating	Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	D	Bus frequency (t <sub>cyc</sub> = 1/f <sub>Bus</sub> )	f <sub>Bus</sub>	DC	_	10	MHz
2	D	Internal low power oscillator period	t <sub>LPO</sub>	700	_	1300	μS
3	D	External reset pulse width <sup>2</sup>	t <sub>extrst</sub>	100	_	_	ns
4	D	Reset low drive	t <sub>rstdrv</sub>	34 x t <sub>cyc</sub>	_	_	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t <sub>MSSU</sub>	500	_	_	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes <sup>3</sup>	t <sub>MSH</sub>	100	_	_	μS
7	D	IRQ pulse width Asynchronous path <sup>2</sup> Synchronous path <sup>4</sup>	t <sub>ILIH,</sub> t <sub>IHIL</sub>	100 1.5 x t <sub>cyc</sub>		_	ns
8	D	Keyboard interrupt pulse width Asynchronous path <sup>2</sup> Synchronous path <sup>4</sup>	t <sub>ILIH</sub> , t <sub>IHIL</sub>	100 1.5 x t <sub>cyc</sub>		_	ns
9	D	Port rise and fall time —  Low output drive (PTxDS = 0) (load = 50 pF) <sup>5</sup> Slew rate control disabled (PTxSE = 0)  Slew rate control enabled (PTxSE = 1)	t <sub>Rise</sub> , t <sub>Fall</sub>		16 23	_ _	ns
9		Port rise and fall time —  High output drive (PTxDS = 1) (load = 50 pF) <sup>5</sup> Slew rate control disabled (PTxSE = 0)  Slew rate control enabled (PTxSE = 1)	t <sub>Rise</sub> , t <sub>Fall</sub>		5 9	_ _	ns
10	D	Voltage regulator recovery time	t <sub>VRR</sub>	_	4	_	μS

Typical values are based on characterization data at V<sub>DD</sub> = 3.0 V, 25 °C unless otherwise stated.

 $<sup>^5</sup>$  Timing is shown with respect to 20%  $\rm V_{DD}$  and 80%  $\rm V_{DD}$  levels. Temperature range  $-40^{\circ}\rm C$  to 85°C.



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<sup>&</sup>lt;sup>2</sup> This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

<sup>&</sup>lt;sup>3</sup> To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t<sub>MSH</sub> after V<sub>DD</sub> rises above V<sub>LVD</sub>.

<sup>&</sup>lt;sup>4</sup> This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.



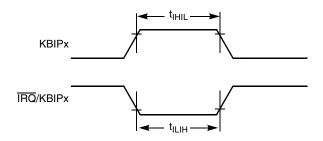


Figure 14. IRQ/KBIPx Timing

## 3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

No.	С	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f <sub>TEXT</sub>	DC	1/4 f <sub>op</sub>	MHz
2	D	External clock period	t <sub>TEXT</sub>	4	_	t <sub>CYC</sub>
3	D	External clock high time	t <sub>TCLKH</sub>	1.5	_	t <sub>CYC</sub>
4	D	External clock low time	t <sub>TCLKL</sub>	1.5	_	t <sub>CYC</sub>
5	D	Input capture pulse width	f <sub>ICPW</sub>	1.5	_	t <sub>CYC</sub>

**Table 13. TPM Input Timing** 

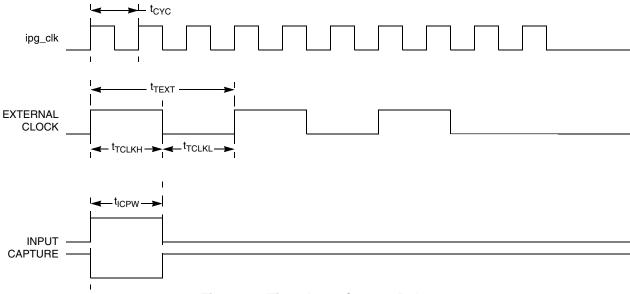


Figure 15. Timer Input Capture Pulse



## 3.11 Analog Comparator (ACMP) Electricals

**Table 14. Analog Comparator Electrical Specifications** 

С	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V <sub>PWR</sub>	1.8	_	3.6	V
D	Supply current (active)	I <sub>DDAC</sub>	_	20	35	μА
D	Analog input voltage	V <sub>AIN</sub>	$V_{SS} - 0.3$	_	$V_{DD}$	V
Р	Analog input offset voltage	V <sub>AIO</sub>	_	20	40	mV
С	Analog comparator hysteresis	V <sub>H</sub>	3.0	9.0	15.0	mV
Р	Analog input leakage current	I <sub>ALKG</sub>	_	_	1.0	μΑ
С	Analog comparator initialization delay	t <sub>AINIT</sub>	_		1.0	μS

## 3.12 ADC Characteristics

**Table 15. 12-Bit ADC Operating Conditions** 

			ı		ı		
Characteristic	Conditions	Symbol	Min	Typical <sup>1</sup>	Max	Unit	Comment
	Absolute	$V_{DDA}$	1.8	_	3.6	V	
Supply voltage	Delta to V <sub>DD</sub> (V <sub>DD</sub> – V <sub>DDA</sub> ) <sup>2</sup>	ΔV <sub>DDA</sub>	-100	0	100	mV	
Ground voltage	Delta to V <sub>SS</sub> (V <sub>SS</sub> – V <sub>SSA</sub> ) <sup>2</sup>	ΔV <sub>SSA</sub>	-100	0	100	mV	
Supply Current	Stop, Reset, Module Off	I <sub>DDAD</sub>	_	0.007	0.8	μΑ	
Input Voltage		V <sub>ADIN</sub>	V <sub>REFL</sub>	_	V <sub>REFH</sub>	V	
Input Capacitance		C <sub>ADIN</sub>	_	4.5	5.5	pF	
Input Resistance		R <sub>ADIN</sub>	_	5	7	kΩ	
	12 bit mode f <sub>ADCK</sub> > 4MHz f <sub>ADCK</sub> < 4MHz			_ _	2 5		
Analog Source Resistance	10 bit mode $f_{ADCK} > 4MHz$ $f_{ADCK} < 4MHz$	R <sub>AS</sub>	_		5 10	kΩ	External to MCU
	8 bit mode (all valid f <sub>ADCK</sub> )		_	_	10		
ADC	High Speed (ADLPC = 0)		0.4	_	8.0		
Conversion Clock Freq.	Low Power (ADLPC = 1)	f <sub>ADCK</sub>	0.4	_	4.0	MHz	

Typical values assume  $V_{DDA} = 3.0 \text{ V}$ , Temp = 25 °C,  $f_{ADCK} = 1.0 \text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.

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<sup>&</sup>lt;sup>2</sup> DC potential difference.



## **NOTE**

 $V_{DDA}/V_{SSA}$  pins do not exist in 16-pin package. The signals are derived internally by double bonding to  $V_{DD}/V_{SS}$  pair of pins.

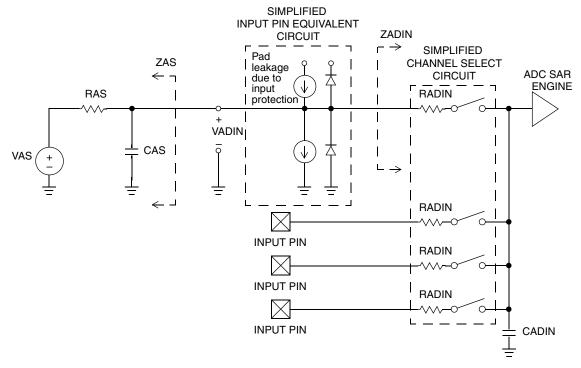


Figure 16. ADC Input Impedance Equivalency Diagram



Table 16. 12-Bit ADC Characteristics ( $V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}$ )

Characteristic	Conditions	С	Symbol	Min	Typical <sup>1</sup>	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1		Т	I <sub>DDAD</sub>	_	120	_	μА	
Supply Current ADLPC=1 ADLSMP=0 ADCO=1		Т	I <sub>DDAD</sub>	_	202	_	μА	
Supply Current ADLPC=0 ADLSMP=1 ADCO=1		Т	I <sub>DDAD</sub>		288		μА	
Supply Current ADLPC=0 ADLSMP=0 ADCO=1		Т	I <sub>DDAD</sub>	_	0.532	1	mA	
Supply Current	Stop, Reset, Module Off	Т	I <sub>DDAD</sub>	_	0.007	0.8	μА	
ADC	High Speed (ADLPC = 0)	_		2	3.3	5	NAL 1-	t <sub>ADACK</sub> =
Asynchronous Clock Source	Low Power (ADLPC = 1)	P	f <sub>ADACK</sub>	1.25	2	3.3	MHz	1/f <sub>ADACK</sub>
Conversion Time (Including	Short Sample (ADLSMP = 0)	т	t <sub>ADC</sub>	_	20	_	ADCK	
sample time)	Long Sample (ADLSMP = 1)	•	ADC	I	40	I	cycles	See reference manual for
Sample Time	Short Sample (ADLSMP = 0)	_ T	+	_	3.5	_	ADCK	conversion time variances
Cample Time	Long Sample (ADLSMP = 1)	•	t <sub>ADS</sub>	ı	23.5	ı	cycles	
Total	12-bit mode	Т		_	±3.0	_		For 28-pin and 24-pin
Unadjusted	10-bit mode	Р	E <sub>TUE</sub>	_	±1	_	LSB <sup>2</sup>	packages only.
Error	8-bit mode	Т		_	±0.5	_		Includes quantization
Total	10-bit mode	Р		_	±1.5	_		For 16-pin
Unadjusted Error	8-bit mode	Т	E <sub>TUE</sub>	_	±0.7	_	LSB <sup>2</sup>	package only. Includes quantization
	12-bit mode	Т		_	±1.75	_		
Differential Non-Linearity	10-bit mode	Р	DNL	_	±0.5	_	LSB <sup>2</sup>	
	8-bit mode	Т		_	±0.3	_	1	
	Monotonicity and No-Missin	g-Code	s guarantee	t c				

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Table 16. 12-Bit ADC Characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)

Characteristic	Conditions	С	Symbol	Min	Typical <sup>1</sup>	Max	Unit	Comment
	12-bit mode	Т		-	±1.5	_		
Integral Non-Linearity	10-bit mode	С	INL	_	±0.5	_	LSB <sup>2</sup>	
,	8-bit mode			-	±0.3	_		
	12-bit mode	С		-	±1.5	_		For 28-pin and
Zero-Scale Error	10-bit mode	Р	E <sub>ZS</sub>	_	±0.5	±1.5	LSB <sup>2</sup>	24-pin packages only.
	8-bit mode	Т		_	±0.5	±0.5		$V_{ADIN} = V_{SSA}$
Zero-Scale	10-bit mode	Р	_		±1.5	±2.1		For 16-pin
Error	8-bit mode	Т	E <sub>ZS</sub>	_	±0.5	±0.7	LSB <sup>2</sup>	package only. V <sub>ADIN</sub> = V <sub>SSA</sub>
	12-bit mode	Т		_	±1	_		For 28-pin and
Full-Scale Error	10-bit mode	Р	E <sub>FS</sub>	_	±0.5	±1	LSB <sup>2</sup>	24-pin packages only.
	8-bit mode	Т		_	±0.5	±0.5		$V_{ADIN} = V_{DDA}$
Full-Scale	10-bit mode	Т	_	_	±1	±1.5		For 16-pin
Error	8-bit mode	Т	E <sub>FS</sub>	_	±0.5	±0.5	LSB <sup>2</sup>	package only. $V_{ADIN} = V_{DDA}$
	12-bit mode			_	-1 to 0	_		
Quantization Error	10-bit mode	D	EQ	_	_	±0.5	LSB <sup>2</sup>	
	8-bit mode			_	_	±0.5		
	12-bit mode			_	±1	_		
Input Leakage Error	10-bit mode	D	E <sub>IL</sub>	0	±0.2	<u>±</u> 4	LSB <sup>2</sup>	Pad leakage <sup>3</sup> * R <sub>AS</sub>
	8-bit mode			0	±0.1	±1.2		AO
Temp Sensor	−40°C− 25°C	D	m	_	1.646	_	mV/°C	
Slope	25°C- 85°C	7	m	_	1.769	_	IIIV/-C	
Temp Sensor Voltage	25°C	D	V <sub>TEMP25</sub>	_	701.2	_	mV	

Typical values assume V<sub>DDA</sub> = 3.0 V, Temp = 25 °C, f<sub>ADCK</sub>=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

## 3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

<sup>&</sup>lt;sup>2</sup> 1 LSB =  $(V_{REFH} - V_{REFL})/2^N$ 

<sup>&</sup>lt;sup>3</sup> Based on input pad leakage current. Refer to pad electricals.



Program and erase operations do not require any special power sources other than the normal  $V_{DD}$  supply. For more detailed information about program/erase operations, see the memory section.

**Table 17. Flash Characteristics** 

С	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase -40°C to 85°C	V <sub>prog/erase</sub>	1.8		3.6	V
D	Supply voltage for read operation	V <sub>Read</sub>	1.8		3.6	V
D	Internal FCLK frequency <sup>1</sup>	f <sub>FCLK</sub>	150		200	kHz
D	Internal FCLK period (1/FCLK)	t <sub>Fcyc</sub>	5		6.67	μS
D	Byte program time (random location) <sup>(2)</sup>	t <sub>prog</sub>		9		t <sub>Fcyc</sub>
D	Byte program time (burst mode) <sup>(2)</sup>	t <sub>Burst</sub>	4			t <sub>Fcyc</sub>
D	Page erase time <sup>2</sup>	t <sub>Page</sub>	4000			t <sub>Fcyc</sub>
D	Mass erase time <sup>(2)</sup>	t <sub>Mass</sub>	20,000			t <sub>Fcyc</sub>
D	Byte program current <sup>3</sup>	RI <sub>DDBP</sub>	_	4	_	mA
D	Page erase current <sup>3</sup>	RI <sub>DDPE</sub>	_	6	_	mA
С	Program/erase endurance <sup>4</sup> T <sub>L</sub> to T <sub>H</sub> = -40°C to + 85°C T = 25 °C	_	10,000	 100,000	_ _	cycles
С	Data retention <sup>5</sup>	t <sub>D_ret</sub>	15	100	_	years

The frequency of this clock is controlled by a software setting.

## 3.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

<sup>&</sup>lt;sup>3</sup> The program and erase currents are additional to the standard run  $I_{DD}$ . These values are measured at room temperatures with  $V_{DD} = 3.0 \text{ V}$ , bus frequency = 4.0 MHz.

Typical endurance for flash was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, Typical Endurance for Nonvolatile Memory.

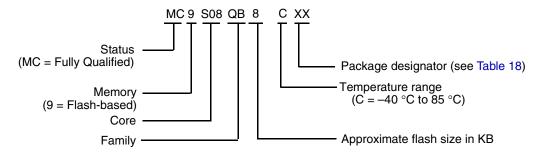
<sup>&</sup>lt;sup>5</sup> **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.* 



## 4 Ordering Information

This section contains ordering information for the device numbering system.

Example of the device numbering system:



## 5 Package Information

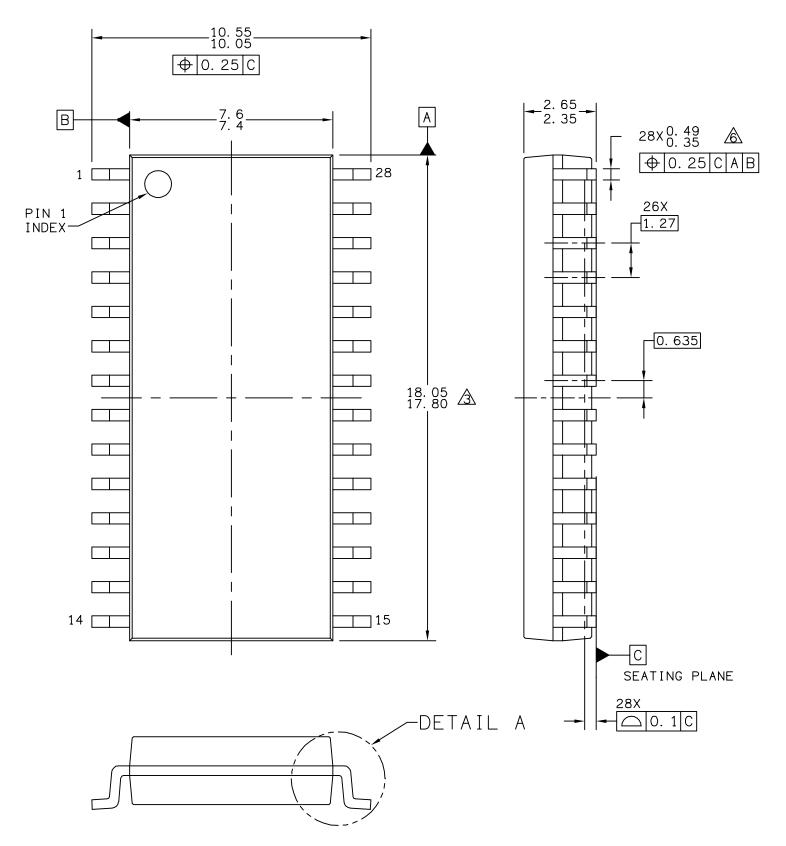
**Table 18. Package Descriptions** 

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
28	Small Outline Integrated Circuit	SOIC	WL	751F	98ASB42345B
24	Quad Flat Non-Leaded	QFN	GK	1982-01	98ARL10608D
16	Thin Shrink Small Outline Package	TSSOP	TG	948F	98ASH70247A

## 5.1 Mechanical Drawings

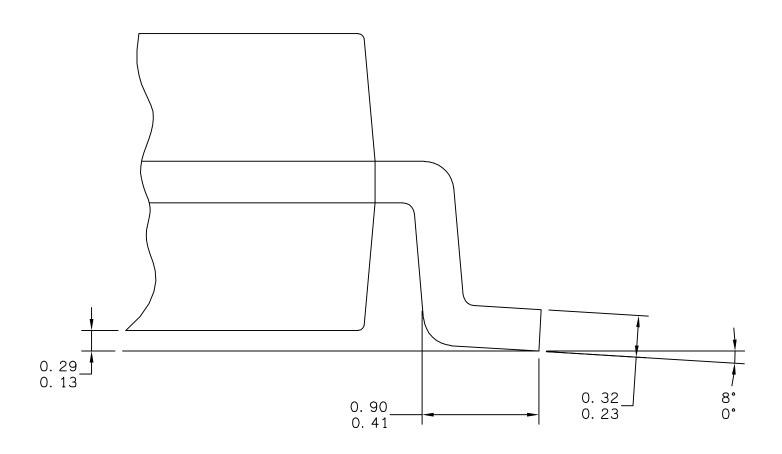
The following pages are mechanical drawings for the packages described in Table 18.





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28 LEAD		DOCUMENT NO	): 98ASB42345B	REV: G
		CASE NUMBER	R: 751F-05	10 MAR 2005
		STANDARD: MS	S-013AE	





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TITLE: SOIC, WIDE BODY,  28 LEAD  CASEOUTLINE		DOCUMENT NO	): 98ASB42345B	REV: G
		CASE NUMBER	2: 751F-05	10 MAR 2005
		STANDARD:	MS-013AE	



#### NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
- 4. 751F-01 THRU -04 OBSOLETE. NEW STANDARD: 751F-05

<u>/5\</u>

THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION.

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TITLE: SOIC, WIDE BOD	ΟY.	DOCUMENT NO	: 98ASB42345B	REV: G
28 LEAD	- · ,	CASE NUMBER	2: 751F-05	10 MAR 2005
CASEOUTLINE		STANDARD: MS	:_0134F	





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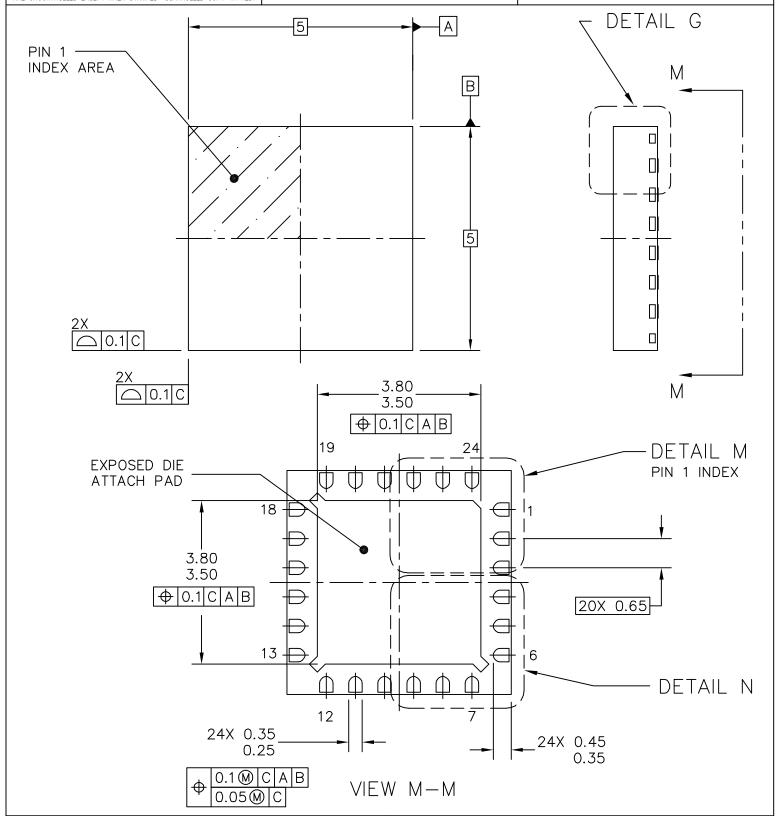
# MECHANICAL OUTLINES DICTIONARY

DO NOT SCALE THIS DRAWING

DOCUMENT NO: 98ARL10608D

PAGE: 1982

REV: 0



TITLE: THERMALLY ENHANCED QUAD

FLAT NON-LEADED PACKAGE (QFN)

24 TERMINAL, 0.65 PITCH (5 X 5 X 1)

CASE NUMBER: 1982-01

STANDARD: JEDEC-MO-220 VHHC-1

PACKAGE CODE: 6238 | SHEET: 1 OF 4





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# MECHANICAL OUTLINES DICTIONARY

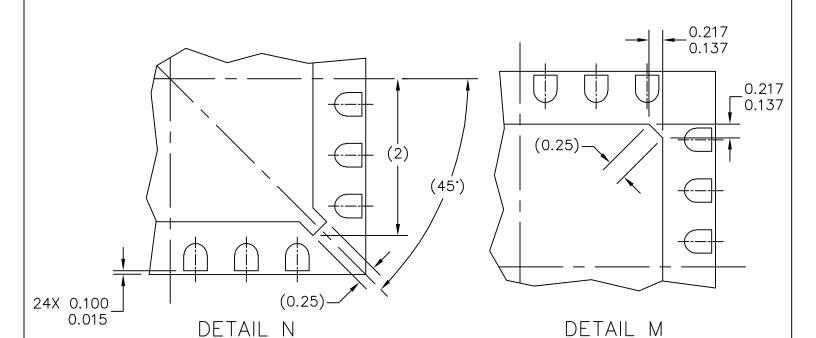
DO NOT SCALE THIS DRAWING

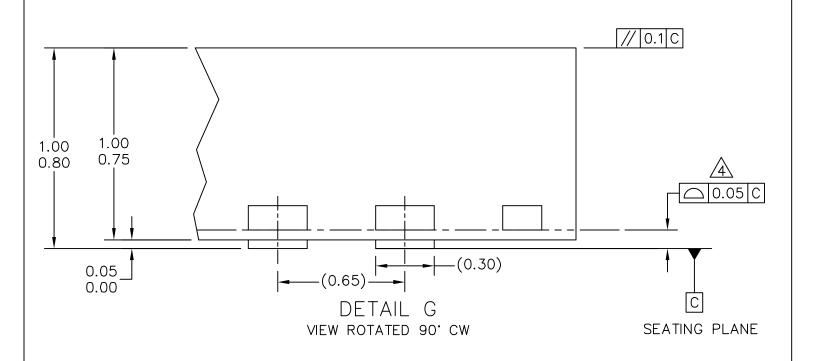
DOCUMENT NO: 98ARL10608D

PAGE: 1982

REV: 0

PREFERED PIN 1 BACKSIDE IDENTIFIER





TITLE: THERMALLY ENHANCED QUAD

FLAT NON-LEADED PACKAGE (QFN)

24 TERMINAL, 0.65 PITCH (5 X 5 X 1)

PREFERRED CORNER CONFIGURATION

CASE NUMBER: 1982-01

STANDARD: JEDEC-MO-220 VHHC-1

PACKAGE CODE: 6238 | SHEET: 2 OF 4



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# MECHANICAL OUTLINES DICTIONARY

DO NOT SCALE THIS DRAWING R

DOCUMENT NO: 98ARL10608D

PAGE:

1982

REV:

0

### NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- 3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFN.

4.

COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.

5. MIN METAL GAP SHOULD BE 0.2MM.

TITLE: THERMALLY ENHANCED QUAD

FLAT NON-LEADED PACKAGE (QFN)

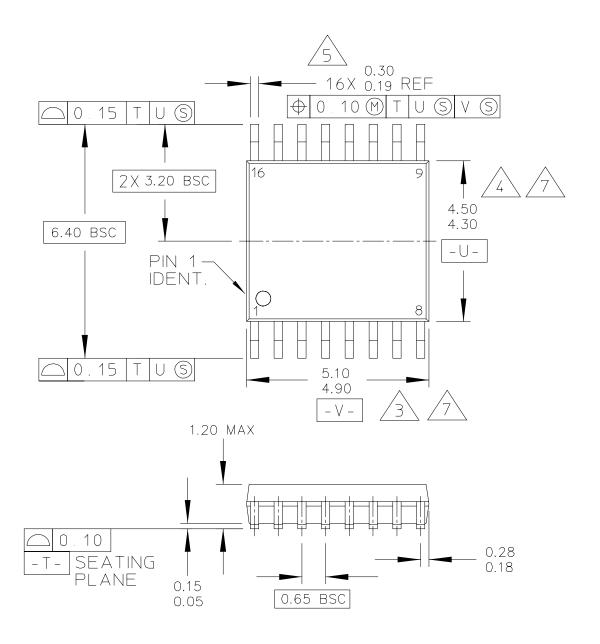
24 TERMINAL, 0.65 PITCH (5 X 5 X 1)

CASE NUMBER: 1982-01

STANDARD: JEDEC-MO-220 VHHC-1

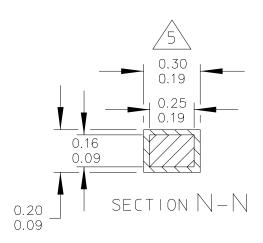
PACKAGE CODE: 6238 | SHEET: 3 OF 4

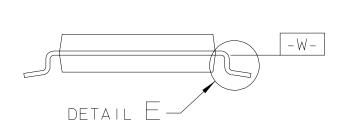


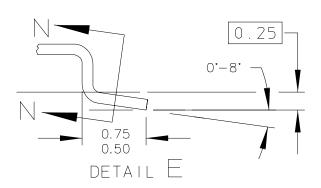


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TITLE:	DOCUMENT NO: 98ASH70247A		REV: B	
16 LD TSSOP, PITCH 0.69	CASE NUMBER: 948F-01 19 MAY 2005			
,		STANDARD: JE	DEC	









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TITLE:  16 LD TSSOP, PITCH 0.65MM		DOCUMENT NO: 98ASH70247A		REV: B
		CASE NUMBER: 948F-01 19 MAY 2		19 MAY 2005
		STANDARD: JE	DEC	



#### NOTES:

- 1. CONTROLLING DIMENSION: MILLIMETER
- 2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.



DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE



DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE



DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.



DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE [-W-]

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TITLE:		DOCUMENT NO: 98ASH70247A		REV: B
16 LD 1550P, PHCH 0.65MM		CASE NUMBER: 948F-01 19 MAY 2005		
		STANDARD: JE	DEC	





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