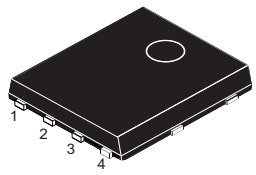
# STL12P6F6

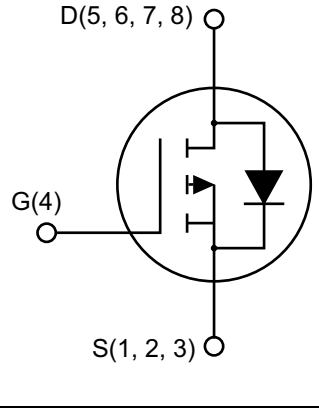
## P-channel 60 V, 0.13 Ω typ., 12 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

**Datasheet - production data**




**PowerFLAT™ 5x6**

**Figure 1. Internal schematic diagram**




## Features

| Order code | $V_{DS}$ | $R_{DS(on)max}$ | $I_D$ |
|---|---|---|---|
| STL12P6F6 | 60 V | 0.16 Ω @ 10 V | 12 A |

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

## Applications

- Switching applications

## Description

This device is an P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits a very low $R_{DS(on)}$ in all packages.

**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STL12P6F6 | 12P6F6 | PowerFLAT 5x6 | Tape and reel |

*Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.*

# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 60 | V |
| $V_{GS}$ | Gate-source voltage | ± 20 | V |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 25 °C | 12 | A |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 100 °C | 8.5 | A |
| $I_{DM}$ (1)(2) | Drain current (pulsed) | 48 | A |
| $I_D$ (3) | Drain current (continuous) at $T_{pcb}$ = 25 °C | 4 | A |
| $I_D$ (3) | Drain current (continuous) at $T_{pcb}$ = 100 °C | 2.8 | A |
| $P_{TOT}$ (1) | Total dissipation at $T_C$ = 25 °C | 75 | W |
| $P_{TOT}$ (3) | Total dissipation at $T_{pcb}$ = 25 °C | 4.8 | W |
| $T_j$ | Operating junction temperature | -55 to 175 | °C |
| $T_{stg}$ | Storage temperature | | °C |

1. The value is according to $R_{thj\text{-}case}$
2. Pulse width is limited by safe operating area.
3. The value is according to $R_{thj\text{-}pcb}$

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 2 | °C/W |
| $R_{thj\text{-}pcb}$ (1) | Thermal resistance junction-pcb max | 31.3 | °C/W |

1. When mounted on FR-4 board of 15 $mm^2$, 2 Oz Cu, t<10 sec

*Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.*

# 2 Electrical characteristics

(Tcase = 25 °C unless otherwise specified).

**Table 4. On /off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0, $I_D$ = 250 µA | 60 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0, $V_{DS}$ = 60 V | | | 1 | µA |
| | | $V_{GS}$ = 0, $V_{DS}$ = 60 V, $T_C$=125 °C | | | 10 | µA |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0, $V_{GS}$ = ± 20 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | | 4 | V |
| $R_{DS(on)}$ | Static drain-source on- resistance | $V_{GS}$ = 10 V, $I_D$ = 1.5 A | | 0.13 | 0.16 | Ω |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{GS}$ = 0, $V_{DS}$ = 48 V, f = 1 MHz | - | 340 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 40 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 20 | - | pF |
| $Q_g$ | Total gate charge | $V_{DD}$ = 30 V, $I_D$ = 3 A, $V_{GS}$ = 10 V (see *Figure 14*) | - | 6.4 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 1.7 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 1.7 | - | nC |

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 48 V, $I_D$ = 1.5 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 13*) | - | 64 | - | ns |
| $t_r$ | Rise time | | - | 5.3 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 14 | - | ns |
| $t_f$ | Fall time | | - | 3.7 | - | ns |

*Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.*

**Table 7. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$<br>$I_{SDM}$ (1) | Source-drain current<br>Source-drain current (pulsed) | | - | | 12<br>48 | A<br>A |
| $V_{SD}$ (2) | Forward on voltage | $V_{GS}$ = 0, $I_{SD}$ = 3 A | - | | 1.1 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 5 A, di/dt = 100 A/µs<br>$V_{DD}$ = 16 V, $T_j$ = 150 °C<br>(see *Figure 15*) | - | 20 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 17.8 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | 1.8 | | A |

1. Pulse width limited by safe operating area.
2. Pulse duration = 300 µs, duty cycle 1.5%

*Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.*

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

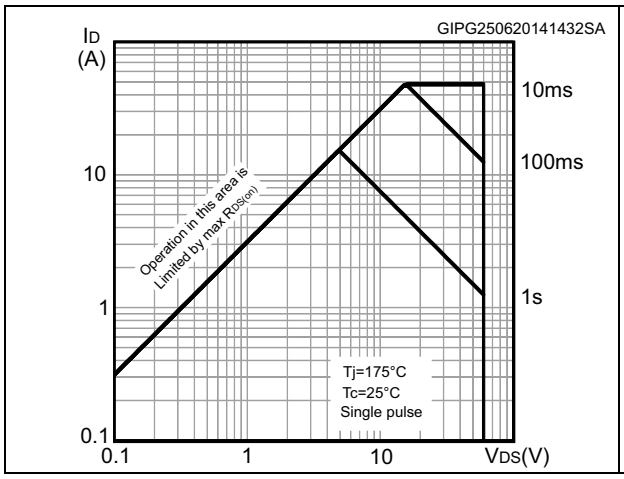



**Figure 3. Thermal impedance**

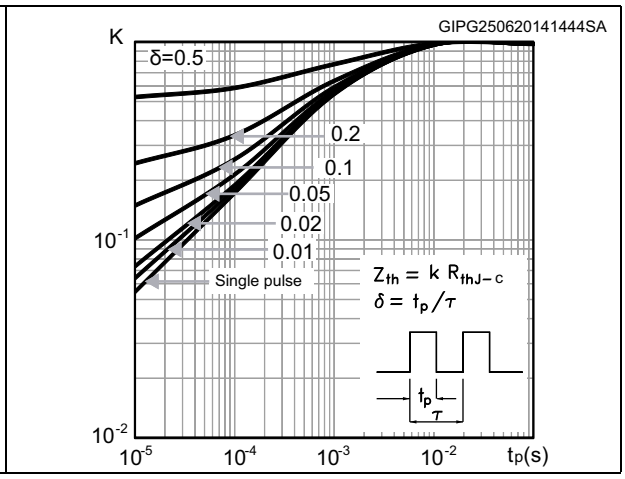



**Figure 4. Output characteristics**

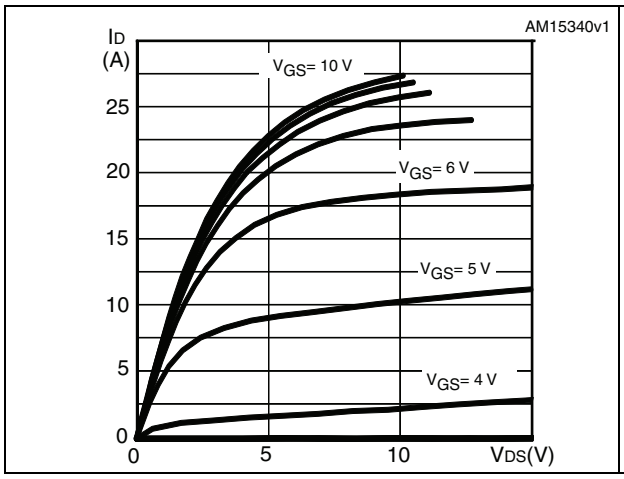



**Figure 5. Transfer characteristics**

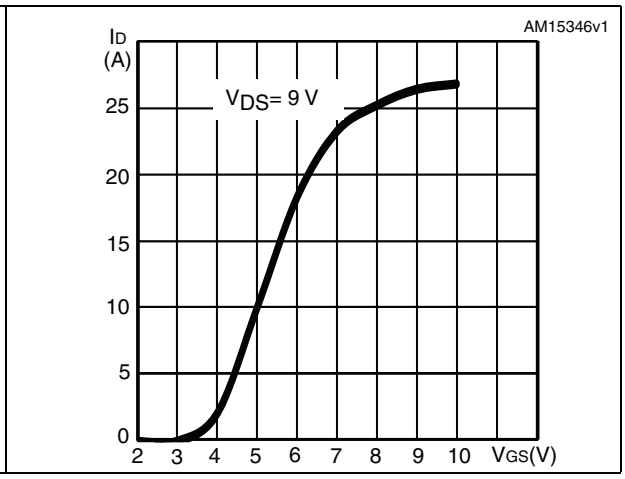



**Figure 6. Gate charge vs gate-source voltage**

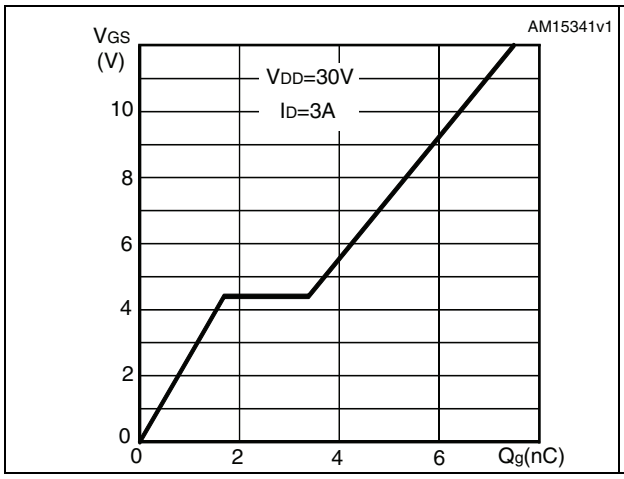



**Figure 7. Static drain-source on-resistance**

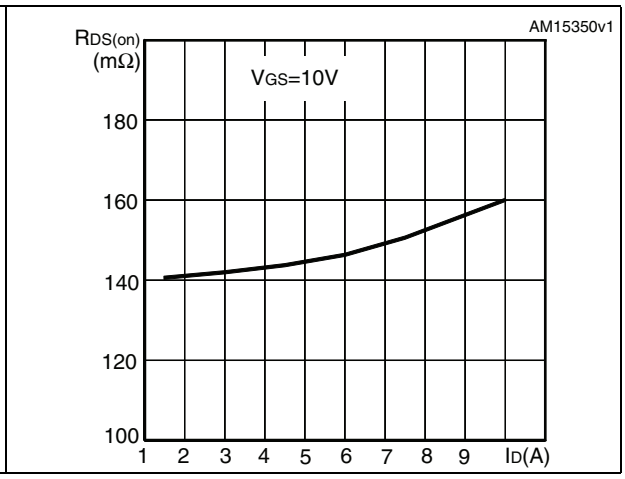


**Figure 8. Capacitance variations**

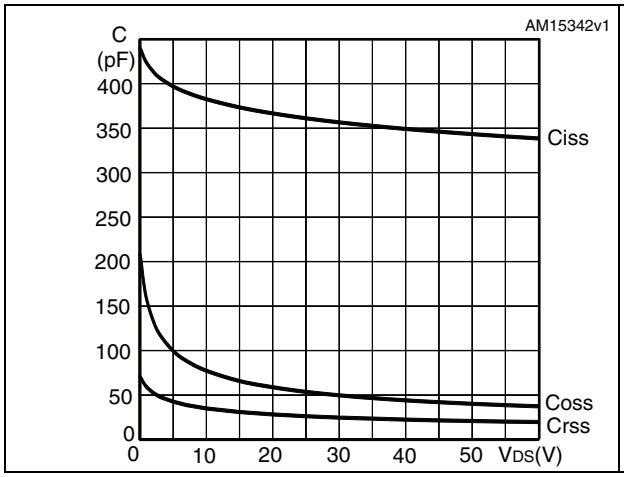



**Figure 9. Normalized $V_{(BR)DSS}$ vs temperature**

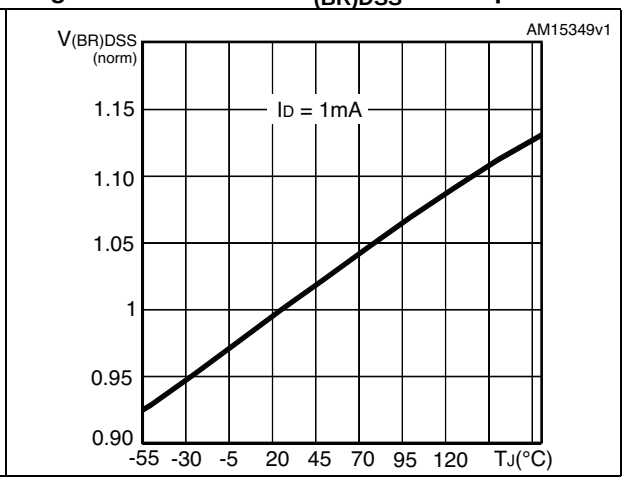



**Figure 10. Normalized gate threshold voltage vs temperature**

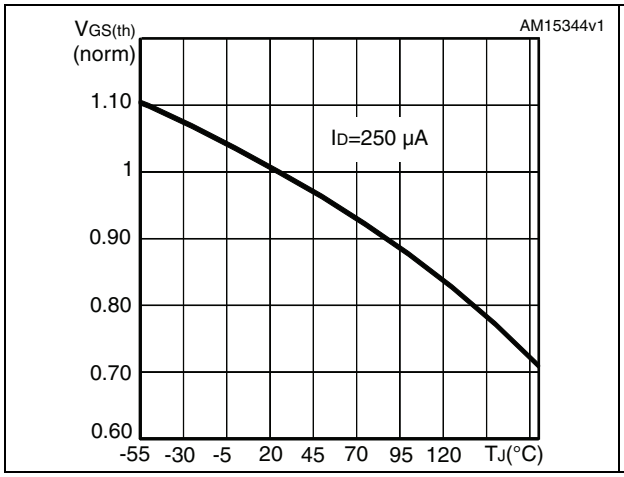



**Figure 11. Normalized on-resistance vs temperature**

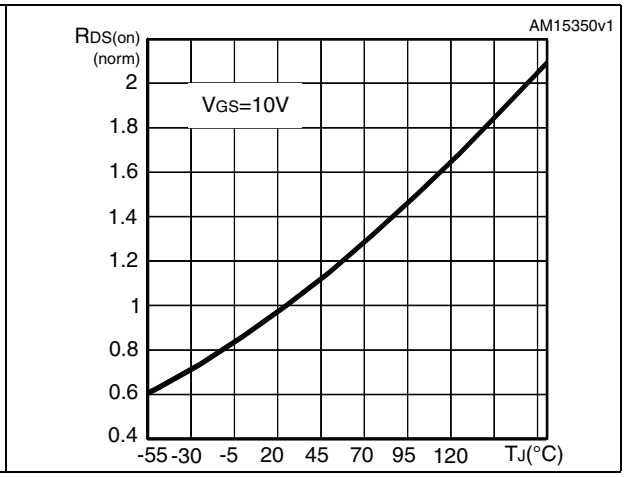
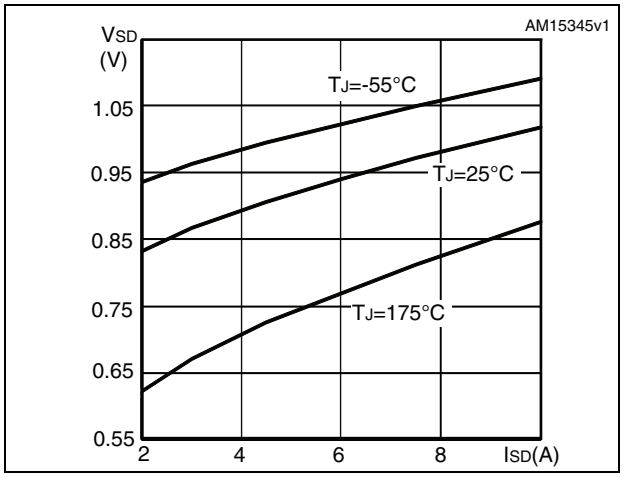



**Figure 12. Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**

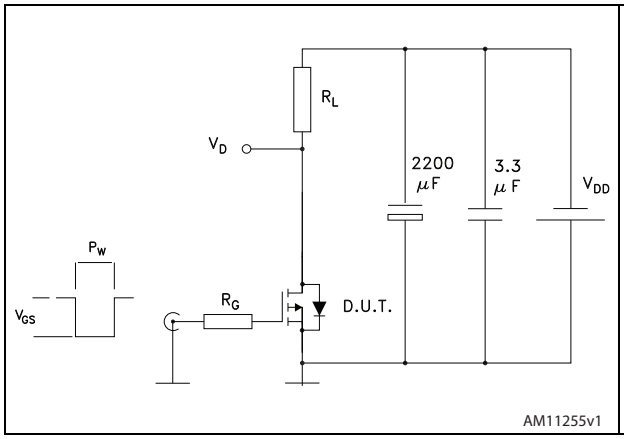



**Figure 14. Gate charge test circuit**

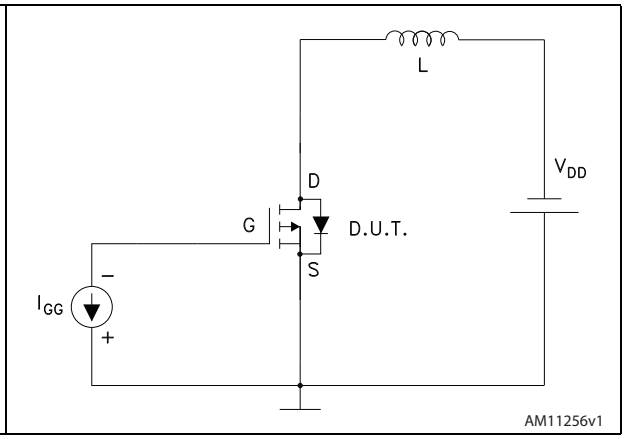
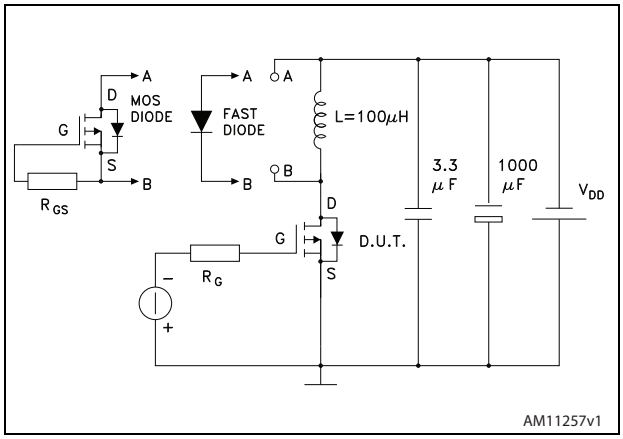



**Figure 15. Test circuit for inductive load switching and diode recovery times**



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

**Figure 16. PowerFLAT™ 5x6 type S-R drawing**

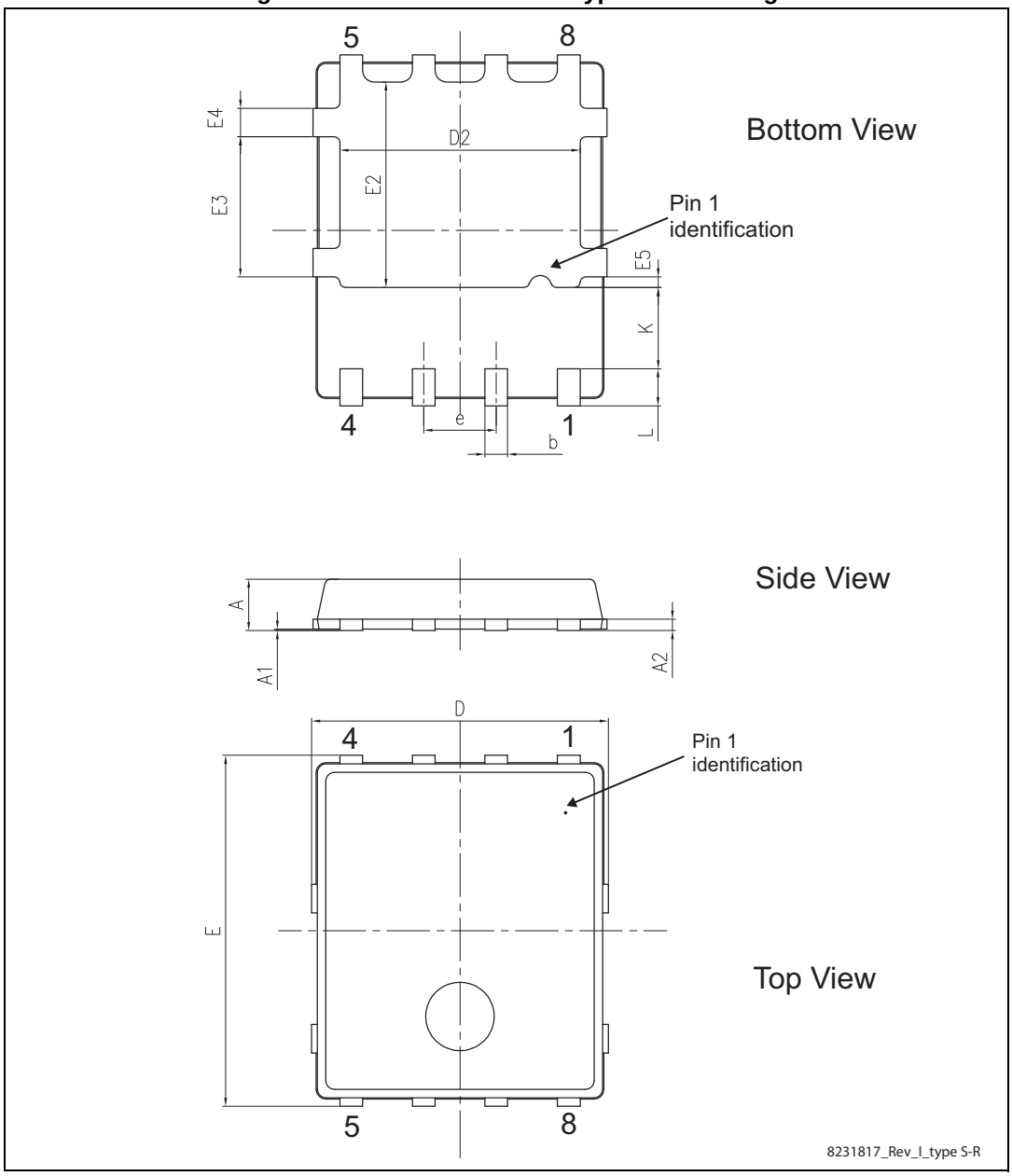
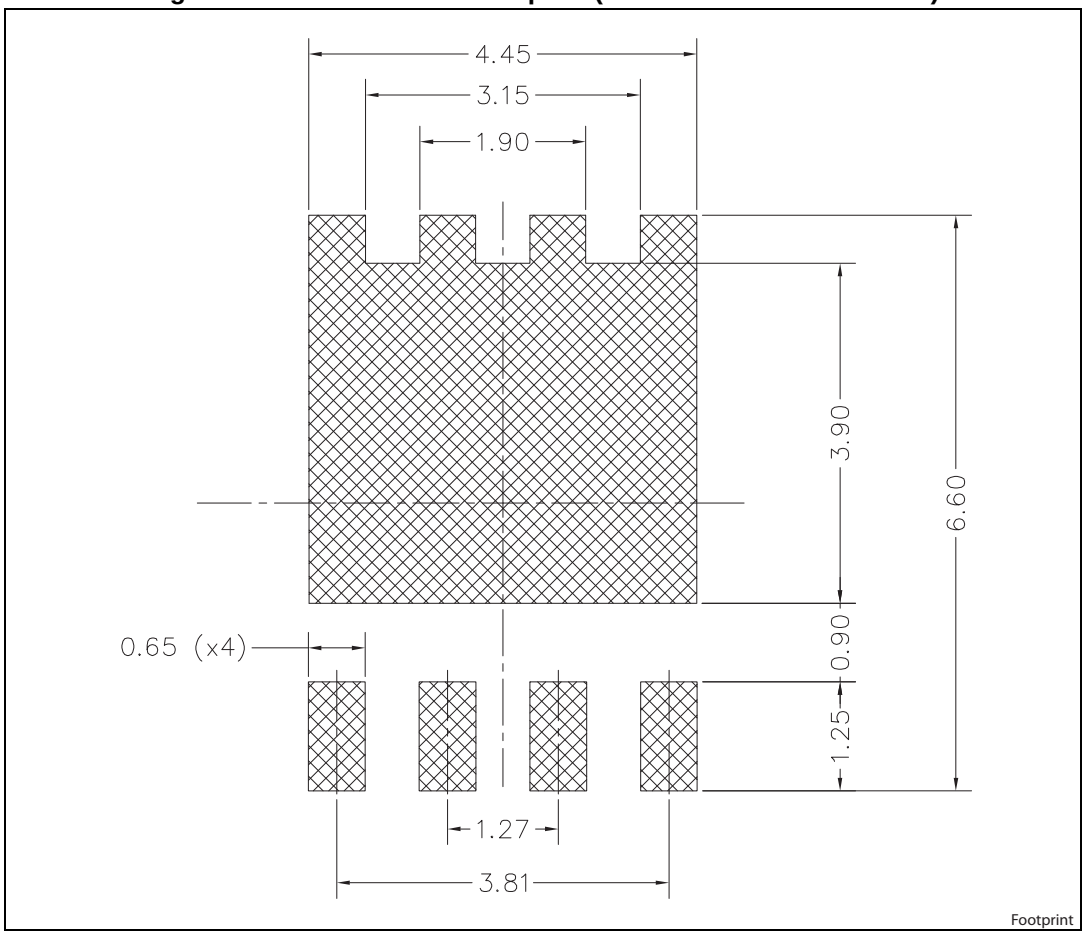


**Table 8. PowerFLAT 5x6 type S-R mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| D | 5.00 | 5.20 | 5.40 |
| D2 | 4.11 | | 4.31 |
| E | 5.95 | 6.15 | 6.35 |
| e | | 1.27 | |
| E2 | 3.50 | | 3.70 |
| E3 | 2.35 | | 2.55 |
| E4 | 0.40 | | 0.60 |
| E5 | 0.08 | | 0.28 |
| K | 1.275 | | 1.575 |
| L | 0.60 | | 0.80 |

**Figure 17. Recommended footprint (dimensions in millimeters)**



# 5 Packaging mechanical data

**Figure 18. PowerFLAT™ 5x6 tape[(a)]**

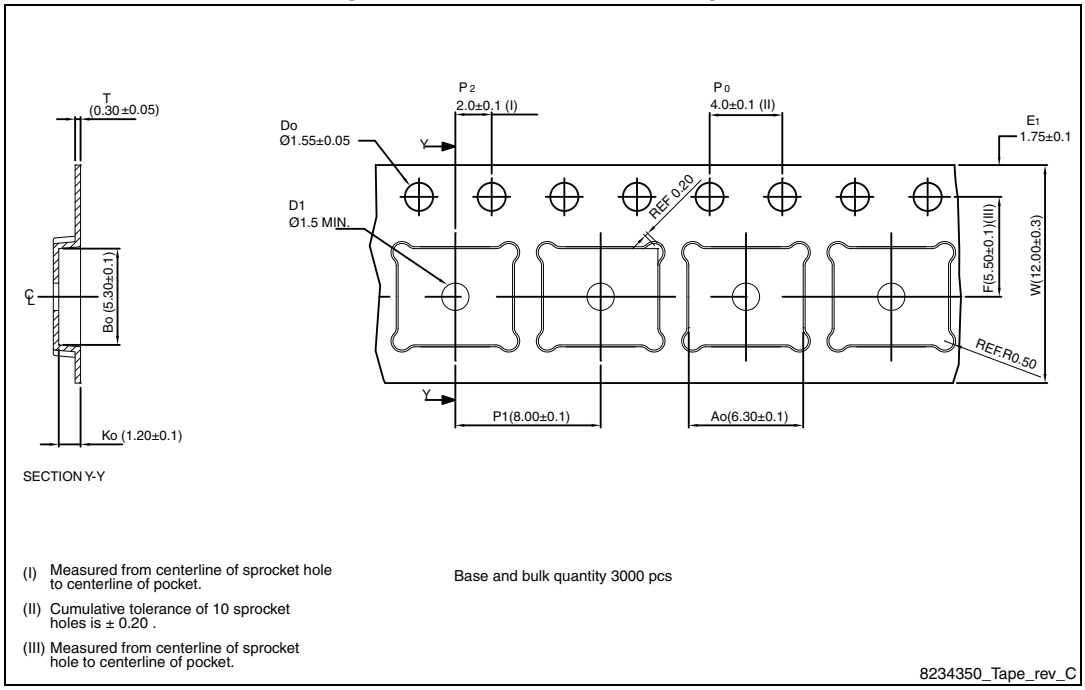
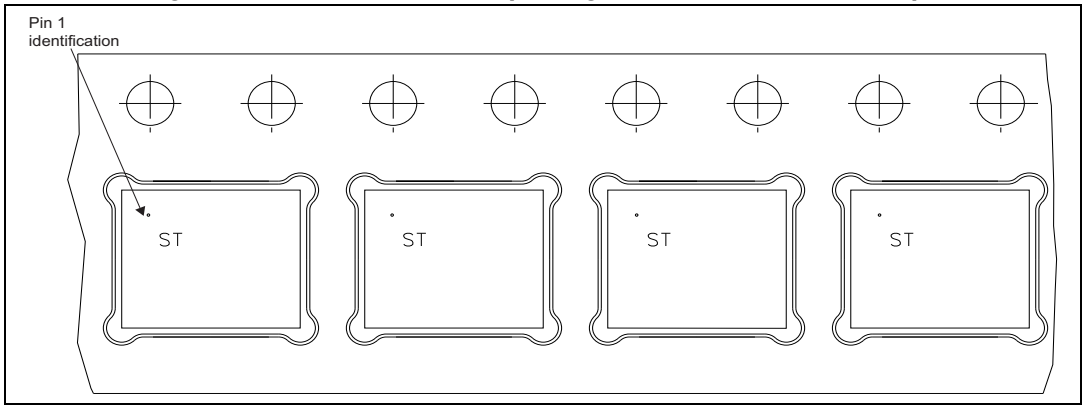
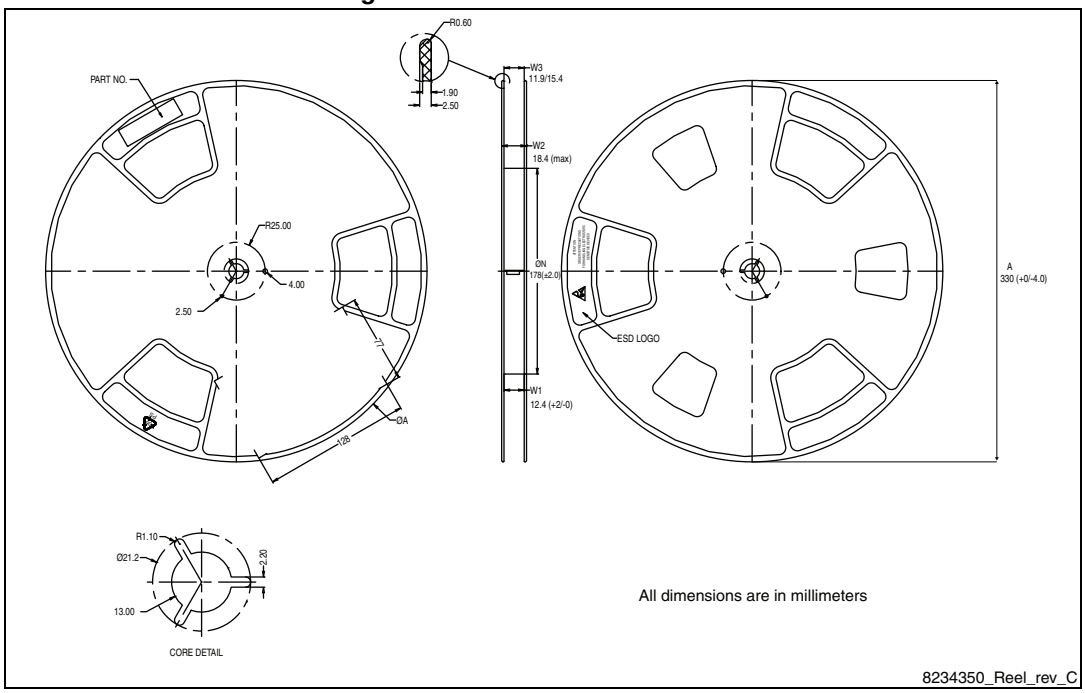



**Figure 19. PowerFLAT™ 5x6 package orientation in carrier tape**




a. All dimensions are in millimeters.

**Figure 20. PowerFLAT™ 5x6 reel**



# 6 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 20-Mar-2013 | 1 | First release. |
| 14-Jul-2014 | 2 | – Modified: $I_D$, and $I_{DM}$ values in *Table 2*<br>– Modified: the entire typical values in *Table 6*<br>– Modified: $I_{SD}$ and $I_{SDM}$ max values in *Table 7*<br>– Added: *Section 2.1: Electrical characteristics (curves)*<br>– Updated: *Section 4: Package mechanical data*<br>– Minor text changes |

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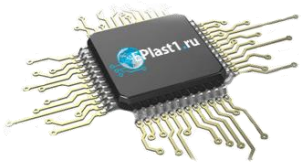
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

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