General Description

The MAX31629 I²C digital thermometer and real-time clock (RTC) integrates the critical functions of a real-time clock and a temperature monitor in a small-outline 8-pin TDFN package. Communication to the device is accomplished through an I²C interface. The wide power-supply range and minimal power requirement of the device allow for accurate time/temperature measurements in battery-powered applications.

The digital thermometer provides 9-bit to 12-bit temperature readings that indicate the temperature of the device.

No additional components are required; the device is truly a “temperature-to-digital” converter.

The clock/calendar provides seconds, minutes, hours, day, day of the week, month, day of the month, and year. The end-of-the-month date is automatically adjusted for months with less than 31 days, including corrections for leap years. It operates in either a 12- or 24-hour format with AM/PM indicator in 12-hour mode. The crystal oscillator frequency is internally divided, as specified by device configuration. An open-drain output is provided that can be used as the oscillator input for a microcontroller.

The open-drain alarm output of the device becomes active when either the measured temperature exceeds the programmed overtemperature limit (TH) or current time reaches the programmed alarm setting. The user can configure which event (time only, temperature only, either, or neither) generates an alarm condition. For storage of general system data or time/temperature data logging, the device features 32 bytes of SRAM. Applications for the device include networking equipment, industrial equipment, office equipment, thermal data loggers, or any microprocessor-based, thermally sensitive system.

Benefits and Features

- Integration of Temperature Sensor and Real-Time Clock Saves Space and Cost
  - Measures Temperatures from -55°C to +125°C (-67°F to +257°F)
  - Real-Time Clock with Leap-Year Compensation through the Year 2100
  - 32 Bytes of SRAM for General Data Storage
  - 8-Pin TDFN Package
- Minimal Power Requirements Allow for Accurate Time/Temperature Measurements in Battery-Powered Applications
  - 2.2V to 5.5V Wide Power-Supply Range
- User-Programmability Flexibly Supports Different Application Requirements
  - Thermometer Resolution is User Programmable to 9, 10, 11, or 12 Bits
  - Thermostatic and Time Alarm Settings are User Definable
  - Dedicated Open-Drain Alarm Output
- Industry-Standard Serial Interface Works with a Variety of Common Microcontrollers
  - Data is Read from/Written to through an I²C Serial Interface (Open-Drain I/O Lines)

Applications

- Networking Equipment
- Industrial Equipment
- Office Equipment
- Data Loggers and Any Thermally Sensitive Systems

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX31629.related.

19-7305; Rev 1; 12/14

maxim integrated™

Absolute Maximum Ratings

Voltage Range on V_{DD} Relative to Ground .....-0.3V to +6.0V
Voltage Range on Any Pin
Relative to Ground..... -0.3V to (V_{DD} + 0.3V)
ESD Protection (all pins, Human Body Model) 2kV
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 24.4mW/°C above +70°C.....1951.2mW

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA})..... 41°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 8°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Recommended Operating Conditions

(T_A = -55°C to +125°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Supply	V_{DD}	(Note 3)	2.2		5.5	V
Input Logic 0	V_{IL}	(Note 3)	-0.5		0.3 x V_{DD}	V
Input Logic 1	V_{IH}	(Note 3)	0.7V_{DD}		V_{DD} + 0.5	V

Electrical Characteristics

(2.2V ≤ V_{DD} ≤ 5.5V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Standby Current	I_{DDS}	V_{DD} = 2.2V (Note 4)			0.1	µA
		V_{DD} = 5.0V (Note 4)			0.2	
Timekeeping Current	I_{DDC}	V_{DD} = 2.2V (Note 5)			0.8	µA
		V_{DD} = 5.0V (Note 5)			1	
I²C Communication	I_{DD2}	V_{DD} = 2.2V (Note 5)			100	µA
		V_{DD} = 5.0V (Note 5)			150	
Thermometer Current	I_{DDT}	V_{DD} = 2.2V (Note 5)			1100	µA
		V_{DD} = 5.0V (Note 5)			1100	
Active Current	I_{DD}	V_{DD} = 2.2V (Note 5)			1100	µA
		V_{DD} = 5.0V (Note 5)			1200	
Logic 0 Output (SDA, ALRM, OSC)	V_{OL}	(Note 6)	0		0.4	V
Input Current, Each I/O Pin		0.4V < $V_{I/O}$ < 0.9 V_{DD}	-10		+10	µA
Thermometer Error	T_{ERR}	-10°C to +85°C, 2.7V < V_{DD} < 5.5V			±2	°C
		4 sigma, 2.7V < V_{DD} < 5.5V			±3	
Resolution			9		12	Bits

Electrical Characteristics (continued)

(2.2V ≤ V_{DD} ≤ 5.5V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Time	t_{CONVT}	9 bits, 2.7V < V_{DD} < 5.5V			25	ms
		10 bits, 2.7V < V_{DD} < 5.5V			50	
		11 bits, 2.7V < V_{DD} < 5.5V			100	
		12 bits, 2.7V < V_{DD} < 5.5V			200	
Crystal Capacitance	C_C	(Note 7)		12.5		pF
ESR					50	kΩ

Nonvolatile Memory (EEPROM) Characteristics

((2.7V ≤ V_{DD} ≤ 5.5V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycle Time	t_{WR}				20	ms
EEPROM Writes	N_{EEWR}	-55°C to +55°C	50,000			Writes
EEPROM Data Retention	t_{EEDR}	-55°C to +55°C	10			Years

I²C AC Electrical Characteristics

(2.2V ≤ V_{DD} ≤ 5.5V, T_A = -55°C to +125°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MAX)}$, unless otherwise noted.) (Note 2) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{CLK}				400	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}	f_{CLK} = 400kHz	1.3			µs
Repeated START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Setup Time		90% of SCL to 90% of SDA, f_{CLK} = 400kHz	0.6			µs
START Condition Hold Time	$t_{HD:STA}$	90% of SDA to 90% of SCL, f_{CLK} = 400kHz	0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$	90% of SCL to 90% of SDA, f_{CLK} = 400kHz	0.6			µs
Clock Low Period	t_{LOW}	10% to 10%	1			µs
Clock High Period	t_{HIGH}	90% to 90%	1			µs
Data-In Hold Time	$t_{HD:DAT}$	(Note 9)	0		0.9	µs

I²C AC Electrical Characteristics (continued)

(2.2V ≤ V_{DD} ≤ 5.5V, T_A = -55°C to +125°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MAX)}$, unless otherwise noted.) (Note 2) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data-In Setup Time	$t_{SU:DAT}$		100			ns
Input Capacitance	C_I			5		pF
Capacitance Load for Each Bus Line	C_B	(Note 10)			300	pF

Note 2: Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.
Note 3: All voltages referenced to ground.
Note 4: Standby current specified with temperature conversions and clock oscillator/buffer shut down, ALRM pin open, and SDA, SCL = V_{DD}, 0°C to +70°C.
Note 5: $I_{DD\_}$ specified with ALRM pin open, and 0°C to +70°C.
Note 6: Logic 0 voltage specified at a sink current of 4mA at V_{DD} = 5.0V and 1.5mA at V_{DD} = 2.2V.
Note 7: Refer to Application Note 58: *Crystal Considerations with Maxim Real-Time Clocks (RTCs)*. Recommnded ESR < 50kΩ.
Note 8: This delay applies only if the oscillator is running. If the oscillator is disabled or stopped, no power-up delay occurs.
Note 9: A master device must provide a hold time of at least 300ns for the SDA signal to bridge the undefined region of SCL's falling edge.
Note 10: C_B is the total capacitance of one bus line in pF..

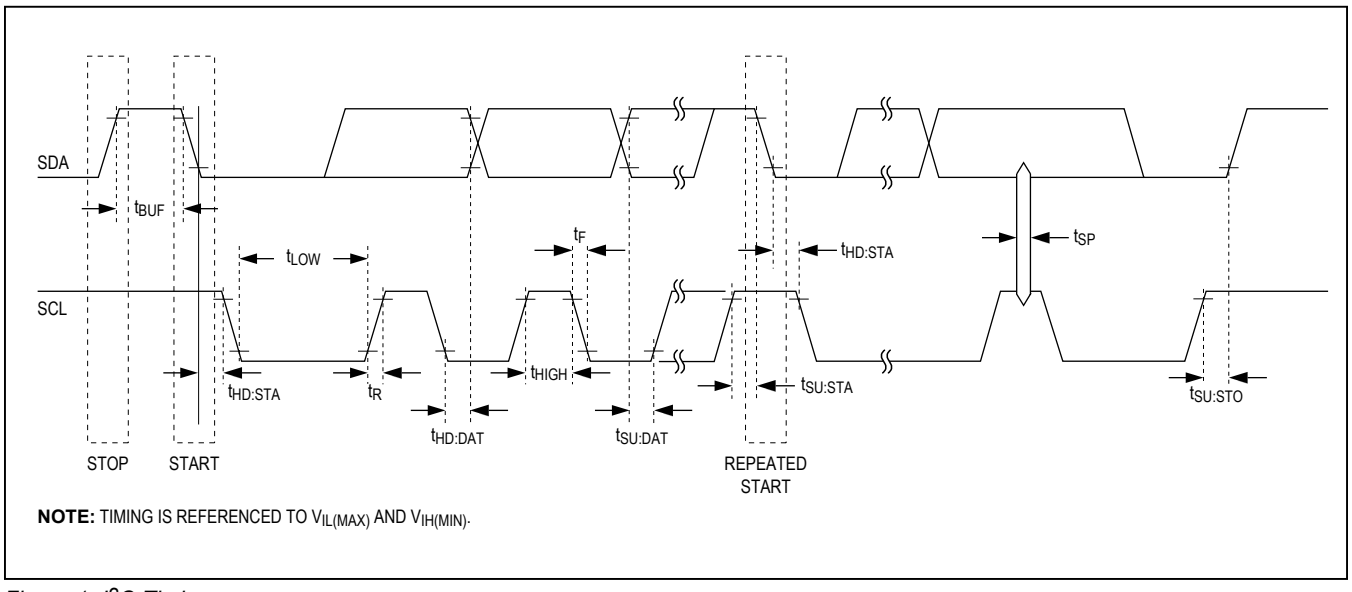
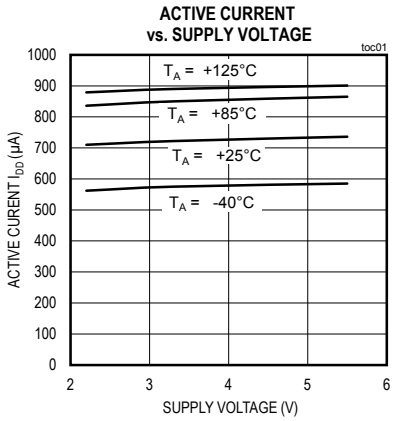
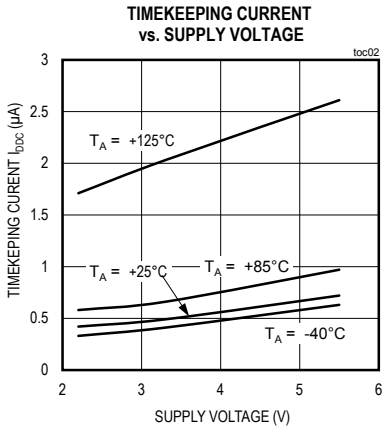


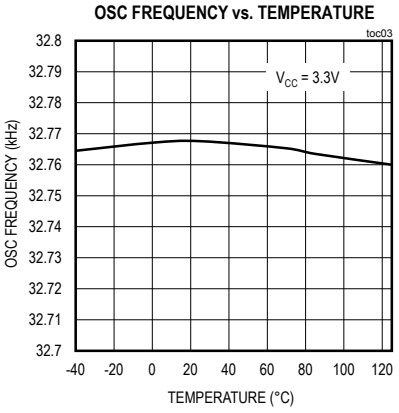
Figure 1. I²C Timing

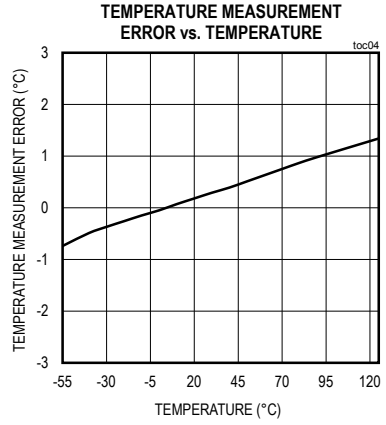
Typical Operating Characteristics

(2.2V ≤ V_{DD} ≤ 5.5V, T_A = +25°C, unless otherwise noted.)

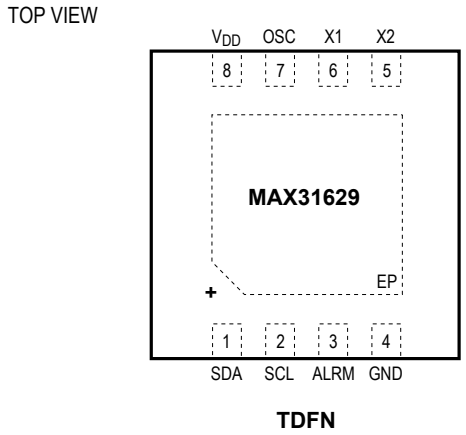








Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	SDA	Serial-Data Input/Output. SDA is the input/output pin for the I²C serial interface. The SDA pin is an open-drain output and requires an external pullup resistor. The pullup voltage can be up to 5.5V, regardless of the voltage on V_{DD}.
2	SCL	Serial-Clock Input. SCL is used to synchronize data movement on the I²C serial interface. The pullup voltage can be up to 5.5V, regardless of the voltage on V_{DD}.
3	ALRM	Thermostat and Clock Alarm Output
4	GND	Ground
5	X2	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. For more information about crystal selection and crystal layout considerations, see the *Applications Information* section and refer to Application Note 58: *Crystal Considerations with Maxim Real-Time Clocks (RTCs)*.
6	X1	
7	OSC	Buffered Oscillator Output
8	V_{DD}	Primary Power Supply. When voltage is applied within normal limits, the device is fully accessible and data can be written and read.
EP	—	Exposed Pad.

Detailed Description

The factory-calibrated temperature sensor requires no external components. The very first time that the MAX31629 is powered up, it begins temperature conversions and performs conversions continuously. The host can periodically read the value in the temperature register, which contains the last completed conversion. As conversions are performed in the background, reading the temperature register does not affect the conversion in progress.

The host can modify the device configuration such that it does not power up in the autoconvert or continuous-convert modes. This could be beneficial in power-sensitive applications.

The real-time clock/calendar maintains a binary-coded decimal (BCD) count of seconds, minutes, hours, day, day of the week, month, day of the month, and year. It does so with an internal oscillator/divider and a required 32.768kHz crystal. The end-of-the month date is automatically updated for months with less than 31 days, including compensation for leap years through the year 2100. The clock format is configurable as a 12-hour (power-up default) or 24-hour format, with an AM/PM indicator in the 12-hour mode. The RTC can be shut down by clearing a bit in the clock register.

The crystal frequency is internally divided by a factor that the user defines. The divided output is buffered and can be used to clock a microcontroller.

The device features an open-drain alarm output that can be configured to activate on a thermal event, time event, either thermal or time, or neither thermal or time (disabled, power-up state). The thermal alarm becomes active when measured temperature is greater than or equal to the value stored in the TH thermostat register. It remains active until temperature is equal to or less than the value stored in TL, allowing for programmable hysteresis. The clock alarm activates at the specific minute of the week that is programmed in the clock alarm register. The time alarm is cleared by reading from or writing to either the clock register or the clock alarm register.

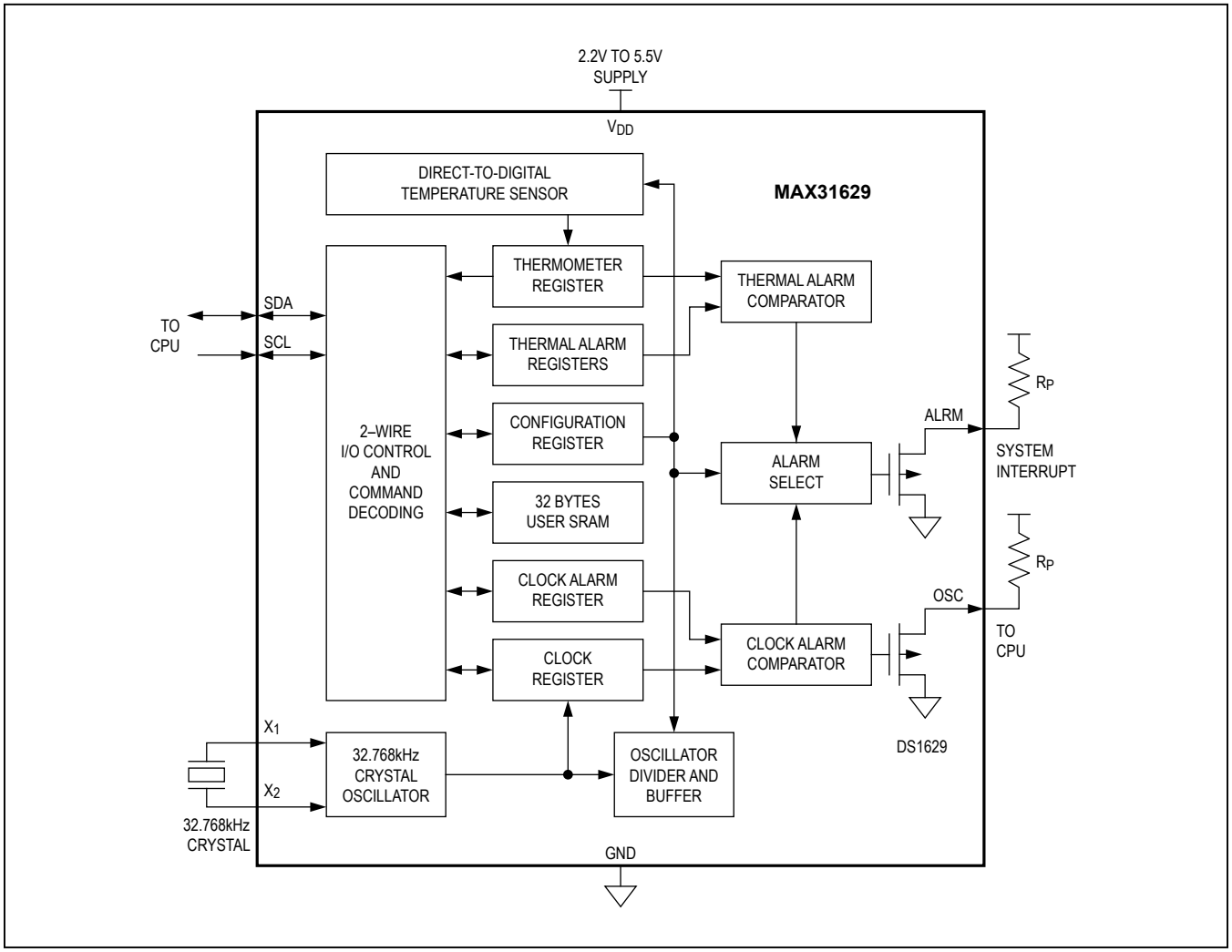
The device Configuration register defines several key items of device functionality. It sets the conversion mode of the digital thermometer and what event, if any, constitutes an alarm condition. It also sets the active state of the alarm output. Finally, it enables/disables and sets the division factor for the oscillator output.

The device also features 32 bytes of SRAM for storage of general information. This memory space has no bearing on thermometer or chronograph operation. Possible uses for this memory are time/temperature histogram storage, thermal data-logging, etc.

Digital data is written to/read from the device through an I2C interface, and all communication is MSb first. Individual registers are accessed by unique 8-bit command protocols.

The device features a wide power-supply range (2.2V ≤ V_{DD} ≤ 5.5V) for clock functionality, SRAM data retention, and I2C communication. EEPROM writes and temperature conversions should only be performed at 2.7V ≤ V_{DD} ≤ 5.5V for reliable results.

Block Diagram



Measuring Temperature

The device measures temperature using a bandgap-based temperature sensor. A delta-sigma analog-to-digital converter (ADC) converts the measured temperature to a 9-, 10-, 11-, or 12-bit (user-selectable) digital value that is calibrated in °C; for °F applications, a lookup table or conversion routine must be used. Throughout this data sheet, the term “conversion” is used to refer to the entire temperature measurement and ADC sequence.

The device can be configured to perform a single conversion, store the result, and return to a standby mode, or it can be programmed to convert continuously. The very first time the device is powered up from the factory, it begins temperature conversions and performs conversions continuously. Regardless of the mode used, the last completed digital temperature conversion is retrieved from the temperature register using the Read Temperature (AAh) protocol, as described in detail in the *Command Set* section. Details on how to change the settings after power-up are contained in the *Configuration/Status Register* section.

The resolution of the output digital temperature data is user-configurable or 9, 10, 11, or 12 bits, corresponding to temperature increments of 0.5°C, 0.25°C, 0.125°C, and 0.0625°C, respectively. The default power-up is 12 bits and can be changed through the R0 and R1 bits in the Resolution register. Note that the conversion time doubles for each bit of resolution.

After each conversion, the digital temperature sensor is stored as a 16-bit two's complement number in the two-byte temperature register, as shown in Table 1. The sign bit (S) indicates if the temperature is positive or negative; for positive numbers, S = 0 and for negative numbers, S = 1. The Read Temperature command [AAh] provides user access to the temperature register. Bits 3:0 of the temperature register are hardwired to 0. When the device is configured for 12-bit resolution, the 12MSbs (bits 15:4) of the temperature register contain temperature data. For 11-bit resolution, the 11MSbs (bits 15:5) of the temperature register contain data, and bit 4 is 0. Likewise, for 10-bit resolution, the 10MSbs (bits 15:6) contain data, and for 9-bit resolution the 9MSbs (bits 15:7) contain data, and all unused LSbs contain 0s. Table 2 gives examples of the 12-bit resolution output data and the corresponding temperatures. The data is transmitted through the I2C serial interface, MSb first. The device can measure temperature over the range of -55°C to +125°C in increments determined by the programmable bits of resolution (see Table 1).

Real-Time Clock/Calendar

The device RTC/calendar data is accessed with the I2C command protocol, C0h. If the R/$\overline{W}$ bit in the I2C control byte is set to 0, then the bus master sets the clock (write to the Clock register). The bus master sets the R/$\overline{W}$ bit to 1 to read the current time (read from the clock register). See the *I2C Serial Data Bus* section for details on this protocol.

The format of the Clock register is shown in Table 3. Data format for the Clock register is BCD. Most of the Clock register is self-explanatory, but a few of the bits require elaboration.

CH = Clock Halt Bit. This bit is set to 0 to enable the oscillator and set to 1 to disable it. If the bit is changed during a write to the clock register, the oscillator does not start (or stop) until the bus master issues a STOP pulse. The device power-up default has the oscillator enabled (CH = 0) so that OSC can be used for clocking a microcontroller at power-up.

12 Mode/24 Mode = Clock Mode Bit. This bit is set high when the clock is in the 12-hour mode and set to 0 in the 24-hour mode. Bit 5 of byte 02h of the Clock register contains the MSb of the hours (1 for hours 20–23) if the clock is in the 24-hour mode. If the clock mode is set to the 12-hour mode, this is the AM/PM bit. In the 12-hour mode, a 0 in this location denotes AM and a 1 denotes PM. When setting the clock, this bit must be written to according to the clock mode used.

Bits in the Clock register filled with 0 are a "don't care" on a write, but always reads out as 0.

Table 1. Temperature/Data Relationships

SIGN	2^6	2^5	2^4	2^3	2^2	2^1	2^0	MSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	0	0	0	0	LSB
MSb	(for 10-bit conversions)	(for 11-bit conversions)	(for 12-bit conversions)				LSb	

Table 2. Temperature Format Examples

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	DIGITAL OUTPUT (HEX)
+125	0111 1101 0000 0000	7D00
+25.0625	0001 1001 0001 0000	1910
+10.125	0000 1010 0010 0000	0A20
+0.5	0000 0000 1000 0000	0080
0	0000 0000 0000 0000	0000
-0.5	1111 1111 1000 0000	FF80
-10.125	1111 0101 1110 0000	F5E0
-25.0625	1110 0110 1111 0000	E6F0
-55	1100 1001 0000 0000	C900

Table 3. Clock Register Format

BYTE ADDRESS	BIT 7 MSb	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSb	BYTE RANGE
00h	CH	10 Seconds			Seconds				00-59
01h	0	10 Minutes			Minutes				00-59
02h	0	12 Mode	AM/PM	10 Hours	Hours				01-12
		24 Mode	10 Hours						00-23
03h	0	0	0	0	0	Day			01-07
04h	0	0	10 Date		Date				01-31*
05h	0	0	0	10 Month	Month				01-12
06h	10 Year				Year				00-99

**Data byte maximum value ranges are from 28–31, depending on the month and year.*

Alarms

The device features an open-drain alarm output with a user-definable active state (factory default is active low). By programming the Configuration register, the user also defines the event, if any, that would generate an alarm condition. The four possibilities are:

1) Temperature alarm only.
2) Time alarm only.
3) Either temperature or time alarm.
4) Alarm disabled (power-up default).

See the *Configuration/Status Register* section for programming protocol. If the user chooses the alarm mode under which a thermal or time event generates an alarm condition, it is possible that either or both are generating the alarm. There are status bits in the Configuration register (TAF, CAF) that define the current state of each alarm. In this way, the master can determine which event generated the alarm. If both events (thermal and time) are in an alarm state, the ALRM output remains active until both are cleared. ALRM is the logical OR of the TAF and CAF flags if the device is configured for either to trigger the ALRM output. Figure 2 illustrates a possible scenario with this alarm mode. See the *Thermometer Alarm* and *Clock Alarm* sections on how respective alarms are cleared.

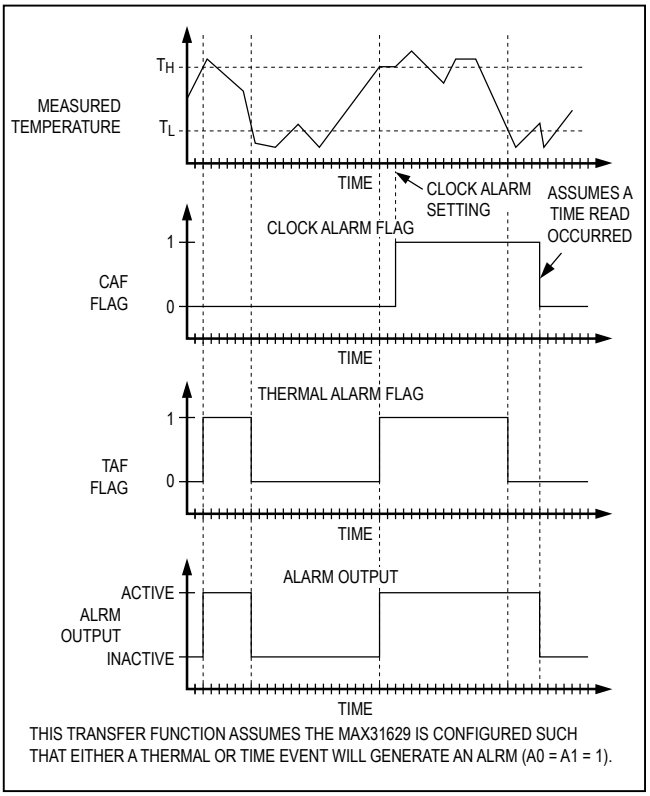


Figure 2. Alarm Transfer Function

Thermometer Alarm

The thermostat comparator updates as soon as a temperature conversion is complete. When the device's temperature meets or exceeds the value stored in the high temperature trip register (TH), the TAF flag becomes active (high), and stays active until the temperature falls below the temperature stored in the low-temperature trigger register (TL).

The respective register can be accessed over the I²C bus through the Access TH (A1h) or Access TL (A2h) commands. Reading from or writing to the respective register is controlled by the state of the R/$\overline{W}$ bit in the I²C control byte (see the *I²C Serial Data Bus* section).

The format of the TH and TL registers is identical to that of the Thermometer register; that is, 9- to 12-bit two's complement representation of the temperature in °C. The TH and TL resolution is determined by the R0 and R1 bits in the Configuration register so the TH and TL resolution matches the output temperature resolution. The TH and TL registers are stored in EEPROM; therefore, they are NV and can be programmed prior to device installation. Writing to and reading from the TH and TL registers is achieved using the Access TH and Access TL commands. When making changes to the TH and TL registers, conversions should first be stopped using the Stop Convert T command if the device is in continuous-conversion mode. Note that if the thermostat function is not used, the TH and TL registers can be used as general-purpose NV memory.

Clock Alarm

The clock alarm flag (CAF) becomes active within one second after the second, minute, hour, and day (of the week) of the Clock register match the respective bytes in the Clock Alarm register. CAF remains active until the bus master writes to or reads from either the Clock register through the C0h command or the Clock Alarm register through the C7h command.

The format of the Clock Alarm register is shown in Table 5. The power-up default of the device has the clock alarm set to 12:00AM on Sunday. The register can be accessed over the I²C bus through the Access Clock Alarm (C7h) command. Reading from or writing to the register is controlled by the state of the R/$\overline{W}$ bit in the I²C control byte (see the *I²C Serial Data Bus* section).

The master must take precaution in programming bit 5 of byte 02h to ensure that the alarm setting matches the current clock mode. Bits designated with a 0 are a "don't care" on writes, but always read out as a 0.

User SRAM

The device has memory reserved for any purpose the user intends. The page is organized as 32 byte-wide locations. The SRAM space is formatted as shown in Table 6. It is accessed through the I²C protocol, 17h. If the R/$\overline{W}$ bit of the control byte is set to 1, the SRAM is read and a 0 in this location allows the master to write to the array. Reads or writes can be performed in the single byte or page mode. As such, the master must write the byte address of the first data location to be accessed.

Table 4. Thermostat Setpoint (TH/TL) Format in °C

SIGN	2^6	2^5	2^4	2^3	2^2	2^1	2^0	MSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	0	0	0	0	LSB
MSb	(for 10-bit conversions)	(for 11-bit conversions)	(for 12-bit conversions)				LSb	

Table 5. Clock Alarm Register Format

BYTE ADDRESS	BIT 7 MSb	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 1 LSb	BYTE RANGE
00h	0	10 Seconds			Seconds				00–59
01h	0	10 Minutes			Minutes				00–59
02h	0	0	AM/PM 10 Hours	10 Hours	Hours				01–12 00–23
03h	0	0	0	0	0	Day			01–07

If the bus master is writing to/reading from the SRAM array in the page mode (multiple byte mode), the address pointer automatically wraps from address 1Fh to 00h following the ACK after byte 1Fh.

The SRAM array does not have a defined power-up default state. See the *Command Set* section for details of the Access Memory protocol.

Configuration/Status Register

The Configuration/Status register is accessed through the Access Configuration (ACh) function command. Writing to or reading from the register is determined by the R/$\overline{W}$ bit of the I2C control byte (see the *I2C Serial Data Bus* section). Data is read from or written to the Configuration register MSb first. The format of the register is illustrated in Table 7. The effect each bit has on device functionality is described along with the power-up state and volatility. The user has read/write access to the MSB and read-only access to the LSB of the register.

1SH = Temperature Conversion Mode: If 1SHOT is 1, the device performs one temperature conversion upon reception of the Start Convert T protocol. If 1SHOT is 0, the device continuously performs temperature conversions and stores the last completed result in the Thermometer register. The user has read/write access to the nonvolatile bit, and the factory-default state is 0 (continuous mode).

POL = ALRM Polarity Bit: If POL = 1, the active state of the ALRM output will be high. A 0 stored in this location sets the thermostat output to an active-low state. The user has read/write access to the nonvolatile POL bit, and the factory-default state is 0 (active low).

CNV = Power-Up Conversion State: If CNV = 0 (factory default), the device automatically initiates a temperature conversion upon power-up and supply stability. Setting CNV = 1 causes the device to power up in a standby state. Table 8 illustrates how the user can set 1SH and CNV, depending on the power consumption sensitivity of the application.

A0, A1 = Alarm Mode: Table 9 defines the device alarm mode, based on the settings of the A0 and A1 bits. These bits define what event activates the ALRM output. The alarm flags (CAF, TAF, CAL, TAL) are functional regardless of the state of these bits. Both locations are read/write and nonvolatile, and the factory-default state disables the ALRM output (A0 = A1 = 0).

OS0, OS1 = Oscillator Output Setting: Table 10 defines the frequency of the OSC output, as defined by the settings of these bits. Both locations are read/write and nonvolatile, and the factory-default state sets the OSC frequency equal to the crystal frequency (OS0 = OS1 = 1). The output should be disabled if the user does not intend to use it to reduce power consumption.

Table 6. SRAM Format

BYTE	CONTENTS
00h	SRAM Byte 0
01h	SRAM Byte 1
02h	SRAM Byte 2
•••	•••
1Eh	SRAM Byte 30
1Fh	SRAM Byte 31

Table 7. Configuration/Status Register

EEPROM	OS1	OS0	A1	A0	0	CNV	POL	1SH	MSB
SRAM	CAF	TAF	CAL	TAL	0	0	0	0	LSB
	MSb							LSb	

Table 8. Thermometer Power-Up Modes

CNV	1SH	MODE
0	0	Powers up converting continuously (factory default).
0	1	Automatically performs one conversion upon power-up. Subsequent conversions require a Start Convert T command.
1	0	Powers up in standby; upon Start Convert T command, conversions are performed continuously.
1	1	Powers up in standby; upon Start Convert T command, a single conversion is performed and stored.

CAF = Clock Alarm Flag: This volatile status bit is set to 1 when the clock comparator is in an active state. Once set, it remains at 1 until reset by writing to or reading from either the Clock register or Clock Alarm register. A 0 in this location indicates the clock is not in an alarm condition. This is a read-only bit (writes to this location constitute a "don't care") and the power-up default is the flag cleared (CAF = 0).

TAF = Thermal Alarm Flag: This volatile status bit is set to 1 when the thermal comparator is in an active state. Once set, it remains at 1 until measured temperature falls below the programmed TL setting. A 0 in this location indicates the thermometer is not in an alarm condition. This is a read-only bit (writes to this location constitute a "don't care") and the power-up default is the flag cleared (TAF = 0).

CAL = Clock Alarm Latch: This volatile status bit is set to 1 when the clock comparator becomes active. Once set, it remains latched until the device power is cycled. A 0 in this location indicates the clock has never been in an alarm condition since the device was powered up. This is a read-only bit (writes to this location constitute a "don't care") and the power-up default is the flag cleared (CAL = 0).

TAL = Thermal Alarm Latch: This volatile status bit is set to 1 when the thermal comparator becomes active. Once set, it remains latched until the device power is cycled. A 0 in this location indicates the device temperature has never exceeded TH since power-up. This is a read-only bit (writes to this location constitute a "don't care") and the power-up default is the flag cleared (TAL = 0).

0 = Don't Care: "Don't care" on a write, but always reads out as a 0.

Resolution Register

The Resolution register is accessed through the Access Resolution (ADh) function command. Writing to or reading from the register is determined by the R/$\overline{W}$ bit of the I2C control byte (see the *I2C Serial Data Bus* section). Data is read from or written to the Configuration register MSb first. The format of the register is illustrated in Table 11. The resolution selection is shown in Table 12. The default value for the resolution is 12 bit. (R0 = R1 = 1).

Table 9. Alarm Mode Configuration

A1	A0	ALARM MODE
0	0	Neither thermal or time (disabled)
0	1	Thermal only
1	0	Time only
1	1	Either thermal or time

Table 10. OSC Frequency Configuration

OS1	OS0	OSC FREQUENCY
0	0	Disabled
0	1	1/8 f_0
1	0	1/4 f_0
1	1	f_0

Table 11. Resolution Register

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	R1	R0
MSb							LSb

Table 12. Resolution Configuration Settings

R1	R0	RESOLUTION (BITS)	TEMPERATURE RESOLUTION (°C)
0	0	9	0.5
0	1	10	0.25
1	0	11	0.125
1	1	12 (default)	0.0625

I²C Serial Data Bus

The device supports a bidirectional 2-wire bus and data-transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving the data is defined as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The MAX31629 operates as a slave on the I²C bus. Connections to the bus are made through the open-drain I/O lines (SDA and SCL).

The following bus protocol has been defined:

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy: Both data and clock lines remain high.

Start Data Transfer: A change in the state of the data line, from high to low, while the clock is high, defines a START condition.

Stop Data Transfer: A change in the state of the data line, from low to high, while the clock line is high, defines the STOP condition.

Data Valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a 9th bit. The maximum clock rate of the device is 400kHz.

Acknowledge: Each receiving device, when addressed, is obliged to generate an “acknowledge” (ACK) after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition. Figure 3 details how data transfer is accomplished on the 2-wire bus.

Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data Transfer from a Master Transmitter to a Slave Receiver:** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2) **Data Transfer from a Slave Transmitter to a Master Receiver:** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” (NACK) is returned. The master device generates all the serial-clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

The MAX31629 can operate in the following two modes:

1) **Slave Receiver Mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2) **Slave Transmitter Mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the device while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Slave Address

A control byte is the first byte received following the START condition from the master device. The control byte has the value of 9Eh. Thus, only one MAX31629 can reside on an I²C bus to avoid contention; however, as many as seven other devices with the 1001 control code can be dropped on the I²C bus so long as none contain the 111 address. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a 1, a read operation is selected; when set to a 0, a write operation is selected. Following the START condition, the MAX31629 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the control byte, the slave device outputs an ACK on the SDA line.

Command Set

The command set for the MAX31629, as shown in Table 13, is as follows:

Access Configuration (ACh)

If R/$\overline{W}$ is 0, this command writes to the Configuration/Status register. After issuing this command, the next data byte value is to be written into the Configuration/Status register. If R/$\overline{W}$ is 1, the next data byte read is the value stored in the Configuration/Status register. Because the MSB of the Configuration/Status register is read/write and the LSB is read-only, the user only needs to write 1 byte to the register. Either 1 or 2 bytes can be read.

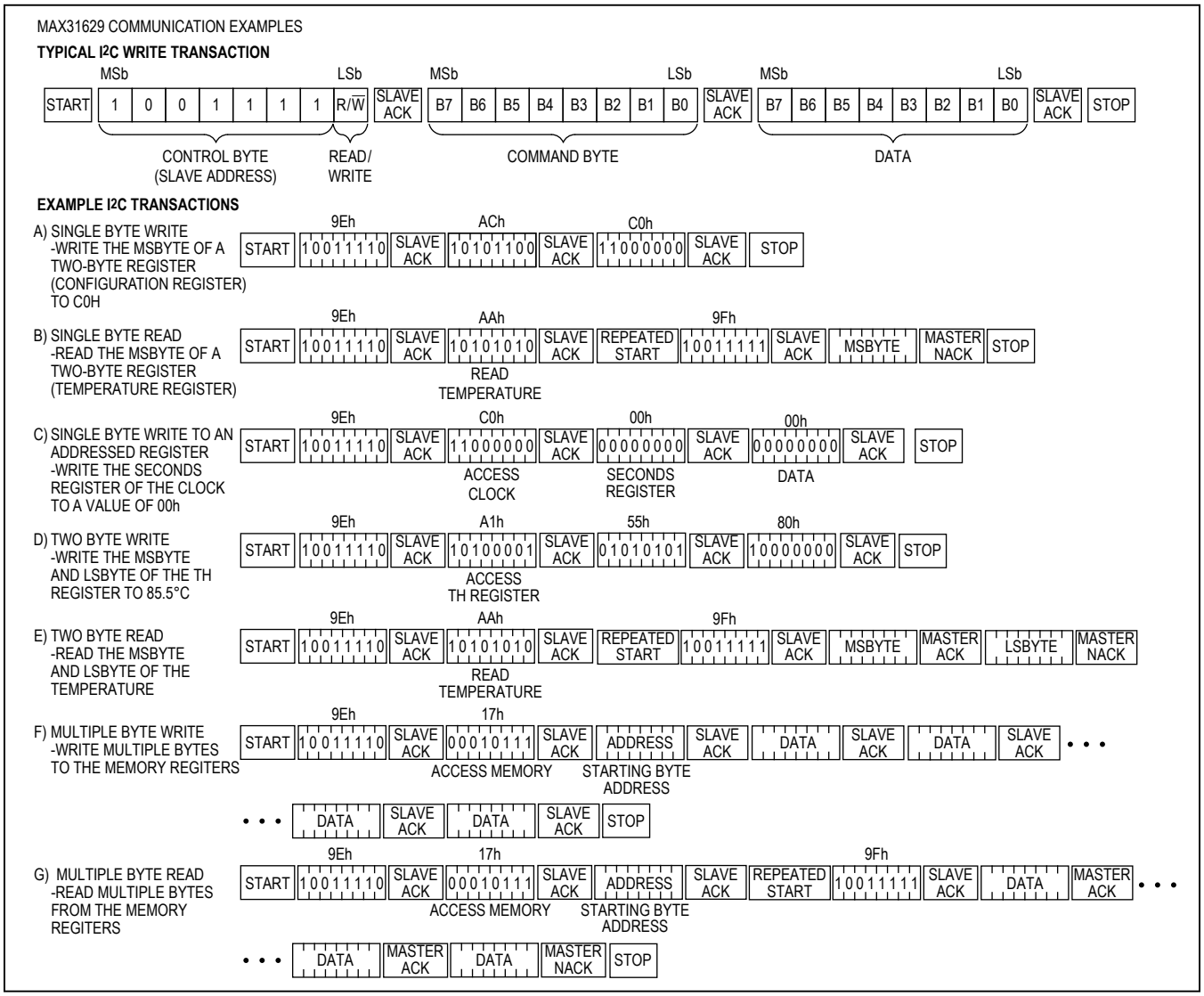


Figure 3. I²C Serial Communication Examples

Access Resolution (ADh)

If R/$\overline{W}$ is 0, this command writes to the Resolution register. After issuing this command, the next data byte value is to be written into the Resolution register. If R/$\overline{W}$ is 1, the next data byte read is the value stored in the Resolution register.

Start Convert T (EEh)

This command begins a temperature conversion. No further data is required. In one-shot mode, the temperature conversion is performed and then the device remains idle. In continuous mode, this command initiates continuous conversions. Issuance of this protocol might not be required upon device power-up, depending on the state of the CNV bit in the Configuration register.

Stop Convert T (22h)

This command stops temperature conversion. No further data is required. This command can be used to halt a MAX31629 in continuous-conversion mode. After issuing this command, the current temperature measurement is completed, and the device remains idle until a Start Convert T is issued to resume conversions.

Read Temperature (AAh)

This command reads the last temperature conversion result from the Thermometer register in the format described in the *Measuring Temperature* section. If one's application can only accept thermometer resolution of 1.0°C, the master must only read the first data byte and follow with a NACK and STOP. For higher resolution, both bytes must be read.

Access Clock (C0h)

Accesses the device's Clock/Calendar register. If R/$\overline{W}$ is 0, the master writes to the Clock register (sets the clock). If R/$\overline{W}$ is 1, the Clock register is read. The Clock register is addressed, so the user must provide a beginning byte address, whether a read or write is performed. A write to or read from this register or the Clock Alarm register is required to clear the clock alarm flag (CAF). See Figure 3 for the protocol and Table 3 for the Clock register map.

Access Clock Alarm (C7h)

Accesses the device's Clock Alarm register. If R/$\overline{W}$ is 0, the master writes to the Clock Alarm register (set/change the alarm). If R/$\overline{W}$ is 1, the Clock Alarm register is read. The Clock Alarm register is addressed, so the user must provide a beginning byte address, whether a read or write is performed. A write to or read from this register or the Clock register is required to clear the clock alarm flag (CAF). See Figure 3 for the protocol and Table 5 for the Clock Alarm register map.

Access TH (A1h)

If R/$\overline{W}$ is 0, this command writes to the TH register. After issuing this command, the next two bytes written to the device, in the format described for thermostat set points, set the high-temperature threshold for operation of the ALRM output and TAF/TAL flags. If R/$\overline{W}$ is 1, the value stored in this register is read back.

Access TL (A2h)

If R/$\overline{W}$ is 0, this command writes to the TL register. After issuing this command, the next two bytes written to the device, in the format described for thermostat set points, sets the low-temperature threshold for operation of the ALRM output and TAF flag. If R/$\overline{W}$ is 1, the value stored in this register is read back.

Access Memory (17h)

This command instructs the device to access the user SRAM array, starting with the specified byte address. Read/write depends upon the state of the R/$\overline{W}$ in the I2C control byte. The user can read/write all 32 bytes in succession within one command sequence, with the pointer automatically incrementing. If the master attempts to read/write more than 32 bytes, the address pointer wraps to the 1st byte (00h) after the 32nd byte (1Fh) is read/written and ACK'd by the master/slave. See Figure 3 for command protocol.

Table 13. Command Set

INSTRUCTION	PROTOCOL	DESCRIPTION	DATA AFTER ISSUING PROTOCOL	NOTES
CONFIGURATION/MEMORY COMMANDS				
Access Configuration	ACh	Writes to 8-bit Configuration register	1 data byte	11, 15
		Reads from Configuration/Status registers	1 or 2 data bytes	
Access Resolution	ADh	Writes to 8-bit Resolution register	1 data byte	11, 15
Access Memory	17h	Writes to SRAM array	Starting address + N - bytes	11, 12
		Reads from SRAM array	Starting address + N - bytes	
THERMOMETER COMMANDS				
Start Convert T	EEh	Initiates temperature conversion(s)	Idle	13
Stop Convert T	22h	Terminates continuous conversions	Idle	13
Read Temperature	AAh	Reads Temperature register	Read 1 or 2 data bytes	14
Access TH	A1h	Writes to/reads from TH register	Write 2 data bytes or read 2 data bytes	11, 15
Access TL	A2h	Writes to/reads from TL register	Write 2 data bytes or read 2 data bytes	11, 15
CLOCK COMMANDS				
Access Clock	C0h	Sets/reads Clock registers	Starting address + N - bytes	11, 12
Access Clock Alarm	C7h	Sets/reads Clock Alarm registers	Starting address + N - bytes	11, 12

Note 11: Data direction depends on the R/$\overline{W}$ bit in the I2C control byte.

Note 12: When accessing (reading from or writing to) addressed SRAM in the page mode, the address pointer automatically rolls from the most significant byte to the least significant byte following the ACK of the most significant byte.

Note 13: In continuous-conversion mode, a Stop Convert T command halts continuous conversion. To restart, the Start Convert T command must be issued. In one-shot mode, a Start Convert T command must be issued for every temperature reading desired.

Note 14: If the user only desires 8-bit thermometer resolution, the master need only read 1 data byte, and follow with a NACK and STOP. If higher resolution is required, 2 bytes must be read.

Note 15: Writing to EEPROM registers typically requires 10ms at room temperature (50ms max). After issuing a write command, no further writes should be requested for 50ms. EEPROM writes should only occur under the conditions $2.7V \le V_{DD} \le 5.5V$ and $0°C \le T_A \le 70°C$.

Sample Command Sequence No. 1

Example: The bus master configures the device in the power-up one-shot mode. It sets the ALRM output active low with only the thermometer generating an ALRM and disables the oscillator output. It then sets the clock to 11:30AM on Tuesday, January 1, 2013. It sets the thermostat with TH = 50°C. See Table 14.

Sample Command Sequence No. 2

Example: Assuming the device is configured such that the clock is running and the thermometer is converting, read the current time and temperature. Also read the status of the alarm flags. See Table 15.

Table 14. Sample Command Sequence No. 1

BUS MASTER MODE	DEVICE MODE	DATA (MSB FIRST)	COMMENTS
TX	RX	START	Bus master initiates a START condition
TX	RX	9Eh	Bus master sends device address; R/$\overline{W}$ = 0
RX	TX	ACK	Device generates acknowledge bit
TX	RX	ACh	Bus master sends access configuration protocol
RX	TX	ACK	Device generates acknowledge bit
TX	RX	11h	Write to configuration as specified
RX	TX	ACK	Device generates acknowledge bit
TX	RX	START	Bus master initiates a repeated START condition
TX	RX	9Eh	Bus master sends device address; R/$\overline{W}$ = 0
RX	TX	ACK	Device generates acknowledge bit
TX	RX	C0h	Bus master sends access clock protocol
RX	TX	ACK	Device generates acknowledge bit
TX	RX	00h	Bus master sends starting clock register address
RX	TX	ACK	Device generates acknowledge bit
TX	RX	00h	Bus master sets seconds and enables the clock
RX	TX	ACK	Device generates acknowledge bit
TX	RX	30h	Bus master sets clock minutes
RX	TX	ACK	Device generates acknowledge bit
TX	RX	51h	Bus master sets clock hours and AM/PM clock mode
RX	TX	ACK	Device generates acknowledge bit
TX	RX	05h	Bus master sets day to Thursday
RX	TX	ACK	Device generates acknowledge bit
TX	RX	01h	Bus master sets date to the first of the month
RX	TX	ACK	Device generates acknowledge bit
TX	RX	01h	Bus master sets month to January
RX	TX	ACK	Device generates acknowledge bit
TX	RX	98h	Bus master sets year to 1998
RX	TX	ACK	Device generates acknowledge bit
TX	RX	START	Bus master initiates a repeated START condition
TX	RX	9Eh	Bus master sends device address; R/$\overline{W}$ = 0
RX	TX	ACK	Device generates acknowledge bit
TX	RX	A1h	Bus master sends access TH protocol
RX	TX	ACK	Device generates acknowledge bit
TX	RX	32h	Bus master writes MSB of TH (50°C)
RX	TX	ACK	Device generates acknowledge bit
TX	RX	00h	Bus master writes LSB of TH (50°C)
RX	TX	ACK	Device generates acknowledge bit
TX	RX	STOP	Bus master initiates STOP condition

Table 15. Sample Command Sequence No. 2

BUS MASTER MODE	DEVICE MODE	DATA (MSB FIRST)	COMMENTS
TX	RX	START	Bus master initiates a START condition
TX	RX	9Eh	Bus master sends device address; R/$\overline{W}$ = 0
RX	TX	ACK	Device generates acknowledge bit
TX	RX	AAh	Bus master sends read temperature protocol
RX	TX	ACK	Device generates acknowledge bit
TX	RX	START	Bus master initiates a Repeated START condition
TX	RX	9Fh	Bus master sends device address; R/$\overline{W}$ = 1
RX	TX	ACK	Device generates acknowledge bit
RX	TX	<data byte>	Device generates MSB of temperature
TX	RX	ACK	Bus master generates acknowledge bit
RX	TX	<data byte>	Device generates LSB of temperature
TX	RX	NACK	Master generates no-acknowledge bit
TX	RX	START	Bus master initiates a repeated START condition
TX	RX	9Eh	Bus master sends device address; R/$\overline{W}$ = 0
RX	TX	ACK	Device generates acknowledge bit
TX	RX	C0h	Bus master sends access clock protocol
RX	TX	ACK	Device generates acknowledge bit
TX	RX	01h	Bus master set clock register address to “minutes”
RX	TX	ACK	Device generates acknowledge bit
TX	RX	START	Bus master initiates a Repeated START condition
TX	RX	9Fh	Bus master sends device address; R/$\overline{W}$ = 1
RX	TX	ACK	Device generates acknowledge bit
RX	TX	<data byte>	Device generates minutes
TX	RX	ACK	Bus master generates acknowledge bit
RX	TX	<data byte>	Device generates hours and clock mode
TX	RX	ACK	Bus master generates acknowledge bit
•	•	•	•
RX	TX	<data byte>	Device generates year
TX	RX	NACK	Master generates no-acknowledge bit
TX	RX	START	Bus master initiates a repeated START condition
TX	RX	9Eh	Bus master sends device address; R/$\overline{W}$ = 0
RX	TX	ACK	Device generates acknowledge bit
TX	RX	ACh	Bus master sends access configuration protocol
RX	TX	ACK	Device generates acknowledge bit
TX	RX	9Fh	Bus master sends device address; R/$\overline{W}$ = 1
RX	TX	ACK	Device generates acknowledge bit
RX	TX	<data byte>	Device generates MSB of Configuration register
TX	RX	ACK	Master generates acknowledge bit
RX	TX	<data byte>	Device generates LSB of Configuration register (flags)
TX	RX	NACK	Master generates no-acknowledge bit
TX	RX	STOP	Bus master initiates STOP condition

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX31629MTA+	-55°C to +125°C	8 TDFN-EP*
MAX31629MTA+T	-55°C to +125°C	8 TDFN-EP*

+Denotes a lead (Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN-EP	T833+2	21-0137	90-0059

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/14	Initial release	—
1	12/14	Updated *Benefits and Features* section	1

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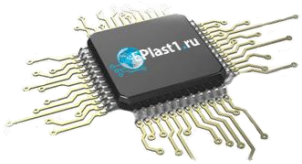
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.