LC²MOS Dual, Complete, 12-Bit/14-Bit Serial DACs

AD7244

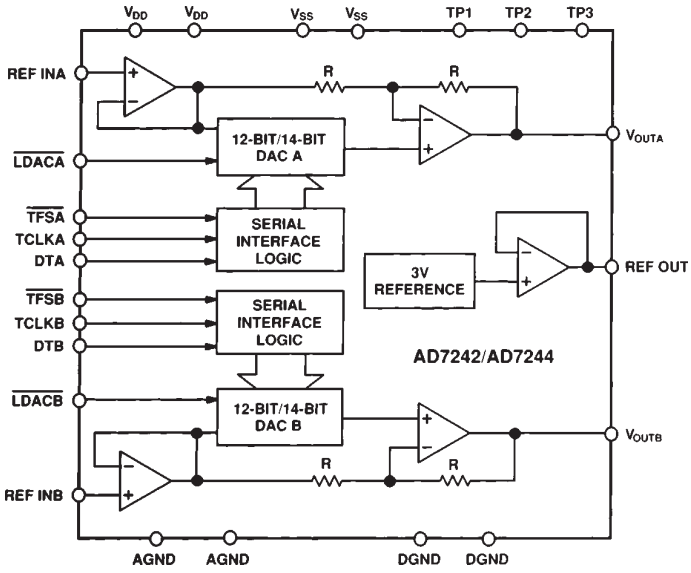
FEATURES

Two 12-Bit/14-Bit DACs with Output Amplifiers
- **AD7242: 12-Bit Resolution**
- **AD7244: 14-Bit Resolution**

On-Chip Voltage Reference
Fast Settling Time
- **AD7242: 3 μs to ±1/2 LSB**
- **AD7244: 4 μs to ±1/2 LSB**

High Speed Serial Interface
Operates from ±5 V Supplies
Specified Over –40°C to +85°C in Plastic Packages
Low Power – 130 mW typ
AD7242 is obsolete

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7242/AD7244 is a fast, complete, dual 12-bit/14-bit voltage output D/A converter. It consists of a 12-bit/14-bit DAC, 3 V buried Zener reference, DAC output amplifiers and high speed serial interface logic.

Interfacing to both DACs is serial, minimizing pin count and allowing a small package size. Standard control signals allow interfacing to most DSP processors and microcontrollers. Asynchronous control of DAC updating for both DACs is made possible with a separate $\overline{\text{LDAC}}$ input for each DAC.

The AD7242/AD7244 operates from ±5 V power supplies, providing an analog output range of ±3 V. A REF OUT/REF IN function allows the DACs to be driven from the on-chip 3 V reference or from an external reference source.

The AD7242/AD7244 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced mixed technology process that combines precision bipolar circuits with low power CMOS logic. Both parts are available in a 24-pin, 0.3-inch wide, plastic or hermetic dual-in-line package (DIP) and in a 28-pin, plastic small outline (SOIC) package. The AD7242 and AD7244 are available in the same pinout to allow easy upgrade from 12-bit to 14-bit performance.

PRODUCT HIGHLIGHTS

1. Complete, Dual 12-Bit/14-Bit DACs
   The AD7242/AD7244 provides the complete function for generating voltages to 12-bit/14-bit resolution. The part features an on-chip reference, output buffer amplifiers and two 12-bit/14-bit D/A converters.
2. High Speed Serial Interface
   The AD7242/AD7244 provides a high speed, easy-to-use, serial interface allowing direct interfacing to DSP processors and microcontrollers. A separate serial port is provided for each DAC.
3. Small Package Size
   The AD7242/AD7244 is available in a 24-pin DIP and a 28-pin SOIC package offering considerable space saving over comparable solutions.

The AD7242 is no longer available.

REV. B

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AD7242/AD7244–SPECIFICATIONS (V_{DD} = +5 V ± 5% V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, REF INA = REF INB = +3 V. V_{OUTA}, V_{OUTB} load to AGND: R_L = 2 kΩ, C_L = 100 pF.

All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	AD7242 J, A Versions[1]	AD7242 K, B Versions[1]	Units	Test Conditions/Comments
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±5	±5	LSB max	
Positive Full-Scale Error[2]	±5	±5	LSB max	
Negative Full-Scale Error[2]	±5	±5	LSB max	
REFERENCE OUTPUT[3]				
REF OUT @ +25°C	2.99/3.01	2.99/3.01	V min/V max	
T_{MIN} to T_{MAX}	2.98/3.02	2.98/3.02	V min/V max	
REF OUT Tempco	35	35	ppm/°C typ	
Reference Load Change (ΔREF OUT vs. ΔI)	–1	–1	mV max	Reference Load Current Change (0 μA–500 μA)
REFERENCE INPUTS				
REF INA, REF INB Input Range	2.85/3.15	2.85/3.15	V min/V max	3 V ± 5%
Input Current	1	1	μA max	
LOGIC INPUTS ($\overline{LDACA}$, $\overline{LDACB}$, $\overline{TFSA}$, $\overline{TFSB}$, TCLKA, TCLKB, DTA, DTB)				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
ANALOG OUTPUTS (V_{OUTA}, V_{OUTB})				
Output Voltage Range	±3	±3	V nom	
DC Output Impedance	0.1	0.1	Ω typ	
Short Circuit Current	20	20	mA typ	
AC CHARACTERISTICS[4]				
Voltage Output Settling Time				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	3	3	μs max	Typically 2 μs
Negative Full-Scale Change	3	3	μs max	Typically 2 μs
Digital-to-Analog Glitch Impulse	10	10	nV secs typ	DAC Code Change All 1s to All 0s
Digital Feedthrough	2	2	nV secs typ	
Channel-to-Channel Isolation	110	110	dB typ	V_{OUT} = 10 kHz Sine Wave
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	V nom	±5% for Specified Performance
I_{DD}	27	27	mA max	Cumulative Current from the Two V_{DD} Pins
I_{SS}	15	15	mA max	Cumulative Current from the Two V_{SS} Pins
Total Power Dissipation	195	195	mW max	Typically 130 mW

NOTES

[1]Temperature ranges are as follows: J, K Versions: –40°C to +85°C; A, B Versions: –40°C to +85°C.

[2]Measured with respect to REF IN and includes bipolar offset error.

[3]For capacitive loads greater than 50 pF, a series resistor is required (see Internal Reference section).

[4]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

Parameter	AD7244 J, A Versions[1]	AD7244 S Version[1]	Units	Test Conditions/Comments
DC ACCURACY				
Resolution	14	14	Bits	
Integral Nonlinearity	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±10	±10	LSB max	
Positive Full-Scale Error[2]	±10	±10	LSB max	
Negative Full-Scale Error[2]	±10	±10	LSB max	
REFERENCE OUTPUT[3]				
REF OUT @ +25°C	2.99/3.01	2.99/3.01	V min/V max	
T_{MIN} to T_{MAX}	2.98/3.02	2.98/3.02	V min/V max	
REF OUT Tempco	35	35	ppm/°C typ	
Reference Load Change				
(ΔREF OUT vs. ΔI)	–1	–1	mV max	Reference Load Current Change (0 μA–500 μA)
REFERENCE INPUTS				
REF INA, REF INB Input Range	2.85/3.15	2.85/3.15	V min/V max	3 V ± 5%
Input Current	1	1	μA max	
LOGIC INPUTS				
($\overline{LDACA}$, $\overline{LDACB}$, $\overline{TFSA}$, $\overline{TFSB}$,				
TCLKA, TCLKB, DTA, DTB)				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
ANALOG OUTPUTS				
(V_{OUTA}, V_{OUTB})				
Output Voltage Range	±3	±3	V nom	
DC Output Impedance	0.1	0.1	Ω typ	
Short Circuit Current	20	20	mA typ	
AC CHARACTERISTICS[4]				
Voltage Output Settling Time				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	4	4	μs max	Typically 2.5 μs
Negative Full-Scale Change	4	4	μs max	Typically 2.5 μs
Digital-to-Analog Glitch Impulse	10	10	nV secs typ	DAC Code Change All 1s to All 0s
Digital Feedthrough	2	2	nV secs typ	
Channel-to-Channel Isolation	110	110	dB typ	V_{OUT} = 10 kHz Sine Wave
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	V nom	±5% for Specified Performance
I_{DD}	27	28	mA max	Cumulative Current from the Two V_{DD} Pins
I_{SS}	15	15	mA max	Cumulative Current from the Two V_{SS} Pins
Total Power Dissipation	195	205	mW max	Typically 130 mW

NOTES
[1]Temperature ranges are as follows: J Version: 0°C to +70°C; A Version: –40°C to +85°C; S Version: –55°C to +125°C.
[2]Measured with respect to REF IN and includes bipolar offset error.
[3]For capacitive loads greater than 50 pF, a series resistor is required (see Internal Reference section).
[4]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V)

Parameter	Limit at T_{MIN}, T_{MAX} (J, K, A, B Versions)	Limit at T_{MIN}, T_{MAX} (S Version)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{TFS}$ to TCLK Falling Edge
t_2	75	100	ns min	TCLK Falling Edge to $\overline{TFS}$
t_3[3]	150	200	ns min	TCLK Cycle Time
t_4	30	40	ns min	Data Valid to TCLK Setup Time
t_5	75	100	ns min	Data Valid to TCLK Hold Time
t_6	40	40	ns min	$\overline{LDAC}$ Pulse Width

NOTES
[1]Timing specifications are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figure 6.
[3]TCLK Mark/Space ratio is 40/60 to 60/40.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

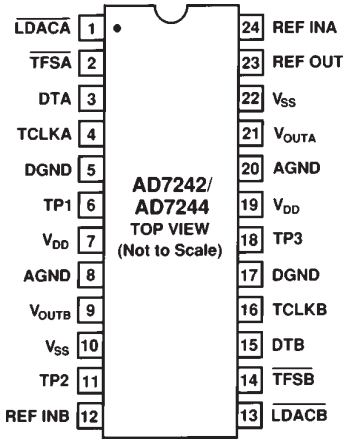
V_{DD} to AGND ..... –0.3 V to +7 V
V_{SS} to AGND ..... +0.3 V to –7 V
AGND to DGND ..... –0.3 V to V_{DD} + 0.3 V
V_{OUT} to AGND ..... V_{SS} to V_{DD}
REF OUT to AGND ..... –0.3 V to V_{DD} + 0.3 V
REF INA, REF INB to AGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Inputs to DGND ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
J, K Versions
AD7244 ..... 0°C to +70°C
AD7242 ..... –40°C to +85°C
A, B Versions ..... –40°C to +85°C
S Version ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Power Dissipation (Any Package) to +75°C ..... 550 mW
Derates above +75°C by ..... 6 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

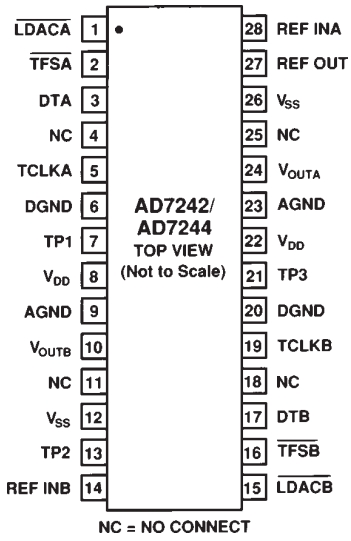
CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7242/AD7244 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

DIP



SOIC



AD7242/AD7244 PIN FUNCTION DESCRIPTION

DIP Pin No.	Mnemonic	Description
1	$\overline{\text{LDACA}}$	Load DAC, Logic Input. A new word is transferred into DAC Latch A from input Latch A on the falling edge of this signal. If $\overline{\text{LDACA}}$ is hard-wired low, data is transferred from input Latch A to DAC Latch A on the sixteenth falling edge of TCLKA after $\overline{\text{TFSA}}$ goes low.
2	$\overline{\text{TFSA}}$	Transmit Frame Synchronization, Logic Input. This is a frame or synchronization signal for DACA data with serial data expected after the falling edge of this signal.
3	DTA	Transmit Data, Logic Input. This is the data input which is used in conjunction with $\overline{\text{TFSA}}$ and TCLKA to transfer serial data to input Latch A.
4	TCLKA	Transmit Clock, Logic Input. Serial data bits for DACA are latched on the falling edge of TCLKA when $\overline{\text{TFSA}}$ is low.
5	DGND	Digital Ground. Both DGND pins for the device must be tied together at the device.
6	TP1	Test Pin 1. Used when testing the device. Do not connect anything to this pin.
7	V_{DD}	Positive Power Supply, 5 V ± 5%. Both V_{DD} pins for the device must be tied together at the device.
8	AGND	Analog Ground. Both AGND pins for the device must be tied together at the device.
9	V_{OUTB}	Analog Output Voltage from DACB. This output comes from a buffer amplifier. The range is bipolar, ±3 V with REF INB = +3 V.
10	V_{SS}	Negative Power Supply, –5 V ± 5%. Both V_{SS} pins for the device must be tied together at the device.
11	TP2	Test Pin 2. Used when testing the device. Do not connect anything to this pin.
12	REF INB	DACB Voltage Reference Input. The voltage reference for DACB is applied to this pin. It is internally buffered before being applied to DACB. The nominal reference voltage for correct operation of the AD7242/AD7244 is 3 V.
13	$\overline{\text{LDACB}}$	Load DAC, Logic Input. A new word is transferred into DAC Latch B from input Latch B on the falling edge of this signal. If $\overline{\text{LDACB}}$ is hard-wired low, data is transferred from input Latch B to DAC Latch B on the sixteenth falling edge of TCLKB after $\overline{\text{TFSB}}$ goes low.
14	$\overline{\text{TFSB}}$	Transmit Frame Synchronization, Logic Input. This is a frame or synchronization signal for DACB data with serial data expected after the falling edge of this signal.
15	DTB	Transmit Data, Logic Input. This is the data input used in conjunction with $\overline{\text{TFSB}}$ and TCLKB to transfer serial data to input Latch B.
16	TCLKB	Transmit Clock, Logic Input. Serial data bits for DACB are latched on the falling edge of TCLKB when $\overline{\text{TFSB}}$ is low.
17	DGND	Digital Ground. Both DGND pins for the device must be tied together at the device.
18	TP3	Test Pin 3. Used when testing the device. Do not connect anything to this pin.
19	V_{DD}	Positive Power Supply, 5 V ± 5%. Both V_{DD} pins for the device must be tied together at the device.
20	AGND	Analog Ground. Both AGND pins for the device must be tied together at the device.
21	V_{OUTA}	Analog Output Voltage from DACA. This output comes from a buffer amplifier. The range is bipolar, ±3 V with REF INA = +3 V.
22	V_{SS}	Negative Power Supply, –5 V ± 5%. Both V_{SS} pins for the device must be tied together at the device.
23	REF OUT	Voltage Reference Output. To operate the DACs with this internal reference, REF OUT should be connected to both REF INA and REF INB. The external load capability of the reference is 500 μA.
24	REF INA	DACA Voltage Reference Input. The voltage reference for DACA is applied to this pin. It is internally buffered before being applied to DACA. The nominal reference voltage for correct operation of the AD7242/AD7244 is 3 V.

CIRCUIT DESCRIPTION

The AD7242/AD7244 contains two 12-bit/14-bit D/A converters, each with an output buffer amplifier. The part also contains a reference input buffer amplifier for each DAC, and an on-chip 3 V reference.

D/A Section

The AD7242/AD7244 contains two 12-bit/14-bit voltage mode D/A converters, each consisting of highly stable thin-film resistors and high speed single-pole, double-throw switches. The simplified circuit diagram for the DAC section is shown in Figure 1. The three MSBs of the data word are decoded to drive the seven switches A-G. On the AD7242, the 9 LSBs switch a 9-bit R-2R ladder structure while on the AD7244, the 11 LSBs switch an 11-bit R-2R ladder structure. The output voltage from this converter has the same polarity as the reference voltage, REF IN.

The REF IN voltage is internally buffered by a unity gain amplifier before being applied to the D/A converters and the bipolar bias circuitry. The D/A converter is configured and scaled for a 3 V reference, and the device is tested with 3 V applied to REF IN. Operating the AD7242/AD7244 at reference voltages outside the ±5% tolerance range may result in degraded performance from the part.

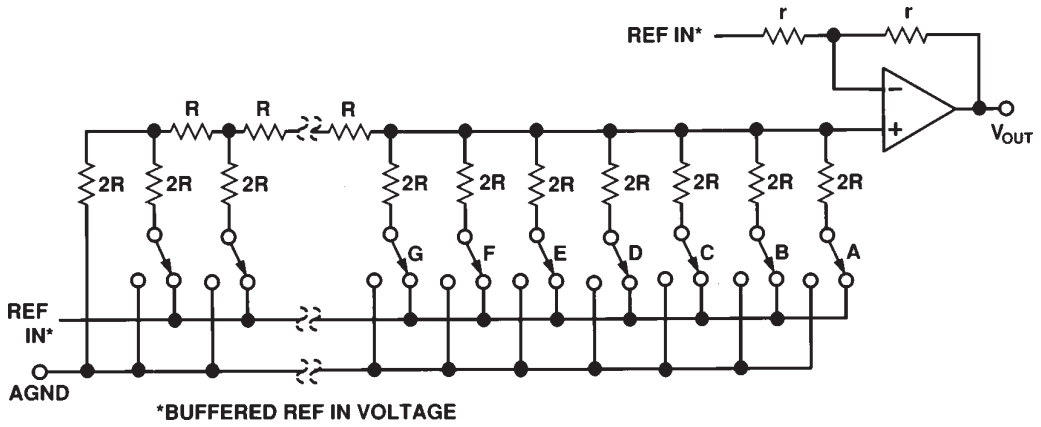


Figure 1. DAC Ladder Structure

Internal Reference

The on-chip reference is a temperature-compensated buried Zener reference that is factory trimmed for 3 V ± 10 mV. The reference can be used to provide both the reference voltage for the two D/A converters and the bipolar biasing circuitry. This is achieved by connecting REF OUT to REF INA and REF INB.

The reference voltage can also be used for other components and is capable of providing up to 500 µA to an external load. The maximum recommended capacitance on the reference output pin for normal operation is 50 pF. If the reference output is required to drive a capacitive load greater than 50 pF, a 200 Ω resistor should be placed in series with the capacitive load. Decoupling the REF OUT pin with a series 200 Ω resistor and a parallel combination of a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor as in Figure 2 reduces the noise spectral density of the reference (see Figure 4). Using this decoupling scheme to generate the reference voltage for REF INA and REF INB gives a channel-to-channel isolation number of 110 dB (connecting REF OUT directly to REF INA and REF INB gives 80 dB). The channel-to-channel isolation is 110 dB using an external reference.

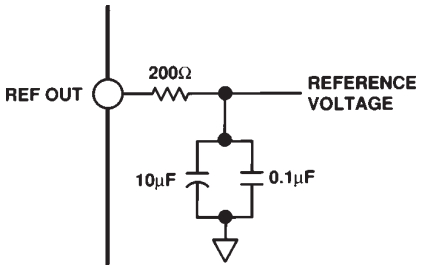


Figure 2. Circuit Connection for REF OUT with an External Capacitive Load of Greater Than 50 pF

External Reference

In some applications, the user may require a system reference or some other external reference to drive the AD7242/AD7244 reference inputs. Figure 3 shows how the AD586 reference can be conditioned to provide the 3 V reference required by the AD7242/AD7244 reference inputs.

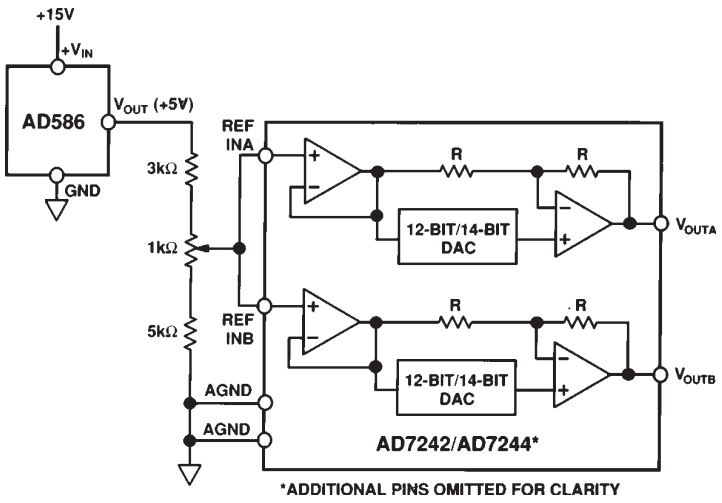


Figure 3. AD586 Driving AD7242/AD7244 Reference Inputs

Output Amplifier

The outputs from each of the voltage-mode DACs are buffered by a noninverting amplifier. The buffer amplifier is capable of developing ±3 V across a 2 kΩ and 100 pF load to ground, and can produce 6 V peak-to-peak sine wave signals to a frequency of 20 kHz. The output is updated on the falling edge of the respective $\overline{\text{LDAC}}$ input. The output voltage settling time, to within 1/2 LSB of its final value, is typically less than 2 µs for the AD7242 and 2.5 µs for the AD7244.

The small signal (200 mV p-p) bandwidth of the output buffer amplifier is typically 1 MHz. The output noise from the amplifier is low, with a figure of 30 nV/√Hz at a frequency of 1 kHz. The broadband noise from the amplifier exhibits a typical peak-to-peak figure of 150 µV for a 1 MHz output bandwidth. Figure 4 shows a typical plot of noise spectral density versus frequency for the output buffer amplifier and for the on-chip reference (including and excluding the decoupling components).

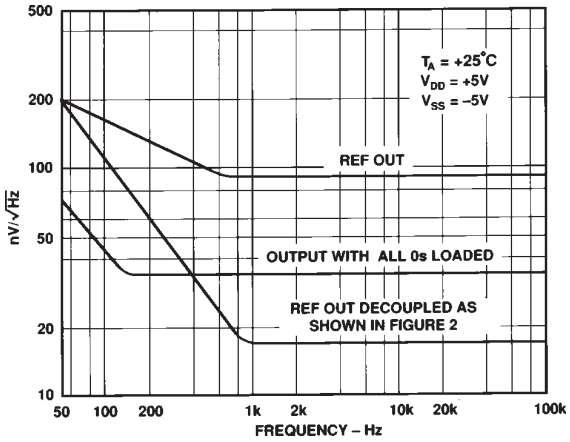


Figure 4. Noise Spectral Density vs. Frequency

TRANSFER FUNCTION

The basic circuit configuration for the AD7242/AD7244 is shown in Figure 5. Table I and Table II show the ideal input code to output voltage relationship for the AD7242 and AD7244 respectively. Input coding for the AD7242/AD7244 is 2s complement.

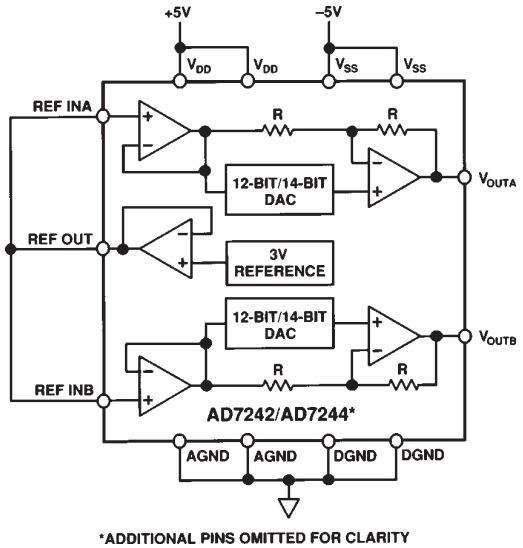


Figure 5. Basic Connection Diagram

For the AD7242, the output voltage can be expressed in terms of the input code, *N*, using the following relationship:

$$V_{OUT} = \frac{2 \bullet N \bullet REF\ IN}{4096}$$

where $-2048 \le N \le +2047$

For the AD7244, the output voltage can be expressed in terms of the input code, *N*, using the following relationship:

$$V_{OUT} = \frac{2 \bullet N \bullet REF\ IN}{16384}$$

where $-8192 \le N \le +8191$

Table I. AD7242 Ideal Input/Output Code Table Code

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}*
01 11 1111 1111	+2.998535 V
01 11 1111 1110	+2.99707 V
00 00 0000 0001	+0.001465 V
00 00 0000 0000	0 V
11 11 1111 1111	–0.001465 V
10 00 0000 0001	–2.998535 V
10 00 0000 0000	–3 V

*Assuming REF IN = +3 V.

Table II. AD7244 Ideal Input/Output Code Table Code

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}*
01 1111 1111 1111	+2.999634 V
01 1111 1111 1110	+2.99268 V
00 0000 0000 0001	+0.000366 V
00 0000 0000 0000	0 V
11 1111 1111 1111	–0.000366 V
10 0000 0000 0001	–2.999634 V
10 0000 0000 0000	–3 V

*Assuming REF IN = +3 V.

TIMING AND CONTROL

Communication with the AD7242/AD7244 is via six serial logic inputs. These consist of separate serial clocks, word framing and data lines for each DAC. DAC updating is controlled by two digital inputs: $\overline{\text{LDACA}}$ for updating V_{OUTA} and $\overline{\text{LDACB}}$ for updating V_{OUTB}. These inputs can be asserted independently of the microprocessor by an external timer when precise updating intervals are required. Alternatively, the $\overline{\text{LDACA}}$ and $\overline{\text{LDACB}}$ inputs can be driven from a decoded address bus allowing the microprocessor control over DAC updating as well as data communication to the AD7242/AD7244 input latches.

The AD7242/AD7244 contains two latches per DAC, an input latch and a DAC latch. Data must be loaded to the input latch under the control of TCLKA, $\overline{\text{TFSA}}$ and DTA for input Latch A and TCLKB, $\overline{\text{TFSB}}$ and DTB for input Latch B. Data is then transferred from input Latch A to DAC Latch A under the control of the $\overline{\text{LDACA}}$ signal, while $\overline{\text{LDACB}}$ controls the loading of DAC Latch B from input Latch B. Only the data held in the DAC latches determines the analog outputs of the AD7242/AD7244.

Data is loaded to the input latches under control of the respective TCLK, $\overline{\text{TFS}}$ and DT signals. The AD7242/AD7244 expects a 16-bit stream of serial data on its DT inputs. Data must be valid on the falling edge of TCLK. The $\overline{\text{TFS}}$ input provides the frame synchronization signal that tells the AD7242/AD7244 that valid serial data will be available on the DT input for the next 16 falling edges of TCLK. Figure 6 shows the timing diagram for operation of either of the two serial input ports on the part.

Although 16 bits of data are clocked into the input latch, only 12 bits are transferred into the DAC latch for the AD7242 and 14 bits are transferred for the AD7244. Therefore, 4 bits in the AD7242 data stream and 2 bits in the AD7244 data stream are don't cares since their value does not affect the DAC latch data. The bit positions are the don't cares followed by the DAC data starting with the MSB (see Figure 6).

The respective $\overline{\text{LDAC}}$ signals control the transfer of data to the respective DAC latches. Normally, data is loaded to the DAC latch on the falling edge of $\overline{\text{LDAC}}$. However, if $\overline{\text{LDAC}}$ is held low, serial data is loaded to the DAC latch on the sixteenth falling edge of TCLK. If $\overline{\text{LDAC}}$ goes low during the loading of serial data to the input latch, no DAC latch update takes place on the falling edge of $\overline{\text{LDAC}}$. If $\overline{\text{LDAC}}$ stays low until the serial transfer is completed, then the update takes place on the sixteenth falling edge of TCLK. If $\overline{\text{LDAC}}$ returns high before the serial data transfer is completed, no DAC latch update takes place.

If seventeen or more TCLK edges occur while $\overline{\text{TFS}}$ is low, the seventeenth (and beyond) clock edges are ignored, i.e., no further data is clocked into the input latch after the sixteenth TCLK edge following a falling edge on $\overline{\text{TFS}}$.

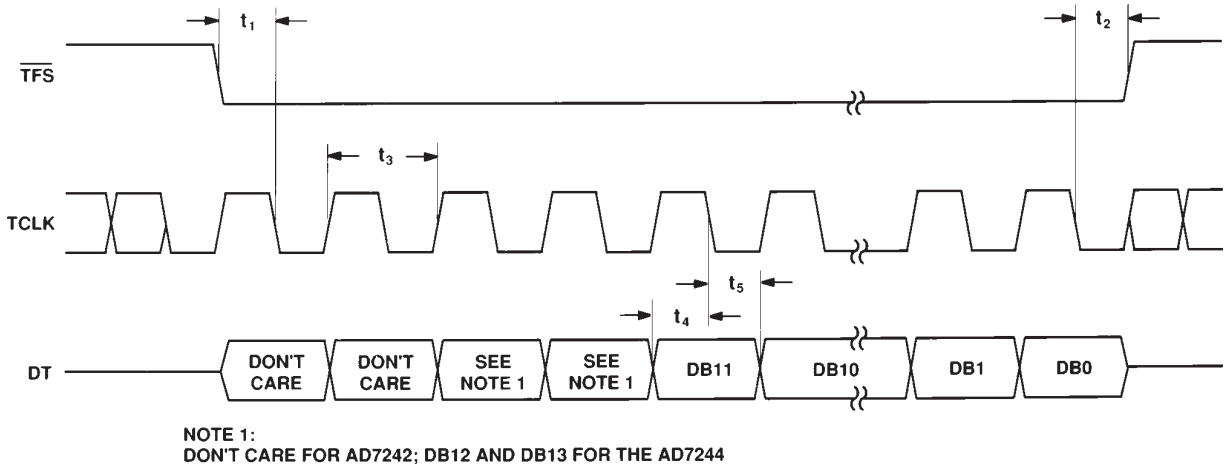


Figure 6. AD7242/AD7244 Timing Diagram

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD7242/AD7244 is via a serial bus that uses standard protocol compatible with DSP processors and microcontrollers. The communication interface consists of a separate transmit section for each of the DACs. Each section has a clock signal, a data signal and a frame or strobe pulse.

Figures 7 through 11 show the AD7242/AD7244 configured for interfacing to a number of popular DSP processors and microcontrollers.

AD7242/AD7244 to ADSP-2101/ADSP-2102 Interface

Figure 7 shows a serial interface between the AD7242/AD7244 and the ADSP-2101/ADSP-2102 DSP processor. The ADSP-2101/ADSP-2102 has two serial ports and, in the interface shown, both serial ports are used, one for each DAC. Both serial ports do not have to be used; in the case where only one serial port is used, an extra line (DACA/$\overline{\text{DACB}}$ as shown in the other serial interfaces) would have to decode the one $\overline{\text{TFS}}$ line to provide $\overline{\text{TFSA}}$ and $\overline{\text{TFSB}}$ lines for the AD7242/AD7244.

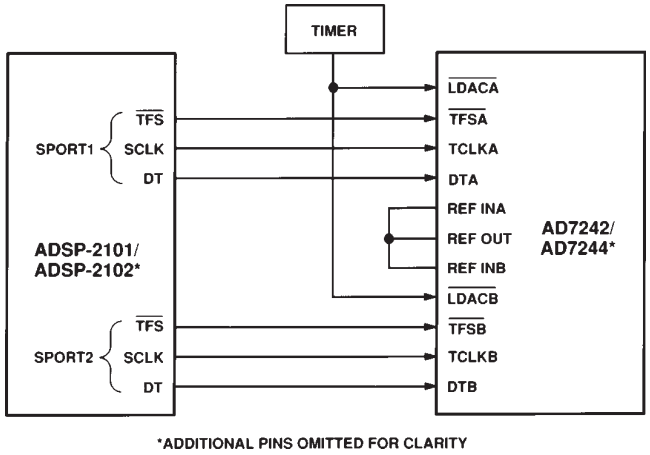


Figure 7. AD7242/AD7244 to ADSP-2101/ADSP-2102 Interface

The three serial lines of the first serial port, SPORT1, of the ADSP-2101/ADSP-2102 connect directly to the three serial input lines of DACA of the AD7242/AD7244. The three serial lines of SPORT2 connect directly to the three serial lines on the DACB serial input port. Data from the ADSP-2101/ADSP-2102 is valid on the falling edge of SCLK. A common LDAC signal is used to drive the $\overline{\text{LDACA}}$ and $\overline{\text{LDACB}}$ inputs. This is shown to be generated from a timer or clock recovery circuit but another control or address line of the ADSP-2101/ADSP-2102 could be used to drive these inputs. Alternatively, the $\overline{\text{LDACA}}$ and $\overline{\text{LDACB}}$ inputs of the AD7242/AD7244 could be hardwired low; in this case the update of the DAC latches and analog outputs takes place on the 16th falling edge of SCLK (after the respective $\overline{\text{TFS}}$ signal goes low).

AD7242/AD7244 to DSP56000 Interface

A serial interface between the AD7242/AD7244 and the DSP56000 is shown in Figure 8. The DSP56000 is configured for normal mode, asynchronous operation with gated clock. It is also set up for a 16-bit word with SCK and SC2 as outputs and the FSL control bit set to a 0. SCK is internally generated on the DSP56000 and applied to both the TCLKA and TCLKB inputs of the AD7242/AD7244. Data from the DSP56000 is valid on the falling edge of SCK. The serial data line, STD drives the DTA and DTB serial input data lines of the AD7242/AD7244.

The SC2 output provides the framing pulse for valid data. This is an active high output and is gated with a DACA/$\overline{\text{DACB}}$ control line before being applied to the $\overline{\text{TFSA}}$ and $\overline{\text{TFSB}}$ inputs of the AD7242/AD7244. The DACA/$\overline{\text{DACB}}$ line determines which DAC serial data is to be transferred to, i.e., which $\overline{\text{TFS}}$ line is active when SC2 is active.

As in the previous interface, a common $\overline{\text{LDAC}}$ input is shown driving the $\overline{\text{LDACA}}$ and $\overline{\text{LDACB}}$ inputs of the AD7242/AD7244. Once again, these $\overline{\text{LDAC}}$ inputs could be hardwired low, in which case V_{OUTA} or V_{OUTB} will be updated on the sixteenth falling edge of SCK after the $\overline{\text{TFSA}}$ or $\overline{\text{TFSB}}$ input goes low.

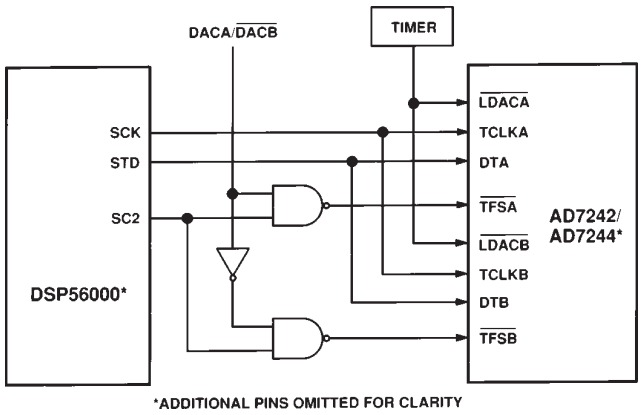


Figure 8. AD7242/AD7244 to DSP56000 Interface

AD7242/AD7244 to TMS320C25 Interface

Figure 9 shows a serial interface between the AD7242/AD7244 and the TMS320C25 DSP processor. In this interface, the CLKX and FSX signals of the TMS320C25 are generated from the clock/timer circuitry. The FSX pin of the TMS320C25 must be configured as an input. CLKX is used to provide both the TCLKA and TCLKB inputs of the AD7242/AD7244. DX of the TMS320C25 is also routed to the serial data line of each input port of the AD7242/AD7244.

Data from the TMS32020 is valid on the falling edge of CLKX after FSX goes low. This FSX signal is gated with the DACA/$\overline{\text{DACB}}$ control line to determine whether $\overline{\text{TFSA}}$ or $\overline{\text{TFSB}}$ goes low when FSX goes low.

The clock/timer circuitry also generates the $\overline{\text{LDAC}}$ signal for the AD7242/AD7244 to synchronize the update of the outputs with the serial transmission. As in the previous interface diagrams, a common $\overline{\text{LDAC}}$ input is shown driving the $\overline{\text{LDACA}}$ and $\overline{\text{LDACB}}$ inputs of the AD7242/AD7244. Once again, these $\overline{\text{LDAC}}$ inputs could be hardwired low, in which case V_{OUTA} or V_{OUTB} will be updated on the sixteenth falling edge of CLKX after the $\overline{\text{TFSA}}$ or $\overline{\text{TFSB}}$ input goes low.

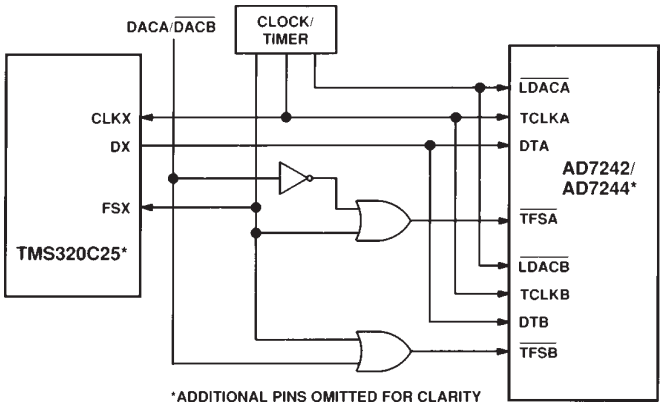


Figure 9. AD7242/AD7244 to TMS320C25 Interface

AD7242/AD7244 to 87C51 Interface

A serial interface between the AD7242/AD7244 and the 87C51 microcontroller is shown in Figure 10. TXD of the 87C51 drives TCLKA and TCLKB of the AD7242/AD7244 while RXD drives the two serial data lines of the part. The $\overline{\text{TFSA}}$ and $\overline{\text{TFSB}}$ signals are derived from P3.2 and P3.3, respectively.

The 87C51 provides the LSB of its SBUF register as the first bit in the serial data stream. Therefore, the user will have to ensure that the data in the SBUF register is correctly arranged so the don't care bits are the first to be transmitted to the AD7242/AD7244; the last bit to be sent is the LSB of the word to be loaded to the AD7242/AD7244. When data is to be transmitted to the part, P3.2 (for DACA) or P3.3 (for DACB) is taken low. Data on RXD is valid on the falling edge of TXD. The 87C51 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7242/AD7244, P3.2 (for DACA) or P3.3 (for DACB) is left low after the first eight bits are transferred and a second byte of data is then serially transferred to the AD7242/AD7244. When the second serial transfer is complete, the P3.2 line (for DACA) or the P3.3 line (for DACB) is taken high.

Figure 10 shows both $\overline{\text{LDAC}}$ inputs of the AD7242/AD7244 hardwired low. As a result, the DAC latch and the analog output of one of the DACs will be updated on the sixteenth falling edge of TXD after the respective $\overline{\text{TFS}}$ signal for that DAC has gone low. Alternatively, the scheme used in previous interfaces, whereby the $\overline{\text{LDAC}}$ inputs are driven from a timer, can be used.

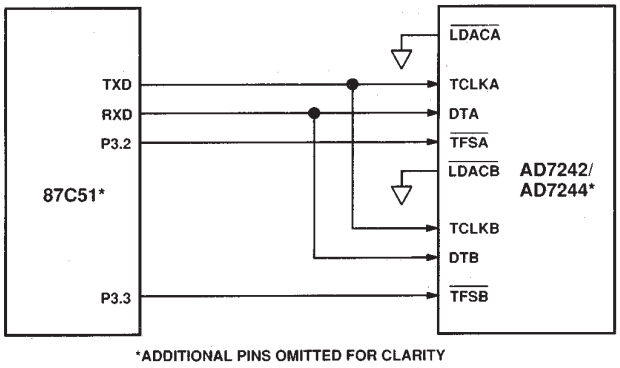


Figure 10. AD7242/AD7244 to 87C51 Interface

AD7242/AD7244 to 68HC11 Interface

Figure 11 shows a serial interface between the AD7242/AD7244 and the 68HC11 microcontroller. SCK of the 68HC11 drives TCLKA and TCLKB of the AD7242/AD7244 while the MOSI output drives the two serial data lines of the AD7242/AD7244. The $\overline{\text{TFSA}}$ and $\overline{\text{TFSB}}$ signals are derived from PC6 and PC7, respectively.

For correct operation of this interface, the 68HC11 should be configured such that its CPOL bit is a 0 and its CPHA bit is a 1. When data is to be transmitted to the part, PC6 (for DACA) or PC7 (for DACB) is taken low. When the 68HC11 is configured like this, data on MOSI is valid on the falling edge of SCK. The 68HCll transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7242/AD7244, PC6 (for DACA) or PC7 (for DACB) is left low after the first eight bits are transferred and a second byte of data is then serially transferred to the AD7242/AD7244. When the second serial transfer is complete, the PC6 line (for DACA) or the PC7 line (for DACB) is taken high.

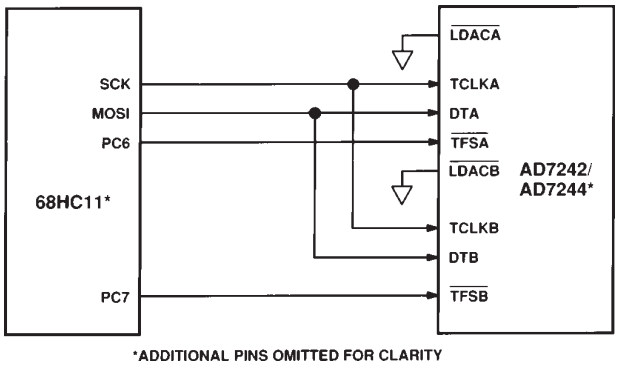


Figure 11. AD7242/AD7244 to 68HC11 Interface

Figure 11 shows both $\overline{\text{LDAC}}$ inputs of the AD7242/AD7244 hardwired low. As a result, the DAC latch and the analog output of one of the DACs will be updated on the sixteenth falling edge of SCK after the respective $\overline{\text{TFS}}$ signal for that DAC has gone low. Alternatively, the scheme used in previous interfaces, whereby the $\overline{\text{LDAC}}$ inputs are driven from a timer, can be used.

APPLYING THE AD7242/AD7244

Good printed circuit board layout is as important as the overall circuit design itself in achieving high speed converter performance. The AD7242 works on an LSB size of 1.465 mV, while the AD7244 works on an LSB size of 366 μV. Therefore, the designer must be conscious of minimizing noise in both the converter itself and in the surrounding circuitry. Switching mode power supplies are not recommended as the switching spikes can feed through to the on-chip amplifier. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors that influence any high performance converter, and a proper PCB layout that minimizes these effects is essential for best performance.

LAYOUT HINTS

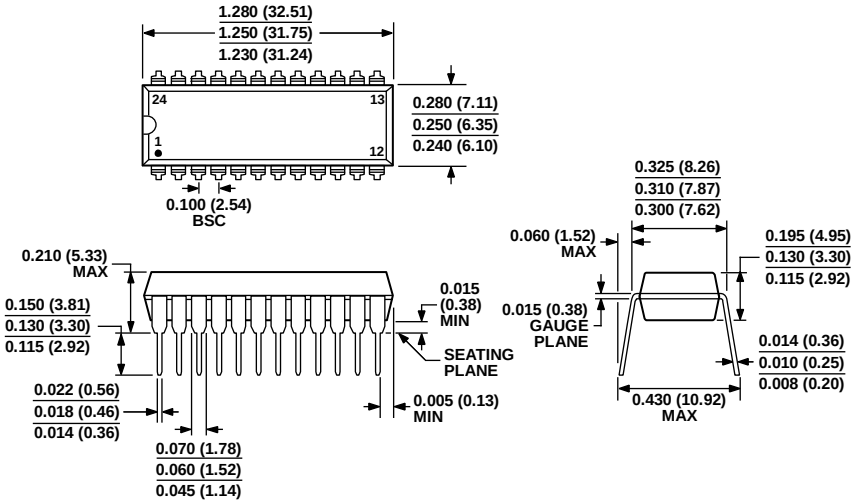
Ensure that the layout for the printed circuit board has separated digital and analog lines as much as possible. Take care not to run any digital track alongside an analog signal track. Establish a single point analog ground (star ground) separate from the logic system ground. Place this star ground as close as possible to the AD7242/AD7244. Connect all analog grounds to this star ground and also connect the AD7242/AD7244 DGND pins to this ground. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of high performance converters. Therefore, the foil width for these tracks should be kept as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise.

NOISE

Keep the signal leads on the V_{OUTA} and V_{OUTB} signals and the signal return leads to AGND as short as possible to minimize noise coupling. In applications where this is not possible, use a shielded cable between the DAC outputs and their destination. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the DAC and its destination device appears as an error voltage in series with the DAC output.

OUTLINE DIMENSIONS



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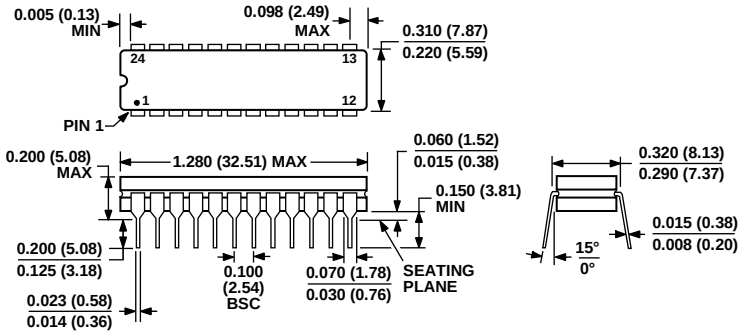
071006-A

Figure 12. 24-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-24-1)
Dimensions shown in inches and (millimeters)



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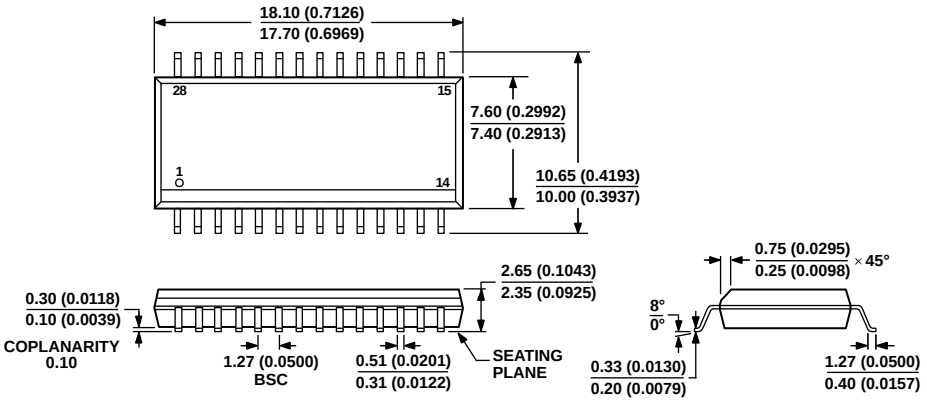
100808-A

Figure 13. 24-Lead Ceramic Dual In-Line Package [CERDIP]
Narrow Body
(Q-24-1)
Dimensions shown in inches and (millimeters)



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06-07-2006-A

Figure 14. 28-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-28)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Integral Nonlinearity	Package Description	Package Options
AD7244JNZ	–40°C to +85°C	±2 LSB max	24-Lead PDIP	N-24-1
AD7244JR	–40°C to +85°C	±2 LSB max	28-Lead SOIC_W	RW-28
AD7244AQ	–40°C to +85°C	±2 LSB max	24-Lead CERDIP	Q-24-1
AD7244JRZ	–40°C to +85°C	±2 LSB max	28-Lead SOIC_W	RW-28
AD7244JRZ-REEL	–40°C to +85°C	±2 LSB max	28-Lead SOIC_W	RW-28

[1] Z = RoHS Compliant Part.

REVISION HISTORY

4/15—Rev. A to Rev. B

Added AD7242 Obsolete Note 1
Updated Outline Dimensions 12
Changes to Ordering Guide 13

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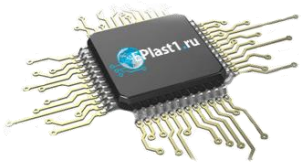
- Защита от снятия компонента с производства.



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