74HC137

3-to-8 line decoder, demultiplexer with address latches; inverting

Rev. 4 — 23 December 2015 Product data sheet

1. General description

The 74HC137 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The 74HC137 is specified in compliance with JEDEC standard no. 7A.

The 74HC137 is a 3-to-8 line decoder, demultiplexer with latches at the three address inputs (An). The 74HC137 essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled ($\overline{LE}$ = LOW), the 74HC137 acts as a 3-to-8 active LOW decoder. When the latch enable ($\overline{LE}$) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as $\overline{LE}$ remains HIGH.

The output enable input ($\overline{E}1$ and E2) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless $\overline{E}1$ is LOW and E2 is HIGH.

The 74HC137 is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

2. Features and benefits

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active LOW mutually exclusive outputs
- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC137D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC137DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1

4. Functional diagram

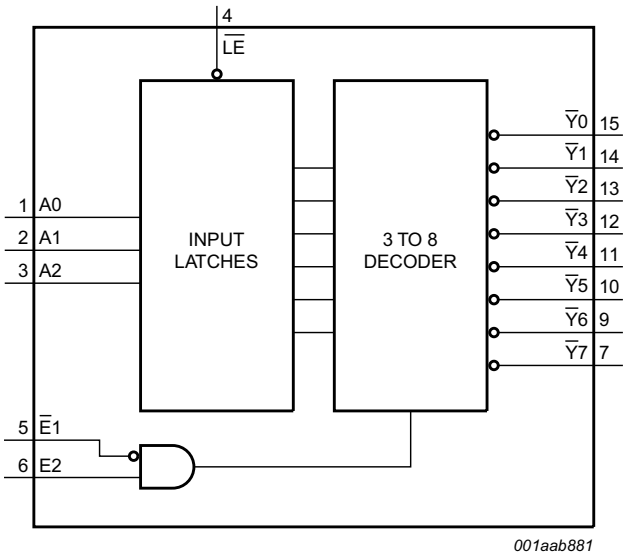


Fig 1. Functional diagram

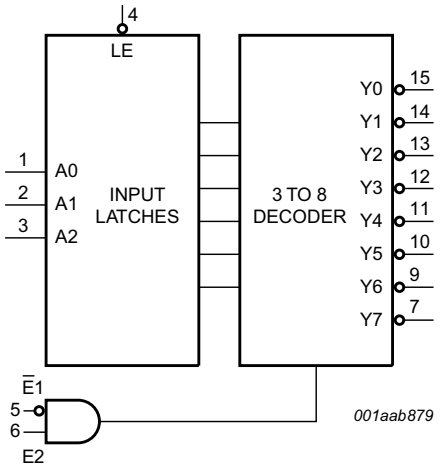


Fig 2. Logic symbol

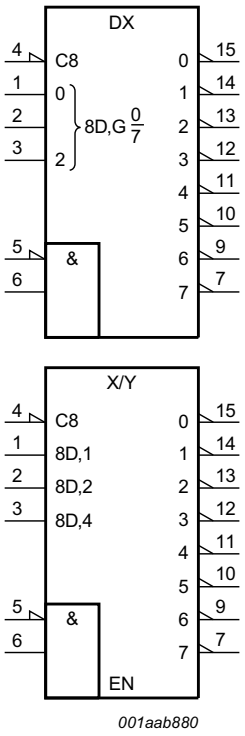


Fig 3. IEC logic symbol

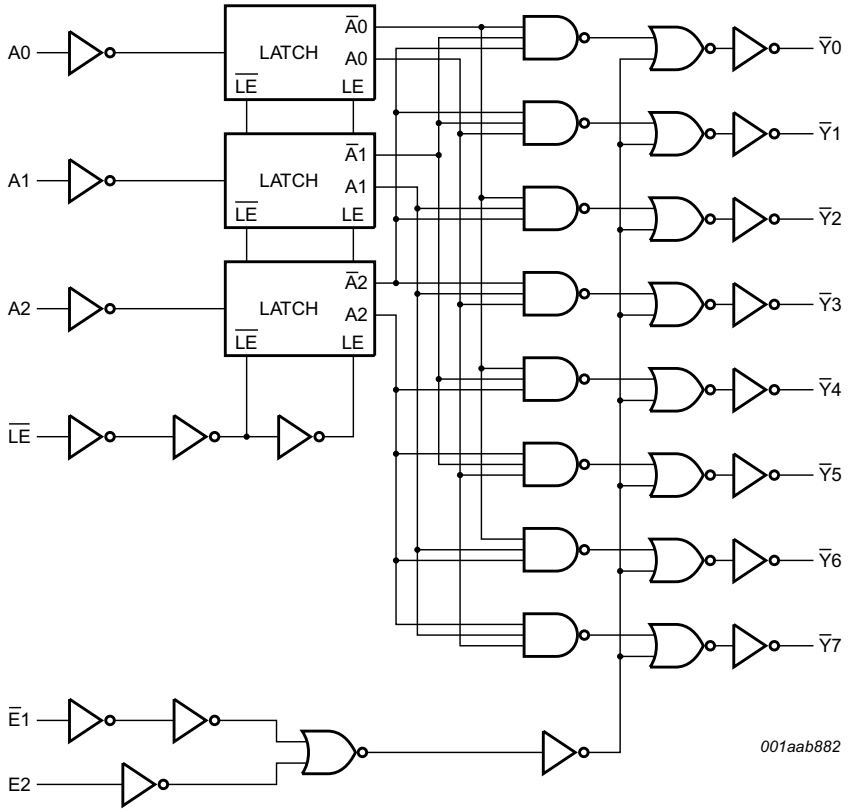


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

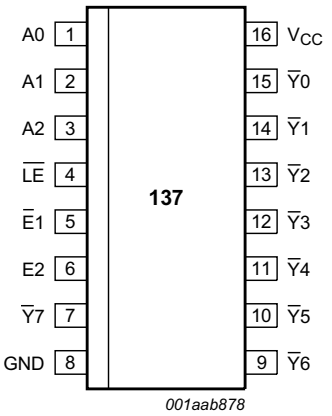


Fig 5. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0	1	data input 0
A1	2	data input 1
A2	3	data input 2
$\overline{LE}$	4	latch enable input (active LOW)
$\overline{E1}$	5	data enable input 1 (active LOW)
E2	6	data enable input 2 (active HIGH)
$\overline{Y7}$	7	multiplexer output 7
GND	8	ground (0 V)
$\overline{Y6}$	9	multiplexer output 6
$\overline{Y5}$	10	multiplexer output 5
$\overline{Y4}$	11	multiplexer output 4
$\overline{Y3}$	12	multiplexer output 3
$\overline{Y2}$	13	multiplexer output 2
$\overline{Y1}$	14	multiplexer output 1
$\overline{Y0}$	15	multiplexer output 0
V_{CC}	16	positive supply voltage

6. Functional description

6.1 Function table

Table 3. Function table[1]

Enable			Input			Output							
$\overline{LE}$	$\overline{E1}$	E2	A0	A1	A2	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
H	L	H	X	X	X	stable							
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
			H	L	L	H	L	H	H	H	H	H	H
			L	H	L	H	H	L	H	H	H	H	H
			H	H	L	H	H	H	L	H	H	H	H
			L	L	H	H	H	H	H	L	H	H	H
			H	L	H	H	H	H	H	H	L	H	H
			L	H	H	H	H	H	H	H	H	L	H
			H	H	H	H	H	H	H	H	H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output diode current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output source or sink current	$V_O = –0.5$ V to $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		–50	-	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	SO16 and SSOP16 packages [1]	-	500	mW

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V
T_{amb}	ambient temperature		–40	-	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	μA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	μA
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}		-		
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}		-		
		I_O = 20 μA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	μA

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{pd}	propagation delay	An to $\overline{Y}$n; see Figure 6 [1]				
		V_{CC} = 2.0 V	-	58	180	ns
		V_{CC} = 4.5 V	-	21	36	ns
		V_{CC} = 6.0 V	-	17	31	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	18	-	ns
		$\overline{LE}$ to $\overline{Y}$n; see Figure 7				
		V_{CC} = 2.0 V	-	55	190	ns
		V_{CC} = 4.5 V	-	20	38	ns
		V_{CC} = 6.0 V	-	16	32	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	ns
		$\overline{E}$1 to $\overline{Y}$n; see Figure 7				
		V_{CC} = 2.0 V	-	50	145	ns
		V_{CC} = 4.5 V	-	18	29	ns
		V_{CC} = 6.0 V	-	14	25	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	15	-	ns
		E2 to $\overline{Y}$n; see Figure 6				
		V_{CC} = 2.0 V	-	50	145	ns
		V_{CC} = 4.5 V	-	18	29	ns
		V_{CC} = 6.0 V	-	14	25	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	15	-	ns
t_t	transition time	see Figure 6 [2]				
		V_{CC} = 2.0 V	-	19	75	ns
		V_{CC} = 4.5 V	-	7	15	ns
		V_{CC} = 6.0 V	-	6	13	ns
t_W	pulse width	$\overline{LE}$ HIGH; see Figure 8				
		V_{CC} = 2.0 V	50	11	-	ns
		V_{CC} = 4.5 V	10	4	-	ns
		V_{CC} = 6.0 V	9	3	-	ns
t_{su}	set-up time	An to $\overline{LE}$; see Figure 8				
		V_{CC} = 2.0 V	50	3	-	ns
		V_{CC} = 4.5 V	10	1	-	ns
		V_{CC} = 6.0 V	9	1	-	ns
t_h	hold time	An to $\overline{LE}$; see Figure 8				
		V_{CC} = 2.0 V	30	3	-	ns
		V_{CC} = 4.5 V	6	1	-	ns
		V_{CC} = 6.0 V	5	1	-	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [3]	-	57	-	pF

Table 7. Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C						
t_{pd}	propagation delay	An to $\overline{Y}$n; see Figure 6 [1]				
		V_{CC} = 2.0 V	-	-	225	ns
		V_{CC} = 4.5 V	-	-	45	ns
		V_{CC} = 6.0 V	-	-	38	ns
		$\overline{LE}$ to $\overline{Y}$n; see Figure 7				
		V_{CC} = 2.0 V	-	-	240	ns
		V_{CC} = 4.5 V	-	-	48	ns
		V_{CC} = 6.0 V	-	-	41	ns
		$\overline{E}$1 to $\overline{Y}$n; see Figure 7				
		V_{CC} = 2.0 V	-	-	180	ns
		V_{CC} = 4.5 V	-	-	36	ns
		V_{CC} = 6.0 V	-	-	31	ns
		E2 to $\overline{Y}$n; see Figure 6				
		V_{CC} = 2.0 V	-	-	180	ns
		V_{CC} = 4.5 V	-	-	36	ns
		V_{CC} = 6.0 V	-	-	31	ns
t_t	transition time	see Figure 6 [2]				
		V_{CC} = 2.0 V	-	-	95	ns
		V_{CC} = 4.5 V	-	-	19	ns
		V_{CC} = 6.0 V	-	-	16	ns
t_W	pulse width	$\overline{LE}$ HIGH; see Figure 8				
		V_{CC} = 2.0 V	65	-	-	ns
		V_{CC} = 4.5 V	13	-	-	ns
		V_{CC} = 6.0 V	11	-	-	ns
t_{su}	set-up time	An to $\overline{LE}$; see Figure 8				
		V_{CC} = 2.0 V	65	-	-	ns
		V_{CC} = 4.5 V	13	-	-	ns
		V_{CC} = 6.0 V	11	-	-	ns
t_h	hold time	An to $\overline{LE}$; see Figure 8				
		V_{CC} = 2.0 V	40	-	-	ns
		V_{CC} = 4.5 V	8	-	-	ns
		V_{CC} = 6.0 V	7	-	-	ns

Table 7. Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +125 °C						
t_{pd}	propagation delay	An to $\overline{Y}$n; see Figure 6 [1]				
		V_{CC} = 2.0 V	-	-	270	ns
		V_{CC} = 4.5 V	-	-	54	ns
		V_{CC} = 6.0 V	-	-	46	ns
		$\overline{LE}$ to $\overline{Y}$n; see Figure 7				
		V_{CC} = 2.0 V	-	-	285	ns
		V_{CC} = 4.5 V	-	-	57	ns
		V_{CC} = 6.0 V	-	-	48	ns
		$\overline{E}$1 to $\overline{Y}$n; see Figure 7				
		V_{CC} = 2.0 V	-	-	220	ns
		V_{CC} = 4.5 V	-	-	44	ns
		V_{CC} = 6.0 V	-	-	38	ns
		E2 to $\overline{Y}$n; see Figure 6				
		V_{CC} = 2.0 V	-	-	220	ns
		V_{CC} = 4.5 V	-	-	44	ns
		V_{CC} = 6.0 V	-	-	38	ns
t_t	transition time	see Figure 6 [2]				
		V_{CC} = 2.0 V	-	-	110	ns
		V_{CC} = 4.5 V	-	-	22	ns
		V_{CC} = 6.0 V	-	-	19	ns
t_W	pulse width	$\overline{LE}$ HIGH; see Figure 8				
		V_{CC} = 2.0 V	-	-	75	ns
		V_{CC} = 4.5 V	-	-	15	ns
		V_{CC} = 6.0 V	-	-	13	ns
t_{su}	set-up time	An to $\overline{LE}$; see Figure 8				
		V_{CC} = 2.0 V	-	-	75	ns
		V_{CC} = 4.5 V	-	-	15	ns
		V_{CC} = 6.0 V	-	-	13	ns

Table 7. Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

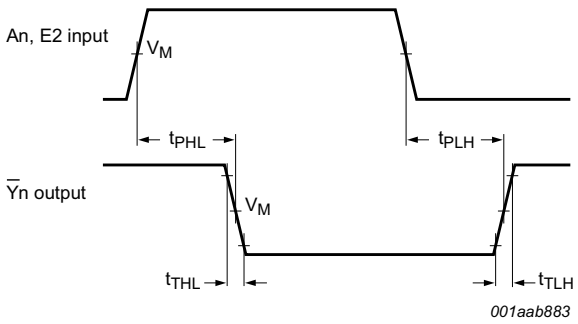
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_h	hold time	An to $\overline{LE}$; see Figure 8				
		V_{CC} = 2.0 V	-	-	45	ns
		V_{CC} = 4.5 V	-	-	9	ns
		V_{CC} = 6.0 V	-	-	8	ns

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

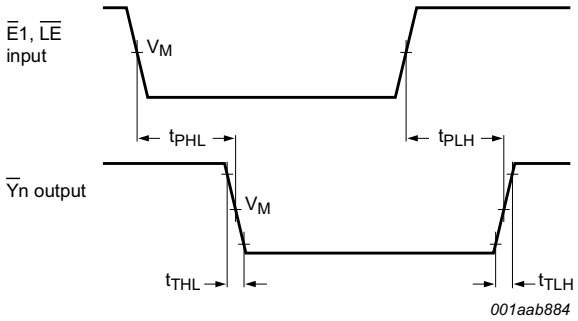
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



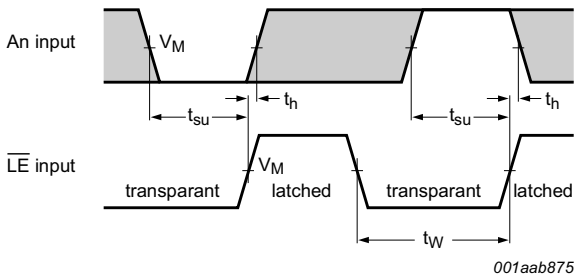
$V_M = 0.5 \times V_I$.

Fig 6. Waveforms showing the address input (An) and enable input (E2) to output ($\overline{Y}$n) propagation delays and the output transition times



$V_M = 0.5 \times V_I$.

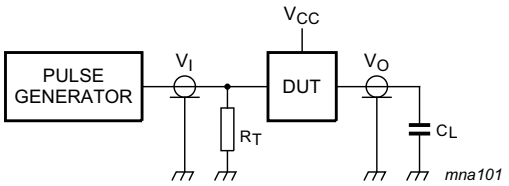
Fig 7. Waveforms showing the enable input ($\overline{E}1$, $\overline{LE}$) to output ($\overline{Y}n$) propagation delays and the output transition times



The shaded areas indicate when the input is permitted to change for predictable output performance.

$V_M = 0.5 \times V_I$.

Fig 8. Waveforms showing the data set-up, hold times for An input to $\overline{LE}$ input and the latch enable pulse width



Test data is given in Table 8.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 9. Test circuit for measuring switching times

Table 8. Test data

Supply	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0 V	V_{CC}	6 ns	50 pF
4.5 V	V_{CC}	6 ns	50 pF
6.0 V	V_{CC}	6 ns	50 pF
5.0 V	V_{CC}	6 ns	15 pF

12. Application information

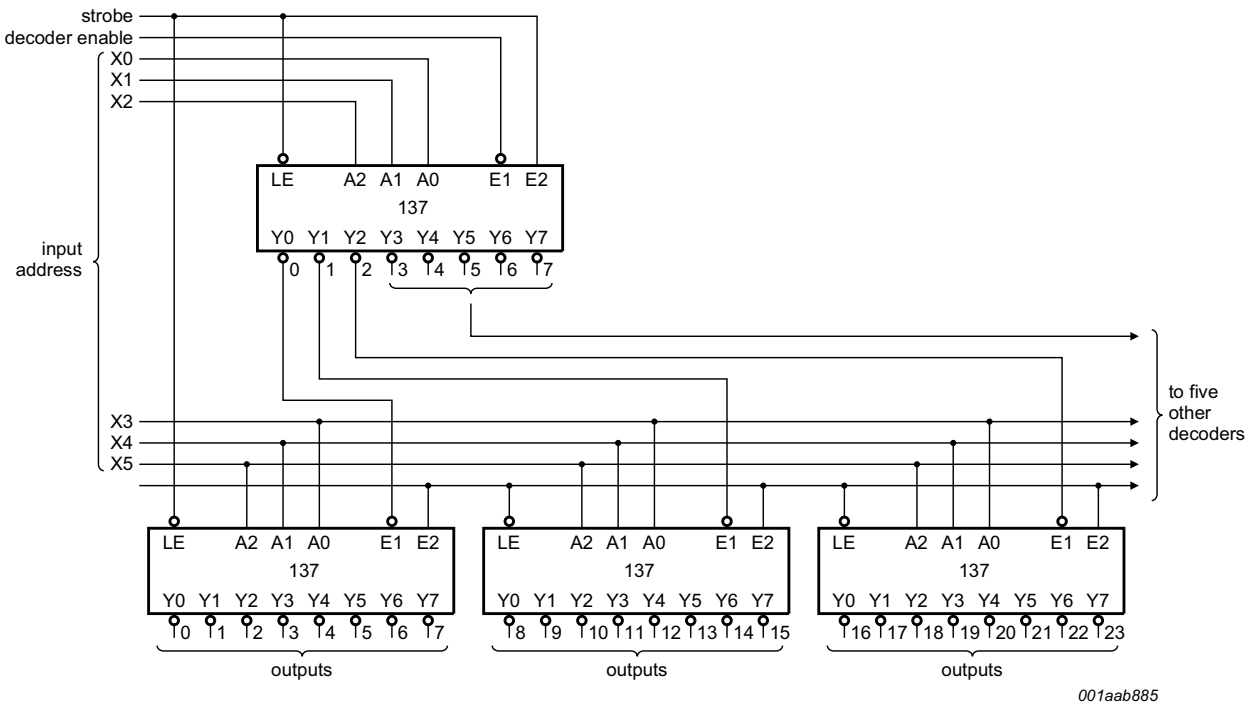
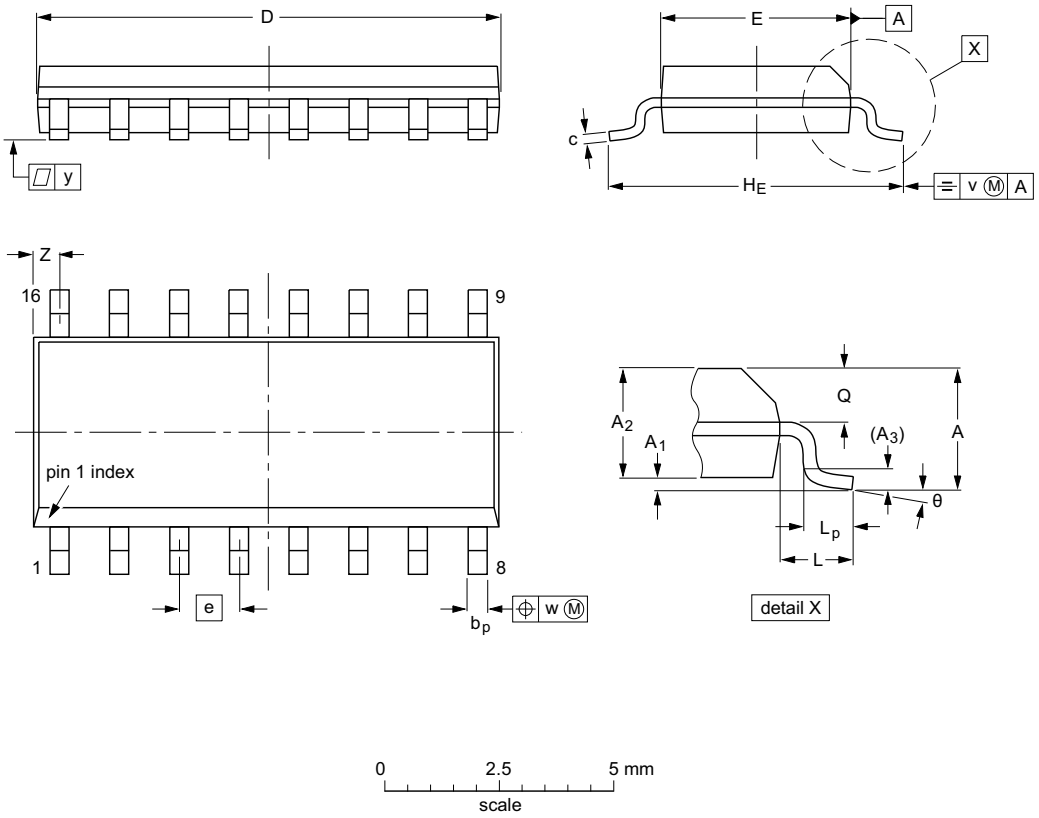


Fig 10. 6-to-64 line decoder with input address storage

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

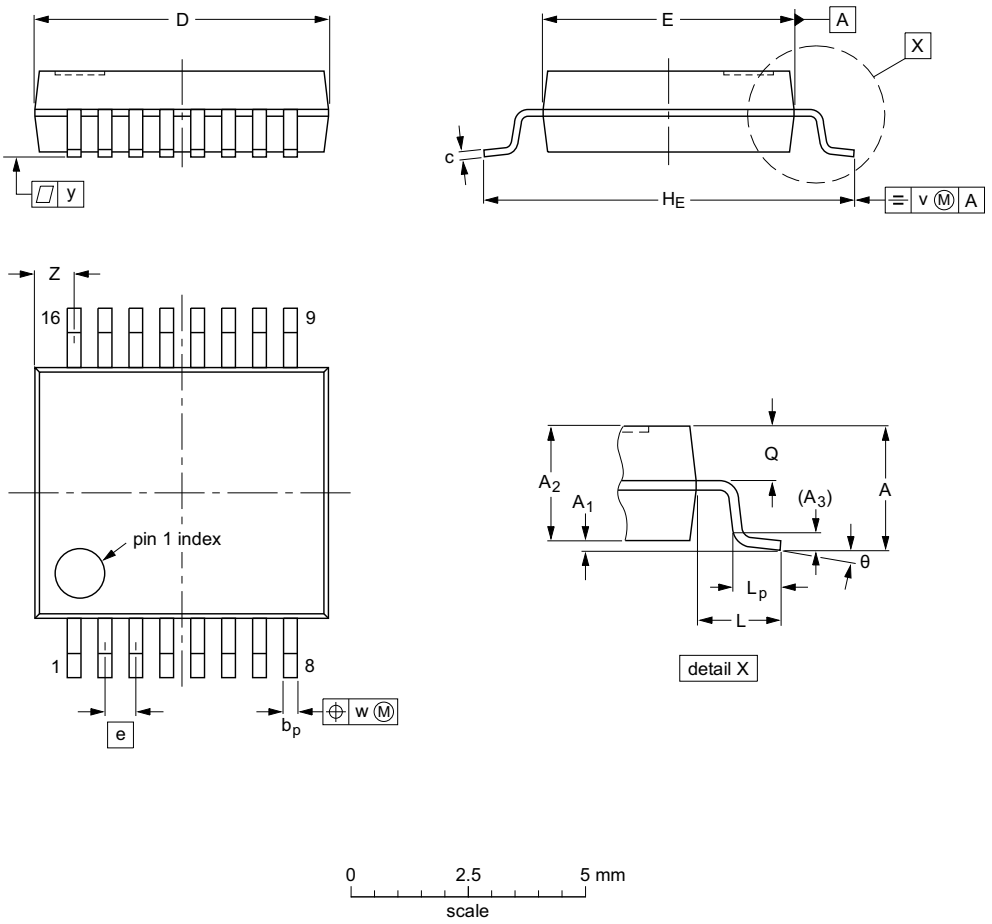
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT338-1 (SSOP16)

14. Abbreviations

Table 9. Abbreviations

Acronym	Abbreviation
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC137 v.4	20151223	Product data sheet	-	74HC137 v.3
Modifications:	• Type numbers 74HC137N (SOT38-4) removed.			
74HC137 v.3	20041111	Product data sheet	-	74HC_HCT137_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Removed type number 74HCT137. • Inserted family specification.			
74HC_HCT137_CNV v.2	19970827	Product specification	-	74HC_HCT137 v.1
74HC_HCT137 v.1	19901201	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 23 December 2015

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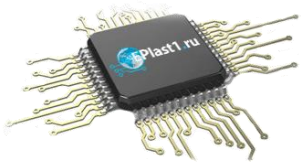

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