International
IOR Rectifier

IR3548

FEATURES

- Integrated Dual, Doubler or Quad mode Driver
- 2 pairs of high and low side MOSFETs
- Peak efficiency up to 94% at 1.2V
- Variable gate drive, VDRV, from 4.25V to 12V to optimize system efficiency
- 5V VCC and VDRV capability for sleep states where only 5V is available
- Input voltage (VIN) range of 4.25V to 17V
- Output current capability of 30A/phase
- Switching frequency up to 1.5MHz
- Ultra-low Rg MOSFET technology minimizes switching losses for optimized high frequency performance
- Synchronous MOSFET with monolithic integrated Schottky diode reduces dead-time and diode reverse recovery losses
- Low quiescent current (1uA typical) for VR12.6/VR12.6+ notebook applications.
- Independent enable control for each phase
- Support both industry standard 3.3V tri-state PWM and IR Active Tri-Level (ATL) PWM logic
- Small 6mm x 8 mm x 0.9mm PQFN package
- Lead-free RoHS compliant package

APPLICATIONS

- High frequency, low profile DC-DC converters
- Voltage Regulators for CPUs, GPUs, and DDR memory arrays of servers, notebook.

DESCRIPTION

The IR3548 is a dual integrated PowIRstage® is a with 2 pairs of co-packed control and synchronous MOSFETs and an optimized dual phase driver. The package is optimized internally for PCB layout, heat transfer and package inductance. The integrated driver is capable of operating as a Dual driver (2 PWM controlling 2 phases), a Doubler driver (1 PWM controlling 2 phases) or a Quad driver (1 PWM controlling 4 phases in two IR3548s).

Up to 1.5MHz switching frequency enables high performance transient response, allowing miniaturization of output inductors, as well as input and output capacitors while maintaining industry leading efficiency. Integrating two phases in one package while still providing superior efficiency and thermal performance, the IR3548 enables smallest size and lower solution cost. The lower quiescent current makes it suitable for next generation VR12.6/VR12.6+ notebook applications.

The IR3548 uses IR's latest generation of low voltage MOSFET technology characterized by ultra-low gate resistance (Rg) and charge (Qg) that result in minimized switching losses. The synchronous MOSFET optimizes conduction losses and features a monolithic integrated Schottky to significantly reduce dead-time and diode conduction and reverse recovery losses.

The IR3548 is optimized specifically for CPU core power delivery in 12Vin applications like servers, certain notebooks, GPU and DR memory designs.

ORDERING INFORMATION

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR3548MTRPBF	PQFN 6 mm x 8 mm	Tape and Reel	3000	

PINOUT DIAGRAM

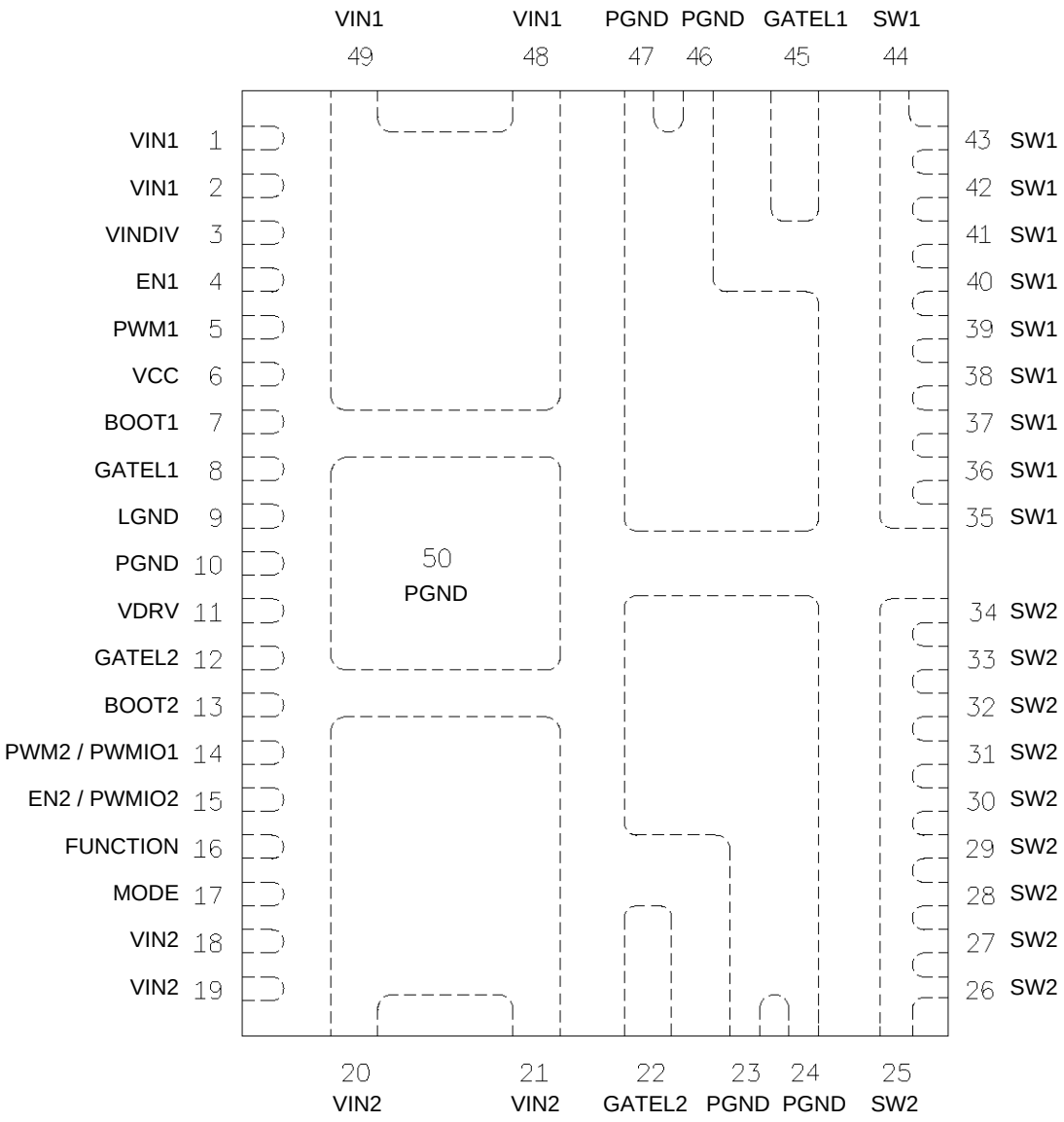


Figure 1: IR3548 Top View

FUNCTIONAL BLOCK DIAGRAM

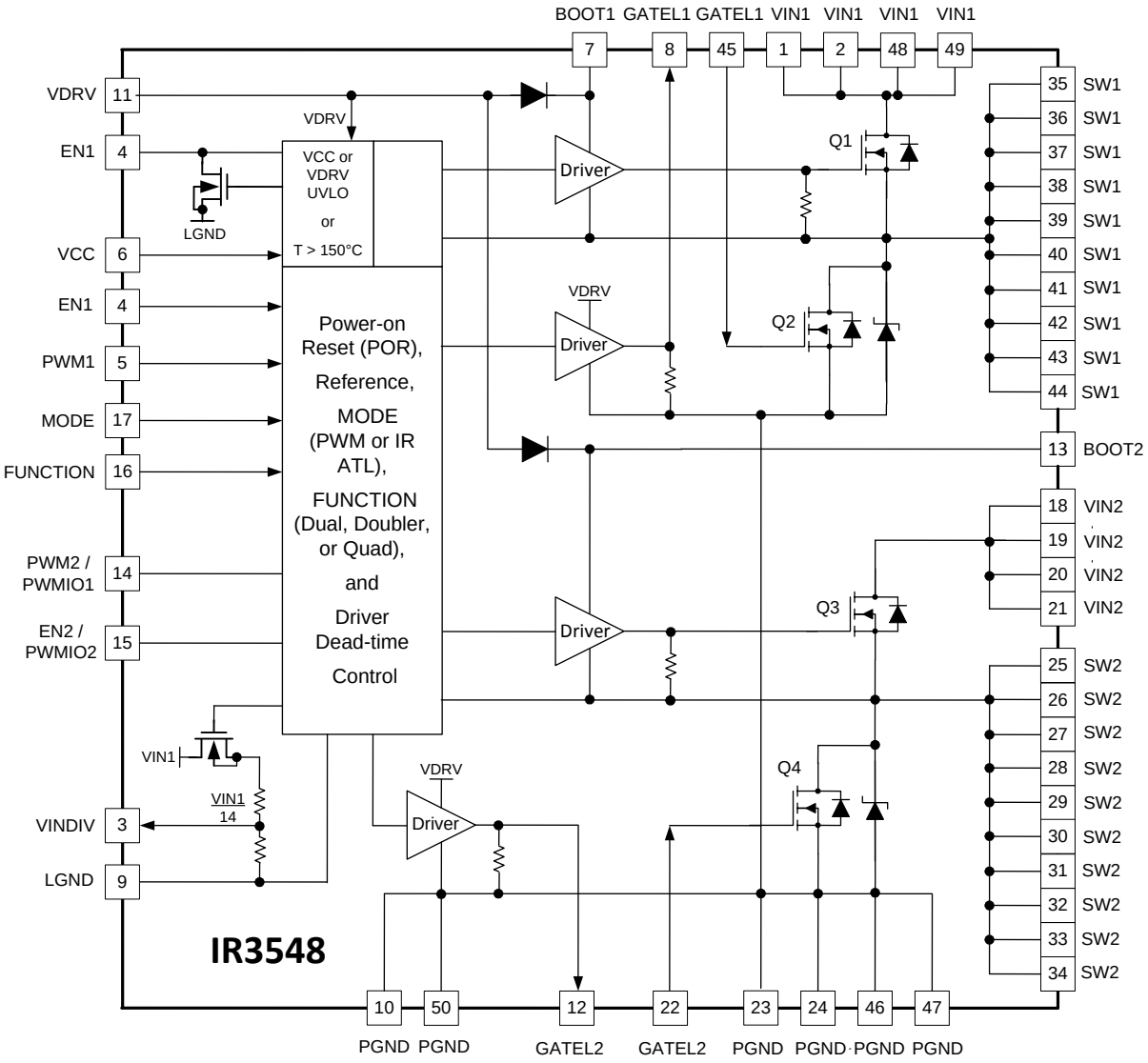


Figure 2: Block Diagram

TABLE 1: FUNCTION AND MODE PIN CONFIGURATION TABLE

PIN 16 "FUNCTION"	PIN 17 "MODE"	Functionality	PWM Mode	Pin 4 "EN1" Function	Pin 14 Function	Pin 15 Function
0	1	DUAL	IR ATL	Loop 1	PWM2	EN2
1	1	DOUBLER	IR ATL	Loops 1 & 2	NA	NA
Float	1	QUAD Master	IR ATL	Loops 1 & 2	PWMIO1 (output)	PWMIO2 (output)
0	0	DUAL	Tri-State	Loop 1	PWM2	EN2
1	0	DOUBLER	Tri-State	Loops 1 & 2	NA	NA
Float	0	QUAD Slave	NA	Loops 1 & 2	PWMIO1 (input)	PWMIO2 (input)

TYPICAL APPLICATION

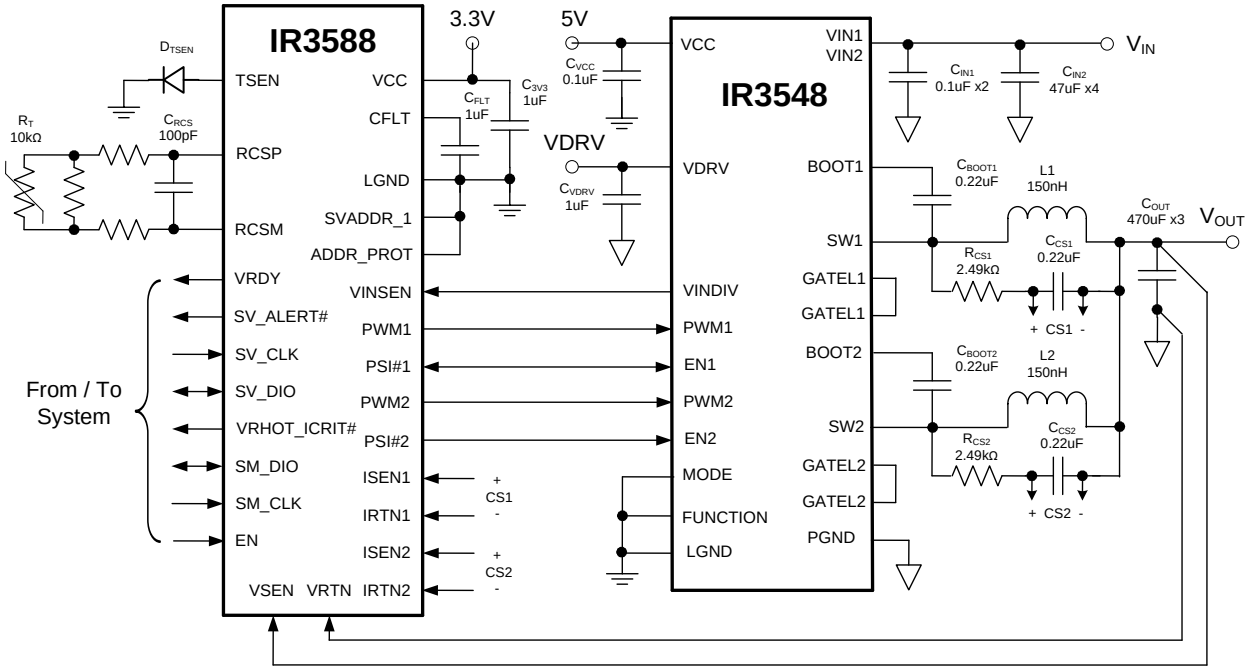


Figure 3: High Density Two-Phase Voltage Regulator, Standard Tri-state PWM, Dual Driver Mode

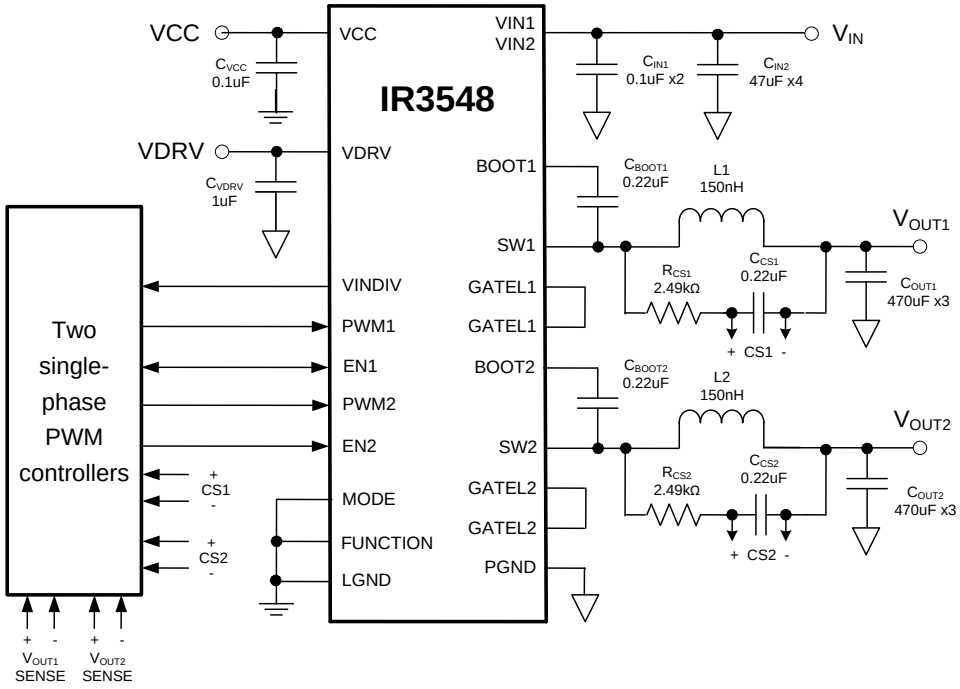


Figure 4: IR3548 Two Single-Phase Voltage Regulators, Standard Tri-state PWM, Dual Driver Mode

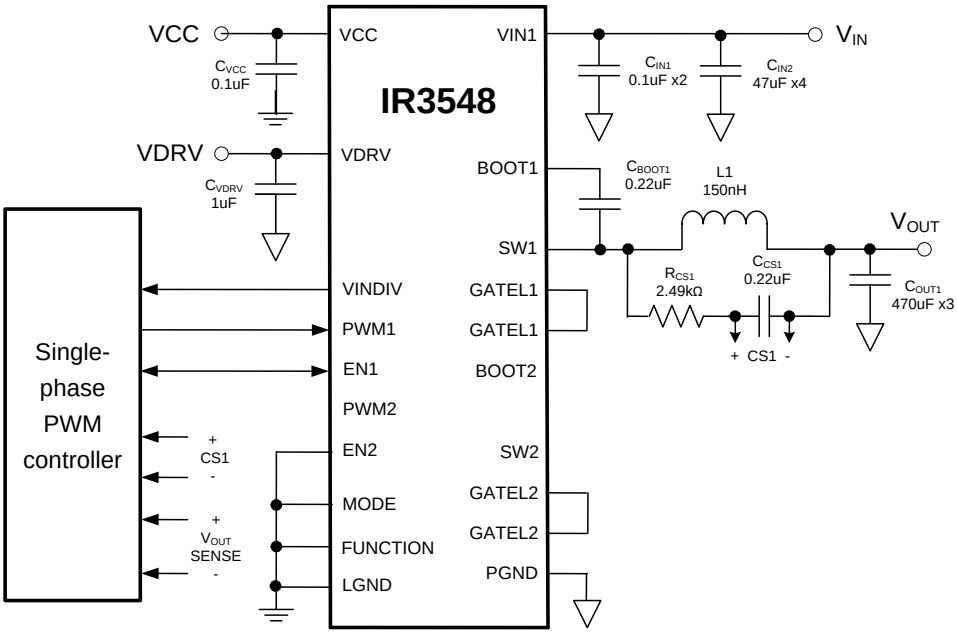


Figure 5: IR3548 Single-phase Voltage Regulator, Standard Tri-state PWM, Dual Driver Mode

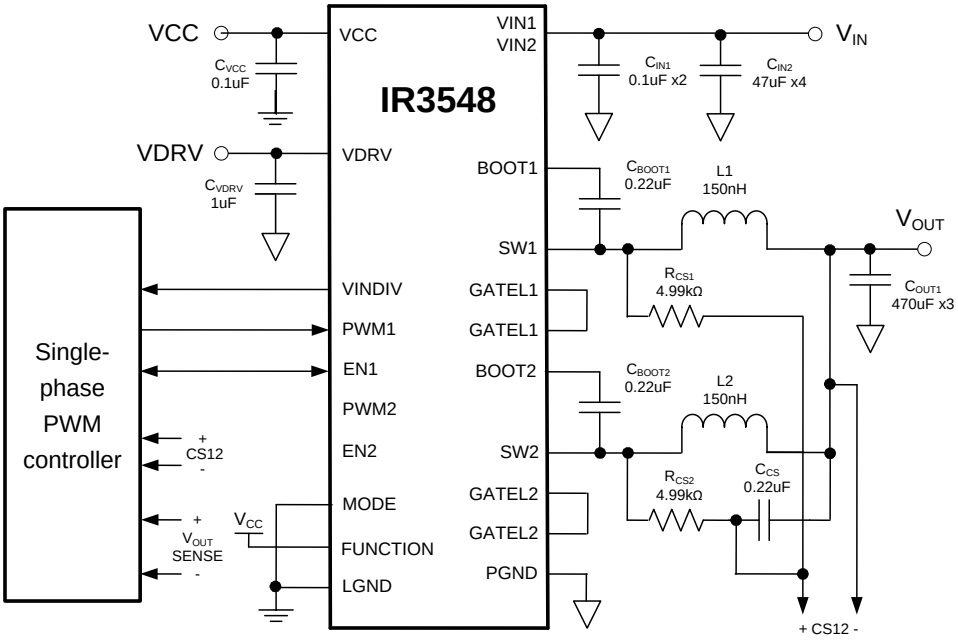


Figure 6: IR3548 Two-Phase Voltage Regulator, Standard Tri-state PWM, Doubler Driver Mode

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1, 2, 48, 49	VIN1	High current input supply pins for Phase 1. Recommended operating range is 4.25V to 17V. Connect at least a 10uF 1206 ceramic capacitor and a 0.1uF 0402 ceramic capacitor. Place the capacitors as close as possible to VIN1 pins and PGND pins (46 and 47). The 0.1uF 0402 capacitor should be on the same side of the PCB as the IR3548.
3	VINDIV	Output containing divided VIN1 analog information, (VIN1-LGND) / 14 with respect to LGND. The internal resistor divider is disconnected from VIN1 when EN1 is low.
4	EN1	Phase 1 ENABLE input in Dual mode and Phases 1 & 2 ENABLE input in Doubler or Quad mode. Grounding this pin places Phase 1 in low quiescent mode as a Dual driver and sets both phases in low quiescent mode as a Doubler or Quad driver. The pin is also used to communicate VDRV UVLO, VCC UVLO or over temperature condition; EN1 is pulsed low under the fault. The pin must be driven high with a pullup resistor or grounded and should not be floated.
5	PWM1	The PWM1 is the control input for the first driver with either an IR ATL compatible signal or an industry standard Tri-State signal. Connect this pin to the PWM output of the controller. As a Dual driver, PWM1 controls gate drivers for Phase 1 (Q1 and Q2), and as a Doubler or Quad driver, PWM1 controls both phases (Q1 and Q2 as well as Q3 and Q4).
6	VCC	Bias voltage for control logic. Connect this pin to a +5V bias supply. Place a high quality low ESR 0.1uF ceramic capacitor from this pin to the LGND pin.
7	BOOT1	Floating bootstrap supply pin for the gate drive of control MOSFET Q1. Connect the bootstrap capacitor between this pin and the SW1 pin. The bootstrap capacitor provides the charge to turn on the control MOSFET Q1. See the Internal Bootstrap Device section under DESCRIPTION for guidance in choosing the capacitor value.
8, 45	GATEL1	Gate connection of the Phase 1 synchronous MOSFET Q2. Use a short, wide and direct PCB trace to connect the two pins.
9	LGND	Bias and reference ground. All control signals are referenced to this node.
10, 23, 24, 46, 47, 50	PGND	High current power ground. Note all pins are internally connected in the package. Provide low resistance connections to the ground plane and respective output capacitors.
11	VDRV	Connect this pin to a separate supply voltage between 4.25V and 12V to vary the drive voltage on both the control and synchronous MOSFETs. Place a high quality low ESR ceramic capacitor from this pin to PGND pin (10).
12, 22	GATEL2	Gate connection of the Phase 2 synchronous MOSFET Q4. Use a short, wide and direct PCB trace to connect the two pins.
13	BOOT2	Floating bootstrap supply pin for the gate drive of control MOSFET Q3. Connect the bootstrap capacitor between this pin and the SW2 pin. The bootstrap capacitor provides the charge to turn on the control MOSFET Q3. See the Internal Bootstrap Device section under DESCRIPTION for guidance in choosing the capacitor value.
14	PWM2 / PWMIO1	Dual function pin. It is PWM2 in Dual mode. The PWM2 is the control input for the second driver with either an IR ATL compatible signal or an industry standard Tri-State signal. Connect this pin to the PWM output of the controller. As a DUAL driver, PWM2 controls gate drivers for Phase 2. As a DOUBLER driver, the pin is un-used and is internally disconnected. As a QUAD driver, the pin becomes PWMIO1, a CMOS input or output depending on the configuration of the IR3548 as a slave or master repectively. Refer to Table 1 on page 3 for more details.
15	EN2 / PWMIO2	Dual function pin. It is Phase 2 ENABLE input as a Dual driver. The pin must be driven high or low in this mode and should not be floated. Grounding this pin places Phase 2 in low quiescent mode. As a DOUBLER driver, the pin is un-used and is internally disconnected. As a QUAD driver, the pin becomes PWMIO2, a CMOS input or output depending on the configuration of the IR3548 as a slave or master respectively. Refer to Table 1 on page 3 for more details.
16	FUNCTION	FUNCTION pin used to select between Dual, Doubler and Quad driver modes. Voltage lower than 0.8V sets Dual mode; voltage higher than 2.0V sets Doubler mode; Floating the pin (or between 1.2V and 1.6V) sets Quad mode. This pin in combination with the MODE pin also determines Master or Slave behavior in Quad mode. The pin status is sensed when EN1 is enabled or VCC UVLO is cleared. Refer to Table 1 on page 3 for more details.

PIN #	PIN NAME	PIN DESCRIPTION
17	MODE	PWM mode pin used to select either IR ATL input or industry tri-state PWM input. This pin in combination with the FUNCTION pin also determines Master or Slave behavior in Quad mode. Pin should be tied to LGND or VCC, and the pin status is sensed at EN1 enable or when VCC UVLO is cleared. Refer to Table 1 on page 3 for more details.
18-21	VIN2	High current input supply pins for Phase 2. Recommended operating range is 4.25V to 17V. Connect at least a 10uF 1206 ceramic capacitor and a 0.1uF 0402 ceramic capacitor. Place the capacitors as close as possible to VIN2 pins and PGND pins (23 and 24). The 0.1uF 0402 capacitor should be on the same side of the PCB as the IR3548.
25-34	SW2	High Current Switch Node for Phase 2 (Q3 and Q4).
35-44	SW1	High Current Switch Node for Phase 1 (Q1 and Q2).

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PIN Number	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1, 2, 48, 49	VIN1	25V	-0.3V	5A RMS	20A RMS
3	VINDIV	VCC +0.3V	-0.3V	1mA	1mA
4	EN1	VCC +0.3V	-0.3V	1mA	50mA
5	PWM1	VCC +0.3V	-0.3V	5mA	1mA
6	VCC	6.5V	-0.3V	NA	100mA
7	BOOT1	15V with respect to SW1, 35V with respect to PGND	-0.3V with respect to SW1	1A for <100ns, 100mA DC	2A for <100ns, 100mA DC
8, 45	GATEL1	15V with respect to PGND	-5V for <200ns, -0.3V DC with respect to PGND	2A for <100ns, 200mA DC	4A for <100ns, 200mA DC
9	LGND	0V	0V	50mA	1mA
10, 23, 24, 46, 47, 50	PGND	300mV	-300mV	40A RMS	80A RMS
11	VDRV	13.2V	-0.3V	NA	200mA
12, 22	GATEL2	15V with respect to PGND	-5V for <200ns, -0.3V DC with respect to PGND	2A for 100ns, 200mA DC	4A for <100ns, 200mA DC
13	BOOT2	15V with respect to SW2, 35V with respect to PGND	-0.3V with respect to SW2	1A for <100ns, 100mA DC	2A for <100ns, 100mA DC
14	PWM2 / PWMIO1	VCC +0.3V	-0.3V	10mA	10mA
15	EN2 / PWMIO2	VCC +0.3V	-0.3V	10mA	10mA
16	FUNCTION	VCC +0.3V	-0.3V	5mA	1mA
17	MODE	VCC +0.3V	-0.3V	5mA	1mA
18-21	VIN2	25V	-0.3V	5A RMS	20A RMS
25-34	SW2	25V	-8V for <200ns, -0.3V DC	50A RMS	25A RMS
35-44	SW1	25V	-8V for <200ns, -0.3V DC	50A RMS	25A RMS

THERMAL INFORMATION	
Thermal Resistance, Junction to Top (θ_{JC_TOP})	11.0 °C/W
Thermal Resistance, Junction to PCB (Pin 47) (θ_{JB})	1.7 °C/W
Thermal Resistance (θ_{JA})[1]	18.4 °C/W
Maximum Operating Junction Temperature	-40°C to 150°C
Maximum Storage Temperature Range	-65°C to 150°C
ESD Rating	HBM Class 1A JEDEC Standard
MSL Rating	3
Reflow Temperature	260°C

Note:

1. Thermal Resistance (θ_{JA}) is measured with the component mounted on a high effective thermal conductivity test board in free air. Refer to International Rectifier Application Note AN-994 for details.

ELECTRICAL SPECIFICATIONS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

PARAMETER	MIN	SYMBOL	MAX	UNIT
Recommended VIN Range	4.25	VIN	17	V
Recommended VCC	4.25	VCC	5.5	V
Recommended VDRV	4.25	VDRV	12	V
Recommended Switching Frequency	200	f_{SW}	1500	kHz
Recommended Operating Junction Temperature	-40	T_J	125	°C

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Efficiency						
PowIRstage® Peak Efficiency	η	Note 2		93.8		%
Bootstrap PFET						
Forward Voltage	V_{FWD_PFET}	I(BOOST) = 35mA	450	595	950	mV
Thermal Flag						
Rising Threshold	T_{RISE}	Note 1		150		°C
Falling Threshold	T_{FALL}	Note 1		130		°C
PWM Input, IR ATL Mode, Figure 8						
PWM Input High Threshold	V_{IH_ATL}		0.95	1.04	1.12	V
PWM Input Low Threshold	V_{IL_ATL}		0.75	0.84	0.93	V
PWM Tri-level High Threshold	V_{TH_ATL}		2.41	2.65	2.79	V
PWM Tri-level Low Threshold	V_{TL_ATL}		2.21	2.45	2.56	V
PWM Input Current Low	I_{L_ATL}	V_{PWM} = 0V	-130	-100	-65	uA
PWM Input Current Mid	I_{M_ATL}	V_{PWM} = 1.8V	-840	-600	-360	uA
PWM Input Current High	I_{H_ATL}	V_{PWM} = 2.7V	-1.4	-1.0	-0.6	mA
Minimum Recognized PWM Pulse Width	MinPWM	Note 1		50		ns
PWM Input, Tri-State Mode (+3.3V or +5V signal level), Figure 7						
PWM Input Rising Threshold	V_{IH_PWM}		2.41	2.65	2.79	V
PWM Input Falling Threshold	V_{IL_PWM}		0.75	0.84	0.93	V
Tri-State LO_GATE Threshold	V_{TL_PWM}		0.95	1.04	1.12	V
Tri-State LO_GATE Hysteresis	V_{TLH_PWM}			200		mV
Tri-State HI_GATE Threshold	V_{TH_PWM}		2.21	2.45	2.56	V
Tri-State HI_GATE Hysteresis	V_{THH_PWM}			200		mV
Tri-State Hold Off Time	T_{THold_PWM}	Note 1		80		ns
PWM Input Pull-Up Voltage	V_{IT_PWM}	PWM Input Floating	1.40	1.60	1.80	V
PWM Input Resistance	R_{PWM}	PWM Input Floating	3.00	3.75	4.50	kΩ
Minimum Recognized PWM Pulse Width	T_{PWM_MIN}	Note 1		30		ns

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VINDIV						
Divider Ratio	VINDIV	VINDIV / VIN	13	14	15	V/V
Disable VIN Bias	I_{VIN_OFF}				1	µA
VINDIV Input Resistance	R_{VINDIV}			540		kΩ
Enable Inputs (EN1, EN2)						
Enable1 Delay	T_{D_EN1}	Power-on delay			10	µs
Enable2 Delay	T_{D_EN2}	Power-on delay			1	µs
Input High Voltage	V_{IH_EN}		1.15	2.00	2.70	V
Input Low Voltage	V_{IL_EN}		0.54	0.80	1.20	V
Input Resistance	R_{EN}	No UVLO or Over Temperature Fault @ 5V	450	500	550	kΩ
EN1 Fault Pull Down Resistance	$R_{EN\_Pull\_Down}$	Note 1			100	ohm
FUNCTION and MODE						
Input High Voltage	$V_{IH\_FUNC\_MODE}$		2			V
Input Low Voltage	$V_{IL\_FUNC\_MODE}$				0.8	V
Maximum Float Pin Capacitance	$C_{FUNC\_MODE\_MAX}$	Note 1			20	pF
PWMIO						
Input High Voltage	V_{IH_PWMIO}		2			V
Input Low Voltage	V_{IL_PWMIO}				0.8	V
Output High Voltage	V_{OH_PWMIO}		2.5		5	V
Output Low Voltage	V_{OL_PWMIO}		0		0.5	V
Supply						
Supply Bias Current Off	I_{VCC_OFF} + I_{VDRV_OFF}	EN1=0V		1	5	uA
VDRV Supply Bias Current	I_{VDRV}	f_{PWM} = 400kHz, VDRV=5V		30	40	mA
VCC Supply Bias Current	I_{VCC_ATL}	ATL PWM Mode		0.865	2	mA
	I_{VCC_PWM}	Tri-state PWM Mode		1.13	2	mA
VCC Rising Threshold for POR	V_{CC_Rise}			3.85	4.20	V
VCC Falling Threshold for POR	V_{CC_Fall}			3.35		V
VDRV Rising Threshold for POR	V_{DRV_Rise}			3.7	4.20	V
VDRV Falling Threshold for POR	V_{DRV_Fall}			3.28		V

Notes

1. Guaranteed by design but not tested in production
2. V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), VCC=7V, C_{IN}=47uF x 4, C_{OUT} =470uF x3, no airflow, no heat sink, 25°C ambient temperature, and 8-layer PCB of 3.7" (L) x 2.6" (W). PWM controller loss and inductor loss are not included.

TIMING DIAGRAMS

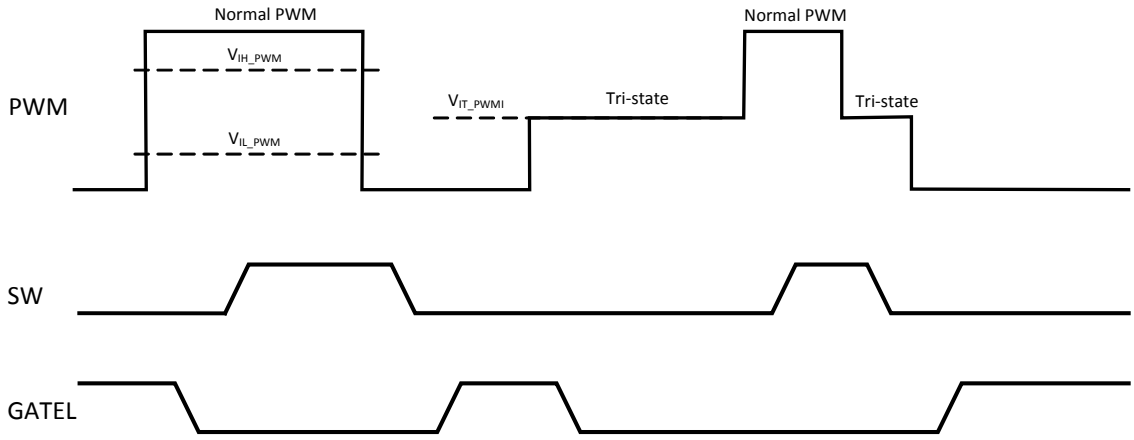


Figure 7: IR3548 Timing Diagram in Standard PWM Mode

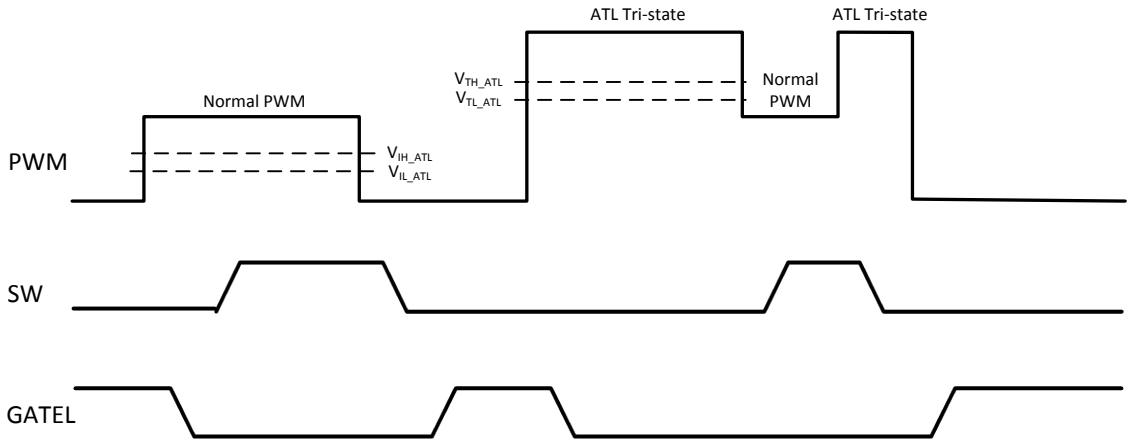
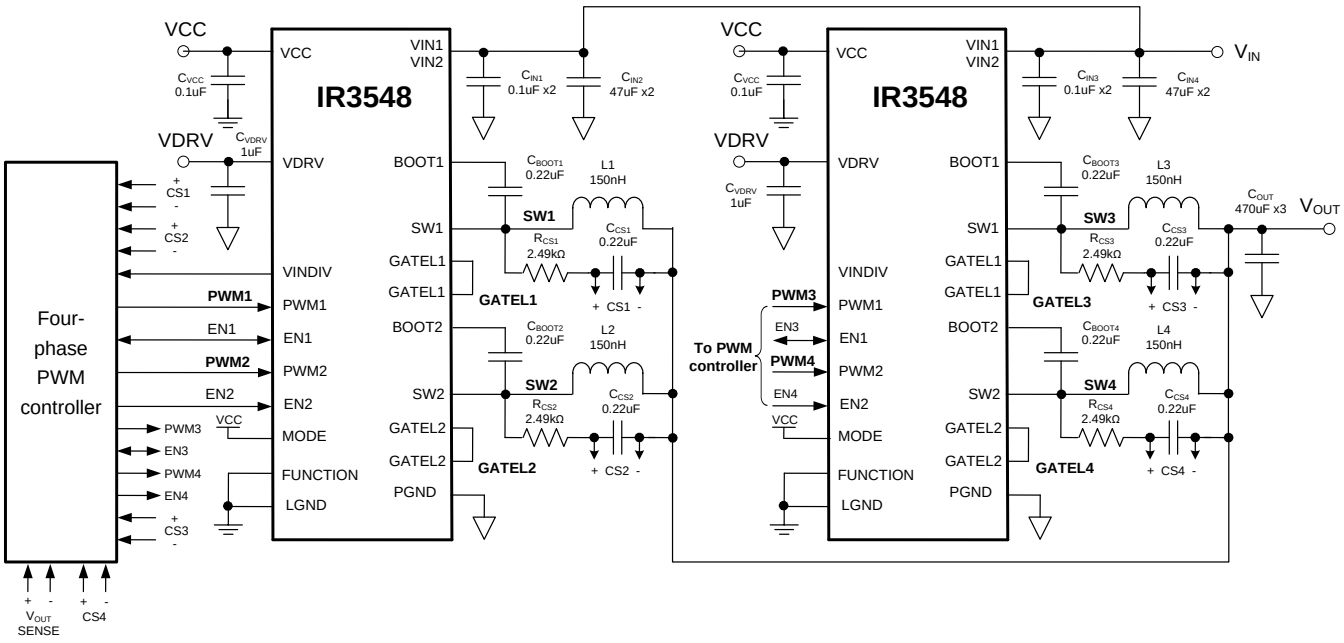


Figure 8: IR3548 Timing Diagram in International Rectifier's Active Tri-Level® (ATL) PWM Mode



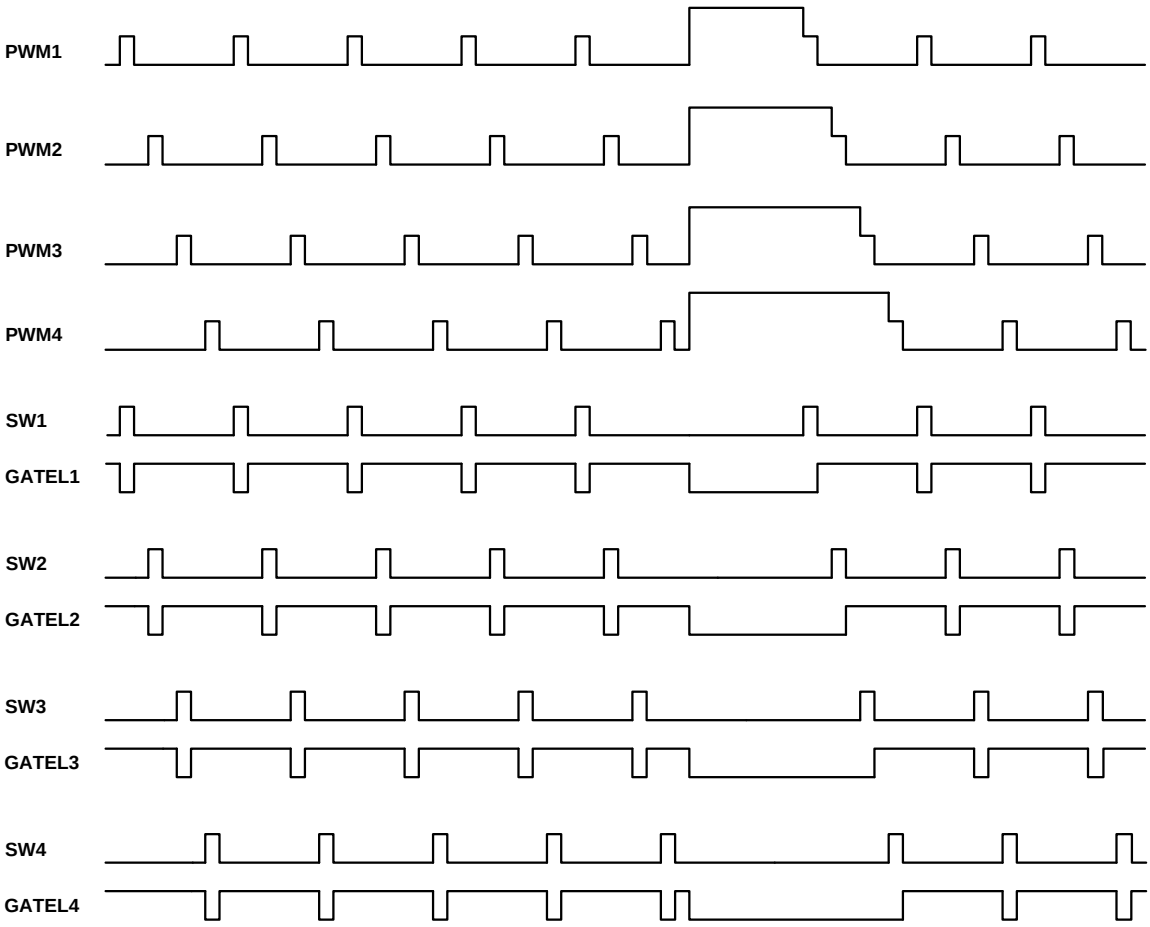
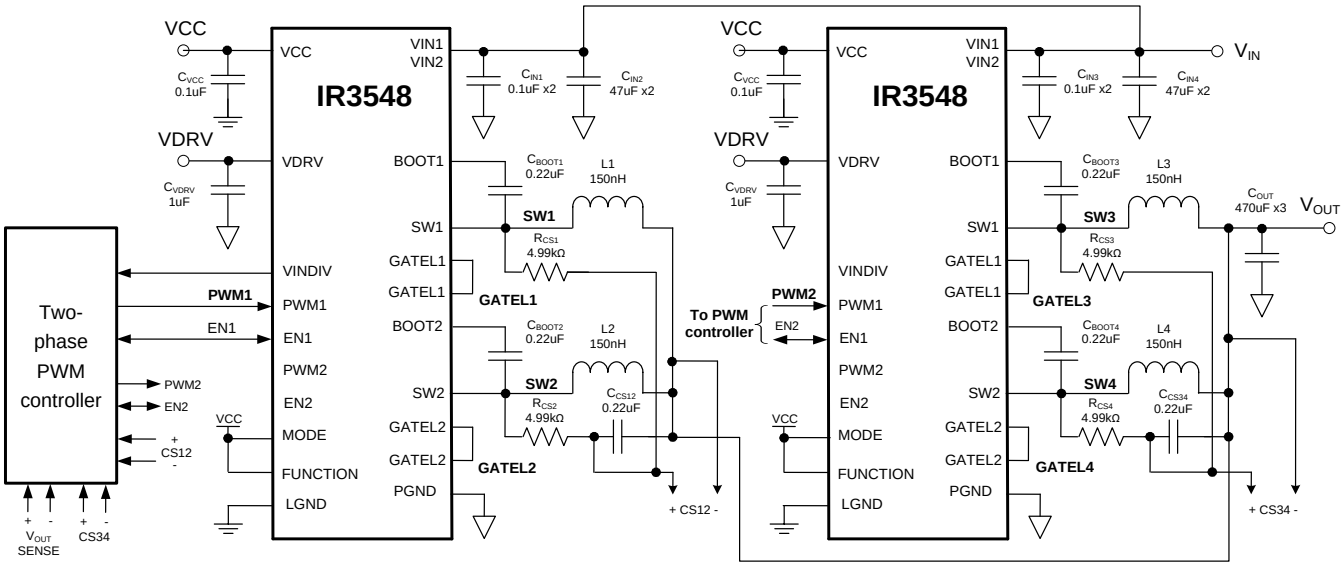


Figure 9: Timing Diagram of the IR3548 Four-phase Voltage Regulator, IR ATL PWM, Dual Driver Mode



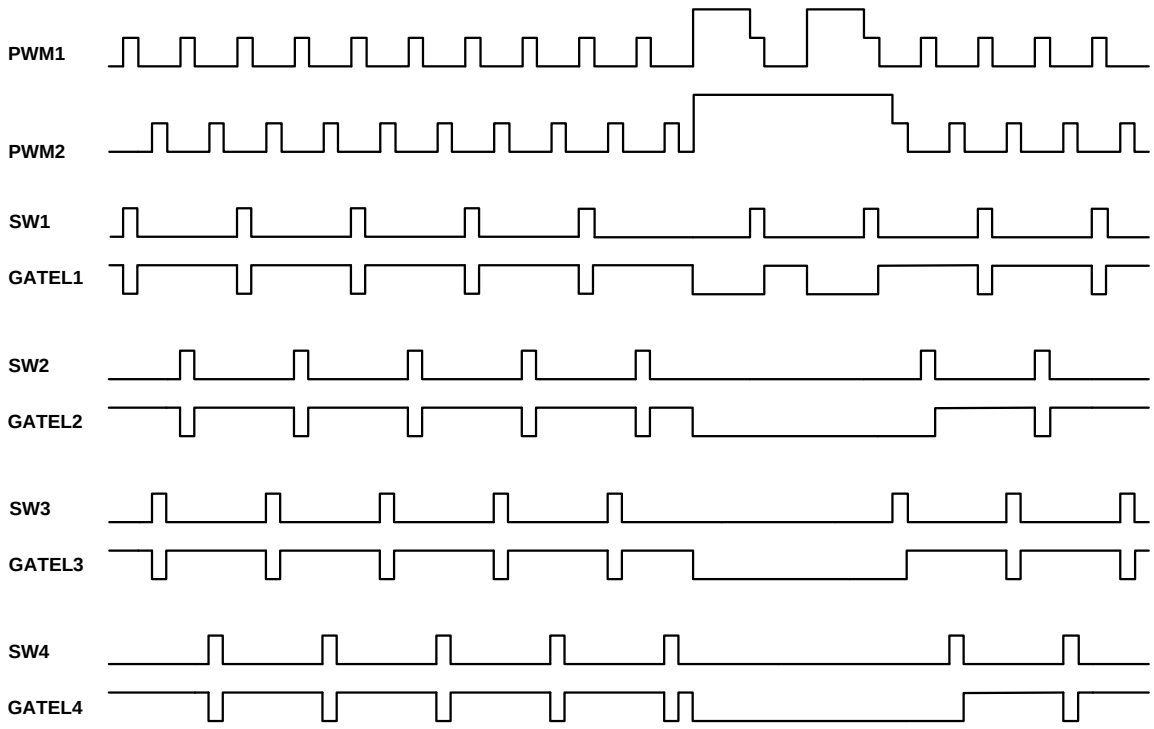
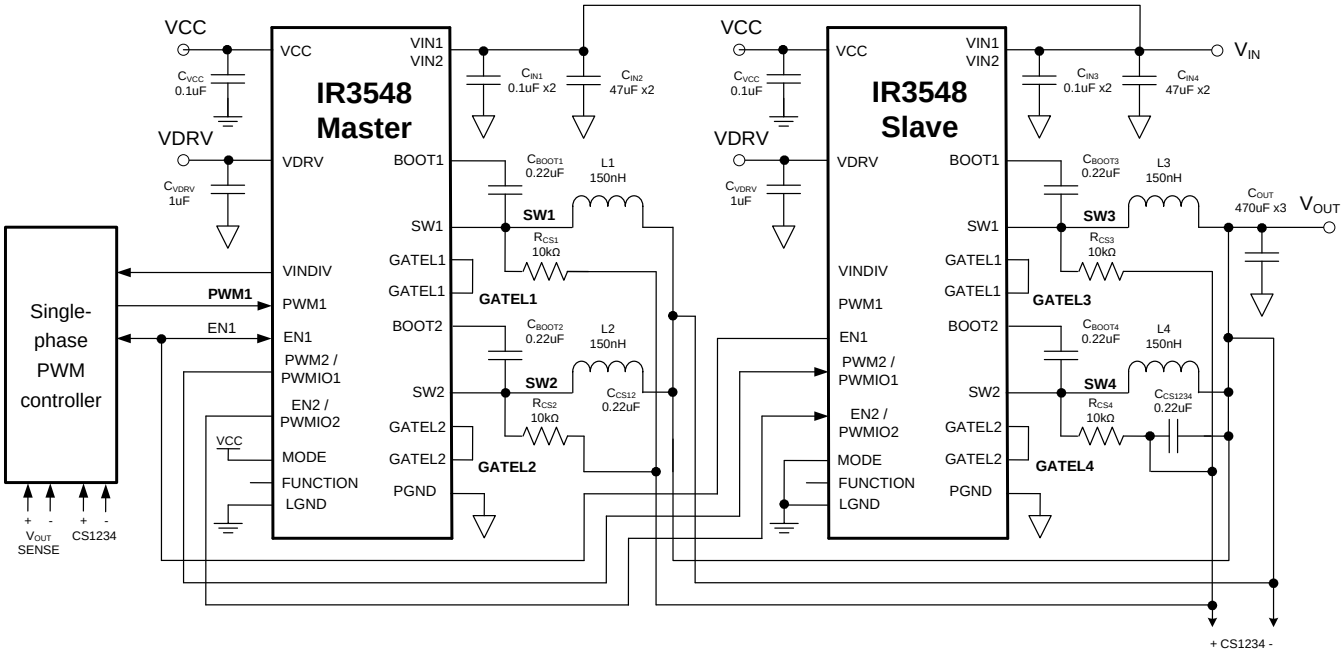


Figure 10: Timing Diagram of the IR3548 Four-phase Voltage Regulator, IR ATL PWM, Doubler Driver Mode



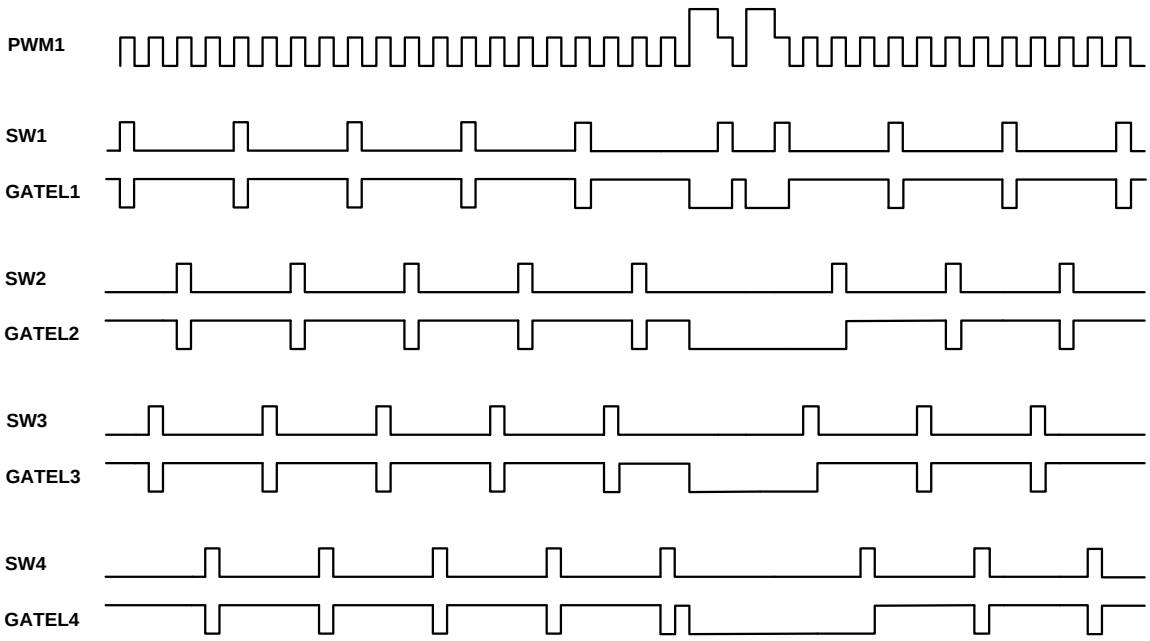


Figure 11: Timing Diagram of the IR3548 Four-phase Vo ltage Regulator, IR ATL PWM, Quad Driver Mode

TYPICAL OPERATING CHARACTERISTICS

Circuit of Figure 34, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), Two Phases, Dual Driver, PWM Mode, Vcc= 5V, VDRV=7V, $T_{AMBIENT}$ = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7”(L) x 2.6”(W), no PWM controller loss, no inductor loss, unless specified otherwise.

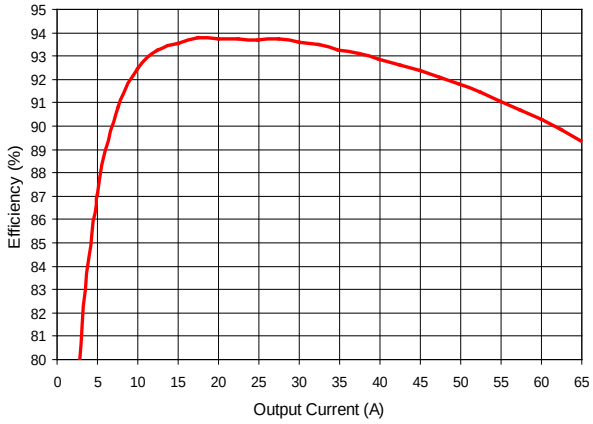


Figure 12: Typical IR3548 Efficiency

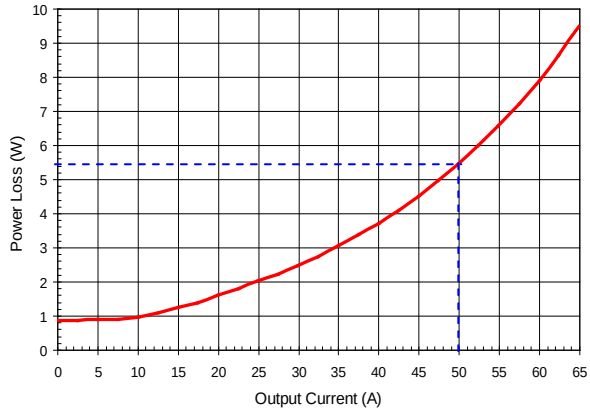


Figure 13: Typical IR3548 Power Loss

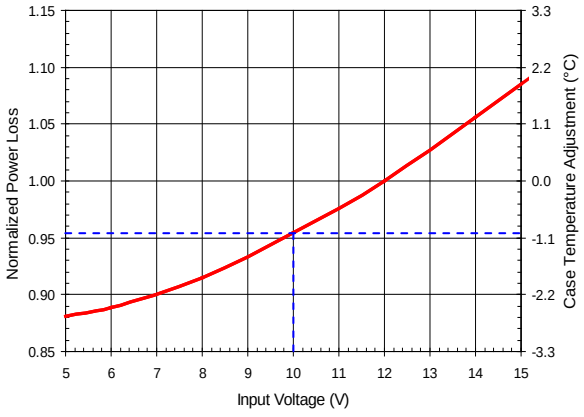


Figure 14: Normalized Power Loss vs. Input Voltage

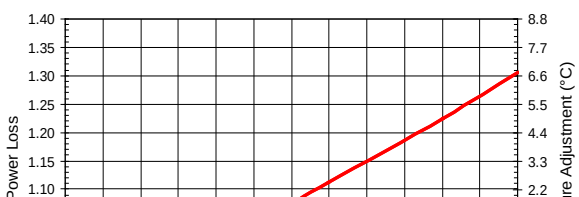


Figure 15: Normalized Power Loss vs. Output Voltage

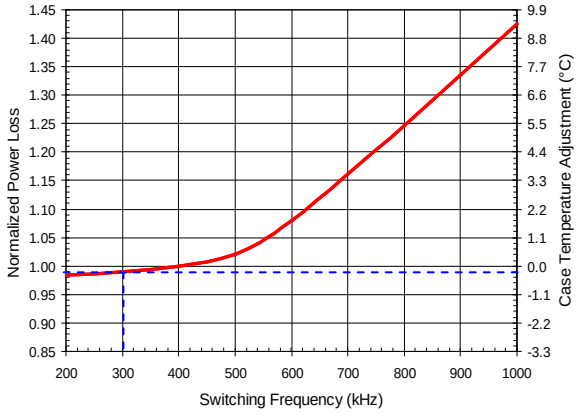


Figure 16: Normalized Power Loss vs. Switching Frequency

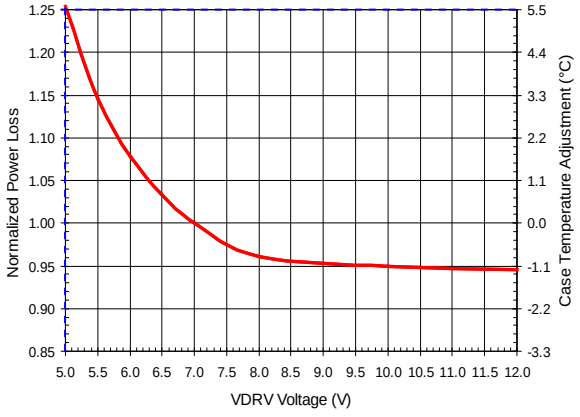


Figure 17: Normalized Power Loss vs. VDRV Voltage

TYPICAL OPERATING CHARACTERISTICS

Circuit of Figure 34, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), Two Phases, Dual Driver, PWM Mode, Vcc= 5V, VDRV=7V, $T_{AMBIENT}$ = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7"(L) x 2.6"(W), no PWM controller loss, no inductor loss, unless specified otherwise.

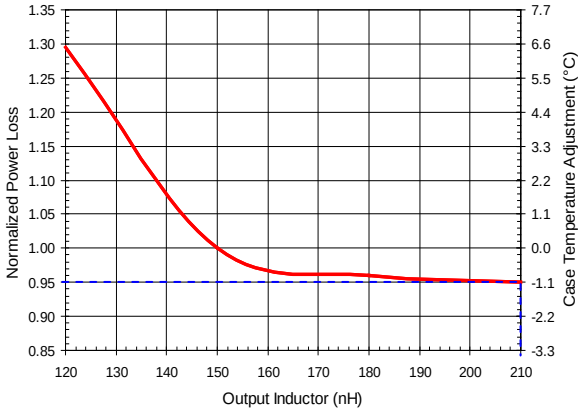


Figure 18 Normalized Power Loss vs. Output Inductor

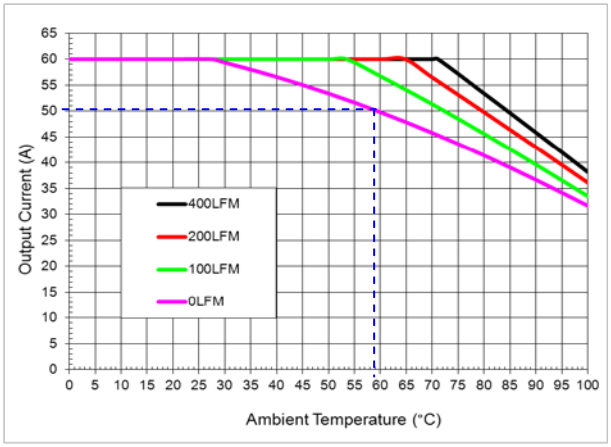


Figure 19 Thermal Derating Curve

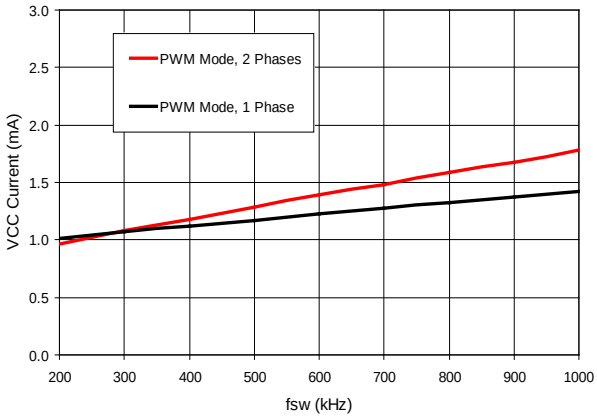


Figure 20 VCC Current vs. Switching Frequency

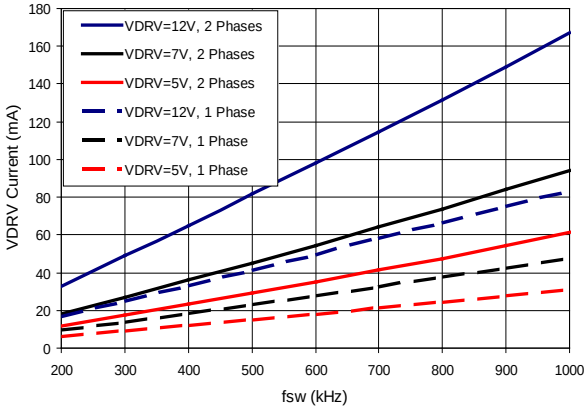


Figure 21 VDRV Current vs. Switching Frequency

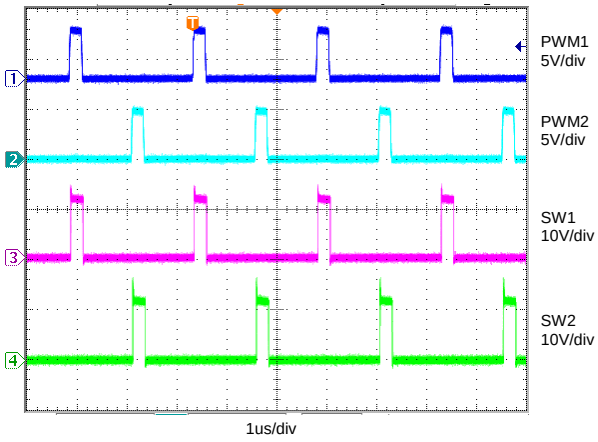


Figure 22 Standard PWM Mode, Dual Driver, 0A

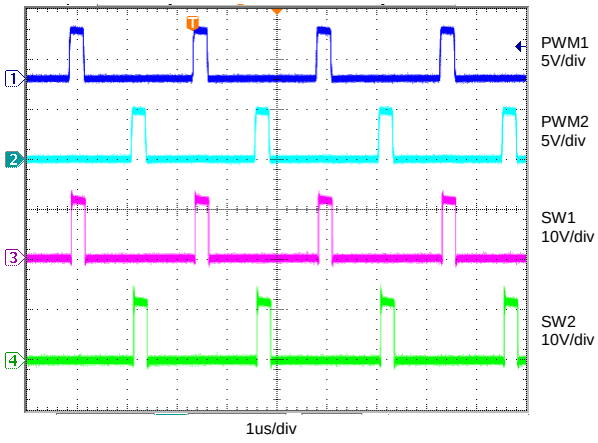


Figure 23 Standard PWM Mode, Dual Driver, 60A

TYPICAL OPERATING CHARACTERISTICS

Circuit of Figure 34, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), Two Phases, Dual Driver, PWM Mode, Vcc= 5V, VDRV=7V, $T_{AMBIENT}$ = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7”(L) x 2.6”(W), no PWM controller loss, no inductor loss, unless specified otherwise.

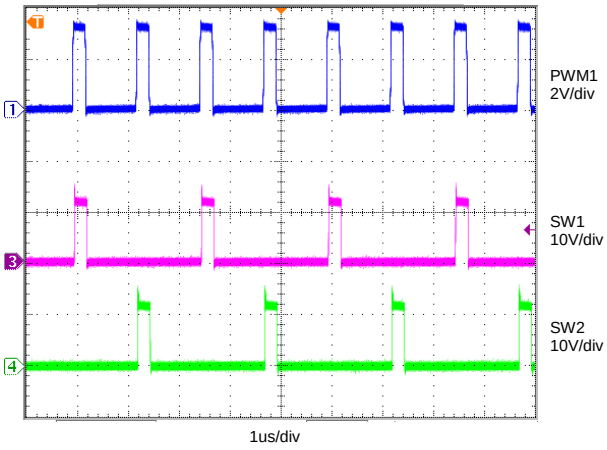


Figure 24 Standard PWM Mode, Doubler Driver, 0A (Circuit of Figure 6)

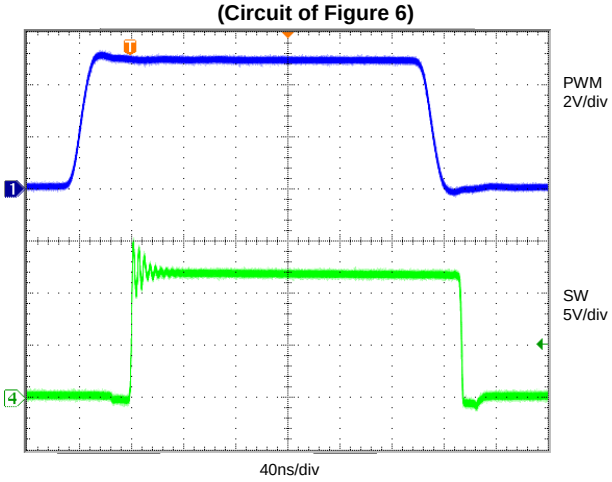


Figure 25 PWM to Switching Delay in PWM Mode, 10A

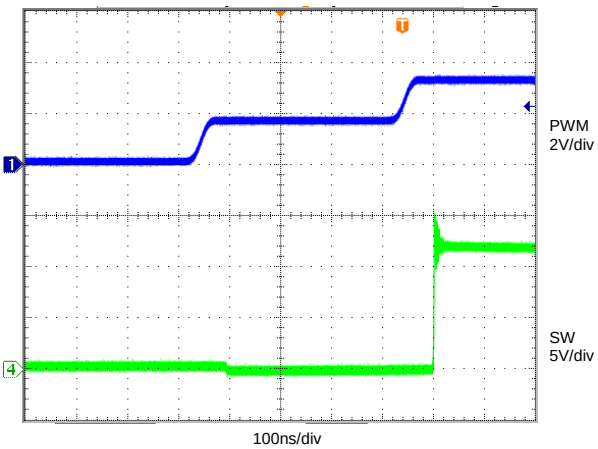


Figure 26 Tristate Delays in PWM Mode, 10A

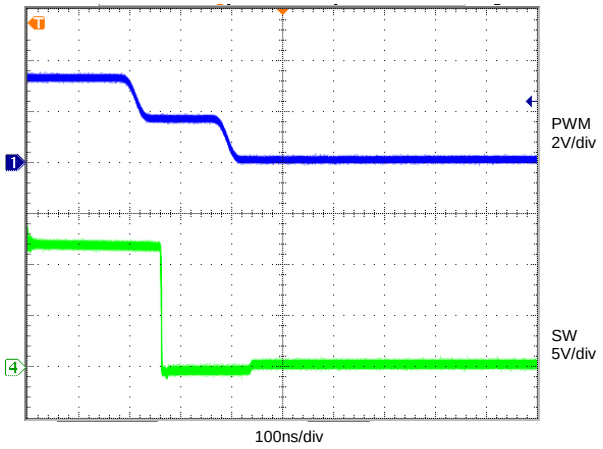


Figure 27 Tristate Delays in PWM Mode, 10A

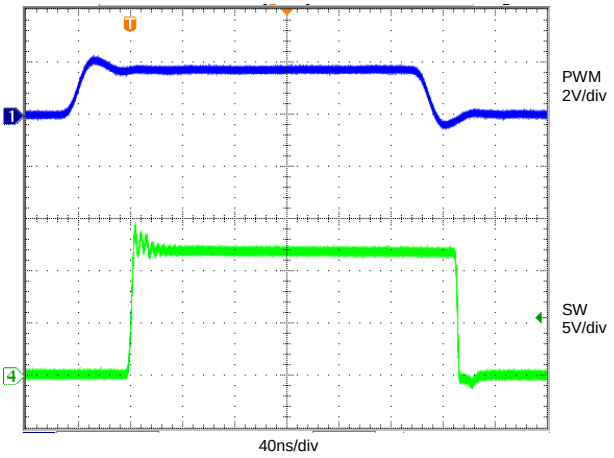


Figure 28 PWM to Switching Delays in IR ATL Mode, 10A (Circuit if Figure 9)

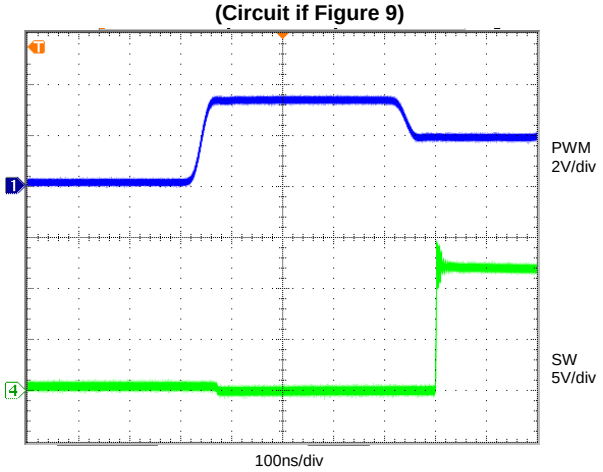


Figure 29 Tristate delays in IR ATL Mode, 10A (Circuit of Figure 9)

TYPICAL OPERATING CHARACTERISTICS

Circuit of Figure 34, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), Two Phases, Dual Driver, PWM Mode, Vcc= 5V, VDRV=7V, $T_{AMBIENT}$ = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7”(L) x 2.6”(W), no PWM controller loss, no inductor loss, unless specified otherwise.

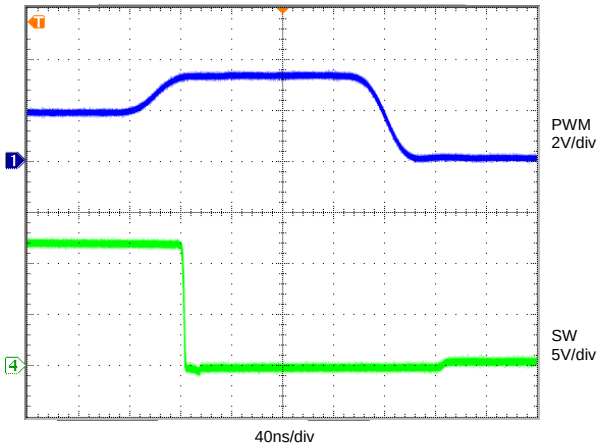


Figure 30 Tristate delays in IR ATL Mode, 10A (Circuit of Figure 9)

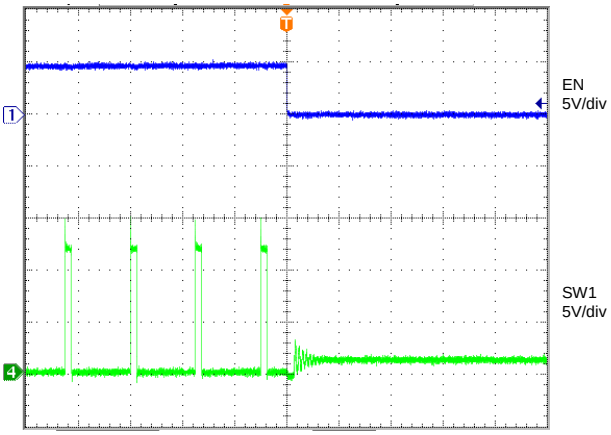


Figure 32 ENABLE Control, 0A

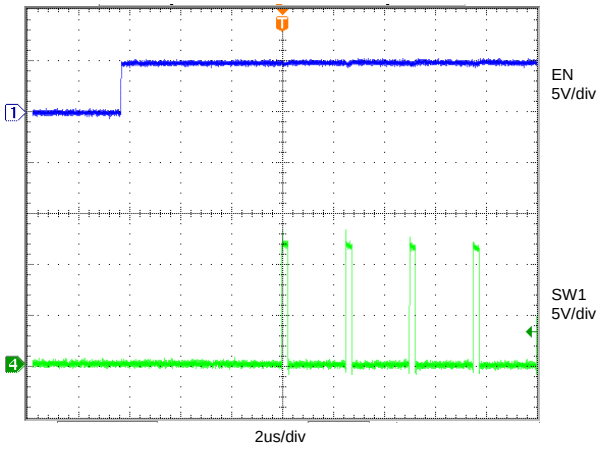


Figure 31 ENABLE Control, 0A

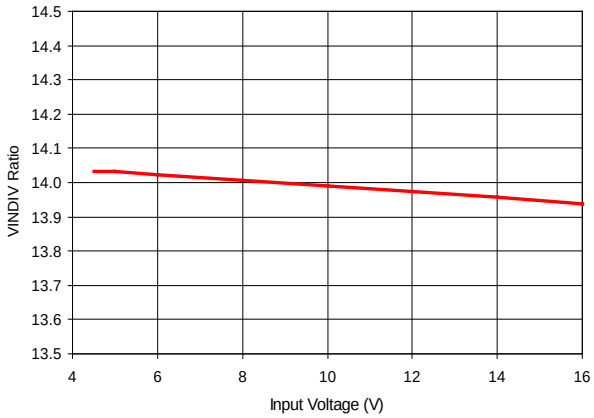


Figure 33 VINDIV to VIN Ratio

GENERAL DESCRIPTION

The IR3548 contains two high-efficiency and high-speed MOSFET drivers optimized to drive two pairs of integrated control and synchronous N-channel MOSFETs up to 1.5MHz.

The IR3548 accepts industry standard 3.3V tri-state PWM signal and is 5V compliant. It also works with International Rectifier's controllers with Active Tri-Level (ATL) PWM outputs. The patented IR ATL PWM allows complete enable and disable control of both MOSFET pairs through the PWM input signal from the controller.

The IR3548 can be configured in three different operating driver modes, Dual driver, Doubler driver and Quad driver so that one PWM signal can control one-, two- or four-phase buck converter.

The IR3548 provides two Enable inputs to control the two independent phases while operating in Dual driver mode, which reduces quiesecent current to 1 uA (typical).

The IR3548 provides Vcc and VDRV Under Voltage Lockout (UVLO) and over temperature fault protection, which pulls low EN1 when the fault occurs. The wide range of the VDRV driver voltage from 4.25V to 12V makes it possible to optimize system efficiency for applications with different switching frequencies, input voltages, and output voltages.

THEORY OF OPERATION

POWER-ON RESET (POR)

The IR3548 incorporates power-on reset protection. This ensures that both the high- and low-side output drivers are active only after the IR3548 supply voltage Vcc and VDRV both have exceeded a certain minimum operating threshold. The Vcc and VDRV supplies are monitored and both drivers are set to the low state, holding both external MOSFETs off.

Once Vcc and VDRV cross the rising POR threshold and if the IR3548 is in IR ATL mode, the outputs are held in the OFF state until a transition from tri-state to active operation is detected at the PWM input. This startup configuration ensures that any undetermined PWM signal levels from a controller in pre-POR state will not result in control MOSFET or synchronous MOSFET turn on until the controller is out of its POR.

For Tri-state PWM mode, the POR operation is the same except that the driver does not look for an input tri-state before functioning.

During normal operation the drivers continue to remain active until Vcc or VDRV fall below their respective falling POR thresholds.

STANDARD 3.3V TRI-STATE PWM MODE

If MODE pin is grounded, the IR3548 accepts standard 3-level 3.3V PWM input signals. As shown in Figure 7, when PWM input is above V_{IH_PWM}, the synchronous MOSFET is turned off and the control MOSFET is turned on. When PWM input is below V_{IL_PWM}, the control MOSFET is turned off and synchronous MOSFET is turned on. If PWM pin is floated, the built-in resistors pull the PWM pin into a tri-state region centered around 1.6V.

IR ACTIVE TRI-LEVEL (ATL) PWM INPUT SIGNAL

When MODE pin is tied to VCC, the IR3548 gate drivers are driven by a patented tri-level PWM control signal provided by the IR digital PWM controllers. During normal operation, the rising and falling edges of the PWM signal transition between 0V and 1.8V to control pulse width modulation of the integrated MOSFETs. To force both MOSFETs off simultaneously, the PWM signal crosses a tri-state voltage level higher than the V_{TH_ATL} tri-state threshold. This threshold based tri-state results in a very fast disable for both the MOSFET pairs with only a small tri-state propagation delay. MOSFET switching resumes when the PWM signal falls below the V_{TL_ATL} tri-state threshold into the normal operating voltage range. Figures 8 shows the PWM input and the corresponding SW and GATEL output of the IR3548.

This fast tri-state operation eliminates the need for any tri-state hold-off time of the PWM signal to dwell in the shutdown window. Dedicated disable or enable pins are not required which simplifies the routing and layout in applications with a limited number of board layers. It also provides the

switching free of shoot-through for slow PWM transition times of up to 20ns. The IR3548 is therefore tolerant of stray capacitance on the PWM signal lines.

The IR3548 provides a pull-up bias current to drive the PWM input to the tri-state condition of 3.3V when the PWM controller output is in its high impedance state. Multi-level pull-up currents are designed to drive worst case stray capacitances and allows for PWM transitions into the tri-state condition rapidly to avoid a prolonged period of MOSFET conduction during faults. The pull-up currents are disabled once the PWM pin exceeds the tri-state threshold to conserve power.

DUAL, DOUBLER OR QUAD DRIVER MODE SELECTION

The FUNCTION pin is used to select three different operating driver modes, Dual driver, Doubler driver and Quad driver so that one PWM can control one-, two- or four-phase buck converter. As shown in Table 1, connecting FUNCTION to LGND sets Dual driver mode while tying FUNCTION pin to Vcc selects Doubler mode. Leaving FUNCTION pin float sets Quad driver mode. These phase modes are shown in Figures 3 to 6 and Figures 9 to 11. Detailed timing diagrams for IR ATL mode can be seen in Figures 9 to 11.

In Dual driver mode, two independent PWM signals control two respective phases with separate ENABLE control. This mode is primarily used in a two-phase converter with a two-phase PWM controller, as shown in Figure 3 and Figure 9. It can also be used in single-phase operation as shown in Figure 5 or in converters with two independent output rails, as shown in Figure 4.

In Doubler driver mode, a single input signal at PWM1 controls two phases, where Phase 1 follows PWM1 signal and Phase 2 is 180° phase behind the PWM1 signal. The current signal of the two phases should be summed and then connected to the PWM controller, as shown in Figure 6 and Figure 10.

In Quad driver mode, two IR3548 devices are used with one configured as a Master and one as a Slave, as shown in Figure 11. One PWM signal at PWM1 controls four phases with the sequence of Phase 1 of the Master IR3548 , Phase 1 of the Slave IR3548, Phase 2 of Master IR3548, and Phase 2 of Slave IR3548. The phase delay is 90° between the phases. The current signal of the four phases should be summed and then connected to the PWM controller.

ENABLE CONTROL

There are two enable inputs in the IR3548, EN1 and EN2. In Dual Mode, each phase has its own enable input. Respective control and synchronous MOSFETs are held off while EN1 and EN2 are low. If only one phase operation is desired, the EN2 pin must be grounded.

In Doubler and Quad modes, only EN1 is available. EN1 low places both phases in high impedance by turning off all four MOSFETs. Internal blocks are shut down to reduce VCC and VDRV quiescent currents to 1uA (typical) when both phases are turned off. The VIN1 input voltage sense resistor divider (VINDIV) is also disconnected when EN1 is low to further reduce bias currents.

The IR3548 is ready to accept PWM activity in less than 10 us after the part is enabled via EN1, as shown in Figure 31.

INTEGRATED BOOTSTRAP PFET

The IR3548 features an integrated bootstrap PFET per phase to reduce external component count. This enables the IR3548 to be used effectively in cost and space sensitive designs.

The bootstrap circuit is used to establish the control MOSFET gate driver bias voltage and consists of a PFET and an external capacitor connected between the SW and BOOT pins of each phase. The external bootstrap capacitor is charged through the PFET when the respective SW node is low.

CONTROL MOSFET DRIVER

Each control MOSFET driver is able to drive a N-channel MOSFET at frequency up to 1.5MHz. The external bootstrap BOOT pin capacitor referenced to the SW node is used to bias the internal MOSFET gate. When the SW node is at ground, the bootstrap capacitor is charged to the VDRV supply voltage using the BOOT PFET and this stored charge is used to bias the internal MOSFET when the PWM signal goes high. Once the control MOSFET is

turned on, the SW voltage is driven to the VIN supply voltage and the BOOT pin voltage is equal to VIN plus the VDRV voltage without any bootstrap diode voltage drop.

When the PWM signal goes low, the control MOSFET is turned off by pulling the gate to the SW voltage.

SYNCHRONOUS MOSFET DRIVER

The IR3548 synchronous MOSFET driver is designed to drive the internal N-channel MOSFET to frequencies of 1.5MHz. The driver is biased from the VDRV supply voltage to turn the MOSFET on.

When the synchronous MOSFET is turned on the SW node is pulled to ground. This allows recharging of the bootstrap capacitor for the next synchronous MOSFET drive event.

ADAPTIVE DEAD TIME ADJUSTMENT

In a synchronous buck converter care should be taken to prevent both control and synchronous MOSFETs from being on simultaneously. Such an event could result in very large shoot-through currents and lead to long term degradation of the power stage. A fixed dead time does not provide optimal performance due to variations in converter duty cycles, bias voltages and temperature.

The IR3548 provides an adaptive dead time adjustment to minimize dead time to an optimum duration which allows for maximum efficiency. The 'break before make' adaptive design is achieved by monitoring gate and SW voltages to determine the ON or OFF status of a MOSFET. Adaptive dead time also provides zero-voltage switching (ZVS) of the synchronous MOSFET with minimum current conduction through its body diode.

During normal operation the PWM transitions between low and high voltage levels to drive the control and synchronous MOSFETs. The high voltage level is 1.8V for IR ATL mode and 3.3V for standard PWM mode.

The PWM signal falling edge transition to a low voltage threshold initiates the control MOSFET driver turn off after a short propagation delay. The dead time control circuit monitors the internal high gate signals and respective SW voltages to ensure the control MOSFET is turned off before turning on the synchronous MOSFET.

The PWM rising edge transition to a high voltage threshold initiates the turn off of the synchronous MOSFET after a small propagation delay. The adaptive dead time circuit provides the appropriate dead time by determining if the synchronous MOSFET gate voltage has crossed the lower threshold before allowing the turn on of the control MOSFET.

INPUT VOLTAGE DIVIDER

The VINDIV can be used to provide input voltage VIN1 information to the PWM controller with a ratio of 1/14 through an internal resistor divider, which is disconnected from VIN1 when EN1 is low to reduce the bias current of the IR3548.

FREQUENCY RANGE

The IR3548 is designed to operate over a wide frequency range. When operating in Dual Mode, the PWM input and respective SW output frequencies are identical. When operating in Doubler mode, the PWM1 input frequency is twice the SW1 or SW2 output frequencies. When operating in Quad mode, the Master PWM1 input frequency is four times the four SW output frequencies.

The lower limit of the output frequency range is dictated by the size of the BOOT capacitor which provides bias to the control MOSFET driver during the entire on-time. The upper limit of frequency is determined by thermal limitations as well as pulse width limitations. The IR3548 is designed to operate with switching frequencies of each phase between 200kHz and 1.5MHz.

USING A DUAL MODE DRIVER AS A SINGLE DRIVER

To use the IR3548 in a single phase converter, simply set Dual mode, ground EN2 pin and leave the unused PWM2 input floating, as shown in Figure 5.

DUAL MODE REACTION TO TRI-STATE PWM INPUT

Anytime there is a tri-state on the PWM1 or PWM2, the respective SW output is tri-stated.

DOUBLER/QUAD MODE REACTION TO TRI-STATE PWM INPUT

In Dual and Quad mode, anytime there is a tri-state on the master PWM1, all outputs (SW1 and SW2) are tri-stated. When the PWM1 transitions from a tri-state to a high and then from a high to a low, only Phase 1 (SW1) operates. This allows the VR to operate properly in PS2 mode and during load releases. In Quad mode, both PWMIO1 and PWMIO2 signals of the master IR3548 go to 5V when PWM1 is tri-state to force the slave IR3548 to keep both control and synchronous MOSFETs off.

Once the PWM1 sees a transition from a low to a high (absence of tri-state), the driver leaves single phase operation and returns to the Doubler or Quad functionality, as shown in Figure 10 and Figure 11.

APPLICATION INFORMATION

CONFIGURING THE PWM AND PHASE MODES

The IR3548 can operate in 3 different PWM input modes including Dual, Doubler and Quad Modes (Master and Slave). Dual and Doubler modes can accept either an IR ATL input PWM signal or a Tri-State PWM signal (3.3V or 5V) while Quad mode can only accept ATL mode since PWM tri-state transition delays can not be tolerated when the PWM needs to operate at 4 times the switching frequency.

Table 1 on page 3 shows the configuration of both the PWM modes and the driver modes utilizing the FUNCTION and MODE pins. Note that depending on the MODE selected in Table 1, Pin 14 (PWM2 / PWMIO1) and Pin 15 (EN2 / PWMIO2) change functions as well.

The FUNCTION and MODE selection pins are latched into the IR3548 at power up and during EN1 cycling, and cannot be changed after these events.

POWER LOSS CALCULATION

The two-phase IR3548 efficiency and power loss measurement circuit is shown in Figure 34.

The IR3548 power loss is determined by,

$$P_{LOSS} = V_{IN} \times I_{IN} + V_{CC} \times I_{VCC} + V_{DRV} \times I_{VDRV} - (V_{SW1} + V_{SW2}) \times I_{OUT} / 2$$

Where both MOSFET loss and the driver loss are included, but the PWM controller and the inductor losses are not included.

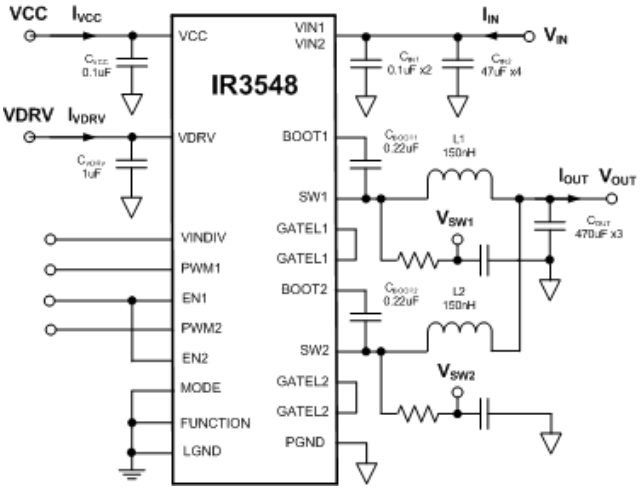


Figure 34: IR3548 Power Loss Measurement

Figure 12 shows the measured two-phase IR3548 efficiency under the default test conditions, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), Dual driver mode, VDRV=7V, $T_{AMBIENT}$ = 25°C, no heat sink, and no air flow.

The measured two-phase IR3548 power loss under the same conditions is provided in Figure 13.

If any of the application conditions, i.e. input voltage, output voltage, switching frequency, VCC MOSFET driver voltage or inductance, is different from those of Figure 13, a set of normalized power loss curves should be used. Obtain the normalizing factors from Figure 14 to Figure 18 for the new application conditions; multiply these factors by the power loss obtained from Figure 13 for the required load current.

As an example, the power loss calculation procedures under different conditions, V_{IN}=10V, V_{OUT}=1V, f_{SW} = 300kHz, L=210nH, VCC=5V, VDRV=5V, I_{OUT}=50A, $T_{AMBIENT}$ = 25°C, no heat sink, and no air flow, are as follows.

1) Determine the power loss at 50A under the default test conditions of V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH, VCC=5V, VDRV=7V, $T_{AMBIENT}$ = 25°C, no heat sink, and no air flow. It is 5.5W from Figure 13.

2) Determine the input voltage normalizing factor with V_{IN}=10V, which is 0.96 based on the dashed lines in Figure 14.

3) Determine the output voltage normalizing factor with V_{OUT}=1V, which is 0.94 based on the dashed lines in Figure 15.

4) Determine the switching frequency normalizing factor with f_{SW} = 300kHz, which is 0.99 based on the dashed lines in Figure 16.

5) Determine the VDRV MOSFET drive voltage normalizing factor with VDRV=5V, which is 1.25 based on the dashed lines in Figure 17.

6) Determine the inductance normalizing factor with L=210nH, which is 0.95 based on the dashed lines in Figure 18.

7) Multiply the power loss under the default conditions by the five normalizing factors to obtain the power loss under the new conditions, which is 5.5W x 0.96 x 0.94 x 0.99 x 1.25 x 0.95 = 5.83W.

THERMAL DERATING

Figure 19 shows the IR3548 thermal derating curve with the case temperature controlled at or below 125°C. The test conditions are V_{IN}=12V, V_{OUT}=1.2V, f_{SW}=400kHz, L=150nH (0.29mΩ), VDRV=7V, $T_{AMBIENT}$ = 0°C to 100°C, no heat sink, and Airflow = 0LFM / 100LFM / 200LFM / 400LFM.

If any of the application condition, i.e. input voltage, output voltage, switching frequency, VDRV MOSFET driver voltage, or inductance is different from those of Figure 19, a set of IR3548 case temperature adjustment curves should be used. Obtain the temperature deltas from Figure 14 to Figure 18 for the new application conditions; sum these deltas and then subtract from the IR3548 case temperature obtained from Figure 19 for the required load current.

The IR3548 safe operating area is obtained with the case temperature controlled at or below 125°C. If a lower case temperature is desired, reduce the highest ambient temperature by the same delta.

As an example, the highest ambient temperature calculation procedures for a different operating condition, V_{IN}=10V, V_{OUT}=1V, f_{SW} = 300kHz, L=210nH, VDRV = 5V, I_{OUT}=50A, $T_{AMBIENT}$ = 25°C, no heat sink, and no air flow, are as follows.

8) From Figure 19, determine the highest ambient temperature at the required load current under the default conditions, which is 59°C at 50A with 0LFM airflow and the IR3548 case temperature of 125°C.

9) Determine the case temperature with V_{IN}=10V, which is -1.0° based on the dashed lines in Figure 14.

10) Determine the case temperature with V_{OUT}=1V, which is -1.4° based on the dashed lines in Figure 15.

11) Determine the case temperature with f_{SW} = 300kHz, which is -0.2° based on the dashed lines in Figure 16.

12) Determine the case temperature with VDRV = 5V, which is +5.5° based on the dashed lines in Figure 17.

13) Determine the case temperature with L=210nH, which is -1.1° based on the dashed lines in Figure 18.

14) Sum the case temperature adjustment from 9) to 13), -1.0° -1.4° -0.2° +5.5° -1.1° = +1.8°. Deduct the delta from the highest ambient temperature in step 8), 59°C - (+1.8°C) = 57.2°C.

15) If the desired IR3548 case temperature is 105°C instead of 125°C, subtract 20°C (=125°C - 105°C) from the highest ambient temperature obtained from 14), i.e. 57.2°C - 20°C = 37.2°C.

INPUT CAPACITORS C_{VIN}

At least one 10uF 1206 ceramic capacitors and one 0.1uF 0402 ceramic capacitor are recommended for decoupling the VIN1 and VIN2 to PGND connection. The 0.1uF 0402 capacitor should be on the same

side of the PCB as the IR3548 and next to the VIN1/VIN2 and PGND pins. Adding additional capacitance and use of capacitors with lower ESR and mounted with low inductance routing will improve efficiency and reduce overall system noise, especially in single-phase designs or during high current operation.

BOOTSTRAP CAPACITORS C_{BOOT1} AND C_{BOOT2}

A minimum of 0.22uF 0402 capacitor is required for the bootstrap circuit. It should be mounted on the same side of the PCB as the IR3548 and as close as possible to the BOOT1 / BOOT2 pin. A low inductance routing of the SW1 / SW2 pin connection to the other terminal of the bootstrap capacitor is strongly recommended.

VCC AND VDRV DECOUPLING CAPACITORS C_{VCC} AND C_{VDRV}

A 0.1uF ceramic decoupling capacitor is required at the VCC pin. A 1uF ceramic decoupling capacitor is required at the VDRV pin. They should be mounted on the same side of the PCB as the IR3548. The VCC capacitor should be as close as possible to the VCC and LGND. The VDRV capacitor should be as close as possible to HVCC/LVCC and PGND (pin 10). Low inductance routing for the decoupling capacitors is strongly recommended.

PCB LAYOUT CONSIDERATIONS

PCB layout and design is important to driver performance in voltage regulator circuits due to the high current slew rate (di/dt) during MOSFET switching. Contact International Rectifier for a layout example suitable for your specific application.

- Locate all power components in each phase as close to each other as practically possible in order to minimize parasitics and losses, allowing for reasonable airflow.
- Input supply decoupling and bootstrap capacitors should be physically located close to their respective IC pins.
- GATEL1 and GATEL2 interconnect trace inductances should be minimized to prevent Cdv/dt turn-on of the low side MOSFETs.
- The ground connection of the IC should be as close as possible to the low-side MOSFET source.
- Use of a copper plane under and around the IC and thermal vias to connect to buried copper layers improves the thermal performance substantially.

METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to prevent shorting.
- Lead land length should be equal to maximum part lead length +0.15 - 0.3 mm outboard extension and 0 to + 0.05mm inboard extension. The outboard extension ensures a large and visible toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width.
- Only 0.30mm diameter via shall be placed in the area of the power pad lands and connected to power planes to minimize the noise effect on the IC and to improve thermal performance.

SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist miss-alignment is a maximum of 0.05mm and it is recommended that the low power signal lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensures NSMD pads.
- The minimum solder resist width is 0.13mm typical.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The power land pads VIN, PGND, and SW should be Solder Mask Defined (SMD).
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

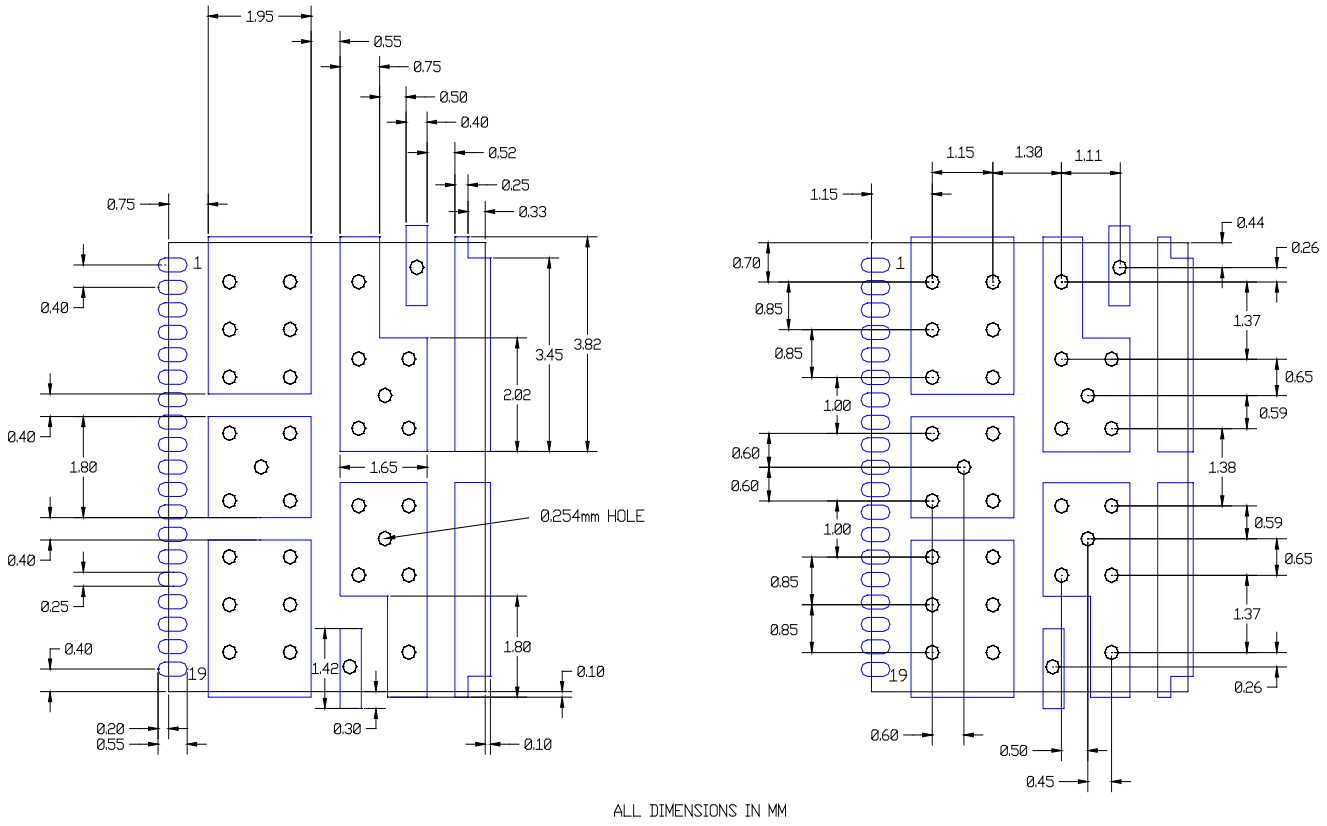


Figure 35: Solder resist

STENCIL DESIGN

- The stencil apertures for the lead lands should be approximately 65% to 75% of the area of the lead lands depending on stencil thickness. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The low power signal stencil lead land apertures should therefore be shortened in length to keep area ratio of 65% to 75% while centered on lead land.
- The power pads VIN, PGND and SW, land pad apertures should be approximately 65% to 75% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open. Solder paste on large pads is broken down into small sections with a minimum gap of 0.2mm between allowing for out-gassing during solder reflow.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.

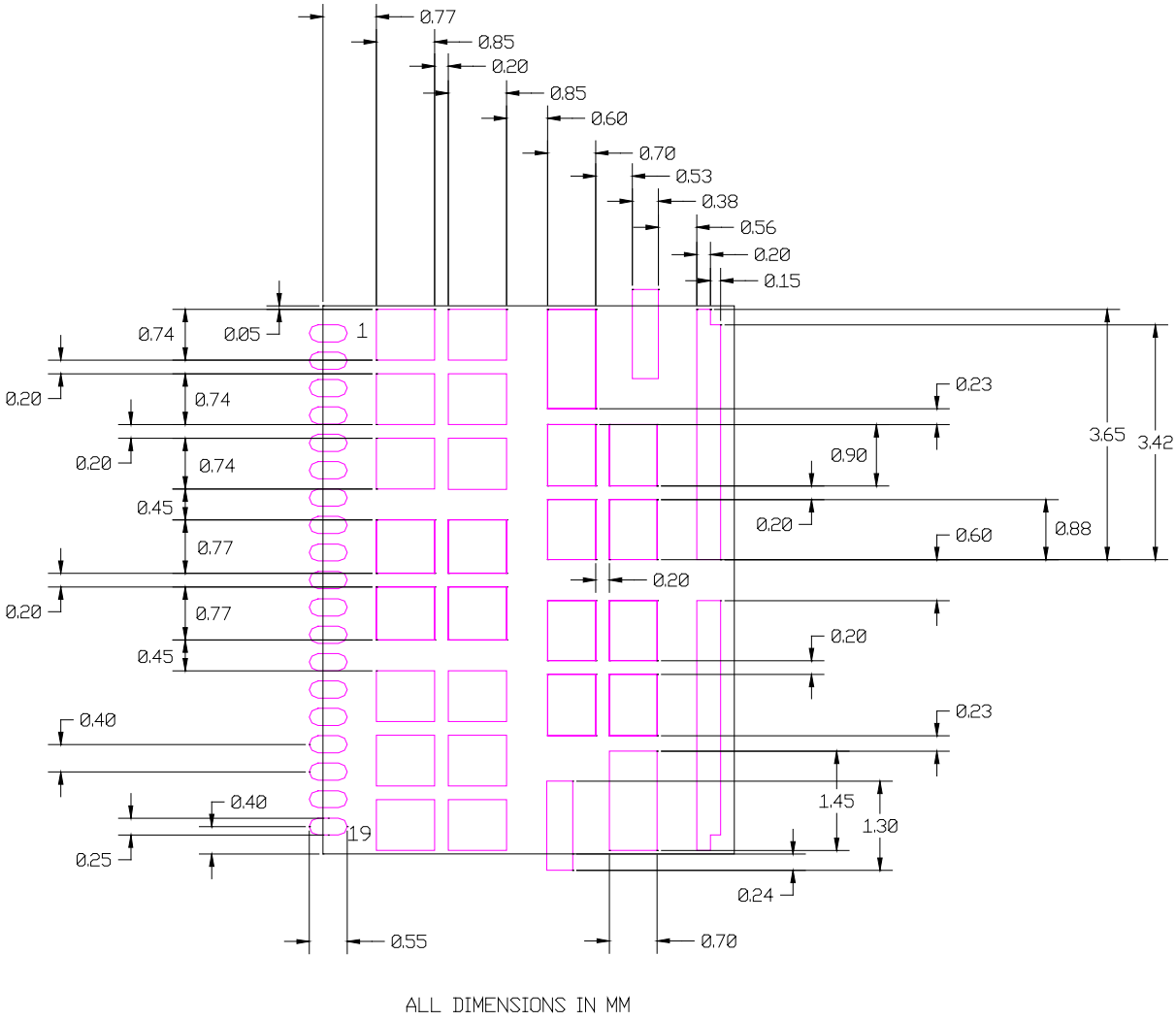


Figure 36: Stencil design

* Contact International Rectifier to receive an electronic PCB Library file in Cadence Allegro or CAD DXF/DWG format.

MARKING INFORMATION

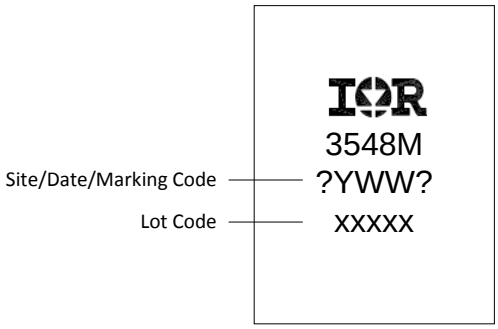
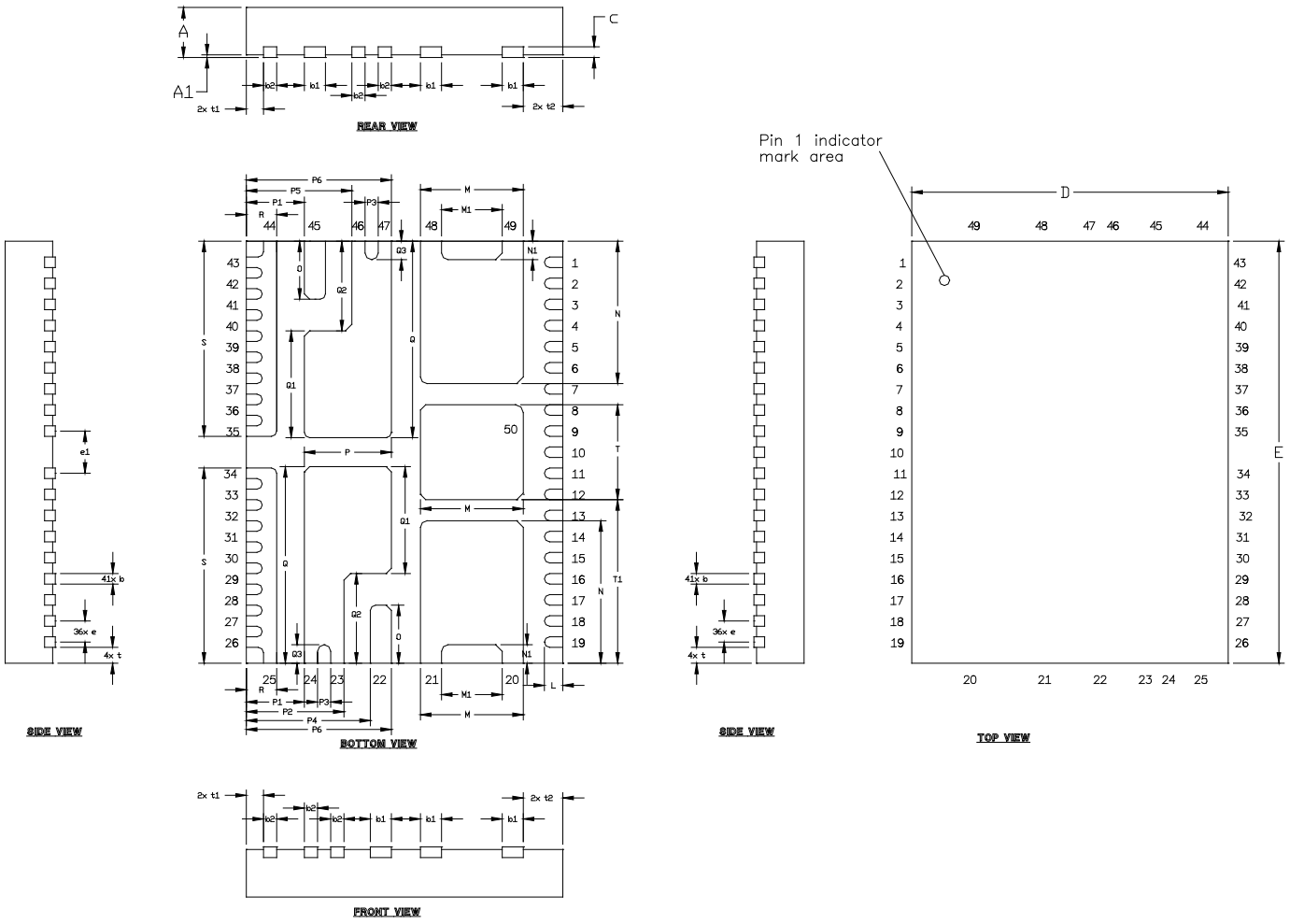


Figure 37: PQFN 6mm x 8mm

PACKAGE INFORMATION



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.800	1.000	.0315	.0394
A1	0.000	0.050	.0000	.0020
b	0.150	0.250	.0059	.0098
b1	0.350	0.450	.0138	.0177
b2	0.200	0.300	.0079	.0118
c	0.203 REF.		.0080 REF.	
D	6.000 BASIC		.2362 BASIC	
E	8.000 BASIC		.3150 BASIC	
e	0.400 BASIC		.0157 BASIC	
e1	0.800 BASIC		.0315 BASIC	
t	0.300 BASIC		.0118 BASIC	
t1	0.325 BASIC		.0128 BASIC	
t2	0.750 BASIC		.0295 BASIC	
L	0.300	0.400	.0118	.0157
M	1.900	2.000	.0748	.0787
M1	1.100	1.200	.0433	.0472
N	2.650	2.750	.1043	.1083
N1	0.300	0.400	.0118	.0157

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
O	1.050	1.150	.0413	.0453
P	1.600	1.700	.0630	.0669
P1	1.050	1.150	.0413	.0453
P2	1.800	1.900	.0709	.0748
P3	0.200	0.300	.0079	.0118
P4	2.300	2.400	.0906	.0945
P5	1.950	2.050	.0768	.0807
P6	2.700	2.800	.1063	.1102
Q	3.675	3.775	.1447	.1486
Q1	1.975	2.075	.0778	.0817
Q2	1.650	1.750	.0650	.0689
Q3	0.300	0.400	.0118	.0157
R	0.525	0.625	.0207	.0246
S	3.650	3.750	.1437	.1476
T	1.750	1.850	.0689	.0728
T1	3.050	3.150	.1201	.1240

Figure 38: PQFN 6mm x 8mm

Data and specifications subject to change without notice.
This product will be designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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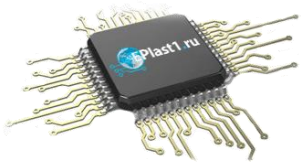
- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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