Enpirion® Power Management Evaluation Board User Guide

ES1030 Four-Channel Sequencer with Digital Feedback

Description

This document describes the connections to and the testing of the ES1030 four-channel power regulator sequencer evaluation board (EVB). The ES1030QI can be chained to provide nested sequencing for over 16 power regulators. The part comes in a tiny 2x3 mm Quad Flat No-lead (STQFN) package and uses the power good (PG) signals from the regulators to confirm the desired sequence is being produced. A complete sequencing solution requires only a few small signal components. A precise sequencing delay is set by a resistor divider from the internally provided reference.

Introduction

The ES1030 sequencer EVB contains one four-channel sequencer chip and component locations and jumpers for flexible connections to the four output ENABLE signals (OE1, OE2, OE3, OE4) and the four digital feedback signals (PG1, PG2, PG3, and PG4). The EVB also provides the chaining signals nFLT_IN, nFLT_O, OE_O, NEXT_IN, and NEXT_O. You can connect multiple EVBs with these chaining signals to provide nested sequencing for additional channels.

Signals to the sequencer are available on the single-row headers on the left and right edges of the EVB. The three-pin headers allow jumpered pull-ups or pass-through of the signals to the single-row headers. The resistor positions provide series and shunt locations for implementing pass-through, divider, or pull-down connections to the signals. The default population of the EVB is for a single four-channel sequencer. Chained operation of multiple EVBs requires some jumper and component changes.

Evaluation Board Overview

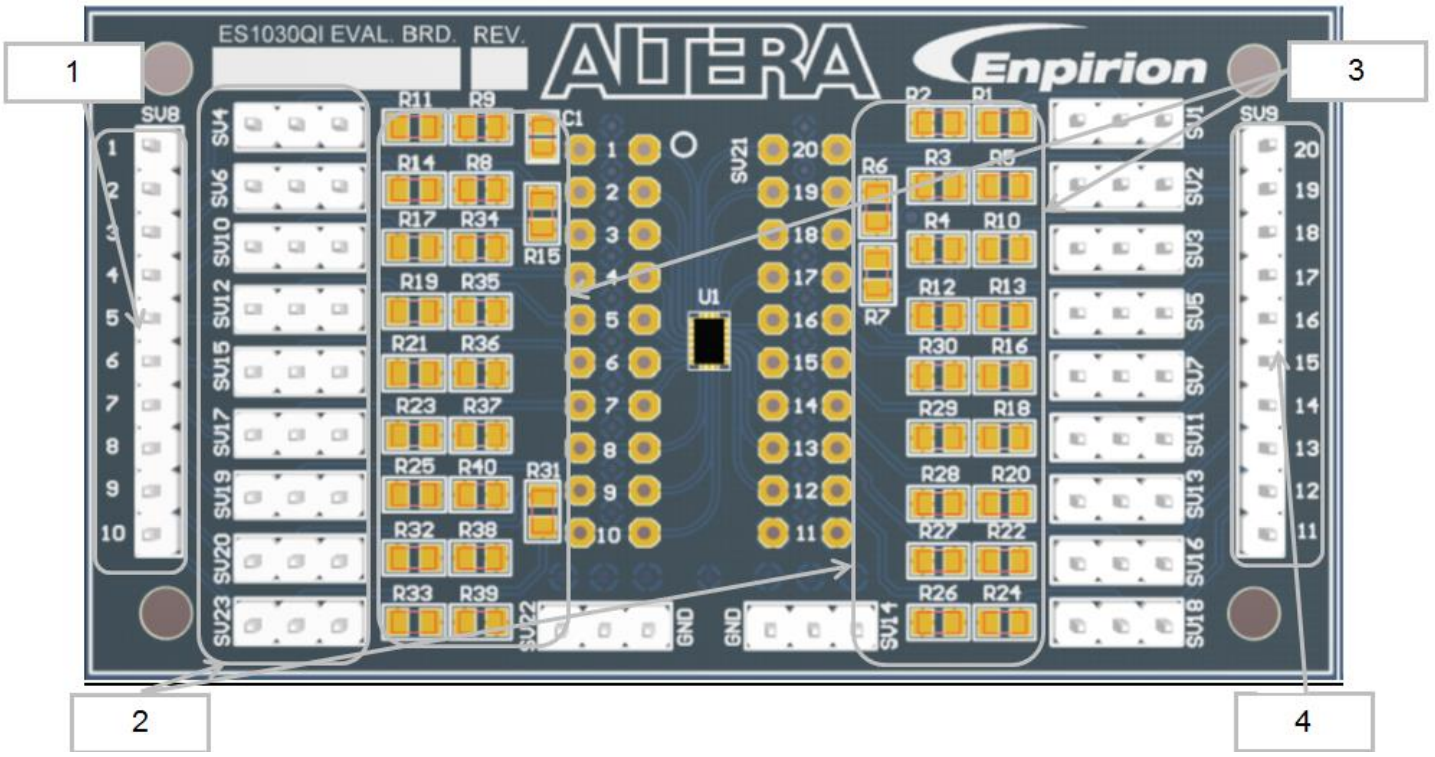


Figure 1: ES1030QI Evaluation Board

Evaluation Board Operating Instructions

In the following instructions, the numbers in brackets [ ] correspond to the numbers in Figure 1.

> **CAUTION**: This kit contains circuitry that is sensitive to static electricity. Please use anti-static precautions before touching or handling the EVB.

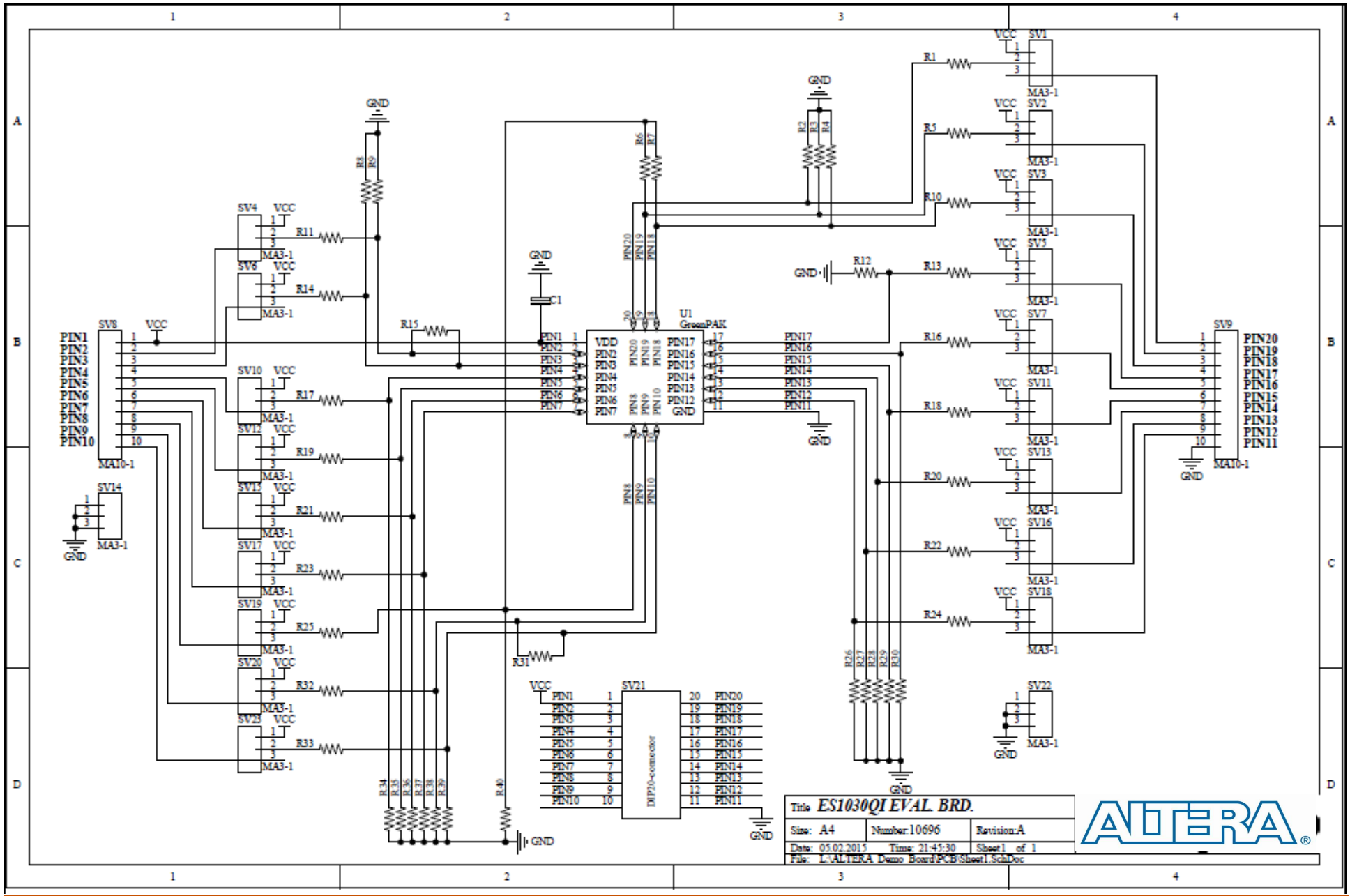
1) **Connect the EVB:**
   - Locate the ES1030 EVB in the kit and connect it to the equipment used for testing. The supply voltage (1.62-5.5V) is connected to SV8 Pin 1 [1] and ground at SV9 Pin 10 [4].
   - For repeated triggering of the sequence, connect a square-wave signal generator to SV9 Pin1 (EN) and GND. The signal amplitude should match the nominal supply voltage (check the terminator requirements), and the frequency should be no more than 10 Hz.
   - Connect the output enable signals (OEx) and power good signals (PGx) to the power regulators to be sequenced, and connect OEx and PGx to an oscilloscope or logic analyzer for observation. For demonstration without external regulators, connect PG1=OE1, PG2=OE2, and so on.
2) **Apply Power:**
   - Apply power to the VDD supply. The OE and PG signals should show a nested sequencing pattern (1-2-3-4 rising and 4-3-2-1 falling).
3) **Test the Module:**
   - To adjust the time delay between successive enables and the qualification window for the PG signals from 0.033ms to 8.04ms, you can change the divider ratio formed by R7 and R40 (keep R7+R40>100kohms). If PG does not rise within the qualification window after the corresponding OE signal, a fault is produced (shown by LOW on nFAULT_O) and the sequence reverses.

For more information, refer to the Enpirion Power Datasheet: *ES1030 Power Rail Sequencer*.

Table of Connections

HEADER/PIN # [1][4]	FUNCTION	IC PIN #	DEFAULT JUMPERS [2]	DEFAULT RESISTORS [3]
SV8/1	VCC/VDD	1	NA	NA
SV8/2	nFAULT_IN	2	SV4 2-3	R11=0, R15=0
SV8/3	nFAULT_O	3	SV6 1-2	R14=100k
SV8/4	OE4	4	SV10 2-3	R17=0
SV8/5	OE3	5	SV12 2-3	R19=0
SV8/6	PG3	6	SV15 2-3	R21=0
SV8/7	PG4	7	SV17 2-3	R23=0
SV8/8	ACNTL	8	NA	R7=100k, R40=100k
SV8/9	NEXT_O	9	NA	R31=0
SV8/10	NEXT_IN	10	NA	NA
SV9/1	EN	20	SV1 2-3	R1=0
SV9/2	OE_O	19	NA	NA
SV9/3	REF_O	18	NA	NA
SV9/4	ALL_PG	17	SV5 2-3	R13=0
SV9/5	POR	16	NA	R16=0
SV9/6	OE1	15	SV11 2-3	R18=0
SV9/7	OE2	14	SV13 2-3	R20=0
SV9/8	PG2	13	SV16 2-3	R22=0
SV9/9	PG1	12	SV18 2-3	R24=0
SV9/10	GND	11	NA	NA

Evaluation Board Schematic



Application Schematic for Four-Channel Nested Sequencer

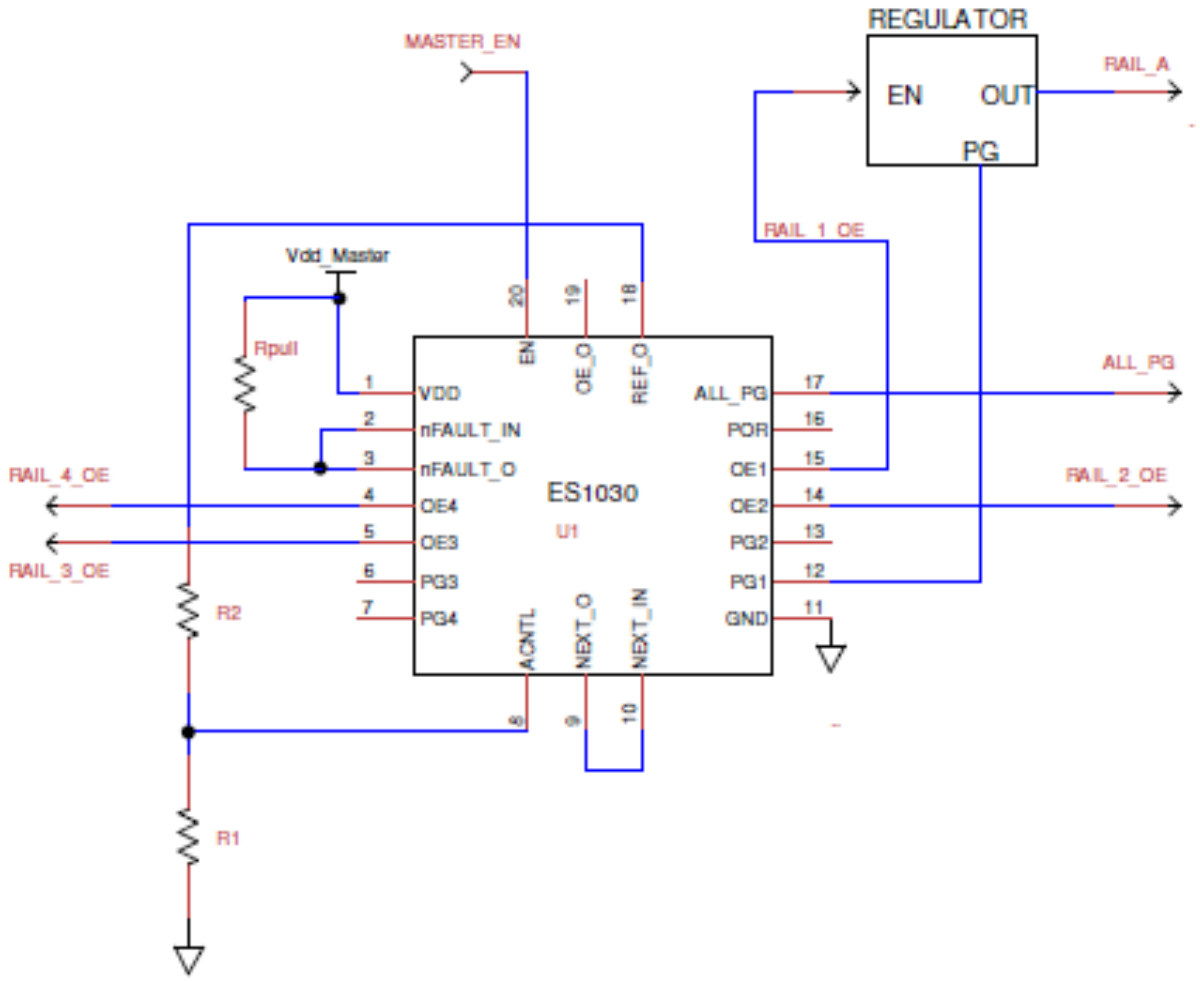


Figure 2: Stand Alone Operation

Notes to **Figure 2**:

1. Unused PG pins may be floated or tied to VDD.
2. ACNTL controls delays based on voltage ratio relative to REF_O: full scale delay (ACTRL at REF_O) is 8.04ms; minimum delay (ACTRL at GND) is 33us.
3. For single device, connect NEXT_O to NEXT_IN.
4. Tie all nFAULT_x pins of all chained devices together. When fault is detected in any device, the device pulls the nFAULT line low, triggering sequential power down starting with the end device. This is released by EN low until FAULT is cleared.
5. ALL_PG is a push-pull output for the logical AND of all PG_ signals.

Application Schematic for Chained Nested Sequencer

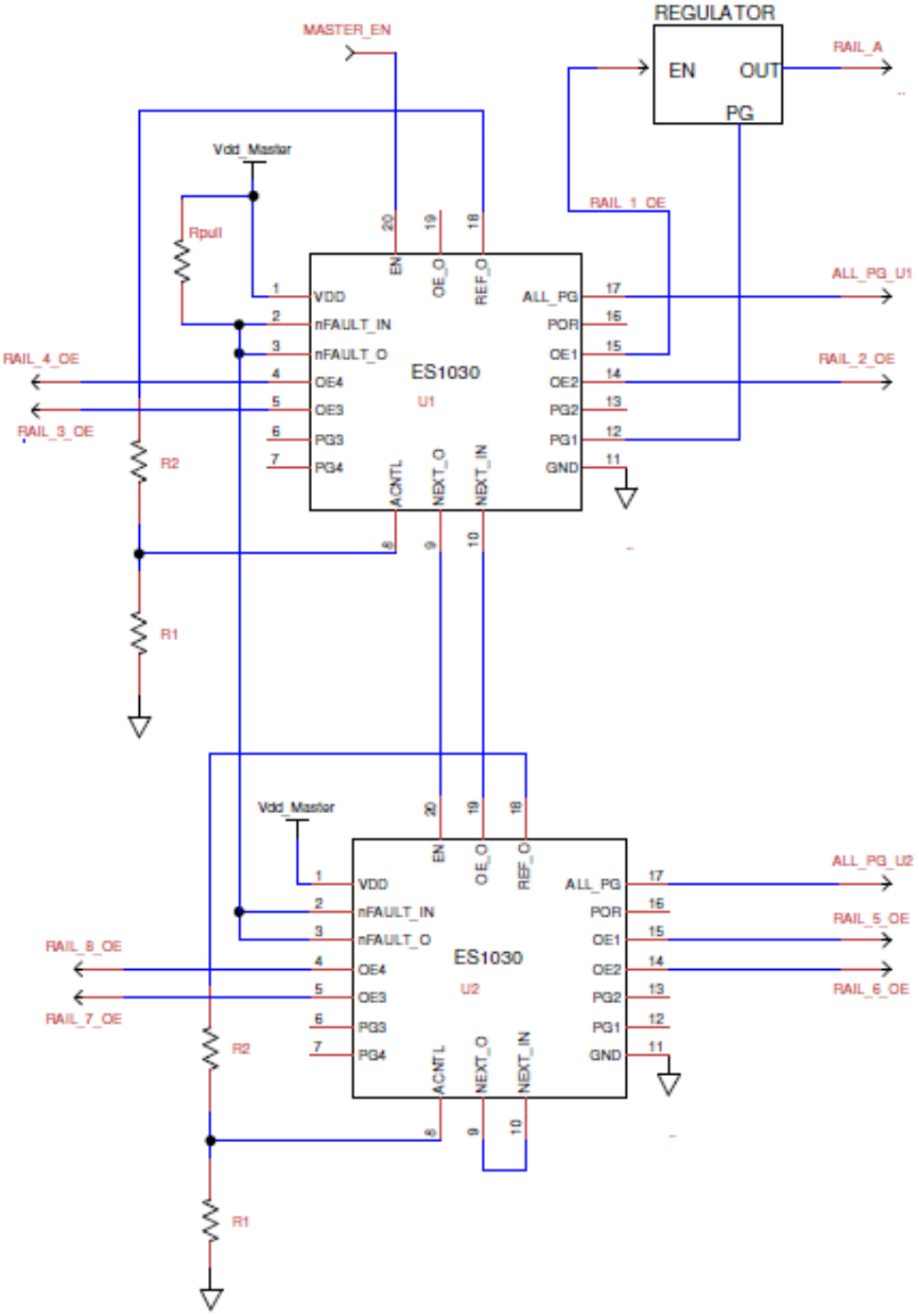


Figure 3: Chained Operation

Notes to **Figure 3**:

1. Connect NEXT_O to NEXT_IN on device at end of chain.
2. Tie all nFAULT_x pins of all chained devices together. When fault is detected in any device, the device pulls the nFAULT line low, triggering sequential power down starting with the end device. This is released by EN low until FAULT is cleared.
3. Tie NEXT_O to EN of following device. Tie NEXT_IN to OE_O of following device.

Bill of Materials

LEVEL	ITEM NUMBER/ MANUFACTUER NAME	ITEM REVISION/ ITEM DESCRIPTION/ MANUFACTUER PART NUMBER	MANUFACTUER PART DESCRIPTION	QUANTITY/ MANUFACTUER PART LIFECYCLE PHASE	REFERENCE DESCRIPTION/ REFERENCE NOTES	ITEM TYPE
0.1	10696	Schematic, ES1030 Evaluation Board		1		Document
0.1	10697	PCB, ES1030 Evaluation Board		11		PCB
0.1	2495/ Panasonic	RESISTOR ZERO OHM 1/10W 5% 0402 SMD/ ERJ-2GE0R00x	RESISTOR ZERO OHM 1/10W 5% 0402 SMD	14/Active	R1, R11, R13, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R31	Resistor
0.1	6237/ Taiyo Yuden	CAP CER 1.0UF 16V X5R 10% 0402/ EMK105BJ105KV-F	CAP CER 1.0UF 16V X5R 10% 0402	1/Active	C1	Capacitor
0.1	Panasonic	RES 100K OHM 1/16W 1% 0402 SMD/ ERJ-2GEJ103X	RES 100K OHM 1/16W 1% 0402 SMD	3/Active	R7, R14, R40	Resistor
0.1	Altera	ES1030 Power Rail Sequencer TQFN-20	ES1030 Power Rail Sequencer TQFN-20	1/Active	U1	Device
0.1	05118/ SAMTEC	CONN HEADER 3POS .100" SNGL TIN/ TSW-103-07-T-S	CONN HEADER 3POS .100" SNGL TIN	13/Active	SV1, SV5, SV7, SV10, SV11, SV12, SV13, SV14, SV15, SV16, SV17, SV18, SV22	Connector/ Contact
0.1	SAMTEC	CONN HEADER 10POS .100" SNGL TIN	CONN HEADER 10POS .100" SNGL TIN	2	SV8, SV9	Connector/ Contact
0.1		JUMPER, 0.100”		14		Connector/ Contact

Test Recommendations

To guarantee measurement accuracy, the following precautions should be observed:

1. You should use a low-loop-inductance scope probe tip, similar to the probe tip illustrated in Figure 4, to measure signals.

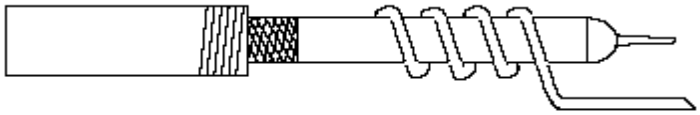


Figure 4: Low-Loop-Inductance Scope Probe Tip

2. Logic signal rise and fall times should be much less than 1us and be monotonic.

Document Revision History

DATE	DOCUMENT VERSION	CHANGES
April 2015	2.0	Text of Instruction 3, Page 2 and Note 2, Page 5, Figures 2-3.
February 2015	1.0	Initial release.

Contact Information

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
Phone: 408-544-7000
www.altera.com

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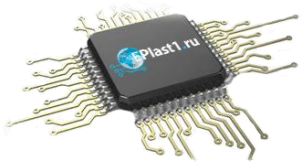

Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.