

R1RP0416D Series

4M High Speed SRAM (256-kword × 16-bit)

REJ03C0108-0100Z

Rev. 1.00

Mar.12.2004

Description

The R1RP0416D Series is a 4-Mbit high speed static RAM organized 256-k word × 16-bit. It has realized high speed access time by employing CMOS process (6-transistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in 400-mil 44-pin plastic SOJ and 400-mil 44-pin plastic TSOPII.

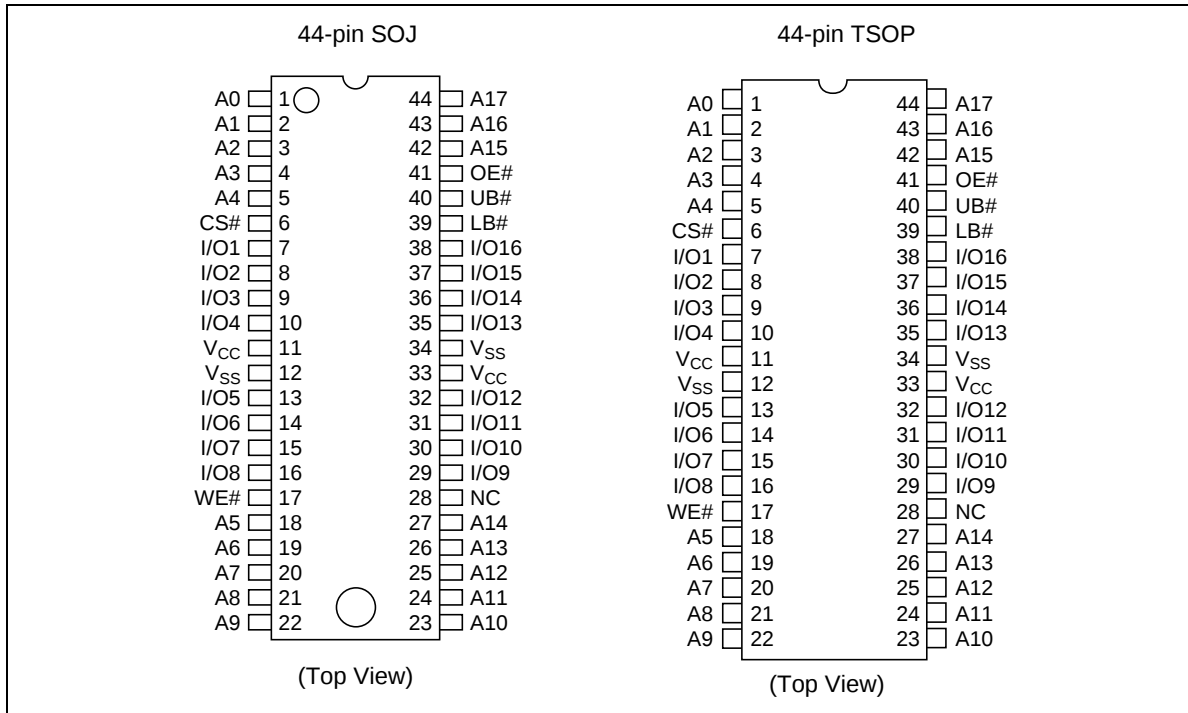
Features

- Single 5.0 V supply: 5.0 V ± 10%
- Access time: 12 ns (max)
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
 - All inputs and outputs
- Operating current: 160 mA (max)
- TTL standby current: 40 mA (max)
- CMOS standby current: 5 mA (max)
 - : 1.0 mA (max) (L-version)
- Data retention current: 0.5 mA (max) (L-version)
- Data retention voltage: 2 V (min) (L-version)
- Center V_{CC} and V_{SS} type pin out

Ordering Information

Type No.	Access time	Package
R1RP0416DGE-2PR	12 ns	400-mil 44-pin plastic SOJ (44P0K)
R1RP0416DGE-2LR	12 ns	
R1RP0416DSB-2PR	12 ns	400-mil 44-pin plastic TSOPII (44P3W-H)
R1RP0416DSB-2LR	12 ns	

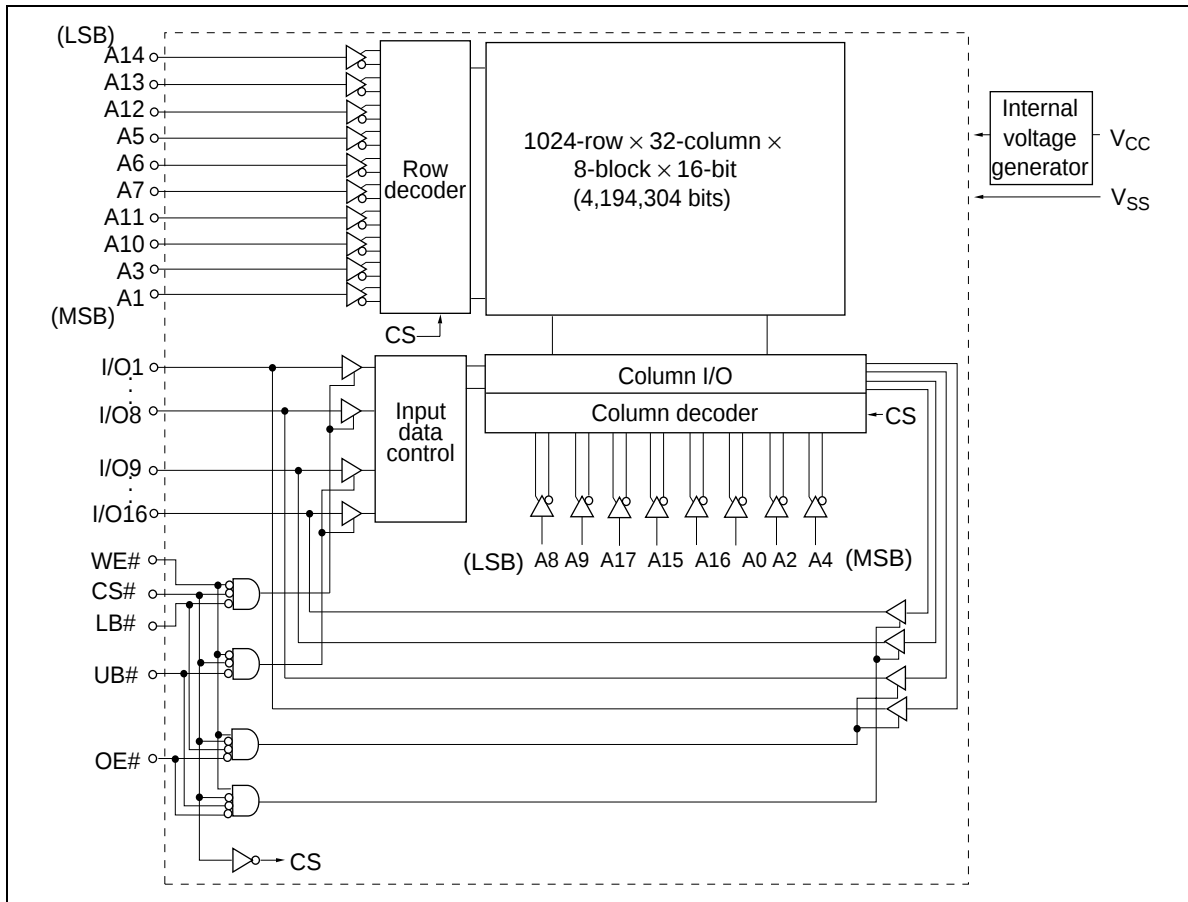
Pin Arrangement



Pin Description

Pin name	Function
A0 to A17	Address input
I/O1 to I/O16	Data input/output
CS#	Chip select
OE#	Output enable
WE#	Write enable
UB#	Upper byte select
LB#	Lower byte select
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

Block Diagram



Operation Table

CS#	OE#	WE#	LB#	UB#	Mode	V _{CC} current	I/O1–I/O8	I/O9–I/O16	Ref. cycle
H	×	×	×	×	Standby	I _{SB} ¹ I _{SB1}	High-Z	High-Z	—
L	H	H	×	×	Output disable	I _{CC}	High-Z	High-Z	—
L	L	H	L	L	Read	I _{CC}	Output	Output	Read cycle
L	L	H	L	H	Lower byte read	I _{CC}	Output	High-Z	Read cycle
L	L	H	H	L	Upper byte read	I _{CC}	High-Z	Output	Read cycle
L	L	H	H	H	—	I _{CC}	High-Z	High-Z	—
L	×	L	L	L	Write	I _{CC}	Input	Input	Write cycle
L	×	L	L	H	Lower byte write	I _{CC}	Input	High-Z	Write cycle
L	×	L	H	L	Upper byte write	I _{CC}	High-Z	Input	Write cycle
L	×	L	H	H	—	I _{CC}	High-Z	High-Z	—

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V _{SS}	V _{CC}	–0.5 to +7.0	V
Voltage on any pin relative to V _{SS}	V _T	–0.5* ¹ to V _{CC} + 0.5* ²	V
Power dissipation	P _T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Notes: 1. V_T (min) = –2.0 V for pulse width (under shoot) ≤ 6 ns.

2. V_T (max) = V_{CC} + 2.0 V for pulse width (over shoot) ≤ 6 ns.

Recommended DC Operating Conditions

(Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC} * ³	4.5	5.0	5.5	V
	V _{SS} * ⁴	0	0	0	V
Input voltage	V _{IH}	2.2	—	V _{CC} + 0.5* ²	V
	V _{IL}	–0.5* ¹	—	0.8	V

Notes: 1. V_{IL} (min) = –2.0 V for pulse width (under shoot) ≤ 6 ns.

2. V_{IH} (max) = V_{CC} + 2.0 V for pulse width (over shoot) ≤ 6 ns.

3. The supply voltage with all V_{CC} pins must be on the same level.

4. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit	Test conditions
Input leakage current	I _{LI}	—	2	μA	V _{IN} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	—	2	μA	V _{IN} = V _{SS} to V _{CC}
Operation power supply current	I _{CC}	—	160	mA	Min cycle CS# = V _{IL} , I _{OUT} = 0 mA Other inputs = V _{IH} /V _{IL}
Standby power supply current	I _{SB}	—	40	mA	Min cycle, CS# = V _{IH} , Other inputs = V _{IH} /V _{IL}
	I _{SB1}	—	5	mA	f = 0 MHz V _{CC} ≥ CS# ≥ V _{CC} - 0.2 V, (1) 0 V ≤ V _{IN} ≤ 0.2 V or (2) V _{CC} ≥ V _{IN} ≥ V _{CC} - 0.2 V
		—* ¹	1.0* ¹		
Output voltage	V _{OL}	—	0.4	V	I _{OL} = 8 mA
	V _{OH}	2.4	—	V	I _{OH} = -4 mA

Note: 1. This characteristics is guaranteed only for L-version.

Capacitance

(Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Max	Unit	Test conditions
Input capacitance* ¹	C _{IN}	—	6	pF	V _{IN} = 0 V
Input/output capacitance* ¹	C _{I/O}	—	8	pF	V _{I/O} = 0 V

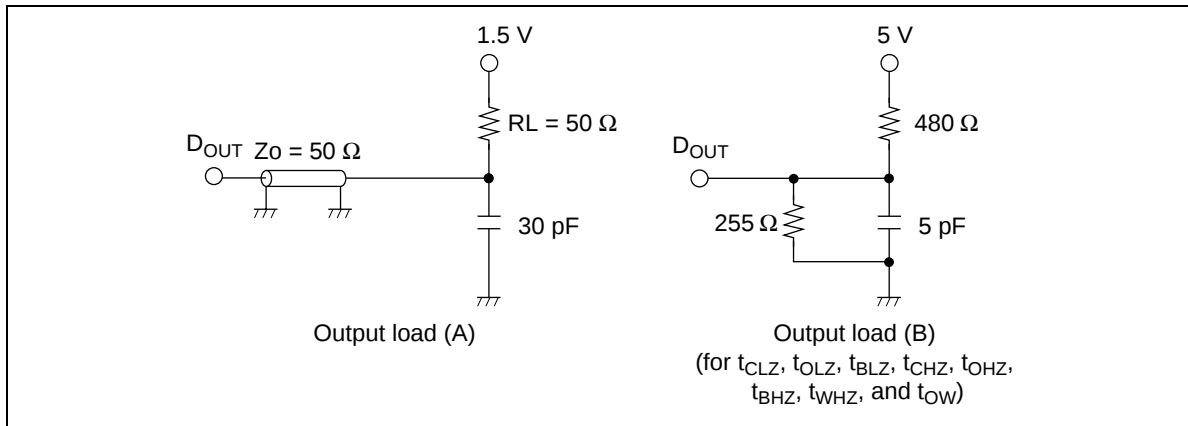
Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



Read Cycle

		R1RP0416D			
		-2			
Parameter	Symbol	Min	Max	Unit	Notes
Read cycle time	t _{RC}	12	—	ns	
Address access time	t _{AA}	—	12	ns	
Chip select access time	t _{ACS}	—	12	ns	
Output enable to output valid	t _{OE}	—	6	ns	
Byte select to output valid	t _{BA}	—	6	ns	
Output hold from address change	t _{OH}	3	—	ns	
Chip select to output in low-Z	t _{CLZ}	3	—	ns	1
Output enable to output in low-Z	t _{OLZ}	0	—	ns	1
Byte select to output in low-Z	t _{BLZ}	0	—	ns	1
Chip deselect to output in high-Z	t _{CHZ}	—	6	ns	1
Output disable to output in high-Z	t _{OHZ}	—	6	ns	1
Byte deselect to output in high-Z	t _{BHZ}	—	6	ns	1

R1RP0416D Series

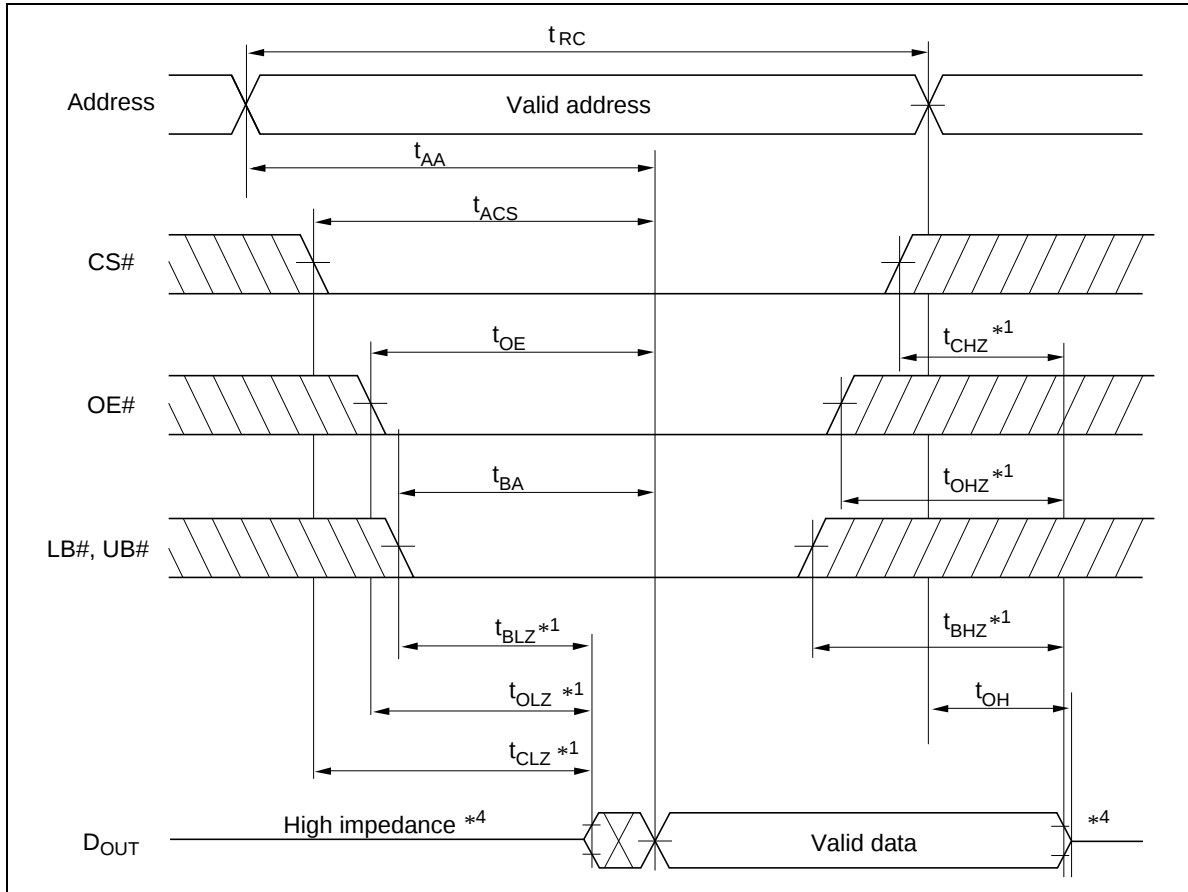
Write Cycle

		R1RP0416D			
		-2			
Parameter	Symbol	Min	Max	Unit	Notes
Write cycle time	t _{WC}	12	—	ns	
Address valid to end of write	t _{AW}	8	—	ns	
Chip select to end of write	t _{CW}	8	—	ns	8
Write pulse width	t _{WP}	8	—	ns	7
Byte select to end of write	t _{BW}	8	—	ns	
Address setup time	t _{AS}	0	—	ns	5
Write recovery time	t _{WR}	0	—	ns	6
Data to write time overlap	t _{DW}	6	—	ns	
Data hold from write time	t _{DH}	0	—	ns	
Write disable to output in low-Z	t _{OW}	3	—	ns	1
Output disable to output in high-Z	t _{OHZ}	—	6	ns	1
Write enable to output in high-Z	t _{WHZ}	—	6	ns	1

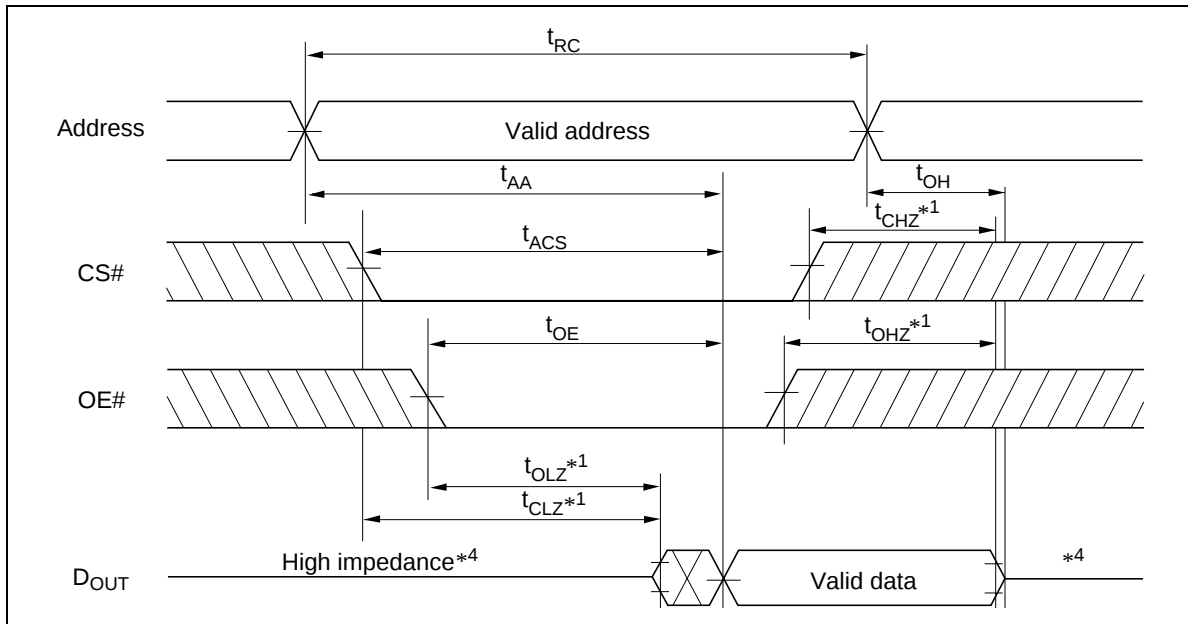
- Notes:
1. Transition is measured ± 200 mV from steady voltage with output load (B). This parameter is sampled and not 100% tested.
 2. If the CS# or LB# or UB# low transition occurs simultaneously with the WE# low transition or after the WE# transition, output remains a high impedance state.
 3. WE# and/or CS# must be high during address transition time.
 4. If CS#, OE#, LB# and UB# are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
 5. t_{AS} is measured from the latest address transition to the latest of CS#, WE#, LB# or UB# going low.
 6. t_{WR} is measured from the earliest of CS#, WE#, LB# or UB# going high to the first address transition.
 7. A write occurs during the overlap of a low CS#, a low WE# and a low LB# or a low UB# (t_{WP}). A write begins at the latest transition among CS# going low, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS# going high, WE# going high and LB# going high or UB# going high.
 8. t_{CW} is measured from the later of CS# going low to the end of write.

Timing Waveforms

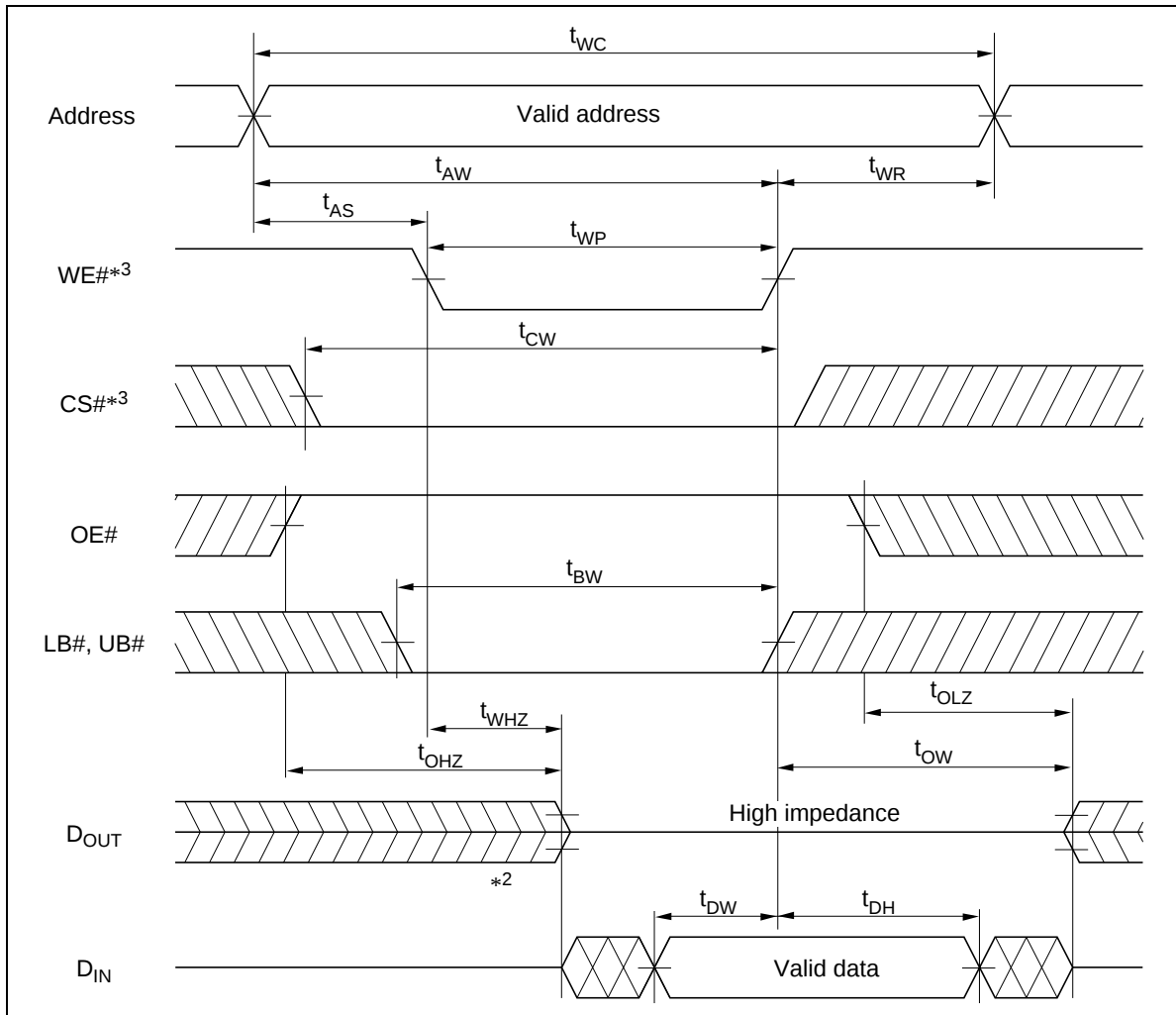
Read Timing Waveform (1) ($WE\# = V_{IH}$)



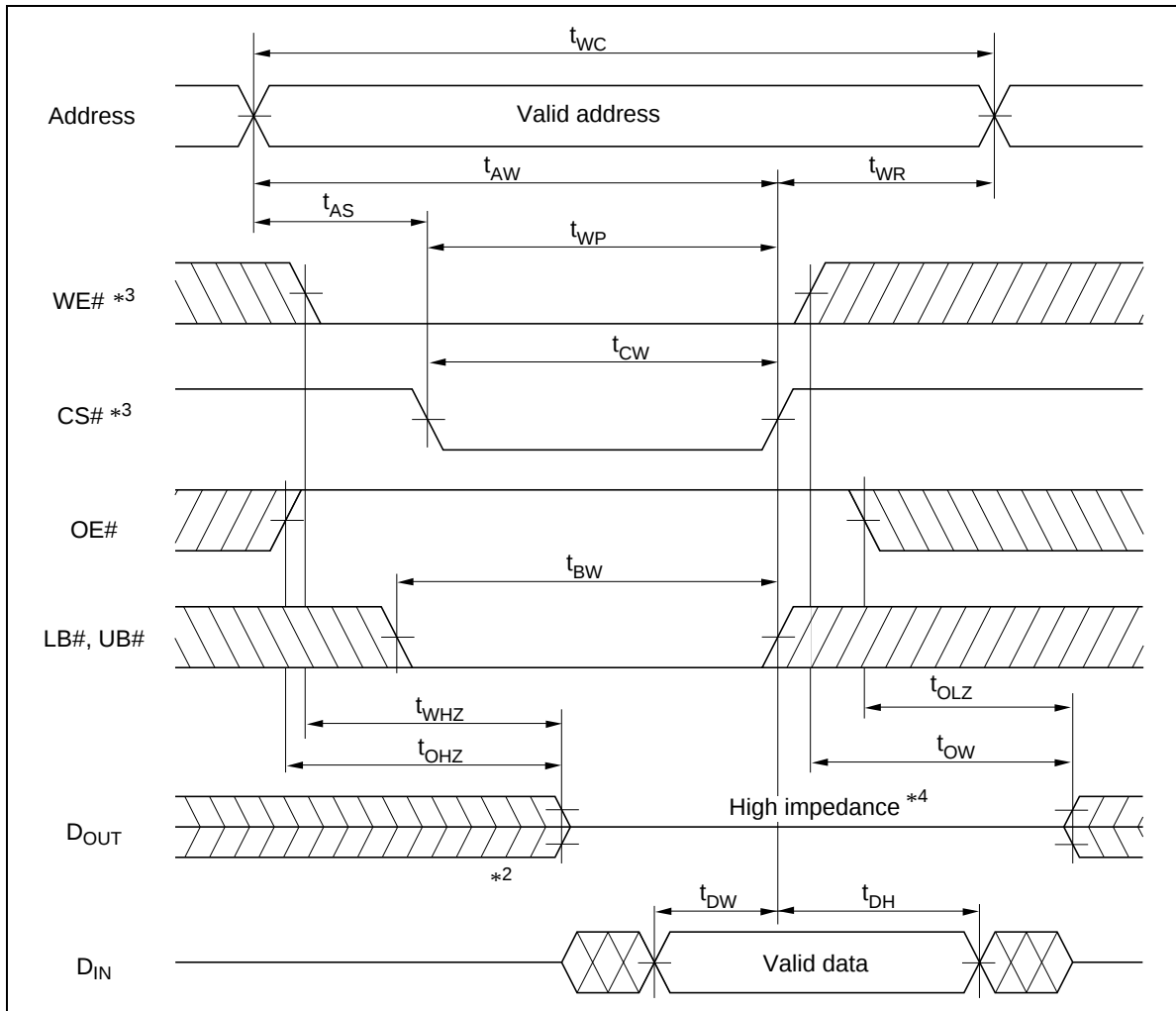
Read Timing Waveform (2) ($WE\# = V_{IH}$, $LB\# = V_{IL}$, $UB\# = V_{IL}$)



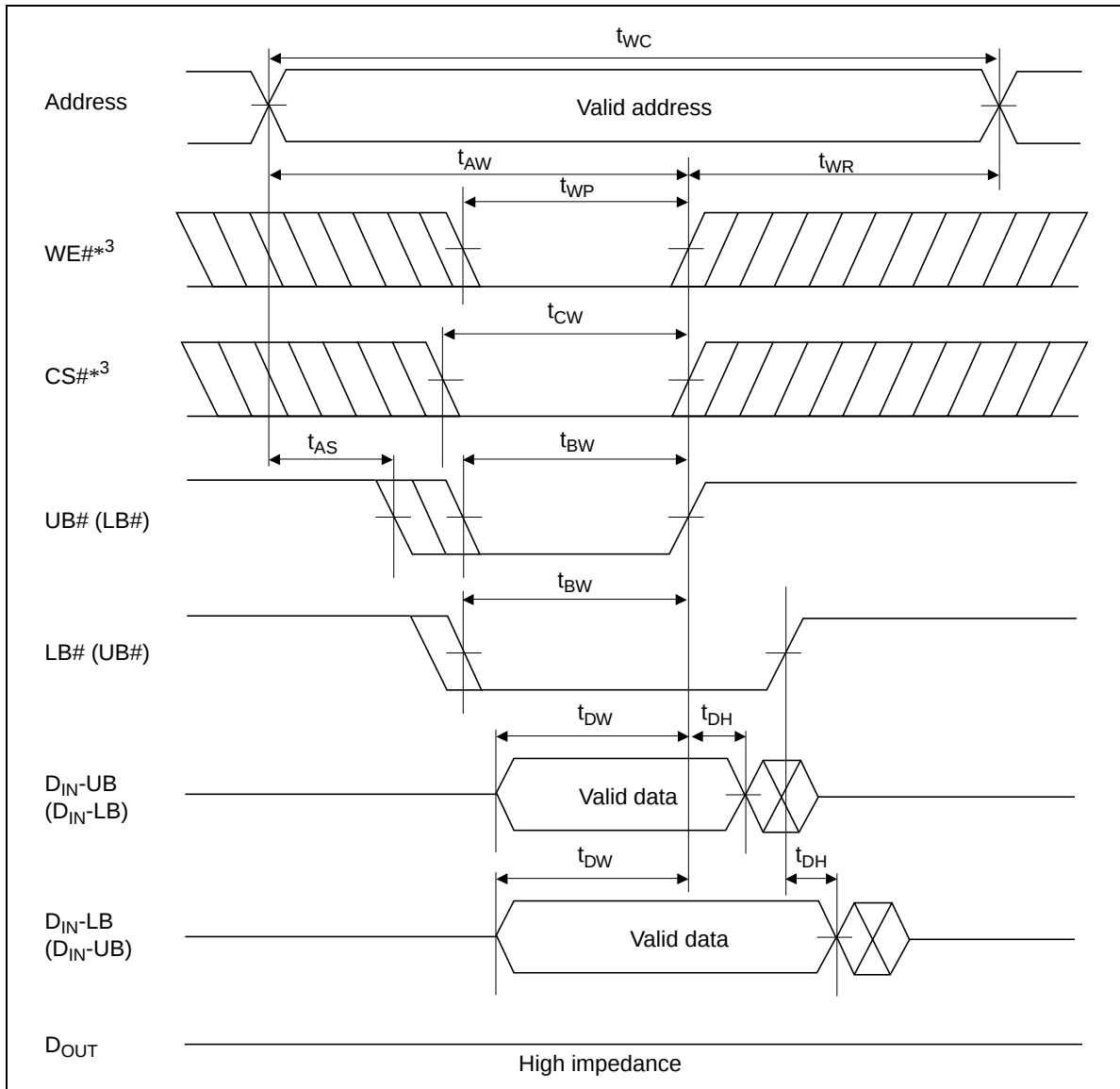
Write Timing Waveform (1) (WE# Controlled)



Write Timing Waveform (2) (CS# Controlled)



Write Timing Waveform (3) (LB#, UB# Controlled, OE# = V_{ih})



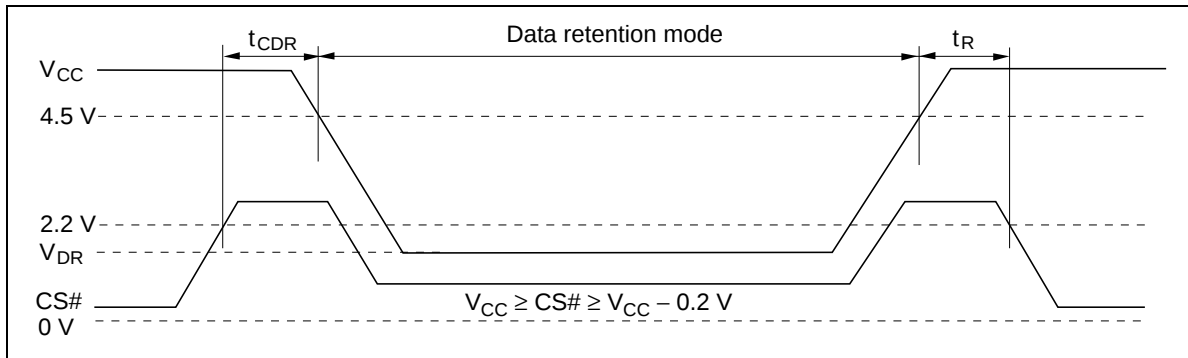
Low V_{CC} Data Retention Characteristics

($T_a = 0$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	V	$V_{CC} \geq CS\# \geq V_{CC} - 0.2\text{ V}$, (1) $0\text{ V} \leq V_{IN} \leq 0.2\text{ V}$ or (2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2\text{ V}$
Data retention current	I_{CCDR}	—	500	μA	$V_{CC} = 3\text{ V}$ $V_{CC} \geq CS\# \geq V_{CC} - 0.2\text{ V}$, (1) $0\text{ V} \leq V_{IN} \leq 0.2\text{ V}$ or (2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2\text{ V}$
Chip deselect to data retention time	t_{CDR}	0	—	ns	See retention waveform
Operation recovery time	t_R	5	—	ms	

Low V_{CC} Data Retention Timing Waveform



Revision History

R1RP0416D Series Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
0.01	Sep. 30, 2003	—	Initial issue
1.00	Mar.12.2004	—	Deletion of Preliminary

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH

Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.

7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.

FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.