



STN4NF06L

N-channel 60 V, 0.07 Ω , 4 A SOT-223
STripFET™ II Power MOSFET

Features

Order code	V _{DSS}	R _{DS(on)} max	I _D
STN4NF06L	60 V	< 0.1 Ω	4 A

- Exceptional dv/dt capability
- Avalanche rugged technology
- 100% avalanche tested
- Low threshold drive

Applications

- Switching application
 - Automotive

Description

This device is a N-channel STripFET™ II Power MOSFET that is the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

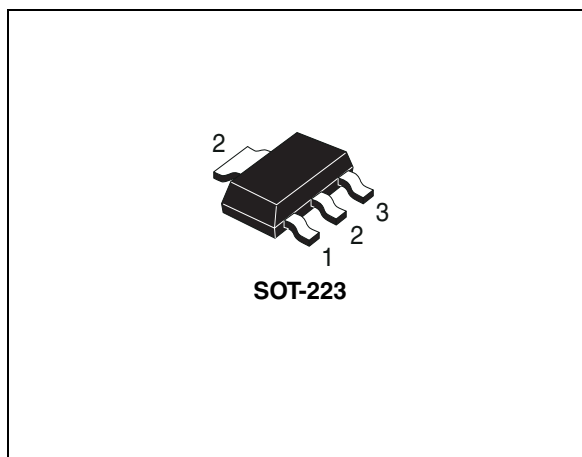


Figure 1. Internal schematic diagram

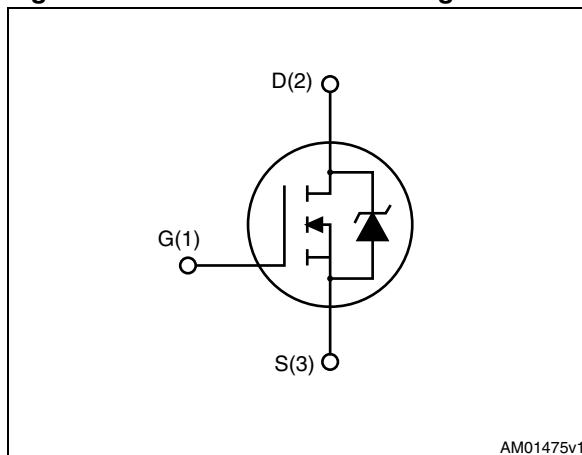


Table 1. Device summary

Order code	Marking	Package	Packaging
STN4NF06L	4NF06L	SOT-223	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60	V
V_{GS}	Gate-source voltage	± 16	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	4	A
I_D	Drain current (continuous) at $T_C=100\text{ }^\circ\text{C}$	2.9	A
$I_{DM}^{(2)}$	Drain current (pulsed)	16	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	3.3	W
	Derating factor	0.026	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	10	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	200	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Current limited by the package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 3\text{ A}$, $di/dt \leq 150\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$.
4. Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = 4\text{ A}$, $V_{DD} = 30\text{ V}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-PCB max.	38	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(2)}$	Thermal resistance junction-PCB max.	100	$^\circ\text{C}/\text{W}$
$T_1^{(3)}$	Maximum lead temperature for soldering purpose typ.	260	$^\circ\text{C}$

1. When Mounted on FR-4 board with 1 inch² pad, 2 oz. of Cu. and $t < 10\text{ sec}$.
2. When mounted on minimum recommended footprint.
3. For 10 sec. 1.6 mm from case.

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	60			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating @ } 125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 16\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1		2.8	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 1.5\text{ A}$ $V_{GS} = 5\text{ V}$, $I_D = 1.5\text{ A}$		0.07 0.085	0.10 0.12	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 1.5\text{ A}$	-	3		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	340		pF
C_{oss}	Output capacitance			63		pF
C_{rss}	Reverse transfer capacitance			30		pF
Q_g	Total gate charge	$V_{DD} = 48\text{ V}$, $I_D = 3\text{ A}$	-	7	9	nC
Q_{gs}	Gate-source charge	$V_{GS} = 5\text{ V}$		1.5		nC
Q_{gd}	Gate-drain charge	(see Figure 15)		2.8		nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time rise time	$V_{DD} = 30\text{ V}$, $I_D = 1.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 5\text{ V}$ (see Figure 14)	-	9	-	ns
t_r				25		
$t_{d(off)}$	Turn-off delay time fall time	$V_{DD} = 30\text{ V}$, $I_D = 1.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 5\text{ V}$ (see Figure 14)	-	20	-	ns
t_f				10		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=4\text{ A}$, $V_{GS}=0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD}=4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=25\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ <i>(see Figure 16)</i>	-	50		ns
Q_{rr}	Reverse recovery charge			88		nC
I_{RRM}	Reverse recovery current			3.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration= 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

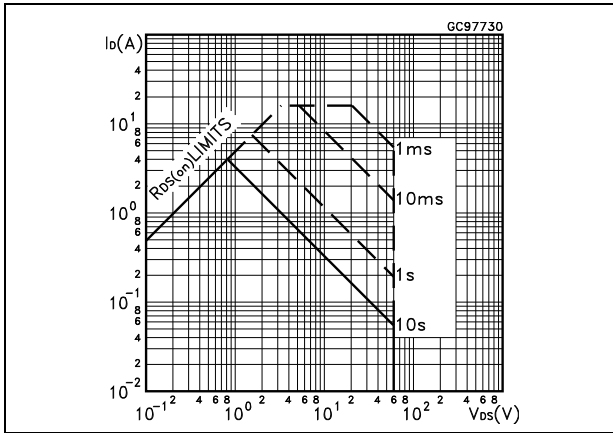


Figure 3. Thermal impedance

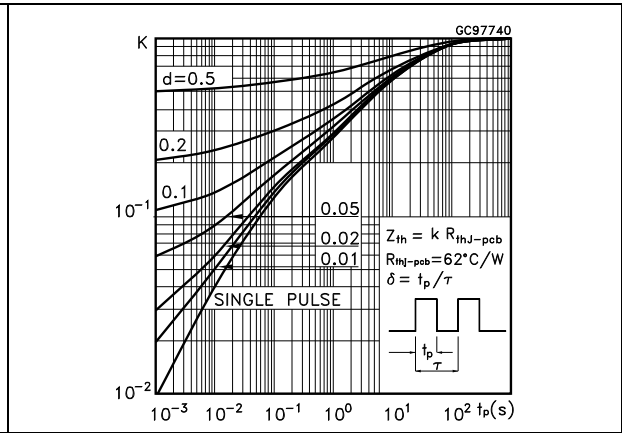


Figure 4. Output characteristics

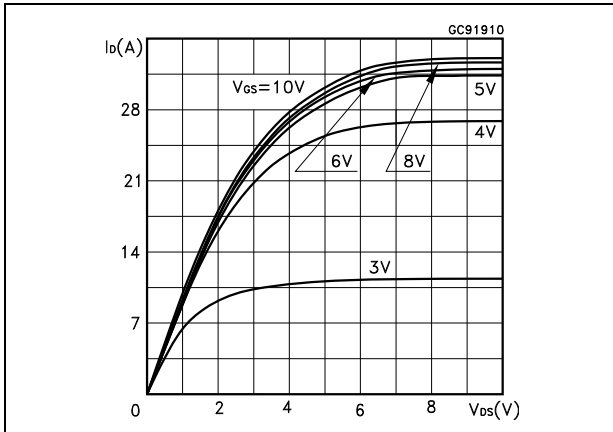


Figure 5. Transfer characteristics

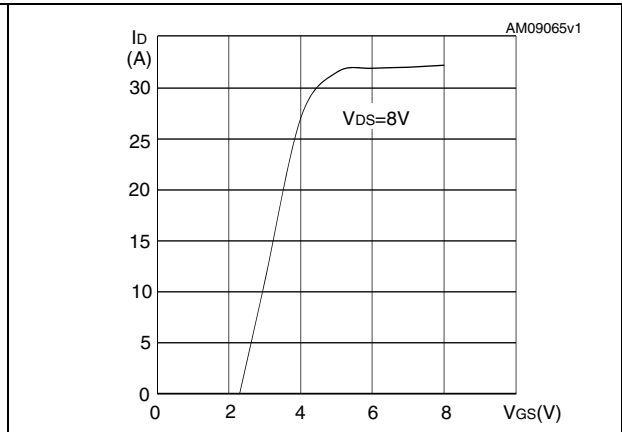


Figure 6. Transconductance

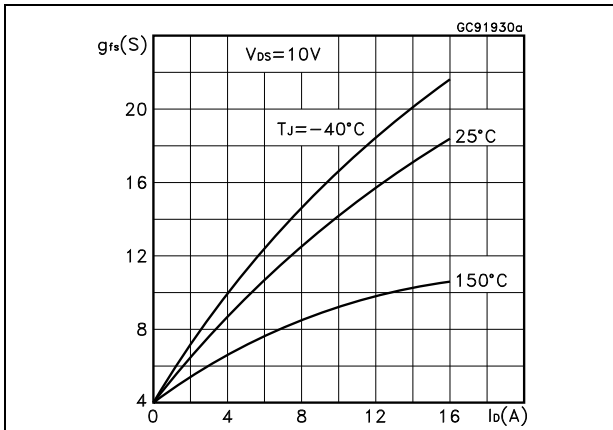


Figure 7. Static drain-source on resistance

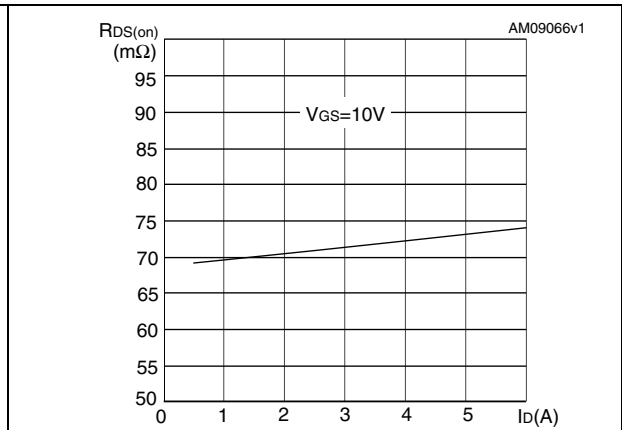


Figure 8. Gate charge vs. gate-source voltage Figure 9. Capacitance variations

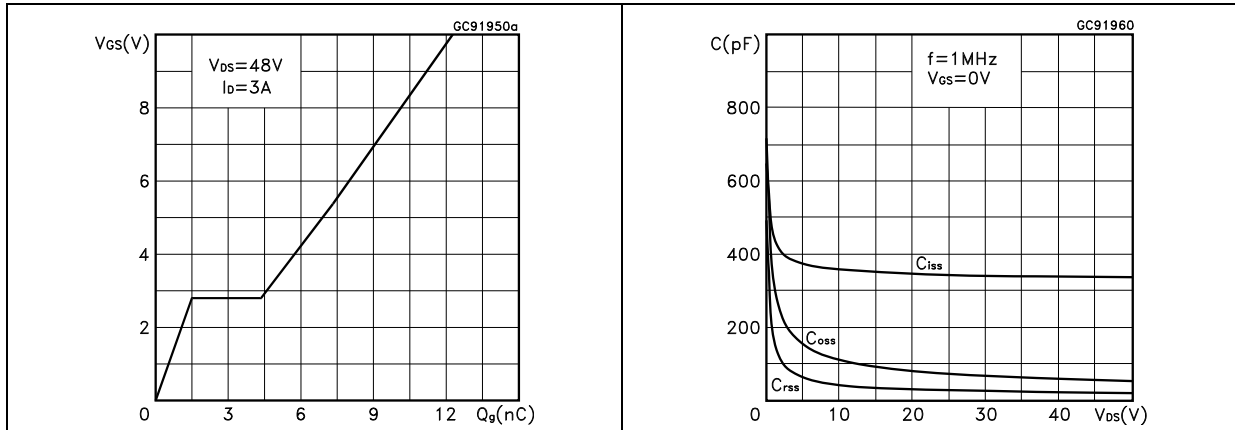


Figure 10. Normalized gate threshold voltage vs. temperature

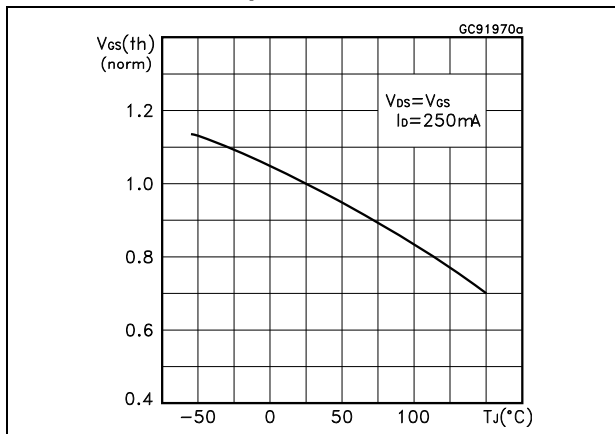


Figure 11. Normalized on resistance vs. temperature

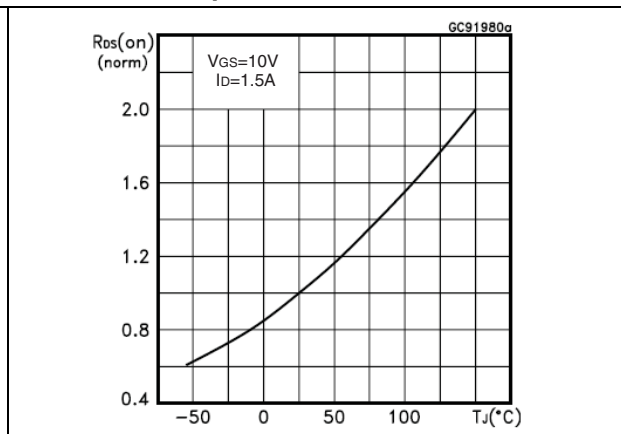


Figure 12. Source-drain diode forward characteristics

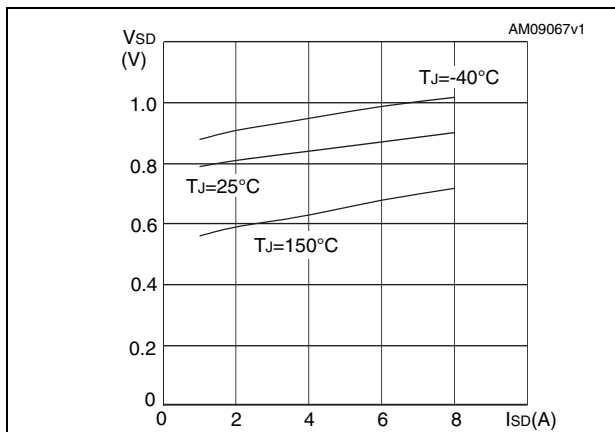
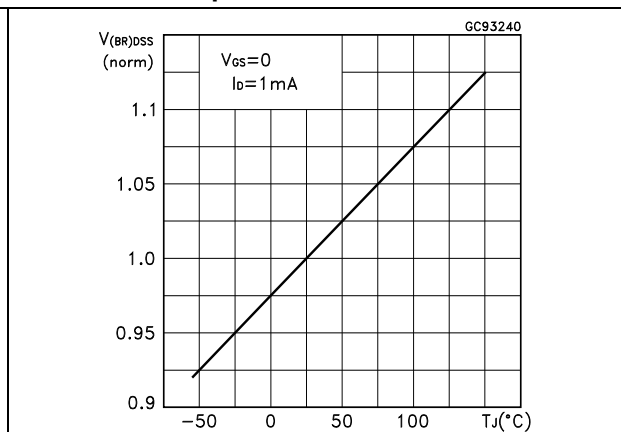


Figure 13. Normalized breakdown voltage vs. temperature



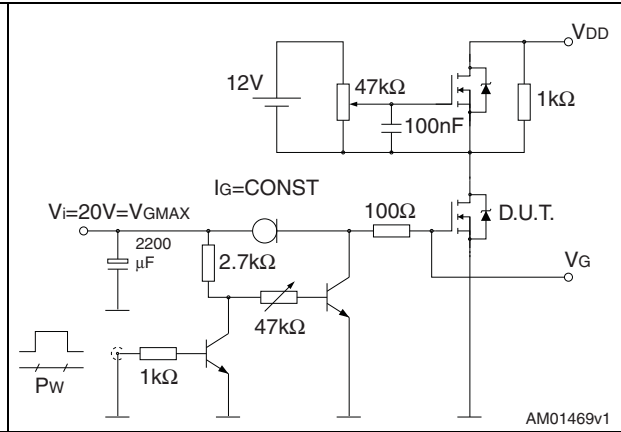
3 Test circuit

Figure 14. Switching times test circuit for resistive load



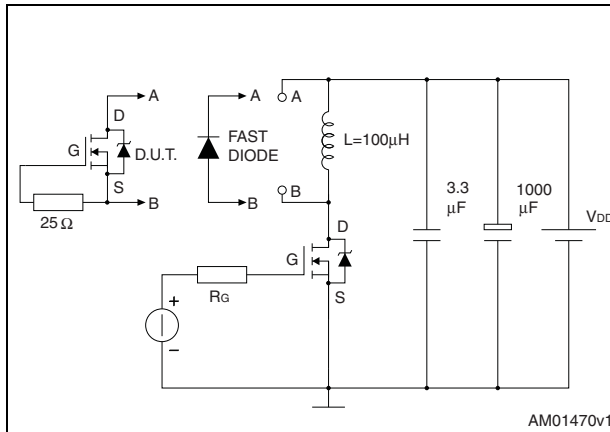
AM01468v1

Figure 15. Gate charge test circuit



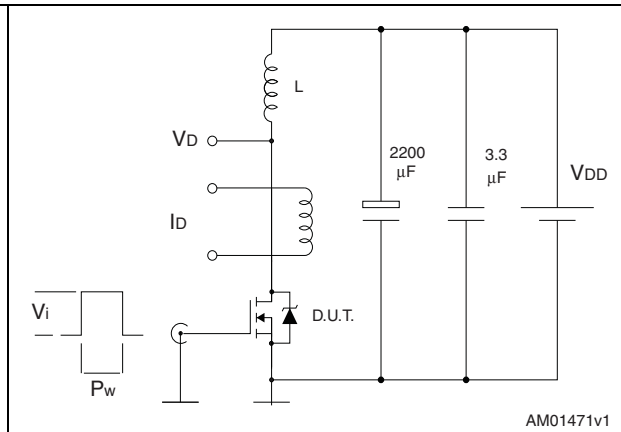
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Figure 16. Test circuit for inductive load switching and diode recovery times



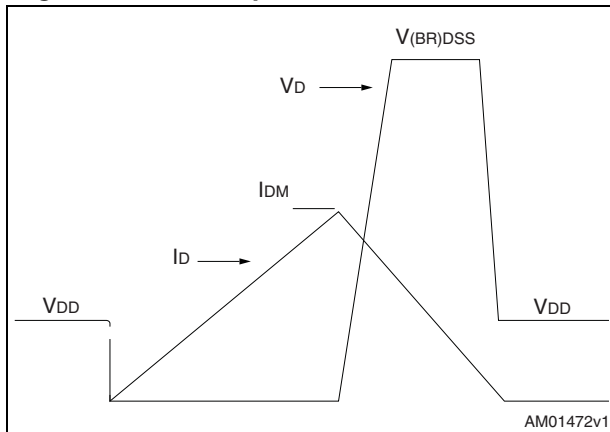
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Figure 17. Unclamped Inductive load test circuit



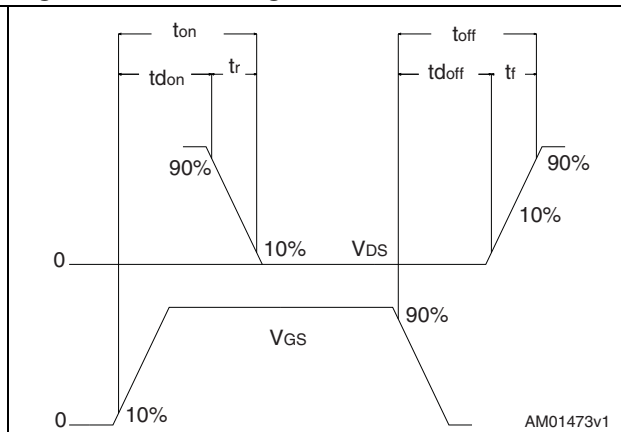
AM01471v1

Figure 18. Unclamped inductive waveform



AM01472v1

Figure 19. Switching time waveform



AM01473v1

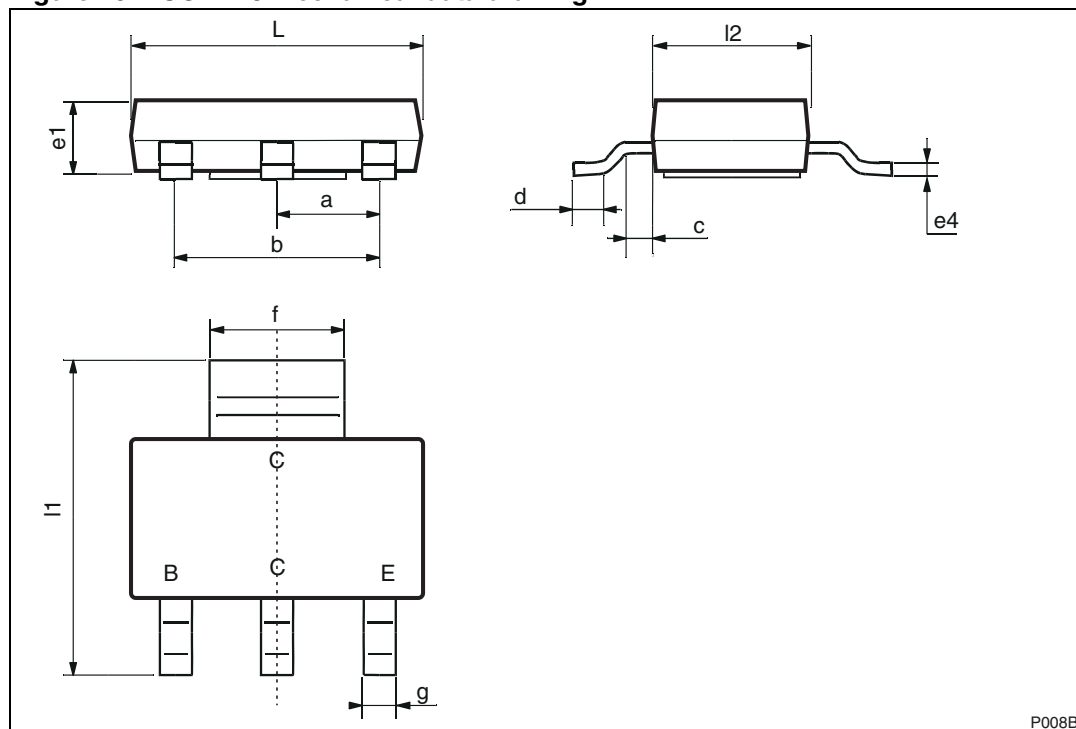
4 Package mechanical data

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Table 8. SOT-223 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
a	2.27	2.3	2.33
b	4.57	4.6	4.63
c	0.2	0.4	0.6
d	0.63	0.65	0.67
e1	1.5	1.6	1.7
e4			0.32
f	2.9	3	3.1
g	0.67	0.7	0.73
l1	6.7	7	7.3
l2	3.5	3.5	3.7
L	6.3	6.5	6.7

Figure 20. SOT-223 mechanical data drawing



P008B

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
22-Apr-2008	1	Initial version.
29-Apr-2011	2	<i>Figure 5, Figure 7, Figure 11 and Figure 12</i> have been updated.

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