



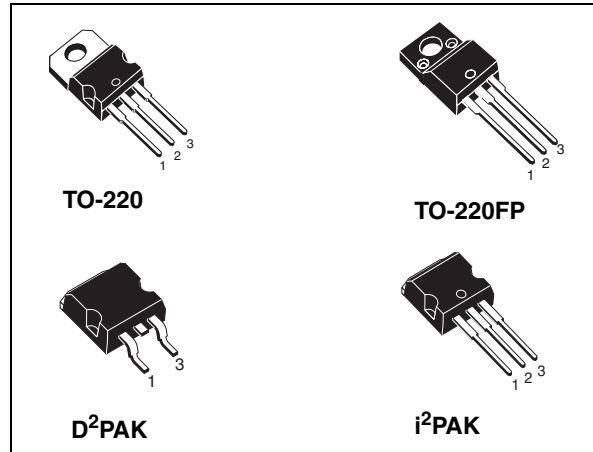
STP11NM60 - STP11NM60FP STB11NM60 - STB11NM60-1

N-channel 650V @ T_{Jmax} - 0.4Ω - 11A TO-220/FP/D²PAK/I²PAK
MDmesh™ Power MOSFET

General features

Type	V_{DSS} (@ $T_J = T_{Jmax}$)	$R_{DS(on)}$	I_D
STP11NM60	650V	$<0.45\Omega$	11A
STP11NM60FP	650V	$<0.45\Omega$	11A
STB11NM60	650V	$<0.45\Omega$	11A
STB11NM60-1	650V	$<0.45\Omega$	11A

- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



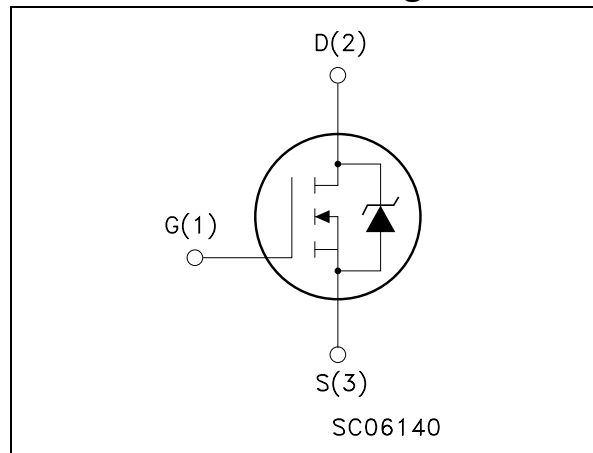
Description

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB11NM60T4	B11NM60	D ² PAK	Tape & reel
STB11NM60-1	B11NM60-1	I ² PAK	Tube
STP11NM60	P11NM60	TO-220	Tube
STP11NM60FP	P11NM60FP	TO-220FP	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/D ² PAK/I ² PAK	TO-220FP	
V _{GS}	Gate- source voltage	±30		V
I _D	Drain current (continuous) at T _C = 25°C	11	11 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C =100°C	7	7 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	44	44 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25°C	160	35	W
	Derating Factor	1.28	0.28	W/°C
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO}	Insulation withstand voltage (DC)	--	2500	V
T _J	Operating junction temperature	-65 to 150		°C
T _{stg}	Storage temperature	150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤ 11A, di/dt ≤ 400A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220/D ² PAK/I ² PAK	TO-220FP	
R _{thj-case}	Thermal resistance junction-case Max	0.78	3.57	°C/W
R _{thj-a}	Thermal resistance junction-ambient Max	62.5		°C/W
T _I	Maximum lead temperature for soldering purpose	300		°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _j Max)	5.5	A
E _{AS}	Single pulse avalanche energy (starting T _j =25°C, I _d =I _{ar} , V _{dd} =50V)	350	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250 µA, V _{GS} = 0	600			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 600 V V _{DS} = 600 V, T _C =125°C			1 10	µA µA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±30V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250µA	3	4	5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 5.5A		0.4	0.45	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 5.5A		5.2		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1000 230 25		pF pF pF
C _{oss eq} ⁽²⁾	Equivalent output capacitance	V _{GS} = 0, V _{DS} = 0V to 480V		100		pF
R _G	Gate input resistance	f = 1 MHz gate DC bias = 0 Test signal level = 20mV open drain		1.6		Ω
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 480V, I _D = 11A V _{GS} = 10V (see Figure 15)		30 10 15		nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

2. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=300\text{ V}$, $I_D=5.5\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 17)		20		ns
t_r	Rise time			20		ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD}=480\text{ V}$, $I_D=11\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 17)		6		ns
t_f	Fall time			11		ns
t_c	Cross-over time			19		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=11\text{ A}$, $V_{GS}=0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD}=11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=100\text{ V}$, $T_j=25^\circ\text{C}$ (see Figure 16)		390		ns
Q_{rr}	Reverse recovery charge			3.8		μC
I_{RRM}	Reverse recovery current			19.5		A
t_{rr}	Reverse recovery time	$I_{SD}=11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=100\text{ V}$, $T_j=150^\circ\text{C}$ (see Figure 16)		570		ns
Q_{rr}	Reverse recovery charge			5.7		μC
I_{RRM}	Reverse recovery current			20		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220/D²PAK/I²PAK

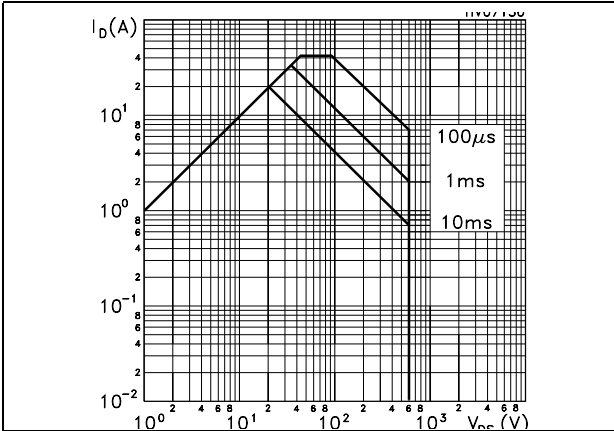


Figure 2. Thermal impedance TO-220 / D²PAK/I²PAK

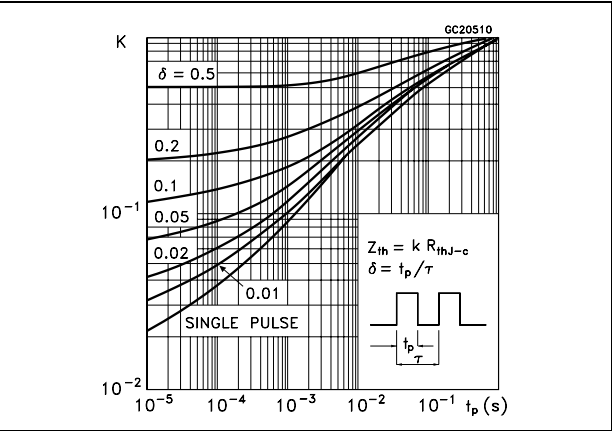


Figure 3. Safe operating area for TO-220FP

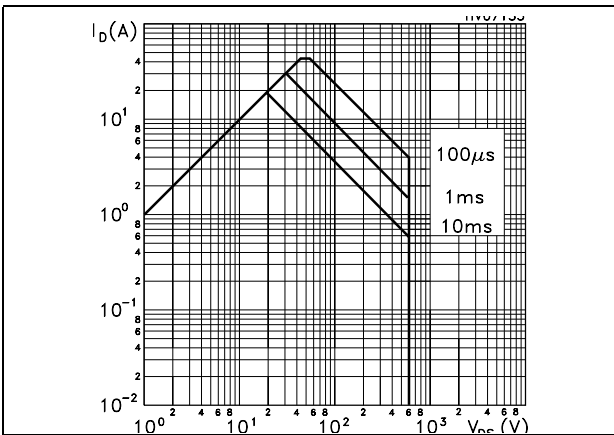


Figure 4. Thermal impedance for TO-220FP

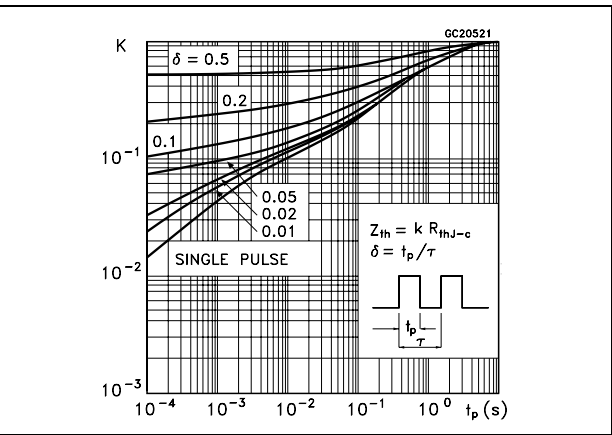


Figure 5. Output characteristics

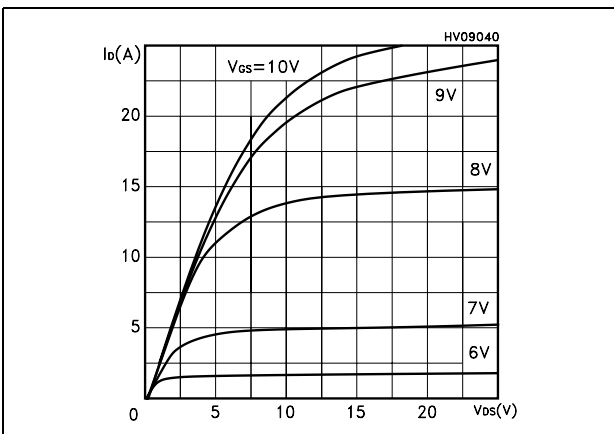


Figure 6. Transfer characteristics

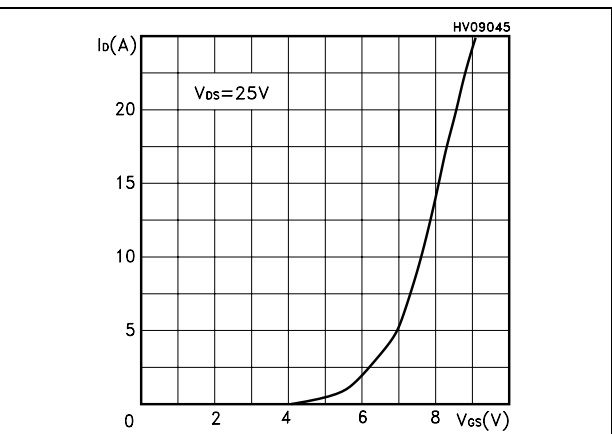


Figure 7. Transconductance

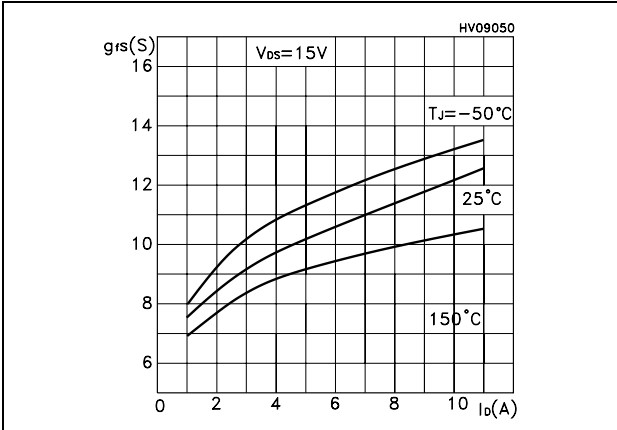


Figure 8. Static drain-source on resistance

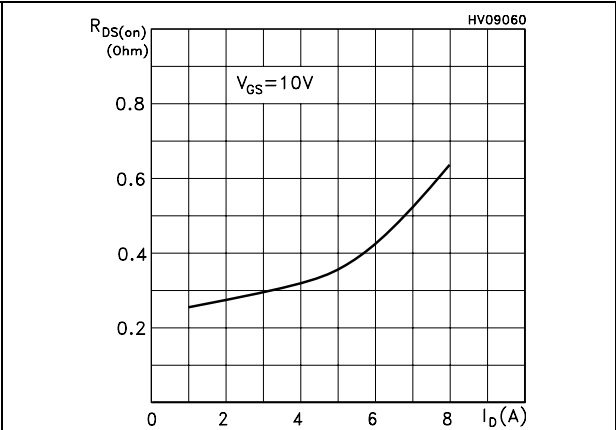


Figure 9. Gate charge vs gate-source voltage

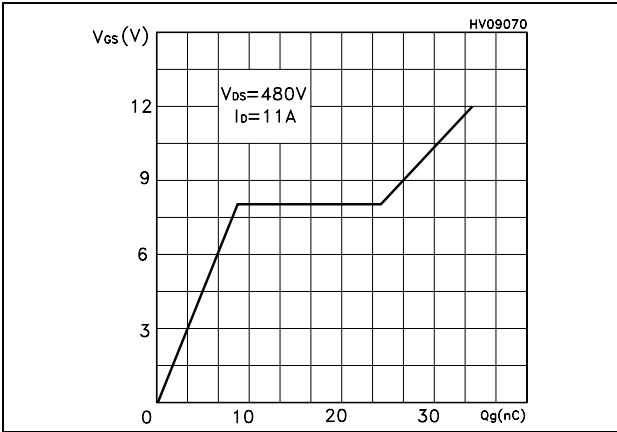


Figure 10. Capacitance variations

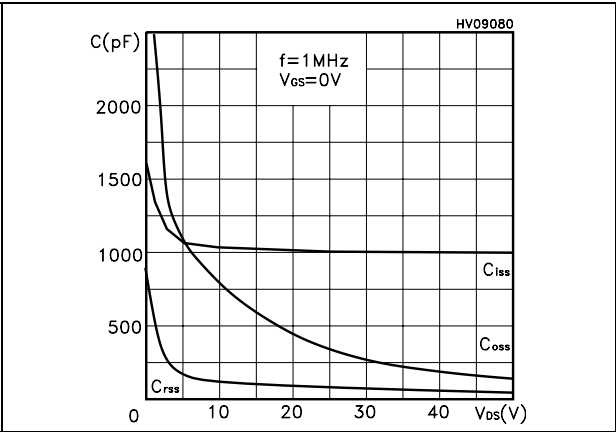


Figure 11. Normalized gate threshold voltage vs temperature

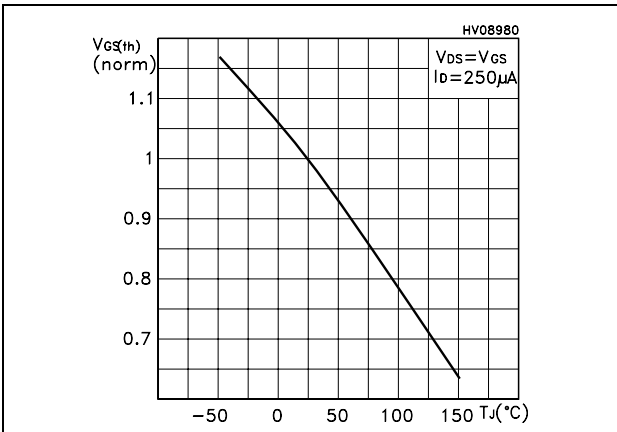


Figure 12. Normalized on resistance vs temperature

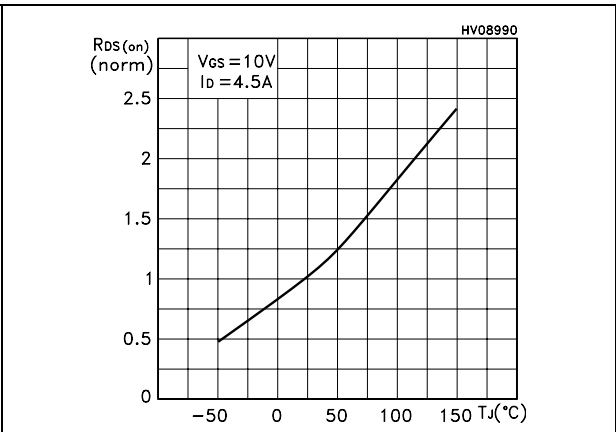
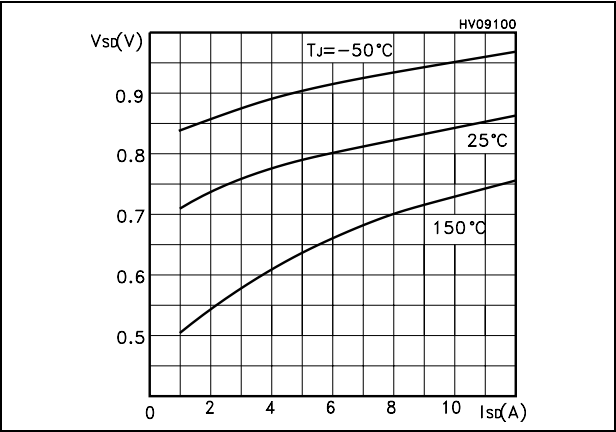


Figure 13. Source-drain diode forward characteristics



3 Test circuit

Figure 14. Switching times test circuit for resistive load

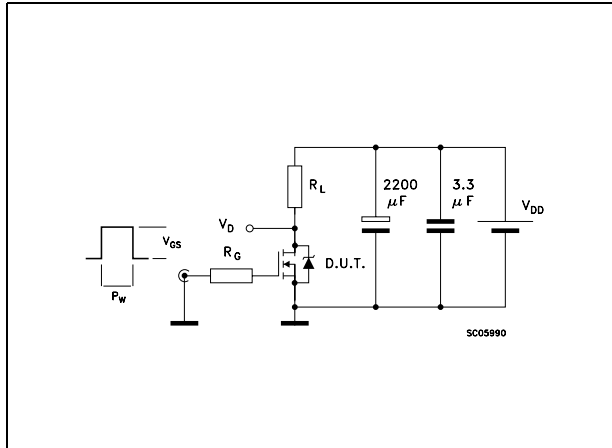


Figure 15. Gate charge test circuit

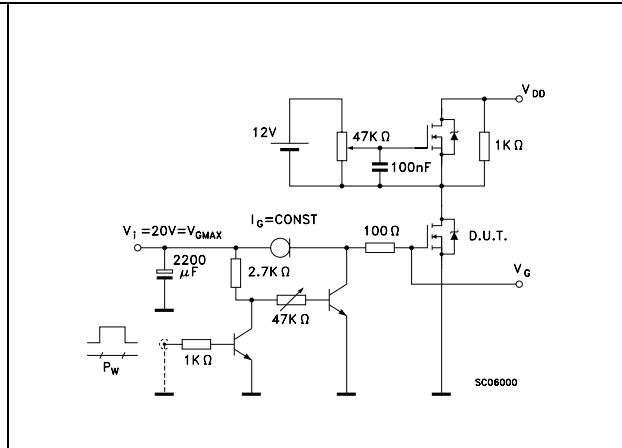


Figure 16. Test circuit for inductive load switching and diode recovery times

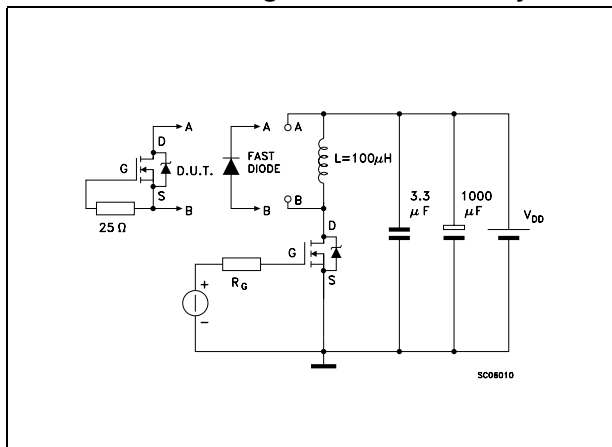


Figure 17. Unclamped Inductive load test circuit

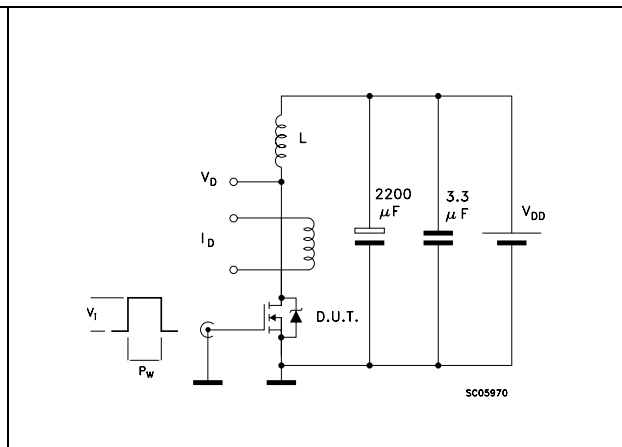


Figure 18. Unclamped inductive waveform

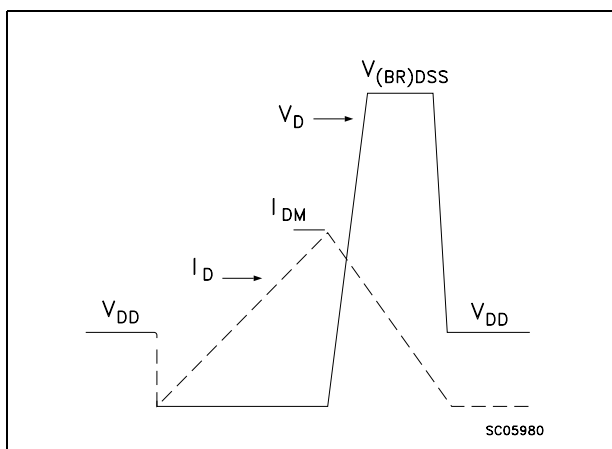
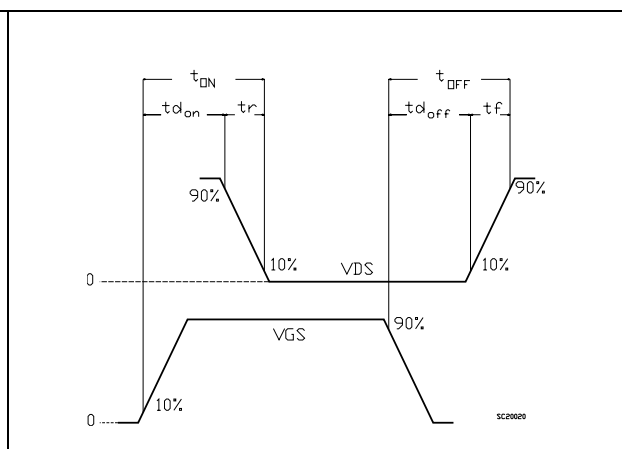


Figure 19. Switching time waveform

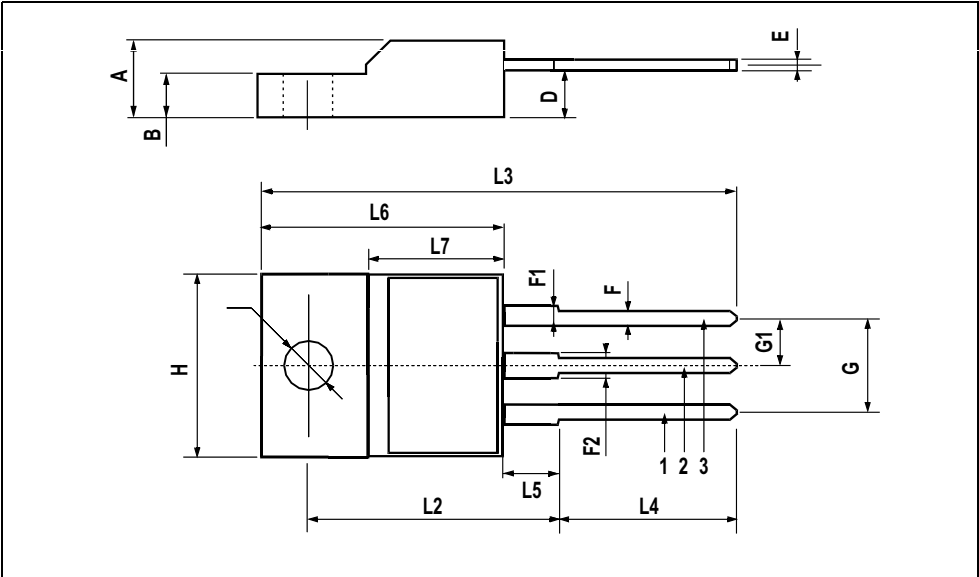


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

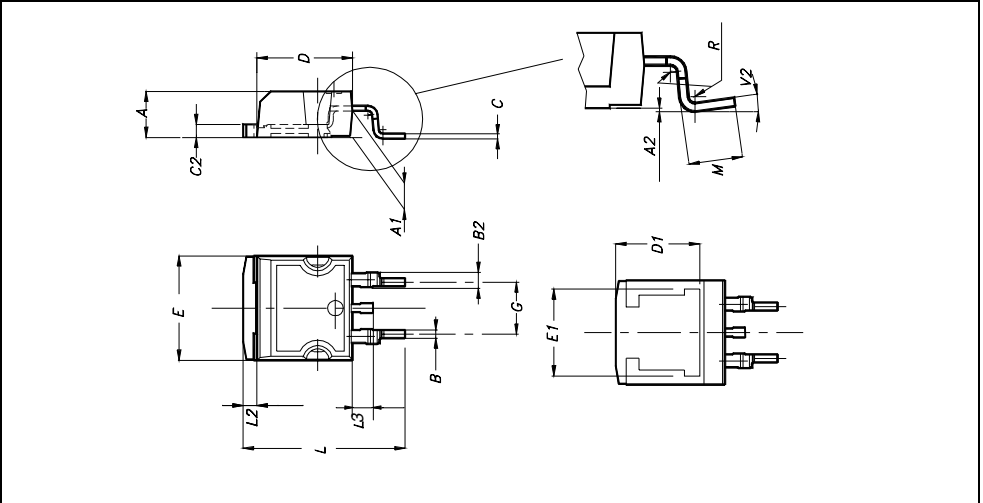
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



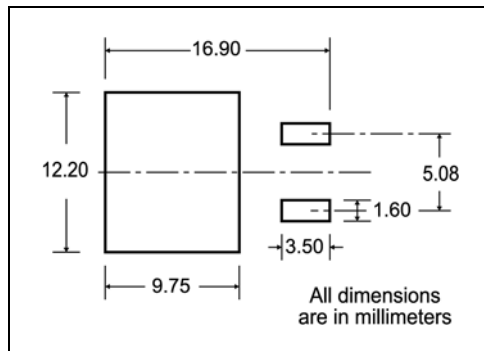
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

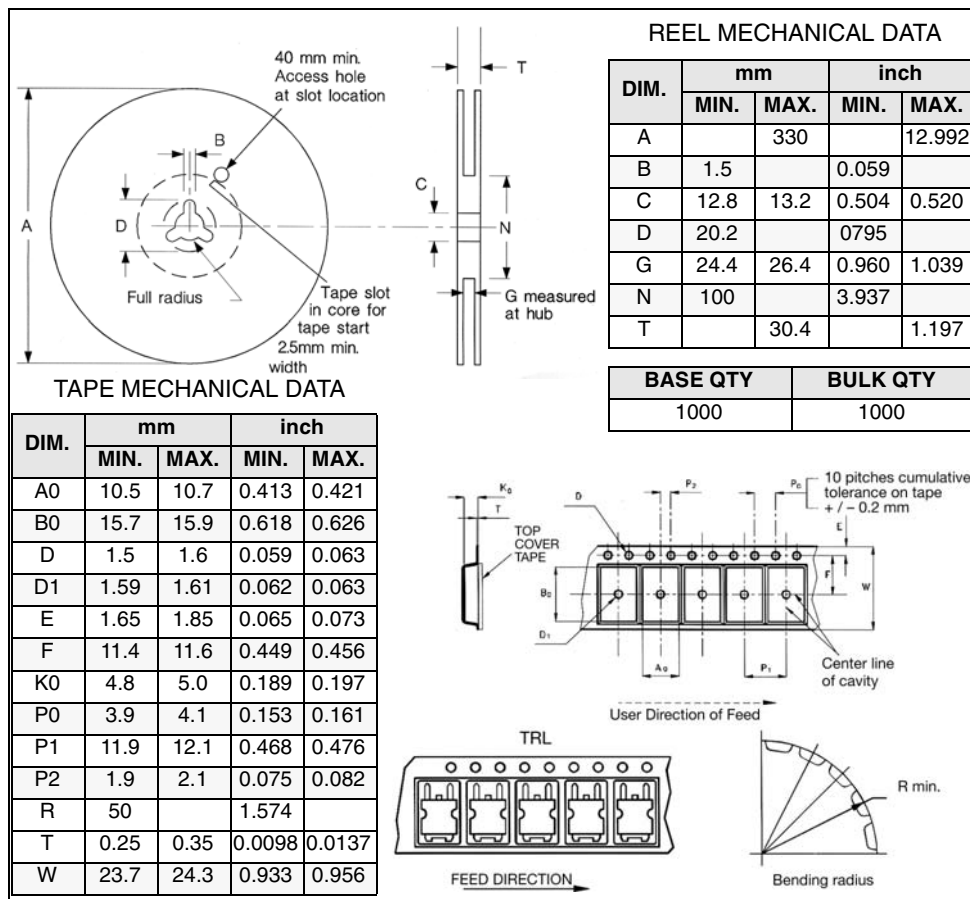


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 8. Revision history

Date	Revision	Changes
09-Sep-2004	1	First Release
10-Jun-2005	2	Typing error, wrong description
26-Jul-2006	3	The document has been reformatted, no content change
31-Aug-2006	4	Typo mistake on order code
21-Dec-2006	5	Various changes on "Test conditions" for Table 5. and Table 6.
12-Jan-2007	6	Order code has been corrected

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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