CC1070 Single Chip Low Power RF Transmitter for Narrowband Systems

Applications

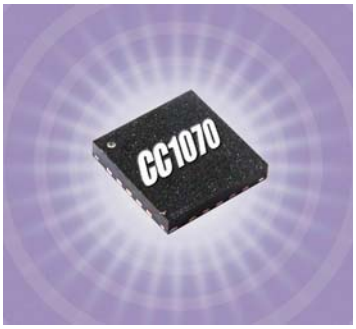
- *Narrowband low power UHF wireless data transmitters*
- *402 / 424 / 426 / 429 / 433 / 447 / 449 / 469 / 868 and 915 MHz ISM/SRD band systems*
- *TPMS – Tire Pressure Monitoring Systems*
- *AMR – Automatic Meter Reading*
- *Wireless alarm and security systems*
- *Home automation*
- *Low power telemetry*

Product Description

CC1070 is a true single-chip UHF transmitter designed for very low power and very low voltage wireless applications. The circuit is mainly intended for the ISM (Industrial, Scientific and Medical) and SRD (Short Range Device) frequency bands at 402, 424, 426, 429, 433, 447, 449, 469, 868 and 915 MHz, but can easily be programmed for multi-channel operation at other frequencies in the 402 - 470 and 804 - 940 MHz range.

The ***CC1070*** is especially suited for narrow-band systems with channel spacings of 12.5 or 25 kHz complying with ARIB STD T-67 and EN 300 220.

The ***CC1070*** main operating parameters can be programmed via a serial bus, thus making ***CC1070*** a very flexible and easy to use transmitter. In a typical application ***CC1070*** will be used together with a microcontroller and a few external passive components.



Features

- True single chip UHF RF transmitter
- Frequency range 402 - 470 MHz and 804 - 940 MHz
- Programmable output power
- Low supply voltage (2.3 to 3.6 V)
- Very few external components required
- Small size (QFN 20 package)
- Pb-free package
- Data rate up to 153.6 kBaud
- OOK, FSK and GFSK data modulation
- Fully on-chip VCO
- Programmable frequency makes crystal temperature drift compensation possible without TCXO
- Suitable for frequency hopping systems
- Suited for systems targeting compliance with EN 300 220, FCC CFR47 part 15 and ARIB STD T-67
- Development kit available
- Easy-to-use software for generating the ***CC1070*** configuration data

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1 Abbreviations

ACP	Adjacent Channel Power
AMR	Automatic Meter Reading
ASK	Amplitude Shift Keying
BOM	Bill Of Materials
bps	bits per second
BT	Bandwidth-Time product (for GFSK)
CW	Continuous Wave
DNM	Do Not Mount
ESR	Equivalent Series Resistance
FHSS	Frequency Hopping Spread Spectrum
FM	Frequency Modulation
FS	Frequency Synthesizer
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
IC	Integrated Circuit
ISM	Industrial Scientific Medical
kbps	kilo bits per second
MCU	Micro Controller Unit
NA	Not Applicable
NRZ	Non Return to Zero
OOK	On-Off Keying
PA	Power Amplifier
PD	Phase Detector / Power Down
PCB	Printed Circuit Board
PN9	Pseudo-random Bit Sequence (9-bit)
PLL	Phase Locked Loop
PSEL	Program Select
RF	Radio Frequency
SPI	Serial Peripheral Interface
SRD	Short Range Device
TBD	To Be Decided/Defined
TX	Transmit (mode)
UHF	Ultra High Frequency
VCO	Voltage Controlled Oscillator
XOSC	Crystal oscillator
XTAL	Crystal

2 Absolute Maximum Ratings

The absolute maximum ratings given Table 1 should under no circumstances be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Min	Max	Unit	Condition
Supply voltage, VDD	-0.3	5.0	V	All supply pins must have the same voltage
Voltage on any pin	-0.3	VDD+0.3, max 5.0	V	
Storage temperature range	-50	150	°C	
Package body temperature		260	°C	Norm: IPC/JEDEC J-STD-020C [1]
Humidity non-condensing	5	85	%	
ESD		500	V	CDM model

Table 1. Absolute maximum ratings

[1] The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices".



Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

3 Operating Conditions

The operating conditions for ***CC1070*** are listed in Table 2.

Parameter	Min	Typ	Max	Unit	Condition / Note
RF Frequency Range	402 804		470 940	MHz MHz	Programmable in <300 Hz steps Programmable in <600 Hz steps
Operating ambient temperature range	-40		105	°C	
Supply voltage	2.3	3.0	3.6	V	The same supply voltage should be used for digital (DVDD) and analog (AVDD) power. A 3.0 ±0.1 V supply is recommended to meet the ARIB STD T-67 output power tolerance requirement.

Table 2. Operating conditions

4 Electrical Specifications

Table 3 to Table 7 gives the ***CC1070*** electrical specifications. All measurements were performed using the 2 layer PCB CC1070EM reference design. This is the same test circuit as shown in Figure 3. Temperature = 25°C, supply voltage = AVDD = DVDD = 3.0 V if nothing else stated. Crystal frequency = 14.7456 MHz.

The electrical specifications given for 868 MHz are also applicable for the 902 – 928 MHz frequency range.

4.1 RF Transmit Section

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Transmit data rate	0.45		153.6	kBaud	The data rate is programmable. See section 10 on page 22 for details. NRZ or Manchester encoding can be used. 153.6 kBaud equals 153.6 kbps using NRZ coding and 76.8 kbps using Manchester coding. See section 9.2 on page 20 for details.
Binary FSK frequency separation	0 0		108 216	kHz kHz	in 402 - 470 MHz range in 804 - 940 MHz range 108/216 kHz is the maximum separation at 1.84 MHz reference frequency. Larger separations can be achieved at higher reference frequencies.
Output power 433 MHz 868 MHz		 -20 to +10 -20 to +8		 dBm dBm	Delivered to 50 Ω single-ended load. The output power is programmable and should not be programmed to exceed +10/+8 dBm at 433/868 MHz under any operating conditions. See section 13 on page 26 for details.
Output power tolerance		 -4 +3		 dB dB	At maximum output power At 2.3 V, +105°C At 3.6 V, -40°C
Harmonics, radiated CW 2nd harmonic, 433 MHz, +10 dBm 3rd harmonic, 433 MHz, +10 dBm 2nd harmonic, 868 MHz, +8 dBm 3rd harmonic, 868 MHz, +8 dBm		 -50 -60 -50 -57		 dBc dBc dBc dBc	Harmonics are measured as EIRP values according to EN 300 220. The antenna (SMAFF-433 and SMAFF-868 from R.W. Badland) plays a part in attenuating the harmonics.
Adjacent channel power (GFSK) 12.5 kHz channel spacing, 433 MHz 25 kHz channel spacing, 868 MHz		 -47 -50		 dBc dBc	For 12.5 kHz channel spacing ACP is measured in a ±4.25 kHz bandwidth at ±12.5 kHz offset. Modulation: 2.4 kBaud NRZ PN9 sequence, ±2.025 kHz frequency deviation. For 25 kHz channel spacing ACP is measured in a ±8.5 kHz bandwidth at ±25 kHz offset. Modulation: 4.8 kBaud NRZ PN9 sequence, ±2.475 kHz frequency deviation.
Occupied bandwidth (99.5%,GFSK) 12.5 kHz channel spacing, 433 MHz 25 kHz channel spacing, 868 MHz		 7 10		 kHz kHz	Bandwidth for 99.5% of total average power. Modulation for 12.5 channel spacing: 2.4 kBaud NRZ PN9 sequence, ±2.025 kHz frequency deviation. Modulation for 25 kHz channel spacing: 4.8 kBaud NRZ PN9 sequence, ±2.475 kHz frequency deviation.

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Modulation bandwidth, 868 MHz 19.2 kBaud, ±9.9 kHz frequency deviation 38.4 kBaud, ±19.8 kHz frequency deviation		 48 106		 kHz kHz	Bandwidth where the power envelope of modulation equals –36 dBm. Spectrum analyzer RBW = 1 kHz.
Spurious emission, radiated CW 47-74, 87.5-118, 174-230, 470-862 MHz 9 kHz – 1 GHz 1 – 4 GHz			 -54 -36 -30	 dBm dBm dBm	At maximum output power, +10/+8 dBm at 433/868 MHz. To comply with EN 300 220, FCC CFR47 part 15 and ARIB STD T-67 an external (antenna) filter, as implemented in the application circuit in Figure 14, must be used and tailored to each individual design to reduce out-of-band spurious emission levels. Spurious emissions can be measured as EIRP values according to EN 300 220. The antenna (SMAFF-433 and SMAFF-868 from R.W. Badland) plays a part in attenuating the spurious emissions. If the output power is increased using an external PA, a filter must be used to attenuate spurs below 862 MHz when operating in the 868 MHz frequency band in Europe. Application Note *AN036 CC1020/1021 Spurious Emission* presents and discusses a solution that reduces the TX mode spurious emission close to 862 MHz by increasing the REF_DIV from 1 to 7.
Optimum load impedance 433 MHz 868 MHz 915 MHz		 91 + j16 34 + j25 28 + j21		 Ω Ω Ω	Transmit mode. For matching details see section 13 on page 26.

Table 3. RF transmit parameters

4.2 Crystal Oscillator Section

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Crystal Oscillator Frequency	4.9152	14.7456	19.6608	MHz	
Crystal operation		Parallel			C4 and C5 are loading capacitors. See section 17 on page 34 for details.
Crystal load capacitance	12 12 12	22 16 16	30 30 16	pF pF pF	4-6 MHz, 22 pF recommended 6-8 MHz, 16 pF recommended 8-20 MHz, 16 pF recommended
Crystal oscillator start-up time		1.55 0.90 0.95 0.63		ms ms ms ms	4.9152 MHz, 12 pF load 9.8304 MHz, 12 pF load 14.7456 MHz, 16 pF load 19.6608 MHz, 12 pF load
External clock signal drive, sine wave		300		mVpp	The external clock signal must be connected to XOSC_Q1 using a DC block (10 nF). Set *XOSC_BYPASS* = 0 in the *INTERFACE* register when using an external clock signal with low amplitude or a crystal.
External clock signal drive, full-swing digital external clock		0 - VDD		V	The external clock signal must be connected to XOSC_Q1. No DC block shall be used. Set *XOSC_BYPASS* = 1 in the *INTERFACE* register when using a full-swing digital external clock
Reference frequency accuracy requirement		+/- 5.7 +/- 2.8 +/- 4 +/- 7		ppm ppm ppm ppm	433 MHz (EN 300 220) 868 MHz (EN 300 220) Must be less than ±5.7 / ±2.8 ppm to comply with EN 300 220 25 kHz channel spacing at 433/868 MHz. Must be less than ±4 ppm to comply with Japanese 12.5 kHz channel spacing regulations (ARIB STD T-67). NOTE: This imposes special requirements on the receiver of the signal. Must be less than ±7 ppm to comply with Korean 12.5 kHz channel spacing regulations. NOTE: This imposes special requirements on the receiver of the signal. NOTE: The reference frequency accuracy (initial tolerance) and drift (aging and temperature dependency) will determine the frequency accuracy of the transmitted signal. Crystal oscillator temperature compensation can be done using the fine frequency programmability.

Table 4. Crystal oscillator parameters

4.3 Frequency Synthesizer Section

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Phase noise, 402 – 470 MHz					Unmodulated carrier
12.5 kHz channel spacing		−87 −95 −100 −105 −114		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz	At 12.5 kHz offset from carrier At 25 kHz offset from carrier At 50 kHz offset from carrier At 100 kHz offset from carrier At 1 MHz offset from carrier Measured using loop filter components given in Table 10. The phase noise will be higher for larger PLL loop filter bandwidth.
Phase noise, 804 - 940 MHz					Unmodulated carrier
25 kHz channel spacing		−81 −89 −96 −103 −122		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz	At 12.5 kHz offset from carrier At 25 kHz offset from carrier At 50 kHz offset from carrier At 100 kHz offset from carrier At 1 MHz offset from carrier Measured using loop filter components given in Table 10. The phase noise will be higher for larger PLL loop filter bandwidth.
PLL loop bandwidth					After PLL and VCO calibration. The PLL loop bandwidth is programmable
12.5 kHz channel spacing, 433 MHz		5		kHz	
25 kHz channel spacing, 868 MHz		7		kHz	
PLL lock time (TX_1 / TX_2 turn time)					One channel frequency step to RF frequency within ±10% of channel spacing. Depends on loop filter component values and *PLL_BW* register setting. See Table 20 on page 32 for more details.
12.5 kHz channel spacing, 433 MHz		180		us	
25 kHz channel spacing, 868 MHz		270		us	
500 kHz channel spacing		14		us	
PLL turn-on time. From power down mode with crystal oscillator running.					Time from writing to registers to RF frequency within ±10% of channel spacing. Depends on loop filter component values and *PLL_BW* register setting. See Table 19 on page 32 for more details.
12.5 kHz channel spacing, 433 MHz		3.2		ms	
25 kHz channel spacing, 868 MHz		2.5		ms	
500 kHz channel spacing		700		us	

Table 5. Frequency synthesizer parameters

4.4 Digital Inputs / Outputs

Parameter	Min	Typ	Max	Unit	Condition / Note
Logic "0" input voltage	0		0.3* VDD	V	
Logic "1" input voltage	0.7* VDD		VDD	V	
Logic "0" output voltage	0		0.4	V	Output current −2.0 mA, 3.0 V supply voltage
Logic "1" output voltage	2.5		VDD	V	Output current 2.0 mA, 3.0 V supply voltage
Logic "0" input current	NA		−1	μA	Input signal equals GND. PSEL has an internal pull-up resistor and during configuration the current will be -350 μA.
Logic "1" input current	NA		1	μA	Input signal equals VDD
DIO setup time	20			ns	TX mode, minimum time DIO must be ready before the positive edge of DCLK. Data should be set up on the negative edge of DCLK.
DIO hold time	10			ns	TX mode, minimum time DIO must be held after the positive edge of DCLK. Data should be set up on the negative edge of DCLK.
Serial interface (PCLK, PDI, PDO and PSEL) timing specification					See Table 11 on page 20 for more details
PA_EN pin drive		 0.90 0.87 0.81 0.69 0.93 0.92 0.89 0.79		 mA mA mA mA mA mA mA mA	Source current 0 V on PA_EN pin 0.5 V on PA_EN pin 1.0 V on PA_EN pin 1.5 V on PA_EN pin Sink current 3.0 V on PA_EN pin 2.5 V on PA_EN pin 2.0 V on PA_EN pin 1.5 V on PA_EN pin

Table 6. Digital inputs / outputs parameters

4.5 Current Consumption

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Power Down mode		0.2	1	μA	Oscillator core off
Current consumption, 433/868 MHz:					
P = −20 dBm		12.3/13.9		mA	The output power is delivered to a 50 Ω single-ended load.
P = −5 dBm		14.7/16.8		mA	
P = 0 dBm		17.5/20.5		mA	See section 12.3 on page 25 for more details.
P = +5 dBm		21.5/25.3		mA	
P = +8 dBm		25.5/33.1		mA	
P = +10 dBm		31/NA		mA	
Current consumption, crystal oscillator		65		μA	14.7456 MHz, 16 pF load crystal
Current consumption, crystal oscillator and bias		500		μA	14.7456 MHz, 16 pF load crystal
Current consumption, crystal oscillator, bias and synthesizer		7.5		mA	14.7456 MHz, 16 pF load crystal

Table 7. Current consumption

5 Pin Assignment

Table 8 provides an overview of the ***CC1070*** pinout.

The ***CC1070*** comes in a QFN20 type package.

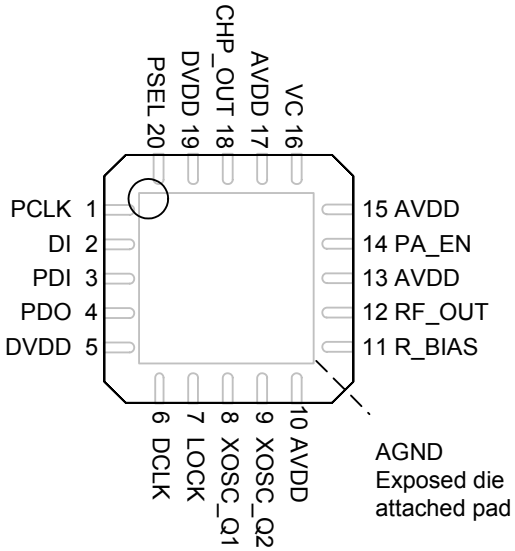


Figure 1. *CC1070* package (top view)

Pin no.	Pin name	Pin type	Description
-	AGND	Ground (analog)	Exposed die attached pad. Must be soldered to a solid ground plane as this is the ground connection for all analog modules See page 39 for more details.
1	PCLK	Digital input	Programming clock for SPI configuration interface
2	DI	Digital input	Data input in transmit mode
3	PDI	Digital input	Programming data input for SPI configuration interface
4	PDO	Digital output	Programming data output for SPI configuration interface
5	DVDD	Power (digital)	Power supply (3 V typical) for digital modules and digital I/O
6	DCLK	Digital output	Clock for transmit data
7	LOCK	Digital output	PLL Lock indicator, active low. Output is asserted (low) when PLL is in lock. The pin can also be used as a general digital output.
8	XOSC_Q1	Analog input	Crystal oscillator or external clock input
9	XOSC_Q2	Analog output	Crystal oscillator
10	AVDD	Power (analog)	Power supply (3 V typical) for crystal oscillator and bias generator (double bonded).
11	R_BIAS	Analog output	Connection for external precision bias resistor (82 kΩ, ± 1%)
12	RF_OUT	RF output	RF signal output to antenna
13	AVDD	Power (analog)	Power supply (3 V typical) for LO buffers, prescaler and PA first stage
14	PA_EN	Digital output	General digital output. Can be used for controlling an external PA, if higher output power is needed.
15	AVDD	Power (analog)	Power supply (3 V typical) for VCO
16	VC	Analog input	VCO control voltage input from external loop filter
17	AVDD	Power (analog)	Power supply (3 V typical) for charge pump and phase detector
18	CHP_OUT	Analog output	PLL charge pump output to external loop filter
19	DVDD	Power (digital)	Power supply connection (3 V typical) for digital modules
20	PSEL	Digital input	Programming chip select, active low, for configuration interface. Internal pull-up resistor.

Table 8. Pin assignment overview

Note:
DCLK, DI and LOCK are high-impedance (3-state) in power down (*BIAS_PD* = 1 in the *MAIN* register).

The exposed die attached pad **must** be soldered to solid ground plane as this is the main ground connection for the chip.

6 Circuit Description

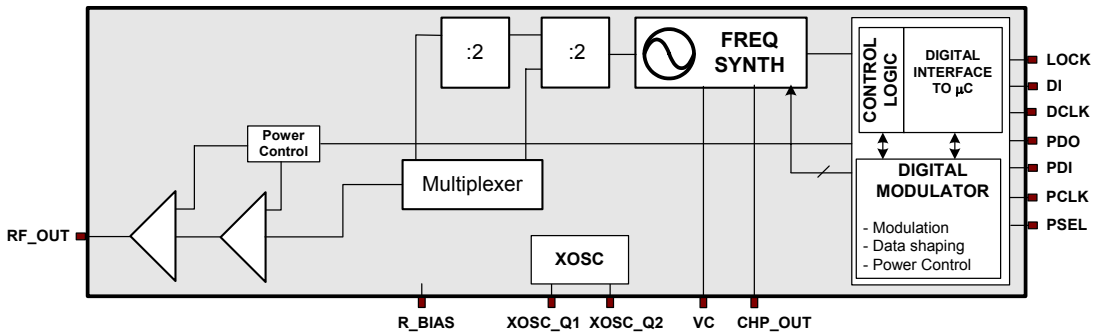


Figure 2. *CC1070* simplified block diagram

A simplified block diagram of ***CC1070*** is shown in Figure 2. Only signal pins are shown.

During transmit operation, the synthesized RF frequency is fed directly to the power amplifier (PA). The RF output is frequency shift keyed (FSK) by the digital bit stream that is fed to the DI pin. Optionally, the internal Gaussian filter can be enabled for Gaussian FSK (GFSK).

The frequency synthesizer includes a completely on-chip LC VCO. The VCO operates in the frequency range 1.608-1.880 GHz. The CHP_OUT pin is the charge pump output and VC is the control node of the on-chip VCO. The external loop filter is placed between these pins. A crystal is to be connected between XOSC_Q1 and XOSC_Q2. A lock signal is available from the PLL.

The 4-wire SPI serial interface is used for configuration.

7 Application Circuit

Very few external components are required for the operation of ***CC1070***. A typical application circuit is shown in Figure 3. The external components are described in Table 9 and values are given in Table 10.

Output matching
L2, C2 and C3 are used to match the transmitter to 50 Ω. See section 13 on page 26 for details. Component values for the matching network are easily calculated using the SmartRF® Studio software.

Bias resistor
The precision bias resistor R1 is used to set an accurate bias current.

PLL loop filter
The loop filter consists of two resistors (R2 and R3) and three capacitors (C6-C8). C7 and C8 may be omitted in applications where high loop bandwidth is desired. The values shown in Table 10 can be used for data rates up to 4.8 kBaud. Component values for higher data rates are easily found using the SmartRF® Studio software.

Crystal
An external crystal with two loading capacitors (C4 and C5) is used for the crystal oscillator. See section 17 on page 34 for details.

Additional filtering
Additional external components (e.g. RF LC or SAW filter) may be used in order to improve the performance in specific applications. See section 13 on page 26 for further information.

Power supply decoupling and filtering
Power supply decoupling and filtering must be used (not shown in the application circuit). The placement and size of the decoupling capacitors and the power supply filtering are very important to

achieve the optimum performance for narrowband applications. TI provides a reference design that should be followed very closely.

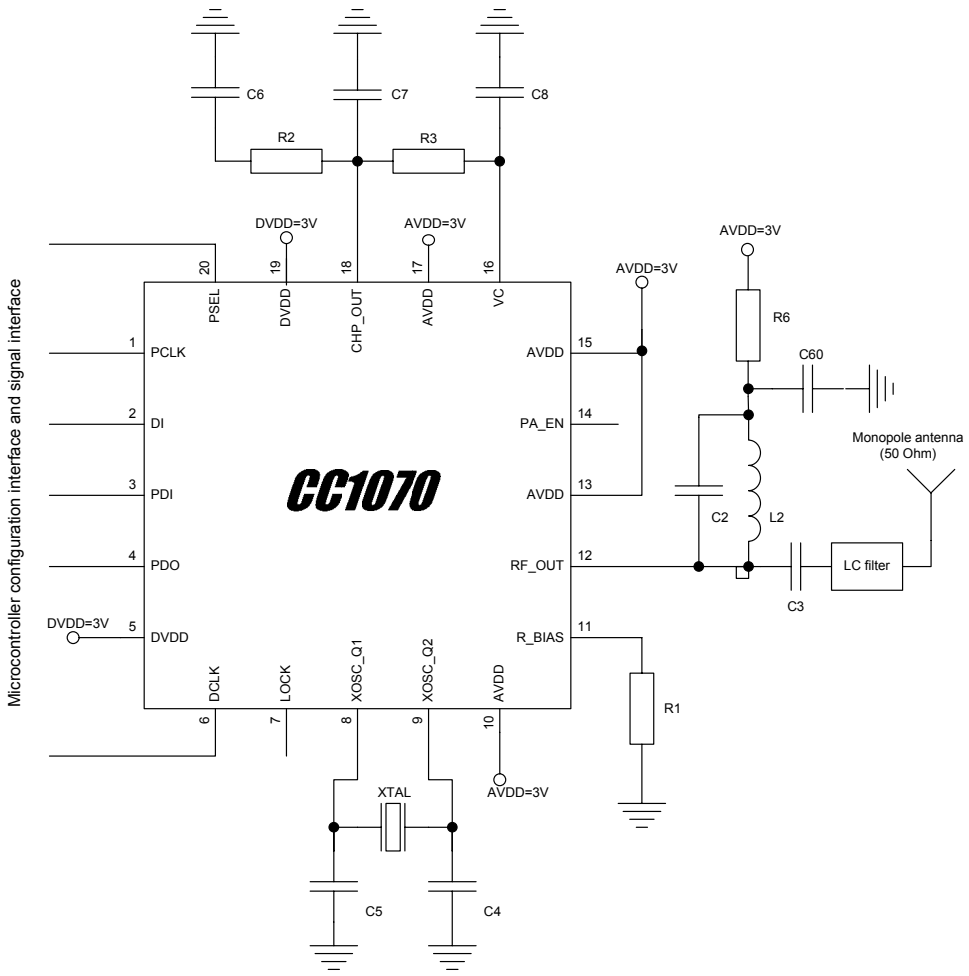


Figure 3. Typical application and test circuit (power supply decoupling not shown)

Ref	Description
C2	PA match, see page 26
C3	PA output match and dc block, see page 26
C4	Crystal load capacitor, see page 34
C5	Crystal load capacitor, see page 34
C6	PLL loop filter capacitor
C7	PLL loop filter capacitor (may be omitted for highest loop bandwidth)
C8	PLL loop filter capacitor (may be omitted for highest loop bandwidth)
C60	Decoupling capacitor
L2	PA match and DC bias (supply voltage), see page 26
R1	Precision resistor for current reference generator
R2	PLL loop filter resistor
R3	PLL loop filter resistor
R6	PA output match, see page 26
XTAL	Crystal, see page 34

Table 9. Overview of external components (excluding supply decoupling capacitors)

Item	433 MHz	868 MHz	915 MHz
C2	2.2 pF, 5%, NP0, 0402	1.5 pF, 5%, NP0, 0402	1.5 pF, 5%, NP0, 0402
C3	5.6 pF, 5%, NP0, 0402	10 pF, 5%, NP0, 0402	10 pF, 5%, NP0, 0402
C4	22 pF, 5%, NP0, 0402	22 pF, 5%, NP0, 0402	22 pF, 5%, NP0, 0402
C5	12 pF, 5%, NP0, 0402	12 pF, 5%, NP0, 0402	12 pF, 5%, NP0, 0402
C6	220 nF, 10%, X7R, 0603	100 nF, 10%, X7R, 0603	100 nF, 10%, X7R, 0603
C7	8.2 nF, 10%, X7R, 0402	3.9 nF, 10%, X7R, 0402	3.9 nF, 10%, X7R, 0402
C8	2.2 nF, 10%, X7R, 0402	1.0 nF, 10%, X7R, 0402	1.0 nF, 10%, X7R, 0402
C60	220 pF, 5%, NP0, 0402	220 pF, 5%, NP0, 0402	220 pF, 5%, NP0, 0402
L2	22 nH, 5%, 0402	6.8 nH, 5%, 0402	6.8 nH, 5%, 0402
R1	82 kΩ, 1%, 0402	82 kΩ, 1%, 0402	82 kΩ, 1%, 0402
R2	1.5 kΩ, 5%, 0402	2.2 kΩ, 5%, 0402	2.2 kΩ, 5%, 0402
R3	4.7 kΩ, 5%, 0402	6.8 kΩ, 5%, 0402	6.8 kΩ, 5%, 0402
R6	82 Ω, 5%, 0402	82 Ω, 5%, 0402	82 Ω, 5%, 0402
XTAL	14.7456 MHz crystal, 16 pF load	14.7456 MHz crystal, 16 pF load	14.7456 MHz crystal, 16 pF load

Note: Items shaded vary for different frequencies. For 433 MHz, 12.5 kHz channel, a loop filter with lower bandwidth is used to improve adjacent and alternate channel rejection.

Table 10. Bill of materials for the application circuit in Figure 3

Note:
The PLL loop filter component values in Table 10 (R2, R3, C6-C8) can be used for data rates up to 4.8 kBaud. The SmartRF® Studio software provides component values for other data rates using the equations on page 29.

In the CC1070EM reference design LQG15HS series inductors from Murata have been used.

8 Configuration Overview

CC1070 can be configured to achieve optimum performance for different applications. Through the programmable configuration registers the following key parameters can be programmed:

- RF output power
- Frequency synthesizer key parameters: RF output frequency, FSK frequency separation, crystal oscillator reference frequency
- Power-down / power-up mode
- Crystal oscillator power-up / power down
- Data rate and data format (NRZ, Manchester coded or UART interface)
- Synthesizer lock indicator mode
- FSK / GFSK / OOK modulation

8.1 Configuration Software

TI provides users of *CC1070* with a software program, SmartRF® Studio (Windows interface) that generates all necessary *CC1070* configuration data based on the user's selections of various parameters. These hexadecimal numbers will then be the necessary input to the microcontroller for the configuration of *CC1070*. In addition, the program will provide the user with the component values needed for the output matching circuit, the PLL loop filter and the LC filter.

Figure 4 shows the user interface of the *CC1070* configuration software.

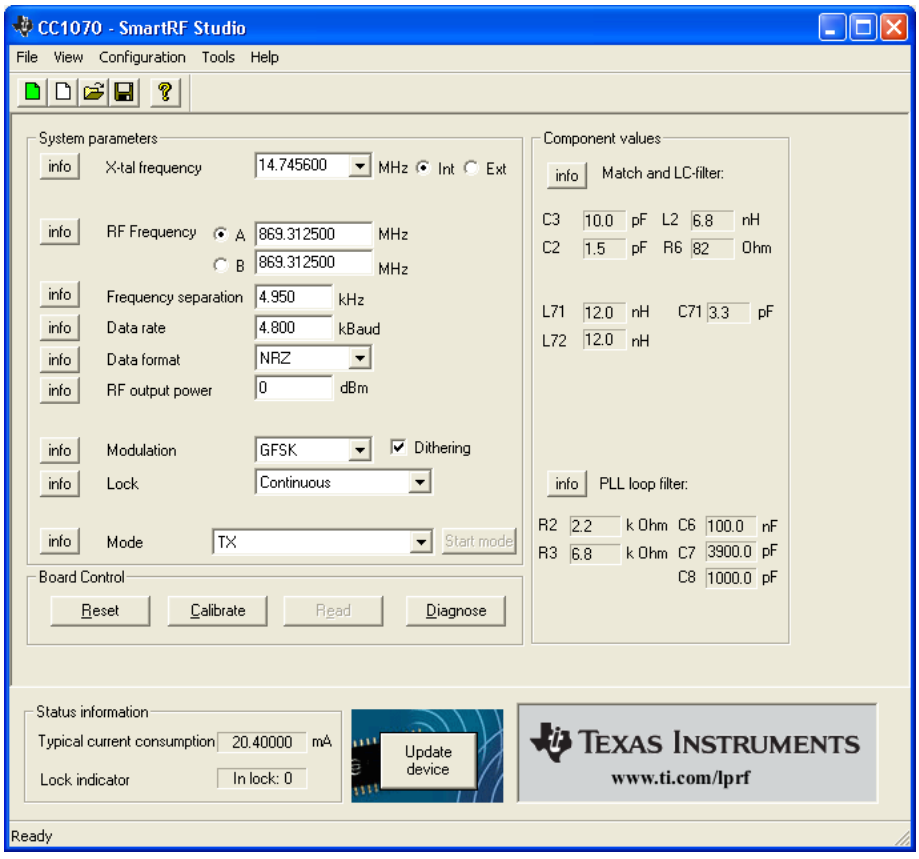


Figure 4. SmartRF® Studio user interface

9 Microcontroller Interface

Used in a typical system, ***CC1070*** will interface to a microcontroller. This microcontroller must be able to:

- Program ***CC1070*** into different modes via the 4-wire serial configuration interface (PDI, PDO, PCLK and PSEL)
- Interface to the synchronous data signal interface (DI and DCLK)
- Optionally, the microcontroller can do data encoding
- Optionally, the microcontroller can monitor the LOCK pin for frequency lock status or other status information.

Configuration interface
The microcontroller interface is shown in Figure 5. The microcontroller uses 3 or 4 I/O pins for the configuration interface (PDI, PDO, PCLK and PSEL). PDO should be connected to a microcontroller input. PDI, PCLK and PSEL must be microcontroller outputs. One I/O pin can be saved if PDI and PDO are connected together and a bi-directional pin is used at the microcontroller.

The microcontroller pins connected to PDI, PDO and PCLK can be used for other purposes when the configuration interface is not used. PDI, PDO and PCLK are high impedance inputs as long as PSEL is not activated (active low).

PSEL has an internal pull-up resistor and should be left open (tri-stated by the microcontroller) or set to a high level during power down mode in order to prevent a trickle current flowing in the pull-up.

Signal interface
The DI pin is used for data to be transmitted. DCLK providing the data timing should be connected to a microcontroller input.

PLL lock signal
Optionally, one microcontroller pin can be used to monitor the LOCK signal. This signal is at low logic level when the PLL is in lock. It can also be used to monitor other internal test signals.

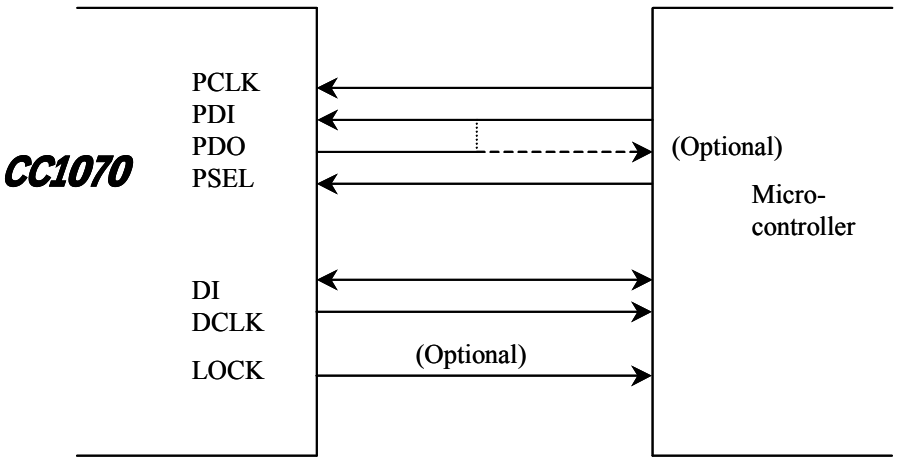


Figure 5. Microcontroller interface

9.1 4-wire Serial Configuration Interface

CC1070 is configured via a simple 4-wire SPI-compatible interface (PDI, PDO, PCLK and PSEL) where ***CC1070*** is the slave. There are 22 8-bit configuration registers and 6 8-bit test-only registers, each addressed by a 7-bit address. A Read/Write bit initiates a read or write operation. A full configuration of ***CC1070*** requires sending 22 data frames of 16 bits each (7 address bits, R/W bit and 8 data bits). The time needed for a full configuration depends on the PCLK frequency. With a PCLK frequency of 10 MHz the full configuration is done in less than 36 μs. Setting the device in power down mode requires sending one frame only and will in this case take less than 2 μs. All registers are also readable.

In each write-cycle, 16 bits are sent on the PDI-line. The seven most significant bits of each data frame (*A6:0)* are the address-bits. *A6* is the MSB (Most Significant Bit) of the address and is sent as the first bit. The next bit is the R/W bit (high for write, low for read). The 8 data-bits are then transferred (*D7:0*). During address and data transfer the PSEL (Program SELect) must be kept low. See Figure 6.

The timing for the programming is also shown in Figure 6 with reference to Table 11. The clocking of the data on PDI is done on the positive edge of PCLK. Data should be set up on the negative edge of PCLK by the microcontroller. When the last bit, *D0*, of the 8 data-bits has been loaded, the data word is loaded in the internal configuration register.

The configuration data will be retained during a programmed power-down mode, but not when the power-supply is turned off. The registers can be programmed in any order.

The configuration registers can also be read by the microcontroller via the same configuration interface. The seven address bits are sent first, then the R/W bit set low to initiate the data read-back. ***CC1070*** then returns the data from the addressed register. PDO is used as the data output and must be configured as an input by the microcontroller. The PDO is set at the negative edge of PCLK and should be sampled at the positive edge. The read operation is illustrated in Figure 7.

PSEL must be set high between each read/write operation.

There are also 5 read-only status registers.

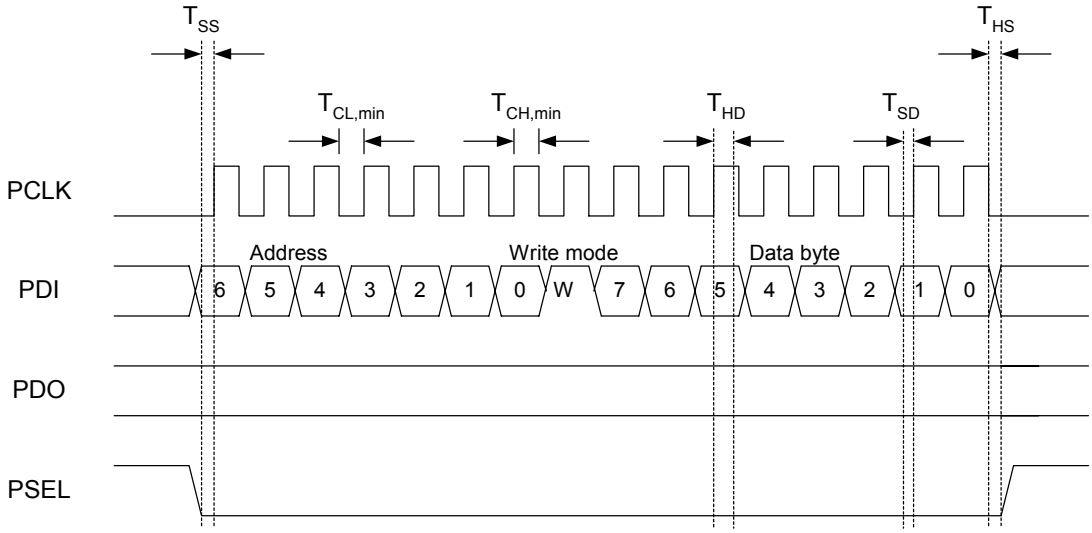


Figure 6. Configuration registers write operation

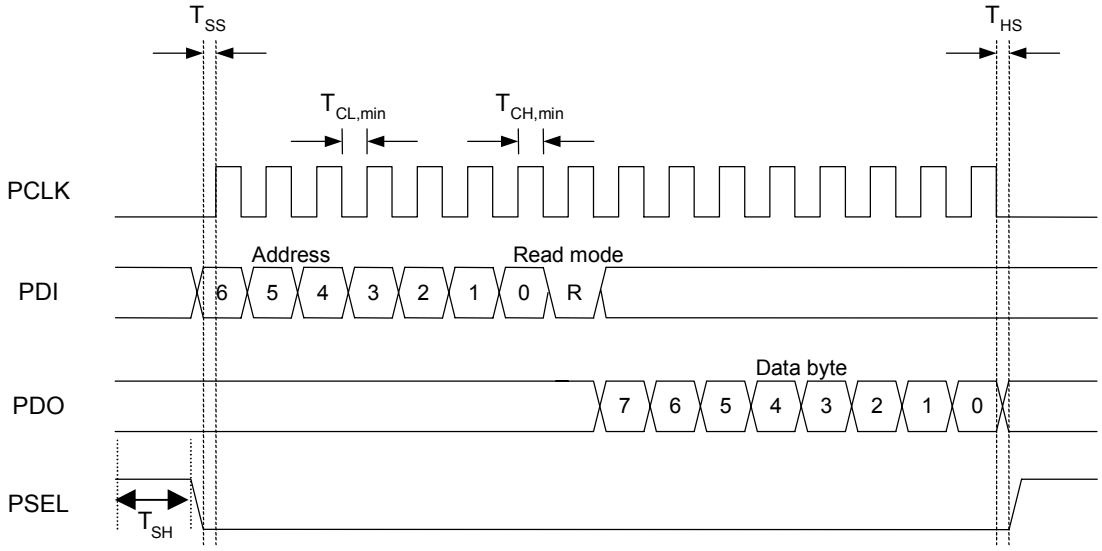


Figure 7. Configuration registers read operation

Parameter	Symbol	Min	Max	Unit	Conditions
PCLK, clock frequency	F_{PCLK}		10	MHz	
PCLK low pulse duration	$T_{CL,min}$	50		ns	The minimum time PCLK must be low.
PCLK high pulse duration	$T_{CH,min}$	50		ns	The minimum time PCLK must be high.
PSEL setup time	T_{SS}	25		ns	The minimum time PSEL must be low before *positive* edge of PCLK.
PSEL hold time	T_{HS}	25		ns	The minimum time PSEL must be held low after the *negative* edge of PCLK.
PSEL high time	T_{SH}	50		ns	The minimum time PSEL must be high.
PDI setup time	T_{SD}	25		ns	The minimum time data on PDI must be ready before the *positive* edge of PCLK.
PDI hold time	T_{HD}	25		ns	The minimum time data must be held at PDI, after the *positive* edge of PCLK.
Rise time	T_{rise}		100	ns	The maximum rise time for PCLK and PSEL
Fall time	T_{fall}		100	ns	The maximum fall time for PCLK and PSEL

Note: The setup and hold times refer to 50% of VDD. The rise and fall times refer to 10% / 90% of VDD. The maximum load that this table is valid for is 20 pF.

Table 11. Serial interface, timing specification

9.2 Signal Interface

The ***CC1070*** can be used with NRZ (Non-Return-to-Zero) data or Manchester (also known as bi-phase-level) encoded data. The data format is controlled by the *DATA_FORMAT[1:0]* bits in the *MODEM* register.

CC1070 can be configured for three different data formats:

Synchronous NRZ mode
During transmit operation, the ***CC1070*** provides the data clock at DCLK and DI is used as data input. Data is clocked into ***CC1070*** at the rising edge of DCLK. The data is modulated at RF without encoding. See Figure 8.

Synchronous Manchester encoded mode
During transmit operation, the ***CC1070*** provides the data clock at DCLK and DI is used as data input. Data is clocked into ***CC1070*** at the rising edge of DCLK and should be in NRZ format. The data is modulated at RF with Manchester code. The encoding is done by ***CC1070***. In this mode the effective bit rate is half the baud rate due to the coding. As an example, 19.2 kBaud Manchester encoded data corresponds to a 9.6 kbps. See Figure 9.

Transparent Asynchronous UART mode
During transmit operation, DI is used as data input. The data is modulated at RF without synchronization or encoding. In this mode, the DCLK pin is not active and can be set to a high or low level by *DATA_FORMAT[0]*. See Figure 10.

Manchester encoding and decoding
In the *Synchronous Manchester encoded mode* ***CC1070*** uses Manchester coding when modulating the data. The Manchester code is based on transitions; a “0” is encoded as a low-to-high transition, a “1” is encoded as a high-to-low transition. See Figure 11.

The Manchester code ensures that the signal has a constant DC component, which is necessary in some FSK receivers/demodulators. Using this mode also ensures compatibility with e.g. CC400/CC900 designs.

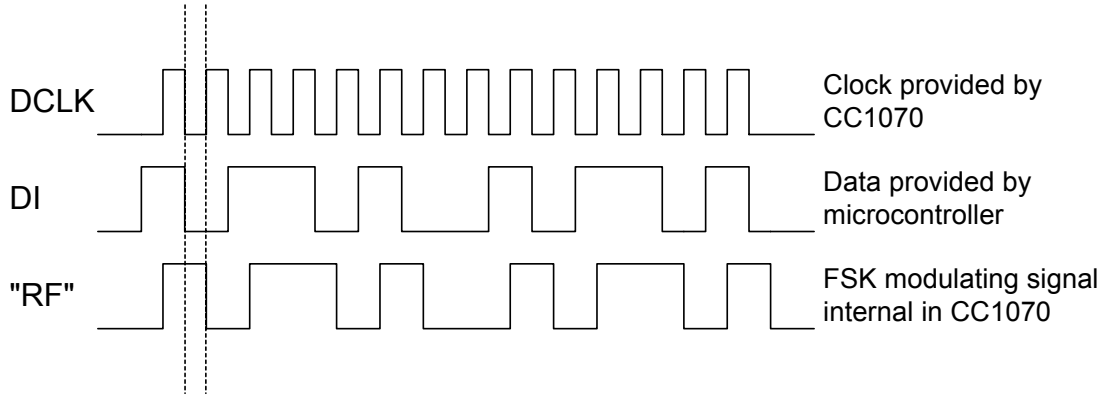


Figure 8. Synchronous NRZ mode

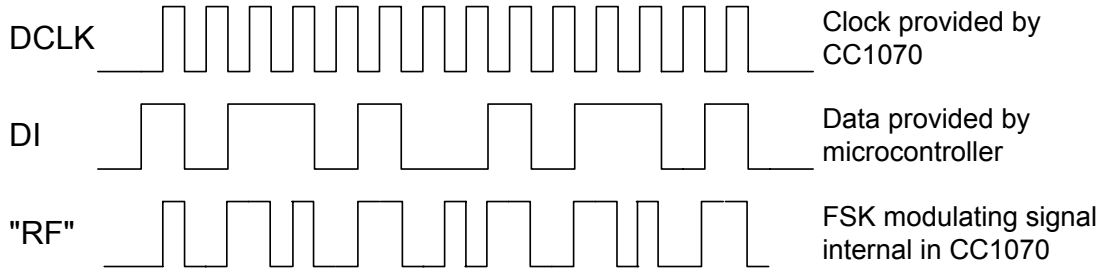


Figure 9. Synchronous Manchester encoded mode

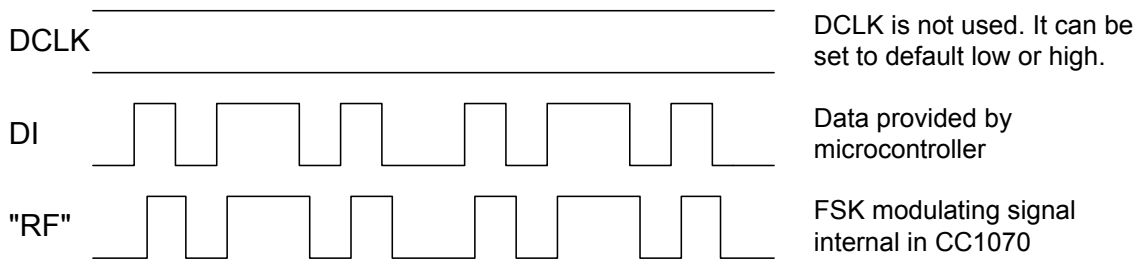


Figure 10. Transparent Asynchronous UART mode

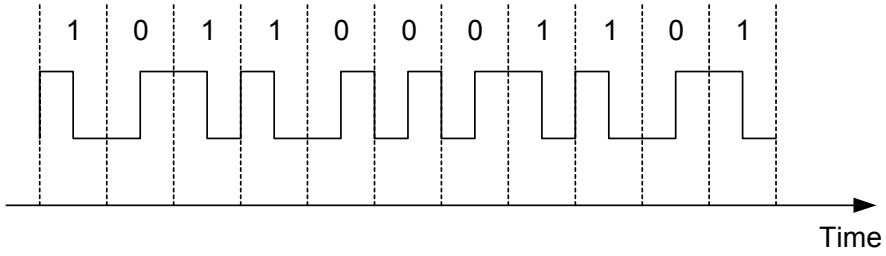


Figure 11. Manchester encoding

10 Data Rate Programming

The data rate (baud rate) is programmable and depends on the crystal frequency and the programming of the *CLOCK* (*CLOCK_A* and *CLOCK_B)* registers.

The baud rate (B.R) is given by

$$B.R. = \frac{f_{xosc}}{8 \cdot (REF_DIV + 1) \cdot DIV1 \cdot DIV2}$$

where DIV1 and DIV2 are given by the value of *MCLK_DIV1* and *MCLK_DIV2*.

Table 14 shows some possible data rates as a function of crystal frequency in synchronous mode. In asynchronous transparent UART mode any data rate up to 153.6 kBaud can be used.

MCLK_DIV1[2:0]	DIV1
000	2.5
001	3
010	4
011	7.5
100	12.5
101	40
110	48
111	64

Table 12. DIV1 for different settings of MCLK_DIV1

MCLK_DIV2[1:0]	DIV2
00	1
01	2
10	4
11	8

Table 13. DIV2 for different settings of MCLK_DIV2

Data rate [kBaud]	Crystal frequency [MHz]						
	4.9152	7.3728	9.8304	12.288	14.7456	17.2032	19.6608
0.45		X			X		
0.5				X			
0.6	X	X	X	X	X	X	X
0.9		X			X		
1				X			
1.2	X	X	X	X	X	X	X
1.8		X			X		
2				X			
2.4	X	X	X	X	X	X	X
3.6		X			X		
4				X			
4.096			X				X
4.8	X	X	X	X	X	X	X
7.2		X			X		
8				X			
8.192			X				X
9.6	X	X	X	X	X	X	X
14.4		X			X		
16				X			
16.384			X				X
19.2	X	X	X	X	X	X	X
28.8		X			X		
32				X			
32.768			X				X
38.4	X	X	X	X	X	X	X
57.6		X			X		
64				X			
65.536							X
76.8	X	X	X	X	X	X	X
115.2		X			X		
128				X			
153.6	X	X	X	X	X	X	X

Table 14. Some possible data rates versus crystal frequency

11 Frequency Programming

Programming the frequency word in the configuration registers sets the operation frequency. There are two frequency words registers, termed *FREQ_A* and *FREQ_B*, which can be programmed to two different frequencies. They can be used for two different channels. The F_REG bit in the MAIN register selects frequency word A or B.

The frequency word is located in *FREQ_2A:FREQ_1A:FREQ_0A* and *FREQ_2B:FREQ_1B:FREQ_0B* for the *FREQ_A* and *FREQ_B* word respectively. The LSB of the *FREQ_0* registers are used to enable dithering, section 11.1.

The PLL output frequency is given by:

$$f_c = f_{ref} \cdot \left(\frac{3}{4} + \frac{FREQ + 0.5 \cdot DITHER}{32768} \right)$$

in the frequency band 402 – 470 MHz, and

$$f_c = f_{ref} \cdot \left(\frac{3}{2} + \frac{FREQ + 0.5 \cdot DITHER}{16384} \right)$$

in the frequency band 804 – 940 MHz.

The *BANDSELECT* bit in the *ANALOG* register controls the frequency band used. *BANDSELECT* = 0 gives 402 – 470 MHz, and *BANDSELECT* = 1 gives 804 - 940 MHz.

The reference frequency is the crystal oscillator clock frequency divided by *REF_DIV* (3 bits in the *CLOCK_A* or *CLOCK_B* register), a number between 1 and 7:

$$f_{ref} = \frac{f_{xosc}}{REF_DIV + 1}$$

FSK frequency deviation is programmed in the *DEVIATION* register. The deviation programming is divided into a mantissa (*TXDEV_M[3:0]*) and an exponent (*TXDEV_X[2:0]*).

Generally *REF_DIV* should be as low as possible but the following requirements must be met

$$9.8304 \geq f_{ref} > \frac{f_c}{256}[MHz]$$

in the frequency band 402 – 470 MHz, and

$$9.8304 \geq f_{ref} > \frac{f_c}{512}[MHz]$$

in the frequency band 804 – 940 MHz.

The PLL output frequency equation above gives the carrier frequency, f_c , in transmit mode (center frequency). The two FSK modulation frequencies are given by:

$$f_0 = f_c - f_{dev}$$

$$f_1 = f_c + f_{dev}$$

where f_{dev} is set by the *DEVIATION* register:

$$f_{dev} = f_{ref} \cdot TXDEV_M \cdot 2^{(TXDEV_X-16)}$$

in the frequency band 402 - 470 MHz, and

$$f_{dev} = f_{ref} \cdot TXDEV_M \cdot 2^{(TXDEV_X-15)}$$

in the frequency band 804 - 940 MHz.

OOK (On-Off Keying) is used if *TXDEV_M[3:0]* = 0000.

The *TX_SHAPING* bit in the *DEVIATION* register controls Gaussian shaping of the modulation signal.

11.1 Dithering

Spurious signals will occur at certain frequencies depending on the division ratios in the PLL. To reduce the strength of these spurs, a common technique is to use a dithering signal in the control of the frequency dividers. Dithering is activated by setting the *DITHER* bit in the *FREQ_0* registers. It is recommended to use the dithering in order to achieve the best possible performance.

12 Transmitter

12.1 FSK Modulation Formats

The data modulator can modulate FSK, which is a two level FSK (Frequency Shift Keying), or GFSK, which is a Gaussian filtered FSK with BT = 0.5. The purpose of the GFSK is to make a more bandwidth efficient system. The modulation and the Gaussian filtering are done internally in the chip. The *TX_SHAPING* bit in the *DEVIATION* register enables the GFSK. GFSK is recommended for narrowband operation.

12.2 OOK Modulation

The data modulator can also do OOK (On-Off Keying) modulation. OOK is an ASK (Amplitude Shift Keying) modulation using 100% modulation depth.

OOK modulation is enabled by setting *TXDEV_M[3:0]* = 0000 in the *DEVIATION* register.

12.3 Output Power Programming

The RF output power from the device is programmable by the 8-bit *PA_POWER* register. Figure 12 and Figure 13 shows the output power and total current consumption as a function of the *PA_POWER* register setting. It is more efficient in terms of current consumption to use either the lower or upper 4-bits in the register to control the power, as shown in the figures. However, the output power can be controlled in finer steps using all the available bits in the *PA_POWER* register.

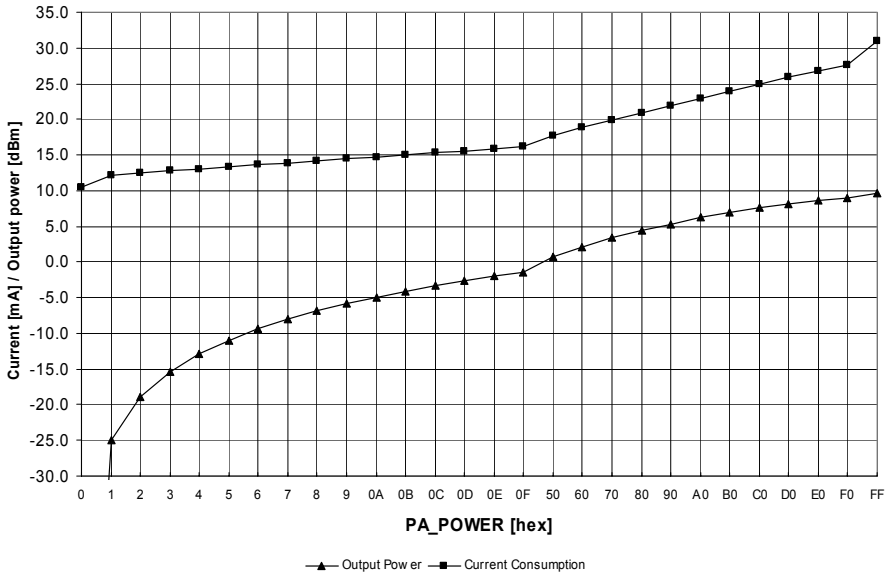


Figure 12. Output power settings and typical current consumption, 433 MHz

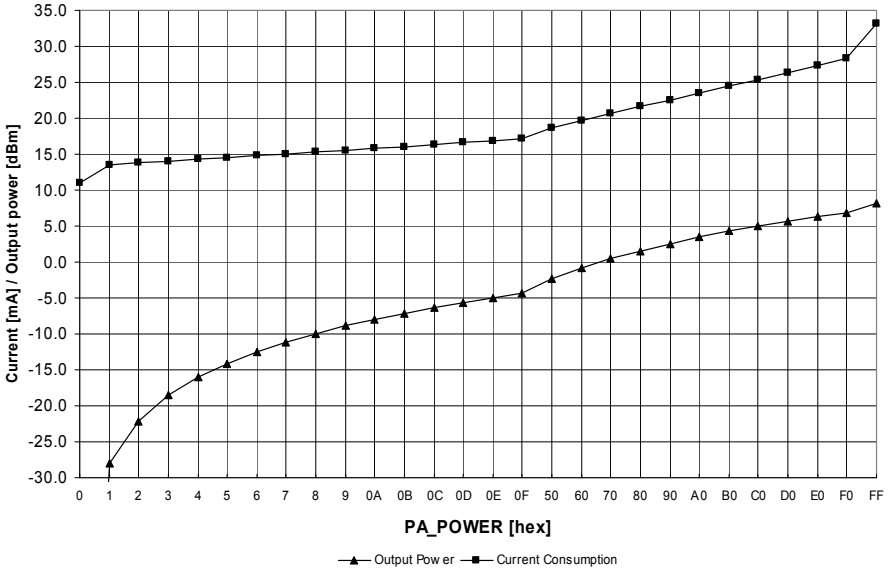


Figure 13. Output power settings and typical current consumption, 868 MHz

12.4 TX Data Latency

The transmitter will add a delay due to the synchronization of the data with DCLK and further clocking into the modulator. The user should therefore add a delay equivalent to at least 2 bits after the data payload has been transmitted before switching off the PA (i.e. before stopping the transmission).

12.5 Reducing Spurious Emission and Modulation Bandwidth

Modulation bandwidth and spurious emission are normally measured with the PA continuously on and a repeated test sequence.

In cases where the modulation bandwidth and spurious emission are measured with the ***CC1070*** switching from power down mode to TX mode, a **PA ramping** sequence could be used to minimize modulation bandwidth and spurious emission.

PA ramping should then be used both when switching the PA on and off. A linear PA ramping sequence can be used where register PA_POWER is changed from 00h to 0Fh and then from 50h to the register setting, which gives the desired output power (e.g. C0h for +5 dBm output power at 868 MHz operation). The longer the time per PA ramping step the better, but setting the total PA ramping time equal to 2 bit periods is a good compromise between performance and PA ramping time.

13 Output Matching and Filtering

When designing the impedance matching network for the ***CC1070*** the circuit must be matched correctly at the harmonic frequencies as well as at the fundamental tone. A recommended matching network is shown in Figure 14. Component values for various frequencies are given in Table 15. Component values for other frequencies can be found using the SmartRF® Studio software.

It is important to remember that the physical layout and the components used contribute significantly to the reflection coefficient, especially at the higher harmonics. For this reason, the frequency response of the matching network should be measured and compared to the response of the TI reference design. Refer to Figure 15 and Table 16 as well as Figure 16 and Table 17.

A recommended application circuit is available from the TI web site (CC1070EM).

Item	433 MHz	868 MHz	915 MHz
C2	2.2 pF, 5%, NP0, 0402	1.5 pF, 5%, NP0, 0402	1.5 pF, 5%, NP0, 0402
C3	5.6 pF, 5%, NP0, 0402	10 pF, 5%, NP0, 0402	10 pF, 5%, NP0, 0402
C60	220 pF, 5%, NP0, 0402	220 pF, 5%, NP0, 0402	220 pF, 5%, NP0, 0402
C71	4.7 pF, 5%, NP0, 0402	3.3 pF, 5%, NP0, 0402	3.3 pF, 5%, NP0, 0402
L2	22 nH, 5%, 0402	6.8 nH, 5%, 0402	6.8 nH, 5%, 0402
L70	47 nH, 5%, 0402	12 nH, 5%, 0402	12 nH, 5%, 0402
L71	47 nH, 5%, 0402	12 nH, 5%, 0402	12 nH, 5%, 0402
R6	82 Ω, 5%, 0402	82 Ω, 5%, 0402	82 Ω, 5%, 0402

Table 15. Component values for the matching network described in Figure 14 (DNM = Do Not Mount).

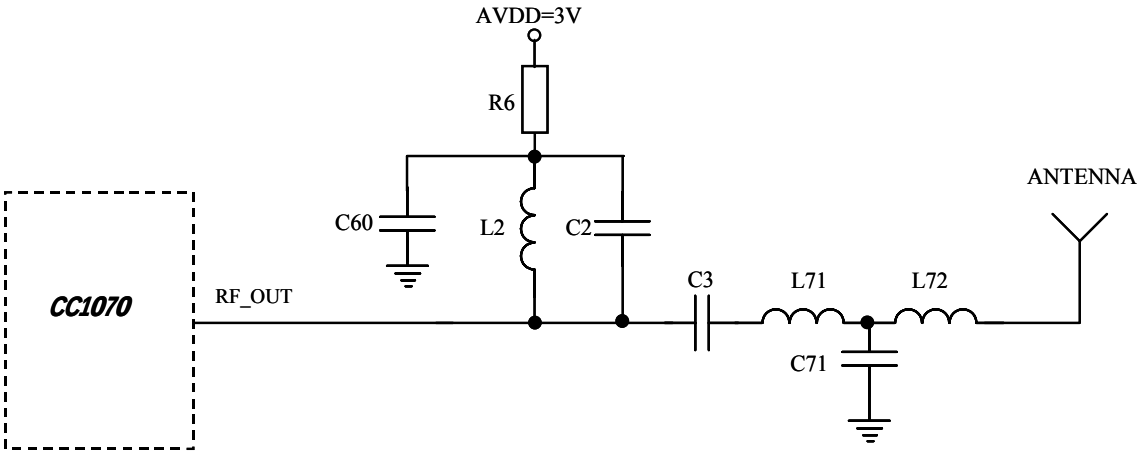


Figure 14. Output matching network

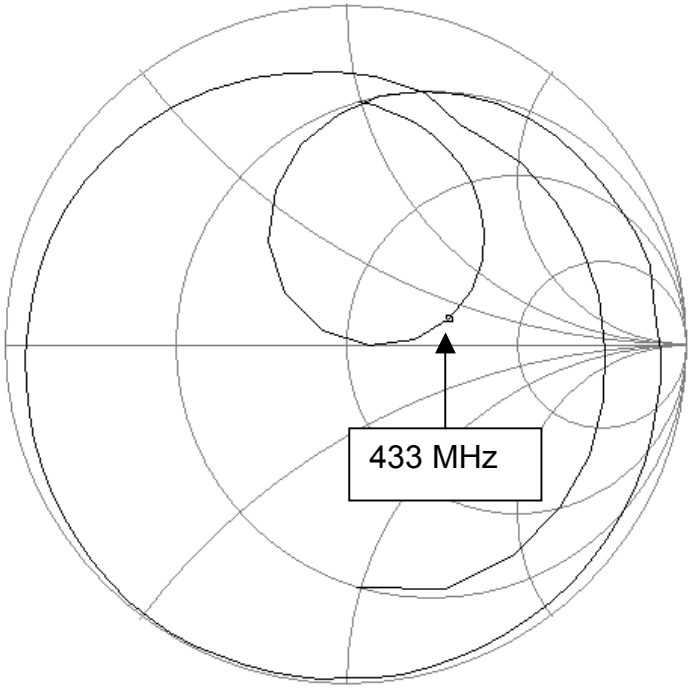


Figure 15. Typical optimum PA load impedance, 433 MHz. The frequency is swept from 300 MHz to 2500 MHz. Values are listed in Table 16

Frequency (MHz)	Real (Ohms)	Imaginary (Ohms)
433	91	16
866	80	-323
1299	1.1	-54
1732	0.4	-23
2165	1.3	-5.3

Table 16. Impedances at the first 5 harmonics (433 MHz matching network)

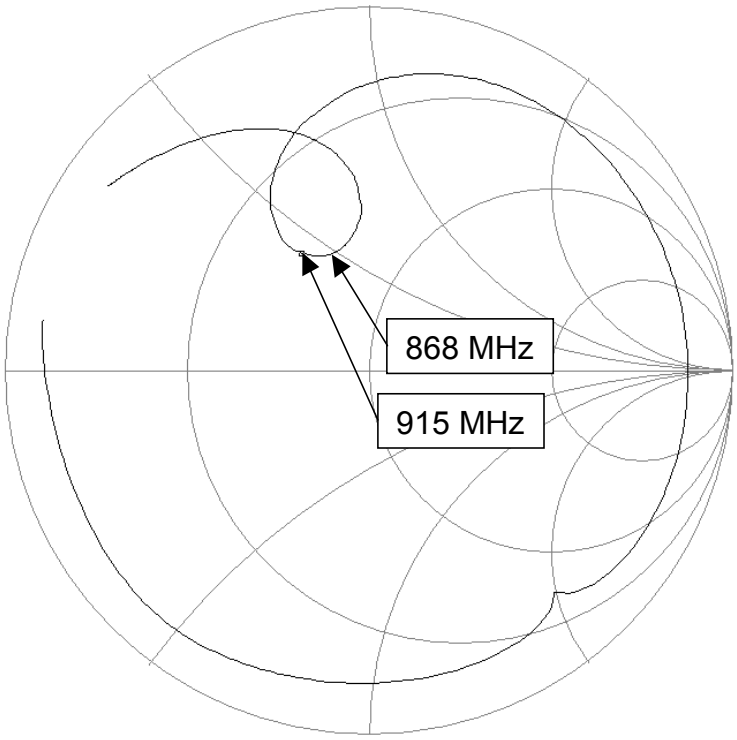


Figure 16. Typical optimum PA load impedance, 868/915 MHz. The frequency is swept from 300 MHz to 2800 MHz. Values are listed in Table 17

Frequency (MHz)	Real (Ohms)	Imaginary (Ohms)
868	34	25
915	28	21
1736	84	-232
1830	31	-130
2604	3.3	-4.7
2745	2.6	2.3

Table 17. Impedances at the first 3 harmonics (868/915 MHz matching network)

14 Frequency Synthesizer

14.1 VCO, Charge Pump and PLL Loop Filter

The VCO is completely integrated and operates in the 1608 – 1880 MHz range. A frequency divider is used to get a frequency in the UHF range (402 – 470 and 804 – 940 MHz). The *BANDSELECT* bit in the *ANALOG* register selects the frequency band.

The VCO frequency is given by:

$$f_{VCO} = f_{ref} \cdot \left(3 + \frac{FREQ + 0.5 \cdot DITHER}{8192}\right)$$

The VCO frequency is divided by 2 and by 4 to generate frequencies in the two bands, respectively.

The VCO sensitivity (sometimes referred to as VCO gain) varies over frequency and operating conditions. Typically the VCO sensitivity varies between 12 and 36 MHz/V. For calculations the geometrical mean at 21 MHz/V can be used. The PLL calibration (explained below) measures the actual VCO sensitivity and adjusts the charge pump current accordingly to achieve correct PLL loop gain and bandwidth (higher charge pump current when VCO sensitivity is lower).

The following equations can be used for calculating PLL loop filter component values, see Figure 3, for a desired PLL loop bandwidth, BW:

C7 = 3037 (f_{ref} / BW^2) –7 [pF]
R2 = 7126 (BW / f_{ref}) [kΩ]
C6 = 80.75 (f_{ref} / BW^2) [nF]
R3 = 21823 (BW / f_{ref}) [kΩ]
C8 = 839 (f_{ref} / BW^2) –6 [pF]

Define a minimum PLL loop bandwidth as $BW_{min} = \sqrt{80.75 \cdot f_{ref} / 220}$. If BW_{min} > Baud rate/3 then set BW = BW_{min} and if BW_{min} < Baud rate/3 then set BW = Baud rate/3 in the above equations.

There are two special cases when using the recommended 14.7456 MHz crystal:

1) If the data rate is 4.8 kBaud or below and the RF operating frequency is in the 402 – 470 MHz frequency range the following loop filter components are recommended:

C6 = 220 nF
C7 = 8200 pF
C8 = 2200 pF
R2 = 1.5 kΩ
R3 = 4.7 kΩ

2) If the data rate is 4.8 kBaud or below and the RF operating frequency is in the 804 – 940 MHz frequency range the following loop filter components are recommended:

C6 = 100 nF
C7 = 3900 pF
C8 = 1000 pF
R2 = 2.2 kΩ
R3 = 6.8 kΩ

After calibration the PLL bandwidth is set by the *PLL_BW* register in combination with the external loop filter components calculated above. The *PLL_BW* can be found from

$$PLL_BW = 146 + 16 \log_2(f_{ref} / 7.126)$$

where f_{ref} is the reference frequency (in MHz). The PLL loop filter bandwidth increases with increasing *PLL_BW* setting.

After calibration the applied charge pump current (*CHP_CURRENT[3:0]*) can be read in the *STATUS1* register. The charge pump current is approximately given by:

$$I_{CHP} = 16 \cdot 2^{CHP_CURRENT\ /\ 4} [uA]$$

The combined charge pump and phase detector gain (in A/rad) is given by the charge pump current divided by 2π.

The PLL bandwidth will limit the maximum modulation frequency and hence data rate.

14.2 VCO and PLL Self-Calibration

To compensate for supply voltage, temperature and process variations, the VCO and PLL must be calibrated. The calibration is performed automatically and sets the maximum VCO tuning range and optimum charge pump current for PLL stability. After setting up the device at the operating frequency, the self-calibration can be initiated by setting the *CAL_START* bit in the *CALIBRATE* register. The calibration result is stored internally in the chip, and is valid as long as power is not turned off. If large supply voltage drops (typically more than 0.25 V) or temperature variations (typically more than 40°C) occur after calibration, a new calibration should be performed.

The nominal VCO control voltage is set by the *CAL_ITERATE[2:0]* bits in the *CALIBRATE* register.

The *CAL_COMPLETE* bit in the *STATUS* register indicates that calibration has finished. The calibration wait time (*CAL_WAIT*) is programmable and is proportional to the internal PLL reference frequency. The highest possible reference frequency should be used to get the minimum calibration time. It is recommended to use *CAL_WAIT[1:0]* = 11 in order to get the most accurate loop bandwidth.

The *CAL_COMPLETE* bit can also be monitored at the LOCK pin, configured by *LOCK_SELECT[3:0]* = 0101, and used as an interrupt input to the microcontroller.

To check that the PLL is in lock the user should monitor the *LOCK_CONTINUOUS* bit in the *STATUS* register. The *LOCK_CONTINUOUS* bit can also be monitored at the LOCK pin, configured by *LOCK_SELECT[3:0]* = 0010.

There are separate calibration values for the two frequency registers. However, dual calibration is possible if all of the below conditions apply:

- The two frequencies A and B differ by less than 1 MHz
- Reference frequencies are equal (*REF_DIV_A[2:0]* = *REF_DIV_B[2:0]* in the *CLOCK_A/CLOCK_B* registers)
- VCO currents are equal (*VCO_CURRENT_A[3:0]* = *VCO_CURRENT_B[3:0]* in the *VCO* register).

The *CAL_DUAL* bit in the *CALIBRATE* register controls dual or separate calibration.

The single calibration algorithm (*CAL_DUAL* = 0) is illustrated in Figure 17. The same algorithm is applicable for dual calibration if *CAL_DUAL* = 1.

TI recommends that single calibration be used for more robust operation.

There is a small, but finite, possibility that the PLL self-calibration will fail. The calibration routine in the source code should include a loop so that the PLL is re-calibrated until PLL lock is achieved if the PLL does not lock the first time. Refer to ***CC1070*** Errata Note 001.

The *CAL_SELECT* bit is used to select the calibration routine. When set high, a fast calibration routine is used.

The table below shows the calibration time when *CAL_SELECT* = 1:

Calibration time [ms]	Reference frequency [MHz]
CAL_WAIT	**7.3728**
00	1.0
01	1.5
10	2.9
11	3.9

Table 18. Typical calibration time when CAL_SELECT = 1

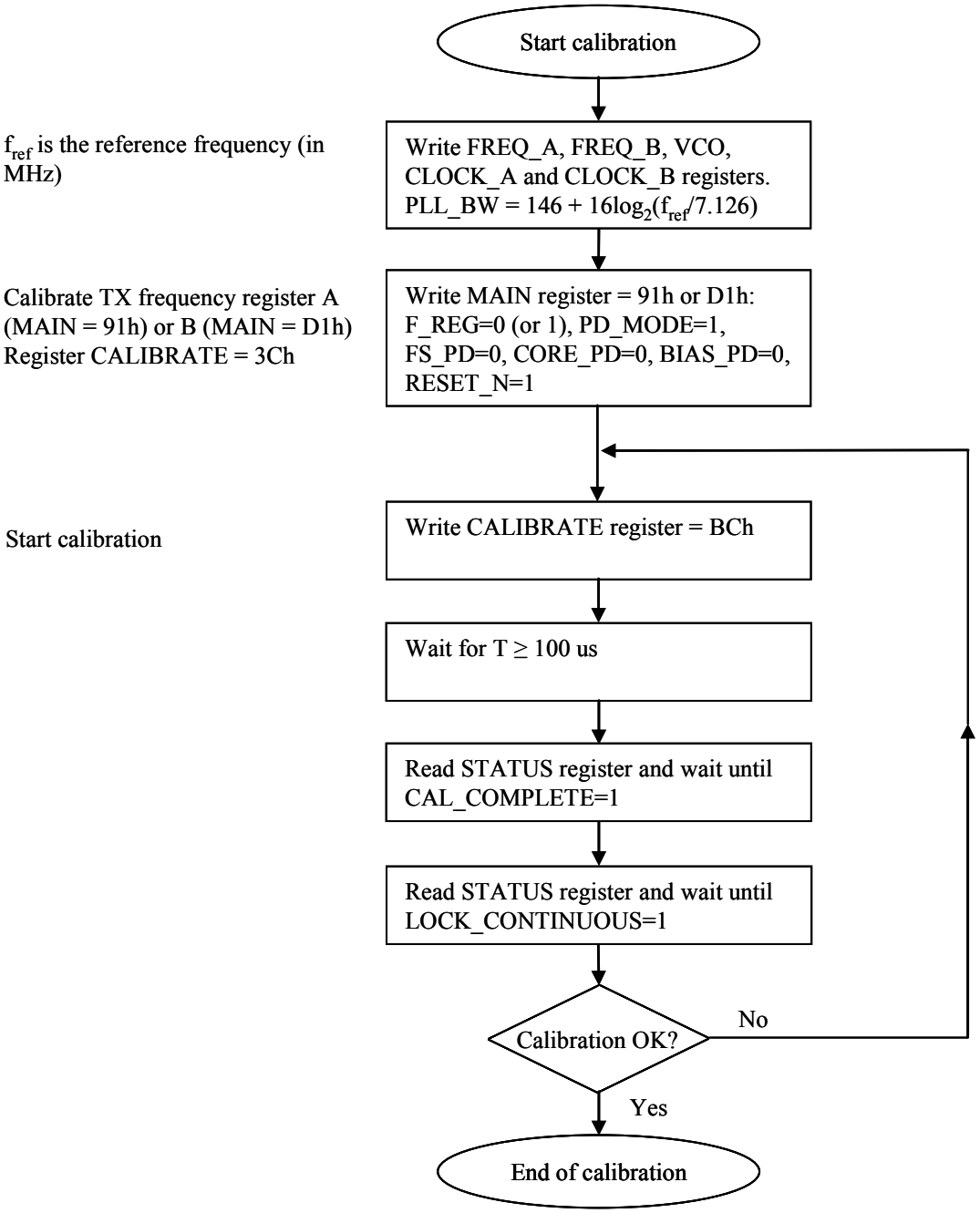


Figure 17. Calibration algorithm

14.3 PLL Turn-on Time versus Loop Filter Bandwidth

If calibration has been performed the PLL turn-on time is the time needed for the PLL to lock to the desired frequency when going from power down mode (with the crystal oscillator running) to TX mode. The PLL turn-on time depends on the PLL loop filter bandwidth. Table 19 gives the PLL turn-on time for different PLL loop filter bandwidths.

C6 [nF]	C7 [pF]	C8 [pF]	R2 [kΩ]	R3 [kΩ]	PLL turn-on time [us]	Comment
220	8200	2200	1.5	4.7	3200	Up to 4.8 kBaud data rate, 12.5 kHz channel spacing
100	3900	1000	2.2	6.8	2500	Up to 4.8 kBaud data rate, 25 kHz channel spacing
56	2200	560	3.3	10	1400	Up to 9.6 kBaud data rate, 50 kHz channel spacing
15	560	150	5.6	18	1300	Up to 19.2 kBaud data rate, 100 kHz channel spacing
3.9	120	33	12	39	1080	Up to 38.4 kBaud data rate, 150 kHz channel spacing
1.0	27	3.3	27	82	950	Up to 76.8 kBaud data rate, 200 kHz channel spacing
0.2	1.5	-	47	150	700	Up to 153.6 kBaud data rate, 500 kHz channel spacing

Table 19. Typical PLL turn-on time to within ±10% of channel spacing for different loop filter bandwidths

14.4 PLL Lock Time versus Loop Filter Bandwidth

If calibration has been performed the PLL lock time is the time needed for the PLL to lock to the desired frequency when going from one transmit frequency to the next by changing the F_REG bit in the *MAIN* register. The PLL lock time depends on the PLL loop filter bandwidth. Table 20 gives the PLL lock time for different PLL loop filter bandwidths.

C6 [nF]	C7 [pF]	C8 [pF]	R2 [kΩ]	R3 [kΩ]	PLL lock time [us]		Comment
					1	2	
220	8200	2200	1.5	4.7	180	1300	Up to 4.8 kBaud data rate, 12.5 kHz channel spacing
100	3900	1000	2.2	6.8	270	830	Up to 4.8 kBaud data rate, 25 kHz channel spacing
56	2200	560	3.3	10	140	490	Up to 9.6 kBaud data rate, 50 kHz channel spacing
15	560	150	5.6	18	70	230	Up to 19.2 kBaud data rate, 100 kHz channel spacing
3.9	120	33	12	39	50	180	Up to 38.4 kBaud data rate, 150 kHz channel spacing
1.0	27	3.3	27	82	15	55	Up to 76.8 kBaud data rate, 200 kHz channel spacing
0.2	1.5	-	47	150	14	28	Up to 153.6 kBaud data rate, 500 kHz channel spacing

Table 20. Typical PLL lock time to within ±10% of channel spacing for different loop filter bandwidths. 1) 1 channel step, 2) 1 MHz step

15 VCO Current Control

The VCO current is programmable and should be set according to operating frequency and output power. Recommended settings for the *VCO_CURRENT* bits in the *VCO* register are shown in the register overview (page 40) and also given by SmartRF® Studio.

The VCO current for frequency *FREQ_A* and *FREQ_B* can be programmed independently.

The bias current for the PA buffers is also programmable. The *BUFF_CURRENT* register controls this current.

16 Power Management

CC1070 offers great flexibility for power management in order to meet strict power consumption requirements in battery-operated applications. Power down mode is controlled through the *MAIN* register. There are separate bits to control the TX part, the frequency synthesizer and the crystal oscillator in the *MAIN* register. This individual control can be used to optimize for lowest possible current consumption in each application. Figure 18 shows a typical power-on and initializing sequences for minimum power consumption.

Figure 19 shows a typical sequence for activating TX mode from power down mode for minimum power consumption.

Note that PSEL should be tri-stated or set to a high level during power down mode in order to prevent a trickle current from flowing in the internal pull-up resistor.

TI recommends resetting the ***CC1070*** (by clearing the *RESET_N* bit in the *MAIN* register) when the chip is powered up initially. All registers that need to be configured should then be programmed (those which differ from their default values). Registers can be programmed freely in any order. The ***CC1070*** should then be calibrated. After this is completed, the ***CC1070*** is ready for use. See the detailed procedure flowcharts in Figure 17 - Figure 19.

Application Note *AN023 CC1020 MCU Interfacing* provides source code for ***CC1020***. This source code can be used as a starting point when writing source code for ***CC1070***.

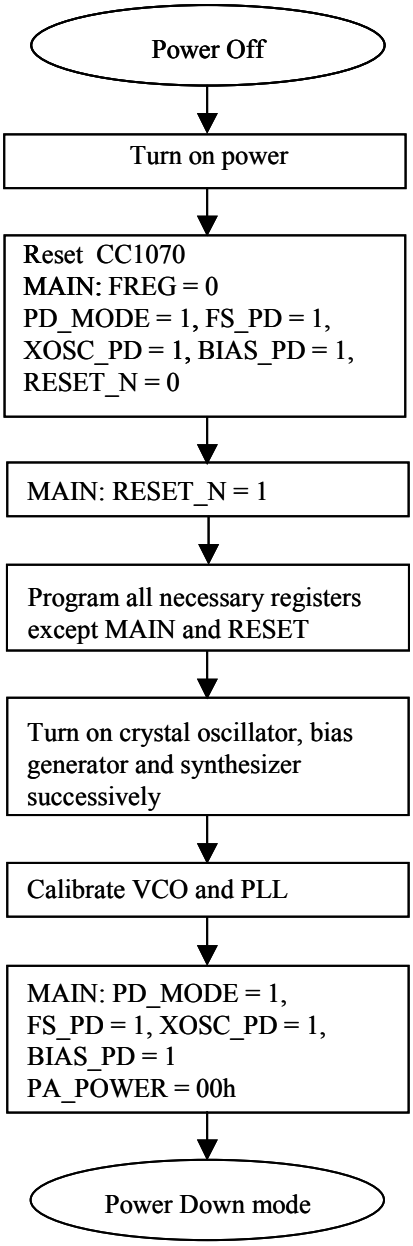


Figure 18. Initializing sequence

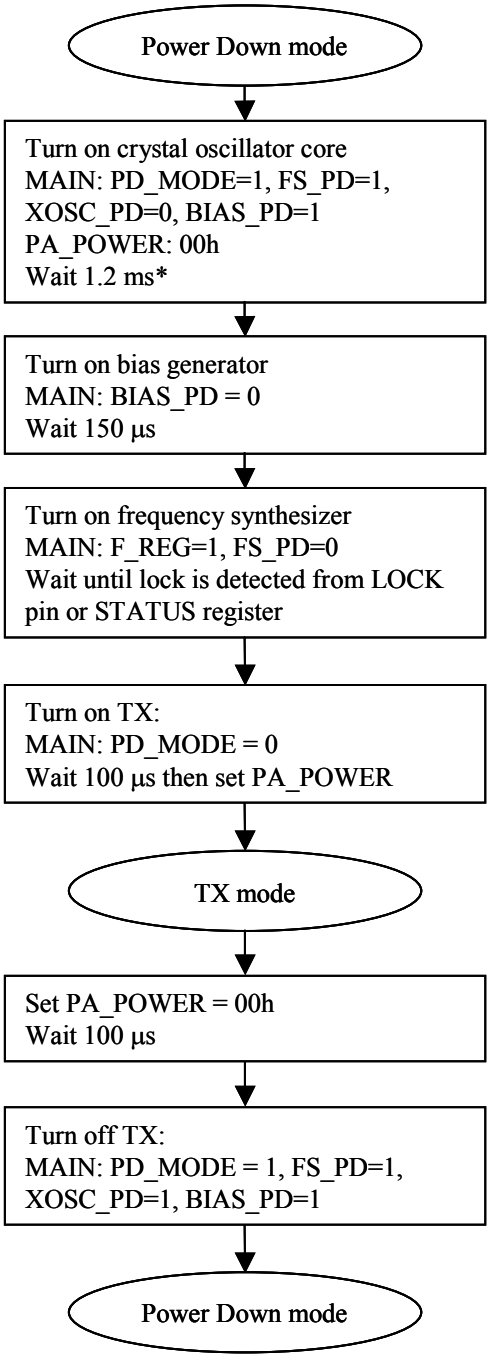


Figure 19. Sequence for activating TX mode

17 Crystal Oscillator

Any crystal frequency in the range 4 - 20 MHz can be used. The crystal frequency is used as reference for the data rate (as well as other internal functions) and in the 4 – 20 MHz range the frequencies 4.9152, 7.3728, 9.8304, 12.2880, 14.7456, 17.2032, 19.6608 MHz will give accurate data rates as shown in Table 14. The crystal frequency will influence the programming of the *CLOCK_A*, *CLOCK_B* and *MODEM* registers.

An external clock signal or the internal crystal oscillator can be used as main frequency reference. An external clock signal should be connected to XOSC_Q1, while XOSC_Q2 should be left open. The *XOSC_BYPASS* bit in the *INTERFACE* register should be set to '1' when an external digital rail-to-rail clock signal is used. No DC block should be used then. A sine with smaller amplitude can also be used. A DC blocking capacitor must then be used (10 nF) and the *XOSC_BYPASS* bit in the *INTERFACE* register should be set to '0'. For input signal amplitude, see section 4.2 on page 8.

Using the internal crystal oscillator, the crystal must be connected between the XOSC_Q1 and XOSC_Q2 pins. The oscillator is designed for parallel mode operation of the crystal. In addition, loading capacitors (C4 and C5) for the crystal are required. The loading capacitor values depend on the total load capacitance, C_L, specified for the crystal. The total load capacitance seen between the crystal terminals should equal C_L for the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C_4} + \frac{1}{C_5}} + C_{parasitic}$$

The parasitic capacitance is constituted by pin input capacitance and PCB stray capacitance. Total parasitic capacitance is typically 8 pF. A trimming capacitor may be placed across C5 for initial tuning if necessary.

The crystal oscillator circuit is shown in Figure 20. Typical component values for different values of C_L are given in Table 21.

The crystal oscillator is amplitude regulated. This means that a high current is required to initiate the oscillations. When the amplitude builds up, the current is reduced to what is necessary to maintain approximately 600 mVpp amplitude. This ensures a fast start-up, keeps the drive level to a minimum and makes the oscillator insensitive to ESR variations. As long as the recommended load capacitance values are used, the ESR is not critical.

The initial tolerance, temperature drift, aging and load pulling should be carefully specified in order to meet the required frequency accuracy in a certain application.

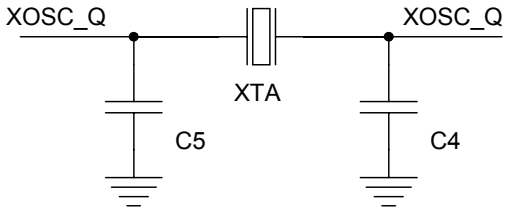


Figure 20. Crystal oscillator circuit

Item	C_L= 12 pF	C_L= 16 pF	C_L= 22 pF
C4	6.8 pF	15 pF	27 pF
C5	6.8 pF	15 pF	27 pF

Table 21. Crystal oscillator component values

18 Built-in Test Pattern Generator

The ***CC1070*** has a built-in test pattern generator that generates a PN9 pseudo random sequence. The *PN9_ENABLE* bit in the *MODEM* register enables the PN9 generator. A transition on the DI pin is required after enabling the PN9 pseudo random sequence.

The PN9 pseudo random sequence is defined by the polynomial $x^9 + x^5 + 1$.

The PN9 generator can be used for transmission of 'real-life' data when measuring narrowband ACP (Adjacent Channel Power), modulation bandwidth or occupied bandwidth.

19 Interrupt upon PLL Lock

In synchronous mode the DCLK pin on ***CC1070*** can be used to give an interrupt signal to wake the microcontroller when the PLL is locked.

PD_MODE[1:0] in the *MAIN* register should be set to 01. If *DCLK_LOCK* in the *INTERFACE* register is set to 1 the DCLK signal is always logic high if the PLL is not in lock. When the PLL locks to the desired frequency the DCLK signal changes to logic 0. When this interrupt has been detected write *PD_MODE[1:0]* = 00. This will enable the DCLK signal.

This function can be used to wait for the PLL to be locked before the PA is ramped up.

20 PA_EN Digital Output Pin

20.1 Interfacing an External PA

CC1070 has a digital output pin, PA_EN, which can be used to control an external PA. The functionality of this pin is controlled through the *INTERFACE* register. The output can also be used as a general digital output control signal.

EXT_PA_POL controls the active polarity of the signal.

EXT_PA controls the function of the pin. If *EXT_PA* = 1, then the PA_EN pin will be activated when the internal PA is turned on. Otherwise, the *EXT_PA_POL* bit controls the PA_EN pin directly.

This pin can therefore also be used as a general control signal, see section 20.2.

20.2 General Purpose Output Control Pins

The digital output pin, PA_EN, can be used as a general control signal by setting *EXT_PA* = 0. The output value is then set directly by the value written to *EXT_PA_POL*.

The LOCK pin can also be used as a general-purpose output pin. The LOCK pin is controlled by *LOCK_SELECT[3:0]* in the *LOCK* register. The LOCK pin is low when *LOCK_SELECT[3:0]* = 0000, and high when *LOCK_SELECT[3:0]* = 0001.

These features can be used to save I/O pins on the microcontroller when the other functions associated with these pins are not used.

20.3 PA_EN Pin Drive

Figure 21 shows the PA_EN pin drive currents. The sink and source currents have opposite signs but absolute values are used in Figure 21.

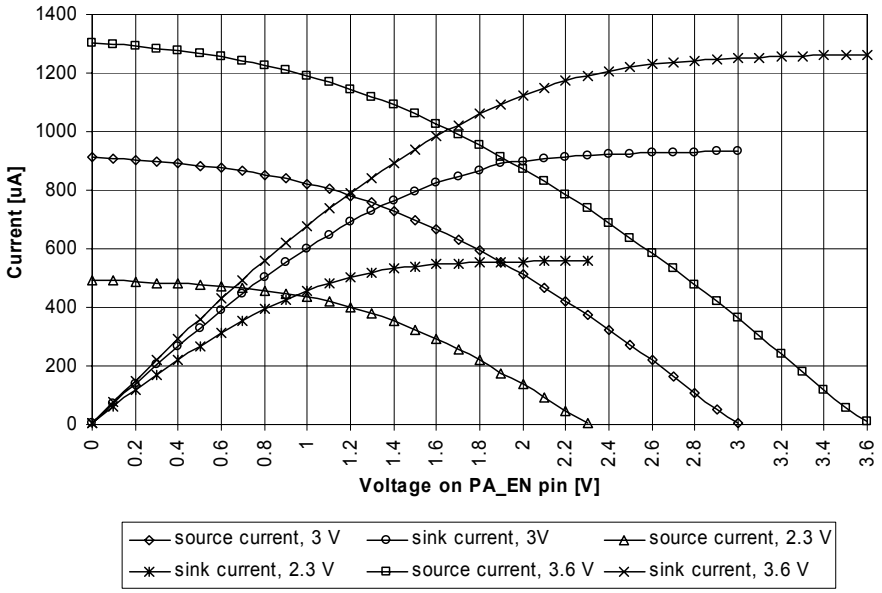


Figure 21. Typical PA_EN pin drive

21 System Considerations and Guidelines

SRD regulations
International regulations and national laws regulate the use of radio receivers and transmitters. SRDs (Short Range Devices) for license free operation are allowed to operate in the 433 and 868 - 870 MHz bands in most European countries. In the United States, such devices operate in the 260 – 470 and 902 - 928 MHz bands. A summary of the most important aspects of these regulations can be found in Application Note *AN001 SRD regulations for license free transceiver operation*, available from the TI web site.

Narrow band systems
CC1070 is specifically designed for narrowband systems complying with ARIB STD T-67 and EN 300 220. The ***CC1070*** meets the strict requirements to ACP (Adjacent Channel Power) and occupied bandwidth for a narrowband transmitter. To meet the ARIB STD T-67 requirements a 3.0 V regulated voltage supply should be used.

Such narrowband performance normally requires the use of external ceramic filters. The ***CC1070*** provides this performance as a true single-chip solution.

Japan and Korea have allocated several frequency bands at 424, 426, 429, 449 and 469 MHz for narrowband license free operation. ***CC1070*** is designed to meet the requirements for operation in all these bands, including the strict requirements for narrowband operation down to 12.5 kHz channel spacing.

A unique feature in ***CC1070*** is the very fine frequency resolution. This can be used for temperature compensation of the crystal if the temperature drift curve is known and a temperature sensor is included in the system. Even initial adjustment can be performed using the frequency programmability. This eliminates the need for an expensive TCXO and trimming in some applications. For more details refer

to Application Note *AN027 Temperature Compensation* available from the TI web site.

In less demanding applications, a crystal with low temperature drift and low aging could be used without further compensation. A trimmer capacitor in the crystal oscillator circuit (in parallel with C5) could be used to set the initial frequency accurately.

CC1070 also has the possibility to use Gaussian shaped FSK (GFSK). This spectrum-shaping feature improves adjacent channel power (ACP) and occupied bandwidth. In 'true' FSK systems with abrupt frequency shifting, the spectrum is inherently broad. By making the frequency shift 'softer', the spectrum can be made significantly narrower. Thus, higher data rates can be transmitted in the same bandwidth using GFSK.

Low cost systems
As the ***CC1070*** provide true narrowband multi-channel performance without any external filters, a very low cost high performance system can be achieved.

The oscillator crystal can then be a low cost crystal with 50 ppm frequency tolerance using the on-chip frequency tuning possibilities.

Battery operated systems
In low power applications the power down mode should be used when ***CC1070*** is not being active. Depending on the start-up time requirement the oscillator core can be powered during power down. See section 16 on page 33 for information on how effective power management can be implemented.

Frequency hopping spread spectrum systems (FHSS)
Due to the very fast locking properties of the PLL, the ***CC1070*** is also very suitable for frequency hopping systems. Hop rates of 1-100 hops/s are commonly used depending on the bit rate and the amount of data to be sent during each transmission. The two frequency registers (*FREQ_A* and *FREQ_B*) are designed such that the 'next' frequency can be programmed while the 'present' frequency is used. The switching between the two frequencies is performed through use of the *MAIN* register. For more details refer to Application Note *AN014 Frequency Hopping Systems* available from the TI web site.

In order to implement a frequency hopping system with ***CC1070*** do the following:

Set the desired frequency, calibrate and store the following register settings in non-volatile memory:

STATUS1[3:0]: CHP_CURRENT[3:0]
STATUS2[4:0]: VCO_ARRAY[4:0]
STATUS3[5:0]:VCO_CAL_CURRENT[5:0]

Repeat the calibration for each desired frequency. *VCO_CAL_CURRENT[5:0]* is not dependent on the RF frequency and the same value can be used for all frequencies.

When performing frequency hopping, write the stored values to the corresponding *TEST1*, *TEST2* and *TEST3* registers, and enable override:

TEST1[3:0]: CHP_CO[3:0]
TEST2[4:0]: VCO_AO[4:0]
TEST2[5]: VCO_OVERRIDE
TEST2[6]: CHP_OVERRIDE
TEST3[5:0]: VCO_CO[5:0]
TEST3[6]: VCO_CAL_OVERRIDE

CHP_CO[3:0] is the register setting read from *CHP_CURRENT[3:0]*, *VCO_AO[4:0]* is the register setting read from *VCO_ARRAY[4:0]* and *VCO_CO[5:0]* is the register setting read from *VCO_CAL_CURRENT[5:0]*.

Assume channel 1 defined by register *FREQ_A* is currently being used and that ***CC1070*** should operate on channel 2 next (to change channel simply write to register *MAIN[6]*). The channel 2 frequency can be set by register *FREQ_B* which can be written to while operating on channel 1. The calibration data must be written to the *TEST1-3* registers after switching to the next frequency. That is, when hopping to a new channel write to register *MAIN[6]* first and the test registers next. The PA should be switched off between each hop and the PLL should be checked for lock before

switching the PA back on after a hop has been performed.

Note that the override bits *VCO_OVERRIDE*, *CHP_OVERRIDE* and *VCO_CAL_OVERRIDE* must be disabled when performing a re-calibration.

22 PCB Layout Recommendations

A two layer PCB with all components placed on the top layer can be used. The bottom layer of the PCB should be the "ground-layer".

The top layer should be used for signal routing, and the open areas should be filled with metallization connected to ground using several vias.

The area under the chip is used for grounding and must be connected to the bottom ground plane with several vias. In the TI reference designs we have placed 8 14 mil (0.36 mm) diameter via holes symmetrically inside the exposed die attached pad. These vias should be "tented" (covered with solder mask) on the component side of the PCB to avoid migration of solder through the vias during the solder reflow process.

Each decoupling capacitor should be placed as close as possible to the supply pin it is supposed to decouple. Each decoupling capacitor should be connected to the power line (or power plane) by separate vias. The best routing is from the power line (or power plane) to the decoupling capacitor and then to the ***CC1070*** supply pin.. Supply power filtering is very important, especially for the VCO supply (pin 15).

Each decoupling capacitor ground pad should be connected to the ground plane using a separate via. Direct connections between neighboring power pins will increase noise coupling and should be avoided unless absolutely necessary.

The external components should ideally be as small as possible and surface mount devices are highly recommended.

Precaution should be used when placing the microcontroller in order to avoid noise interfering with the RF circuitry.

A CC1020/1070DK Development Kit with a fully assembled CC1070EM Evaluation Module is available. It is strongly advised that this reference layout is followed very closely in order to obtain the best performance. The layout Gerber files are available from the TI web site.

23 Antenna Considerations

CC1070 can be used together with various types of antennas. The most common antennas for short-range communication are monopole, helical and loop antennas.

Monopole antennas are resonant antennas with a length corresponding to one quarter of the electrical wavelength ($\lambda/4$). They are very easy to design and can be implemented simply as a "piece of wire" or even integrated onto the PCB.

Non-resonant monopole antennas shorter than $\lambda/4$ can also be used, but at the expense of range. In size and cost critical applications such an antenna may very well be integrated onto the PCB.

Helical antennas can be thought of as a combination of a monopole and a loop antenna. They are a good compromise in size critical applications. But helical antennas tend to be more difficult to optimize than the simple monopole.

Loop antennas are easy to integrate into the PCB, but are less effective due to difficult impedance matching because of their very low radiation resistance.

For low power applications the λ/4-monopole antenna is recommended due to its simplicity as well as providing the best range. The length of the λ/4-monopole antenna is given by:

$$L = 7125 / f$$

where f is in MHz, giving the length in cm. An antenna for 868 MHz should be 8.2 cm, and 16.4 cm for 433 MHz.

The antenna should be connected as close as possible to the IC. If the antenna is located away from the input pin the antenna should be matched to the feeding transmission line (50 Ω).

For a more thorough background on antennas, please refer to Application *Note AN003 SRD Antennas* available from the TI web site.

24 Configuration Registers

The configuration of ***CC1070*** is done by programming the 8-bit configuration registers. The configuration data based on selected system parameters are most easily found by using the SmartRF® Studio software. Complete descriptions of the registers are given in the following tables. After a RESET is programmed, all the registers have default values. The *TEST* registers also get default values after a RESET, and should not be altered by the user.

TI recommends using the register settings found using the SmartRF® Studio software. These are the register settings that TI specifies across temperature, voltage and process. Please check the TI web site for regularly updates to the SmartRF® Studio software.

24.1 CC1070 Register Overview

ADDRESS	Byte Name	Description
00h	MAIN	Main control register
01h	INTERFACE	Interface control register
02h	RESET	Digital module reset register
03h	-	Not used
04h	FREQ_2A	Frequency register 2A
05h	FREQ_1A	Frequency register 1A
06h	FREQ_0A	Frequency register 0A
07h	CLOCK_A	Clock generation register A
08h	FREQ_2B	Frequency register 2B
09h	FREQ_1B	Frequency register 1B
0Ah	FREQ_0B	Frequency register 0B
0Bh	CLOCK_B	Clock generation register B
0Ch	VCO_CUR	VCO current control register
0Dh	MODEM	Modem control register
0Eh	DEVIATION	TX frequency deviation register
0Fh	-	Not used
10h	-	Not used
11h	-	Not used
12h	-	Not used
13h	-	Not used
14h	-	Not used
15h	LOCK	Lock control register
16h	-	Not used
17h	ANALOG	Analog modules control register
18h	BUFF_SWING	LO buffer and prescaler swing control register
19h	BUFF_CURRENT	LO buffer and prescaler bias current control register
1Ah	PLL_BW	PLL loop bandwidth / charge pump current control register
1Bh	CALIBRATE	PLL calibration control register
1Ch	PA_POWER	Power amplifier output power register
1Dh	-	Not used
1Eh	-	Not used
1Fh	-	Not used
20h	POWERDOWN	Power-down control register
21h	TEST1	Test register for overriding PLL calibration
22h	TEST2	Test register for overriding PLL calibration
23h	TEST3	Test register for overriding PLL calibration
24h	TEST4	Test register for charge pump and IF chain testing
25h	TEST5	Test register for ADC testing
26h	-	Not used
27h	-	Not used
28h	TEST_NFC	Test register for calibration
40h	STATUS	Status information register (PLL lock, RSSI, calibration ready, etc.)
41h	RESET_DONE	Status register for digital module reset
42h	-	Not used
43h	-	Not used
44h	-	Not used
45h	STATUS1	Status of PLL calibration results etc. (test only)
46h	STATUS2	Status of PLL calibration results etc. (test only)
47h	STATUS3	Status of PLL calibration results etc. (test only)
48h	-	Not used
49h	-	Not used
4Ah	-	Not used
4Bh	-	Not used

MAIN Register (00h)

REGISTER	NAME	Default value	Active	Description
MAIN[7]	-	1	-	reserved
MAIN[6]	F_REG	-	-	Selection of Frequency Register, 0: Register A, 1: Register B
MAIN[5:4]	PD_MODE[1:0]	-	-	Power down mode 0 (00): Normal operation 1 (01): PA in power-down. 2 (10): Individual modules can be put in power-down by programming the POWERDOWN register 3 (11): reserved
MAIN[3]	FS_PD	-	H	Power Down of Frequency Synthesizer
MAIN[2]	XOSC_PD	-	H	Power Down of Crystal Oscillator Core
MAIN[1]	BIAS_PD	-	H	Power Down of BIAS (Global Current Generator) and Crystal Oscillator Buffer
MAIN[0]	RESET_N	-	L	Reset, active low. Writing RESET_N low will write default values to all other registers than MAIN. Bits in MAIN do not have a default value and will be written directly through the configuration interface. Must be set high to complete reset.

INTERFACE Register (01h)

REGISTER	NAME	Default value	Active	Description
INTERFACE[7]	XOSC_BYPASS	0	H	Bypass internal crystal oscillator, use external clock 0: Internal crystal oscillator is used, or external sine wave fed through a coupling capacitor 1: Internal crystal oscillator in power down, external clock with rail-to-rail swing is used
INTERFACE[6]	-			reserved
INTERFACE[5]	DCLK_LOCK	0	H	Gate DCLK signal with PLL lock signal in synchronous mode Only applies when PD_MODE = “01” 0: DCLK is always 1 1: DCLK is always 1 unless PLL is in lock
INTERFACE[4]	-			reserved
INTERFACE[3]	EXT_PA	0	H	Use PA_EN pin to control external PA 0: PA_EN pin always equals EXT_PA_POL bit 1: PA_EN pin is asserted when internal PA is turned on
INTERFACE[2]	-			reserved
INTERFACE[1]	EXT_PA_POL	0	H	Polarity of external PA control 0: PA_EN pin is “0” when activating external PA 1: PA_EN pin is “1” when activating external PA
INTERFACE[0]	-			reserved

RESET Register (02h)

REGISTER	NAME	Default value	Active	Description
RESET[7]	-			reserved
RESET[6]	-			reserved
RESET[5]	GAUSS_RESET_N	0	L	Reset Gaussian data filter
RESET[4]				reserved
RESET[3]	PN9_RESET_N	0	L	Reset modulator and PN9 PRBS generator
RESET[2]	SYNTH_RESET_N	0	L	Reset digital part of frequency synthesizer
RESET[1]	-			reserved
RESET[0]	CAL_LOCK_RESET_N	0	L	Reset calibration logic and lock detector

Note: For reset of CC1070 write RESET_N=0 in the MAIN register. The RESET register should not be used during normal operation

Bits in the RESET register are self-clearing (will be set to 1 when the reset operation starts). Relevant digital clocks must be running for the resetting to complete. After writing to the RESET register, the user should verify that all reset operations have been completed, by reading the RESET_DONE status register (41h) until all bits equal 1.

FREQ_2A Register (04h)

REGISTER	NAME	Default value	Active	Description
FREQ_2A[7:0]	FREQ_A[22:15]	131	-	8 MSB of frequency control word A

FREQ_1A Register (05h)

REGISTER	NAME	Default value	Active	Description
FREQ_1A[7:0]	FREQ_A[14:7]	177	-	Bit 15 to 8 of frequency control word A

FREQ_0A Register (06h)

REGISTER	NAME	Default value	Active	Description
FREQ_0A[7:1]	FREQ_A[6:0]	124	-	7 LSB of frequency control word A
FREQ_0A[0]	DITHER_A	1	H	Enable dithering for frequency A

CLOCK_A Register (07h)

REGISTER	NAME	Default value	Active	Description
CLOCK_A[7:5]	REF_DIV_A[2:0]	2	-	Reference frequency divisor (A): 0: Not supported 1: REF_CLK frequency = Crystal frequency / 2 … 7: REF_CLK frequency = Crystal frequency / 8 It is recommended to use the highest possible reference clock frequency that allows the desired Baud rate.
CLOCK_A[4:2]	MCLK_DIV1_A[2:0]	4	-	Modem clock divider 1 (A): 0: Divide by 2.5 1: Divide by 3 2: Divide by 4 3: Divide by 7.5 (2.5·3) 4: Divide by 12.5 (2.5·5) 5: Divide by 40 (2.5·16) 6: Divide by 48 (3·16) 7: Divide by 64 (4·16)
CLOCK_A[1:0]	MCLK_DIV2_A[1:0]	0	-	Modem clock divider 2 (A): 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 MODEM_CLK frequency is FREF frequency divided by the product of divider 1 and divider 2. Baud rate is MODEM_CLK frequency divided by 8.

FREQ_2B Register (08h)

REGISTER	NAME	Default value	Active	Description
FREQ_2B[7:0]	FREQ_B[22:15]	131	-	8 MSB of frequency control word B

FREQ_1B Register (09h)

REGISTER	NAME	Default value	Active	Description
FREQ_1B[7:0]	FREQ_B[14:7]	189	-	Bit 15 to 8 of frequency control word B

FREQ_0B Register (0Ah)

REGISTER	NAME	Default value	Active	Description
FREQ_0B[7:1]	FREQ_B[6:0]	124	-	7 LSB of frequency control word B
FREQ_0B[0]	DITHER_B	1	H	Enable dithering for frequency B

CLOCK_B Register (0Bh)

REGISTER	NAME	Default value	Active	Description
CLOCK_B[7:5]	REF_DIV_B[2:0]	2	-	Reference frequency divisor (B): 0: Not supported 1: REF_CLK frequency = Crystal frequency / 2 … 7: REF_CLK frequency = Crystal frequency / 8
CLOCK_B[4:2]	MCLK_DIV1_B[2:0]	4	-	Modem clock divider 1 (B): 0: Divide by 2.5 1: Divide by 3 2: Divide by 4 3: Divide by 7.5 (2.5·3) 4: Divide by 12.5 (2.5·5) 5: Divide by 40 (2.5·16) 6: Divide by 48 (3·16) 7: Divide by 64 (4·16)
CLOCK_B[1:0]	MCLK_DIV2_B[1:0]	0	-	Modem clock divider 2 (B): 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 MODEM_CLK frequency is FREF frequency divided by the product of divider 1 and divider 2. Baud rate is MODEM_CLK frequency divided by 8.

VCO Register (0Ch)

REGISTER	NAME	Default value	Active	Description
VCO[7:4]	VCO_CURRENT_A[3:0]	8	-	Control of current in VCO core for frequency A 0: 1.4 mA current in VCO core 1: 1.8 mA current in VCO core 2: 2.1 mA current in VCO core 3: 2.5 mA current in VCO core 4: 2.8 mA current in VCO core 5: 3.2 mA current in VCO core 6: 3.5 mA current in VCO core 7: 3.9 mA current in VCO core 8: 4.2 mA current in VCO core 9: 4.6 mA current in VCO core 10: 4.9 mA current in VCO core 11: 5.3 mA current in VCO core 12: 5.6 mA current in VCO core 13: 6.0 mA current in VCO core 14: 6.4 mA current in VCO core 15: 6.7 mA current in VCO core Recommended setting: VCO_CURRENT_A=4
VCO[3:0]	VCO_CURRENT_B[3:0]	8	-	Control of current in VCO core for frequency B The current steps are the same as for *VCO_CURRENT_A* Recommended setting: VCO_CURRENT_B=4

MODEM Register (0Dh)

REGISTER	NAME	Default value	Active	Description
MODEM[7]	-	0	-	Reserved, write 0 (spare register)
MODEM[6:4]	-		-	Reserved
MODEM[3]	-	0	-	Reserved, write 0 (spare register)
MODEM[2]	PN9_ENABLE	0	H	Enable scrambling with PN9 pseudo-random bit sequence 0: PN9 scrambling is disabled 1: PN9 scrambling is enabled (x^9+x^5+1)
MODEM[1:0]	DATA_FORMAT[1:0]	0	-	Modem data format 0 (00): NRZ operation 1 (01): Manchester operation 2 (10): Transparent asynchronous UART operation, set DCLK=0 3 (11): Transparent asynchronous UART operation, set DCLK=1

DEVIATION Register (0Eh)

REGISTER	NAME	Default value	Active	Description
DEVIATION[7]	TX_SHAPING	1	H	Enable Gaussian shaping of transmitted data Recommended setting: TX_SHAPING=1
DEVIATION[6:4]	TXDEV_X[2:0]	6	-	Transmit frequency deviation exponent
DEVIATION [3:0]	TXDEV_M[3:0]	8	-	Transmit frequency deviation mantissa Deviation in 402-470 MHz band: $F_{REF} \cdot TXDEV_M \cdot 2^{(TXDEV_X-16)}$ Deviation in 804-940 MHz band: $F_{REF} \cdot TXDEV_M \cdot 2^{(TXDEV_X-15)}$ On-off-keying (OOK) is used in RX/TX if TXDEV_M[3:0]=0 To find TXDEV_M given the deviation and TXDEV_X: $TXDEV_M = deviation \cdot 2^{(16-TXDEV_X)}/F_{REF}$ in 402-470 MHz band. $TXDEV_M = deviation \cdot 2^{(15-TXDEV_X)}/F_{REF}$ in 804-940 MHz band. Decrease TXDEV_X and try again if TXDEV_M<8. Increase TXDEV_X and try again if TXDEV_M≥16.

LOCK Register (15h)

REGISTER	NAME	Default value	Active	Description
LOCK[7:4]	LOCK_SELECT[3:0]	0	-	Selection of signals to LOCK pin 0: Set to 0 1: Set to 1 2: LOCK_CONTINUOUS (active low) 3: LOCK_INSTANT (active low) 4: Set to 0 5: CAL_COMPLETE (active low) 6: Set to 0 7: FXOSC 8: REF_CLK 9: Set to 0 10: Set to 0 11: PRE_CLK 12: DS_CLK 13: MODEM_CLK 14: VCO_CAL_COMP 15: F_COMP
LOCK[3]	WINDOW_WIDTH	0	-	Selects lock window width 0: Lock window is 2 prescaler clock cycles wide 1: Lock window is 4 prescaler clock cycles wide Recommended setting: WINDOW_WIDTH=0.
LOCK[2]	LOCK_MODE	0	-	Selects lock detector mode 0: Counter restart mode 1: Up/Down counter mode Recommended setting: LOCK_MODE=0.
LOCK[1:0]	LOCK_ACCURACY[1:0]	0	-	Selects lock accuracy (counter threshold values) 0: Declare lock at counter value 127, out of lock at value 111 1: Declare lock at counter value 255, out of lock at value 239 2: Declare lock at counter value 511, out of lock at value 495 3: Declare lock at counter value 1023, out of lock at value 1007

Note: Set LOCK_SELECT=2 to use the LOCK pin as a lock indicator.

ANALOG Register (17h)

REGISTER	NAME	Default value	Active	Description
ANALOG[7]	BANDSELECT	1	-	Frequency band selection 0: 402-470 MHz band 1: 804-940 MHz band
ANALOG[6]	-			reserved
ANALOG[5]	-			reserved
ANALOG[4]	PD_LONG	0	H	Selects short or long reset delay in phase detector 0: Short reset delay 1: Long reset delay Recommended setting: PD_LONG=0.
ANALOG[3]	-	0	-	Reserved, write 0 (spare register)
ANALOG[2]	PA_BOOST	0	H	Boost PA bias current for higher output power Recommended setting: PA_BOOST=1.
ANALOG[1:0]	DIV_BUFF_CURRENT[1:0]	3	-	Overall bias current adjustment for VCO divider and buffers 0: 4/6 of nominal VCO divider and buffer current 1: 4/5 of nominal VCO divider and buffer current 2: Nominal VCO divider and buffer current 3: 4/3 of nominal VCO divider and buffer current Recommended settings: DIV_BUFF_CURRENT=3

BUFF_SWING Register (18h)

REGISTER	NAME	Default value	Active	Description
BUFF_SWING[7:6]	PRE_SWING[1:0]	3	-	Prescaler swing. Fractions for *PRE_CURRENT*=0: 0: 2/3 of nominal swing 1: 1/2 of nominal swing 2: 4/3 of nominal swing 3: Nominal swing Recommended setting: PRE_SWING=0.
BUFF_SWING[5:3]	-			reserved
BUFF_SWING[2:0]	TX_SWING[2:0]	1	-	LO buffer swing, in TX (to power amplifier driver) 0: Smallest load resistance (smallest swing) … 7: Largest load resistance (largest swing) Recommended settings: TX_SWING=4 for 402-470 MHz TX_SWING=0 for 804-940 MHz.

BUFF_CURRENT Register (19h)

REGISTER	NAME	Default value	Active	Description
BUFF_CURRENT[7:6]	PRE_CURRENT[1:0]	1	-	Prescaler current scaling 0: Nominal current 1: 2/3 of nominal current 2: 1/2 of nominal current 3: 2/5 of nominal current Recommended setting: PRE_CURRENT=0.
BUFF_CURRENT[5:3]	-			reserved
BUFF_CURRENT[2:0]	TX_CURRENT[2:0]	5	-	LO buffer current, in TX (to PA driver) 0: Minimum buffer current … 7: Maximum buffer current Recommended settings: TX_CURRENT=2 for 402-470 MHz TX_CURRENT=4 for 804-940 MHz.

PLL_BW Register (1Ah)

REGISTER	NAME	Default value	Active	Description
PLL_BW[7:0]	PLL_BW[7:0]	134	-	Charge pump current scaling/rounding factor. Used to calibrate charge pump current for the desired PLL loop bandwidth. The value is given by: PLL_BW = 146 + 16 $\log_2(f_{ref}/7.126)$ where f_{ref} is the reference frequency in MHz.

CALIBRATE Register (1Bh)

REGISTER	NAME	Default value	Active	Description
CALIBRATE[7]	CAL_START	0	↑	↑ 1: Calibration started 0: Calibration inactive
CALIBRATE[6]	CAL_DUAL	0	H	Use calibration results for both frequency A and B 0: Store results in A or B defined by F_REG (MAIN[6]) 1: Store calibration results in both A and B
CALIBRATE[5:4]	CAL_WAIT[1:0]	0	-	Selects dividers for clock used during calibration, and thereby calibration wait time. Encoding when CAL_SELECT = 1: 0 – divider 8 1 – divider 16 2 – divider 40 3 – divider 80 Encoding when CAL_SELECT = 0: 0 – divider 80 1 – divider 128 2 – divider 160 3 – divider 256 For CAL_SELECT = 0 this leads to: 0: Calibration time is approx. 90000 F_REF periods 1: Calibration time is approx. 110000 F_REF periods 2: Calibration time is approx. 130000 F_REF periods 3: Calibration time is approx. 200000 F_REF periods Recommended setting: CAL_WAIT=3 for best accuracy in calibrated PLL loop filter bandwidth.
CALIBRATE[3]	CAL_SELECT	1	-	Selects calibration routine 0: CC1020 style calibration 1: New calibration routine (default) Recommended setting: CAL_SELECT=1.
CALIBRATE[2:0]	CAL_ITERATE[2:0]	5	-	Iteration start value for calibration DAC 0 (000): DAC start value 1, VC<0.49V after calibration 1 (001): DAC start value 2, VC<0.66V after calibration 2 (010): DAC start value 3, VC<0.82V after calibration 3 (011): DAC start value 4, VC<0.99V after calibration 4 (100): DAC start value 5, VC<1.15V after calibration 5 (101): DAC start value 6, VC<1.32V after calibration 6 (110): DAC start value 7, VC<1.48V after calibration 7 (111): DAC start value 8, VC<1.65V after calibration Recommended setting: CAL_ITERATE=4.

PA_POWER Register (1Ch)

REGISTER	NAME	Default value	Active	Description
PA_POWER[7:4]	PA_HIGH [3:0]	0	-	Controls output power in high-power array 0: High-power array is off 1: Minimum high-power array output power … 15: Maximum high-power array output power
PA_POWER[3:0]	PA_LOW[3:0]	15	-	Controls output power in low-power array 0: Low-power array is off 1: Minimum low-power array output power … 15: Maximum low-power array output power It is more efficient in terms of current consumption to use either the lower or upper 4-bits in the PA_POWER register to control the power.

POWERDOWN Register (20h)

REGISTER	NAME	Default value	Active	Description
POWERDOWN[7]	PA_PD	0	H	Sets PA in power-down when *PD_MODE[1:0]*=2
POWERDOWN[6]	VCO_PD	0	H	Sets VCO in power-down when *PD_MODE[1:0]*=2
POWERDOWN[5]	BUFF_PD	0	H	Sets VCO divider, LO buffers and prescaler in power-down when *PD_MODE[1:0]*=2
POWERDOWN[4]	CHP_PD	0	H	Sets charge pump in power-down when *PD_MODE[1:0]*=2
POWERDOWN[3]	-			reserved
POWERDOWN[2]	-			reserved
POWERDOWN[1]	-			reserved
POWERDOWN[0]	-			reserved

TEST1 Register (21h, for test only)

REGISTER	NAME	Default value	Active	Description
TEST1[7:4]	CAL_DAC_OPEN[3:0]	4	-	Calibration DAC override value, active when BREAK_LOOP=1
TEST1[3:0]	CHP_CO[3:0]	13	-	Charge pump current override value

TEST2 Register (22h, for test only)

REGISTER	NAME	Default value	Active	Description
TEST2[7]	BREAK_LOOP	0	H	0: PLL loop closed 1: PLL loop open
TEST2[6]	CHP_OVERRIDE	0	H	0: use calibrated value 1: use CHP_CO[3:0] value
TEST2[5]	VCO_OVERRIDE	0	H	0: use calibrated value 1: use VCO_AO[4:0] value
TEST2[4:0]	VCO_AO[4:0]	16	-	VCO_ARRAY override value

TEST3 Register (23h, for test only)

REGISTER	NAME	Default value	Active	Description
TEST3[7]	VCO_CAL_MANUAL	0	H	Enables “manual” VCO calibration (test only)
TEST3[6]	VCO_CAL_OVERRIDE	0	H	Override VCO current calibration 0: Use calibrated value 1: Use VCO_CO[5:0] value VCO_CAL_OVERRIDE controls VCO_CAL_CLK if VCO_CAL_MANUAL=1. Negative transitions are then used to sample VCO_CAL_COMP.
TEST3[5:0]	VCO_CO[5:0]	6	-	VCO_CAL_CURRENT override value

TEST4 Register (24h, for test only)

REGISTER	NAME	Default value	Active	Description
TEST4[7]	CHP_DISABLE	0	H	Disable normal charge pump operation
TEST4[6]	CHP_TEST_UP	0	H	Force charge pump to output “up” current
TEST4[5]	CHP_TEST_DN	0	H	Force charge pump to output “down” current
TEST4[4:3]	-			reserved
TEST4[2]	-			reserved
TEST4[1]	-			reserved
TEST4[0]	-			reserved

TEST5 Register (25h, for test only)

REGISTER	NAME	Default value	Active	Description
TEST5[7]	F_COMP_ENABLE	0	H	Enable frequency comparator output F_COMP from phase detector
TEST5[6]	SET_DITHER_CLOCK	1	H	Enable dithering of delta-sigma clock
TEST5[5]	-			reserved
TEST5[4]	-			reserved
TEST5[3]	-			reserved
TEST5[2]	-			reserved
TEST5[1:0]	-			reserved

TEST_NFC Register (28h, for test only)

REGISTER	NAME	Default value	Active	Description
TEST_NFC[7:6]	CAL_WTIME_2	0	-	Wait time vcdac, vco_array, chp_current calibrations. Encoding: 0 – 1 clock cycle 1 – 2 clock cycles 2 – 6 clock cycles 3 – 50 clock cycles
TEST_NFC[5:4]	CAL_WTIME_1	1	-	Wait time vco_cal_current calibration. Encoding: 0 – 1 clock cycle 1 – 12 clock cycles 2 – 63 clock cycles 3 – 127 clock cycles
TEST_NFC[3:0]	CAL_DEC_LIMIT	5	-	Calibration decision limit in new frequency comparator

STATUS Register (40h, read only)

REGISTER	NAME	Default value	Active	Description
STATUS[7]	CAL_COMPLETE	-	H	Set to 0 when PLL calibration starts, and set to 1 when calibration has finished
STATUS[6]	-	-		reserved
STATUS[5]	LOCK_INSTANT	-	H	Instantaneous PLL lock indicator
STATUS[4]	LOCK_CONTINUOUS	-	H	PLL lock indicator, as defined by LOCK_ACCURACY. Set to 1 when PLL is in lock
STATUS[3]	-			reserved
STATUS[2]	LOCK	-	H	Logical level on LOCK pin
STATUS[1]	DCLK	-	H	Logical level on DCLK pin
STATUS[0]	DIO	-	H	Logical level on DIO pin

RESET_DONE Register (41h, read only, test only)

REGISTER	NAME	Default value	Active	Description
RESET_DONE[7]	-			reserved
RESET_DONE[6]	-			reserved
RESET_DONE[5]	GAUSS_RESET_DONE	-	H	Reset of Gaussian data filter done
RESET_DONE[4]	-			reserved
RESET_DONE[3]	PN9_RESET_DONE	-	H	Reset of PN9 PRBS generator
RESET_DONE[2]	SYNTH_RESET_DONE	-	H	Reset digital part of frequency synthesizer done
RESET_DONE[1]	-			reserved
RESET_DONE[0]	CAL_LOCK_RESET_DONE	-	H	Reset of calibration logic and lock detector done

STATUS1 Register (45h, for test only)

REGISTER	NAME	Default value	Active	Description
STATUS1[7:4]	CAL_DAC[3:0]	-	-	Status vector defining applied Calibration DAC value
STATUS1[3:0]	CHP_CURRENT[3:0]	-	-	Status vector defining applied CHP_CURRENT value

STATUS2 Register (46h, for test only)

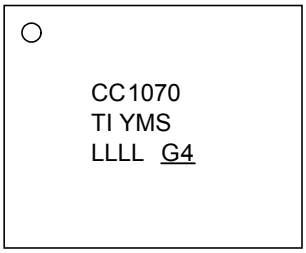
REGISTER	NAME	Default value	Active	Description
STATUS2[7:5]	CC1070_VERSION[2:0]	-	-	CC1070 version code: 0: Pre-production version 1: First production version 2-7: Reserved for future use
STATUS2[4:0]	VCO_ARRAY[4:0]	-	-	Status vector defining applied VCO_ARRAY value

STATUS3 Register (47h, for test only)

REGISTER	NAME	Default value	Active	Description
STATUS3[7]	F_COMP	-	-	Frequency comparator output from phase detector
STATUS3[6]	VCO_CAL_COMP	-	-	Readout of VCO current calibration comparator Equals 1 if current defined by VCO_CURRENT_A/B is larger than the VCO core current
STATUS3[5:0]	VCO_CAL_CURRENT[5:0]	-	-	Status vector defining applied VCO_CAL_CURRENT value

25 Package Marking

When contacting technical support with a chip-related question, please state the entire marking information as stated below (this is for RGW package).



o – pin one symbolization
TI – TI letters
YM – Year Month Date Code
SLLLL – Assembly Lot Code
G4 – fixed code

25.1 Soldering Information

The recommendation for lead-free reflow in IPC/JEDEC J-STD-020 should be followed.

25.2 Tray Specification

QFN 5x5 mm standard shipping tray.

Tray Specification				
Package	Tray Width	Tray Height	Tray Length	Units per Tray
QFN 20 (RSQ)	135.9 mm	7.62 mm	315 mm	490

25.3 Carrier Tape and Reel Specification

Carrier tape and reel is in accordance with EIA Specification 481.

Tape and Reel Specification					
Package	Tape Width	Component Pitch	Hole Pitch	Reel Diameter	Units per Reel
QFN 20 (RSQR)	12 mm	8 mm	4 mm	13”	5000

26 Ordering Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead Finish	MSL Peak Temp (3)
CC1070RSQ	NRND	QFN	RSQ	20	490	Green (RoHS & no Sb/Br)	Matte Tin	LEVEL3-260C 1 YEAR
CC1070RSQR	NRND	QFN	RSQ	20	5000	Green (RoHS & no Sb/Br)	Matte Tin	LEVEL3-260C 1 YEAR
CC1070RGWT	Active	QFN	RGW	20	250	Green (RoHS & no Sb/Br)	Cu NiPdAu	LEVEL3-260C 1 YEAR
CC1070RGWR	Active	QFN	RGW	20	3000	Green (RoHS & no Sb/Br)	Cu NiPdAu	LEVEL3-260C 1 YEAR

Orderable Evaluation Module	Description	Minimum Order Quantity
CC1020_1070DK-433	CC1020/1070 Development Kit, 433 MHz	1
CC1020_1070DK-868/915	CC1020/1070 Development Kit, 868/915 MHz	1

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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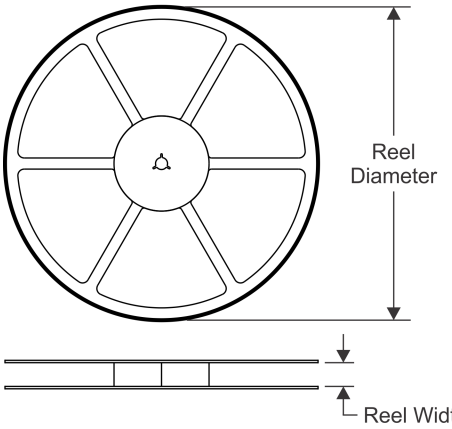
27 General Information

Document Revision History

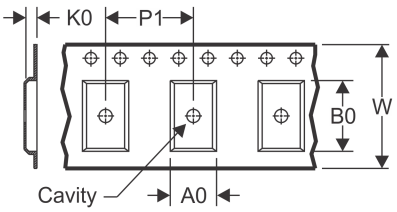
Revision	Date	Description/Changes
1.0	2003-10-30	Initial release.
1.1	2005-02-09	The various sections have been reorganized to improve readability Added chapter numbering Reorganized electrical specification section Electrical specifications updated Changed “channel width” to “channel spacing” Changes to current consumption figures in TX mode and crystal oscillator, bias and synthesizer mode Included data on PA_EN pin drive Included data on PLL lock time Included data on PLL turn-on time Updates to section on output power programming Updates to section on output matching Updates to section on VCO and PLL self-calibration Updates to section on VCO, charge pump and PLL loop filter New bill of materials for operation at 433 MHz and 868/915 MHz Added recommended PCB footprint for package (QFN 20) Added list of abbreviations Changes to ordering information
1.2	2005-10-20	Calibration routine flow chart changed Added chapter on TX data latency
1.3 SWRS043	2006-02-01	Updates to Ordering Information and Address Information. The lowest supply voltage has been changed from 2.1 V to 2.3 V
SWRS043A	2010-01-06	Removed logo from header Changed numbering on capacitors connected to XOSC_Q1 and XOSC_Q2 in figure 3 and figure 20 to reflect the reference design. Changes to chapter on Package Description Changes to chapter on Package Marking Removed chapter on Package Thermal Properties Changes to Ordering Information Removed chapter on Product Status Definition Tape and Reel Information on new package (RGW) added Removed chapter on Address Information Added ESD results

TAPE AND REEL INFORMATION

REEL DIMENSIONS

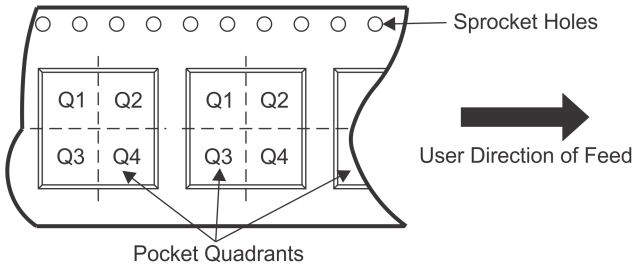


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

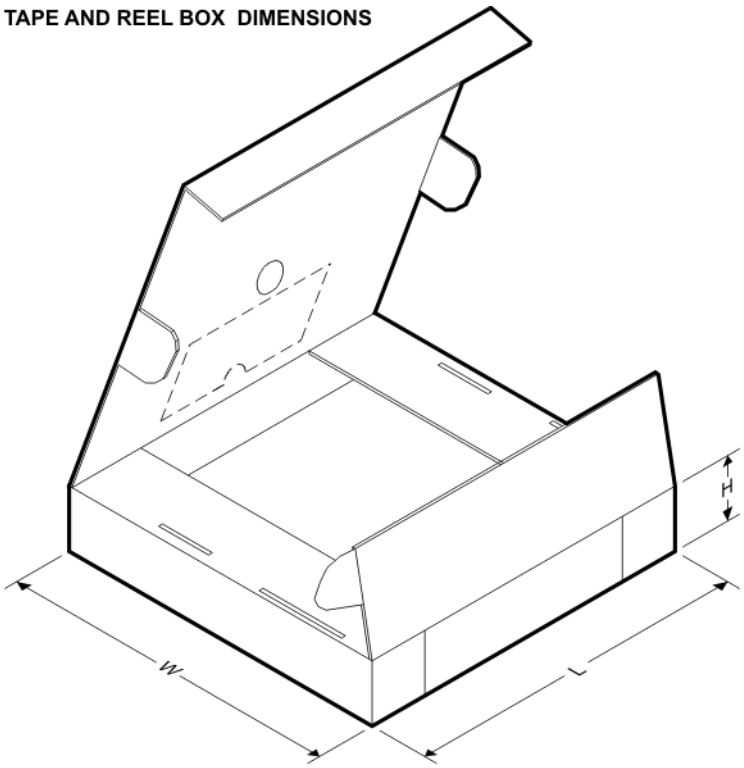
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC1070RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
CC1070RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC1070RGWR	VQFN	RGW	20	3000	338.1	338.1	20.6
CC1070RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

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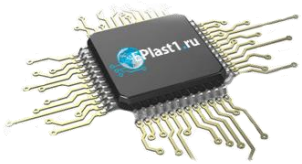
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Как с нами связаться

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