



CMOS Static RAM 1 Meg (128K x 8-Bit) Revolutionary Pinout

IDT71124

Features

- ◆ 128K x 8 advanced high-speed CMOS static RAM
- ◆ JEDEC revolutionary pinout (center power/GND) for reduced noise.
- ◆ Equal access and cycle times
 - Commercial: 12/15/20ns
 - Industrial: 15/20ns
- ◆ One Chip Select plus one Output Enable pin
- ◆ Bidirectional inputs and outputs directly TTL-compatible
- ◆ Low power consumption via chip deselect
- ◆ Available in a 32-pin 400 mil Plastic SOJ.

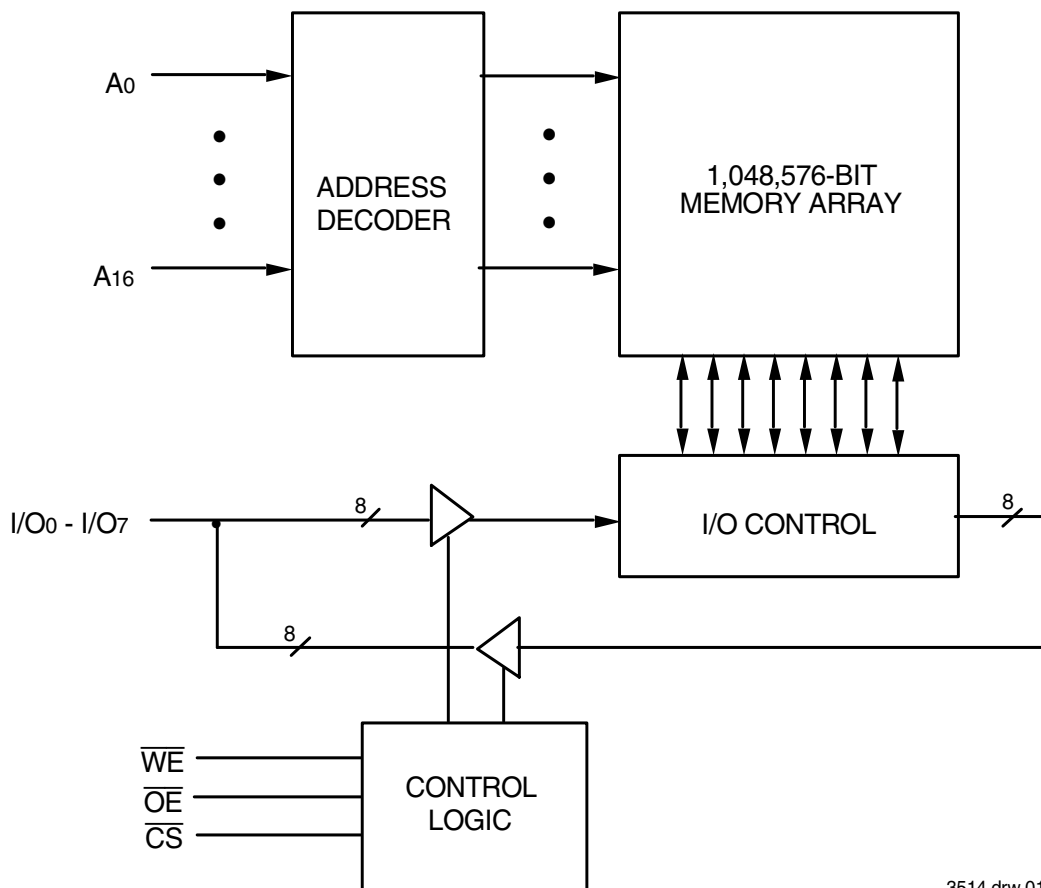
Description

The IDT71124 is a 1,048,576-bit high-speed static RAM organized as 128K x 8. It is fabricated using high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs. The JEDEC centerpower/GND pinout reduces noise generation and improves system performance.

The IDT71124 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns available. All bidirectional inputs and outputs of the IDT71124 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

The IDT71124 is packaged in a 32-pin 400 mil Plastic SOJ.

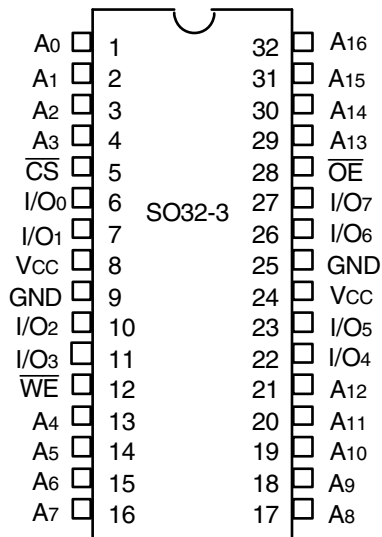
Functional Block Diagram



3514 drw 01

APRIL 2013

Pin Configuration



3514 drw 02

SOJ Top View

Truth Table^(1,2)

| \overline{CS} | \overline{OE} | \overline{WE} | I/O | Function |
|--------------------------------|-----------------|-----------------|---------|-----------------------------|
| L | L | H | DATAOUT | Read Data |
| L | X | L | DATAIN | Write Data |
| L | H | H | High-Z | Output Disabled |
| H | X | X | High-Z | Deselected - Standby (1sB) |
| V _{HC} ⁽³⁾ | X | X | High-Z | Deselected - Standby (1sB1) |

3514 tbl 01

- NOTES:
- H = V_{HH}, L = V_{IL}, x = Don't care.
 - V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V.
 - Other inputs \geq V_{HC} or \leq V_{LC}.

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Value | Unit |
|----------------------------------|--------------------------------------|-----------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7.0 ⁽²⁾ | V |
| T _A | Operating Temperature | 0 to +70 | °C |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -55 to +125 | °C |
| P _T | Power Dissipation | 1.25 | W |
| I _{OUT} | DC Output Current | 50 | mA |

3514 tbl 02

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{CC} + 0.5V.

Capacitance

(T_A = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|------------------|--------------------------|------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 8 | pF |
| C _{I/O} | I/O Capacitance | V _{OUT} = 3dV | 8 | pF |

3514 tbl 03

NOTE:

- This parameter is guaranteed by device characterization, but is not production tested.

Recommended Operating Temperature and Supply Voltage

| Grade | Temperature | GND | V _{CC} |
|------------|----------------|-----|-----------------|
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |
| Industrial | -40°C to +85°C | 0V | 5.0V ± 10% |

3514 tbl 04

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|---------------------|------|-----------------------|------|
| V _{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage | 2.2 | — | V _{CC} + 0.5 | V |
| V _{IL} | Input Low Voltage | -0.5 ⁽¹⁾ | — | 0.8 | V |

3514 tbl 05

DC Electrical Characteristics

($V_{CC} = 5.0V \pm 10\%$, Commercial and Industrial Temperature Ranges)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|------------|------------------------|---|------|------|---------------|
| $ I_{LI} $ | Input Leakage Current | $V_{CC} = \text{Max.}, V_{IN} = \text{GND to } V_{CC}$ | — | 5 | μA |
| $ I_{LO} $ | Output Leakage Current | $V_{CC} = \text{Max.}, \overline{CS} = V_{IH}, V_{OUT} = \text{GND to } V_{CC}$ | — | 5 | μA |
| V_{OL} | Output Low Voltage | $I_{OL} = 8\text{mA}, V_{CC} = \text{Min.}$ | — | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -4\text{mA}, V_{CC} = \text{Min.}$ | 2.4 | — | V |

3514 tbl 06

DC Electrical Characteristics⁽¹⁾

($V_{CC} = 5.0V \pm 10\%$, $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$)

| Symbol | Parameter | 71124S12 | 71124S15 | | 71124S20 | | Unit |
|-----------|---|----------|----------|------|----------|------|------|
| | | Com'l. | Com'l. | Ind. | Com'l. | Ind. | |
| I_{CC} | Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, $V_{CC} = \text{Max.}, f = f_{MAX}^{(2)}$ | 160 | 155 | 155 | 140 | 140 | mA |
| I_{SB} | Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, $V_{CC} = \text{Max.}, f = f_{MAX}^{(2)}$ | 40 | 40 | 40 | 40 | 40 | mA |
| I_{SB1} | Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, $V_{CC} = \text{Max.}, f = 0^{(2)}$ $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$ | 10 | 10 | 10 | 10 | 10 | mA |

NOTES:

- All values are maximum guaranteed values.
- $f_{MAX} = 1/t_{rc}$ (all address inputs are cycling at f_{MAX}): $f = 0$ means no address input lines are changing.

3514 tbl 07

AC Test Conditions

| | |
|-------------------------------|--------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 3ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| AC Test Load | See Figure 1 and 2 |

3514 tbl 08

AC Test Loads

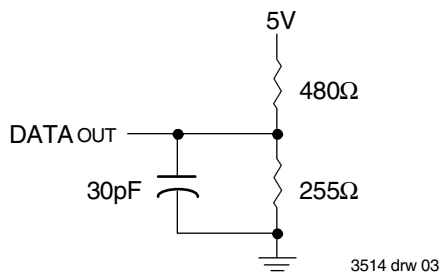
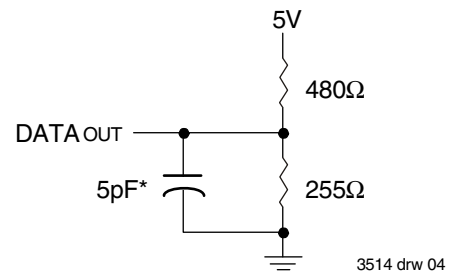


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ} , t_{OLZ} , t_{CHZ} , t_{OHZ} , t_{OW} , and t_{WHZ})

AC Electrical Characteristics

(V_{cc} = 5.0V ± 10%, Commercial and Industrial Temperature Ranges)

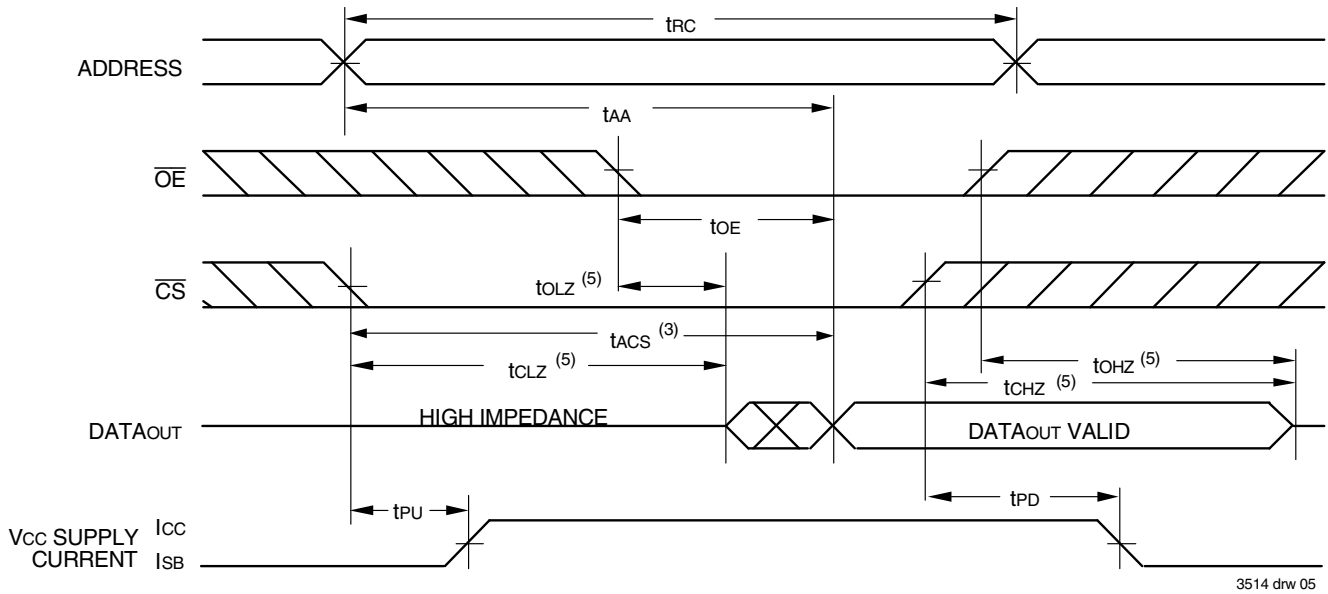
| Symbol | Parameter | 71124S12 ⁽²⁾ | | 71124S15 | | 71124S20 | | Unit |
|---------------------------------|------------------------------------|-------------------------|------|----------|------|----------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t _{RC} | Read Cycle Time | 12 | — | 15 | — | 20 | — | ns |
| t _{AA} | Address Access Time | — | 12 | — | 15 | — | 20 | ns |
| t _{ACS} | Chip Select Access Time | — | 12 | — | 15 | — | 20 | ns |
| t _{CLZ} ⁽¹⁾ | Chip Select to Output in Low-Z | 3 | — | 3 | — | 3 | — | ns |
| t _{CHZ} ⁽¹⁾ | Chip Deselect to Output in High-Z | 0 | 6 | 0 | 7 | 0 | 8 | ns |
| t _{OE} | Output Enable to Output Valid | — | 6 | — | 7 | — | 8 | ns |
| t _{OLZ} ⁽¹⁾ | Output Enable to Output in Low-Z | 0 | — | 0 | — | 0 | — | ns |
| t _{OHZ} ⁽¹⁾ | Output Disable to Output in High-Z | 0 | 5 | 0 | 5 | 0 | 7 | ns |
| t _{OH} | Output Hold from Address Change | 4 | — | 4 | — | 4 | — | ns |
| t _{PU} ⁽¹⁾ | Chip Select to Power-Up Time | 0 | — | 0 | — | 0 | — | ns |
| t _{PD} ⁽¹⁾ | Chip Deselect to Power-Down Time | — | 12 | — | 15 | — | 20 | ns |
| WRITE CYCLE | | | | | | | | |
| t _{WC} | Write Cycle Time | 12 | — | 15 | — | 20 | — | ns |
| t _{AW} | Address Valid to End of Write | 8 | — | 12 | — | 15 | — | ns |
| t _{CW} | Chip Select to End of Write | 8 | — | 12 | — | 15 | — | ns |
| t _{AS} | Address Set-up Time | 0 | — | 0 | — | 0 | — | ns |
| t _{WP} | Write Pulse Width | 8 | — | 12 | — | 15 | — | ns |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | ns |
| t _{DW} | Data Valid to End-of-Write | 6 | — | 8 | — | 9 | — | ns |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | 0 | — | ns |
| t _{OW} ⁽¹⁾ | Output active from End-of-Write | 3 | — | 3 | — | 4 | — | ns |
| t _{WHZ} ⁽¹⁾ | Write Enable to Output in High-Z | 0 | 5 | 0 | 5 | 0 | 8 | ns |

3514 tbl 09

NOTE:

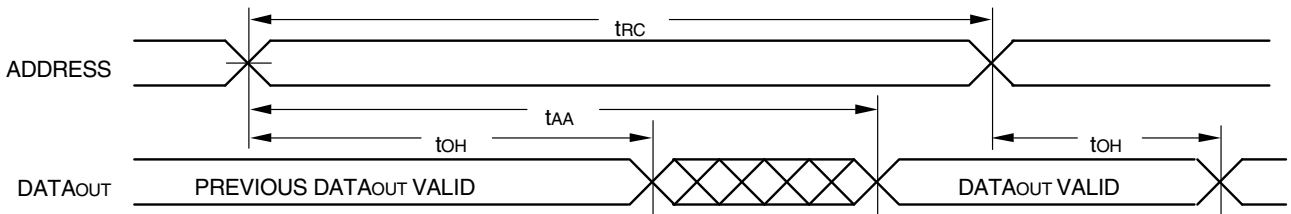
1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.
2. There is no industrial temperature offering for the 12ns speed grade.

Timing Waveform of Read Cycle No. 1⁽¹⁾



3514 drw 05

Timing Waveform of Read Cycle No. 2^(1,2,4)

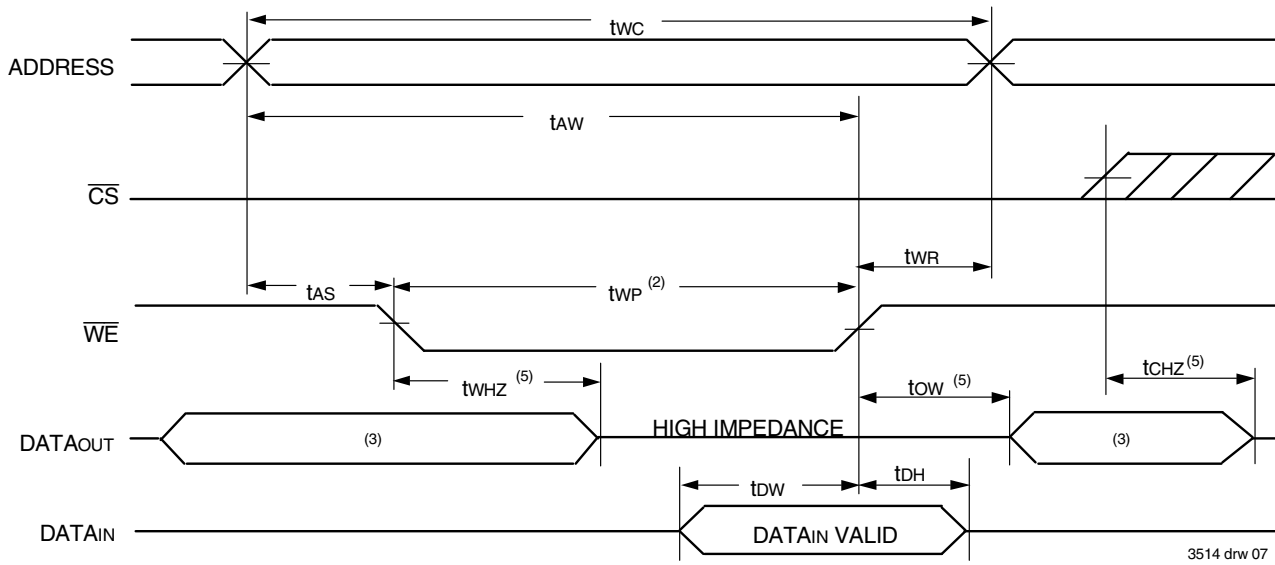


3514 drw 06

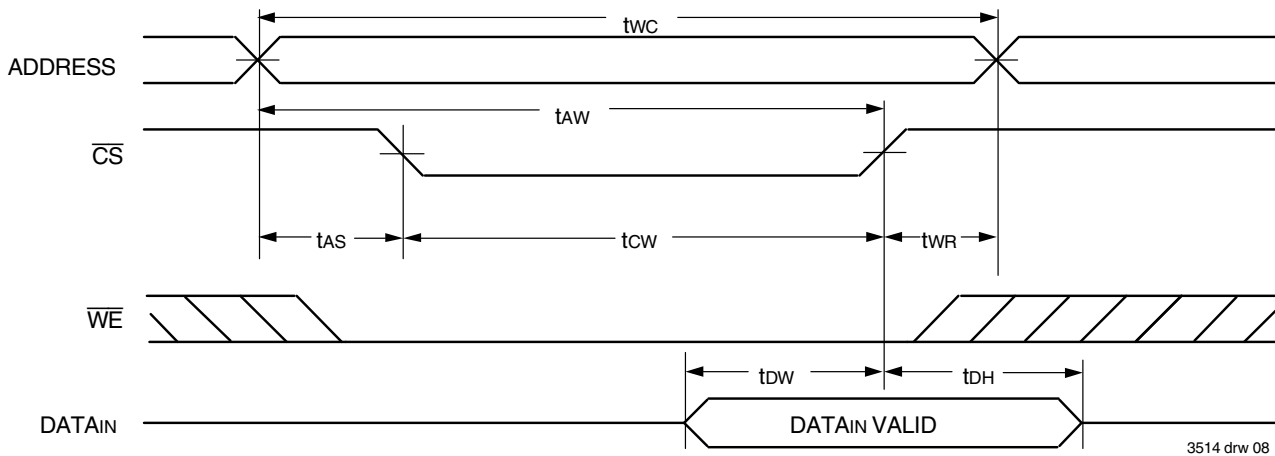
NOTES:

1. \overline{WE} is HIGH for Read Cycle.
2. Device is continuously selected, \overline{CS} is LOW.
3. Address must be valid prior to or coincident with the later of \overline{CS} transition LOW; otherwise t_{AA} is the limiting parameter.
4. \overline{OE} is LOW.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

Timing Waveform of Write Cycle No. 1 (\overline{WE} Controlled Timing)^(1,2,4)



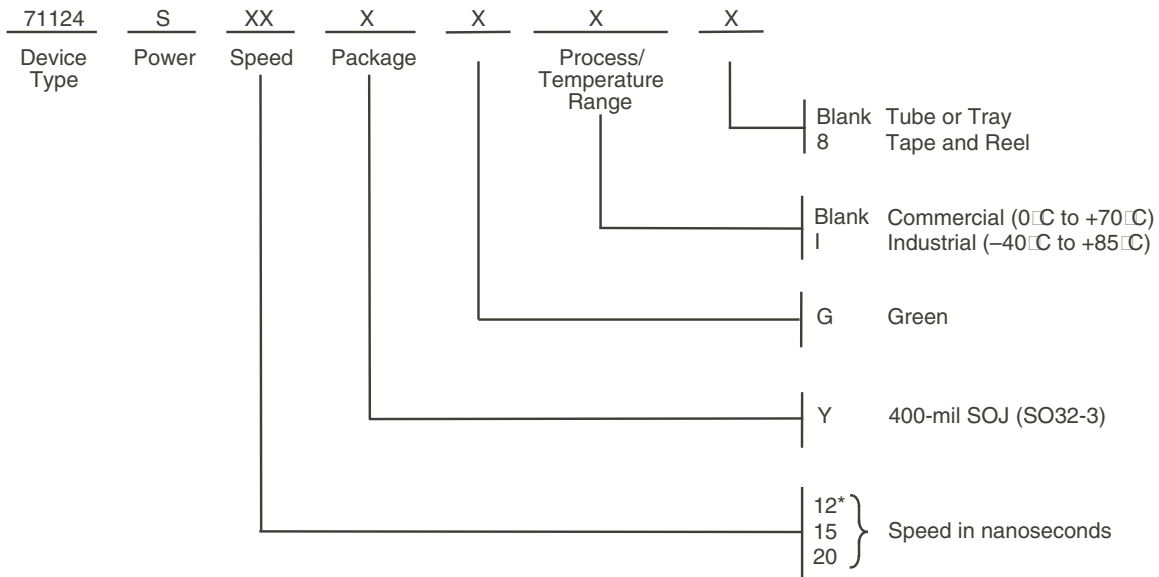
Timing Waveform of Write Cycle No. 2 (\overline{CS} Controlled Timing)^(1,4)



NOTES:

1. A write occurs during the overlap of a LOW \overline{CS} and a LOW \overline{WE} .
2. \overline{OE} is continuously HIGH. During a \overline{WE} controlled write cycle with \overline{OE} LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{OW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP} .
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the \overline{CS} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high impedance state. \overline{CS} must be active during the t_{CW} write period.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

Ordering Information



3514 drw 09

* No industrial temp on 12ns speed

Datasheet Document History

| | | |
|-----------|----------------|---|
| 08/05/99: | | Updated to new format |
| | Pg. 3 | Removed military entries on DC table |
| | Pg. 4 | Removed Note 1 and renumbered footnotes |
| | Pg. 6 | Revised footnotes on Write Cycle No. 1 diagram |
| 08/13/99: | Pg. 8 | Added Datasheet Document History |
| 09/30/99: | Pg. 1, 3, 4, 7 | Added 12ns, 15ns, and 20ns industrial temperature speed grade offerings |
| 02/18/00: | Pg. 3 | Revise LSB for Industrial Temperature offerings to meet commercial specifications |
| 03/14/00: | Pg. 3 | Revised LSB to accommodate speed functionality |
| 04/01/00: | Pg.4 | Tightened tAW, tCW, tWP and tDW within the AC Electrical Characteristics |
| 08/09/00: | | Not recommended for new designs |
| 02/01/01: | | Removed "Not recommended for new designs" |
| 10/23/08: | Pg.7 | Removed "IDT" from the orderable part number |
| 04/02/13: | Pg.1 | Removed 12ns speed from the Industrial temp offering. Removed IDT in reference to fabrication |
| | Pg.3 | Removed the industrial 12ns speed grade information from the DC Electrical Chars table 07 |
| | Pg.4 | Added footnote 2 to AC Electrical Chars table 09 to indicate that there is no industrial 12ns speed |
| | Pg.7 | Added Tape & Reel and Green designators to the ordering information. Added a footnote to the ordering information to indicate that there is no industrial 12ns speed offering |



CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or
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Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.