

MJD41C, NJVMJD41CT4G (NPN), MJD42C, NJVMJD42CT4G, NJVMJD42CRLG (PNP)

Complementary Power Transistors

DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

Features

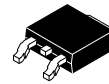
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("1" Suffix)
- Electrically Similar to Popular TIP41 and TIP42 Series
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings:
 - ♦ Human Body Model, 3B > 8000 V
 - ♦ Machine Model, C > 400 V
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Packages*



ON Semiconductor®

<http://onsemi.com>

**SILICON
POWER TRANSISTORS
6 AMPERES
100 VOLTS, 20 WATTS**

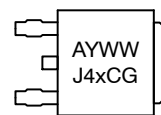


**DPAK
CASE 369C
STYLE 1**

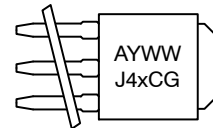


**DPAK-3
CASE 369D
STYLE 1**

MARKING DIAGRAMS



DPAK



DPAK-3

A = Assembly Location
Y = Year
WW = Work Week
J4xC = Device Code
x = 1 or 2
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current Continuous Peak	I_C	6 10	Adc
Base Current	I_B	2	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	20 0.16	W W/ $^\circ\text{C}$
Total Power Dissipation (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.75 0.014	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	6.25	$^\circ\text{C/W}$
Thermal Resistance, Junction–to–Ambient (Note 1)	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (Note 2) (I _C = 30 mAdc, I _B = 0)	V _{CEO(sus)}	100	–	Vdc
Collector Cutoff Current (V _{CE} = 60 Vdc, I _B = 0)	I _{CEO}	–	50	μAdc
Collector Cutoff Current (V _{CE} = 100 Vdc, V _{EB} = 0)	I _{CES}	–	10	μAdc
Emitter Cutoff Current (V _{BE} = 5 Vdc, I _C = 0)	I _{EBO}	–	0.5	mAdc

ON CHARACTERISTICS (Note 2)

DC Current Gain (I _C = 0.3 Adc, V _{CE} = 4 Vdc) (I _C = 3 Adc, V _{CE} = 4 Vdc)	h _{FE}	30 15	– 75	
Collector–Emitter Saturation Voltage (I _C = 6 Adc, I _B = 600 mAdc)	V _{CE(sat)}	–	1.5	Vdc
Base–Emitter On Voltage (I _C = 6 Adc, V _{CE} = 4 Vdc)	V _{BE(on)}	–	2	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product (Note 3) (I _C = 500 mAdc, V _{CE} = 10 Vdc, f _{test} = 1 MHz)	f _T	3	–	MHz
Small–Signal Current Gain (I _C = 0.5 Adc, V _{CE} = 10 Vdc, f = 1 kHz)	h _{fe}	20	–	

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3. f_T = |h_{fe}| • f_{test}.

ORDERING INFORMATION

Device	Package Type	Package	Shipping [†]
MJD41CRLG	DPAK (Pb–Free)	369C	1,800 / Tape & Reel
MJD41CT4G	DPAK (Pb–Free)	369C	2,500 / Tape & Reel
NJVMJD41CT4G	DPAK (Pb–Free)	369C	2,500 / Tape & Reel
MJD42CG	DPAK (Pb–Free)	369C	75 Units / Rail
MJD42C1G	DPAK–3 (Pb–Free)	369D	75 Units / Rail
MJD42CRLG	DPAK (Pb–Free)	369C	1,800 / Tape & Reel
NJVMJD42CRLG	DPAK (Pb–Free)	369C	1,800 / Tape & Reel
MJD42CT4G	DPAK (Pb–Free)	369C	2,500 / Tape & Reel
NJVMJD42CT4G	DPAK (Pb–Free)	369C	2,500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

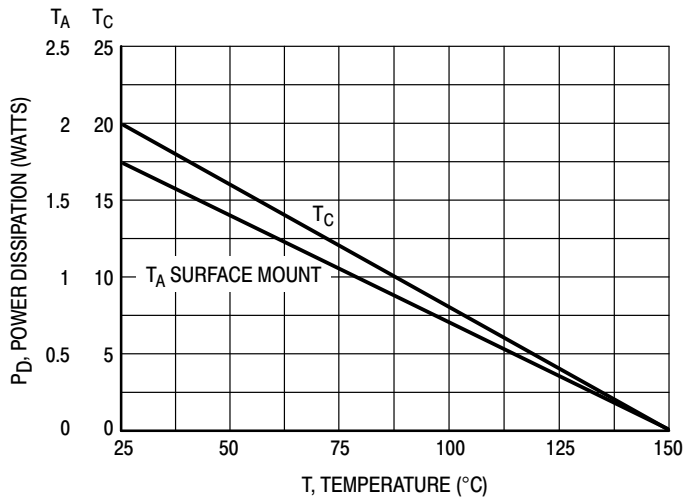
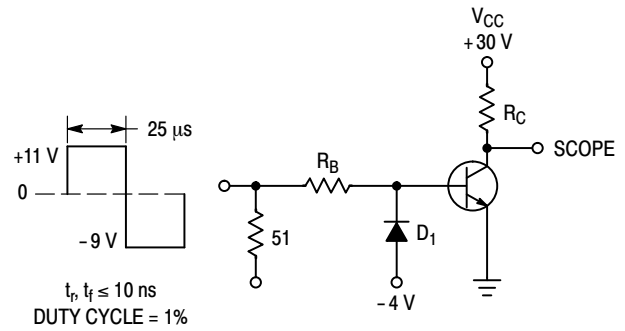


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
 D_1 MUST BE FAST RECOVERY TYPE, e.g.:
 MSB5300 USED ABOVE $I_B \approx 100$ mA
 MSD6100 USED BELOW $I_B \approx 100$ mA
 REVERSE ALL POLARITIES FOR PNP.

Figure 2. Switching Time Test Circuit

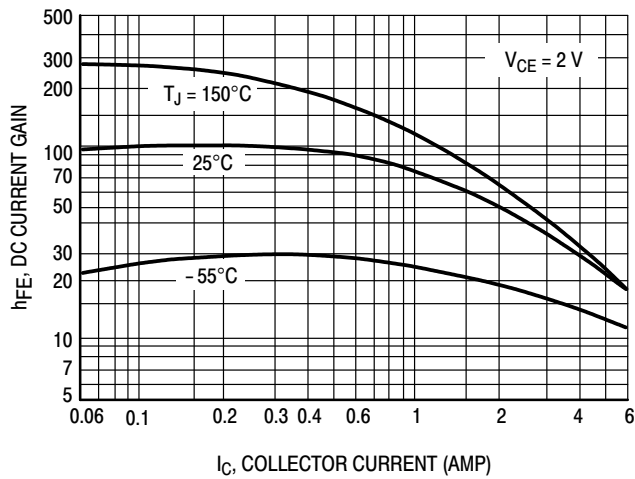


Figure 3. DC Current Gain

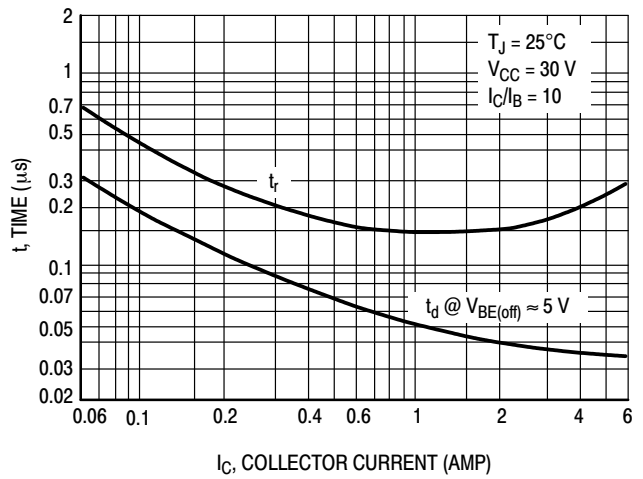


Figure 4. Turn-On Time

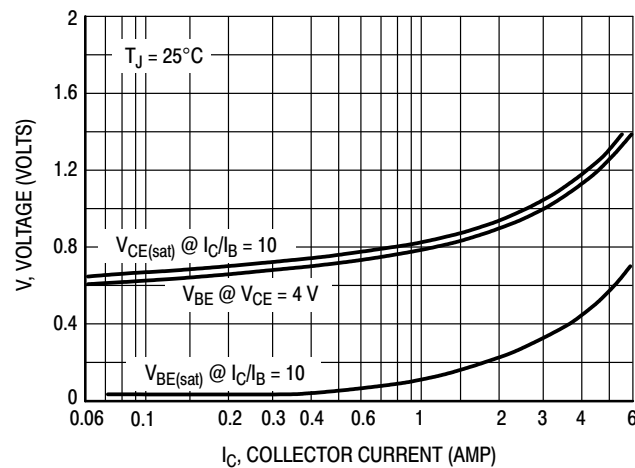


Figure 5. "On" Voltages

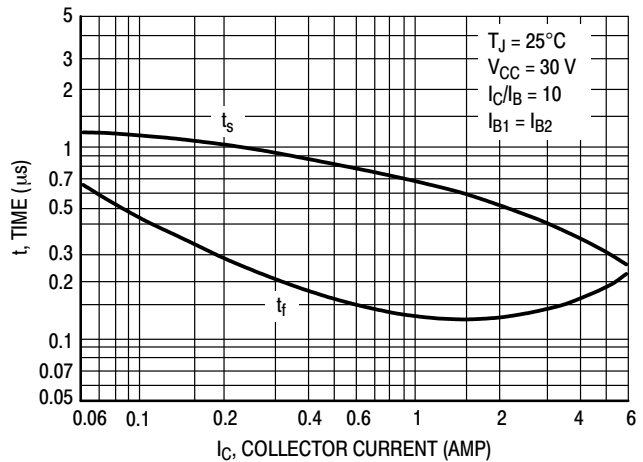


Figure 6. Turn-Off Time

MJD41C, NJVMJD41CT4G (NPN), MJD42C, NJVMJD42CT4G, NJVMJD42CRLG (PNP)

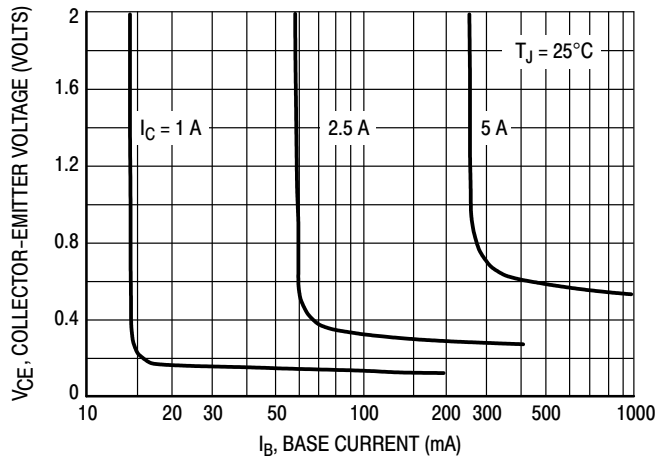


Figure 7. Collector Saturation Region

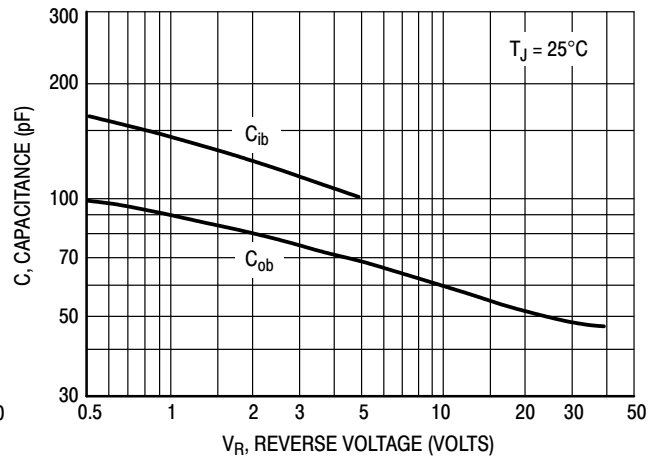


Figure 8. Capacitance

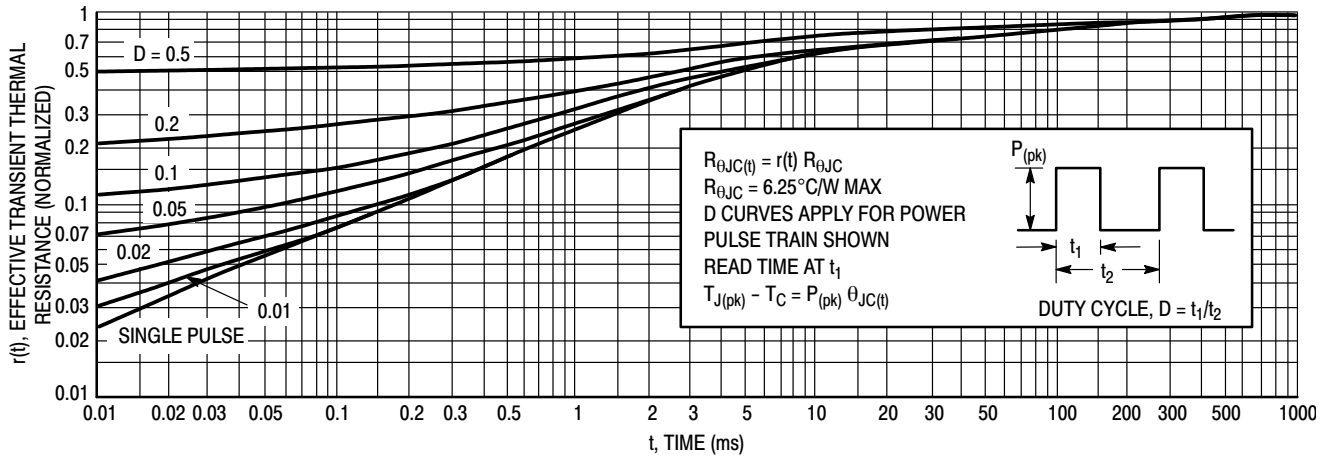


Figure 9. Thermal Response

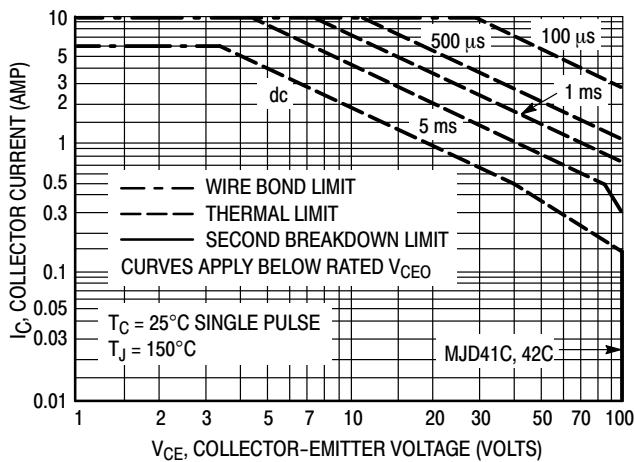


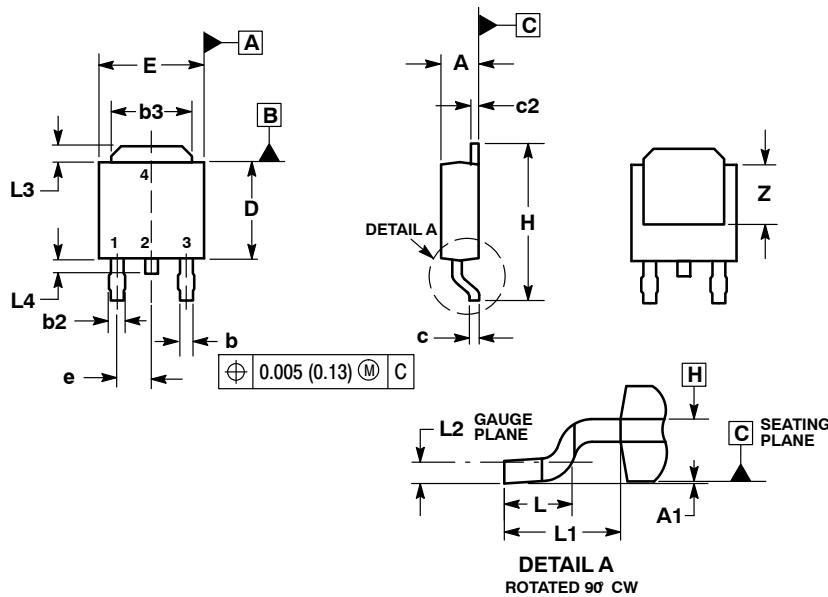
Figure 10. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

PACKAGE DIMENSIONS

DPAK
CASE 369C-01
ISSUE D

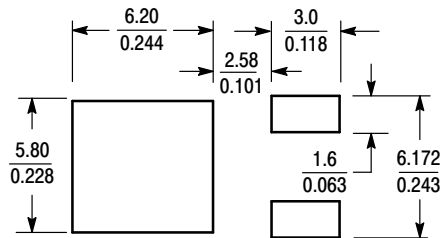


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}} \right)$

STYLE 1:

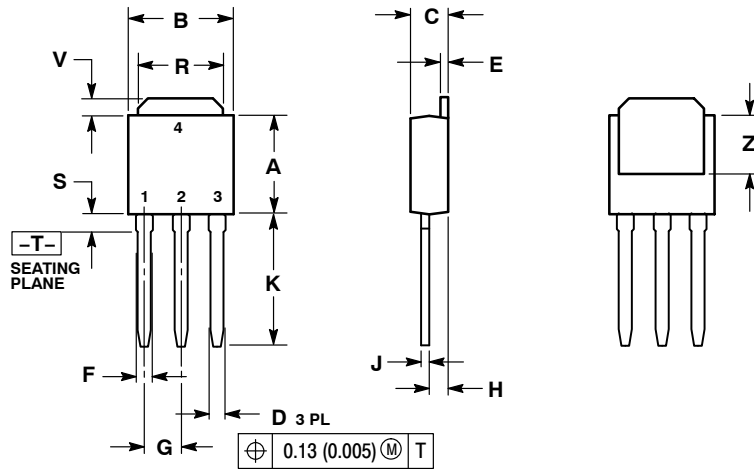
- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

IPAK CASE 369D-01 ISSUE C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 1:

1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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- Техническая поддержка проекта;
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