TMP175
TMP75

SBOS288J − JANUARY 2004 − REVISED DECEMBER 2007

Digital Temperature Sensor with Two-Wire Interface

FEATURES

- **27 ADDRESSES (TMP175)**
  8 ADDRESSES (TMP75)
- **DIGITAL OUTPUT: Two-Wire Serial Interface**
- **RESOLUTION: 9- to 12-Bits, User-Selectable**
- **ACCURACY:**
  ±1.5°C (max) from −25°C to +85°C
  ±2.0°C (max) from −40°C to +125°C
- **LOW QUIESCENT CURRENT:**
  50μA, 0.1μA Standby
- **WIDE SUPPLY RANGE: 2.7V to 5.5V**
- **SMALL SO-8 AND MSOP-8 PACKAGES**

APPLICATIONS

- **POWER-SUPPLY TEMPERATURE MONITORING**
- **COMPUTER PERIPHERAL THERMAL PROTECTION**
- **NOTEBOOK COMPUTERS**
- **CELL PHONES**
- **BATTERY MANAGEMENT**
- **OFFICE MACHINES**
- **THERMOSTAT CONTROLS**
- **ENVIRONMENTAL MONITORING AND HVAC**
- **ELECTROMECHANICAL DEVICE TEMPERATURE**

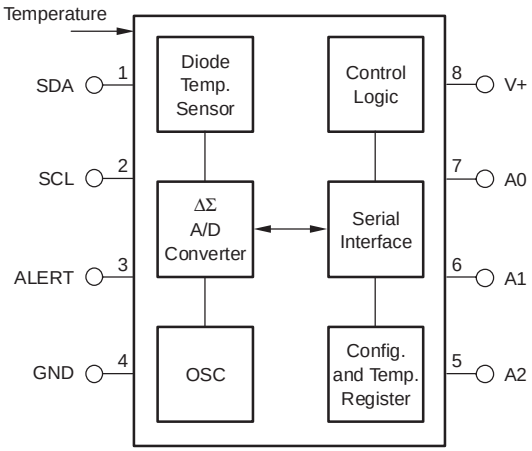
DESCRIPTION

The TMP175 and TMP75 are two-wire, serial output temperature sensors available in SO-8 and MSOP-8 packages. Requiring no external components, the TMP175 and TMP75 are capable of reading temperatures with a resolution of 0.0625°C.

The TMP175 and TMP75 feature a Two-Wire interface that is SMBus-compatible, with the TMP175 allowing up to 27 devices on one bus and the TMP75 allowing up to eight devices on one bus. The TMP175 and TMP75 both feature an SMBus Alert function.

The TMP175 and TMP75 are ideal for extended temperature measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.

The TMP175 and TMP75 are specified for operation over a temperature range of −40°C to +125°C.



TMP175, TMP75

ABSOLUTE MAXIMUM RATINGS(1)

Power Supply, V+	7.0V
Input Voltage(2)	−0.5V to 7.0V
Input Current	10mA
Operating Temperature Range	−55°C to +127°C
Storage Temperature Range	−60°C to +130°C
Junction Temperature (T_J max)	+150°C
ESD Rating:	
Human Body Model (HBM)	4000V
Charged Device Model (CDM)	1000V
Machine Model (MM)	300V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Input voltage rating applies to all TMP175 and TMP75 input voltages.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

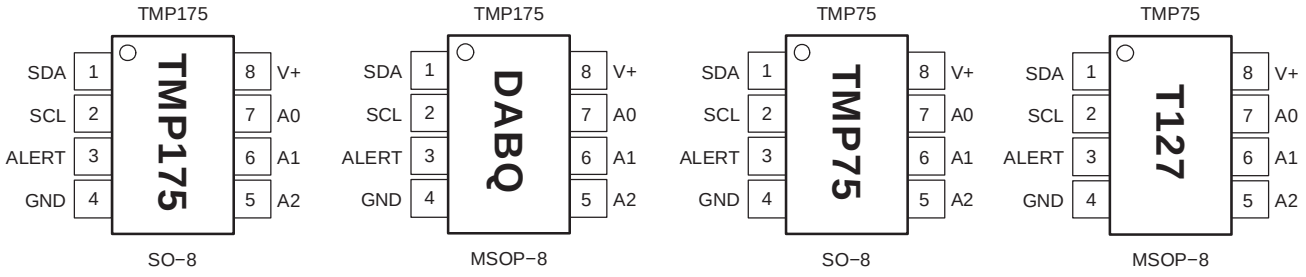
ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
TMP175	SO-8	D	TMP175
TMP175	MSOP-8	DGK	DABQ
TMP75	SO-8	D	TMP75
TMP75	MSOP-8	DGK	T127

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN ASSIGNMENTS

Top View



NOTE: Pin 1 is determined by orienting the package marking as indicated in the diagram.

ELECTRICAL CHARACTERISTICS

At T_A = −40°C to +125°C, and V+ = 2.7V to 5.5V, unless otherwise noted.

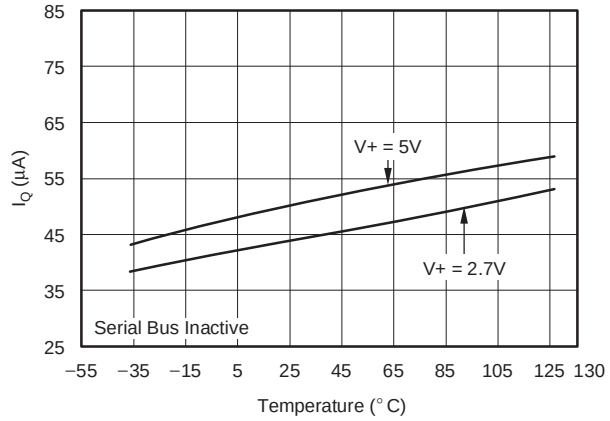
PARAMETER	CONDITION	TMP175			TMP75			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE INPUT								
Range		−40		+125	−40		+125	°C
Accuracy (Temperature Error)	−25°C to +85°C		±0.5	±1.5		±0.5	±2.0	°C
	−40°C to +125°C		±1.0	±2.0		±1.0	±3.0	°C
vs Supply			0.2	±0.5		0.2	±0.5	°C/V
Resolution(1)	Selectable		+0.0625			+0.0625		°C
DIGITAL INPUT/OUTPUT								
Input Capacitance			3			3		pF
Input Logic Levels:								
V_{IH}		0.7(V+)		6.0	0.7(V+)		6.0	V
V_{IL}		−0.5		0.3(V+)	−0.5		0.3(V+)	V
Leakage Input Current, I_{IN}	$0V \le V_{IN} \le 6V$			1			1	µA
Input Voltage Hysteresis	SCL and SDA Pins		500			500		mV
Output Logic Levels:								
V_{OL} SDA	I_{OL} = 3mA	0	0.15	0.4	0	0.15	0.4	V
V_{OL} ALERT	I_{OL} = 4mA	0	0.15	0.4	0	0.15	0.4	V
Resolution	Selectable		9 to 12			9 to 12		Bits
Conversion Time	9-Bit		27.5	37.5		27.5	37.5	ms
	10-Bit		55	75		55	75	ms
	11-Bit		110	150		110	150	ms
	12-Bit		220	300		220	300	ms
Timeout Time		25	54	74	25	54	74	ms
POWER SUPPLY								
Operating Range		2.7		5.5	2.7		5.5	V
Quiescent Current I_Q	Serial Bus Inactive		50	85		50	85	µA
	Serial Bus Active, SCL Freq = 400kHz		100			100		µA
	Serial Bus Active, SCL Freq = 3.4MHz		410			410		µA
Shutdown Current I_{SD}	Serial Bus Inactive		0.1	3		0.1	3	µA
	Serial Bus Active, SCL Freq = 400kHz		60			60		µA
	Serial Bus Active, SCL Freq = 3.4MHz		380			380		µA
TEMPERATURE RANGE								
Specified Range		−40		+125	−40		+125	°C
Operating Range		−55		+127	−55		+127	°C
Thermal Resistance θ_{JA}								
MSOP-8			250			250		°C/W
SO-8			150			150		°C/W

(1) Specified for 12-bit resolution.

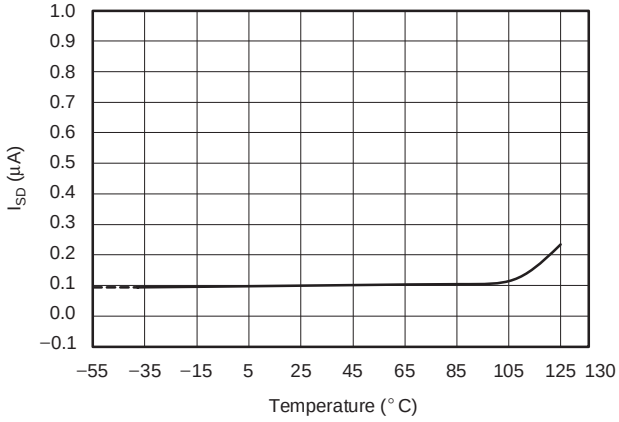
TYPICAL CHARACTERISTICS

At T_A = +25°C and V+ = 5.0V, unless otherwise noted.

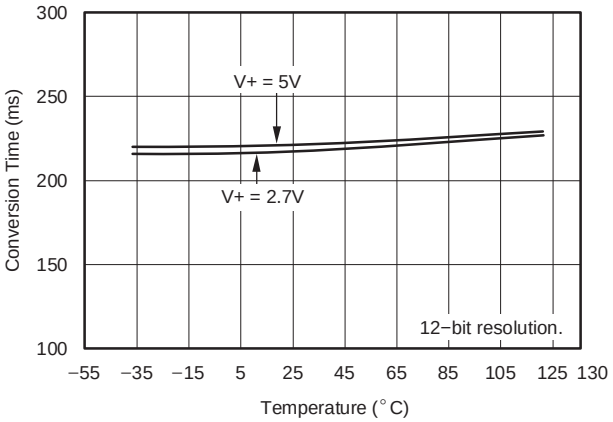
QUIESCENT CURRENT vs TEMPERATURE



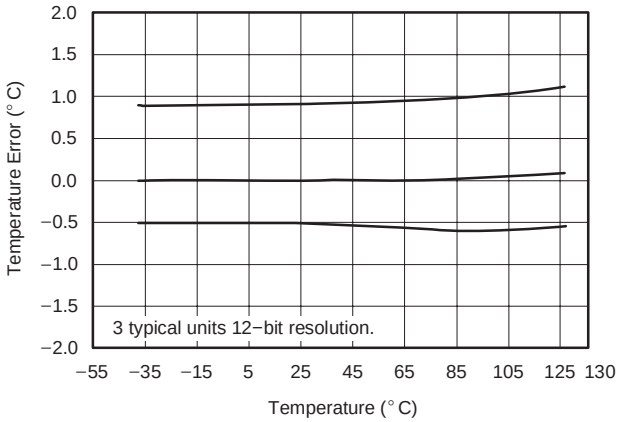
SHUTDOWN CURRENT vs TEMPERATURE



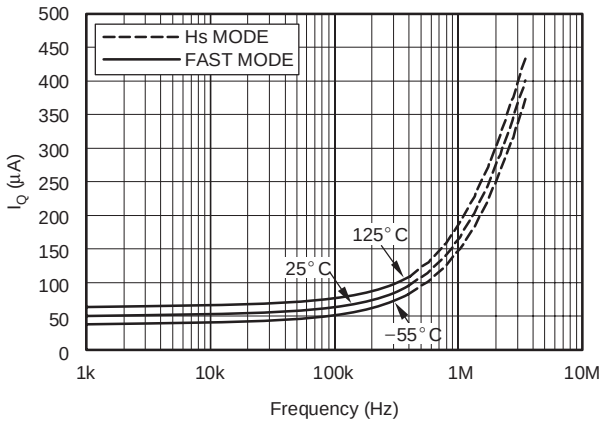
CONVERSION TIME vs TEMPERATURE



TEMPERATURE ACCURACY vs TEMPERATURE



QUIESCENT CURRENT WITH
BUS ACTIVITY vs TEMPERATURE



APPLICATIONS INFORMATION

The TMP175 and TMP75 are digital temperature sensors that are optimal for thermal management and thermal protection applications. The TMP175 and TMP75 are Two-Wire and SMBus interface-compatible, and are specified over a temperature range of −40°C to +125°C.

The TMP175 and TMP75 require no external components for operation except for pull-up resistors on SCL, SDA, and ALERT, although a 0.1µF bypass capacitor is recommended, as shown in Figure 1.

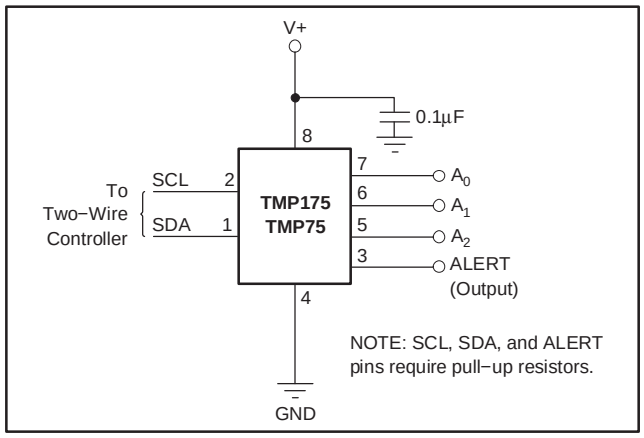


Figure 1. Typical Connections of the TMP175 and TMP75

The sensing device of the TMP175 and TMP75 is the chip itself. Thermal paths run through the package leads as well as the plastic package. The lower thermal resistance of metal causes the leads to provide the primary thermal path.

To maintain accuracy in applications requiring air or surface temperature measurement, care should be taken to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive will assist in achieving accurate surface temperature measurement.

POINTER REGISTER

Figure 2 shows the internal register structure of the TMP175 and TMP75. The 8-bit Pointer Register of the devices is used to address a given data register. The Pointer Register uses the two LSBs to identify which of the data registers should respond to a read or write command. Table 1 identifies the bits of the Pointer Register byte. Table 2 describes the pointer address of the registers available in the TMP175 and TMP75. Power-up reset value of P1/P0 is 00.

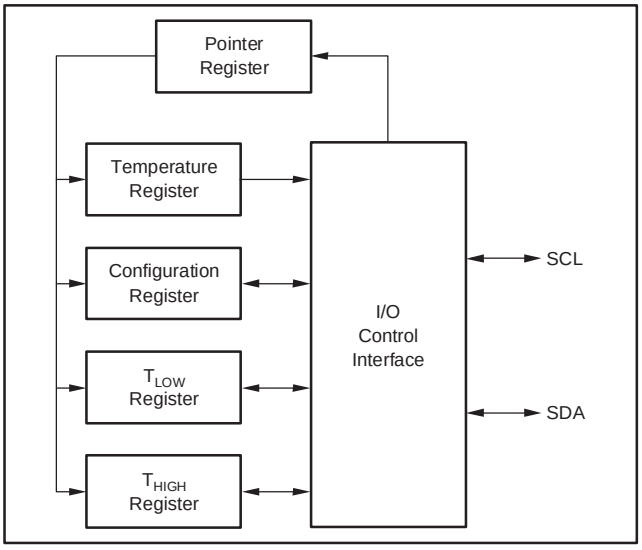


Figure 2. Internal Register Structure of the TMP175 and TMP75

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

Table 1. Pointer Register Byte

P1	P0	REGISTER
0	0	Temperature Register (READ Only)
0	1	Configuration Register (READ/WRITE)
1	0	T_{LOW} Register (READ/WRITE)
1	1	T_{HIGH} Register (READ/WRITE)

Table 2. Pointer Addresses of the TMP175 and TMP75

TEMPERATURE REGISTER

The Temperature Register of the TMP175 or TMP75 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in Table 3 and Table 4. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. Data format for temperature is summarized in Table 5. Following power-up or reset, the Temperature Register will read 0°C until the first conversion is complete.

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

Table 3. Byte 1 of Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

Table 4. Byte 2 of Temperature Register

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
−0.25	1111 1111 1100	FFC
−25	1110 0111 0000	E70
−55	1100 1001 0000	C90

Table 5. Temperature Data Format

The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration Register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits in the Temperature Register are used with the unused LSBs set to zero.

CONFIGURATION REGISTER

The Configuration Register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. The format of the Configuration Register for the TMP175 and TMP75 is shown in Table 6, followed by a breakdown of the register bits. The power-up/reset value of the Configuration Register is all bits equal to 0.

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS	R1	R0	F1	F0	POL	TM	SD

Table 6. Configuration Register Format

SHUTDOWN MODE (SD)

The Shutdown Mode of the TMP175 and TMP75 allows the user to save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to typically less than 0.1μA. Shutdown Mode is enabled when the SD bit is 1; the device will shut down once the current conversion is completed. When SD is equal to 0, the device will maintain a continuous conversion state.

THERMOSTAT MODE (TM)

The Thermostat Mode bit of the TMP175 and TMP75 indicates to the device whether to operate in Comparator Mode (TM = 0) or Interrupt Mode (TM = 1). For more information on comparator and interrupt modes, see the *High and Low Limit Registers* section.

POLARITY (POL)

The Polarity Bit of the TMP175 and TMP75 allows the user to adjust the polarity of the ALERT pin output. If POL = 0, the ALERT pin will be active LOW, as shown in Figure 3. For POL = 1, the ALERT pin will be active HIGH, and the state of the ALERT pin is inverted.

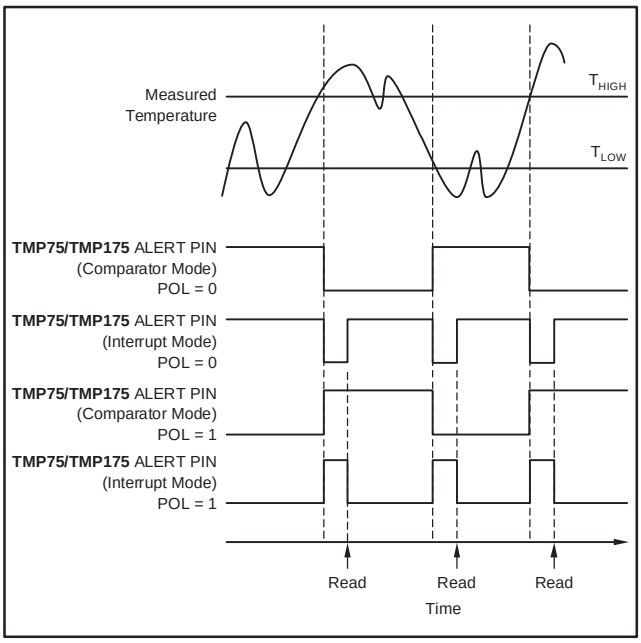


Figure 3. Output Transfer Function Diagrams

FAULT QUEUE (F1/F0)

A fault condition is defined as when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} Registers. Additionally, the number of fault conditions required to generate an alert may be programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements in order to trigger the alert function. Table 7 defines the number of measured faults that may be programmed to trigger an alert condition in the device. For T_{HIGH} and T_{LOW} register format and byte order, see the section *High and Low Limit Registers*.

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

Table 7. Fault Settings of the TMP175 and TMP75

CONVERTER RESOLUTION (R1/R0)

The Converter Resolution Bits control the resolution of the internal Analog-to-Digital (A/D) converter. This allows the user to maximize efficiency by programming for higher

resolution or faster conversion time. Table 8 identifies the Resolution Bits and the relationship between resolution and conversion time.

R1	R0	RESOLUTION	CONVERSION TIME (typical)
0	0	9 Bits (0.5°C)	27.5ms
0	1	10 Bits (0.25°C)	55ms
1	0	11 Bits (0.125°C)	110ms
1	1	12 Bits (0.0625°C)	220ms

Table 8. Resolution of the TMP175 and TMP75

ONE-SHOT (OS)

The TMP175 and TMP75 feature a One-Shot Temperature Measurement Mode. When the device is in Shutdown Mode, writing a '1' to the OS bit will start a single temperature conversion. The device will return to the shutdown state at the completion of the single conversion. This is useful to reduce power consumption in the TMP175 and TMP75 when continuous temperature monitoring is not required. When the configuration register is read, the OS will always read zero.

HIGH AND LOW LIMIT REGISTERS

In Comparator Mode (TM = 0), the ALERT pin of the TMP175 and TMP75 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin will remain active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In Interrupt Mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus Alert Response Address. The ALERT pin will also be cleared if the device is placed in Shutdown Mode. Once the ALERT pin is cleared, it will only become active again by the temperature falling below T_{LOW}. When the temperature falls below T_{LOW}, the ALERT pin will become active and remain active until cleared by a read operation of any register or a successful response to the SMBus Alert Response Address. Once the ALERT pin is cleared, the above cycle will repeat, with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the General Call Reset command. This will also clear the state of the internal registers in the device returning the device to Comparator Mode (TM = 0).

Both operational modes are represented in Figure 3. Table 9 and Table 10 describe the format for the T_{HIGH} and T_{LOW} registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up reset values for T_{HIGH} and T_{LOW} are:

$$T_{HIGH} = 80°C \text{ and } T_{LOW} = 75°C$$

The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register.

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	H3	H2	H1	H0	0	0	0	0

Table 9. Bytes 1 and 2 of T_{HIGH} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	L3	L2	L1	L0	0	0	0	0

Table 10. Bytes 1 and 2 of T_{LOW} Register

All 12 bits for the Temperature, T_{HIGH}, and T_{LOW} registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in T_{HIGH} and T_{LOW} can affect the ALERT output even if the converter is configured for 9-bit resolution.

SERIAL INTERFACE

The TMP175 and TMP75 operate only as slave devices on the Two-Wire bus and SMBus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP175 and TMP75 both support the transmission protocol for fast (1kHz to 400kHz) and high-speed (1kHz to 3.4MHz) modes. All data bytes are transmitted MSB first.

SERIAL BUS ADDRESS

To communicate with the TMP175 and TMP75, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The TMP175 features three address pins to allow up to 27 devices to be addressed on a single bus interface. Table 11 describes the pin logic levels used to properly connect up to 27 devices. '1' indicates the pin is connected to the supply (V_{CC}); '0' indicates the pin is connected to GND; *Float* indicates the pin is left unconnected. The state of pins A0, A1, and A2 is sampled on every bus communication and should be set prior to any activity on the interface.

The TMP75 features three address pins allowing up to eight devices to be connected per bus. Pin logic levels are described in Table 12. The address pins of the TMP175 and TMP75 are read after reset, at start of communication, or in response to a Two-Wire address acquire request. Following reading the state of the pins the address is latched to minimize power dissipation associated with detection.

A2	A1	A0	SLAVE ADDRESS
0	0	0	1001000
0	0	1	1001001
0	1	0	1001010
0	1	1	1001011
1	0	0	1001100
1	0	1	1001101
1	1	0	1001110
1	1	1	1001111
Float	0	0	1110000
Float	0	Float	1110001
Float	0	1	1110010
Float	1	0	1110011
Float	1	Float	1110100
Float	1	1	1110101
Float	Float	0	1110110
Float	Float	1	1110111
0	Float	0	0101000
0	Float	1	0101001
1	Float	0	0101010
1	Float	1	0101011
0	0	Float	0101100
0	1	Float	0101101
1	0	Float	0101110
1	1	Float	0101111
0	Float	Float	0110101
1	Float	Float	0110110
Float	Float	Float	0110111

Table 11. Address Pins and Slave Addresses for the TMP175

A2	A1	A0	SLAVE ADDRESS
0	0	0	1001000
0	0	1	1001001
0	1	0	1001010
0	1	1	1001011
1	0	0	1001100
1	0	1	1001101
1	1	0	1001110
1	1	1	1001111

Table 12. Address Pins and Slave Addresses for the TMP75

BUS OVERVIEW

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data-line (SDA) from a HIGH to LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge Bit. During data transfer SDA must remain stable while SCL is HIGH, as any change in SDA while SCL is HIGH will be interpreted as a control signal.

Once all data has been transferred, the master generates a STOP condition indicated by pulling SDA from LOW to HIGH, while SCL is HIGH.

WRITING/READING TO THE TMP175 AND TMP75

Accessing a particular register on the TMP175 and TMP75 is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit LOW. Every write operation to the TMP175 and TMP75 requires a value for the Pointer Register. (Refer to Figure 5.)

When reading from the TMP175 and TMP75, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit LOW, followed by the Pointer Register Byte. No additional data is required. The master can then generate a START condition and send the slave address byte with the R/$\overline{W}$ bit HIGH to initiate the read command. See Figure 7 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the Pointer Register bytes, as the TMP175 and TMP75 will remember the Pointer Register value until it is changed by the next write operation.

Note that register bytes are sent most-significant byte first, followed by the least significant byte.

SLAVE MODE OPERATIONS

The TMP175 and TMP75 can operate as slave receivers or slave transmitters.

Slave Receiver Mode:

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit LOW. The TMP175 or TMP75 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer Register. The TMP175 or TMP75 then acknowledges reception of the Pointer Register byte. The next byte or bytes are written to the register addressed by the Pointer Register. The TMP175 and TMP75 will acknowledge reception of each data byte. The master may terminate data transfer by generating a START or STOP condition.

Slave Transmitter Mode:

The first byte is transmitted by the master and is the slave address, with the R/$\overline{W}$ bit HIGH. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the Pointer Register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master may terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

SMBus ALERT FUNCTION

The TMP175 and TMP75 support the SMBus Alert function. When the TMP75 and TMP175 are operating in Interrupt Mode (TM = 1), the ALERT pin of the TMP75 or TMP175 may be connected as an SMBus Alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP75 or TMP175 is active, the devices will acknowledge the SMBus Alert command and respond by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte will indicate if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the ALERT condition. This bit will be HIGH if the temperature is greater than or equal to T_{HIGH}. This bit will be LOW if the temperature is less than T_{LOW}. Refer to Figure 8 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command will determine which device will clear its ALERT status. If the TMP75 or TMP175 wins the arbitration, its ALERT pin will become inactive at the completion of the SMBus Alert command. If the TMP75 or TMP175 loses the arbitration, its ALERT pin will remain active.

GENERAL CALL

The TMP175 and TMP75 respond to a Two-Wire General Call address (0000000) if the eighth bit is 0. The device will acknowledge the General Call address and respond to commands in the second byte. If the second byte is 00000100, the TMP175 and TMP75 will latch the status of their address pins, but will not reset. If the second byte is 00000110, the TMP175 and TMP75 will latch the status of their address pins and reset their internal registers to their power-up values.

HIGH-SPEED MODE

In order for the Two-Wire bus to operate at frequencies above 400kHz, the master device must issue an Hs-mode master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP175 and TMP75 will not acknowledge this byte, but will switch their input filters on SDA and SCL and their output filters on SDA to operate in Hs-mode, allowing transfers at up to 3.4MHz. After the Hs-mode master code has been issued, the master will transmit a Two-Wire slave address to initiate a data transfer operation. The bus will continue to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP175 and TMP75 will switch the input and output filter back to fast-mode operation.

TIMEOUT FUNCTION

The TMP175 and TMP75 will reset the serial interface if either SCL or SDA are held LOW for 54ms (typ) between a START and STOP condition. The TMP175 and TMP75 will release the bus if it is pulled LOW and will wait for a START condition. To avoid activating the timeout function, it is necessary to maintain a communication speed of at least 1kHz for SCL operating frequency.

TIMING DIAGRAMS

The TMP175 and TMP75 are Two-Wire and SMBus compatible. Figure 4 to Figure 8 describe the various operations on the TMP175 and TMP75. Bus definitions are given below. Parameters for Figure 4 are defined in Table 13.

Bus Idle: Both SDA and SCL lines remain HIGH.

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a Not-Acknowledge on the last byte that has been transmitted by the slave.

PARAMETER		FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
SCL Operating Frequency	$f_{(SCL)}$	0.001	0.4	0.001	3.4	MHz
Bus Free Time Between STOP and START Condition	$t_{(BUF)}$	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	100		100		ns
Repeated START Condition Setup Time	$t_{(SUSTA)}$	100		100		ns
STOP Condition Setup Time	$t_{(SUSTO)}$	100		100		ns
Data Hold Time	$t_{(HDDAT)}$	0		0		ns
Data Setup Time	$t_{(SUDAT)}$	100		10		ns
SCL Clock LOW Period	$t_{(LOW)}$	1300		160		ns
SCL Clock HIGH Period	$t_{(HIGH)}$	600		60		ns
Clock/Data Fall Time	t_F		300		160	ns
Clock/Data Rise Time for SCLK ≤ 100kHz	t_R t_R		300 1000		160	ns ns

Table 13. Timing Diagram Definitions for the TMP175 and TMP75

TWO-WIRE TIMING DIAGRAMS

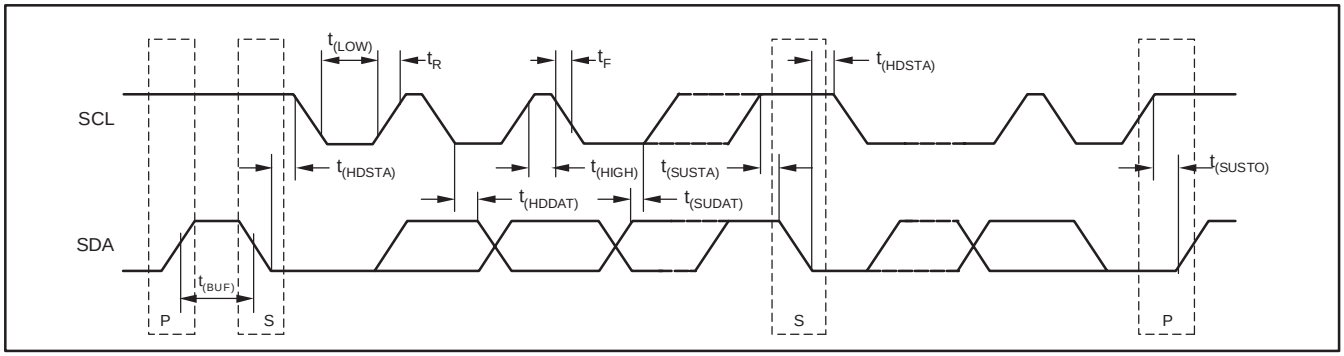


Figure 4. Two-Wire Timing Diagram

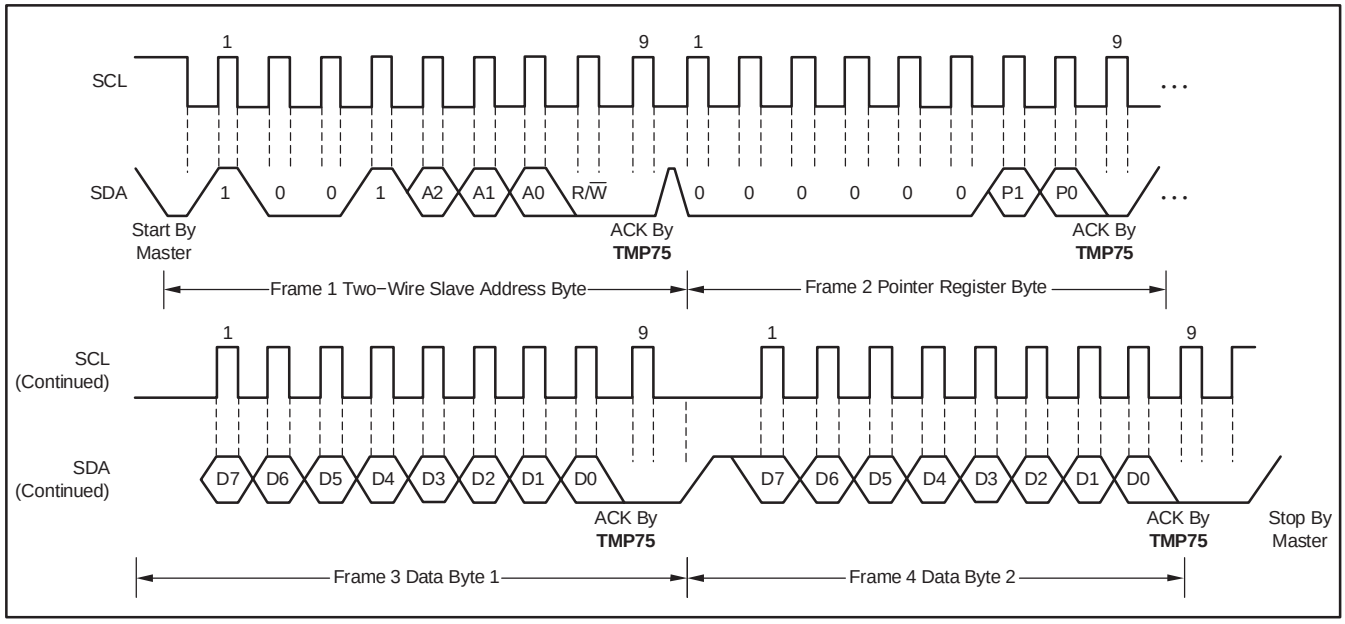


Figure 5. Two-Wire Timing Diagram for TMP75 Write Word Format

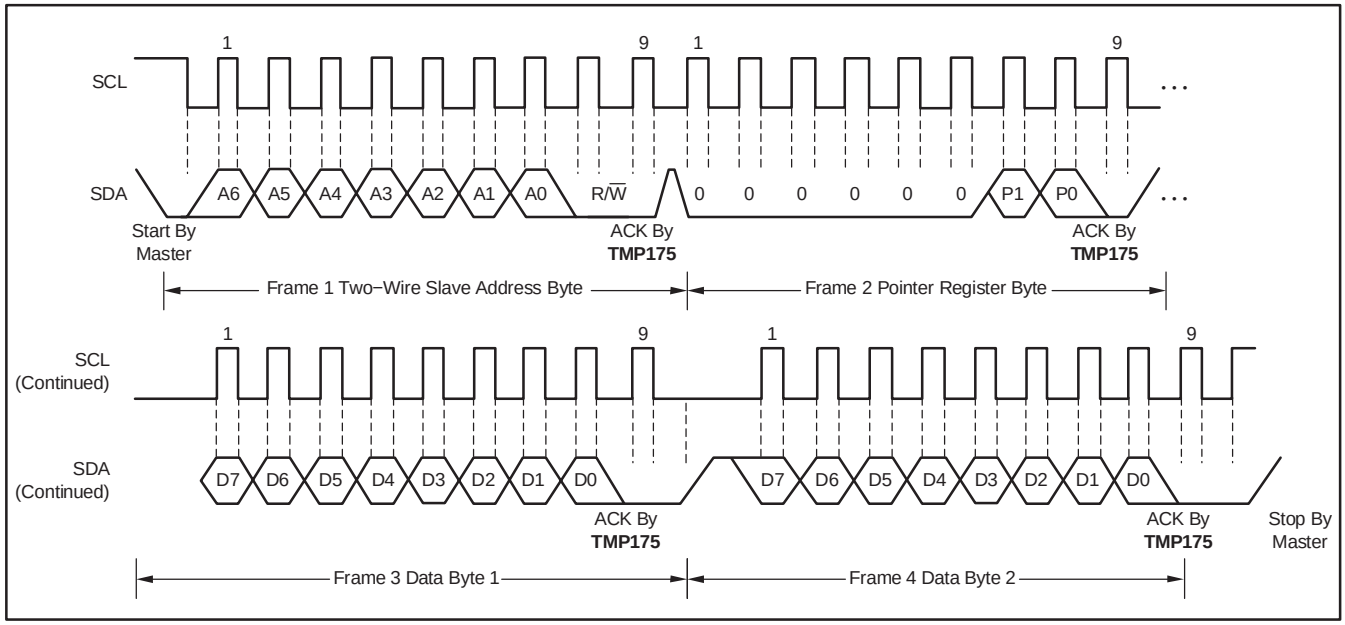


Figure 6. Two-Wire Timing Diagram for TMP175 Write Word Format

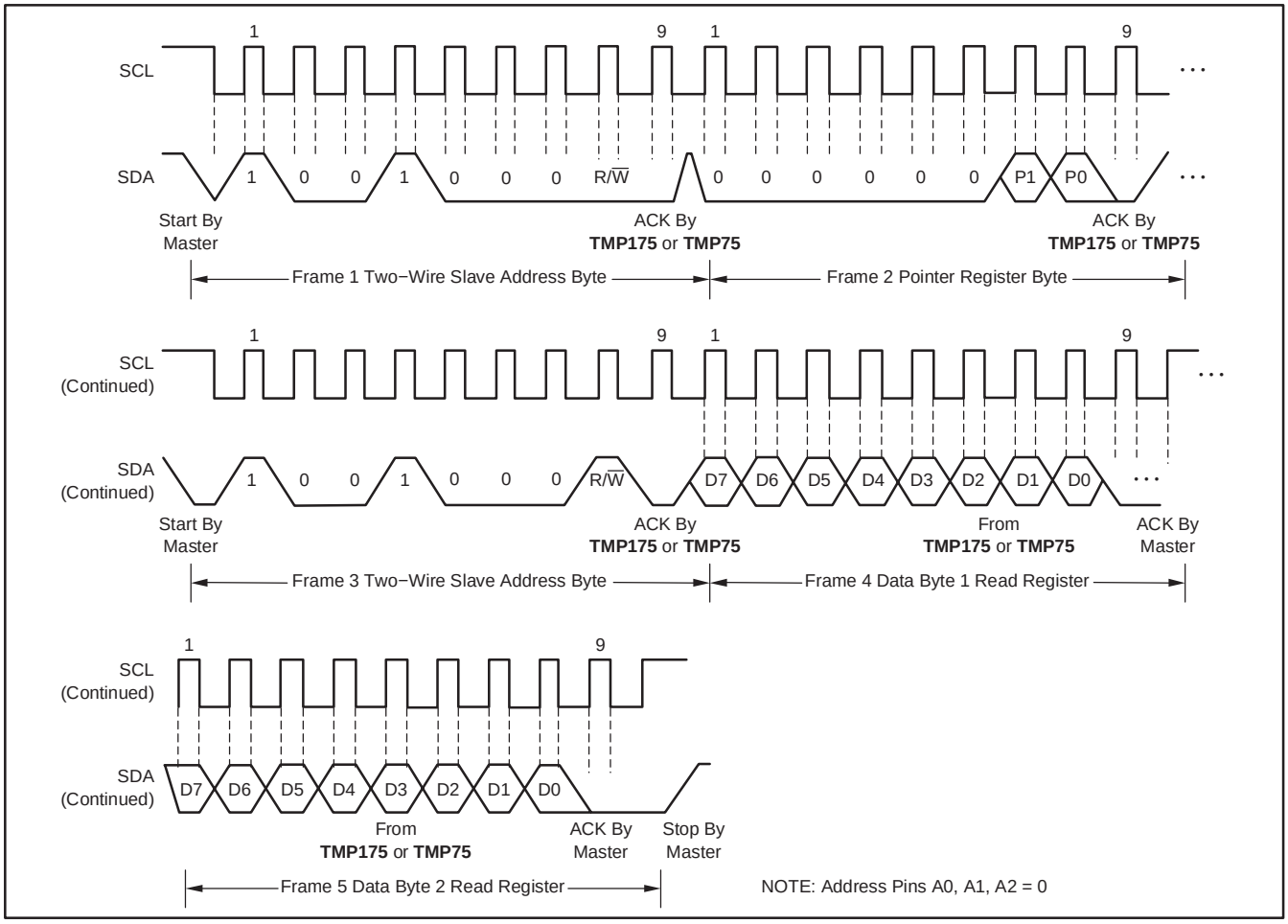


Figure 7. Two-Wire Timing Diagram for Read Word Format

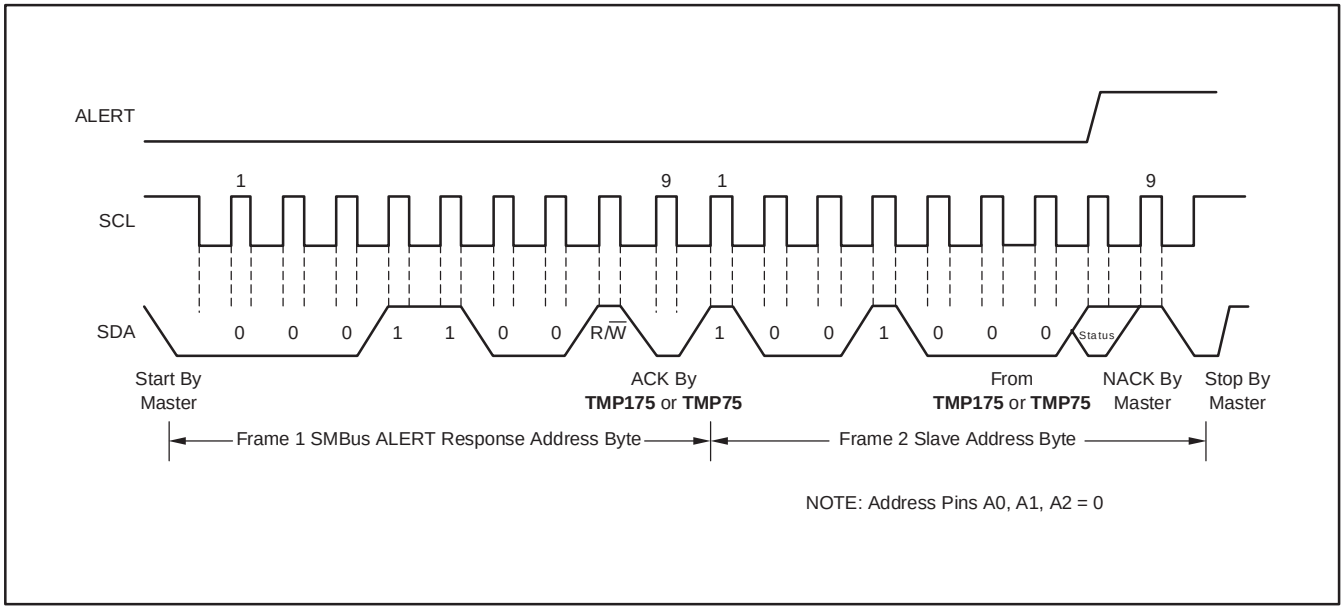


Figure 8. Timing Diagram for SMBus ALERT

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TMP175AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	
TMP175AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	
TMP175AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TMP175AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TMP175AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TMP175AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TMP175AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TMP175AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TMP75AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	
TMP75AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	
TMP75AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TMP75AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TMP75AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TMP75AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TMP75AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	
TMP75AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

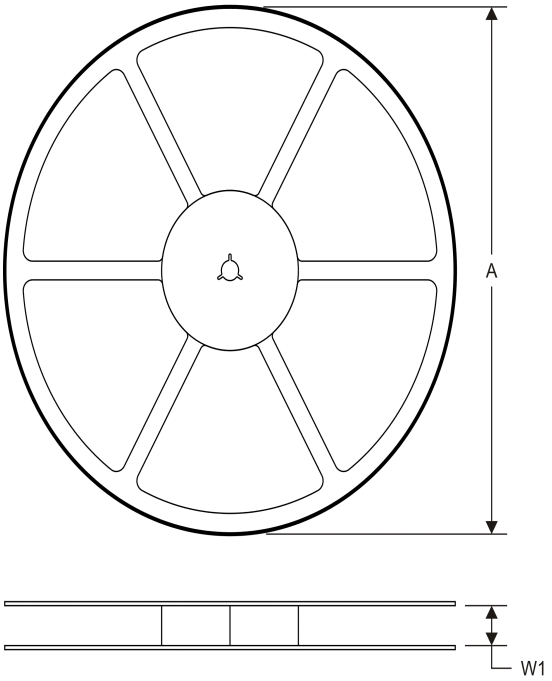
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

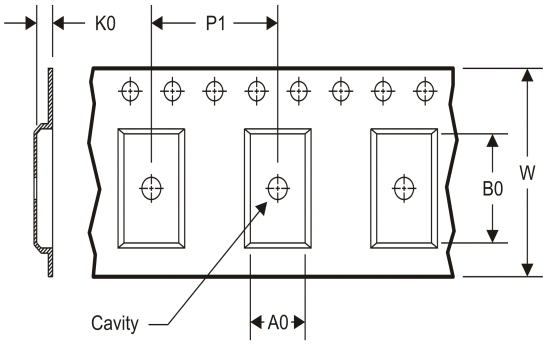
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



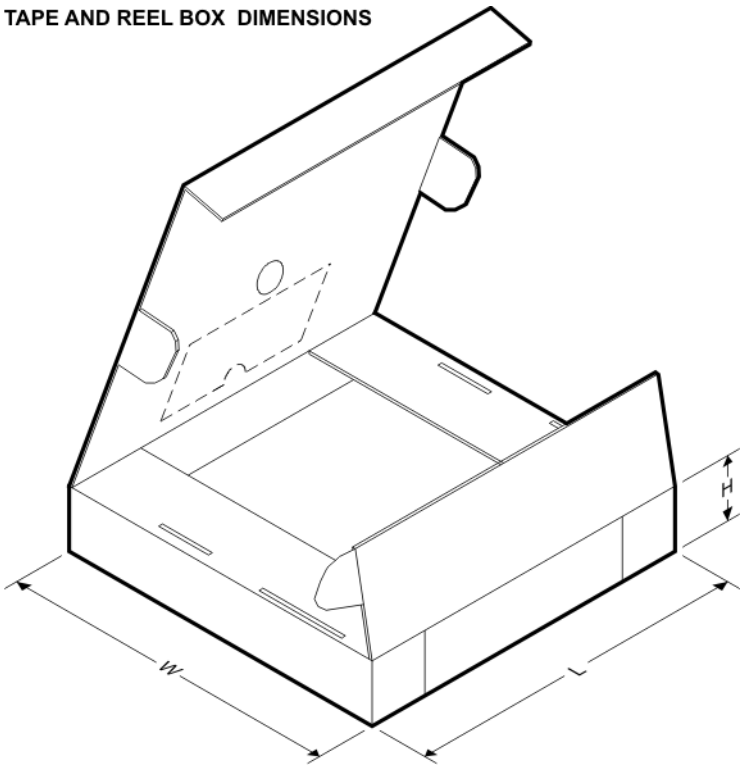
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP175AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP175AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TMP175AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TMP175AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP175AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TMP75AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP75AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP75AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

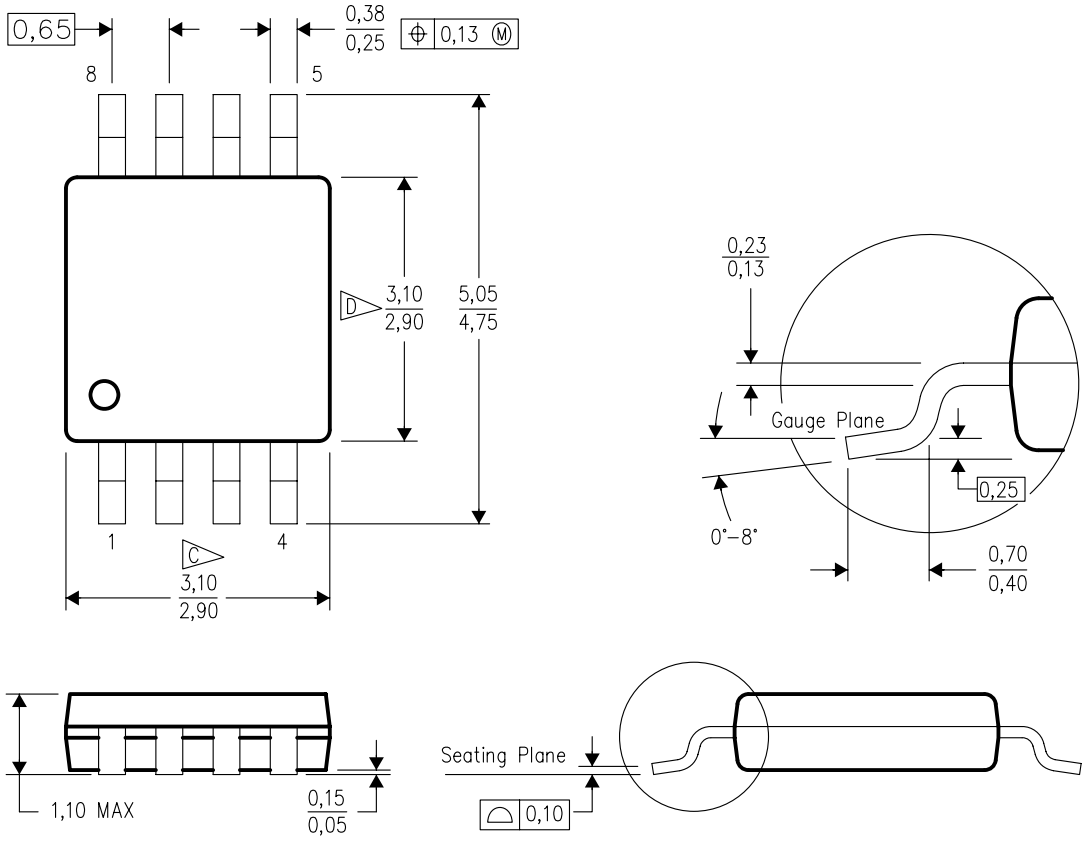
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP175AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP175AIDGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
TMP175AIDGKT	VSSOP	DGK	8	250	195.0	200.0	45.0
TMP175AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TMP175AIDR	SOIC	D	8	2500	367.0	367.0	35.0
TMP75AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP75AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TMP75AIDR	SOIC	D	8	2500	367.0	367.0	35.0

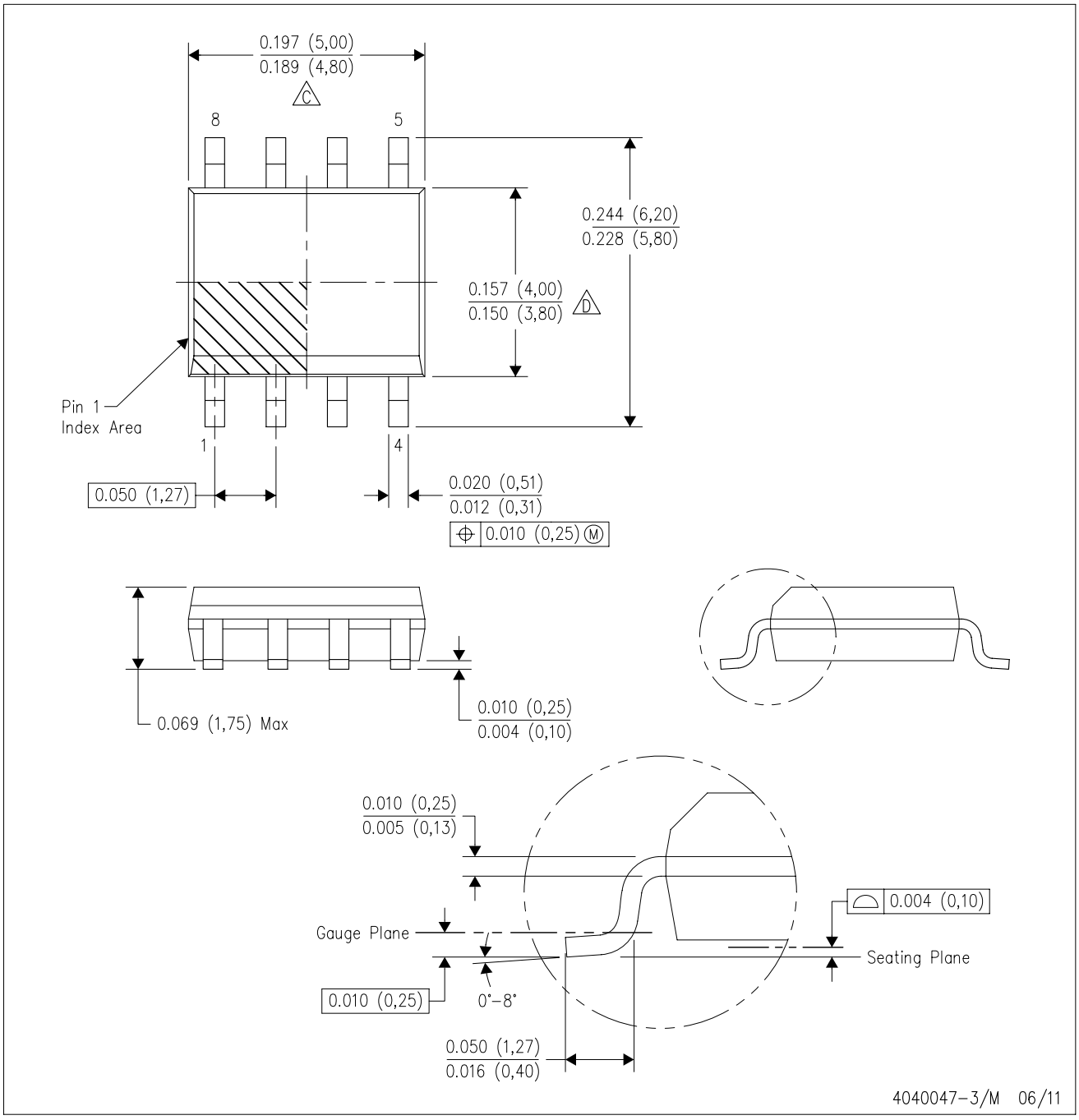
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

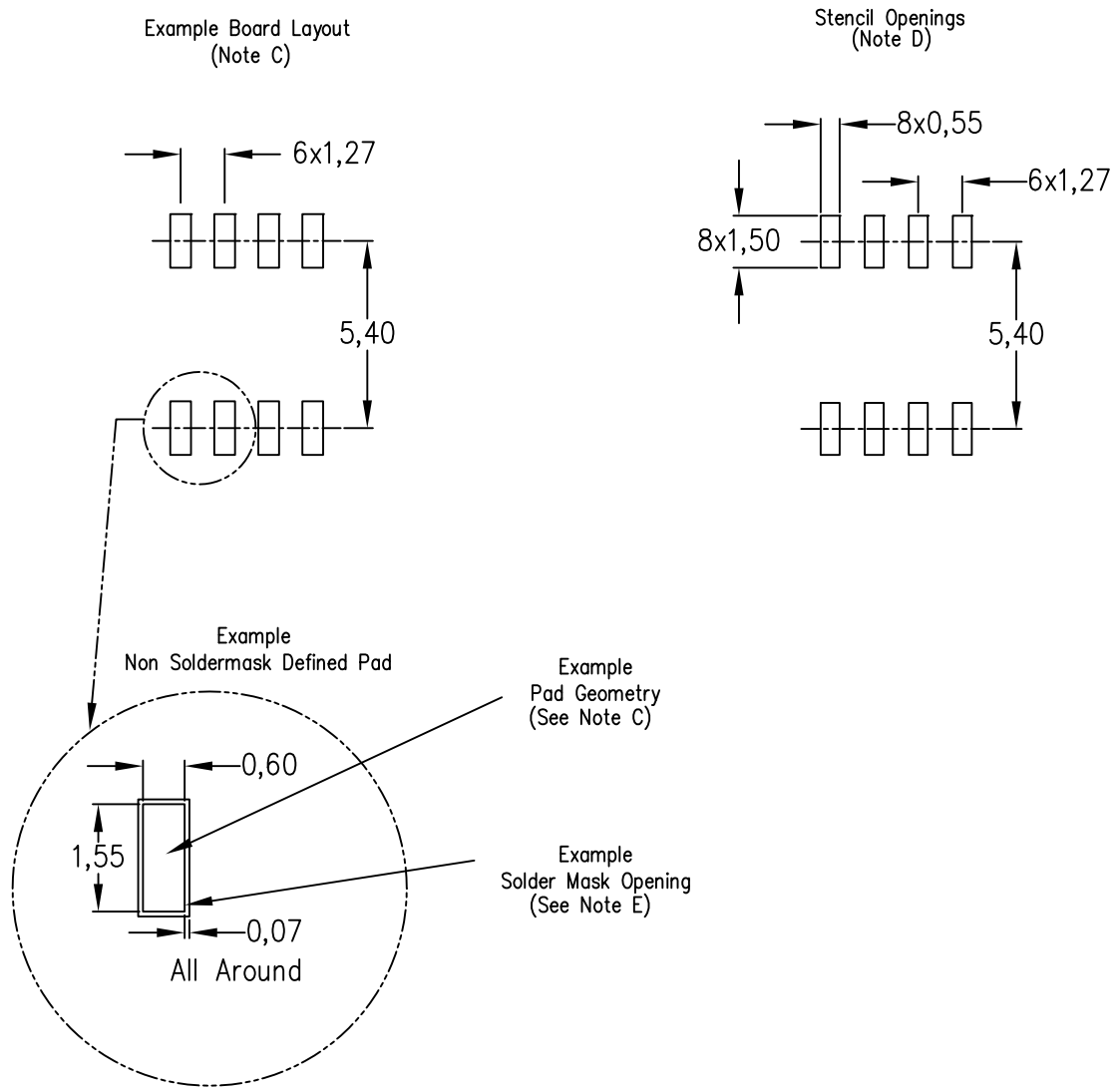
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

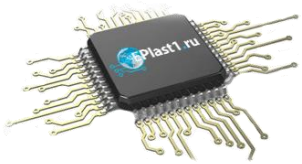
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.