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# MB9B160R Series

# 32-bit ARM® Cortex®-M4F FM4 Microcontroller

The MB9B160R Series are a highly integrated 32-bit microcontrollers dedicated for embedded controllers with high-performance and competitive cost.

These series are based on the ARM® Cortex®-M4F Processor with on-chip Flash memory and SRAM, and has peripheral functions such as Motor Control Timers, ADCs and Communication Interfaces (UART, CSIO, $I^2C$, LIN).

## Features

### 32-bit ARM® Cortex®-M4F Core

- Processor version: r0p1
- Up to 160 MHz Frequency Operation
- FPU built-in
- Support DSP instruction
- Memory Protection Unit (MPU): improves the reliability of an embedded system
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

### On-chip Memories

#### [Flash memory]

These series are based on two independent on-chip Flash memories.

- MainFlash memory
  - Up to 1024 Kbytes
  - Built-in Flash Accelerator System with 16 Kbytes trace buffer memory
  - The read access to Flash memory can be achieved without wait-cycle up to operation frequency of 72 MHz. Even at the operation frequency more than 72 MHz, an equivalent access to Flash memory can be obtained by Flash Accelerator System.
  - Security function for code protection
- WorkFlash memory
  - 32 Kbytes
  - Read cycle:
    - 6 wait-cycle: the operation frequency more than 120 MHz, and up to 160 MHz
    - 4 wait-cycle: the operation frequency more than 72 MHz, and up to 120 MHz
    - 2 wait-cycle: the operation frequency more than 40 MHz, and up to 72 MHz
    - 0 wait-cycle: the operation frequency up to 40 MHz
  - Security function is shared with code protection

#### [SRAM]

This is composed of three independent SRAMs (SRAM0, SRAM1 and SRAM2). SRAM0 is connected to I-code bus or D-code bus of Cortex-M4F core. SRAM1 and SRAM2 are connected to System bus of Cortex-M4F core.

- SRAM0: Up to 64 Kbytes
- SRAM1: Up to 32 Kbytes
- SRAM2: Up to 32 Kbytes

### External Bus Interface

- Supports SRAM, NOR, NAND Flash and SDRAM device
- Up to 9 chip selects CS0 to CS8 (CS8 is only for SDRAM)
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Maximum Access size: 256M byte
- Supports Address/Data multiplex
- Supports external RDY function
- Supports scramble function
- Possible to set the validity/invalidity of the scramble function for the external areas 0x6000_0000 to 0xDFFF_FFFF in 4 Mbytes units.
- Possible to set two kinds of the scramble key
- Note: It is necessary to prepare the dedicated software library to use the scramble function.

### Multi-function Serial Interface (Max 8 channels)

- 64 bytes with FIFO (the FIFO step numbers are variable depending on the settings of the communication mode or bit length.)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - $I^2C$

### [UART]

- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

### [CSIO]

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detect function available
- Serial chip select function (ch.6 and ch.7 only)
- Supports high-speed SPI (ch.4 and ch.6 only)
- Data length 5 to 16-bit

### [LIN]

- LIN protocol Rev.2.1 supported
- Full-duplex double buffer
- Master/Slave mode supported
- LIN break field generation (can change to 13 to 16-bit length)
- LIN break delimiter generation (can change to 1 to 4-bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

### [$I^2C$]

- Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported
- Fast-mode Plus (Fm+) (Max 1000 kbps, only for ch.3 = ch.A and ch.7 = ch.B) supported

## DMA Controller (8 channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

## DSTC (Descriptor System data Transfer Controller) (128 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor system and, following the specified contents of the Descriptor which has already been constructed on the memory, can access directly the memory /peripheral device and performs the data transfer operation.

It supports the software activation, the hardware activation and the chain activation functions.

## A/D Converter (Max 24 channels)

### [12-bit A/D Converter]

- Successive Approximation type
- Built-in 3 units
- Conversion time: 0.5 µs @ 5 V
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

## DA converter (Max 2 channels)

- R-2R type
- 12-bit resolution

## Base Timer (Max 8 channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

## General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 100 high-speed general-purpose I/O ports @ 120 pin Package
- Some pin is 5V tolerant I/O.
- See “Pin Description” and “I/O Circuit Type” for the corresponding pins.

### Multi-function Timer (Max 2 units)

The Multi-function timer is composed of the following blocks.

Minimum resolution: 6.25 ns

- 16-bit free-run timer × 3 ch./unit
- Input capture × 4 ch./unit
- Output compare × 6 ch./unit
- A/D activation compare × 6 ch./unit
- Waveform generator × 3 ch./unit
- 16-bit PPG timer × 3 ch./unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

### Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- Interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

### Quadrature Position/Revolution Counter (QPRC) (Max 2 channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

### Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic ( = Reload)
- One-shot

### Watch Counter

The Watch counter is used for wake up from the low-power consumption mode. It is possible to select the main clock, sub clock, built-in high-speed CR clock or built-in low-speed CR clock as the clock source.

Interval timer: up to 64s (Max) @ Sub Clock: 32.768 kHz

### External Interrupt Controller Unit

- External interrupt input pin: Max 16 pins
- Include one non-maskable interrupt (NMI)

### Watchdog Timer (2 channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

"Hardware" watchdog timer is clocked by low-speed internal CR oscillator. Therefore, "Hardware" watchdog is active in any power saving mode except STOP.

### CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

### SD Card Interface

It is possible to use the SD card that conforms to the following standards.

- Part 1 Physical Layer Specification version 3.01
- Part E1 SDIO Specification version 3.00
- Part A2 SD Host Controller Standard Specification version 3.00
- 1-bit or 4-bit data bus

## Clock and Reset

### [Clocks]

Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

- Main clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- High-speed internal CR Clock: 4 MHz
- Low-speed internal CR Clock: 100 kHz
- Main PLL Clock

### [Resets]

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timers reset
- Low voltage detector reset
- Clock supervisor reset

## Clock Super Visor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

## Low-Voltage Detector (LVD)

This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

## Low-power Consumption Mode

Six low-power consumption modes are supported.

- SLEEP
- TIMER
- RTC
- STOP
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

## VBAT

The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32 kHz oscillation circuit
- Power-on circuit
- Back up register: 32 bytes
- Port circuit

## Debug

- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

## Unique ID

Unique value of the device (41-bit) is set.

## Power Supply

Two Power Supplies

- Wide range voltage: VCC = 2.7 V to 5.5 V
- Power supply for VBAT: VBAT = 2.7 V to 5.5 V

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# 1. Product Lineup

## Memory Size

| Product name | | MB9BF166M/N/R | MB9BF167M/N/R | MB9BF168M/N/R |
|---|---|---|---|---|
| MainFlash memory | | 512 Kbytes | 768 Kbytes | 1024 Kbytes |
| WorkFlash memory | | 32 Kbytes | 32 Kbytes | 32 Kbytes |
| On-chip SRAM | | 64 Kbytes | 96 Kbytes | 128 Kbytes |
| | SRAM0 | 32 Kbytes | 48 Kbytes | 64 Kbytes |
| | SRAM1 | 16 Kbytes | 24 Kbytes | 32 Kbytes |
| | SRAM1 | 16 Kbytes | 24 Kbytes | 32 Kbytes |

## Function

| Product name | | | MB9BF166M<br>MB9BF167M<br>MB9BF168M | MB9BF166N<br>MB9BF167N<br>MB9BF168N | MB9BF166R<br>MB9BF167R<br>MB9BF168R |
|---|---|---|---|---|---|
| Pin count | | | 80 | 100/112 | 120/144 |
| CPU | | | Cortex-M4F, MPU, NVIC 128ch. | | |
| | Freq. | | 160 MHz | | |
| Power supply voltage range | | | 2.7 V to 5.5 V | | |
| DMAC | | | 8 ch. | | |
| DSTC | | | 128 ch. | | |
| External Bus Interface | | | Addr:19-bit (Max),<br>R/W data: 8-bit (Max),<br>CS:5 (Max),<br>SRAM,<br>NOR Flash | Addr:25-bit (Max),<br>R/W data: 8-/16-bit (Max),<br>CS:9 (Max),<br>SRAM,<br>NOR Flash,<br>SDRAM | Addr:25-bit (Max),<br>R/W data: 8-/16-bit (Max),<br>CS:9 (Max),<br>SRAM,<br>NOR Flash,<br>NAND Flash, SDRAM |
| Multi-function Serial Interface (UART/CSIO/LIN/I$^2$C) | | | 8 ch. (Max) | | |
| Base Timer<br>(PWC/Reload timer/PWM/PPG) | | | 8 ch. (Max) | | |
| MF Timer | A/D activation compare | 6 ch. | 2 units (Max) | | |
| | Input capture | 4 ch. | | | |
| | Free-run timer | 3 ch. | | | |
| | Output compare | 6 ch. | | | |
| | Waveform generator | 3 ch. | | | |
| | PPG | 3 ch. | | | |
| SD Card Interface | | | 1 unit | | |
| QPRC | | | 2 ch. (Max) | | |
| Dual Timer | | | 1 unit | | |
| Real-Time Clock | | | 1 unit | | |
| Watch Counter | | | 1 unit | | |
| CRC Accelerator | | | Yes | | |
| Watchdog Timer | | | 1 ch. (SW) + 1 ch. (HW) | | |
| External Interrupts | | | 16 pins (Max) + NMI × 1 | | |
| I/O Ports | | | 63 pins (Max) | 80 pins (Max) | 100 pins (Max) |
| 12-bit A/D Converter | | | 16 ch. (3 units) | 24 ch. (3 units) | |
| 12-bit D/A Converter | | | 2 units (Max) | | |
| CSV (Clock Super Visor) | | | Yes | | |
| LVD (Low-Voltage Detector) | | | 2 ch. | | |
| Built-in CR | High-speed | | 4 MHz | | |
| | Low-speed | | 100 kHz | | |
| Debug Function | | | SWJ-DP/ETM | | |
| Unique ID | | | Yes | | |

***Notes:***

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
- *See "12. Electrical Characteristics 12.4. AC* Characteristics *12.4.3.* Built-in *CR Oscillation Characteristics" for accuracy of built-in CR.*

## 2. Packages

| Package \ Product name | MB9BF166M<br>MB9BF167M<br>MB9BF168M | MB9BF166N<br>MB9BF167N<br>MB9BF168N | MB9BF166R<br>MB9BF167R<br>MB9BF168R |
|---|---|---|---|
| LQFP: LQH080 (0.5 mm pitch) | ❍ | - | - |
| LQFP: LQJ080 (0.65 mm pitch) | ❍ | - | - |
| QFP: PQH100 (0.65 mm pitch) | - | ❍ | - |
| LQFP: LQI100 (0.5 mm pitch) | - | ❍ | - |
| LQFP: LQM120 (0.5 mm pitch) | - | - | ❍ |
| BGA: LDC112 (0.5 mm pitch) | - | ❍ | - |
| BGA: LDC144 (0.5 mm pitch) | - | - | ❍ |

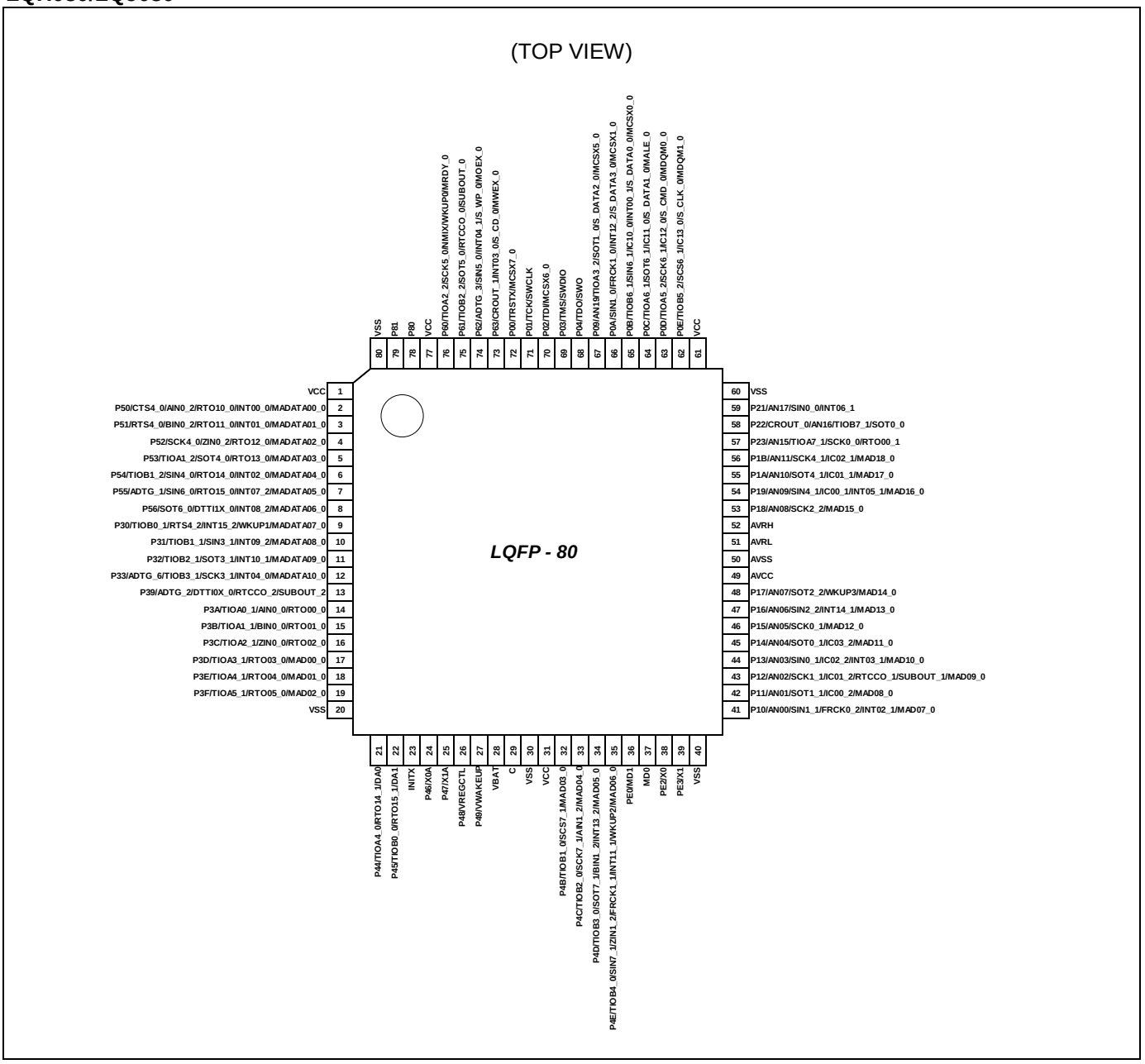
❍: Supported

***Note:***

- *See "Package Dimensions" for detailed information on each package.*

# 3. Pin Assignment

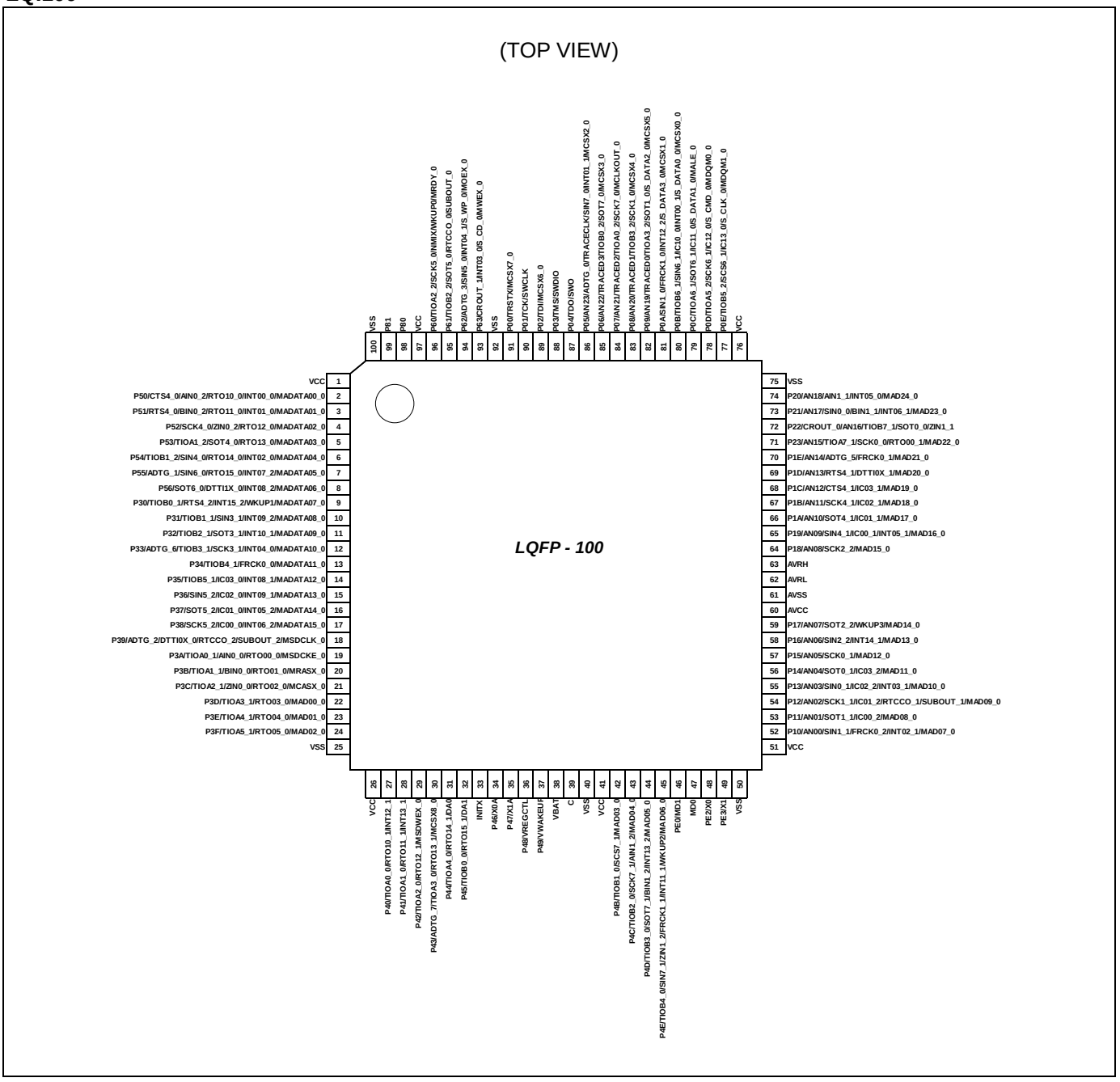
## LQH080/LQJ080




***Note:***

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

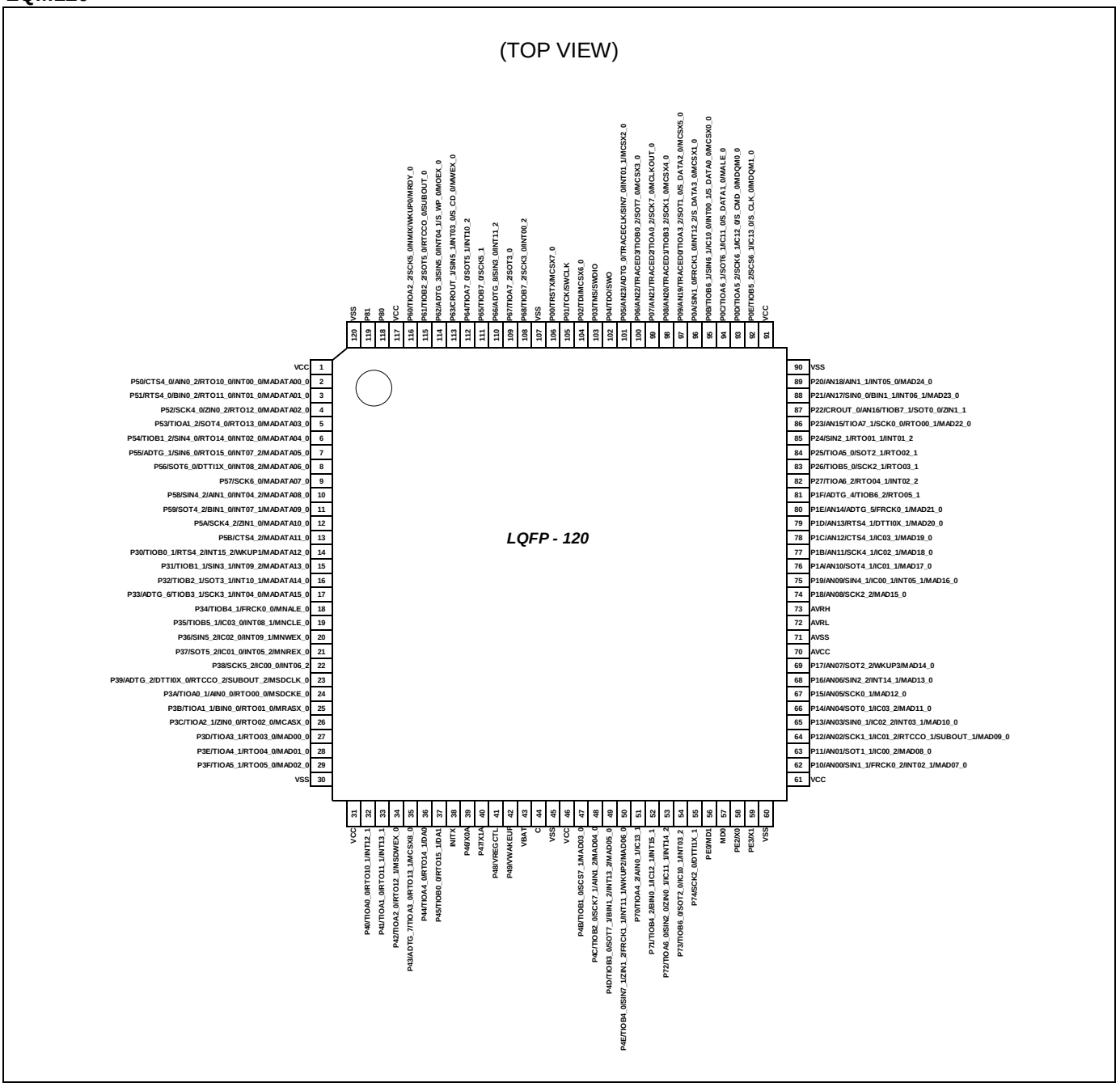
## LQI100




***Note:***

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

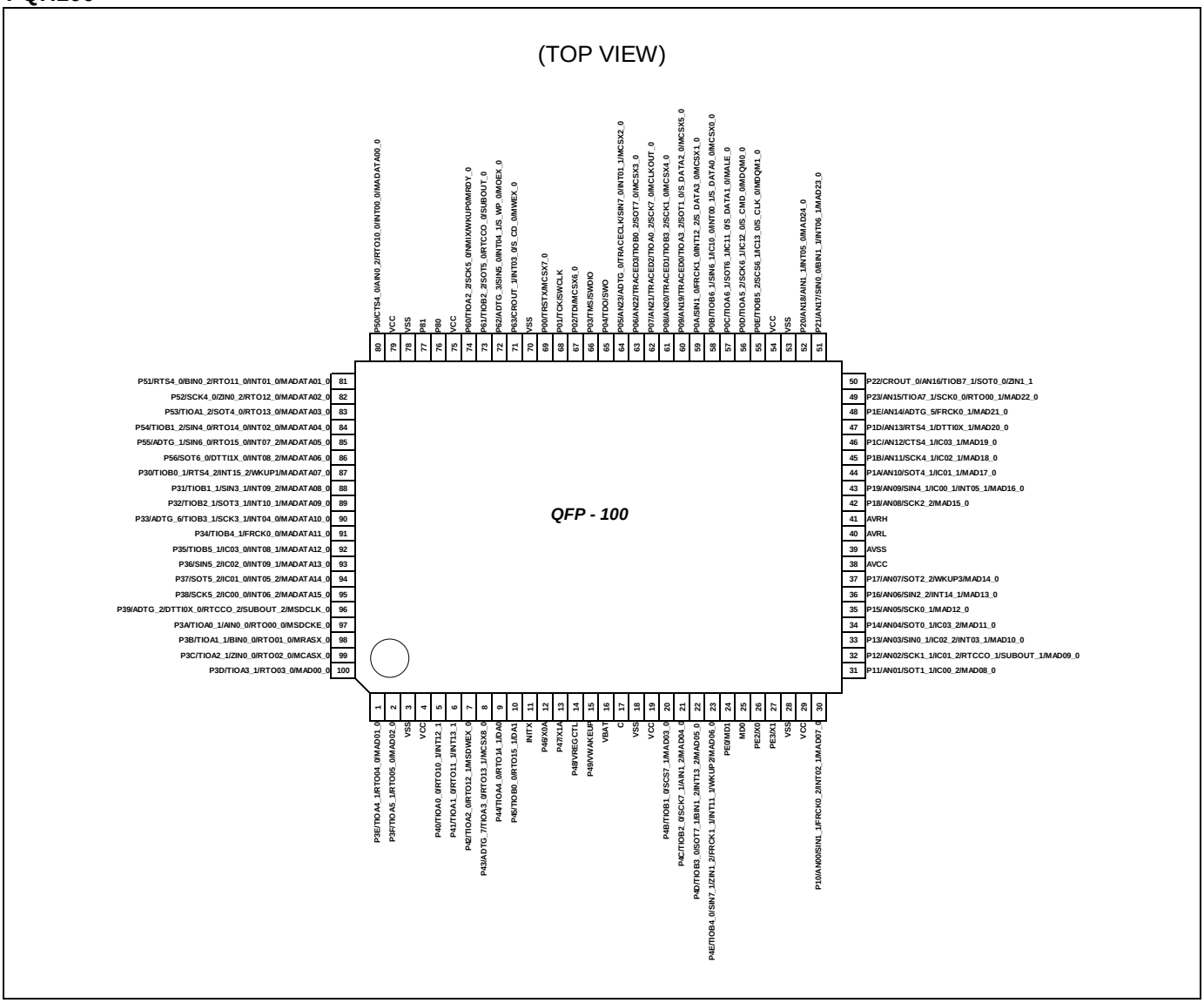
## LQM120




***Note:***

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

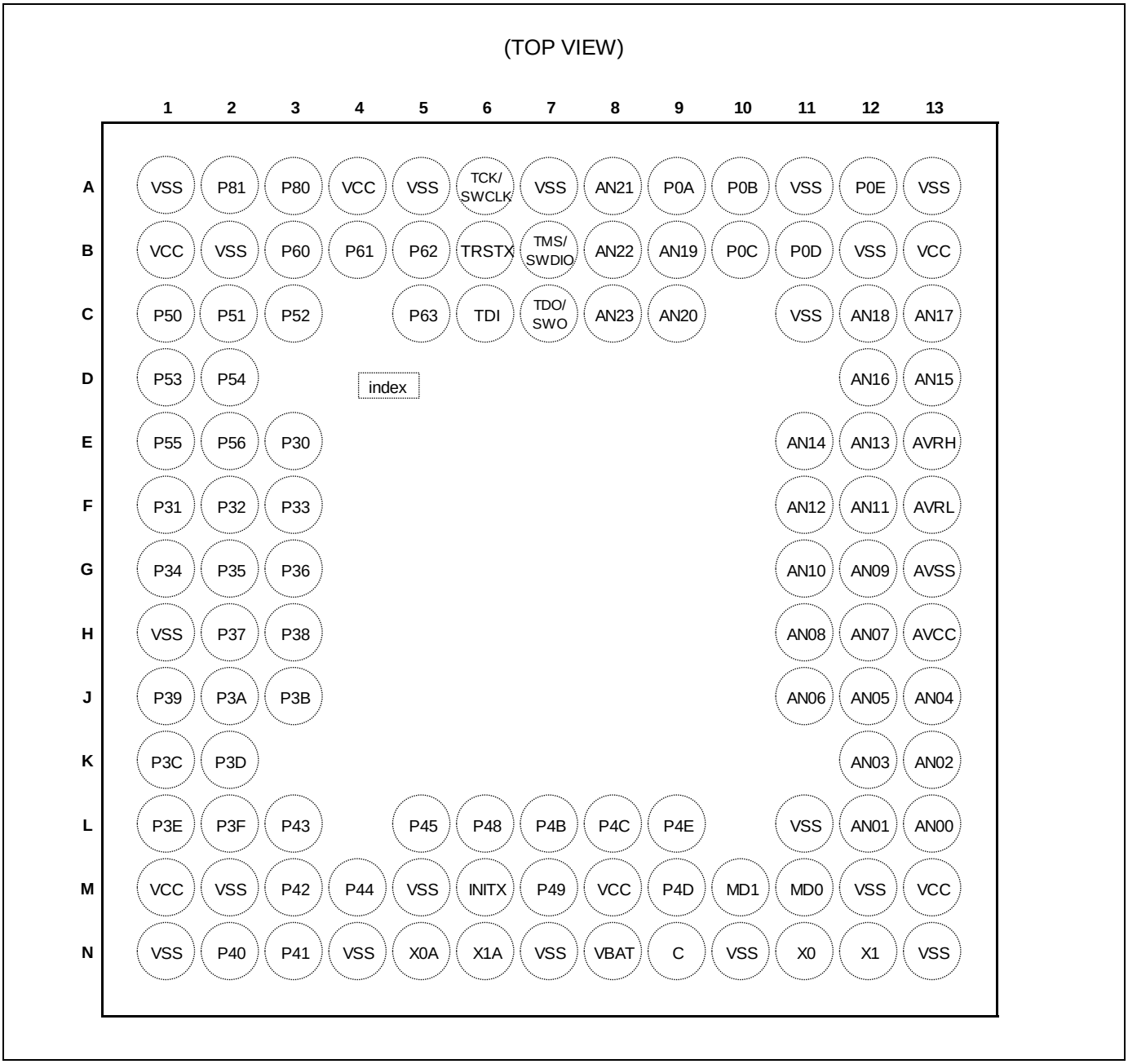
## PQH100




***Note:***

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

**LDC112**

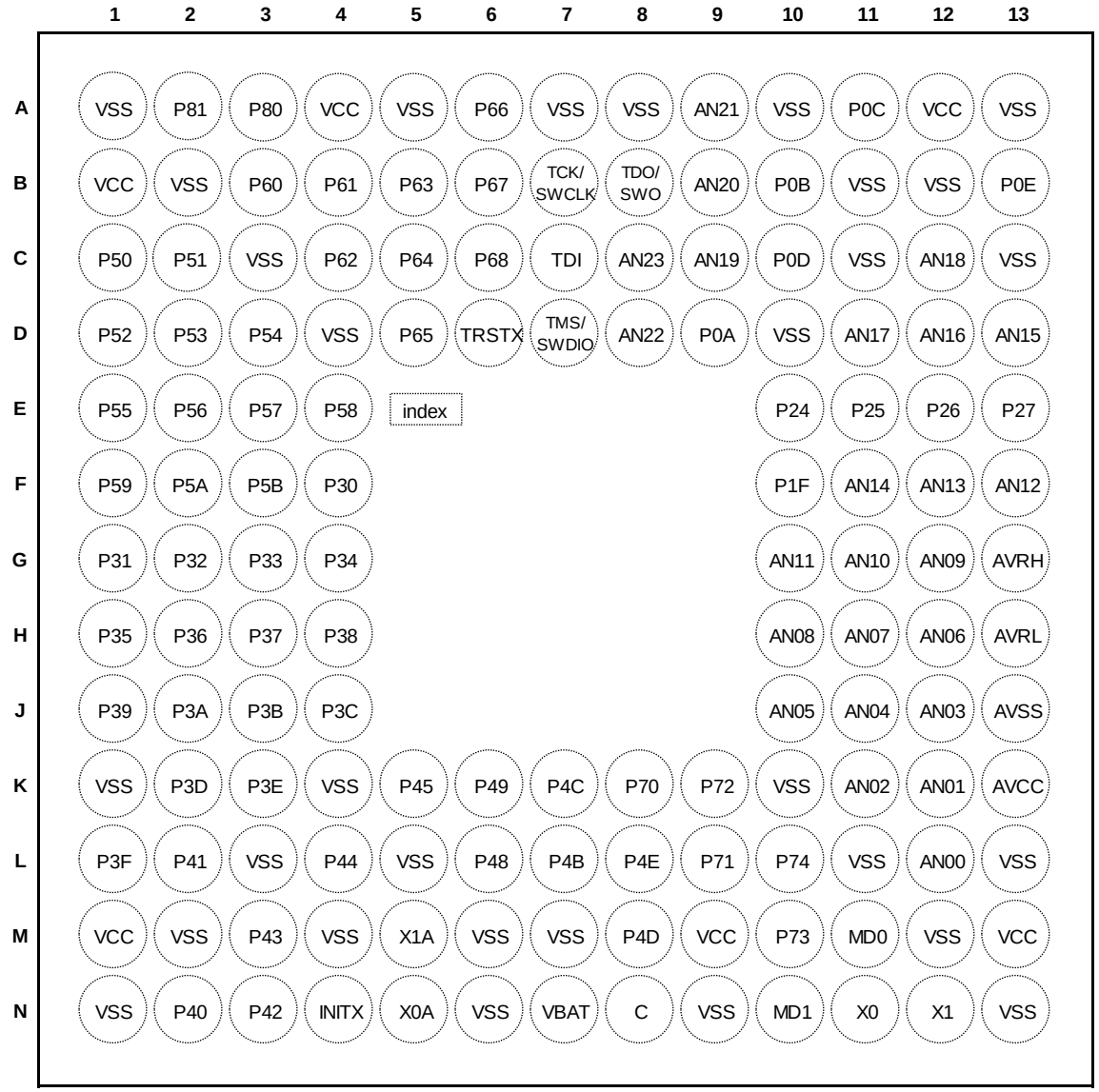



***Note:***

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

**LDC144**

(TOP VIEW)




***Note:***

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

# 4. Pin Description

### List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

| Pin No | | | | | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|---|---|
| LQFP120 | LQFP100 | LQFP80 | QFP100 | BGA112 | BGA144 | | | |
| 1 | 1 | 1 | 79 | B1 | B1 | VCC | - | - |
| 2 | 2 | 2 | 80 | C1 | C1 | P50<br>CTS4_0<br>AIN0_2<br>RTO10_0 (PPG10_0)<br>INT00_0<br>MADATA00_0 | E | K |
| 3 | 3 | 3 | 81 | C2 | C2 | P51<br>RTS4_0<br>BIN0_2<br>RTO11_0 (PPG10_0)<br>INT01_0<br>MADATA01_0 | E | K |
| 4 | 4 | 4 | 82 | C3 | D1 | P52<br>SCK4_0 (SCL4_0)<br>ZIN0_2<br>RTO12_0 (PPG12_0)<br>MADATA02_0 | E | I |
| 5 | 5 | 5 | 83 | D1 | D2 | P53<br>TIOA1_2<br>SOT4_0 (SDA4_0)<br>RTO13_0 (PPG12_0)<br>MADATA03_0 | E | I |
| 6 | 6 | 6 | 84 | D2 | D3 | P54<br>TIOB1_2<br>SIN4_0<br>RTO14_0 (PPG14_0)<br>INT02_0<br>MADATA04_0 | E | K |
| 7 | 7 | 7 | 85 | E1 | E1 | P55<br>ADTG_1<br>SIN6_0<br>RTO15_0 (PPG14_0)<br>INT07_2<br>MADATA05_0 | E | K |

| Pin No | | | | | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|---|---|
| LQFP120 | LQFP100 | LQFP80 | QFP100 | BGA112 | BGA144 | | | |
| 8 | 8 | 8 | 86 | E2 | E2 | P56<br>SOT6_0 (SDA6_0)<br>DTTI1X_0<br>INT08_2<br>MADATA06_0 | E | K |
| 9 | - | - | - | - | E3 | P57<br>SCK6_0 (SCL6_0)<br>MADATA07_0 | E | I |
| 10 | - | - | - | - | E4 | P58<br>SIN4_2<br>AIN1_0<br>INT04_2<br>MADATA08_0 | E | K |
| 11 | - | - | - | - | F1 | P59<br>SOT4_2 (SDA4_2)<br>BIN1_0<br>INT07_1<br>MADATA09_0 | E | K |
| 12 | - | - | - | - | F2 | P5A<br>SCK4_2 (SCL4_2)<br>ZIN1_0<br>MADATA10_0 | E | I |
| 13 | - | - | - | - | F3 | P5B<br>CTS4_2<br>MADATA11_0 | E | I |
| 14 | 9 | 9 | 87 | E3 | F4 | P30<br>TIOB0_1<br>RTS4_2<br>INT15_2<br>WKUP1 | E | Q |
| - | | | | | - | MADATA07_0 | | |
| 14 | - | - | - | - | F4 | MADATA12_0 | | |
| 15 | 10 | 10 | 88 | F1 | G1 | P31<br>TIOB1_1<br>SIN3_1<br>INT09_2 | I | K |
| - | | | | | - | MADATA08_0 | | |
| 15 | - | - | - | - | G1 | MADATA13_0 | | |

| Pin No | | | | | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|---|---|
| LQFP120 | LQFP100 | LQFP80 | QFP100 | BGA112 | BGA144 | | | |
| 16 | 11 | 11 | 89 | F2 | G2 | P32 | N | K |
| | | | | | | TIOB2_1 | | |
| | | | | | | SOT3_1 (SDA3_1) | | |
| | | | | | | INT10_1 | | |
| - | | | | | - | MADATA09_0 | | |
| 16 | - | - | - | - | G2 | MADATA14_0 | | |
| 17 | 12 | 12 | 90 | F3 | G3 | P33 | N | K |
| | | | | | | ADTG_6 | | |
| | | | | | | TIOB3_1 | | |
| | | | | | | SCK3_1 (SCL3_1) | | |
| | | | | | | INT04_0 | | |
| - | | | | | - | MADATA10_0 | | |
| 17 | - | - | - | - | G3 | MADATA15_0 | | |
| 18 | 13 | - | 91 | G1 | G4 | P34 | E | I |
| | | | | | | TIOB4_1 | | |
| | | | | | | FRCK0_0 | | |
| - | | | | | - | MADATA11_0 | | |
| 18 | - | - | - | - | G4 | MNALE_0 | | |
| 19 | 14 | - | 92 | G2 | H1 | P35 | E | K |
| | | | | | | TIOB5_1 | | |
| | | | | | | IC03_0 | | |
| | | | | | | INT08_1 | | |
| - | | | | | - | MADATA12_0 | | |
| 19 | - | - | - | - | H1 | MNCLE_0 | | |

| Pin No | | | | | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|---|---|
| LQFP120 | LQFP100 | LQFP80 | QFP100 | BGA112 | BGA144 | | | |
| 20 | 15 | - | 93 | G3 | H2 | P36<br>SIN5_2<br>IC02_0<br>INT09_1 | E | K |
| - | | | | | - | MADATA13_0 | | |
| 20 | - | - | - | - | H2 | MNWEX_0 | | |
| 21 | 16 | - | 94 | H2 | H3 | P37<br>SOT5_2 (SDA5_2)<br>IC01_0<br>INT05_2 | E | K |
| - | | | | | - | MADATA14_0 | | |
| 21 | - | - | - | - | H3 | MNREX_0 | | |
| 22 | 17 | - | 95 | H3 | H4 | P38<br>SCK5_2 (SCL5_2)<br>IC00_0<br>INT06_2 | E | K |
| - | | | | | - | MADATA15_0 | | |
| 23 | 18 | 13 | 96 | J1 | J1 | P39<br>ADTG_2<br>DTTI0X_0<br>RTCCO_2<br>SUBOUT_2 | L | I |
| | | - | | | | MSDCLK_0 | | |
| 24 | 19 | 14 | 97 | J2 | J2 | P3A<br>TIOA0_1<br>AIN0_0<br>RTO00_0 (PPG00_0) | G | I |
| | | - | | | | MSDCKE_0 | | |
| 25 | 20 | 15 | 98 | J3 | J3 | P3B<br>TIOA1_1<br>BIN0_0<br>RTO01_0 (PPG00_0) | G | I |
| | | - | | | | MRASX_0 | | |

| Pin No | | | | | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|---|---|
| LQFP120 | LQFP100 | LQFP80 | QFP100 | BGA112 | BGA144 | | | |
| 26 | 21 | 16 | 99 | K1 | J4 | P3C<br>TIOA2_1<br>ZIN0_0<br>RTO02_0 (PPG02_0) | G | I |
| | | - | | | | MCASX_0 | | |
| 27 | 22 | 17 | 100 | K2 | K2 | P3D<br>TIOA3_1<br>RTO03_0 (PPG02_0)<br>MAD00_0 | G | I |
| 28 | 23 | 18 | 1 | L1 | K3 | P3E<br>TIOA4_1<br>RTO04_0 (PPG04_0)<br>MAD01_0 | G | I |
| 29 | 24 | 19 | 2 | L2 | L1 | P3F<br>TIOA5_1<br>RTO05_0 (PPG04_0)<br>MAD02_0 | G | I |
| 30 | 25 | 20 | 3 | N1 | N1 | VSS | - | - |
| 31 | 26 | - | 4 | M1 | M1 | VCC | - | - |
| 32 | 27 | - | 5 | N2 | N2 | P40<br>TIOA0_0<br>RTO10_1 (PPG10_1)<br>INT12_1 | G | K |
| 33 | 28 | - | 6 | N3 | L2 | P41<br>TIOA1_0<br>RTO11_1 (PPG10_1)<br>INT13_1 | G | K |
| 34 | 29 | - | 7 | M3 | N3 | P42<br>TIOA2_0<br>RTO12_1 (PPG12_1)<br>MSDWEX_0 | G | I |
| 35 | 30 | - | 8 | L3 | M3 | P43<br>ADTG_7<br>TIOA3_0<br>RTO13_1 (PPG12_1)<br>MCSX8_0 | G | I |

| Pin No | | | | | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|---|---|
| LQFP120 | LQFP100 | LQFP80 | QFP100 | BGA112 | BGA144 | | | |
| 36 | 31 | 21 | 9 | M4 | L4 | P44<br>TIOA4_0<br>RTO14_1 (PPG14_1)<br>DA0 | R | J |
| 37 | 32 | 22 | 10 | L5 | K5 | P45<br>TIOB0_0<br>RTO15_1 (PPG14_1)<br>DA1 | R | J |
| 38 | 33 | 23 | 11 | M6 | N4 | INITX | B | C |
| 39 | 34 | 24 | 12 | N5 | N5 | P46<br>X0A | P | S |
| 40 | 35 | 25 | 13 | N6 | M5 | P47<br>X1A | Q | T |
| 41 | 36 | 26 | 14 | L6 | L6 | P48<br>VREGCTL | O | U |
| 42 | 37 | 27 | 15 | M7 | K6 | P49<br>VWAKEUP | O | U |
| 43 | 38 | 28 | 16 | N8 | N7 | VBAT | - | - |
| 44 | 39 | 29 | 17 | N9 | N8 | C | - | - |
| 45 | 40 | 30 | 18 | N10 | N9 | VSS | - | - |
| 46 | 41 | 31 | 19 | M8 | M9 | VCC | - | - |
| 47 | 42 | 32 | 20 | L7 | L7 | P4B<br>TIOB1_0<br>SCS7_1<br>MAD03_0 | E | I |
| 48 | 43 | 33 | 21 | L8 | K7 | P4C<br>TIOB2_0<br>SCK7_1 (SCL7_1)<br>AIN1_2<br>MAD04_0 | N | I |
| 49 | 44 | 34 | 22 | M9 | M8 | P4D<br>TIOB3_0<br>SOT7_1 (SDA7_1)<br>BIN1_2<br>INT13_2<br>MAD05_0 | N | K |
| 50 | 45 | 35 | 23 | L9 | L8 | P4E<br>TIOB4_0<br>SIN7_1<br>ZIN1_2<br>FRCK1_1<br>INT11_1<br>WKUP2<br>MAD06_0 | I | Q |

| Pin No | | | | | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|---|---|
| LQFP120 | LQFP100 | LQFP80 | QFP100 | BGA112 | BGA144 | | | |
| 51 | - | - | - | - | K8 | P70<br>TIOA4_2<br>AIN0_1<br>IC13_1 | E | I |
| 52 | - | - | - | - | L9 | P71<br>TIOB4_2<br>BIN0_1<br>IC12_1<br>INT15_1 | E | K |
| 53 | - | - | - | - | K9 | P72<br>TIOA6_0<br>SIN2_0<br>ZIN0_1<br>IC11_1<br>INT14_2 | E | K |
| 54 | - | - | - | - | M10 | P73<br>TIOB6_0<br>SOT2_0 (SDA2_0)<br>IC10_1<br>INT03_2 | E | K |
| 55 | - | - | - | - | L10 | P74<br>SCK2_0 (SCL2_0)<br>DTTI1X_1 | E | I |
| 56 | 46 | 36 | 24 | M10 | N10 | PE0<br>MD1 | C | E |
| 57 | 47 | 37 | 25 | M11 | M11 | MD0 | J | D |
| 58 | 48 | 38 | 26 | N11 | N11 | PE2<br>X0 | A | A |
| 59 | 49 | 39 | 27 | N12 | N12 | PE3<br>X1 | A | B |
| 60 | 50 | 40 | 28 | N13 | N13 | VSS | - | - |
| 61 | 51 | - | 29 | M13 | M13 | VCC | - | - |
| 62 | 52 | 41 | 30 | L13 | L12 | P10<br>AN00<br>SIN1_1<br>FRCK0_2<br>INT02_1<br>MAD07_0 | F | M |
| 63 | 53 | 42 | 31 | L12 | K12 | P11<br>AN01<br>SOT1_1 (SDA1_1)<br>IC00_2<br>MAD08_0 | F | L |

| Pin No | | | | | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|---|---|
| LQFP120 | LQFP100 | LQFP80 | QFP100 | BGA112 | BGA144 | | | |
| 64 | 54 | 43 | 32 | K13 | K11 | P12<br>AN02<br>SCK1_1 (SCL1_1)<br>IC01_2<br>RTCCO_1<br>SUBOUT_1<br>MAD09_0 | F | L |
| 65 | 55 | 44 | 33 | K12 | J12 | P13<br>AN03<br>SIN0_1<br>IC02_2<br>INT03_1<br>MAD10_0 | F | M |
| 66 | 56 | 45 | 34 | J13 | J11 | P14<br>AN04<br>SOT0_1 (SDA0_1)<br>IC03_2<br>MAD11_0 | F | L |
| 67 | 57 | 46 | 35 | J12 | J10 | P15<br>AN05<br>SCK0_1 (SCL0_1)<br>MAD12_0 | F | L |
| 68 | 58 | 47 | 36 | J11 | H12 | P16<br>AN06<br>SIN2_2<br>INT14_1<br>MAD13_0 | F | M |
| 69 | 59 | 48 | 37 | H12 | H11 | P17<br>AN07<br>SOT2_2 (SDA2_2)<br>WKUP3<br>MAD14_0 | F | P |
| 70 | 60 | 49 | 38 | H13 | K13 | AVCC | - | - |
| 71 | 61 | 50 | 39 | G13 | J13 | AVSS | - | - |
| 72 | 62 | 51 | 40 | F13 | H13 | AVRL | - | - |
| 73 | 63 | 52 | 41 | E13 | G13 | AVRH | - | - |
| 74 | 64 | 53 | 42 | H11 | H10 | P18<br>AN08<br>SCK2_2 (SCL2_2)<br>MAD15_0 | F | L |

| Pin No | | | | | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|---|---|
| LQFP120 | LQFP100 | LQFP80 | QFP100 | BGA112 | BGA144 | | | |
| 75 | 65 | 54 | 43 | G12 | G12 | P19<br>AN09<br>SIN4_1<br>IC00_1<br>INT05_1<br>MAD16_0 | F | M |
| 76 | 66 | 55 | 44 | G11 | G11 | P1A<br>AN10<br>SOT4_1 (SDA4_1)<br>IC01_1<br>MAD17_0 | M | L |
| 77 | 67 | 56 | 45 | F12 | G10 | P1B<br>AN11<br>SCK4_1 (SCL4_1)<br>IC02_1<br>MAD18_0 | M | L |
| 78 | 68 | - | 46 | F11 | F13 | P1C<br>AN12<br>CTS4_1<br>IC03_1<br>MAD19_0 | F | L |
| 79 | 69 | - | 47 | E12 | F12 | P1D<br>AN13<br>RTS4_1<br>DTTI0X_1<br>MAD20_0 | F | L |
| 80 | 70 | - | 48 | E11 | F11 | P1E<br>AN14<br>ADTG_5<br>FRCK0_1<br>MAD21_0 | F | L |
| 81 | - | - | - | - | F10 | P1F<br>ADTG_4<br>TIOB6_2<br>RTO05_1 (PPG04_1) | E | I |
| 82 | - | - | - | - | E13 | P27<br>TIOA6_2<br>RTO04_1 (PPG04_1)<br>INT02_2 | E | K |

| Pin No | | | | | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|---|---|
| LQFP120 | LQFP100 | LQFP80 | QFP100 | BGA112 | BGA144 | | | |
| 83 | - | - | - | - | E12 | P26<br>TIOB5_0<br>SCK2_1 (SCL2_1)<br>RTO03_1 (PPG02_1) | E | I |
| 84 | - | - | - | - | E11 | P25<br>TIOA5_0<br>SOT2_1 (SDA2_1)<br>RTO02_1 (PPG02_1) | E | I |
| 85 | - | - | - | - | E10 | P24<br>SIN2_1<br>RTO01_1 (PPG00_1)<br>INT01_2 | E | K |
| 86 | 71 | 57<br>- | 49 | D13 | D13 | P23<br>AN15<br>TIOA7_1<br>SCK0_0 (SCL0_0)<br>RTO00_1 (PPG00_1)<br>MAD22_0 | F | L |
| 87 | 72 | 58<br>- | 50 | D12 | D12 | P22<br>CROUT_0<br>AN16<br>TIOB7_1<br>SOT0_0 (SDA0_0)<br>ZIN1_1 | F | L |
| 88 | 73 | 59<br>-<br>59<br>- | 51 | C13 | D11 | P21<br>AN17<br>SIN0_0<br>BIN1_1<br>INT06_1<br>MAD23_0 | F | M |
| 89 | 74 | - | 52 | C12 | C12 | P20<br>AN18<br>AIN1_1<br>INT05_0<br>MAD24_0 | F | M |
| 90 | 75 | 60 | 53 | A13 | A13 | VSS | - | - |
| 91 | 76 | 61 | 54 | B13 | A12 | VCC | - | - |

| Pin No | | | | | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|---|---|
| LQFP120 | LQFP100 | LQFP80 | QFP100 | BGA112 | BGA144 | | | |
| 92 | 77 | 62 | 55 | A12 | B13 | P0E<br>TIOB5_2<br>SCS6_1<br>IC13_0<br>S_CLK_0<br>MDQM1_0 | L | I |
| 93 | 78 | 63 | 56 | B11 | C10 | P0D<br>TIOA5_2<br>SCK6_1 (SCL6_1)<br>IC12_0<br>S_CMD_0<br>MDQM0_0 | L | I |
| 94 | 79 | 64 | 57 | B10 | A11 | P0C<br>TIOA6_1<br>SOT6_1 (SDA6_1)<br>IC11_0<br>S_DATA1_0<br>MALE_0 | L | I |
| 95 | 80 | 65 | 58 | A10 | B10 | P0B<br>TIOB6_1<br>SIN6_1<br>IC10_0<br>INT00_1<br>S_DATA0_0<br>MCSX0_0 | L | K |
| 96 | 81 | 66 | 59 | A9 | D9 | P0A<br>SIN1_0<br>FRCK1_0<br>INT12_2<br>S_DATA3_0<br>MCSX1_0 | L | K |
| 97 | 82 | 67<br>-<br>67 | 60 | B9 | C9 | P09<br>AN19<br>TRACED0<br>TIOA3_2<br>SOT1_0 (SDA1_0)<br>S_DATA2_0<br>MCSX5_0 | M | N |
| 98 | 83 | - | 61 | C9 | B9 | P08<br>AN20<br>TRACED1<br>TIOB3_2<br>SCK1_0 (SCL1_0)<br>MCSX4_0 | F | N |

| Pin No | | | | | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|---|---|
| LQFP120 | LQFP100 | LQFP80 | QFP100 | BGA112 | BGA144 | | | |
| 99 | 84 | - | 62 | A8 | A9 | P07<br>AN21<br>TRACED2<br>TIOA0_2<br>SCK7_0 (SCL7_0)<br>MCLKOUT_0 | F | N |
| 100 | 85 | - | 63 | B8 | D8 | P06<br>AN22<br>TRACED3<br>TIOB0_2<br>SOT7_0 (SDA7_0)<br>MCSX3_0 | F | N |
| 101 | 86 | - | 64 | C8 | C8 | P05<br>AN23<br>ADTG_0<br>TRACECLK<br>SIN7_0<br>INT01_1<br>MCSX2_0 | F | O |
| 102 | 87 | 68 | 65 | C7 | B8 | P04<br>TDO<br>SWO | E | G |
| 103 | 88 | 69 | 66 | B7 | D7 | P03<br>TMS<br>SWDIO | E | G |
| 104 | 89 | 70 | 67 | C6 | C7 | P02<br>TDI<br>MCSX6_0 | E | H |
| 105 | 90 | 71 | 68 | A6 | B7 | P01<br>TCK<br>SWCLK | E | G |
| 106 | 91 | 72 | 69 | B6 | D6 | P00<br>TRSTX<br>MCSX7_0 | E | H |
| 107 | 92 | - | 70 | A5 | A7 | VSS | - | - |
| 108 | - | - | - | - | C6 | P68<br>TIOB7_2<br>SCK3_0 (SCL3_0)<br>INT00_2 | E | K |
| 109 | - | - | - | - | B6 | P67<br>TIOA7_2<br>SOT3_0 (SDA3_0) | E | I |

| Pin No | | | | | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|---|---|
| LQFP120 | LQFP100 | LQFP80 | QFP100 | BGA112 | BGA144 | | | |
| 110 | - | - | - | - | A6 | P66<br>ADTG_8<br>SIN3_0<br>INT11_2 | E | K |
| 111 | - | - | - | - | D5 | P65<br>TIOB7_0<br>SCK5_1 (SCL5_1) | E | I |
| 112 | - | - | - | - | C5 | P64<br>TIOA7_0<br>SOT5_1 (SDA5_1)<br>INT10_2 | E | K |
| 113 | 93 | 73 | 71 | C5 | B5 | P63<br>CROUT_1<br>SIN5_1<br>INT03_0<br>S_CD_0<br>MWEX_0 | E | K |
| | - | - | - | - | | | | |
| | 93 | 73 | 71 | C5 | | | | |
| 114 | 94 | 74 | 72 | B5 | C4 | P62<br>ADTG_3<br>SIN5_0<br>INT04_1<br>S_WP_0<br>MOEX_0 | I | K |
| 115 | 95 | 75 | 73 | B4 | B4 | P61<br>TIOB2_2<br>SOT5_0 (SDA5_0)<br>RTCCO_0<br>SUBOUT_0 | E | I |
| 116 | 96 | 76 | 74 | B3 | B3 | P60<br>TIOA2_2<br>SCK5_0 (SCL5_0)<br>NMIX<br>WKUP0<br>MRDY_0 | I | F |
| 117 | 97 | 77 | 75 | A4 | A4 | VCC | - | - |
| 118 | 98 | 78 | 76 | A3 | A3 | P80 | H | R |
| 119 | 99 | 79 | 77 | A2 | A2 | P81 | H | R |

| Pin No | | | | | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|---|---|
| LQFP120 | LQFP100 | LQFP80 | QFP100 | BGA112 | BGA144 | | | |
| 120 | 100 | 80 | 78 | A1 | A1 | | - | - |
| - | - | - | - | A7 | A5 | | - | - |
| - | - | - | - | B2 | A8 | | - | - |
| - | - | - | - | B12 | A10 | | - | - |
| - | - | - | - | C11 | B2 | | - | - |
| - | - | - | - | H1 | B11 | | - | - |
| - | - | - | - | N4 | B12 | | - | - |
| - | - | - | - | M5 | C3 | | - | - |
| - | - | - | - | N7 | C11 | | - | - |
| - | - | - | - | L11 | C13 | | - | - |
| - | - | - | - | A11 | D4 | | - | - |
| - | - | - | - | M12 | D10 | | - | - |
| - | - | - | - | M2 | K1 | VSS | - | - |
| - | - | - | - | - | K4 | | - | - |
| - | - | - | - | - | K10 | | - | - |
| - | - | - | - | - | L3 | | - | - |
| - | - | - | - | - | L5 | | - | - |
| - | - | - | - | - | L11 | | - | - |
| - | - | - | - | - | L13 | | - | - |
| - | - | - | - | - | M2 | | - | - |
| - | - | - | - | - | M4 | | - | - |
| - | - | - | - | - | M6 | | - | - |
| - | - | - | - | - | M7 | | - | - |
| - | - | - | - | - | M12 | | - | - |
| - | - | - | - | - | N6 | | - | - |

## List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

| Pin function | Pin name | Function description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP 120 | LQFP 100 | LQFP 80 | QFP 100 | BGA 112 | BGA 144 |
| ADC | ADTG_0 | A/D converter external trigger input pin | 101 | 86 | - | 64 | C8 | C8 |
| | ADTG_1 | | 7 | 7 | 7 | 85 | E1 | E1 |
| | ADTG_2 | | 23 | 18 | 13 | 96 | J1 | J1 |
| | ADTG_3 | | 114 | 94 | 74 | 72 | B5 | C4 |
| | ADTG_4 | | 81 | - | - | - | - | F10 |
| | ADTG_5 | | 80 | 70 | - | 48 | E11 | F11 |
| | ADTG_6 | | 17 | 12 | 12 | 90 | F3 | G3 |
| | ADTG_7 | | 35 | 30 | - | 8 | L3 | M3 |
| | ADTG_8 | | 110 | - | - | - | - | A6 |
| | AN00 | A/D converter analog input pin. ANxx describes ADC ch.xx. | 62 | 52 | 41 | 30 | L13 | L12 |
| | AN01 | | 63 | 53 | 42 | 31 | L12 | K12 |
| | AN02 | | 64 | 54 | 43 | 32 | K13 | K11 |
| | AN03 | | 65 | 55 | 44 | 33 | K12 | J12 |
| | AN04 | | 66 | 56 | 45 | 34 | J13 | J11 |
| | AN05 | | 67 | 57 | 46 | 35 | J12 | J10 |
| | AN06 | | 68 | 58 | 47 | 36 | J11 | H12 |
| | AN07 | | 69 | 59 | 48 | 37 | H12 | H11 |
| | AN08 | | 74 | 64 | 53 | 42 | H11 | H10 |
| | AN09 | | 75 | 65 | 54 | 43 | G12 | G12 |
| | AN10 | | 76 | 66 | 55 | 44 | G11 | G11 |
| | AN11 | | 77 | 67 | 56 | 45 | F12 | G10 |
| | AN12 | | 78 | 68 | - | 46 | F11 | F13 |
| | AN13 | | 79 | 69 | - | 47 | E12 | F12 |
| | AN14 | | 80 | 70 | - | 48 | E11 | F11 |
| | AN15 | | 86 | 71 | 57 | 49 | D13 | D13 |
| | AN16 | | 87 | 72 | 58 | 50 | D12 | D12 |
| | AN17 | | 88 | 73 | 59 | 51 | C13 | D11 |
| | AN18 | | 89 | 74 | - | 52 | C12 | C12 |
| | AN19 | | 97 | 82 | 67 | 60 | B9 | C9 |
| | AN20 | | 98 | 83 | - | 61 | C9 | B9 |
| | AN21 | | 99 | 84 | - | 62 | A8 | A9 |
| | AN22 | | 100 | 85 | - | 63 | B8 | D8 |
| | AN23 | | 101 | 86 | - | 64 | C8 | C8 |
| Base Timer 0 | TIOA0_0 | Base timer ch.0 TIOA pin | 32 | 27 | - | 5 | N2 | N2 |
| | TIOA0_1 | | 24 | 19 | 14 | 97 | J2 | J2 |
| | TIOA0_2 | | 99 | 84 | - | 62 | A8 | A9 |
| | TIOB0_0 | Base timer ch.0 TIOB pin | 37 | 32 | 22 | 10 | L5 | K5 |
| | TIOB0_1 | | 14 | 9 | 9 | 87 | E3 | F4 |
| | TIOB0_2 | | 100 | 85 | - | 63 | B8 | D8 |
| Base Timer 1 | TIOA1_0 | Base timer ch.1 TIOA pin | 33 | 28 | - | 6 | N3 | L2 |
| | TIOA1_1 | | 25 | 20 | 15 | 98 | J3 | J3 |
| | TIOA1_2 | | 5 | 5 | 5 | 83 | D1 | D2 |
| | TIOB1_0 | Base timer ch.1 TIOB pin | 47 | 42 | 32 | 20 | L7 | L7 |
| | TIOB1_1 | | 15 | 10 | 10 | 88 | F1 | G1 |
| | TIOB1_2 | | 6 | 6 | 6 | 84 | D2 | D3 |
| Base Timer 2 | TIOA2_0 | Base timer ch.2 TIOA pin | 34 | 29 | - | 7 | M3 | N3 |
| | TIOA2_1 | | 26 | 21 | 16 | 99 | K1 | J4 |
| | TIOA2_2 | | 116 | 96 | 76 | 74 | B3 | B3 |
| | TIOB2_0 | Base timer ch.2 TIOB pin | 48 | 43 | 33 | 21 | L8 | K7 |
| | TIOB2_1 | | 16 | 11 | 11 | 89 | F2 | G2 |
| | TIOB2_2 | | 115 | 95 | 75 | 73 | B4 | B4 |

| Pin function | Pin name | Function description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP 120 | LQFP 100 | LQFP 80 | QFP 100 | BGA 112 | BGA 144 |
| Base Timer 3 | TIOA3_0 | Base timer ch.3 TIOA pin | 35 | 30 | - | 8 | L3 | M3 |
| | TIOA3_1 | | 27 | 22 | 17 | 100 | K2 | K2 |
| | TIOA3_2 | | 97 | 82 | 67 | 60 | B9 | C9 |
| | TIOB3_0 | Base timer ch.3 TIOB pin | 49 | 44 | 34 | 22 | M9 | M8 |
| | TIOB3_1 | | 17 | 12 | 12 | 90 | F3 | G3 |
| | TIOB3_2 | | 98 | 83 | - | 61 | C9 | B9 |
| Base Timer 4 | TIOA4_0 | Base timer ch.4 TIOA pin | 36 | 31 | 21 | 9 | M4 | L4 |
| | TIOA4_1 | | 28 | 23 | 18 | 1 | L1 | K3 |
| | TIOA4_2 | | 51 | - | - | - | - | K8 |
| | TIOB4_0 | Base timer ch.4 TIOB pin | 50 | 45 | 35 | 23 | L9 | L8 |
| | TIOB4_1 | | 18 | 13 | - | 91 | G1 | G4 |
| | TIOB4_2 | | 52 | - | - | - | - | L9 |
| Base Timer 5 | TIOA5_0 | Base timer ch.5 TIOA pin | 84 | - | - | - | - | E11 |
| | TIOA5_1 | | 29 | 24 | 19 | 2 | L2 | L1 |
| | TIOA5_2 | | 93 | 78 | 63 | 56 | B11 | C10 |
| | TIOB5_0 | Base timer ch.5 TIOB pin | 83 | - | - | - | - | E12 |
| | TIOB5_1 | | 19 | 14 | - | 92 | G2 | H1 |
| | TIOB5_2 | | 92 | 77 | 62 | 55 | A12 | B13 |
| Base Timer 6 | TIOA6_0 | Base timer ch.6 TIOA pin | 53 | - | - | - | - | K9 |
| | TIOA6_1 | | 94 | 79 | 64 | 57 | B10 | A11 |
| | TIOA6_2 | | 82 | - | - | - | - | E13 |
| | TIOB6_0 | Base timer ch.6 TIOB pin | 54 | - | - | - | - | M10 |
| | TIOB6_1 | | 95 | 80 | 65 | 58 | A10 | B10 |
| | TIOB6_2 | | 81 | - | - | - | - | F10 |
| Base Timer 7 | TIOA7_0 | Base timer ch.7 TIOA pin | 112 | - | - | - | - | C5 |
| | TIOA7_1 | | 86 | 71 | 57 | 49 | D13 | D13 |
| | TIOA7_2 | | 109 | - | - | - | - | B6 |
| | TIOB7_0 | Base timer ch.7 TIOB pin | 111 | - | - | - | - | D5 |
| | TIOB7_1 | | 87 | 72 | 58 | 50 | D12 | D12 |
| | TIOB7_2 | | 108 | - | - | - | - | C6 |
| Debugger | SWCLK | Serial wire debug interface clock input pin | 105 | 90 | 71 | 68 | A6 | B7 |
| | SWDIO | Serial wire debug interface data input / output pin | 103 | 88 | 69 | 66 | B7 | D7 |
| | SWO | Serial wire viewer output pin | 102 | 87 | 68 | 65 | C7 | B8 |
| | TCK | JTAG test clock input pin | 105 | 90 | 71 | 68 | A6 | B7 |
| | TDI | JTAG test data input pin | 104 | 89 | 70 | 67 | C6 | C7 |
| | TDO | JTAG debug data output pin | 102 | 87 | 68 | 65 | C7 | B8 |
| | TMS | JTAG test mode state input/output pin | 103 | 88 | 69 | 66 | B7 | D7 |
| | TRACECLK | Trace CLK output pin of ETM | 101 | 86 | - | 64 | C8 | C8 |
| | TRACED0 | Trace data output pin of ETM | 97 | 82 | - | 60 | B9 | C9 |
| | TRACED1 | | 98 | 83 | - | 61 | C9 | B9 |
| | TRACED2 | | 99 | 84 | - | 62 | A8 | A9 |
| | TRACED3 | | 100 | 85 | - | 63 | B8 | D8 |
| | TRSTX | JTAG test reset Input pin | 106 | 91 | 72 | 69 | B6 | D6 |

| Pin function | Pin name | Function description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP 120 | LQFP 100 | LQFP 80 | QFP 100 | BGA 112 | BGA 144 |
| External Bus | MAD00_0 | External bus interface address bus | 27 | 22 | 17 | 100 | K2 | K2 |
| | MAD01_0 | | 28 | 23 | 18 | 1 | L1 | K3 |
| | MAD02_0 | | 29 | 24 | 19 | 2 | L2 | L1 |
| | MAD03_0 | | 47 | 42 | 32 | 20 | L7 | L7 |
| | MAD04_0 | | 48 | 43 | 33 | 21 | L8 | K7 |
| | MAD05_0 | | 49 | 44 | 34 | 22 | M9 | M8 |
| | MAD06_0 | | 50 | 45 | 35 | 23 | L9 | L8 |
| | MAD07_0 | | 62 | 52 | 41 | 30 | L13 | L12 |
| | MAD08_0 | | 63 | 53 | 42 | 31 | L12 | K12 |
| | MAD09_0 | | 64 | 54 | 43 | 32 | K13 | K11 |
| | MAD10_0 | | 65 | 55 | 44 | 33 | K12 | J12 |
| | MAD11_0 | | 66 | 56 | 45 | 34 | J13 | J11 |
| | MAD12_0 | | 67 | 57 | 46 | 35 | J12 | J10 |
| | MAD13_0 | | 68 | 58 | 47 | 36 | J11 | H12 |
| | MAD14_0 | | 69 | 59 | 48 | 37 | H12 | H11 |
| | MAD15_0 | | 74 | 64 | 53 | 42 | H11 | H10 |
| | MAD16_0 | | 75 | 65 | 54 | 43 | G12 | G12 |
| | MAD17_0 | | 76 | 66 | 55 | 44 | G11 | G11 |
| | MAD18_0 | | 77 | 67 | 56 | 45 | F12 | G10 |
| | MAD19_0 | | 78 | 68 | - | 46 | F11 | F13 |
| | MAD20_0 | | 79 | 69 | - | 47 | E12 | F12 |
| | MAD21_0 | | 80 | 70 | - | 48 | E11 | F11 |
| | MAD22_0 | | 86 | 71 | - | 49 | D13 | D13 |
| | MAD23_0 | | 88 | 73 | - | 51 | C13 | D11 |
| | MAD24_0 | | 89 | 74 | - | 52 | C12 | C12 |

| Pin function | Pin name | Function description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP 120 | LQFP 100 | LQFP 80 | QFP 100 | BGA 112 | BGA 144 |
| External Bus | MCSX0_0 | External bus interface chip select output pin | 95 | 80 | 65 | 58 | A10 | B10 |
| | MCSX1_0 | | 96 | 81 | 66 | 59 | A9 | D9 |
| | MCSX2_0 | | 101 | 86 | - | 64 | C8 | C8 |
| | MCSX3_0 | | 100 | 85 | - | 63 | B8 | D8 |
| | MCSX4_0 | | 98 | 83 | - | 61 | C9 | B9 |
| | MCSX5_0 | | 97 | 82 | 67 | 60 | B9 | C9 |
| | MCSX6_0 | | 104 | 89 | 70 | 67 | C6 | C7 |
| | MCSX7_0 | | 106 | 91 | 72 | 69 | B6 | D6 |
| | MCSX8_0 | | 35 | 30 | - | 8 | L3 | M3 |
| | MADATA00_0 | External bus interface data bus (Address / data multiplex bus) | 2 | 2 | 2 | 80 | C1 | C1 |
| | MADATA01_0 | | 3 | 3 | 3 | 81 | C2 | C2 |
| | MADATA02_0 | | 4 | 4 | 4 | 82 | C3 | D1 |
| | MADATA03_0 | | 5 | 5 | 5 | 83 | D1 | D2 |
| | MADATA04_0 | | 6 | 6 | 6 | 84 | D2 | D3 |
| | MADATA05_0 | | 7 | 7 | 7 | 85 | E1 | E1 |
| | MADATA06_0 | | 8 | 8 | 8 | 86 | E2 | E2 |
| | MADATA07_0 | | 9 | 9 | 9 | 87 | E3 | E3 |
| | MADATA08_0 | | 10 | 10 | 10 | 88 | F1 | E4 |
| | MADATA09_0 | | 11 | 11 | 11 | 89 | F2 | F1 |
| | MADATA10_0 | | 12 | 12 | 12 | 90 | F3 | F2 |
| | MADATA11_0 | | 13 | 13 | - | 91 | G1 | F3 |
| | MADATA12_0 | | 14 | 14 | - | 92 | G2 | F4 |
| | MADATA13_0 | | 15 | 15 | - | 93 | G3 | G1 |
| | MADATA14_0 | | 16 | 16 | - | 94 | H2 | G2 |
| | MADATA15_0 | | 17 | 17 | - | 95 | H3 | G3 |
| | MDQM0_0 | External bus interface byte mask signal output pin | 93 | 78 | 63 | 56 | B11 | C10 |
| | MDQM1_0 | | 92 | 77 | 62 | 55 | A12 | B13 |
| | MALE_0 | External bus interface Address Latch enable output signal for multiplex | 94 | 79 | 64 | 57 | B10 | A11 |
| | MRDY_0 | External bus interface external RDY input signal | 116 | 96 | 76 | 74 | B3 | B3 |
| | MCLKOUT_0 | External bus interface external clock output pin | 99 | 84 | - | 62 | A8 | A9 |
| | MNALE_0 | External bus interface ALE signal to control NAND Flash output pin | 18 | - | - | - | - | G4 |
| | MNCLE_0 | External bus interface CLE signal to control NAND Flash output pin | 19 | - | - | - | - | H1 |
| | MNREX_0 | External bus interface read enable signal to control NAND Flash | 21 | - | - | - | - | H3 |
| | MNWEX_0 | External bus interface write enable signal to control NAND Flash | 20 | - | - | - | - | H2 |
| | MOEX_0 | External bus interface read enable signal for SRAM | 114 | 94 | 74 | 72 | B5 | C4 |
| | MWEX_0 | External bus interface write enable signal for SRAM | 113 | 93 | 73 | 71 | C5 | B5 |
| External Bus | MSDCLK_0 | SDRAM interface SDRAM clock output pin | 23 | 18 | - | 96 | J1 | J1 |
| | MSDCKE_0 | SDRAM interface SDRAM clock enable pin | 24 | 19 | - | 97 | J2 | J2 |
| | MRASX_0 | SDRAM interface SDRAM row address strobe pin | 25 | 20 | - | 98 | J3 | J3 |
| | MCASX_0 | SDRAM interface SDRAM column address strobe pin | 26 | 21 | - | 99 | K1 | J4 |
| | MSDWEX_0 | SDRAM interface SDRAM write enable pin | 34 | 29 | - | 7 | M3 | N3 |

| Pin function | Pin name | Function description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP 120 | LQFP 100 | LQFP 80 | QFP 100 | BGA 112 | BGA 144 |
| External Interrupt | INT00_0 | External interrupt request 00 input pin | 2 | 2 | 2 | 80 | C1 | C1 |
| | INT00_1 | | 95 | 80 | 65 | 58 | A10 | B10 |
| | INT00_2 | | 108 | - | - | - | - | C6 |
| | INT01_0 | External interrupt request 01 input pin | 3 | 3 | 3 | 81 | C2 | C2 |
| | INT01_1 | | 101 | 86 | - | 64 | C8 | C8 |
| | INT01_2 | | 85 | - | - | - | - | E10 |
| | INT02_0 | External interrupt request 02 input pin | 6 | 6 | 6 | 84 | D2 | D3 |
| | INT02_1 | | 62 | 52 | 41 | 30 | L13 | L12 |
| | INT02_2 | | 82 | - | - | - | - | E13 |
| | INT03_0 | External interrupt request 03 input pin | 113 | 93 | 73 | 71 | C5 | B5 |
| | INT03_1 | | 65 | 55 | 44 | 33 | K12 | J12 |
| | INT03_2 | | 54 | - | - | - | - | M10 |
| | INT04_0 | External interrupt request 04 input pin | 17 | 12 | 12 | 90 | F3 | G3 |
| | INT04_1 | | 114 | 94 | 74 | 72 | B5 | C4 |
| | INT04_2 | | 10 | - | - | - | - | E4 |
| | INT05_0 | External interrupt request 05 input pin | 89 | 74 | - | 52 | C12 | C12 |
| | INT05_1 | | 75 | 65 | 54 | 43 | G12 | G12 |
| | INT05_2 | | 21 | 16 | - | 94 | H2 | H3 |
| | INT06_1 | External interrupt request 06 input pin | 88 | 73 | 59 | 51 | C13 | D11 |
| | INT06_2 | | 22 | 17 | - | 95 | H3 | H4 |
| | INT07_1 | External interrupt request 07 input pin | 11 | - | - | - | - | F1 |
| | INT07_2 | | 7 | 7 | 7 | 85 | E1 | E1 |
| | INT08_1 | External interrupt request 08 input pin | 19 | 14 | - | 92 | G2 | H1 |
| | INT08_2 | | 8 | 8 | 8 | 86 | E2 | E2 |
| | INT09_1 | External interrupt request 09 input pin | 20 | 15 | - | 93 | G3 | H2 |
| | INT09_2 | | 15 | 10 | 10 | 88 | F1 | G1 |
| | INT10_1 | External interrupt request 10 input pin | 16 | 11 | 11 | 89 | F2 | G2 |
| | INT10_2 | | 112 | - | - | - | - | C5 |
| | INT11_1 | External interrupt request 11 input pin | 50 | 45 | 35 | 23 | L9 | L8 |
| | INT11_2 | | 110 | - | - | - | - | A6 |
| | INT12_1 | External interrupt request 12 input pin | 32 | 27 | - | 5 | N2 | N2 |
| | INT12_2 | | 96 | 81 | 66 | 59 | A9 | D9 |
| | INT13_1 | External interrupt request 13 input pin | 33 | 28 | - | 6 | N3 | L2 |
| | INT13_2 | | 49 | 44 | 34 | 22 | M9 | M8 |
| | INT14_1 | External interrupt request 14 input pin | 68 | 58 | 47 | 36 | J11 | H12 |
| | INT14_2 | | 53 | - | - | - | - | K9 |
| | INT15_1 | External interrupt request 15 input pin | 52 | - | - | - | - | L9 |
| | INT15_2 | | 14 | 9 | 9 | 87 | E3 | F4 |
| | NMIX | Non-Maskable Interrupt input pin | 116 | 96 | 76 | 74 | B3 | B3 |

| Pin function | Pin name | Function description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP 120 | LQFP 100 | LQFP 80 | QFP 100 | BGA 112 | BGA 144 |
| GPIO | P00 | General-purpose I/O port 0 | 106 | 91 | 72 | 69 | B6 | D6 |
| | P01 | | 105 | 90 | 71 | 68 | A6 | B7 |
| | P02 | | 104 | 89 | 70 | 67 | C6 | C7 |
| | P03 | | 103 | 88 | 69 | 66 | B7 | D7 |
| | P04 | | 102 | 87 | 68 | 65 | C7 | B8 |
| | P05 | | 101 | 86 | - | 64 | C8 | C8 |
| | P06 | | 100 | 85 | - | 63 | B8 | D8 |
| | P07 | | 99 | 84 | - | 62 | A8 | A9 |
| | P08 | | 98 | 83 | - | 61 | C9 | B9 |
| | P09 | | 97 | 82 | 67 | 60 | B9 | C9 |
| | P0A | | 96 | 81 | 66 | 59 | A9 | D9 |
| | P0B | | 95 | 80 | 65 | 58 | A10 | B10 |
| | P0C | | 94 | 79 | 64 | 57 | B10 | A11 |
| | P0D | | 93 | 78 | 63 | 56 | B11 | C10 |
| | P0E | | 92 | 77 | 62 | 55 | A12 | B13 |
| | P10 | General-purpose I/O port 1 | 62 | 52 | 41 | 30 | L13 | L12 |
| | P11 | | 63 | 53 | 42 | 31 | L12 | K12 |
| | P12 | | 64 | 54 | 43 | 32 | K13 | K11 |
| | P13 | | 65 | 55 | 44 | 33 | K12 | J12 |
| | P14 | | 66 | 56 | 45 | 34 | J13 | J11 |
| | P15 | | 67 | 57 | 46 | 35 | J12 | J10 |
| | P16 | | 68 | 58 | 47 | 36 | J11 | H12 |
| | P17 | | 69 | 59 | 48 | 37 | H12 | H11 |
| | P18 | | 74 | 64 | 53 | 42 | H11 | H10 |
| | P19 | | 75 | 65 | 54 | 43 | G12 | G12 |
| | P1A | | 76 | 66 | 55 | 44 | G11 | G11 |
| | P1B | | 77 | 67 | 56 | 45 | F12 | G10 |
| | P1C | | 78 | 68 | - | 46 | F11 | F13 |
| | P1D | | 79 | 69 | - | 47 | E12 | F12 |
| | P1E | | 80 | 70 | - | 48 | E11 | F11 |
| | P1F | | 81 | - | - | - | - | F10 |
| | P20 | General-purpose I/O port 2 | 89 | 74 | - | 52 | C12 | C12 |
| | P21 | | 88 | 73 | 59 | 51 | C13 | D11 |
| | P22 | | 87 | 72 | 58 | 50 | D12 | D12 |
| | P23 | | 86 | 71 | 57 | 49 | D13 | D13 |
| | P24 | | 85 | - | - | - | - | E10 |
| | P25 | | 84 | - | - | - | - | E11 |
| | P26 | | 83 | - | - | - | - | E12 |
| | P27 | | 82 | - | - | - | - | E13 |

| Pin function | Pin name | Function description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP 120 | LQFP 100 | LQFP 80 | QFP 100 | BGA 112 | BGA 144 |
| GPIO | P30 | General-purpose I/O port 3 | 14 | 9 | 9 | 87 | E3 | F4 |
| | P31 | | 15 | 10 | 10 | 88 | F1 | G1 |
| | P32 | | 16 | 11 | 11 | 89 | F2 | G2 |
| | P33 | | 17 | 12 | 12 | 90 | F3 | G3 |
| | P34 | | 18 | 13 | - | 91 | G1 | G4 |
| | P35 | | 19 | 14 | - | 92 | G2 | H1 |
| | P36 | | 20 | 15 | - | 93 | G3 | H2 |
| | P37 | | 21 | 16 | - | 94 | H2 | H3 |
| | P38 | | 22 | 17 | - | 95 | H3 | H4 |
| | P39 | | 23 | 18 | 13 | 96 | J1 | J1 |
| | P3A | | 24 | 19 | 14 | 97 | J2 | J2 |
| | P3B | | 25 | 20 | 15 | 98 | J3 | J3 |
| | P3C | | 26 | 21 | 16 | 99 | K1 | J4 |
| | P3D | | 27 | 22 | 17 | 100 | K2 | K2 |
| | P3E | | 28 | 23 | 18 | 1 | L1 | K3 |
| | P3F | | 29 | 24 | 19 | 2 | L2 | L1 |
| | P40 | General-purpose I/O port 4 | 32 | 27 | - | 5 | N2 | N2 |
| | P41 | | 33 | 28 | - | 6 | N3 | L2 |
| | P42 | | 34 | 29 | - | 7 | M3 | N3 |
| | P43 | | 35 | 30 | - | 8 | L3 | M3 |
| | P44 | | 36 | 31 | 21 | 9 | M4 | L4 |
| | P45 | | 37 | 32 | 22 | 10 | L5 | K5 |
| | P46 | | 39 | 34 | 24 | 12 | N5 | N5 |
| | P47 | | 40 | 35 | 25 | 13 | N6 | M5 |
| | P48 | | 41 | 36 | 26 | 14 | L6 | L6 |
| | P49 | | 42 | 37 | 27 | 15 | M7 | K6 |
| | P4B | | 47 | 42 | 32 | 20 | L7 | L7 |
| | P4C | | 48 | 43 | 33 | 21 | L8 | K7 |
| | P4D | | 49 | 44 | 34 | 22 | M9 | M8 |
| | P4E | | 50 | 45 | 35 | 23 | L9 | L8 |
| | P50 | General-purpose I/O port 5 | 2 | 2 | 2 | 80 | C1 | C1 |
| | P51 | | 3 | 3 | 3 | 81 | C2 | C2 |
| | P52 | | 4 | 4 | 4 | 82 | C3 | D1 |
| | P53 | | 5 | 5 | 5 | 83 | D1 | D2 |
| | P54 | | 6 | 6 | 6 | 84 | D2 | D3 |
| | P55 | | 7 | 7 | 7 | 85 | E1 | E1 |
| | P56 | | 8 | 8 | 8 | 86 | E2 | E2 |
| | P57 | | 9 | - | - | - | - | E3 |
| | P58 | | 10 | - | - | - | - | E4 |
| | P59 | | 11 | - | - | - | - | F1 |
| | P5A | | 12 | - | - | - | - | F2 |
| | P5B | | 13 | - | - | - | - | F3 |

| Pin function | Pin name | Function description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP 120 | LQFP 100 | LQFP 80 | QFP 100 | BGA 112 | BGA 144 |
| GPIO | P60 | General-purpose I/O port 6 | 116 | 96 | 76 | 74 | B3 | B3 |
| | P61 | | 115 | 95 | 75 | 73 | B4 | B4 |
| | P62 | | 114 | 94 | 74 | 72 | B5 | C4 |
| | P63 | | 113 | 93 | 73 | 71 | C5 | B5 |
| | P64 | | 112 | - | - | - | - | C5 |
| | P65 | | 111 | - | - | - | - | D5 |
| | P66 | | 110 | - | - | - | - | A6 |
| | P67 | | 109 | - | - | - | - | B6 |
| | P68 | | 108 | - | - | - | - | C6 |
| | P70 | General-purpose I/O port 7 | 51 | - | - | - | - | K8 |
| | P71 | | 52 | - | - | - | - | L9 |
| | P72 | | 53 | - | - | - | - | K9 |
| | P73 | | 54 | - | - | - | - | M10 |
| | P74 | | 55 | - | - | - | - | L10 |
| | P80 | General-purpose I/O port 8 | 118 | 98 | 78 | 76 | A3 | A3 |
| | P81 | | 119 | 99 | 79 | 77 | A2 | A2 |
| | PE0 | General-purpose I/O port E | 56 | 46 | 36 | 24 | M10 | N10 |
| | PE2 | | 58 | 48 | 38 | 26 | N11 | N11 |
| | PE3 | | 59 | 49 | 39 | 27 | N12 | N12 |
| Multi- function Serial 0 | SIN0_0 | Multi-function serial interface ch.0 input pin | 88 | 73 | 59 | 51 | C13 | D11 |
| | SIN0_1 | | 65 | 55 | 44 | 33 | K12 | J12 |
| | SOT0_0 (SDA0_0) | Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an $I^2C$ (operation mode 4). | 87 | 72 | 58 | 50 | D12 | D12 |
| | SOT0_1 (SDA0_1) | | 66 | 56 | 45 | 34 | J13 | J11 |
| | SCK0_0 (SCL0_0) | Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SCL0 when it is used in an $I^2C$ (operation mode 4). | 86 | 71 | 57 | 49 | D13 | D13 |
| | SCK0_1 (SCL0_1) | | 67 | 57 | 46 | 35 | J12 | J10 |
| Multi- function Serial 1 | SIN1_0 | Multi-function serial interface ch.1 input pin | 96 | 81 | 66 | 59 | A9 | D9 |
| | SIN1_1 | | 62 | 52 | 41 | 30 | L13 | L12 |
| | SOT1_0 (SDA1_0) | Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an $I^2C$ (operation mode 4). | 97 | 82 | 67 | 60 | B9 | C9 |
| | SOT1_1 (SDA1_1) | | 63 | 53 | 42 | 31 | L12 | K12 |
| | SCK1_0 (SCL1_0) | Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation modes 4) and as SCL1 when it is used in an $I^2C$ (operation mode 4). | 98 | 83 | - | 61 | C9 | B9 |
| | SCK1_1 (SCL1_1) | | 64 | 54 | 43 | 32 | K13 | K11 |

| Pin function | Pin name | Function description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP 120 | LQFP 100 | LQFP 80 | QFP 100 | BGA 112 | BGA 144 |
| Multi- function Serial 2 | SIN2_0 | Multi-function serial interface ch.2 input pin | 53 | - | - | - | - | K9 |
| | SIN2_1 | | 85 | - | - | - | - | E10 |
| | SIN2_2 | | 68 | 58 | 47 | 36 | J11 | H12 |
| | SOT2_0 (SDA2_0) | Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an $I^2C$ (operation mode 4). | 54 | - | - | - | - | M10 |
| | SOT2_1 (SDA2_1) | | 84 | - | - | - | - | E11 |
| | SOT2_2 (SDA2_2) | | 69 | 59 | 48 | 37 | H12 | H11 |
| | SCK2_0 (SCL2_0) | Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a CSIO (operation modes 2) and as SCL2 when it is used in an $I^2C$ (operation mode 4). | 55 | - | - | - | - | L10 |
| | SCK2_1 (SCL2_1) | | 83 | - | - | - | - | E12 |
| | SCK2_2 (SCL2_2) | | 74 | 64 | 53 | 42 | H11 | H10 |
| Multi- function Serial 3 | SIN3_0 | Multi-function serial interface ch.3 input pin | 110 | - | - | - | - | A6 |
| | SIN3_1 | | 15 | 10 | 10 | 88 | F1 | G1 |
| | SOT3_0 (SDA3_0) | Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an $I^2C$ (operation mode 4). | 109 | - | - | - | - | B6 |
| | SOT3_1 (SDA3_1) | | 16 | 11 | 11 | 89 | F2 | G2 |
| | SCK3_0 (SCL3_0) | Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an $I^2C$ (operation mode 4). | 108 | - | - | - | - | C6 |
| | SCK3_1 (SCL3_1) | | 17 | 12 | 12 | 90 | F3 | G3 |
| Multi- function Serial 4 | SIN4_0 | Multi-function serial interface ch.4 input pin | 6 | 6 | 6 | 84 | D2 | D3 |
| | SIN4_1 | | 75 | 65 | 54 | 43 | G12 | G12 |
| | SIN4_2 | | 10 | - | - | - | - | E4 |
| | SOT4_0 (SDA4_0) | Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an $I^2C$ (operation mode 4). | 5 | 5 | 5 | 83 | D1 | D2 |
| | SOT4_1 (SDA4_1) | | 76 | 66 | 55 | 44 | G11 | G11 |
| | SOT4_2 (SDA4_2) | | 11 | - | - | - | - | F1 |
| | SCK4_0 (SCL4_0) | Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation modes 2) and as SCL4 when it is used in an $I^2C$ (operation mode 4). | 4 | 4 | 4 | 82 | C3 | D1 |
| | SCK4_1 (SCL4_1) | | 77 | 67 | 56 | 45 | F12 | G10 |
| | SCK4_2 (SCL4_2) | | 12 | - | - | - | - | F2 |
| | CTS4_0 | Multi-function serial interface ch.4 CTS input pin | 2 | 2 | 2 | 80 | C1 | C1 |
| | CTS4_1 | | 78 | 68 | - | 46 | F11 | F13 |
| | CTS4_2 | | 13 | - | - | - | - | F3 |
| | RTS4_0 | Multi-function serial interface ch.4 RTS output pin | 3 | 3 | 3 | 81 | C2 | C2 |
| | RTS4_1 | | 79 | 69 | - | 47 | E12 | F12 |
| | RTS4_2 | | 14 | 9 | 9 | 87 | E3 | F4 |

| Pin function | Pin name | Function description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP 120 | LQFP 100 | LQFP 80 | QFP 100 | BGA 112 | BGA 144 |
| Multi- function Serial 5 | SIN5_0 | Multi-function serial interface ch.5 input pin | 114 | 94 | 74 | 72 | B5 | C4 |
| | SIN5_1 | | 113 | - | - | - | - | B5 |
| | SIN5_2 | | 20 | 15 | - | 93 | G3 | H2 |
| | SOT5_0 (SDA5_0) | Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an $I^2C$ (operation mode 4). | 115 | 95 | 75 | 73 | B4 | B4 |
| | SOT5_1 (SDA5_1) | | 112 | - | - | - | - | C5 |
| | SOT5_2 (SDA5_2) | | 21 | 16 | - | 94 | H2 | H3 |
| | SCK5_0 (SCL5_0) | Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation modes 2) and as SCL5 when it is used in an $I^2C$ (operation mode 4). | 116 | 96 | 76 | 74 | B3 | B3 |
| | SCK5_1 (SCL5_1) | | 111 | - | - | - | - | D5 |
| | SCK5_2 (SCL5_2) | | 22 | 17 | - | 95 | H3 | H4 |
| Multi- function Serial 6 | SIN6_0 | Multi-function serial interface ch.6 input pin | 7 | 7 | 7 | 85 | E1 | E1 |
| | SIN6_1 | | 95 | 80 | 65 | 58 | A10 | B10 |
| | SOT6_0 (SDA6_0) | Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an $I^2C$ (operation mode 4). | 8 | 8 | 8 | 86 | E2 | E2 |
| | SOT6_1 (SDA6_1) | | 94 | 79 | 64 | 57 | B10 | A11 |
| | SCK6_0 (SCL6_0) | Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation modes 2) and as SCL6 when it is used in an $I^2C$ (operation mode 4). | 9 | - | - | - | - | E3 |
| | SCK6_1 (SCL6_1) | | 93 | 78 | 63 | 56 | B11 | C10 |
| | SCS6_1 | Multi-function serial interface ch.6 serial chip select pin | 92 | 77 | 62 | 55 | A12 | B13 |
| Multi- function Serial 7 | SIN7_0 | Multi-function serial interface ch.7 input pin | 101 | 86 | - | 64 | C8 | C8 |
| | SIN7_1 | | 50 | 45 | 35 | 23 | L9 | L8 |
| | SOT7_0 (SDA7_0) | Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an $I^2C$ (operation mode 4). | 100 | 85 | - | 63 | B8 | D8 |
| | SOT7_1 (SDA7_1) | | 49 | 44 | 34 | 22 | M9 | M8 |
| | SCK7_0 (SCL7_0) | Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation modes 2) and as SCL7 when it is used in an $I^2C$ (operation mode 4). | 99 | 84 | - | 62 | A8 | A9 |
| | SCK7_1 (SCL7_1) | | 48 | 43 | 33 | 21 | L8 | K7 |
| | SCS7_1 | Multi-function serial interface ch.7 serial chip select pin | 47 | 42 | 32 | 20 | L7 | L7 |

| Pin function | Pin name | Function description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP 120 | LQFP 100 | LQFP 80 | QFP 100 | BGA 112 | BGA 144 |
| Multi-function Timer 0 | DTTI0X_0 | Input signal controlling wave form generator outputs RTO00 to RTO05 of Multi-function timer 0. | 23 | 18 | 13 | 96 | J1 | J1 |
| | DTTI0X_1 | | 79 | 69 | - | 47 | E12 | F12 |
| | FRCK0_0 | 16-bit free-run timer ch.0 external clock input pin | 18 | 13 | - | 91 | G1 | G4 |
| | FRCK0_1 | | 80 | 70 | - | 48 | E11 | F11 |
| | FRCK0_2 | | 62 | 52 | 41 | 30 | L13 | L12 |
| | IC00_0 | 16-bit input capture ch.0 input pin of Multi-function timer 0. ICxx describes channel number. | 22 | 17 | - | 95 | H3 | H4 |
| | IC00_1 | | 75 | 65 | 54 | 43 | G12 | G12 |
| | IC00_2 | | 63 | 53 | 42 | 31 | L12 | K12 |
| | IC01_0 | | 21 | 16 | - | 94 | H2 | H3 |
| | IC01_1 | | 76 | 66 | 55 | 44 | G11 | G11 |
| | IC01_2 | | 64 | 54 | 43 | 32 | K13 | K11 |
| | IC02_0 | | 20 | 15 | - | 93 | G3 | H2 |
| | IC02_1 | | 77 | 67 | 56 | 45 | F12 | G10 |
| | IC02_2 | | 65 | 55 | 44 | 33 | K12 | J12 |
| | IC03_0 | | 19 | 14 | - | 92 | G2 | H1 |
| | IC03_1 | | 78 | 68 | - | 46 | F11 | F13 |
| | IC03_2 | | 66 | 56 | 45 | 34 | J13 | J11 |
| | RTO00_0 (PPG00_0) | Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes. | 24 | 19 | 14 | 97 | J2 | J2 |
| | RTO00_1 (PPG00_1) | | 86 | 71 | 57 | 49 | D13 | D13 |
| | RTO01_0 (PPG00_0) | Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes. | 25 | 20 | 15 | 98 | J3 | J3 |
| | RTO01_1 (PPG00_1) | | 85 | - | - | - | - | E10 |
| | RTO02_0 (PPG02_0) | Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes. | 26 | 21 | 16 | 99 | K1 | J4 |
| | RTO02_1 (PPG02_1) | | 84 | - | - | - | - | E11 |
| | RTO03_0 (PPG02_0) | Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes. | 27 | 22 | 17 | 100 | K2 | K2 |
| | RTO03_1 (PPG02_1) | | 83 | - | - | - | - | E12 |
| | RTO04_0 (PPG04_0) | Wave form generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes. | 28 | 23 | 18 | 1 | L1 | K3 |
| | RTO04_1 (PPG04_1) | | 82 | - | - | - | - | E13 |
| | RTO05_0 (PPG04_0) | Wave form generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes. | 29 | 24 | 19 | 2 | L2 | L1 |
| | RTO05_1 (PPG04_1) | | 81 | - | - | - | - | F10 |

| Pin function | Pin name | Function description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP 120 | LQFP 100 | LQFP 80 | QFP 100 | BGA 112 | BGA 144 |
| Multi-function Timer 1 | DTTI1X_0 | Input signal controlling wave form generator outputs RTO10 to RTO15 of Multi-function timer 1. | 8 | 8 | 8 | 86 | E2 | E2 |
| | DTTI1X_1 | | 55 | - | - | - | - | L10 |
| | FRCK1_0 | 16-bit free-run timer ch.1 external clock input pin | 96 | 81 | 66 | 59 | A9 | D9 |
| | FRCK1_1 | | 50 | 45 | 35 | 23 | L9 | L8 |
| | IC10_0 | 16-bit input capture ch.1 input pin of Multi-function timer 1. ICxx describes channel number. | 95 | 80 | 65 | 58 | A10 | B10 |
| | IC10_1 | | 54 | - | - | - | - | M10 |
| | IC11_0 | | 94 | 79 | 64 | 57 | B10 | A11 |
| | IC11_1 | | 53 | - | - | - | - | K9 |
| | IC12_0 | | 93 | 78 | 63 | 56 | B11 | C10 |
| | IC12_1 | | 52 | - | - | - | - | L9 |
| | IC13_0 | | 92 | 77 | 62 | 55 | A12 | B13 |
| | IC13_1 | | 51 | - | - | - | - | K8 |
| | RTO10_0 (PPG10_0) | Wave form generator output pin of Multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes. | 2 | 2 | 2 | 80 | C1 | C1 |
| | RTO10_1 (PPG10_1) | | 32 | 27 | - | 5 | N2 | N2 |
| | RTO11_0 (PPG10_0) | Wave form generator output pin of Multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes. | 3 | 3 | 3 | 81 | C2 | C2 |
| | RTO11_1 (PPG10_1) | | 33 | 28 | - | 6 | N3 | L2 |
| | RTO12_0 (PPG12_0) | Wave form generator output pin of Multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes. | 4 | 4 | 4 | 82 | C3 | D1 |
| | RTO12_1 (PPG12_1) | | 34 | 29 | - | 7 | M3 | N3 |
| | RTO13_0 (PPG12_0) | Wave form generator output pin of Multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes. | 5 | 5 | 5 | 83 | D1 | D2 |
| | RTO13_1 (PPG12_1) | | 35 | 30 | - | 8 | L3 | M3 |
| | RTO14_0 (PPG14_0) | Wave form generator output pin of Multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes. | 6 | 6 | 6 | 84 | D2 | D3 |
| | RTO14_1 (PPG14_1) | | 36 | 31 | 21 | 9 | M4 | L4 |
| | RTO15_0 (PPG14_0) | Wave form generator output pin of Multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes. | 7 | 7 | 7 | 85 | E1 | E1 |
| | RTO15_1 (PPG14_1) | | 37 | 32 | 22 | 10 | L5 | K5 |
| Quadrature Position/ Revolution Counter 0 | AIN0_0 | QPRC ch.0 AIN input pin | 24 | 19 | 14 | 97 | J2 | J2 |
| | AIN0_1 | | 51 | - | - | - | - | K8 |
| | AIN0_2 | | 2 | 2 | 2 | 80 | C1 | C1 |
| | BIN0_0 | QPRC ch.0 BIN input pin | 25 | 20 | 15 | 98 | J3 | J3 |
| | BIN0_1 | | 52 | - | - | - | - | L9 |
| | BIN0_2 | | 3 | 3 | 3 | 81 | C2 | C2 |
| | ZIN0_0 | QPRC ch.0 ZIN input pin | 26 | 21 | 16 | 99 | K1 | J4 |
| | ZIN0_1 | | 53 | - | - | - | - | K9 |
| | ZIN0_2 | | 4 | 4 | 4 | 82 | C3 | D1 |
| Quadrature Position/ Revolution Counter 1 | AIN1_0 | QPRC ch.1 AIN input pin | 10 | - | - | - | - | E4 |
| | AIN1_1 | | 89 | 74 | - | 52 | C12 | C12 |
| | AIN1_2 | | 48 | 43 | 33 | 21 | L8 | K7 |
| | BIN1_0 | QPRC ch.1 BIN input pin | 11 | - | - | - | - | F1 |
| | BIN1_1 | | 88 | 73 | - | 51 | C13 | D11 |
| | BIN1_2 | | 49 | 44 | 34 | 22 | M9 | M8 |
| | ZIN1_0 | QPRC ch.1 ZIN input pin | 12 | - | - | - | - | F2 |
| | ZIN1_1 | | 87 | 72 | - | 50 | D12 | D12 |
| | ZIN1_2 | | 50 | 45 | 35 | 23 | L9 | L8 |

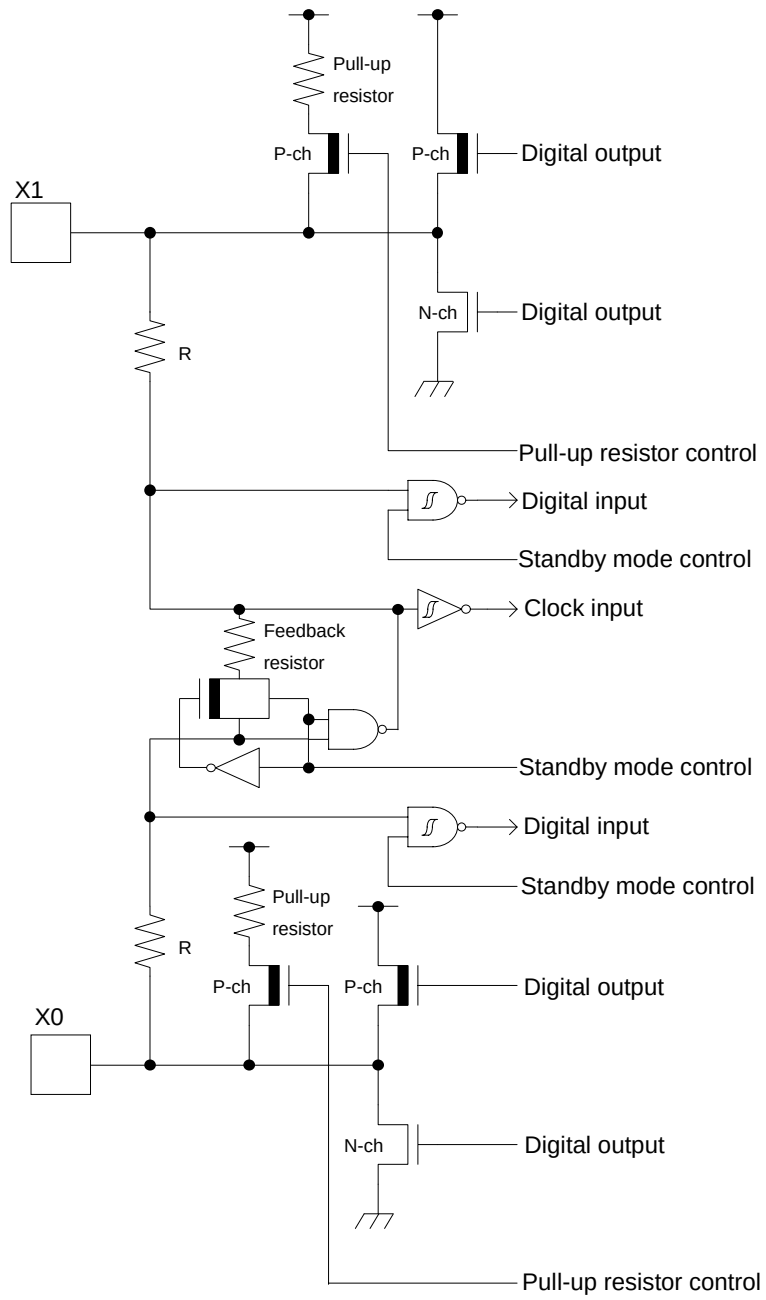
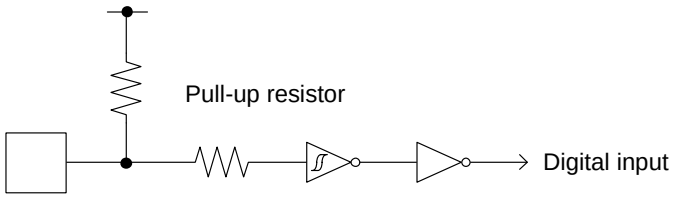
| Pin function | Pin name | Function description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP 120 | LQFP 100 | LQFP 80 | QFP 100 | BGA 112 | BGA 144 |
| Real-time clock | RTCCO_0 | 0.5 seconds pulse output pin of Real-time clock | 115 | 95 | 75 | 73 | B4 | B4 |
| | RTCCO_1 | | 64 | 54 | 43 | 32 | K13 | K11 |
| | RTCCO_2 | | 23 | 18 | 13 | 96 | J1 | J1 |
| | SUBOUT_0 | Sub clock output pin | 115 | 95 | 75 | 73 | B4 | B4 |
| | SUBOUT_1 | | 64 | 54 | 43 | 32 | K13 | K11 |
| | SUBOUT_2 | | 23 | 18 | 13 | 96 | J1 | J1 |
| Low-Power Consumption Mode | WKUP0 | Deep standby mode return signal input pin 0 | 116 | 96 | 76 | 74 | B3 | B3 |
| | WKUP1 | Deep standby mode return signal input pin 1 | 14 | 9 | 9 | 87 | E3 | F4 |
| | WKUP2 | Deep standby mode return signal input pin 2 | 50 | 45 | 35 | 23 | L9 | L8 |
| | WKUP3 | Deep standby mode return signal input pin 3 | 69 | 59 | 48 | 37 | H12 | H11 |
| DAC | DA0 | D/A converter ch.0 analog output pin | 36 | 31 | 21 | 9 | M4 | L4 |
| | DA1 | D/A converter ch.1 analog output pin | 37 | 32 | 22 | 10 | L5 | K5 |
| VBAT | VREGCTL | On-board regulator control pin | 41 | 36 | 26 | 14 | L6 | L6 |
| | VWAKEUP | The return signal input pin from a hibernation state | 42 | 37 | 27 | 15 | M7 | K6 |
| SD I/F | S_CLK_0 | SD memory card interface<br>SD memory card clock output pin | 92 | 77 | 62 | 55 | A12 | B13 |
| | S_CMD_0 | SD memory card interface<br>SD memory card command output | 93 | 78 | 63 | 56 | B11 | C10 |
| | S_DATA1_0 | SD memory card interface<br>SD memory card data bus | 94 | 79 | 64 | 57 | B10 | A11 |
| | S_DATA0_0 | | 95 | 80 | 65 | 58 | A10 | B10 |
| | S_DATA3_0 | | 96 | 81 | 66 | 59 | A9 | D9 |
| | S_DATA2_0 | | 97 | 82 | 67 | 60 | B9 | C9 |
| | S_CD_0 | SD memory card interface<br>SD memory card detection pin | 113 | 93 | 73 | 71 | C5 | B5 |
| | S_WP_0 | SD memory card interface<br>SD memory card write protection | 114 | 94 | 74 | 72 | B5 | C4 |
| Reset | INITX | External Reset Input pin.<br>A reset is valid when INITX = "L". | 38 | 33 | 23 | 11 | M6 | N4 |
| Mode | MD1 | Mode 1 pin.<br>During serial programming to Flash memory, MD1 = "L" must be input. | 56 | 46 | 36 | 24 | M10 | N10 |
| | MD0 | Mode 0 pin.<br>During normal operation, MD0 = "L" must be input. During serial programming to Flash memory, MD0 = "H" must be input. | 57 | 47 | 37 | 25 | M11 | M11 |
| Power | VCC | Power supply Pin | 1 | 1 | 1 | 79 | B1 | B1 |
| | | | 31 | 26 | - | 4 | M1 | M1 |
| | | | 46 | 41 | 31 | 19 | M8 | M9 |
| | | | 61 | 51 | - | 29 | M13 | M13 |
| | | | 91 | 76 | 61 | 54 | B13 | A12 |
| | | | 117 | 97 | 77 | 75 | A4 | A4 |

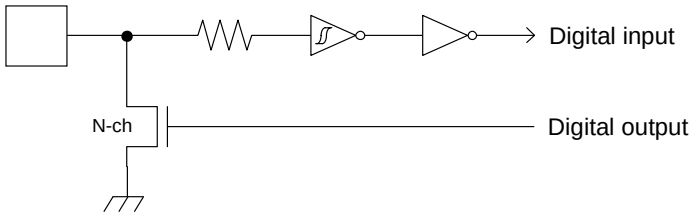
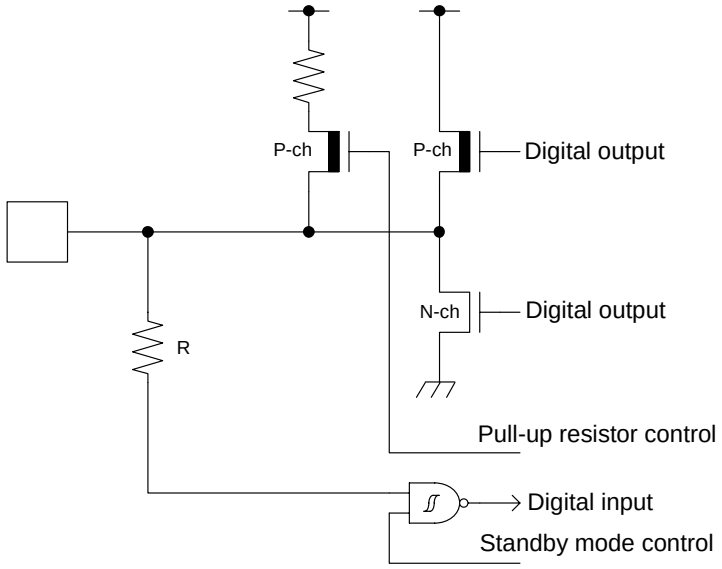
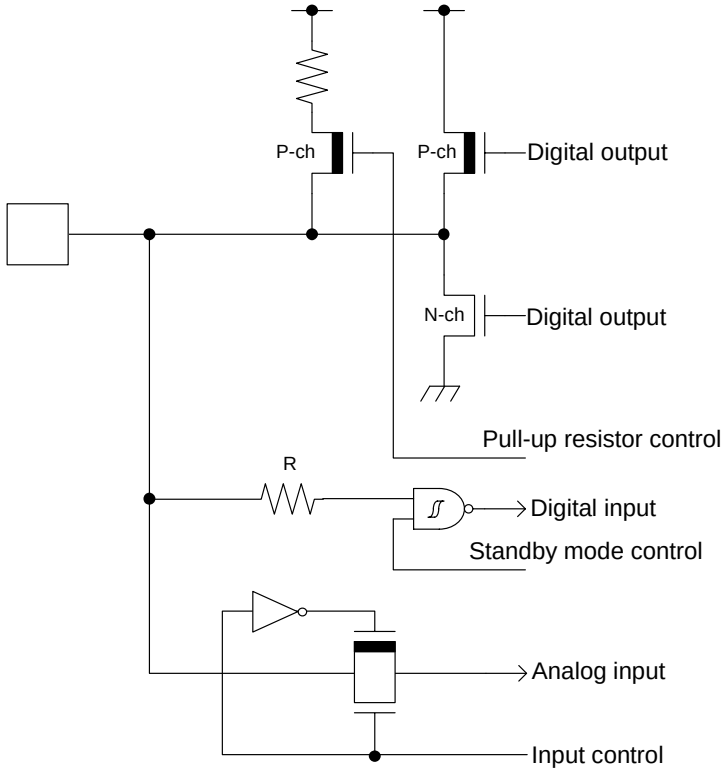
| Pin function | Pin name | Function description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP 120 | LQFP 100 | LQFP 80 | QFP 100 | BGA 112 | BGA 144 |
| GND | VSS | GND Pin | 107 | 92 | - | 70 | A5 | A7 |
| | | | 30 | 25 | 20 | 3 | N1 | N1 |
| | | | 45 | 40 | 30 | 18 | N10 | N9 |
| | | | 60 | 50 | 40 | 28 | N13 | N13 |
| | | | 90 | 75 | 60 | 53 | A13 | A13 |
| | | | 120 | 100 | 80 | 78 | A1 | A1 |
| | | | - | - | - | - | A7 | A5 |
| | | | - | - | - | - | B2 | A8 |
| | | | - | - | - | - | B12 | A10 |
| | | | - | - | - | - | C11 | B2 |
| | | | - | - | - | - | H1 | B11 |
| | | | - | - | - | - | N4 | B12 |
| | | | - | - | - | - | M5 | C3 |
| | | | - | - | - | - | N7 | C11 |
| | | | - | - | - | - | L11 | C13 |
| | | | - | - | - | - | A11 | D4 |
| | | | - | - | - | - | M12 | D10 |
| | | | - | - | - | - | M2 | K1 |
| | | | - | - | - | - | - | K4 |
| | | | - | - | - | - | - | K10 |
| | | | - | - | - | - | - | L3 |
| | | | - | - | - | - | - | L5 |
| | | | - | - | - | - | - | L11 |
| | | | - | - | - | - | - | L13 |
| | | | - | - | - | - | - | M2 |
| GND | VSS | GND Pin | - | - | - | - | - | M4 |
| | | | - | - | - | - | - | M6 |
| | | | - | - | - | - | - | M7 |
| | | | - | - | - | - | - | M12 |
| | | | - | - | - | - | - | N6 |
| Clock | X0 | Main clock (oscillation) input pin | 58 | 48 | 38 | 26 | N11 | N11 |
| | X1 | Main clock (oscillation) I/O pin | 59 | 49 | 39 | 27 | N12 | N12 |
| | X0A | Sub clock (oscillation) input pin | 39 | 34 | 24 | 12 | N5 | N5 |
| | X1A | Sub clock (oscillation) I/O pin | 40 | 35 | 25 | 13 | N6 | M5 |
| | CROUT_0 | Built-in high-speed CR-osc clock output port | 87 | 72 | 58 | 50 | D12 | D12 |
| | CROUT_1 | | 113 | 93 | 73 | 71 | C5 | B5 |
| ADC Power | AVCC | A/D converter and D/A converter analog power supply pin | 70 | 60 | 49 | 38 | H13 | K13 |
| | AVRL | A/D converter analog reference voltage input pin | 72 | 62 | 51 | 40 | F13 | H13 |
| | AVRH | A/D converter analog reference voltage input pin | 73 | 63 | 52 | 41 | E13 | G13 |
| VBAT Power | VBAT | VBAT power supply pin. Backup power supply (battery etc.) and system power supply. | 43 | 38 | 28 | 16 | N8 | N7 |
| ADC GND | AVSS | A/D converter and D/A converter GND pin | 71 | 61 | 50 | 39 | G13 | J13 |
| C pin | C | Power supply stabilization capacity pin | 44 | 39 | 29 | 17 | N9 | N8 |

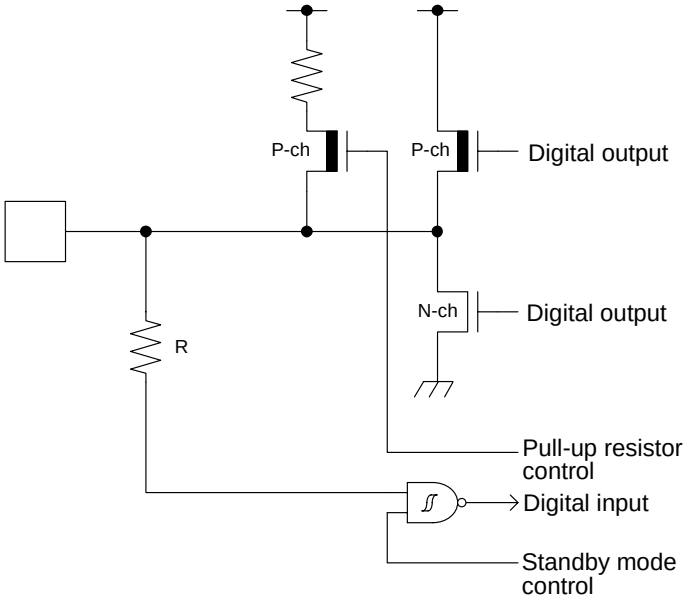
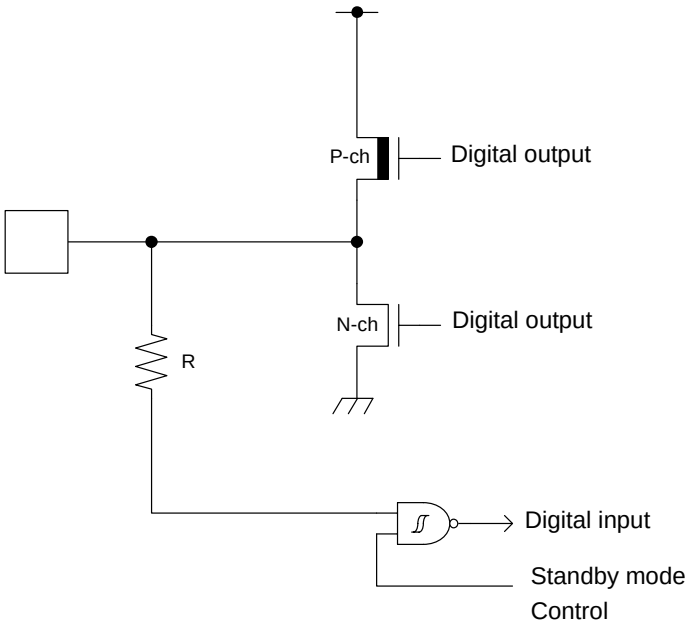
***Note:***

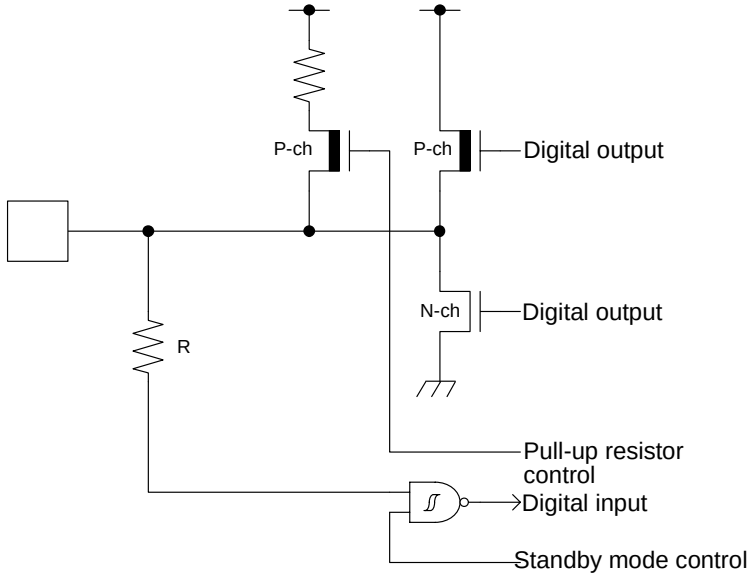
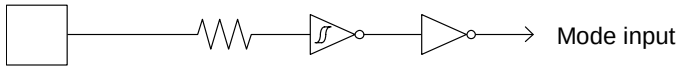
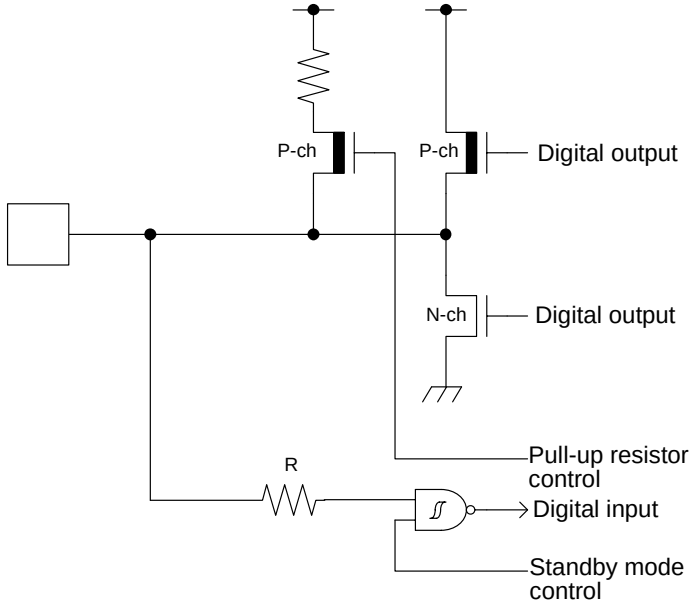
- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

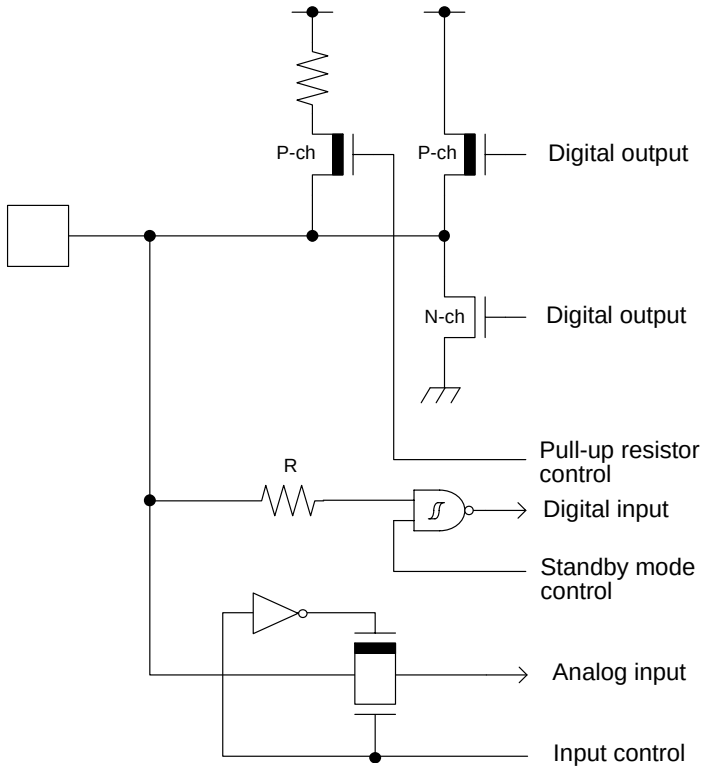
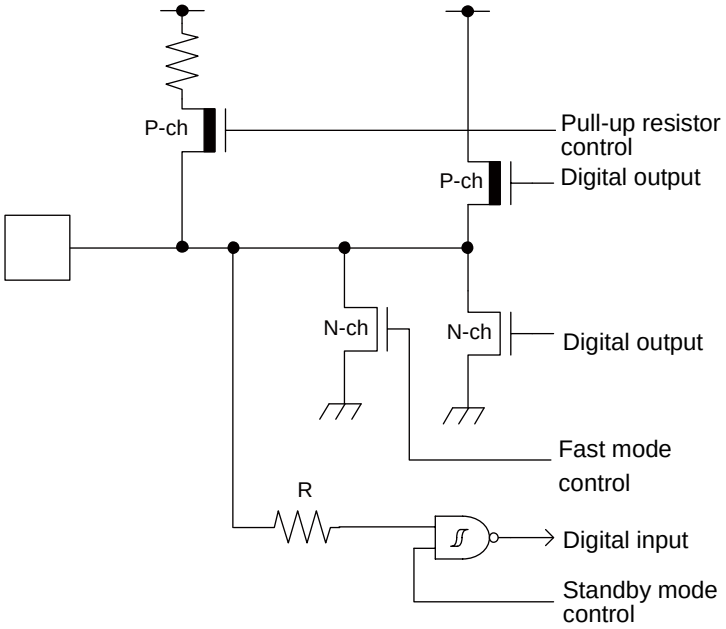
## 5. I/O Circuit Type

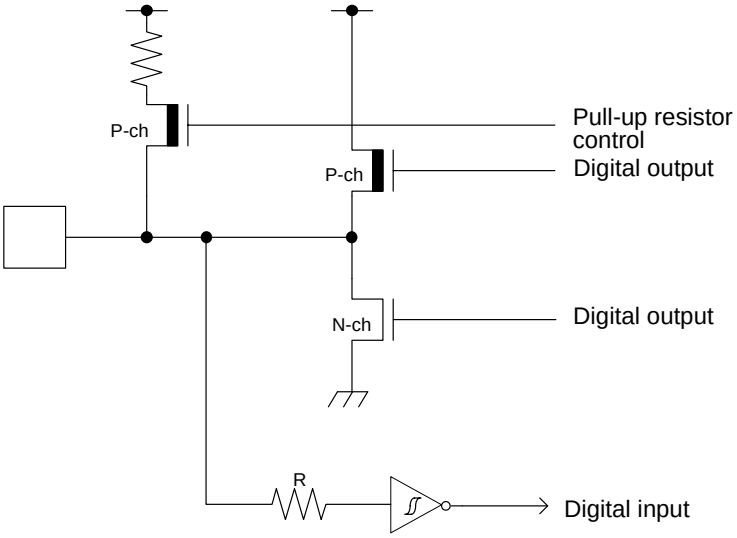
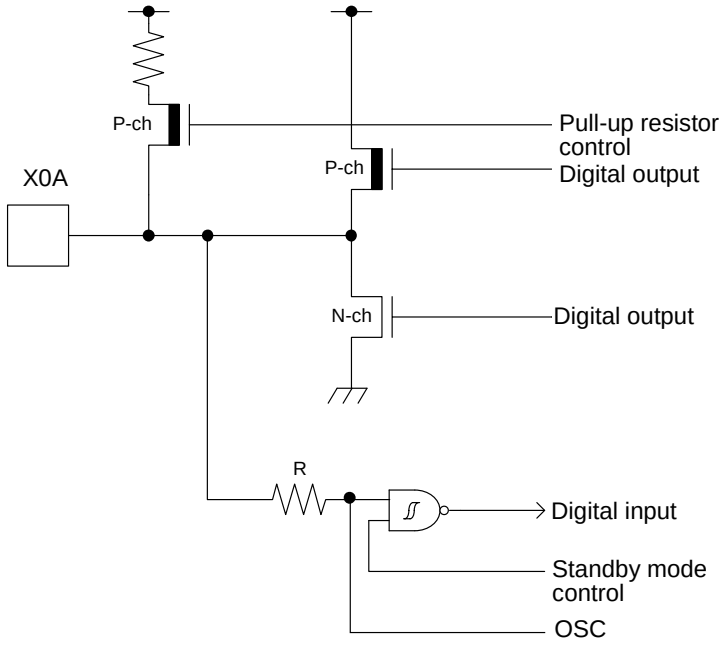
| Type | Circuit | Remarks |
|---|---|---|
| A |  | It is possible to select the main oscillation / GPIO function<br><br>When the main oscillation is selected.<br>• Oscillation feedback resistor : Approximately 1 MΩ<br>• With Standby mode control<br><br>When the GPIO is selected.<br>• CMOS level output.<br>• CMOS level hysteresis input<br>• With pull-up resistor control<br>• With standby mode control<br>• Pull-up resistor : Approximately 50 kΩ<br>• $I_{OH}$ = -4 mA, $I_{OL}$ = 4 mA |
| B |  | • CMOS level hysteresis input<br>• Pull-up resistor : Approximately 50 kΩ |

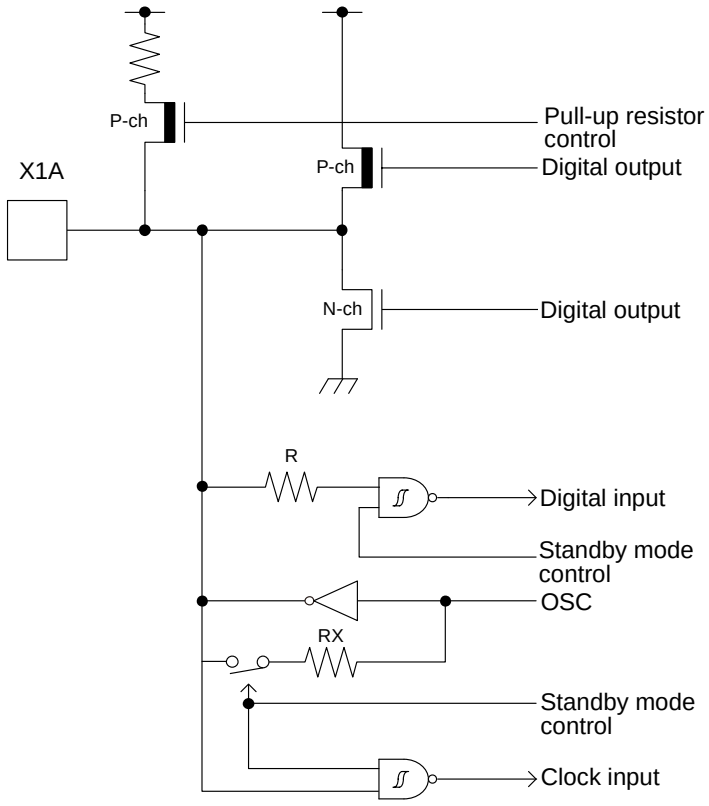
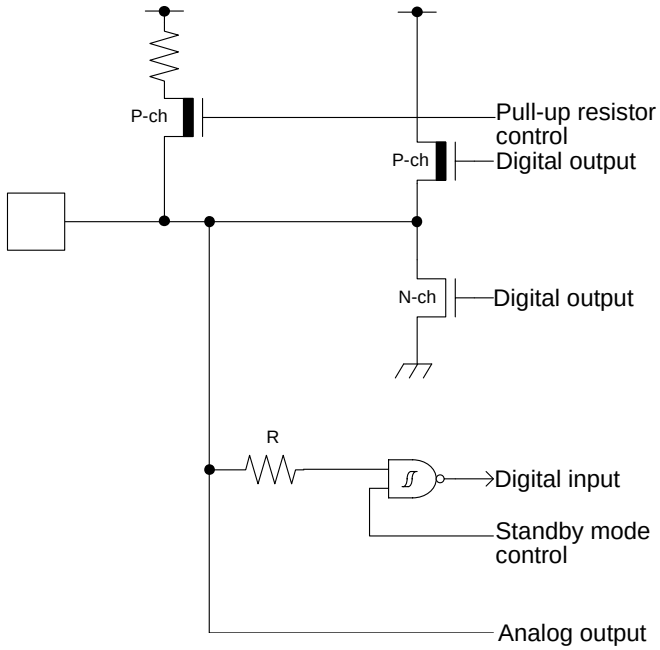
| Type | Circuit | Remarks |
|---|---|---|
| C |  | • Open drain output<br>• CMOS level hysteresis input |
| E |  | • CMOS level output<br>• CMOS level hysteresis input<br>• With pull-up resistor control<br>• With standby mode control<br>• Pull-up resistor<br>: Approximately 50 kΩ<br>• $I_{OH}$ = -4 mA, $I_{OL}$ = 4 mA |
| F |  | • CMOS level output<br>• CMOS level hysteresis input<br>• With input control<br>• Analog input<br>• With pull-up resistor control<br>• With standby mode control<br>• Pull-up resistor<br>: Approximately 50 kΩ<br>• $I_{OH}$ = -4 mA, $I_{OL}$ = 4 mA |

| Type | Circuit | Remarks |
|---|---|---|
| G |  | • CMOS level output<br>• CMOS level hysteresis input<br>• With pull-up resistor control<br>• With standby mode control<br>• Pull-up resistor : Approximately 50 kΩ<br>• $I_{OH}$ = -12 mA, $I_{OL}$ = 12 mA |
| H |  | • CMOS level output<br>• CMOS level hysteresis input<br>• With standby mode control<br>• $I_{OH}$ = -20.5 mA, $I_{OL}$ = 18.5 mA |

| Type | Circuit | Remarks |
|---|---|---|
| I |  | • CMOS level output<br>• CMOS level hysteresis input<br>• 5V tolerant<br>• With standby mode control<br>• Pull-up resistor : Approximately 50 kΩ<br>• $I_{OH}$ = -4 mA, $I_{OL}$ = 4 mA<br>• Available to control of PZR registers. |
| J |  | CMOS level hysteresis input |
| L |  | • CMOS level output<br>• CMOS level hysteresis input<br>• With pull-up resistor control<br>• With standby mode control<br>• Pull-up resistor : Approximately 50 kΩ<br>• $I_{OH}$ = -8 mA, $I_{OL}$ = 8 mA |

| Type | Circuit | Remarks |
|---|---|---|
| M |  | • CMOS level output<br>• CMOS level hysteresis input<br>• With input control<br>• Analog input<br>• With pull-up resistor control<br>• With standby mode control<br>• Pull-up resistor : Approximately 50 kΩ<br>• $I_{OH}$ = -8 mA, $I_{OL}$ = 8 mA |
| N |  | • CMOS level output<br>• CMOS level hysteresis input<br>• 5V tolerant<br>• Pull-up resistor control<br>• Standby mode control<br>• Pull-up resistor: approximately 50 kΩ<br>• $I_{OH}$ = -4 mA, $I_{OL}$ = 4 mA (GPIO)<br>• $I_{OL}$ = 20 mA (Fast mode Plus)<br>• Available to control of PZR register (pseudo-open drain control)<br>• For PZR registers, refer to GPIO in the FM4 Family Peripheral Manual Main Part (002-04856).<br>• When this pin is used as an $I^2C$ pin, the digital output P-ch transistor is always off. |

| Type | Circuit | Remarks |
|---|---|---|
| O |  | ・CMOS level output<br>・CMOS level hysteresis input<br>・5 V tolerant<br>・Pull-up resistor control<br>・Pull-up resistor: approximately 50 kΩ<br>・$I_{OH}$ = -4 mA, $I_{OL}$ = 4 mA<br>・Available to control of PZR register (pseudo-open drain control)<br>・For PZR registers, refer to GPIO in the “FM4 Family Peripheral Manual Main Part (002-04856)”.<br>・For I/O setting, refer to VBAT Domain in the FM4 Family Peripheral Manual Main Part (002-04856). |
| P |  | • CMOS level output<br>• CMOS level hysteresis input<br>• With pull-up resistor control<br>• With standby mode control<br>• Pull-up resistor : Approximately 50 kΩ<br>• $I_{OH}$ = -4 mA, $I_{OL}$ = 4 mA<br>• For I/O setting, refer to VBAT Domain in the Peripheral Manual |

| Type | Circuit | Remarks |
|---|---|---|
| Q |  | It is possible to select the sub oscillation / GPIO function<br><br>When the sub oscillation is selected.<br>• Oscillation feedback resistor : Approximately 10 MΩ<br>• With Standby mode control<br><br>• When the GPIO is selected.<br>• CMOS level output.<br>• CMOS level hysteresis input<br>• With pull-up resistor control<br>• With standby mode control<br>• Pull-up resistor : Approximately 50 kΩ<br>• $I_{OH}$ = -4 mA, $I_{OL}$ = 4 mA<br>• For I/O setting, refer to VBAT Domain in the Peripheral Manual |
| R |  | • CMOS level output<br>• CMOS level hysteresis input<br>• Analog output<br>• With pull-up resistor control<br>• With standby mode control<br>• Pull-up resistor : Approximately 50 kΩ<br>• $I_{OH}$ = -12 mA, $I_{OL}$ = 12 mA (4.5 V to 5.5 V)<br>• $I_{OH}$ = -8 mA, $I_{OL}$ = 8 mA (2.7 V to 4.5 V) |

# 6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

## 6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

### Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

### Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

### Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

### Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

### Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

### Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

### Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

## 6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

### Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

### Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

### Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

### Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

### Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

### Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

## 6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

# 7. Handling Devices

### Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each POWER pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between VCC and VSS near this device.

### Power supply pins

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1 V/µs at a momentary fluctuation such as switching the power supply.

### Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

### Sub crystal oscillator

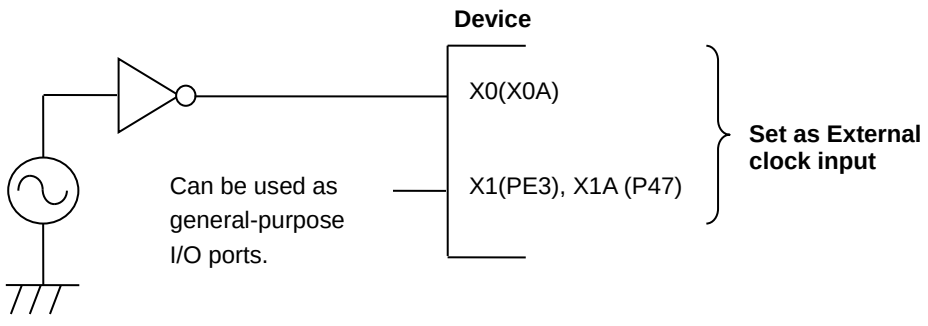
This series sub oscillator circuit is low gain to keep the low current consumption.
The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

- Surface mount type
  - Size: More than 3.2 mm × 1.5 mm
  - Load capacitance: Approximately 6 pF to 7 pF
- Lead type
  - Load capacitance: Approximately 6 pF to 7 pF

### Using an external clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

● Example of Using an External Clock

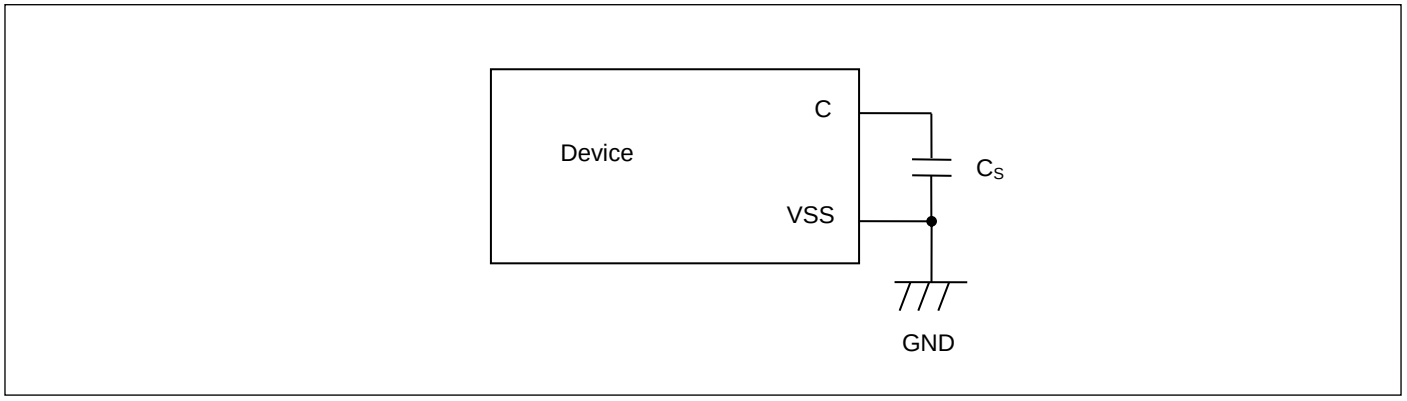


### Handling when using Multi-function serial pin as I²C pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled.
However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

### C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor ($C_S$) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.




### Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

### Notes on power-on

Turn power on/off in the following order or at the same time. The device operates normally after all power on.

VBAT only Power-on is possible when VBAT and VCC turns Power-on and Hibernation control is setting and then VCC turns Power-off. About Hibernation control, see Chapter 7-2: VBAT Domain(A) in FM4 Family Peripheral Manual Main Part(002-04856).
If not using the A/D converter and D/A converter, connect AVCC = VCC and AVSS = VSS.

Turning on : VBAT → VCC

VCC → AVCC → AVRH

Turning off : AVRH → AVCC → VCC

VCC → VBAT

### Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

### Differences in features among the products with different memory sizes and between Flash products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

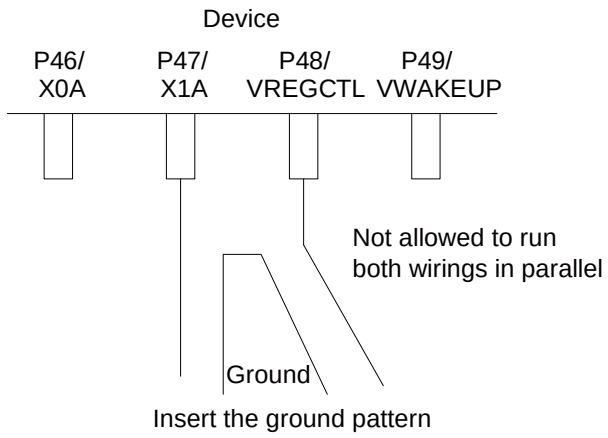
If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

### Pull-Up function of 5V tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5V tolerant I/O.

### Adjoining wiring on circuit board

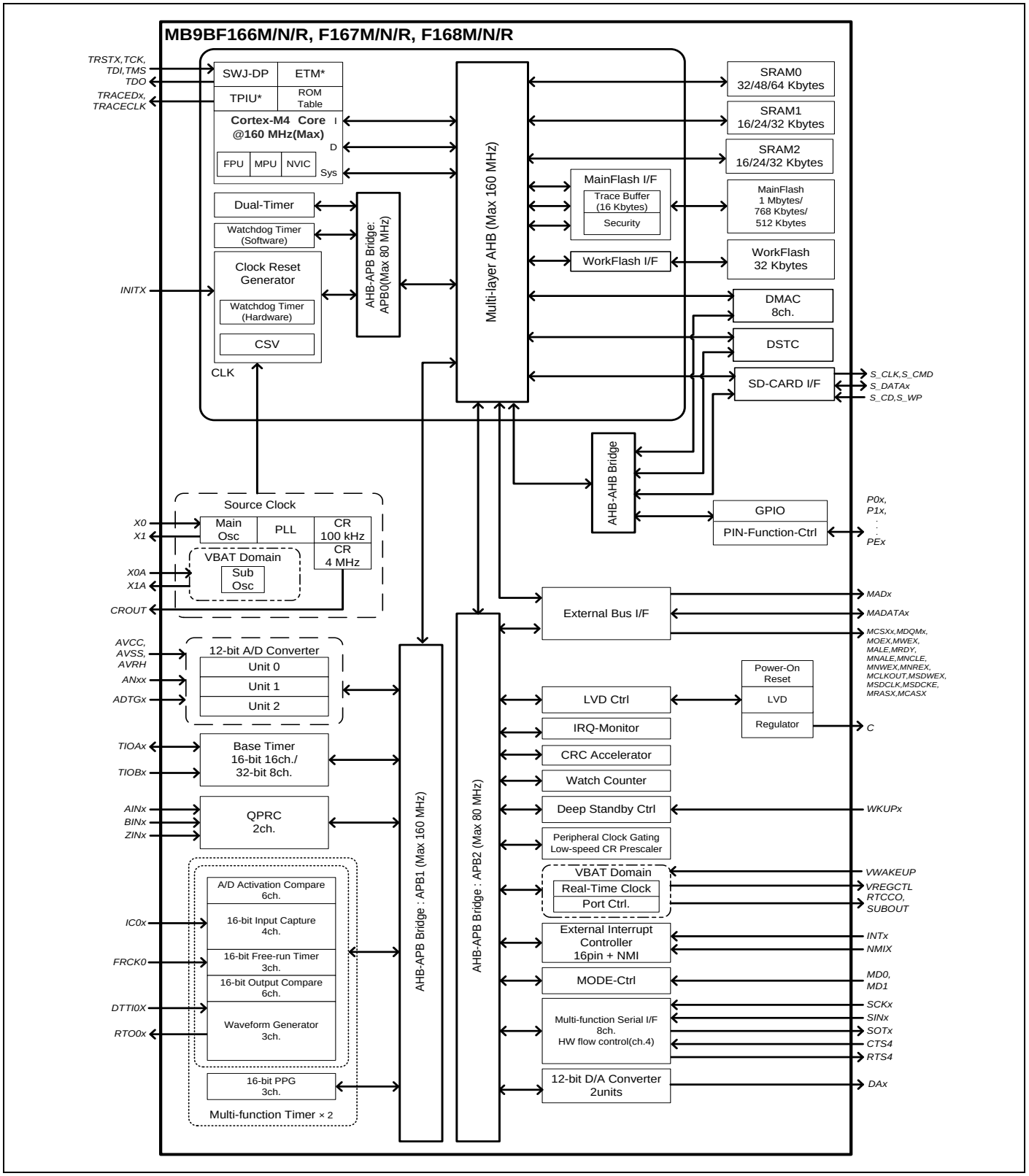
If wiring of the crystal oscillation circuit X1A adjoins and also runs in parallel with the wiring of P48/VREGCTL, there is a possibility that the oscillation erroneously counts because X1A has noise with the change of P48/VREGCTL. Keep as much distance as possible between both wirings and insert the ground pattern between them in order to avoid this possibility.




### Handling when using debug pins

When debug pins(TDO/TMS/TDI/TCK/TRSTX or SWO/SWDIO/SWCLK) are set to GPIO or other peripheral functions, only set them as output, do not set them as input.

## 8. Block Diagram



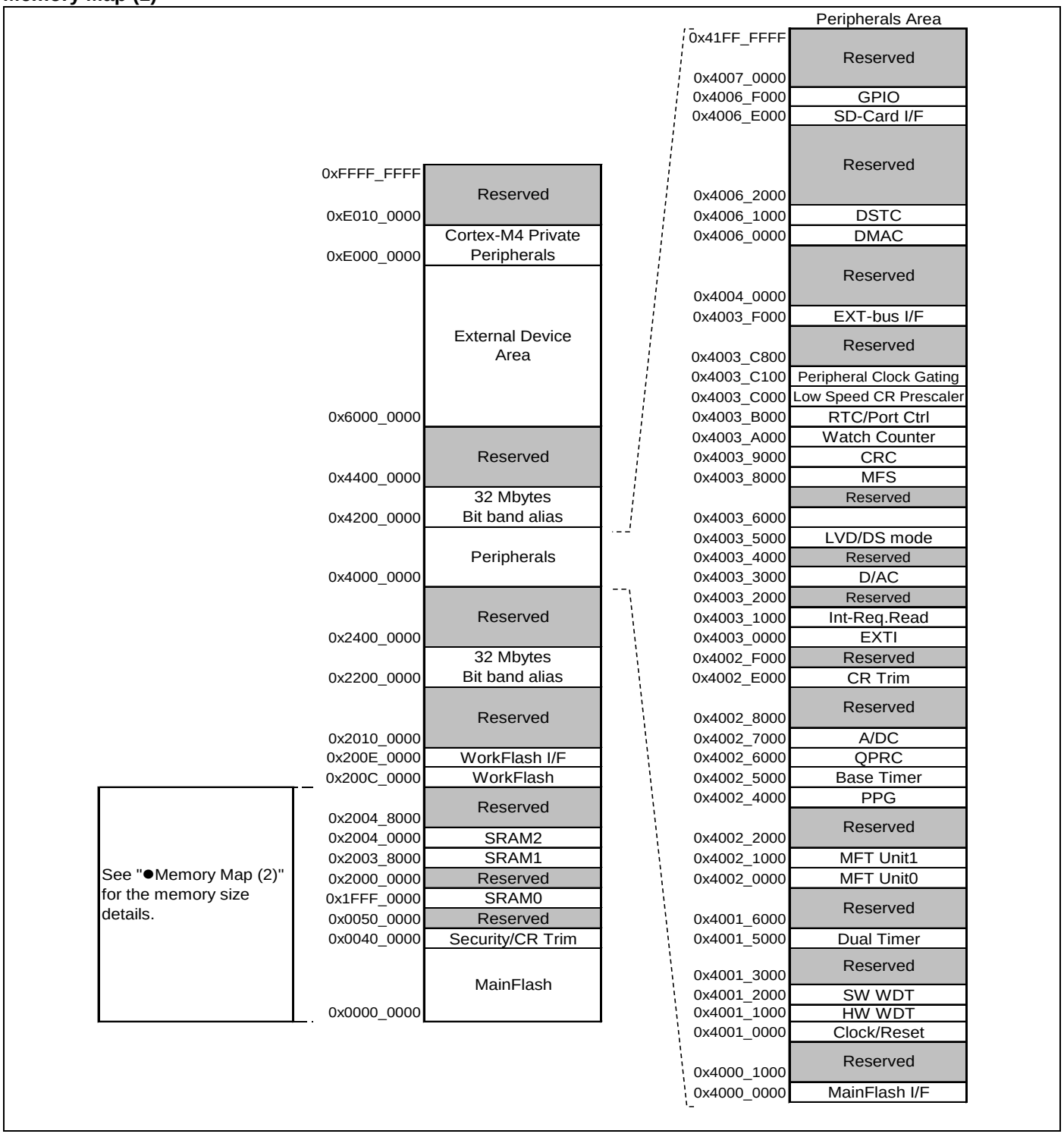

*: For the MB9BF166M, MB9BF167M and MB9BF168M, ETM is not available.

## 9. Memory Size

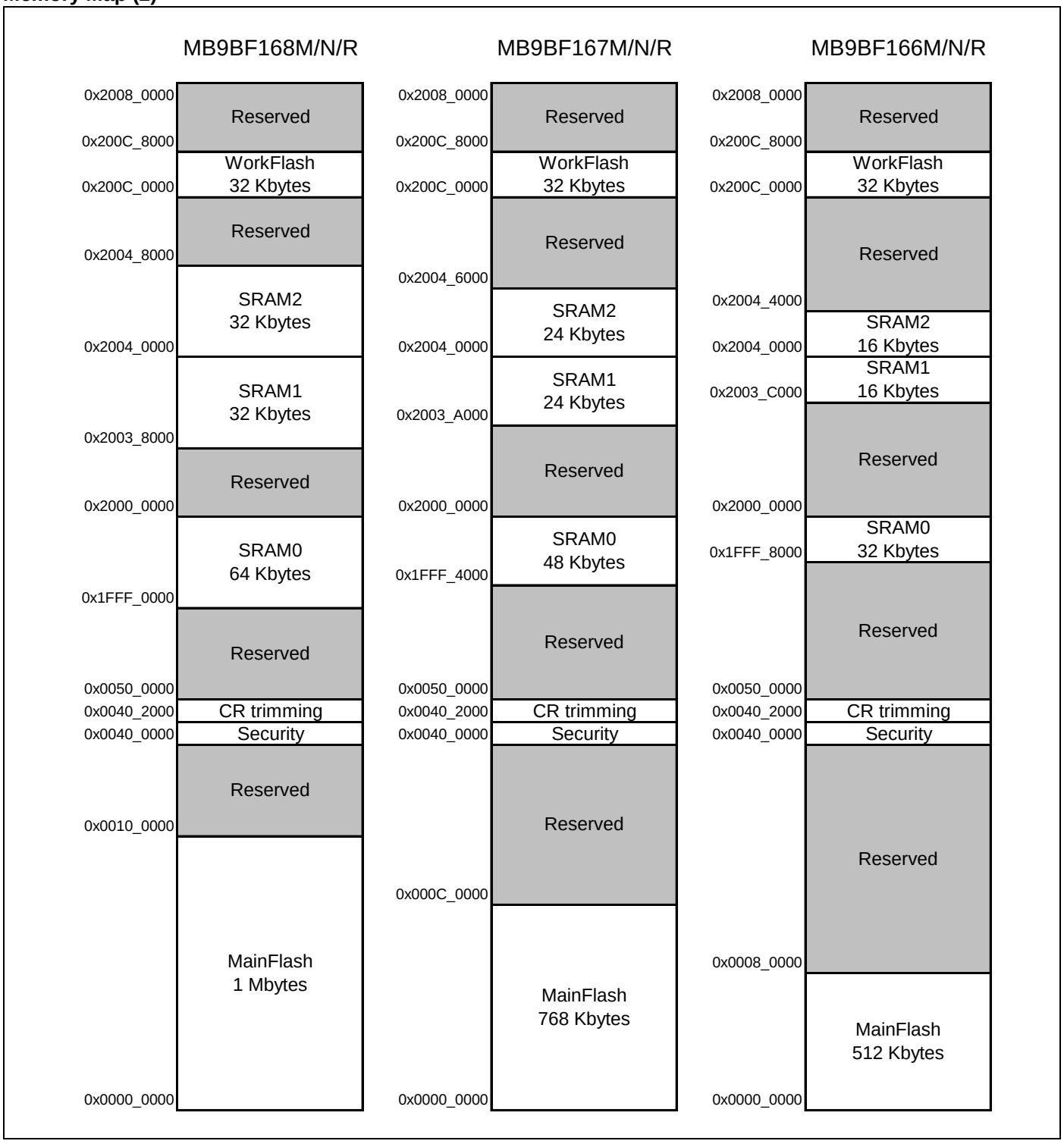
See "Memory size" in "Product Lineup" to confirm the memory size.

## 10. Memory Map

### Memory Map (1)



**Memory Map (2)**


MB9BF168M/N/R
0x2008_0000
Reserved
0x200C_8000
WorkFlash
32 Kbytes
0x200C_0000
Reserved
0x2004_8000
SRAM2
32 Kbytes
0x2004_0000
SRAM1
32 Kbytes
0x2003_8000
Reserved
0x2000_0000
SRAM0
64 Kbytes
0x1FFF_0000
Reserved
0x0050_0000
0x0040_2000
CR trimming
0x0040_0000
Security
Reserved
0x0010_0000
MainFlash
1 Mbytes
0x0000_0000
MB9BF167M/N/R
0x2008_0000
Reserved
0x200C_8000
WorkFlash
32 Kbytes
0x200C_0000
Reserved
0x2004_6000
SRAM2
24 Kbytes
0x2004_0000
SRAM1
24 Kbytes
0x2003_A000
Reserved
0x2000_0000
SRAM0
48 Kbytes
0x1FFF_4000
Reserved
0x0050_0000
0x0040_2000
CR trimming
0x0040_0000
Security
Reserved
0x000C_0000
MainFlash
768 Kbytes
0x0000_0000
MB9BF166M/N/R
0x2008_0000
Reserved
0x200C_8000
WorkFlash
32 Kbytes
0x200C_0000
Reserved
0x2004_4000
SRAM2
16 Kbytes
0x2004_0000
SRAM1
16 Kbytes
0x2003_C000
Reserved
0x2000_0000
SRAM0
32 Kbytes
0x1FFF_8000
Reserved
0x0050_0000
0x0040_2000
CR trimming
0x0040_0000
Security
Reserved
0x0008_0000
MainFlash
512 Kbytes
0x0000_0000

## Peripheral Address Map

| Start address | End address | Bus | Peripherals |
|---|---|---|---|
| 0x4000_0000 | 0x4000_0FFF | AHB | MainFlash I/F register |
| 0x4000_1000 | 0x4000_FFFF | | Reserved |
| 0x4001_0000 | 0x4001_0FFF | APB0 | Clock/Reset Control |
| 0x4001_1000 | 0x4001_1FFF | | Hardware Watchdog timer |
| 0x4001_2000 | 0x4001_2FFF | | Software Watchdog timer |
| 0x4001_3000 | 0x4001_4FFF | | Reserved |
| 0x4001_5000 | 0x4001_5FFF | | Dual-Timer |
| 0x4001_6000 | 0x4001_FFFF | | Reserved |
| 0x4002_0000 | 0x4002_0FFF | APB1 | Multi-function timer unit0 |
| 0x4002_1000 | 0x4002_1FFF | | Multi-function timer unit1 |
| 0x4002_2000 | 0x4003_FFFF | | Reserved |
| 0x4002_4000 | 0x4002_4FFF | | PPG |
| 0x4002_5000 | 0x4002_5FFF | | Base Timer |
| 0x4002_6000 | 0x4002_6FFF | | Quadrature Position/Revolution Counter |
| 0x4002_7000 | 0x4002_7FFF | | A/D Converter |
| 0x4002_8000 | 0x4002_DFFF | | Reserved |
| 0x4002_E000 | 0x4002_EFFF | | Internal CR trimming |
| 0x4002_F000 | 0x4002_FFFF | | Reserved |
| 0x4003_0000 | 0x4003_0FFF | APB2 | External Interrupt Controller |
| 0x4003_1000 | 0x4003_1FFF | | Interrupt Request Batch-Read Function |
| 0x4003_2000 | 0x4003_4FFF | | Reserved |
| 0x4003_3000 | 0x4003_3FFF | | D/A Converter |
| 0x4003_4000 | 0x4003_4FFF | | Reserved |
| 0x4003_5000 | 0x4003_57FF | | Low Voltage Detector |
| 0x4003_5800 | 0x4003_5FFF | | Deep standby mode Controller |
| 0x4003_6000 | 0x4003_7FFF | | Reserved |
| 0x4003_8000 | 0x4003_8FFF | | Multi-function serial Interface |
| 0x4003_9000 | 0x4003_9FFF | | CRC |
| 0x4003_A000 | 0x4003_AFFF | | Watch Counter |
| 0x4003_B000 | 0x4003_BFFF | | RTC/Port Ctrl |
| 0x4003_C000 | 0x4003_C0FF | | Low-speed CR Prescaler |
| 0x4003_C100 | 0x4003_C7FF | | Peripheral Clock Gating |
| 0x4003_C800 | 0x4003_EFFF | | Reserved |
| 0x4003_F000 | 0x4003_FFFF | | External Memory interface |
| 0x4004_0000 | 0x4005_FFFF | AHB | Reserved |
| 0x4006_0000 | 0x4006_0FFF | | DMAC register |
| 0x4006_1000 | 0x4006_3FFF | | DSTC register |
| 0x4006_4000 | 0x4006_DFFF | | Reserved |
| 0x4006_E000 | 0x4006_EFFF | | SD-Card I/F |
| 0x4006_F000 | 0x4006_FFFF | | GPIO |
| 0x4006_7000 | 0x41FF_FFFF | | Reserved |
| 0x200E_0000 | 0x200E_FFFF | | WorkFlash I/F register |

## 11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX = 0

  This is the period when the INITX pin is the "L" level.

- INITX = 1

  This is the period when the INITX pin is the "H" level.

- SPL = 0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "0".

- SPL = 1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "1".

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at "0"

  This is the status that the input function cannot be used. Internal input is fixed at "L".

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

- Setting prohibition

  Prohibition of a setting by specification limitation.

## List of Pin Status

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or SLEEP mode state | TIMER mode, RTC mode, or STOP mode state | | Deep standby RTC mode or Deep standby STOP mode state | | Return from Deep standby mode state |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | | Power supply stable | | Power supply stable |
| | | - | INITX = 0 | INITX = 1 | INITX = 1 | INITX = 1 | | INITX = 1 | | INITX = 1 |
| | | - | - | - | - | SPL = 0 | SPL = 1 | SPL = 0 | SPL = 1 | - |
| A | GPIO selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at "0" | GPIO selected Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | GPIO selected |
| | Main crystal oscillator input pin/ External main clock input selected | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled |
| B | GPIO selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at "0" | GPIO selected Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | GPIO selected |
| | External main clock input selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at "0" | Maintain previous state | Hi-Z / Internal input fixed at "0" | Maintain previous state |
| | Main crystal oscillator output pin | Hi-Z / Internal input fixed at "0"/ or Input enable | Hi-Z / Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0" | Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0" | Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0" | Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0" | Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0" | Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0" |
| C | INITX input pin | Pull-up / Input enabled | Pull-up / Input enabled | Pull-up / Input enabled | Pull-up / Input enabled | Pull-up / Input enabled | Pull-up / Input enabled | Pull-up / Input enabled | Pull-up / Input enabled | Pull-up / Input enabled |
| D | Mode input pin | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled |
| E | Mode input pin | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled |
| | GPIO selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z / Input enabled | GPIO selected | Hi-Z / Input enabled | GPIO selected |

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or SLEEP mode state | TIMER mode, RTC mode, or STOP mode state | | Deep standby RTC mode or Deep standby STOP mode state | | Return from Deep standby mode state |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | | Power supply stable | | Power supply stable |
| | | - | INITX = 0 | INITX = 1 | INITX = 1 | INITX = 1 | | INITX = 1 | | INITX = 1 |
| | | - | - | - | - | SPL = 0 | SPL = 1 | SPL = 0 | SPL = 1 | - |
| F | NMIX selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state | WKUP input enabled | Hi-Z / WKUP input enabled | GPIO selected |
| | Resource other than above selected | Hi-Z | Hi-Z / Input enabled | Hi-Z / Input enabled | | | Hi-Z / Internal input fixed at "0" | | | |
| | GPIO selected | | | | | | | | | Maintain previous state |
| G | JTAG selected | Hi-Z | Pull-up / Input enabled | Pull-up / Input enabled | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state |
| | GPIO selected | Setting disabled | Setting disabled | Setting disabled | | | Hi-Z / Internal input fixed at "0" | GPIO selected Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | GPIO selected |
| H | JTAG selected | Hi-Z | Pull-up / Input enabled | Pull-up / Input enabled | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state |
| | Resource other than above selected | Setting disabled | Setting disabled | Setting disabled | | | Hi-Z / Internal input fixed at "0" | GPIO selected Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | GPIO selected |
| | GPIO selected | | | | | | | | | |
| I | Resource selected | Hi-Z | Hi-Z / Input enabled | Hi-Z / Input enabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at "0" | GPIO selected Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | GPIO selected |
| | GPIO selected | | | | | | | | | |
| J | Analog output selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | *2 | *3 | GPIO selected Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | GPIO selected |
| | Resource other than above selected | Hi-Z | Hi-Z / Input enabled | Hi-Z / Input enabled | | Maintain previous state | Hi-Z / Internal input fixed at "0" | | | |
| | GPIO selected | | | | | | | | | |

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or SLEEP mode state | TIMER mode, RTC mode, or STOP mode state | | Deep standby RTC mode or Deep standby STOP mode state | | Return from Deep standby mode state |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | | Power supply stable | | Power supply stable |
| | | - | INITX = 0 | INITX = 1 | INITX = 1 | INITX = 1 | | INITX = 1 | | INITX = 1 |
| | | - | - | - | - | SPL = 0 | SPL = 1 | SPL = 0 | SPL = 1 | - |
| K | External interrupt enabled selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state | GPIO selected Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | GPIO selected |
| | Resource other than above selected | Hi-Z | Hi-Z / Input enabled | Hi-Z / Input enabled | | | Hi-Z / Internal input fixed at "0" | | | |
| | GPIO selected | | | | | | | | | |
| L | Analog input selected | Hi-Z | Hi-Z / Internal input fixedat "0" / Analog input enabled | Hi-Z / Internal input fixedat "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled |
| | Resource other than above selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at "0" | GPIO selected Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | GPIO selected |
| | GPIO selected | | | | | | | | | |
| M | Analog input selected | Hi-Z | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled |
| | External interrupt enabled selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state | GPIO selected Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | GPIO selected |
| | Resource other than above selected | | | | | | Hi-Z / Internal input fixed at "0" | | | |
| | GPIO selected | | | | | | | | | |

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or SLEEP mode state | TIMER mode, RTC mode, or STOP mode state | | Deep standby RTC mode or Deep standby STOP mode state | | Return from Deep standby mode state |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | | Power supply stable | | Power supply stable |
| | | - | INITX = 0 | INITX = 1 | INITX = 1 | INITX = 1 | | INITX = 1 | | INITX = 1 |
| | | - | - | - | - | SPL = 0 | SPL = 1 | SPL = 0 | SPL = 1 | - |
| N | Analog input selected | Hi-Z | Hi-Z / Internal input fixed at"0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled |
| | Trace selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Trace output | GPIO selected Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | GPIO selected |
| | Resource other than above selected | | | | | | Hi-Z / Internal input fixed at "0" | | | |
| | GPIO selected | | | | | | | | | |
| O | Analog input selected | Hi-Z | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled |
| | Trace selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Trace output | GPIO selected Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | GPIO selected |
| | External interrupt enabled selected | | | | | | Maintain previous state | | | |
| | Resource other than above selected | | | | | | Hi-Z / Internal input fixed at "0" | | | |
| | GPIO selected | | | | | | | | | |

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or SLEEP mode state | TIMER mode, RTC mode, or STOP mode state | | Deep standby RTC mode or Deep standby STOP mode state | | Return from Deep standby mode state |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | | Power supply stable | | Power supply stable |
| | | - | INITX = 0 | INITX = 1 | INITX = 1 | INITX = 1 | | INITX = 1 | | INITX = 1 |
| | | - | - | - | - | SPL = 0 | SPL = 1 | SPL = 0 | SPL = 1 | - |
| P | Analog input selected | Hi-Z | Hi-Z / Internal input fixedat "0" / Analog input enabled | Hi-Z / Internal input fixedat "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled |
| | WKUP enabled | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state | WKUP input enabled | Hi-Z / WKUP input enabled | GPIO selected |
| | Resource other than above selected | | | | | | Hi-Z / Internal input fixed at "0" | GPIO selected Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | |
| | GPIO selected | | | | | | | | | |
| Q | WKUP enabled | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state | WKUP input enabled | Hi-Z / WKUP input enabled | GPIO selected |
| | External interrupt enabled selected | | | | | | | GPIO selected Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | |
| | Resource other than above selected | Hi-Z | Hi-Z / Input enabled | Hi-Z / Input enabled | | | Hi-Z / Internal input fixed at "0" | | | |
| | GPIO selected | | | | | | | | | |
| R | GPIO selected | Hi-Z | Hi-Z / Input enabled | Hi-Z / Input enabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at "0" | GPIO selected Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | GPIO selected |

*1: Oscillation is stopped at Sub timer mode, sub CR timer mode, RTC mode, STOP mode, Deep standby RTC mode, and Deep standby STOP mode.

*2: Maintain previous state at timer mode. GPIO selected Internal input fixed at "0" at RTC mode, STOP mode.

*3: Maintain previous state at timer mode. Hi-Z/Internal input fixed at "0" at RTC mode, STOP mode.

## List of VBAT Domain Pin Status

| VBAT pin status type | Function group | Power-on reset*1 | INITX input state | Device internal reset state | Run mode or SLEEP mode state | TIMER mode, RTC mode, or STOP mode state | | Deep standby RTC mode or Deep standby STOP mode state | | Return from Deep standby mode state | VBAT RTC mode state | Return from VBAT RTC mode state |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | | Power supply stable | | Power supply stable | Power supply stable | Power supply stable |
| | | - | INITX = 0 | INITX = 1 | INITX = 1 | INITX = 1 | | INITX = 1 | | INITX = 1 | - | - |
| | | - | - | - | - | SPL = 0 | SPL = 1 | SPL = 0 | SPL = 1 | - | - | - |
| S | GPIO selected | Setting disabled | Maintain Previous state | Maintain Previous state | Maintain previous state | Maintain previous state | Maintain Previous state | Maintain Previous state | Maintain Previous state | Maintain Previous state | Setting prohibition | - |
| | Sub crystal oscillator input pin / External sub clock input selected | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Maintain previous state | Maintain previous state |
| T | GPIO selected | Setting disabled | Maintain Previous state | Maintain Previous state | Maintain previous state | Maintain previous state | Maintain Previous state | Maintain Previous state | Maintain Previous state | Maintain Previous state | Setting prohibition | - |
| | External sub clock input selected | Setting disabled | Maintain Previous state | Maintain Previous state | Maintain previous state | Maintain previous state | Maintain Previous state | Maintain previous state | Maintain Previous state | Maintain previous state | Maintain previous state | Maintain previous state |
| | Sub crystal oscillator output pin | Hi-Z / Internal input fixed at "0"/ or Input enable | Maintain Previous state | Maintain Previous state | Maintain previous state | Maintain previous state/When oscillation stops, Hi-Z*2 | Maintain previous state/When oscillation stops, Hi-Z*2 | Maintain previous state/When oscillation stops, Hi-Z*2 | Maintain previous state/When oscillation stops, Hi-Z*2 | Maintain Previous state | Maintain previous state | Maintain previous state |
| U | Resource selected / GPIO selected | Hi-Z | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state |

*1: When VBAT and VCC power on.

*2: When the SOSCNTL bit in the WTOSCCNT register is 0, the sub crystal oscillator output pin is maintained in the previous state.
When the SOSCNTL bit in the WTOSCCNT register is 1, oscillation is stopped at Stop mode and Deep Standby Stop

# 12. Electrical Characteristics

## 12.1 Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage *1, *2 | $V_{CC}$ | $V_{SS}$ - 0.5 | $V_{SS}$ + 6.5 | V | |
| Power supply voltage (VBAT) *1, *3 | $V_{BAT}$ | $V_{SS}$ - 0.5 | $V_{SS}$ + 6.5 | V | |
| Analog power supply voltage *1, *4 | $AV_{CC}$ | $V_{SS}$ - 0.5 | $V_{SS}$ + 6.5 | V | |
| Analog reference voltage *1, *4 | AVRH | $V_{SS}$ - 0.5 | $V_{SS}$ + 6.5 | V | |
| Input voltage *1 | $V_I$ | $V_{SS}$ - 0.5 | $V_{CC}$ + 0.5 (≤ 6.5V) | V | |
| | | $V_{SS}$ - 0.5 | $V_{SS}$ + 6.5 | V | 5V tolerant |
| Analog pin input voltage *1 | $V_{IA}$ | $V_{SS}$ - 0.5 | $AV_{CC}$ + 0.5 (≤ 6.5V) | V | |
| Output voltage *1 | $V_O$ | $V_{SS}$ - 0.5 | $V_{CC}$ + 0.5 (≤ 6.5V) | V | |
| "L" level maximum output current *5 | $I_{OL}$ | - | 10 | mA | 4mA type |
| | | | 20 | mA | 8mA type |
| | | | 20 | mA | 12mA type |
| | | | 22.4 | mA | $I^2C$ Fm+ |
| "L" level average output current *6 | $I_{OLAV}$ | - | 4 | mA | 4mA type |
| | | | 8 | mA | 8mA type |
| | | | 12 | mA | 12mA type |
| | | | 20 | mA | $I^2C$ Fm+ |
| "L" level total maximum output current | $\sum I_{OL}$ | - | 100 | mA | |
| "L" level total maximum output current *7 | $\sum I_{OLAV}$ | - | 50 | mA | |
| "H" level maximum output current *5 | $I_{OH}$ | - | - 10 | mA | 4mA type |
| | | | 20 | mA | 8mA type |
| | | | - 20 | mA | 12mA type |
| "H" level average output current *6 | $I_{OHAV}$ | - | - 4 | mA | 4mA type |
| | | | 8 | mA | 8mA type |
| | | | - 12 | mA | 12mA type |
| "H" level total maximum output current | $\sum I_{OH}$ | - | - 100 | mA | |
| "H" level total average output current *7 | $\sum I_{OHAV}$ | - | - 50 | mA | |
| Storage temperature | $T_{STG}$ | - 55 | + 150 | °C | |

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0V$.

*2: $V_{CC}$ must not drop below $V_{SS}$ - 0.5V.

*3: $V_{BAT}$ must not drop below $V_{SS}$ - 0.5V.

*4: Ensure that the voltage does not exceed $V_{CC}$ + 0.5V, for example, when the power is turned on.

*5: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*6: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100ms period.

*7: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100ms.

***WARNING:***

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.*
  *Do not exceed any of these ratings.*

## 12.2 Recommended Operating Conditions

| Parameter | | Symbol | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Power supply voltage | | $V_{CC}$ | - | 2.7*3 | 5.5 | V | |
| Power supply voltage (VBAT) | | $V_{BAT}$ | - | 2.7 | 5.5 | V | |
| Analog power supply voltage | | $AV_{CC}$ | - | 2.7 | 5.5 | V | $AV_{CC} = V_{CC}$ |
| Analog reference voltage | | AVRH | - | *2 | $AV_{CC}$ | V | |
| Operating temperature | Junction temperature | Tj | - | - 40 | + 125 | °C | |
| | Ambient temperature | $T_A$ | - | - 40 | *1 | °C | |

*1: The maximum temperature of the ambient temperature ($T_A$) can guarantee a range that does not exceed the junction temperature (Tj).

The calculation formula of the ambient temperature ($T_A$) is shown below.

$T_A(Max) = Tj(Max) - Pd(Max) \times \theta ja$

Pd: Power dissipation (W)
θja: Package thermal resistance (°C/W)

$Pd\ (Max) = V_{CC} \times I_{CC}\ (Max) + \Sigma\ (I_{OL} \times V_{OL}) + \Sigma\ ((V_{CC} - V_{OH}) \times (-I_{OH}))$

$I_{OL}$: "L" level output current
$I_{OH}$: "H" level output current
$V_{OL}$: "L" level output voltage
$V_{OH}$: "H" level output voltage

*2: The minimum value of Analog reference voltage depends on the value of compare clock cycle (Tcck). See 12.5. 12-bit A/D Converter" for the details.

*3: Between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate.

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

**Table for package thermal resistance and maximum permissible power**

| Package | Printed circuit board | Thermal resistance θja (°C/W) | Maximum permissible power (mW) | |
|---|---|---|---|---|
| | | | $T_A$ = +85°C | $T_A$ = +105°C |
| LQH080 (0.5mm pitch) | Single-layered both sides | 60 | 667 | 333 |
| | 4 layers | 39 | 1026 | 513 |
| LQJ080 (0.65mm pitch) | Single-layered both sides | 58 | 690 | 335 |
| | 4 layers | 38 | 1053 | 526 |
| LQI100 (0.5mm pitch) | Single-layered both sides | 57 | 702 | 351 |
| | 4 layers | 38 | 1053 | 526 |
| PQH100 (0.65mm pitch) | Single-layered both sides | 48 | 833 | 417 |
| | 4 layers | 34 | 1177 | 588 |
| LQM120 (0.5mm pitch) | Single-layered both sides | 62 | 645 | 323 |
| | 4 layers | 43 | 930 | 465 |
| LDC112 (0.5mm pitch) | Single-layered both sides | 60 | 667 | 333 |
| | 4 layers | 40 | 1000 | 500 |
| LDC144 (0.5mm pitch) | Single-layered both sides | 55 | 727 | 364 |
| | 4 layers | 40 | 1000 | 500 |

***WARNING:***

- *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
  *Any use of semiconductor devices will be under their recommended operating condition.*
  *Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.*
  *No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

### Calculation method of power dissipation (Pd)

The power dissipation is shown in the following formula.

$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$

$I_{OL}$: "L" level output current
$I_{OH}$: "H" level output current
$V_{OL}$: "L" level output voltage
$V_{OH}$: "H" level output voltage

$I_{CC}$ is a current consumed in device.
It can be analyzed as follows.

$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$

$I_{CC}(INT)$: Current consumed in internal logic and memory, etc. through regulator
$\Sigma I_{CC}(IO)$: Sum of current (I/O switching current) consumed in output pin

For $I_{CC}$ (INT), it can be anticipated by 12.3.1 “Current Rating" in 12.3. DC Characteristics" (This rating value does not include $I_{CC}$ (IO) for a value at pin fixed).
For Icc (IO), it depends on system used by customers.
The calculation formula is shown below.

$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times fsw$

$C_{INT}$: Pin internal load capacitance
$C_{EXT}$: External load capacitance of output pin
$f_{SW}$: Pin switching frequency

| Parameter | Symbol | Conditions | Capacitance value |
|---|---|---|---|
| Pin internal load capacitance | $C_{INT}$ | 4mA type | 1.93pF |
| | | 8mA type | 3.45pF |
| | | 12mA type | 3.42pF |

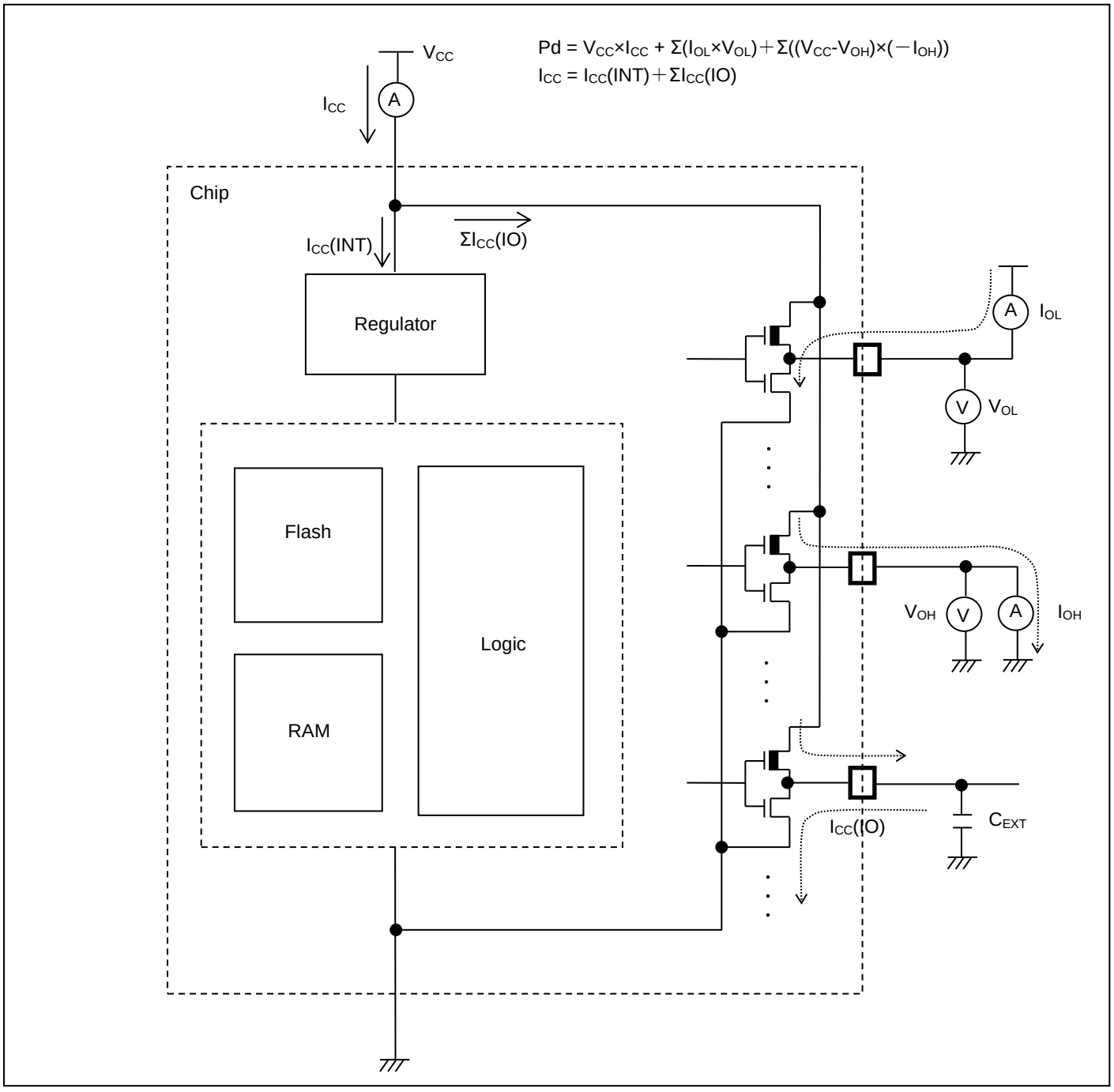
Calculate $I_{CC}$ (Max) as follows when the power dissipation can be evaluated by yourself.

1. Measure current value $I_{CC}$ (Typ) at normal temperature (+25°C).
2. Add maximum leak current value $I_{CC}$ (leak_max) at operating on a value in (1).

$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak_max)$

| Parameter | Symbol | Conditions | Current value |
|---|---|---|---|
| Maximum leak current at operating | $I_{CC}$(leak_max) | Tj = +125°C | 45.5mA |
| | | Tj = +105°C | 26.8mA |
| | | Tj = +85°C | 16.2mA |

**Current explanation diagram**



## 12.3 DC Characteristics

### *12.3.1 Current Rating*

**Table 12-1. Typical and maximum current consumption in Normal operation(PLL), code running from Flash memory (Flash accelerator mode and trace buffer function enabled)**

| Parameter | Symbol | Pin name | Conditions | Frequency*4 | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | | Typ*1 | Max*2 | | |
| Power supply current | $I_{CC}$ | VCC | Normal operation*5,*6 (PLL) | 160MHz | 54 | 103 | mA | *3 When all peripheral clocks are ON |
| | | | | 144MHz | 49 | 98 | | |
| | | | | 120MHz | 41 | 90 | | |
| | | | | 100MHz | 35 | 84 | | |
| | | | | 80MHz | 28 | 77 | | |
| | | | | 60MHz | 22 | 71 | | |
| | | | | 40MHz | 16 | 64 | | |
| | | | | 20MHz | 8.9 | 58 | | |
| | | | | 8MHz | 5.1 | 54 | | |
| | | | | 4MHz | 3.8 | 53 | | |
| | | | | 160MHz | 34 | 83 | mA | *3 When all peripheral clocks are OFF |
| | | | | 144MHz | 31 | 80 | | |
| | | | | 120MHz | 26 | 75 | | |
| | | | | 100MHz | 22 | 71 | | |
| | | | | 80MHz | 18 | 67 | | |
| | | | | 60MHz | 14 | 63 | | |
| | | | | 40MHz | 10 | 59 | | |
| | | | | 20MHz | 6.2 | 55 | | |
| | | | | 8MHz | 3.8 | 53 | | |
| | | | | 4MHz | 3.1 | 52 | | |

**Table 12-2. Typical and maximum current consumption in Normal operation(PLL), code with data accessing running from Flash memory (Flash accelerator mode and trace buffer function disabled)**

| Parameter | Symbol | Pin name | Conditions | Frequency*7 | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | | Typ*1 | Max*2 | | |
| Power supply current | $I_{CC}$ | VCC | Normal operation*8 (PLL) | 160MHz | 74 | 126 | mA | *3 When all peripheral clocks are ON |
| | | | | 144MHz | 68 | 120 | | |
| | | | | 120MHz | 59 | 112 | | |
| | | | | 100MHz | 52 | 104 | | |
| | | | | 80MHz | 44 | 97 | | |
| | | | | 60MHz | 36 | 89 | | |
| | | | | 40MHz | 27 | 79 | | |
| | | | | 20MHz | 17 | 67 | | |
| | | | | 8MHz | 8.3 | 58 | | |
| | | | | 4MHz | 5.4 | 55 | | |
| | | | | 160MHz | 51 | 103 | mA | *3 When all peripheral clocks are OFF |
| | | | | 144MHz | 47 | 100 | | |
| | | | | 120MHz | 42 | 94 | | |
| | | | | 100MHz | 37 | 90 | | |
| | | | | 80MHz | 33 | 85 | | |
| | | | | 60MHz | 28 | 80 | | |
| | | | | 40MHz | 21 | 73 | | |
| | | | | 20MHz | 13 | 64 | | |
| | | | | 8MHz | 6.9 | 56 | | |
| | | | | 4MHz | 4.6 | 54 | | |

*1: $T_A$ = +25°C, $V_{CC}$ = 3.3V

*2: Tj = +125°C, $V_{CC}$ = 5.5V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0 = PCLK1 = PCLK2 = HCLK/2

*5: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

*6: Data access is nothing to MainFlash memory

*7: Frequency is a value of HCLK. PCLK0 = PCLK2 = HCLK/2, PCLK1 = HCLK

*8: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

**Table 12-3. Typical and maximum current consumption in Normal operation(PLL), code with data accessing running from Flash memory (flash 0 wait-cycle mode and read access 0 wait)**

| Parameter | Symbol | Pin name | Conditions | Frequency*4 (MHz) | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | | Typ*1 | Max*2 | | |
| Power supply current | $I_{CC}$ | VCC | Normal operation*5 (PLL) | 72MHz | 46 | 98 | mA | *3 When all peripheral clocks are ON |
| | | | | 60MHz | 40 | 92 | | |
| | | | | 48MHz | 33 | 85 | | |
| | | | | 36MHz | 27 | 78 | | |
| | | | | 24MHz | 19 | 70 | | |
| | | | | 12MHz | 11 | 61 | | |
| | | | | 8MHz | 8.5 | 58 | | |
| | | | | 4MHz | 5.5 | 55 | | |
| | | | | 72MHz | 33 | 85 | mA | *3 When all peripheral clocks are OFF |
| | | | | 60MHz | 29 | 81 | | |
| | | | | 48MHz | 25 | 76 | | |
| | | | | 36MHz | 20 | 71 | | |
| | | | | 24MHz | 15 | 65 | | |
| | | | | 12MHz | 9.2 | 59 | | |
| | | | | 8MHz | 6.9 | 56 | | |
| | | | | 4MHz | 4.6 | 54 | | |

*1: $T_A$ = +25°C, $V_{CC}$ = 3.3V

*2: Tj = +125°C, $V_{CC}$ = 5.5V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0 = PCLK1 = PCLK2 = HCLK

*5: When 0 wait-cycle mode (FRWTR.RWT = 00, FSYNDN.SD = 00)

**Table 12-4. Typical and maximum current consumption in Normal operation(other than PLL), code with data accessing running from Flash memory (flash 0 wait-cycle mode and read access 0 wait**

| Parameter | Symbol | Pin name | Conditions | Frequency*4 | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | | Typ*1 | Max*2 | | |
| Power supply current | $I_{CC}$ | VCC | Normal operation*5 (built-in high-speed CR) | 4MHz | 3.3 | 51 | mA | *3 When all peripheral clocks are ON |
| | | | | | 2.8 | 51 | mA | *3 When all peripheral clocks are OFF |
| | | | Normal operation*5 (sub oscillation) | 32kHz | 0.64 | 48 | mA | *3 When all peripheral clocks are ON |
| | | | | | 0.56 | 48 | mA | *3 When all peripheral clocks are OFF |
| | | | Normal operation*5 (built-in low-speed CR) | 100kHz | 0.64 | 48 | mA | *3 When all peripheral clocks are ON |
| | | | | | 0.58 | 48 | mA | *3 When all peripheral clocks are OFF |

*1: $T_A$ = +25°C, $V_{CC}$ = 3.3V

*2: Tj = +125°C, $V_{CC}$ = 5.5V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0 = PCLK1 = PCLK2 = HCLK/2

*5: When 0 wait-cycle mode (FRWTR.RWT = 00, FSYNDN.SD = 000)

**Table 12-5. Typical and maximum current consumption in Sleep operation(PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2**

| Parameter | Symbol | Pin name | Conditions | Frequency*4 | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | | Typ*1 | Max*2 | | |
| Power supply current | $I_{CCS}$ | VCC | Sleep operation (PLL) | 160MHz | 35 | 84 | mA | *3 When all peripheral clocks are ON |
| | | | | 144MHz | 32 | 81 | | |
| | | | | 120MHz | 27 | 76 | | |
| | | | | 100MHz | 23 | 72 | | |
| | | | | 80MHz | 19 | 68 | | |
| | | | | 60MHz | 15 | 64 | | |
| | | | | 40MHz | 11 | 60 | | |
| | | | | 20MHz | 6.5 | 55 | | |
| | | | | 8MHz | 4.1 | 53 | | |
| | | | | 4MHz | 3.3 | 52 | | |
| | | | | 160MHz | 16 | 65 | mA | *3 When all peripheral clocks are OFF |
| | | | | 144MHz | 14 | 63 | | |
| | | | | 120MHz | 12 | 61 | | |
| | | | | 100MHz | 11 | 60 | | |
| | | | | 80MHz | 9.0 | 58 | | |
| | | | | 60MHz | 7.4 | 56 | | |
| | | | | 40MHz | 5.6 | 54 | | |
| | | | | 20MHz | 3.9 | 53 | | |
| | | | | 8MHz | 2.9 | 52 | | |
| | | | | 4MHz | 2.6 | 51 | | |

**Table 12-6. Typical and maximum current consumption in Sleep operation(PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK**

| Parameter | Symbol | Pin name | Conditions | Frequency*5 | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | | Typ*1 | Max*2 | | |
| Power supply current | $I_{CCS}$ | VCC | Sleep operation (PLL) | 72MHz | 22 | 71 | mA | *3 When all peripheral clocks are ON |
| | | | | 60MHz | 19 | 68 | | |
| | | | | 48MHz | 16 | 64 | | |
| | | | | 36MHz | 12 | 61 | | |
| | | | | 24MHz | 9.0 | 58 | | |
| | | | | 12MHz | 5.8 | 55 | | |
| | | | | 8MHz | 4.6 | 54 | | |
| | | | | 4MHz | 3.6 | 52 | | |
| | | | | 72MHz | 9.5 | 58 | mA | *3 When all peripheral clocks are OFF |
| | | | | 60MHz | 8.3 | 57 | | |
| | | | | 48MHz | 7.1 | 56 | | |
| | | | | 36MHz | 5.8 | 55 | | |
| | | | | 24MHz | 4.6 | 53 | | |
| | | | | 12MHz | 3.5 | 52 | | |
| | | | | 8MHz | 3.0 | 52 | | |
| | | | | 4MHz | 2.7 | 51 | | |

*1: $T_A$ = +25°C, $V_{CC}$ = 3.3V

*2: Tj = +125°C, $V_{CC}$ = 5.5V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0 = PCLK1 = PCLK2 = HCLK/2

*5: Frequency is a value of HCLK. PCLK0 = PCLK1 = PCLK2 = HCLK

**Table 12-7. Typical and maximum current consumption in Sleep operation(other than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2**

| Parameter | Symbol | Pin name | Conditions | Frequency*4 | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | | Typ*1 | Max*2 | | |
| Power supply current | $I_{CCS}$ | VCC | Sleep operation (built-in high-speed CR) | 4MHz | 1.5 | 49 | mA | *3 When all peripheral clocks are ON |
| | | | | | 1.0 | 49 | mA | *3 When all peripheral clocks are OFF |
| | | | Sleep operation (sub oscillation) | 32kHz | 0.59 | 48 | mA | *3 When all peripheral clocks are ON |
| | | | | | 0.51 | 48 | mA | *3 When all peripheral clocks are OFF |
| | | | Sleep operation (built-in low-speed CR) | 100kHz | 0.61 | 48 | mA | *3 When all peripheral clocks are ON |
| | | | | | 0.53 | 48 | mA | *3 When all peripheral clocks are OFF |

*1: $T_A$ = +25°C, $V_{CC}$ = 3.3V

*2: Tj = +125°C, $V_{CC}$ = 5.5V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0 = PCLK1 = PCLK2 = HCLK/2

**Table 12-8. Typical and maximum current consumption in STOP mode, TIMER mode and RTC mode**

| Parameter | Symbol | Pin name | Conditions | Frequency | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | | Typ*1 | Max*2 | | |
| Power supply current | $I_{CCH}$ | VCC | STOP mode | - | 0.33 | 1.8 | mA | *3, *4 $T_A$ = +25°C |
| | | | | | - | 15 | mA | *3, *4 $T_A$ = +85°C |
| | | | | | - | 22 | mA | *3, *4 $T_A$ = +105°C |
| | $I_{CCT}$ | | TIMER mode (built-in high-speed CR) | 4MHz | 0.70 | 2.2 | mA | *3, *4 $T_A$ = +25°C |
| | | | | | - | 16 | mA | *3, *4 $T_A$ = +85°C |
| | | | | | - | 22 | mA | *3, *4 $T_A$ = +105°C |
| | | | TIMER mode (sub oscillation) | 32kHz | 0.33 | 1.8 | mA | *3, *4 $T_A$ = +25°C |
| | | | | | - | 15 | mA | *3, *4 $T_A$ = +85°C |
| | | | | | - | 22 | mA | *3, *4 $T_A$ = +105°C |
| | | | TIMER mode (built-in low-speed CR) | 100kHz | 0.34 | 1.8 | mA | *3, *4 $T_A$ = +25°C |
| | | | | | - | 15 | mA | *3, *4 $T_A$ = +85°C |
| | | | | | - | 22 | mA | *3, *4 $T_A$ = +105°C |
| | $I_{CCR}$ | | RTC mode (sub oscillation) | 32kHz | 0.33 | 1.8 | mA | *3, *4 $T_A$ = +25°C |
| | | | | | - | 15 | mA | *3, *4 $T_A$ = +85°C |
| | | | | | - | 22 | mA | *3, *4 $T_A$ = +105°C |

*1: $V_{CC}$ = 3.3V

*2: $V_{CC}$ = 5.5V

*3: When all ports are fixed.

*4: When LVD is OFF

**Table 12-9. Typical and maximum current consumption in Deep Standby STOP mode, Deep Standby RTC mode and VBAT**

| Parameter | Symbol | Pin name | Conditions | Frequency | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | | Typ*1 | Max*2 | | |
| Power supply current | $I_{CCHD}$ | VCC | Deep standby STOP mode (When RAM is OFF) | - | 29 | 140 | µA | *3, *4 $T_A$ = +25°C |
| | | | | | - | 644 | µA | *3, *4 $T_A$ = +85°C |
| | | | | | - | 1011 | µA | *3, *4 $T_A$ = +105°C |
| | | | Deep standby STOP mode (When RAM is ON) | | 48 | 273 | µA | *3, *4 $T_A$ = +25°C |
| | | | | | - | 2676 | µA | *3, *4 $T_A$ = +85°C |
| | | | | | - | 4162 | µA | *3, *4 $T_A$ = +105°C |
| | $I_{CCRD}$ | | Deep standby RTC mode (When RAM is OFF) | 32kHz | 29 | 140 | µA | *3, *4 $T_A$ = +25°C |
| | | | | | - | 644 | µA | *3, *4 $T_A$ = +85°C |
| | | | | | - | 1011 | µA | *3, *4 $T_A$ = +105°C |
| | | | Deep standby RTC mode (When RAM is ON) | | 48 | 273 | µA | *3, *4 $T_A$ = +25°C |
| | | | | | - | 2676 | µA | *3, *4 $T_A$ = +85°C |
| | | | | | - | 4162 | µA | *3, *4 $T_A$ = +105°C |
| | $I_{CCVBAT}$ | VBAT | RTC stop*6 | - | 0.015 | 0.29 | µA | *3, *4, *5 $T_A$ = +25°C |
| | | | | | - | 5.77 | µA | *3, *4, *5 $T_A$ = +85°C |
| | | | | | - | 10.6 | µA | *3, *4, *5 $T_A$ = +105°C |
| | | | RTC operation*6 | | 1.53 | 22.6 | µA | *3, *4 $T_A$ = +25°C |
| | | | | | - | 35.2 | µA | *3, *4 $T_A$ = +85°C |
| | | | | | - | 41.8 | µA | *3, *4 $T_A$ = +105°C |

*1: $V_{CC}$ = 3.3V

*2: $V_{CC}$ = 5.5V

*3: When all ports are fixed.

*4: When LVD is OFF

*5: When sub oscillation is OFF

*6: In the case of setting RTC after VCC power on

**Table 12-10. Typical and maximum current consumption in Low-voltage detection circuit, Main flash memory write/erase**

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Low-voltage detection circuit (LVD) power supply current | $I_{CCLVD}$ | VCC | At operation | - | 4 | 7 | µA | For occurrence of interrupt |
| Main flash memory write/erase current | $I_{CCFLASH}$ | | At Write/Erase | - | 13.4 | 15.9 | mA | |
| Work flash memory write/erase current | $I_{CCWFLASH}$ | | At Write/Erase | - | 11.5 | 13.6 | mA | |

## Peripheral current dissipation

| Clock system | Peripheral | Unit | Frequency (MHz) | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | 40 | 80 | 160 | | |
| HCLK | GPIO | All ports | 0.22 | 0.43 | 0.85 | mA | |
| | DMAC | - | 0.74 | 1.48 | 2.88 | | |
| | DSTC | - | 0.32 | 0.61 | 1.17 | | |
| | External bus I/F | - | 0.14 | 0.27 | 0.55 | | |
| | SD card I/F | - | 0.93 | 1.81 | 3.63 | | |
| PCLK1 | Base timer | 4ch. | 0.16 | 0.34 | 0.66 | mA | |
| | Multi-functional timer/PPG | 1unit/4ch. | 0.55 | 1.09 | 2.17 | | |
| | Quadrature position/Revolution counter | 1unit | 0.04 | 0.09 | 0.17 | | |
| | A/DC | 1unit | 0.20 | 0.39 | 0.78 | | |
| PCLK2 | Muli-function serial | 1ch. | 0.31 | 0.62 | - | mA | |

### 12.3.2 Pin Characteristics

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage (hysteresis input) | $V_{IHS}$ | CMOS hysteresis input pin, MD0, MD1 | - | $V_{CC}$×0.8 | - | $V_{CC}$ + 0.3 | V | |
| | | 5V tolerant input pin | - | $V_{CC}$×0.8 | - | $V_{SS}$ + 5.5 | V | |
| | | Input pin doubled as $I^2C$ Fm+ | - | $V_{CC}$×0.7 | - | $V_{SS}$ + 5.5 | V | |
| "L" level input voltage (hysteresis input) | $V_{ILS}$ | CMOS hysteresis input pin, MD0, MD1 | - | $V_{SS}$ - 0.3 | - | $V_{CC}$×0.2 | V | |
| | | 5V tolerant input pin | - | $V_{SS}$ - 0.3 | - | $V_{CC}$×0.2 | V | |
| | | Input pin doubled as $I^2C$ Fm+ | - | $V_{SS}$ | - | $V_{CC}$×0.3 | V | |
| "H" level output voltage | $V_{OH}$ | 4mA type | $V_{CC}$ ≥ 4.5 V, $I_{OH}$ = - 4mA | $V_{CC}$ - 0.5 | - | $V_{CC}$ | V | |
| | | | $V_{CC}$ < 4.5 V, $I_{OH}$ = - 2mA | | | | | |
| | | 8mA type | $V_{CC}$ ≥ 4.5 V, $I_{OH}$ = - 8mA | $V_{CC}$ - 0.5 | - | $V_{CC}$ | V | |
| | | | $V_{CC}$ < 4.5 V, $I_{OH}$ = - 4mA | | | | | |
| | | 12mA type | $V_{CC}$ ≥ 4.5 V, $I_{OH}$ = - 12mA | $V_{CC}$ - 0.5 | - | $V_{CC}$ | V | |
| | | | $V_{CC}$ < 4.5 V, $I_{OH}$ = - 8mA | | | | | |
| | | The pin doubled as $I^2C$ Fm+ | $V_{CC}$ ≥ 4.5 V, $I_{OH}$ = - 4mA | $V_{CC}$ - 0.5 | - | $V_{CC}$ | V | At GPIO |
| | | | $V_{CC}$ < 4.5 V, $I_{OH}$ = - 3mA | | | | | |

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "L" level output voltage | $V_{OL}$ | 4mA type | $V_{CC} \geq 4.5$ V, $I_{OL}$ = 4mA | $V_{SS}$ | - | 0.4 | V | |
| | | | $V_{CC} < 4.5$ V, $I_{OL}$ = 2mA | | | | | |
| | | 8mA type | $V_{CC} \geq 4.5$ V, $I_{OH}$ = 8mA | $V_{SS}$ | - | 0.4 | V | |
| | | | $V_{CC} < 4.5$ V, $I_{OH}$ = 4mA | | | | | |
| | | 12mA type | $V_{CC} \geq 4.5$ V, $I_{OL}$ = 12mA | $V_{SS}$ | - | 0.4 | V | |
| | | | $V_{CC} < 4.5$ V, $I_{OL}$ = 8mA | | | | | |
| | | The pin doubled as $I^2C$ Fm+ | $V_{CC} \geq 4.5$ V, $I_{OH}$ = 4mA | $V_{SS}$ | - | 0.4 | V | At GPIO |
| | | | $V_{CC} < 4.5$ V, $I_{OH}$ = 3mA | | | | | |
| | | | $V_{CC} \leq 5.5$ V, $I_{OH}$ = 20mA | | | | | At $I^2C$ Fm+ |
| Input leak current | $I_{IL}$ | - | - | - 5 | - | + 5 | µA | |
| Pull-up resistor value | $R_{PU}$ | Pull-up pin | $V_{CC} \geq 4.5$ V | 25 | 50 | 100 | kΩ | |
| | | | $V_{CC} < 4.5$ V | 30 | 80 | 200 | | |
| Input capacitance | $C_{IN}$ | Other than VCC, VBAT, VSS, AVCC, AVSS, AVRH | - | - | 5 | 15 | pF | |

## 12.4 AC Characteristics

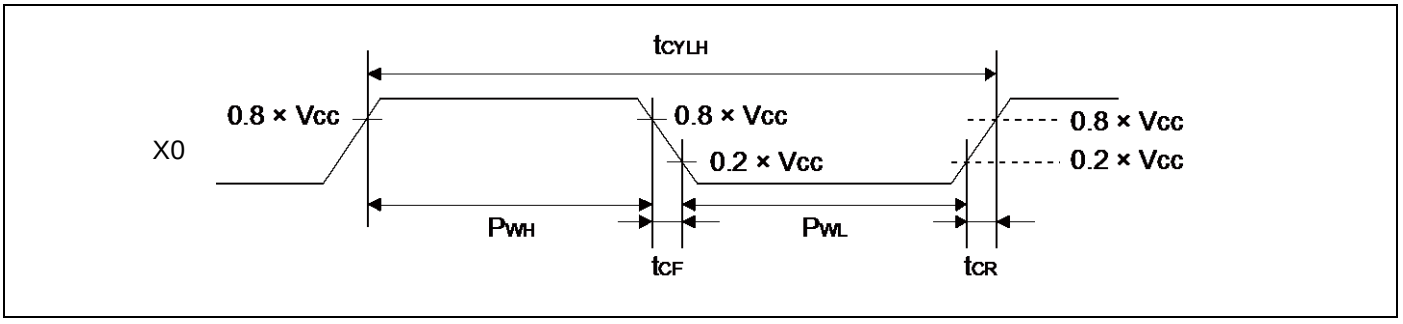
### *12.4.1 Main Clock Input Characteristics*

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input frequency | $F_{CH}$ | X0, X1 | $V_{CC} \geq 4.5V$ | 4 | 48 | MHz | When crystal oscillator is connected |
| | | | $V_{CC} < 4.5V$ | 4 | 20 | | |
| | | | $V_{CC} \geq 4.5V$ | 4 | 48 | MHz | When using external clock |
| | | | $V_{CC} < 4.5V$ | 4 | 20 | | |
| Input clock cycle | $t_{CYLH}$ | | $V_{CC} \geq 4.5V$ | 20.83 | 250 | ns | When using external clock |
| | | | $V_{CC} < 4.5V$ | 50 | 250 | | |
| Input clock pulse width | - | | PWH/tCYLH, PWL/tCYLH | 45 | 55 | % | When using external clock |
| Input clock rising time and falling time | $t_{CF}$, $t_{CR}$ | | - | - | 5 | ns | When using external clock |
| Internal operating clock*1 frequency | $F_{CC}$ | - | - | - | 160 | MHz | Base clock (HCLK/FCLK) |
| | $F_{CP0}$ | - | - | - | 80 | MHz | APB0 bus clock*2 |
| | $F_{CP1}$ | - | - | - | 160 | MHz | APB1 bus clock*2 |
| | $F_{CP2}$ | - | - | - | 80 | MHz | APB2 bus clock*2 |
| Internal operating clock*1 cycle time | $t_{CYCC}$ | - | - | 6.25 | - | ns | Base clock (HCLK/FCLK) |
| | $t_{CYCP0}$ | - | - | 12.5 | - | ns | APB0 bus clock*2 |
| | $t_{CYCP1}$ | - | - | 6.25 | - | ns | APB1 bus clock*2 |
| | $t_{CYCP2}$ | - | - | 12.5 | - | ns | APB2 bus clock*2 |

*1: For more information about each internal operating clock, see “Chapter: Clock” in “FM4 Family Peripheral Manual”.

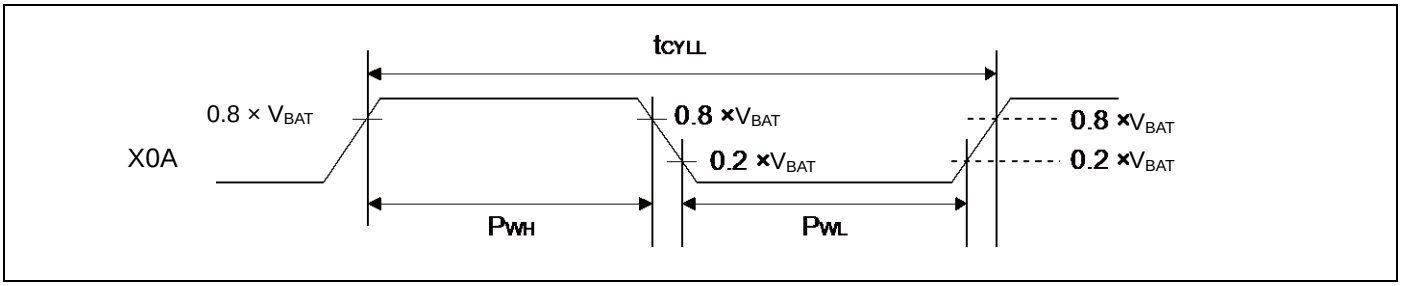
*2: For about each APB bus which each peripheral is connected to, see “Block Diagram” in this datasheet.



### 12.4.2 Sub Clock Input Characteristics

($V_{BAT}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input frequency | 1/ $t_{CYLL}$ | X0A, X1A | - | - | 32.768 | - | kHz | When crystal oscillator is connected |
| | | | - | 32 | - | 100 | kHz | When using external clock |
| Input clock cycle | $t_{CYLL}$ | | - | 10 | - | 31.25 | µs | When using external clock |
| Input clock pulse width | - | | $P_{WH}/t_{CYLL}$, $P_{WL}/t_{CYLL}$ | 45 | - | 55 | % | When using external clock |




### 12.4.3 Built-in CR Oscillation Characteristics

#### Built-in High-speed CR

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $F_{CRH}$ | Tj = -20°C to + 105°C | 3.92 | 4 | 4.08 | MHz | When trimming*1 |
| | | Tj = - 40°C to + 125°C | 3.88 | 4 | 4.12 | | |
| Clock frequency | $F_{CRH}$ | Tj = - 40°C to + 125°C | 3 | 4 | 5 | | When not trimming |
| Frequency stabilization time | $t_{CRWT}$ | - | - | - | 30 | µs | *2 |

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency/temperature trimming.

*2: This is the time to stabilize the frequency of high-speed CR clock after setting trimming value. This period is able to use high-speed CR clock as source clock.

#### Built-in Low-speed CR

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $F_{CRL}$ | - | 50 | 100 | 150 | kHz | |

### 12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input clock of PLL)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| PLL oscillation stabilization wait time*1 (LOCK UP time) | $t_{LOCK}$ | 200 | - | - | µs | |
| PLL input clock frequency | $F_{PLLI}$ | 4 | - | 16 | MHz | |
| PLL multiplication rate | - | 13 | - | 80 | multiplier | |
| PLL macro oscillation clock frequency | $F_{PLLO}$ | 200 | - | 320 | MHz | |
| Main PLL clock frequency*2 | $F_{CLKPLL}$ | - | - | 160 | MHz | |

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see “Chapter: Clock” in “FM4 Family Peripheral Manual”.

### 12.4.5 Operating Conditions of Main PLL (In the case of using built-in high-speed CR clock for input clock of main PLL)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| PLL oscillation stabilization wait time*1 (LOCK UP time) | $t_{LOCK}$ | 200 | - | - | µs | |
| PLL input clock frequency | $F_{PLLI}$ | 3.8 | 4 | 4.2 | MHz | |
| PLL multiplication rate | - | 50 | - | 75 | multiplier | |
| PLL macro oscillation clock frequency | $F_{PLLO}$ | 190 | - | 320 | MHz | |
| Main PLL clock frequency*2 | $F_{CLKPLL}$ | - | - | 160 | MHz | |

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see “Chapter: Clock” in “FM4 Family Peripheral Manual”.

***Note:***

- *Make sure to input to the main PLL source clock, the high-speed CR clock (CLKHC) that the frequency and temperature has been trimmed.*

### 12.4.6 Reset Input Characteristics

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Reset input time | $t_{INITX}$ | INITX | - | 500 | - | ns | |

### 12.4.7 Power-on Reset Timing

($V_{SS}$ = 0V, $T_A$ = -40°C to +85°C)

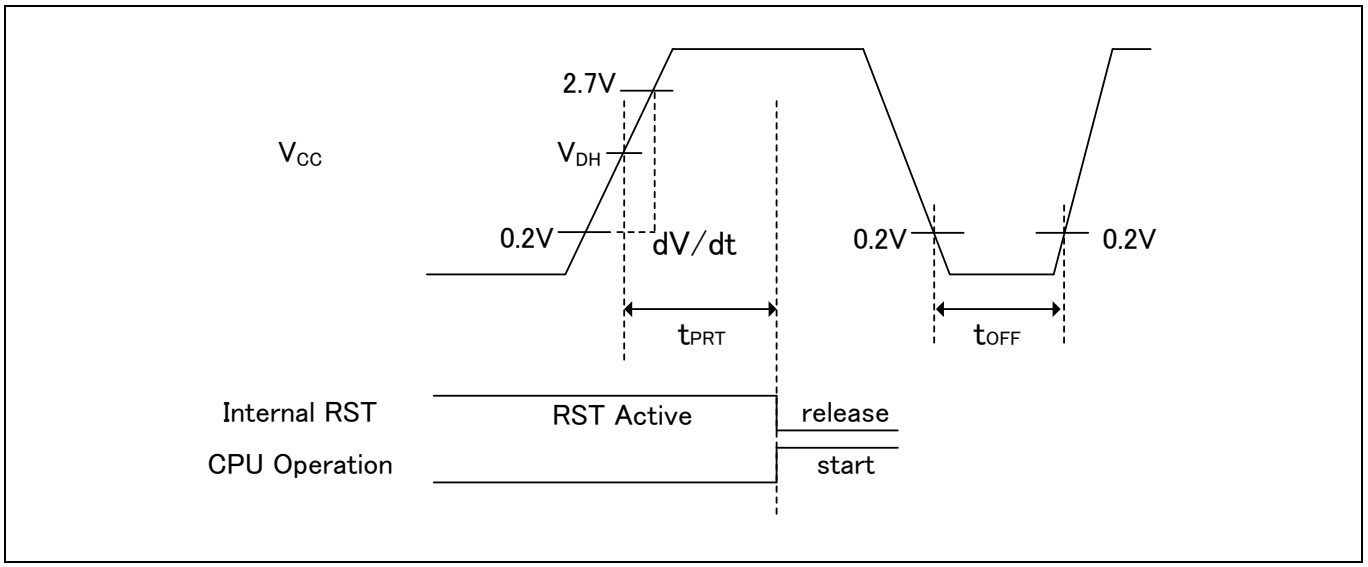
| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply shut down time | $t_{OFF}$ | VCC | - | 50 | - | - | ms | *1 |
| Power ramp rate | dV/dt | | $V_{CC}$: 0.2V to 2.70V | 1.3 | - | 1000 | mV/µs | *2 |
| Time until releasing Power-on reset | $t_{PRT}$ | | - | 0.33 | - | 0.60 | ms | |

*1: $V_{CC}$ must be held below 0.2V for a minimum period of $t_{OFF}$. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start ($t_{OFF}$>50ms).

***Note:***

- *If $t_{OFF}$ cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per 12. 4. 6.*




***Glossary:***

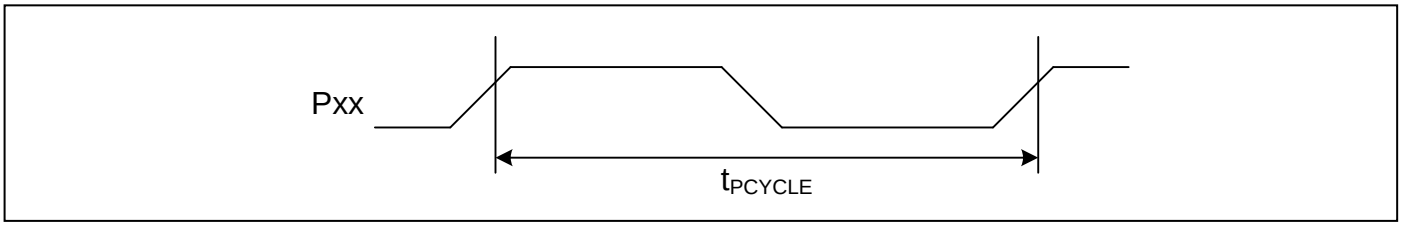
- $V_{DH}$: detection voltage of Low Voltage detection reset. See “12.7. Low-Voltage Detection Characteristics”.

### 12.4.8 GPIO Output Characteristics

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Output frequency | $t_{PCYCLE}$ | Pxx* | $V_{CC}$ ≥ 4.5 V | - | 50 | MHz |
| | | | $V_{CC}$ < 4.5 V | - | 32 | MHz |

*: GPIO is a target.



### 12.4.9 External Bus Timing

#### External bus clock output characteristics

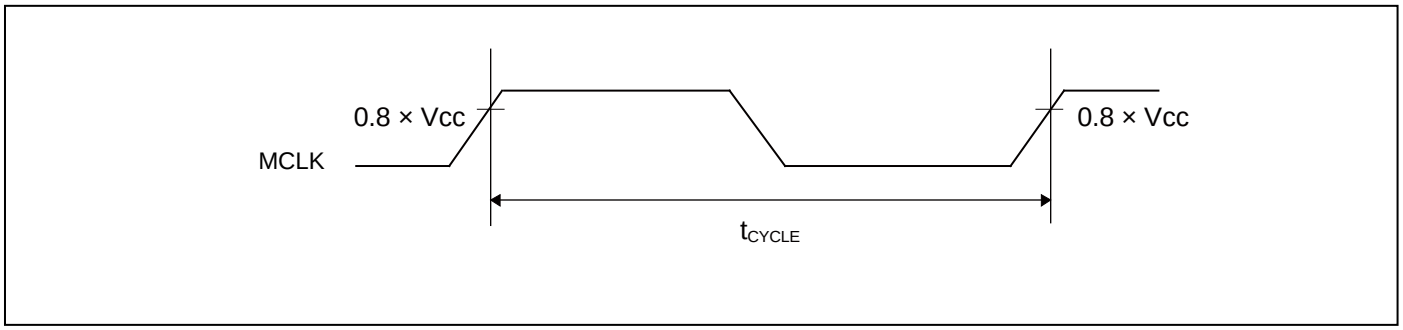
($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Output frequency | $t_{CYCLE}$ | MCLKOUT*1 | $V_{CC} \geq 4.5$ V | - | 50*2 | MHz |
| | | | $V_{CC} < 4.5$ V | - | 32*3 | MHz |

*1: The external bus clock (MCLKOUT) is a divided clock of HCLK.
For more information about setting of clock divider, see “Chapter: External Bus Interface” in “FM4 Family Peripheral Manual”.

*2: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 100MHz.

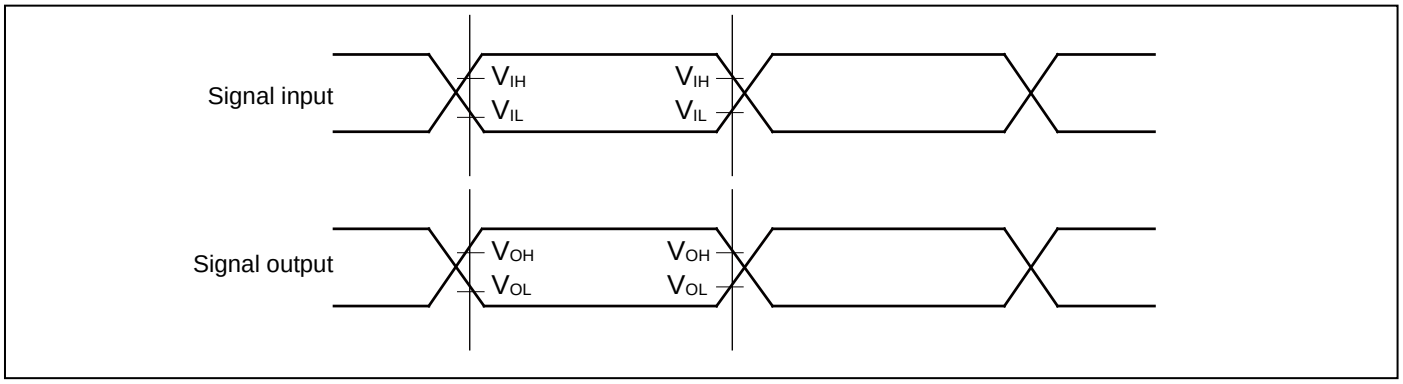
*3: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 64MHz.




#### External bus signal input/output characteristics

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Conditions | Value | Unit | Remarks |
|---|---|---|---|---|---|
| Signal input characteristics | $V_{IH}$ | - | 0.8 × $V_{CC}$ | V | |
| | $V_{IL}$ | | 0.2 × $V_{CC}$ | V | |
| Signal output characteristics | $V_{OH}$ | | 0.8 × $V_{CC}$ | V | |
| | $V_{OL}$ | | 0.2 × $V_{CC}$ | V | |



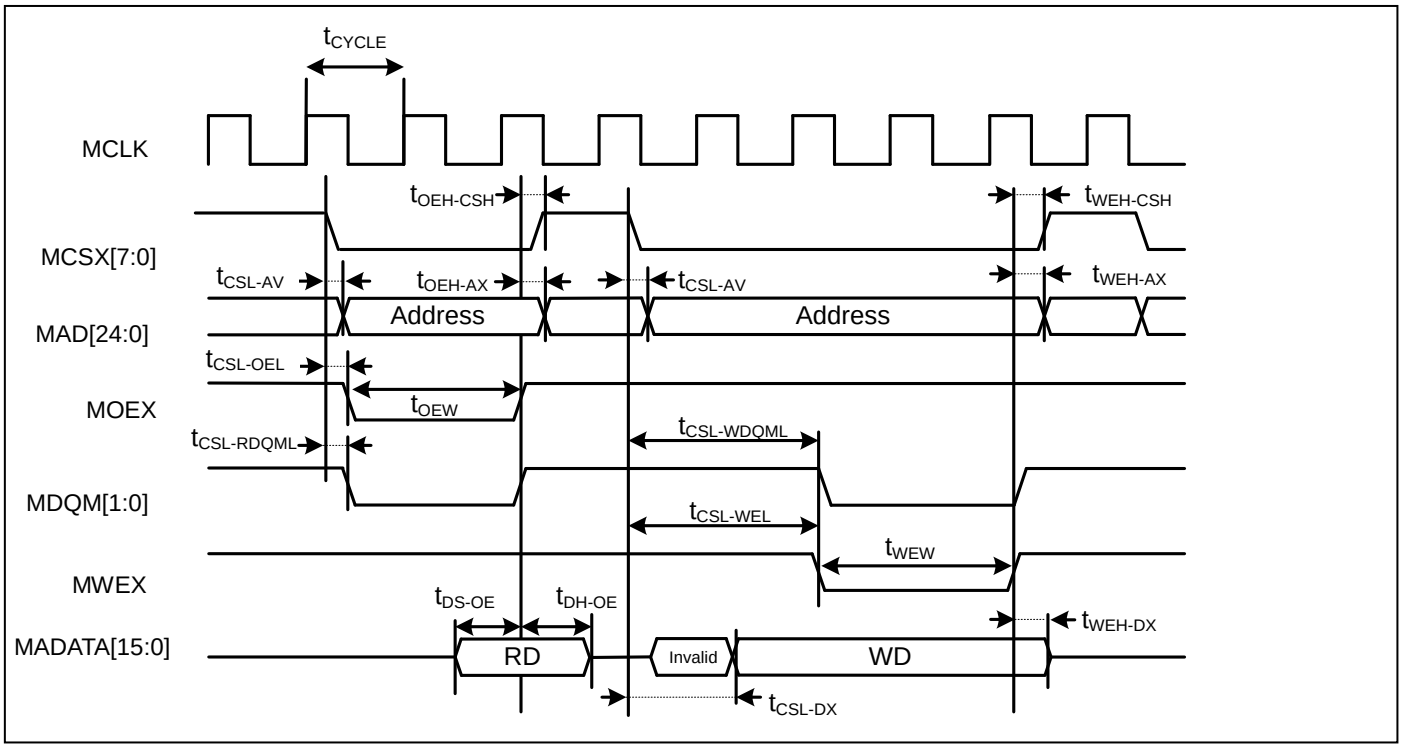
### Separate Bus Access Asynchronous SRAM Mode

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| MOEX Mininum pulse width | $t_{OEW}$ | MOEX | $V_{CC} \geq 4.5V$ | MCLK×n-3 | - | ns |
| | | | $V_{CC} < 4.5V$ | | | |
| MCSX↓→Address output delay time | $t_{CSL-AV}$ | MCSX[7:0], MAD[24:0] | $V_{CC} \geq 4.5V$ | -9 | +9 | ns |
| | | | $V_{CC} < 4.5V$ | -12 | +12 | |
| MOEX↑→Address hold time | $t_{OEH-AX}$ | MOEX, MAD[24:0] | $V_{CC} \geq 4.5V$ | 0 | MCLK×m+9 | ns |
| | | | $V_{CC} < 4.5V$ | | MCLK×m+12 | |
| MCSX↓→ MOEX↓ delay time | $t_{CSL-OEL}$ | MOEX, MCSX[7:0] | $V_{CC} \geq 4.5V$ | MCLK×m-9 | MCLK×m+9 | ns |
| | | | $V_{CC} < 4.5V$ | MCLK×m-12 | MCLK×m+12 | |
| MOEX↑→ MCSX↑ time | $t_{OEH-CSH}$ | | $V_{CC} \geq 4.5V$ | 0 | MCLK×m+9 | ns |
| | | | $V_{CC} < 4.5V$ | | MCLK×m+12 | |
| MCSX↓→MDQM↓ delay time | $t_{CSL-RDQML}$ | MCSX, MDQM[1:0] | $V_{CC} \geq 4.5V$ | MCLK×m-9 | MCLK×m+9 | ns |
| | | | $V_{CC} < 4.5V$ | MCLK×m-12 | MCLK×m+12 | |
| Data set up→MOEX↑ time | $t_{DS-OE}$ | MOEX, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 20 | - | ns |
| | | | $V_{CC} < 4.5V$ | 38 | - | |
| MOEX↑→ Data hold time | $t_{DH-OE}$ | MOEX, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 0 | - | ns |
| | | | $V_{CC} < 4.5V$ | | | |
| MWEX Mininum pulse width | $t_{WEW}$ | MWEX | $V_{CC} \geq 4.5V$ | MCLK×n-3 | - | ns |
| | | | $V_{CC} < 4.5V$ | | | |
| MWEX↑→Address output delay time | $t_{WEH-AX}$ | MWEX, MAD[24:0] | $V_{CC} \geq 4.5V$ | 0 | MCLK×m+9 | ns |
| | | | $V_{CC} < 4.5V$ | | MCLK×m+12 | |
| MCSX↓→MWEX↓ delay time | $t_{CSL-WEL}$ | MWEX, MCSX[7:0] | $V_{CC} \geq 4.5V$ | MCLK×n-9 | MCLK×n+9 | ns |
| | | | $V_{CC} < 4.5V$ | MCLK×n-12 | MCLK×n+12 | |
| MWEX↑→MCSX↑ delay time | $t_{WEH-CSH}$ | | $V_{CC} \geq 4.5V$ | 0 | MCLK×m+9 | ns |
| | | | $V_{CC} < 4.5V$ | | MCLK×m+12 | |
| MCSX↓→MDQM↓ delay time | $t_{CSL-WDQML}$ | MCSX, MDQM[1:0] | $V_{CC} \geq 4.5V$ | MCLK×n-9 | MCLK×n+9 | ns |
| | | | $V_{CC} < 4.5V$ | MCLK×n-12 | MCLK×n+12 | |
| MCSX↓→ Data output time | $t_{CSL-DX}$ | MCSX, MADATA[15:0] | $V_{CC} \geq 4.5V$ | MCLK-9 | MCLK+9 | ns |
| | | | $V_{CC} < 4.5V$ | MCLK-12 | MCLK+12 | |
| MWEX↑→ Data hold time | $t_{WEH-DX}$ | MWEX, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 0 | MCLK×m+9 | ns |
| | | | $V_{CC} < 4.5V$ | | MCLK×m+12 | |

***Note:***

- *When the external load capacitance $C_L$ = 30pF (m = 0 to 15, n = 1 to 16)*


tCYCLE
MCLK
tOEH-CSH
tWEH-CSH
MCSX[7:0]
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
Address
Address
MAD[24:0]
tCSL-OEL
tOEW
MOEX
tCSL-RDQML
tCSL-WDQML
MDQM[1:0]
tCSL-WEL
tWEW
MWEX
tDS-OE
tDH-OE
tWEH-DX
MADATA[15:0]
RD
Invalid
WD
tCSL-DX

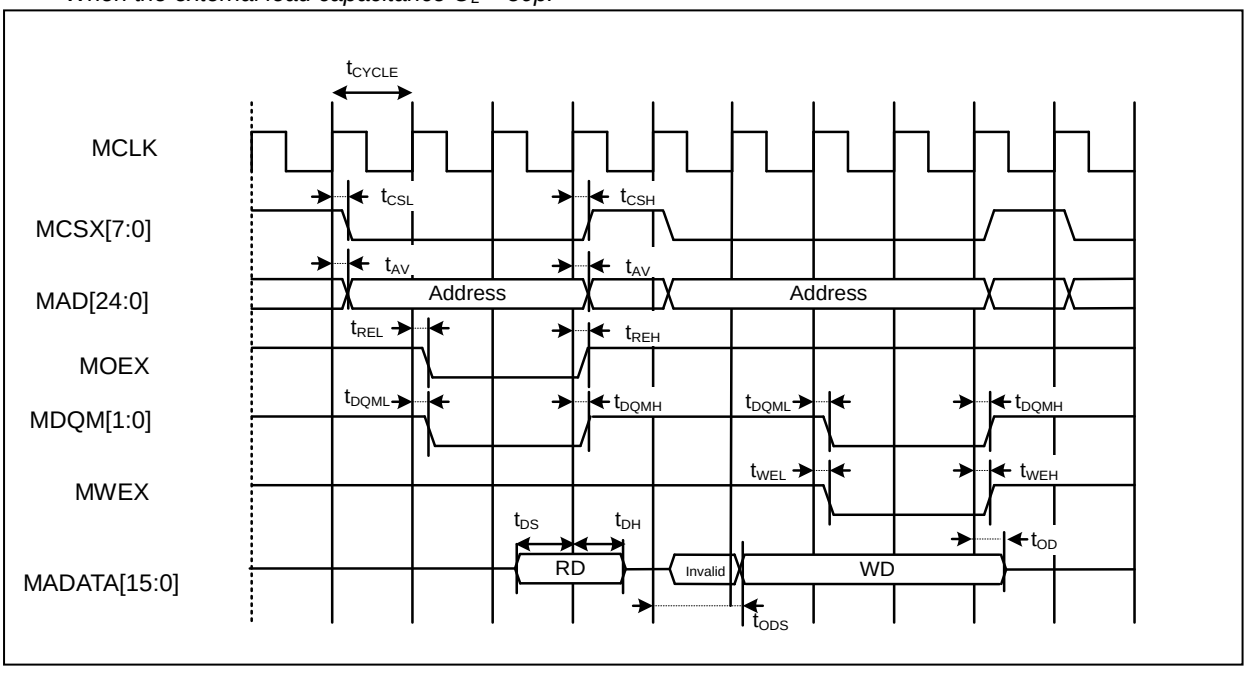
## Separate Bus Access Synchronous SRAM Mode

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Address delay time | $t_{AV}$ | MCLK, MAD[24:0] | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| MCSX delay time | $t_{CSL}$ | MCLK, MCSX[7:0] | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| | $t_{CSH}$ | | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| MOEX delay time | $t_{REL}$ | MCLK, MOEX | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| | $t_{REH}$ | | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| Data set up →MCLK↑ time | $t_{DS}$ | MCLK, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 19 | - | ns |
| | | | $V_{CC} < 4.5V$ | 37 | | |
| MCLK↑→ Data hold time | $t_{DH}$ | MCLK, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 0 | - | ns |
| | | | $V_{CC} < 4.5V$ | | | |
| MWEX delay time | $t_{WEL}$ | MCLK, MWEX | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| | $t_{WEH}$ | | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| MDQM[1:0] delay time | $t_{DQML}$ | MCLK, MDQM[1:0] | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| | $t_{DQMH}$ | | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| MCLK↑→ Data output time | $t_{ODS}$ | MCLK, MADATA[15:0] | $V_{CC} \geq 4.5V$ | MCLK+1 | MCLK+18 | ns |
| | | | $V_{CC} < 4.5V$ | | MCLK+24 | |
| MCLK↑→ Data hold time | $t_{OD}$ | MCLK, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 1 | 18 | ns |
| | | | $V_{CC} < 4.5V$ | | 24 | |

***Note:***

- *When the external load capacitance $C_L$ = 30pF*



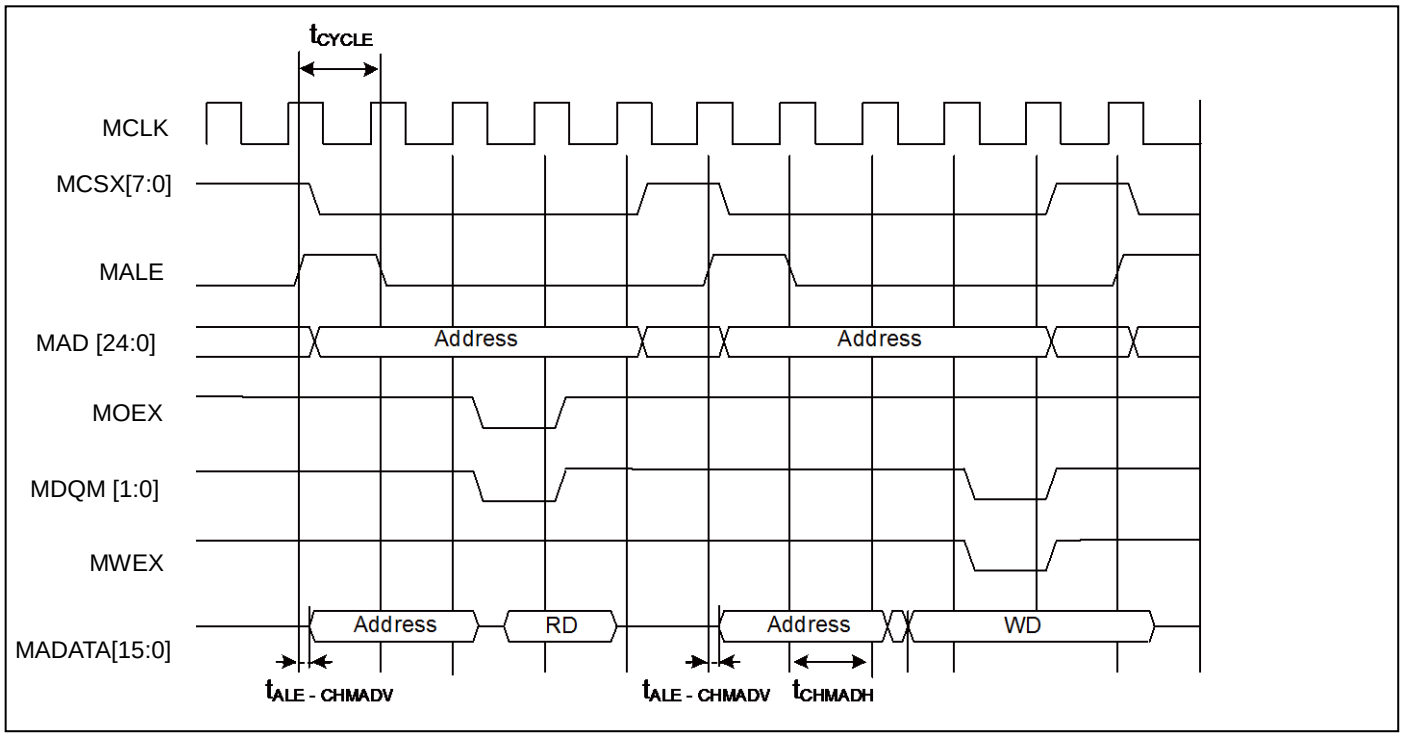
### Multiplexed Bus Access Asynchronous SRAM Mode

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Multiplexed address delay time | $t_{ALE-CHMADV}$ | MALE, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 0 | 10 | ns |
| | | | $V_{CC} < 4.5V$ | | 20 | |
| Multiplexed address hold time | $t_{CHMADH}$ | | $V_{CC} \geq 4.5V$ | MCLK×n+0 | MCLK×n+10 | ns |
| | | | $V_{CC} < 4.5V$ | MCLK×n+0 | MCLK×n+20 | |

***Note:***

- *When the external load capacitance $C_L$ = 30pF (m = 0 to 15, n = 1 to 16)*



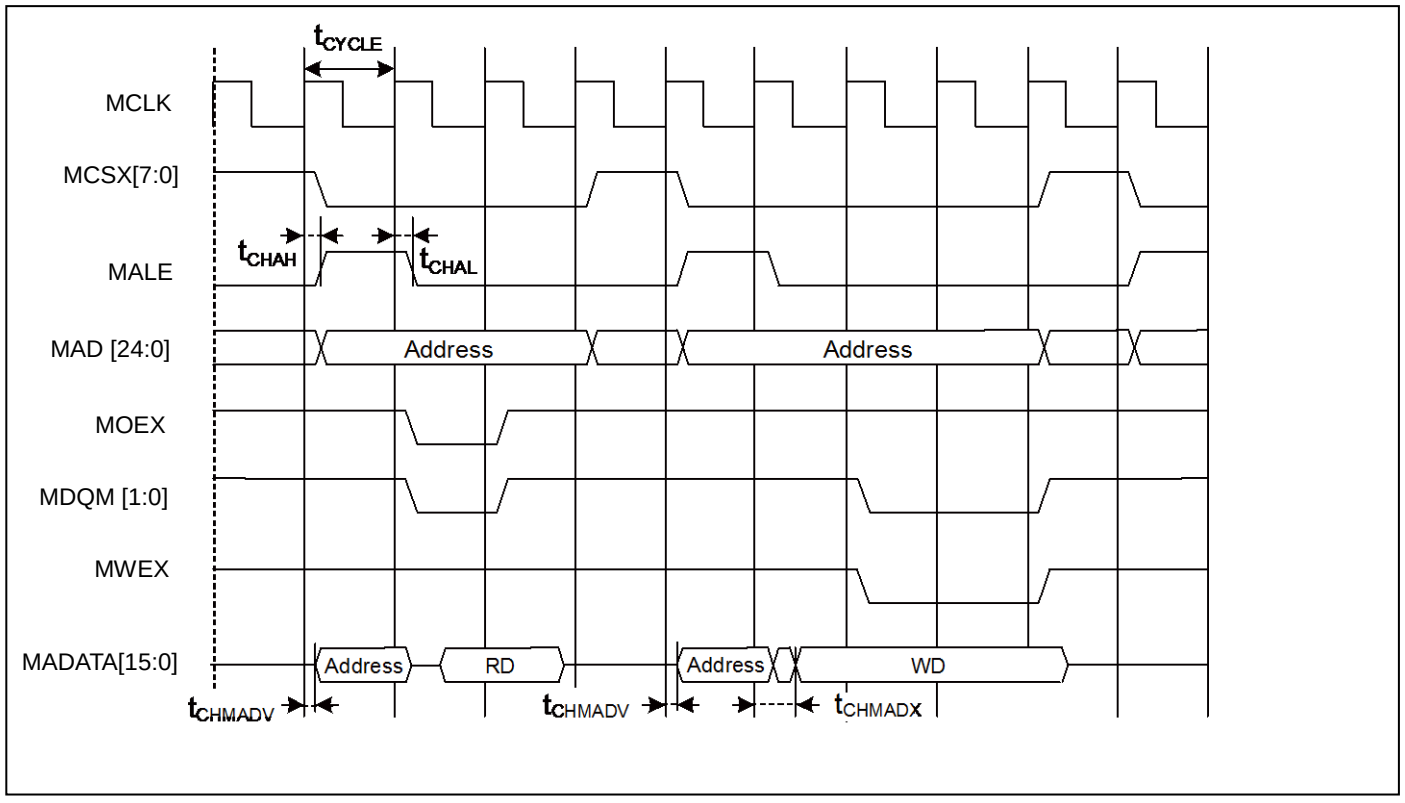
### Multiplexed Bus Access Synchronous SRAM Mode

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| MALE delay time | $t_{CHAL}$ | MCLK, ALE | $V_{CC} \geq 4.5V$ | 1 | 9 | ns | |
| | | | $V_{CC} < 4.5V$ | | 12 | ns | |
| | $t_{CHAH}$ | | $V_{CC} \geq 4.5V$ | 1 | 9 | ns | |
| | | | $V_{CC} < 4.5V$ | | 12 | ns | |
| MCLK↑→ Multiplexed address delay time | $t_{CHMADV}$ | MCLK, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 1 | $t_{OD}$ | ns | |
| | | | $V_{CC} < 4.5V$ | | | | |
| MCLK↑→ Multiplexed data output time | $t_{CHMADX}$ | | $V_{CC} \geq 4.5V$ | 1 | $t_{OD}$ | ns | |
| | | | $V_{CC} < 4.5V$ | | | | |

***Note:***

- *When the external load capacitance $C_L$ = 30pF*



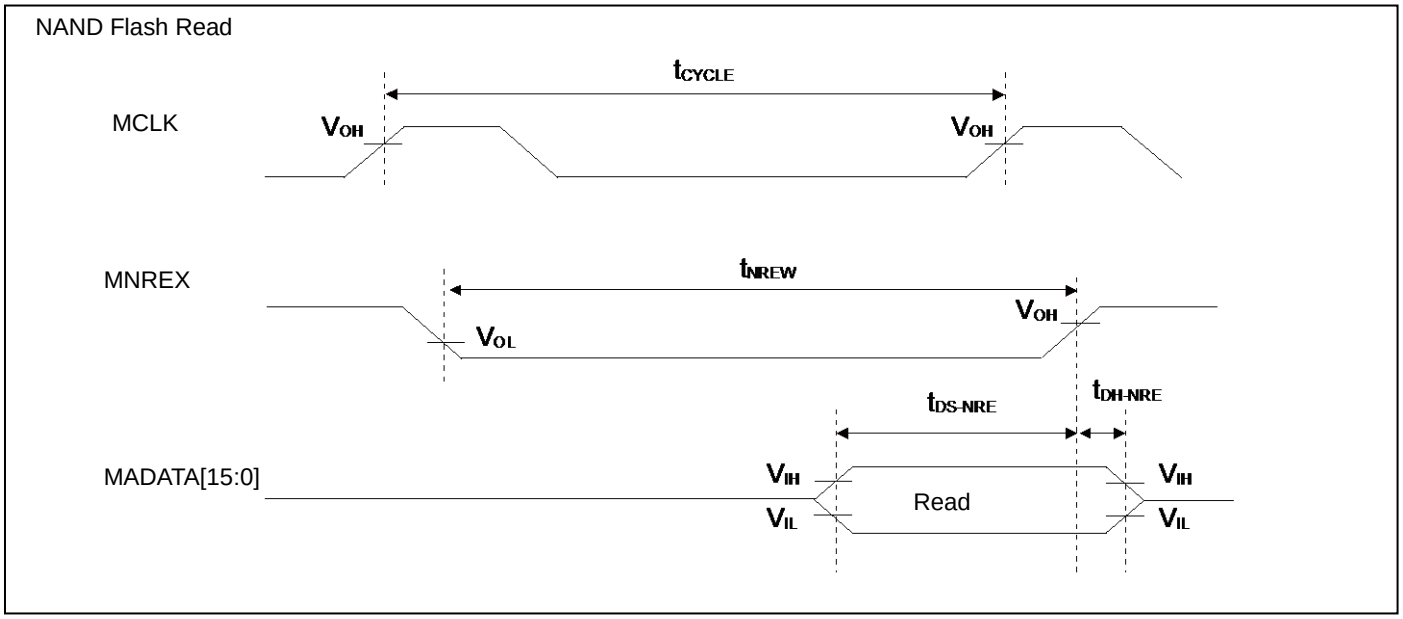
### NAND Flash Mode

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

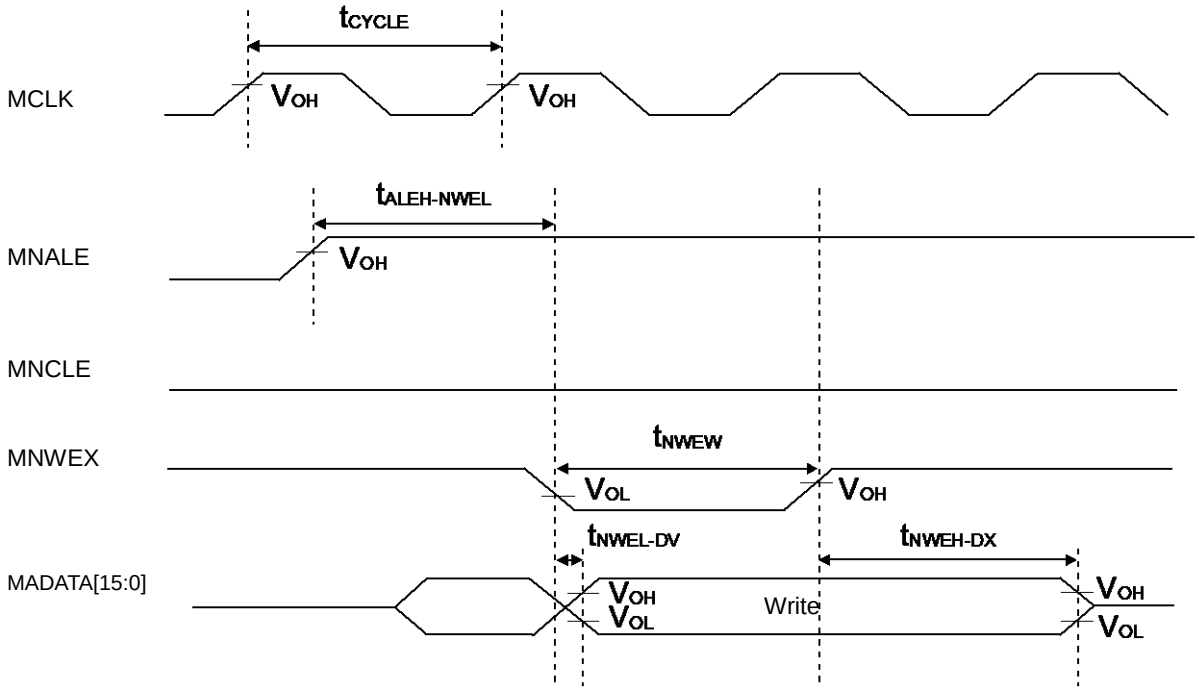
| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| MNREX Min pulse width | $t_{NREW}$ | MNREX | $V_{CC} \geq 4.5V$ | MCLK×n-3 | - | ns |
| | | | $V_{CC} < 4.5V$ | | | |
| Data set up →MNREX↑ time | $t_{DS-NRE}$ | MNREX, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 20 | - | ns |
| | | | $V_{CC} < 4.5V$ | 38 | - | |
| MNREX↑→ Data hold time | $t_{DH-NRE}$ | MNREX, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 0 | - | ns |
| | | | $V_{CC} < 4.5V$ | | | |
| MNALE↑→ MNWEX delay time | $t_{ALEH-NWEL}$ | MNALE, MNWEX | $V_{CC} \geq 4.5V$ | MCLK×m-9 | MCLK×m+9 | ns |
| | | | $V_{CC} < 4.5V$ | MCLK×m-12 | MCLK×m+12 | |
| MNALE↓→ MNWEX delay time | $t_{ALEL-NWEL}$ | MNALE, MNWEX | $V_{CC} \geq 4.5V$ | MCLK×m-9 | MCLK×m+9 | ns |
| | | | $V_{CC} < 4.5V$ | MCLK×m-12 | MCLK×m+12 | |
| MNCLE↑→ MNWEX delay time | $t_{CLEH-NWEL}$ | MNCLE, MNWEX | $V_{CC} \geq 4.5V$ | MCLK×m-9 | MCLK×m+9 | ns |
| | | | $V_{CC} < 4.5V$ | MCLK×m-12 | MCLK×m+12 | |
| MNWEX↑→ MNCLE delay time | $t_{NWEH-CLEL}$ | MNCLE, MNWEX | $V_{CC} \geq 4.5V$ | 0 | MCLK×m+9 | ns |
| | | | $V_{CC} < 4.5V$ | | MCLK×m+12 | |
| MNWEX Min pulse width | $t_{NWEW}$ | MNWEX | $V_{CC} \geq 4.5V$ | MCLK×n-3 | - | ns |
| | | | $V_{CC} < 4.5V$ | | | |
| MNWEX↓→ Data output time | $t_{NWEL-DV}$ | MNWEX, MADATA[15:0] | $V_{CC} \geq 4.5V$ | - 9 | + 9 | ns |
| | | | $V_{CC} < 4.5V$ | -12 | +12 | |
| MNWEX↑→ Data hold time | $t_{NWEH-DX}$ | MNWEX, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 0 | MCLK×m+9 | ns |
| | | | $V_{CC} < 4.5V$ | | MCLK×m+12 | |

***Note:***

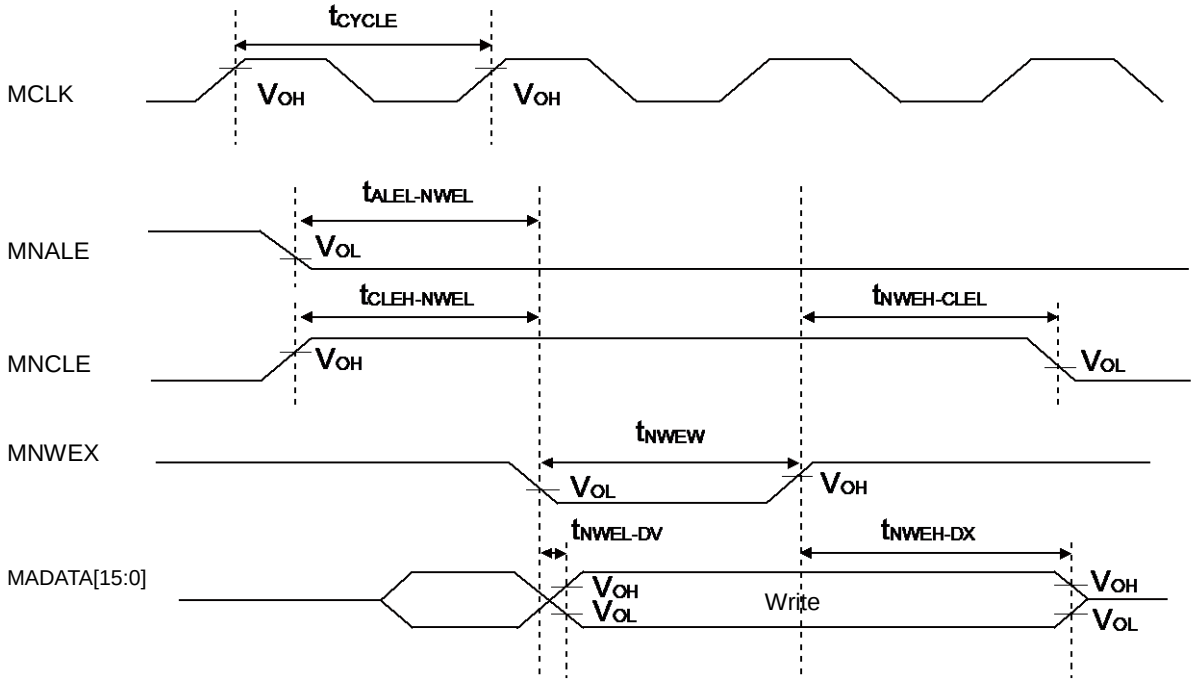
- *When the external load capacitance $C_L$ = 30pF (m = 0 to 15, n = 1 to 16)*



NAND Flash Address Write




NAND Flash Command Write

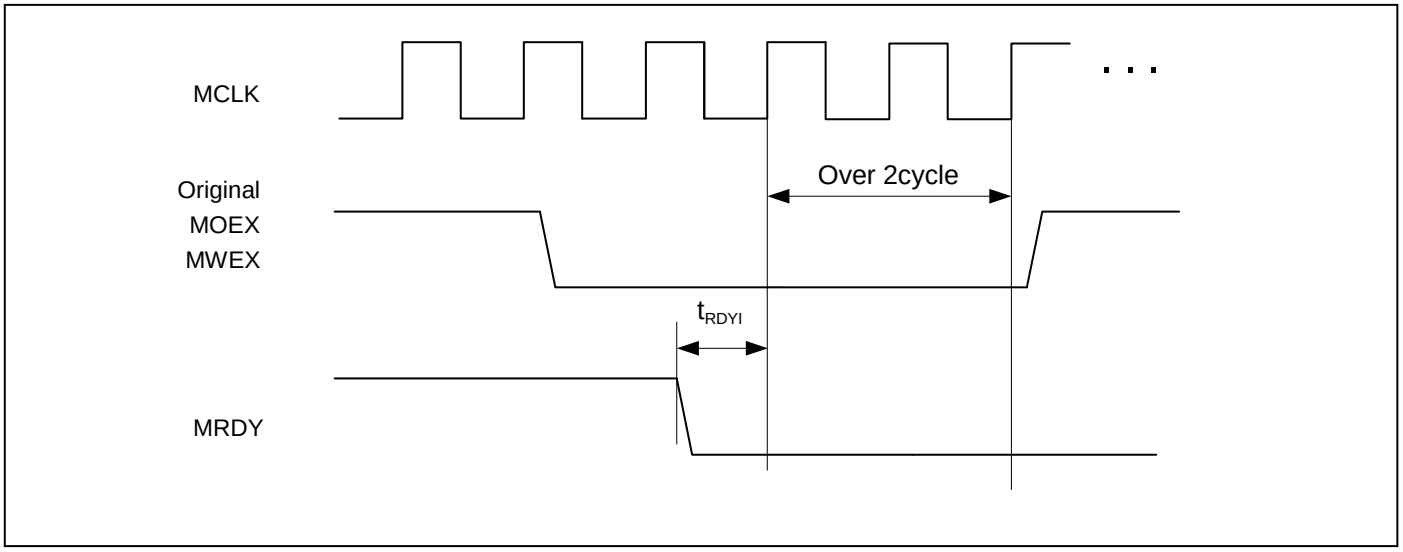


## External Ready Input Timing

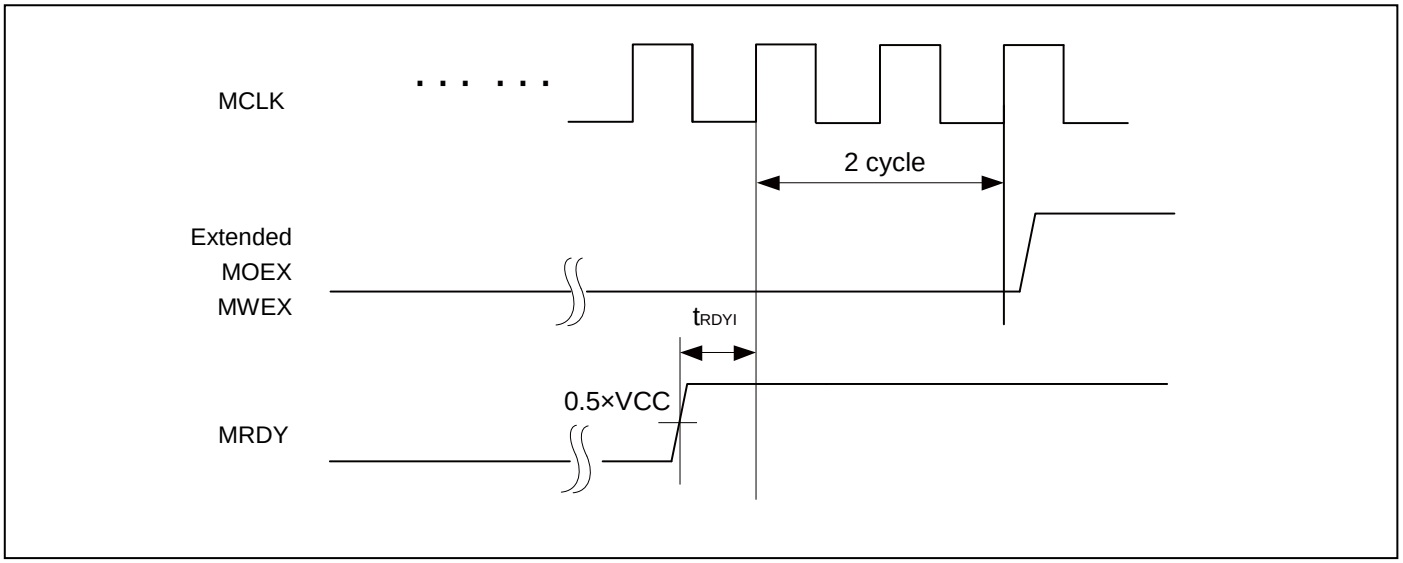
($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| MCLK↑ MRDY input setup time | $t_{RDYI}$ | MCLK, MRDY | $V_{CC}$ ≥ 4.5V | 19 | - | ns | |
| | | | $V_{CC}$ < 4.5V | 37 | | | |

**When RDY is input**




**When RDY is released**



### SDRAM Mode

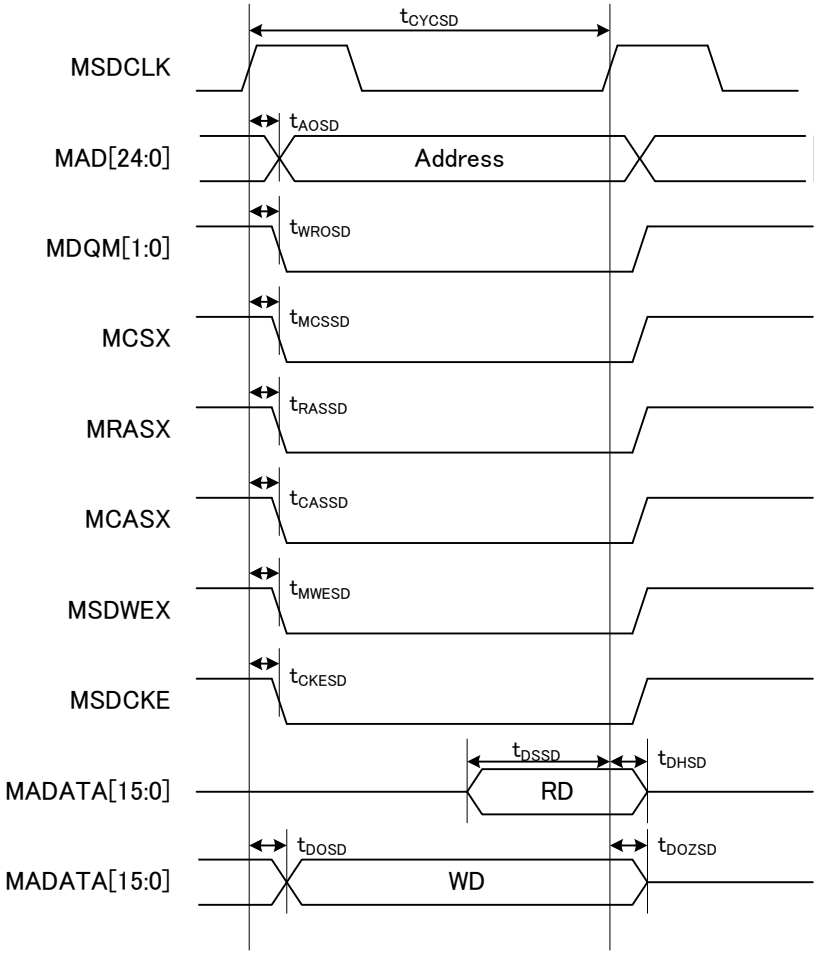
($V_{CC}$ = 2.7V to 3.6V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Output frequency | $t_{CYCSD}$ | MSDCLK | - | 32 | MHz |
| Address delay time | $t_{AOSD}$ | MSDCLK, MAD[15:0] | 2 | 12 | ns |
| MSDCLK↑→Data output delay time | $t_{DOSD}$ | MSDCLK, MADATA[31:0] | 2 | 12 | ns |
| MSDCLK↑→Data output Hi-Z time | $t_{DOZSD}$ | MSDCLK, MADATA[31:0] | 2 | 20 | ns |
| MDQM[1:0] delay time | $t_{WROSD}$ | MSDCLK, MDQM[1:0] | 1 | 12 | ns |
| MCSX delay time | $t_{MCSSD}$ | MSDCLK, MCSX8 | 2 | 12 | ns |
| MRASX delay time | $t_{RASSD}$ | MSDCLK, MRASX | 2 | 12 | ns |
| MCASX delay time | $t_{CASSD}$ | MSDCLK, MCASX | 2 | 12 | ns |
| MSDWEX delay time | $t_{MWESD}$ | MSDCLK, MSDWEX | 2 | 12 | ns |
| MSDCKE delay time | $t_{CKESD}$ | MSDCLK, MSDCKE | 2 | 12 | ns |
| Data set up time | $t_{DSSD}$ | MSDCLK, MADATA[31:0] | 23 | - | ns |
| Data hold time | $t_{DHSD}$ | MSDCLK, MADATA[31:0] | 0 | - | ns |

***Note:***

- *When the external load capacitance $C_L$ = 30pF*

SDRAM Access

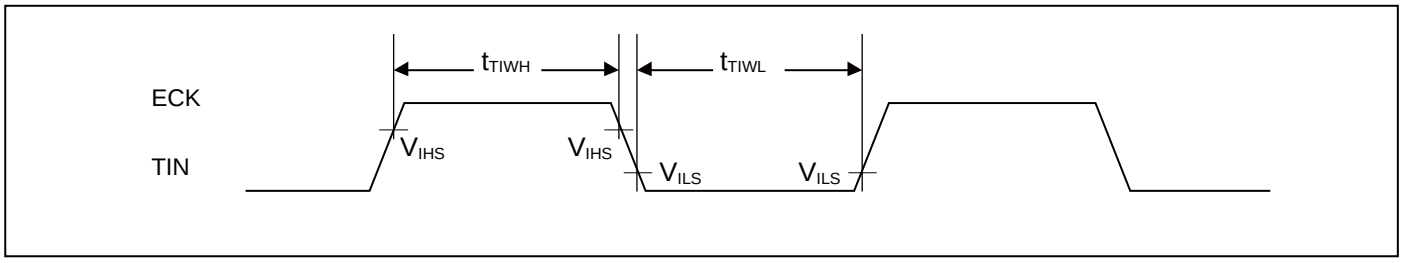


### *12.4.10 Base Timer Input Timing*

#### Timer input timing

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

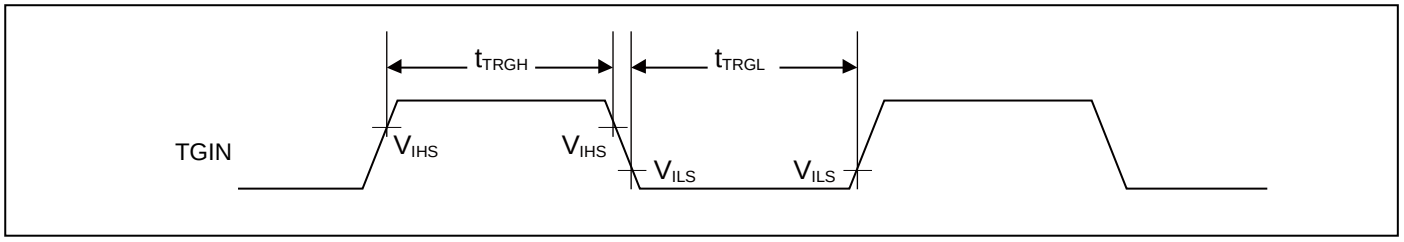
| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TIWH}$, $t_{TIWL}$ | TIOAn/TIOBn (when using as ECK, TIN) | - | $2t_{CYCP}$ | - | ns | |




#### Trigger input timing

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$, $t_{TRGL}$ | TIOAn/TIOBn (when using as TGIN) | - | $2t_{CYCP}$ | - | ns | |




***Note:***

*$t_{CYCP}$ indicates the APB bus clock cycle time.*

About the APB bus number which the Base Timer is connected to, see “Block Diagram” in this datasheet.

### *12.4.11 CSIO/UART Timing*

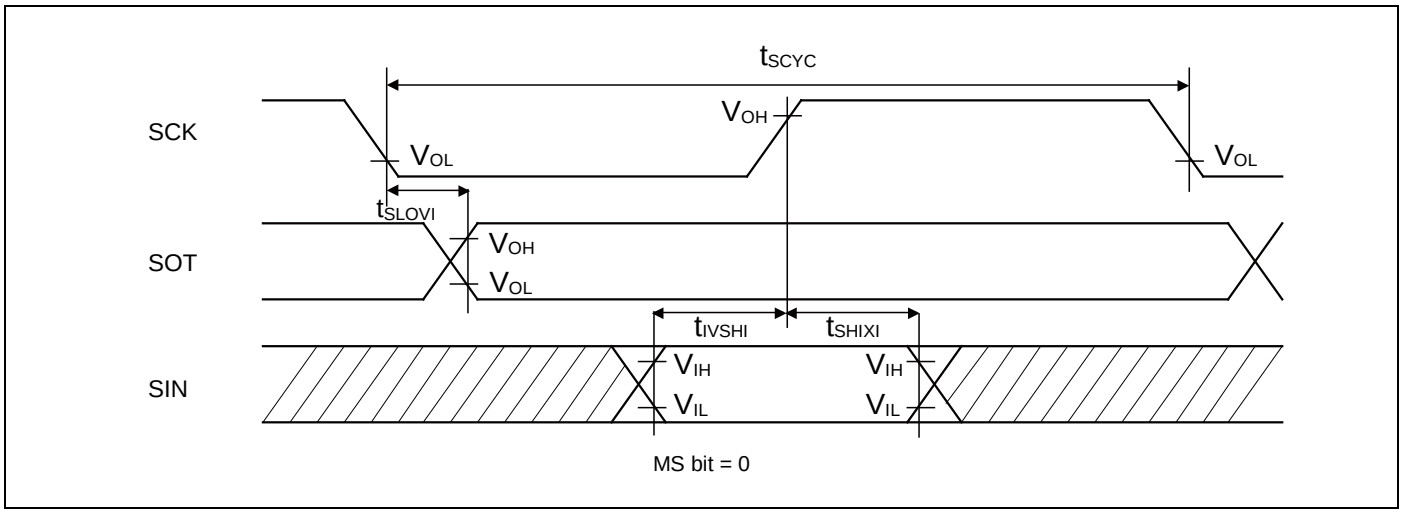
#### Synchronous serial (SPI = 0, SCINV = 0)

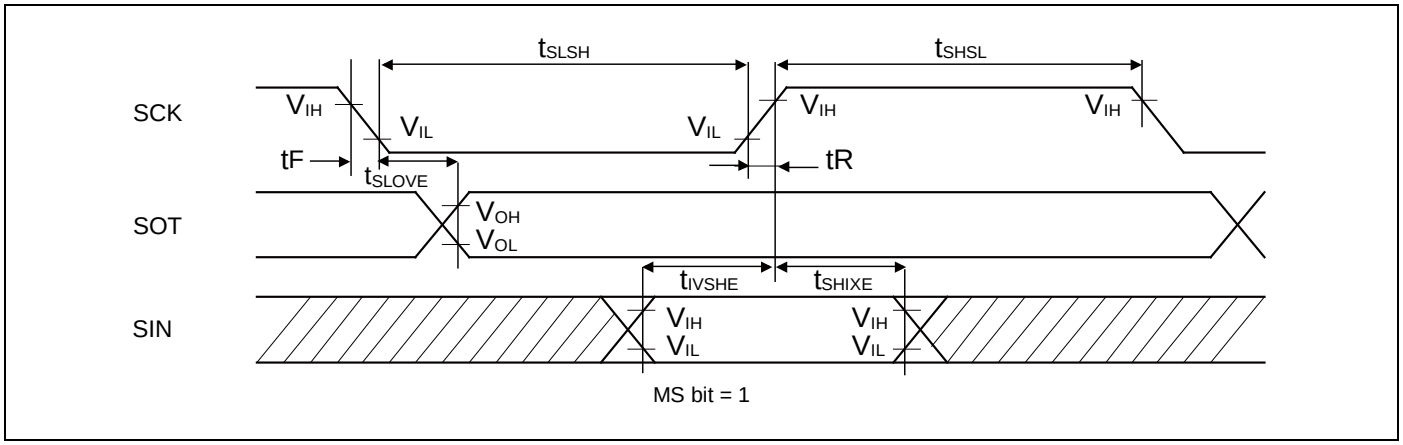
($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Baud rate | - | - | - | - | 8 | - | 8 | Mbps |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Internal shift clock operation | $4t_{CYCP}$ | - | $4t_{CYCP}$ | - | ns |
| SCK↓→SOT delay time | $t_{SLOVI}$ | SCKx, SOTx | | - 30 | + 30 | - 20 | + 20 | ns |
| SIN→SCK↑ setup time | $t_{IVSHI}$ | SCKx, SINx | | 50 | - | 30 | - | ns |
| SCK↑→SIN hold time | $t_{SHIXI}$ | SCKx, SINx | | 0 | - | 0 | - | ns |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCKx | External shift clock operation | $2t_{CYCP}$ - 10 | - | $2t_{CYCP}$ - 10 | - | ns |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK↓→SOT delay time | $t_{SLOVE}$ | SCKx, SOTx | | - | 50 | - | 30 | ns |
| SIN→SCK↑ setup time | $t_{IVSHE}$ | SCKx, SINx | | 10 | - | 10 | - | ns |
| SCK↑→SIN hold time | $t_{SHIXE}$ | SCKx, SINx | | 20 | - | 20 | - | ns |
| SCK falling time | tF | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | tR | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

- *The above characteristics apply to CLK synchronous mode.*
- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *These characteristics only guarantee the same relocate port number.*
  *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance $C_L$ = 30pF.*


tSCYC
SCK
VOH
VOL
VOL
tSLOVI
SOT
VOH
VOL
tIVSHI
tSHIXI
SIN
VIH
VIL
VIH
VIL
MS bit = 0


tSLSH
tSHSL
SCK
VIH
VIL
VIL
VIH
VIH
tF
tSLOVE
tR
SOT
VOH
VOL
tIVSHE
tSHIXE
SIN
VIH
VIL
VIH
VIL
MS bit = 1

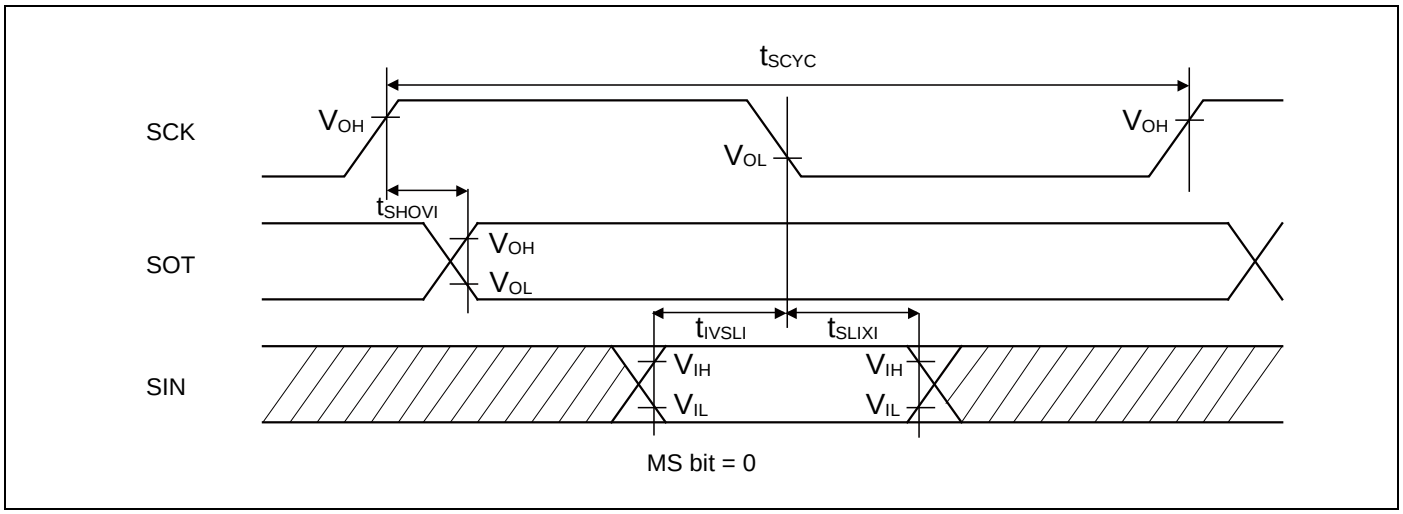
### Synchronous serial (SPI = 0, SCINV = 1)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

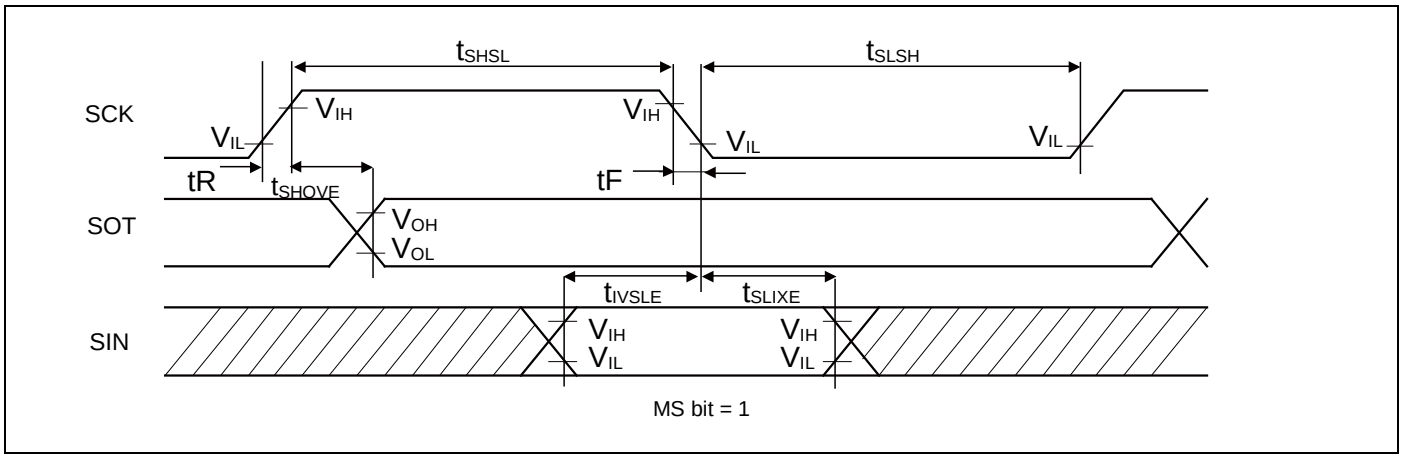
| Parameter | Symbol | Pin name | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Baud rate | - | - | - | - | 8 | - | 8 | Mbps |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Internal shift clock operation | $4t_{CYCP}$ | - | $4t_{CYCP}$ | - | ns |
| SCK↑→SOT delay time | $t_{SHOVI}$ | SCKx, SOTx | | - 30 | + 30 | - 20 | + 20 | ns |
| SIN→SCK↓ setup time | $t_{IVSLI}$ | SCKx, SINx | | 50 | - | 30 | - | ns |
| SCK↓→SIN hold time | $t_{SLIXI}$ | SCKx, SINx | | 0 | - | 0 | - | ns |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCKx | External shift clock operation | $2t_{CYCP}$ - 10 | - | $2t_{CYCP}$ - 10 | - | ns |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK↑→SOT delay time | $t_{SHOVE}$ | SCKx, SOTx | | - | 50 | - | 30 | ns |
| SIN→SCK↓ setup time | $t_{IVSLE}$ | SCKx, SINx | | 10 | - | 10 | - | ns |
| SCK↓→SIN hold time | $t_{SLIXE}$ | SCKx, SINx | | 20 | - | 20 | - | ns |
| SCK falling time | tF | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | tR | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

- *The above characteristics apply to CLK synchronous mode.*
- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *These characteristics only guarantee the same relocate port number.*
  *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance $C_L$ = 30pF.*




MS bit = 0




MS bit = 1

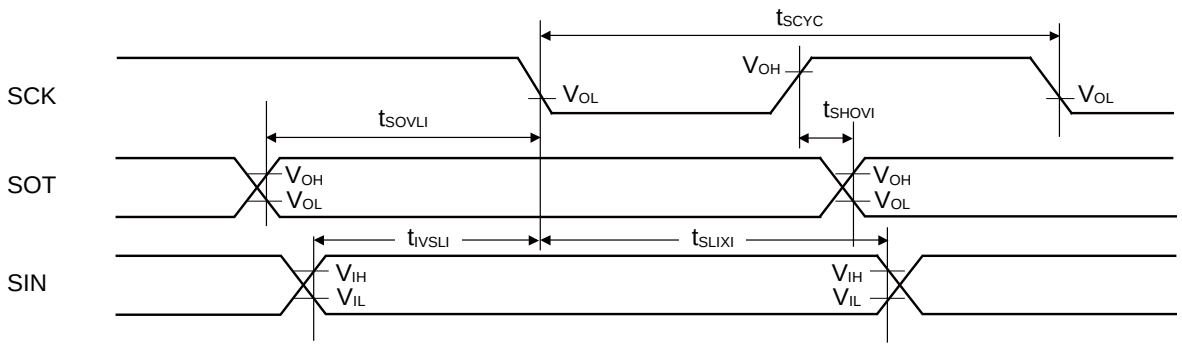
### Synchronous serial (SPI = 1, SCINV = 0)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

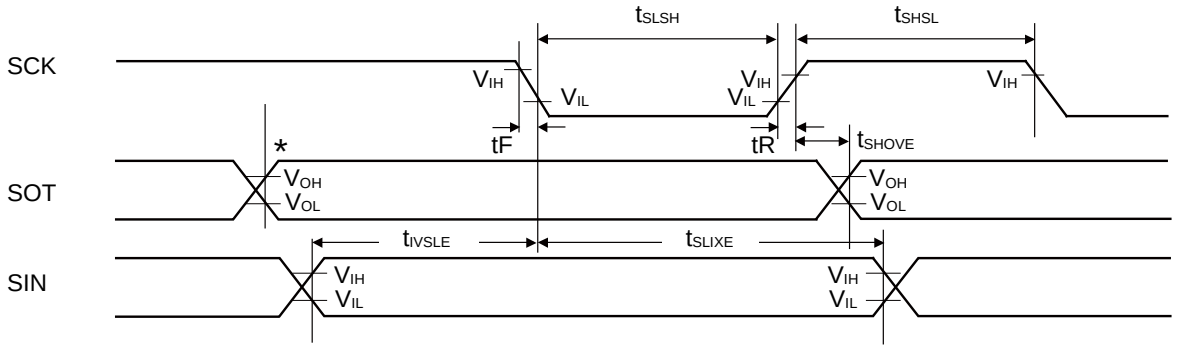
| Parameter | Symbol | Pin name | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Baud rate | - | - | - | - | 8 | - | 8 | Mbps |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Internal shift clock operation | $4t_{CYCP}$ | - | $4t_{CYCP}$ | - | ns |
| SCK↑→SOT delay time | $t_{SHOVI}$ | SCKx, SOTx | | - 30 | + 30 | - 20 | + 20 | ns |
| SIN→SCK↓ setup time | $t_{IVSLI}$ | SCKx, SINx | | 50 | - | 30 | - | ns |
| SCK↓→SIN hold time | $t_{SLIXI}$ | SCKx, SINx | | 0 | - | 0 | - | ns |
| SOT→SCK↓ delay time | $t_{SOVLI}$ | SCKx, SOTx | | $2t_{CYCP}$ - 30 | - | $2t_{CYCP}$ - 30 | - | ns |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCKx | External shift clock operation | $2t_{CYCP}$ - 10 | - | $2t_{CYCP}$ - 10 | - | ns |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK↑→SOT delay time | $t_{SHOVE}$ | SCKx, SOTx | | - | 50 | - | 30 | ns |
| SIN→SCK↓ setup time | $t_{IVSLE}$ | SCKx, SINx | | 10 | - | 10 | - | ns |
| SCK↓→SIN hold time | $t_{SLIXE}$ | SCKx, SINx | | 20 | - | 20 | - | ns |
| SCK falling time | tF | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | tR | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

- *The above characteristics apply to CLK synchronous mode.*
- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
- *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *These characteristics only guarantee the same relocate port number.*
  *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance $C_L$ = 30pF.*




MS bit = 0




MS bit = 1

*: Changes when writing to TDR register

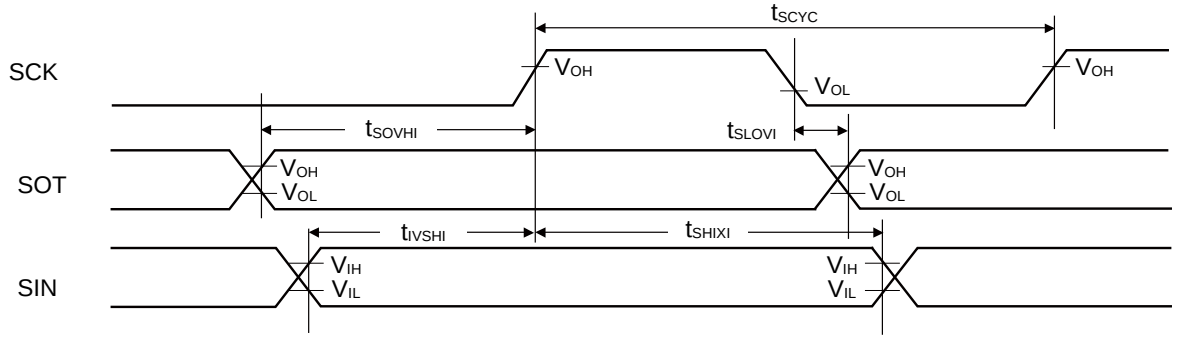
### Synchronous serial (SPI = 1, SCINV = 1)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

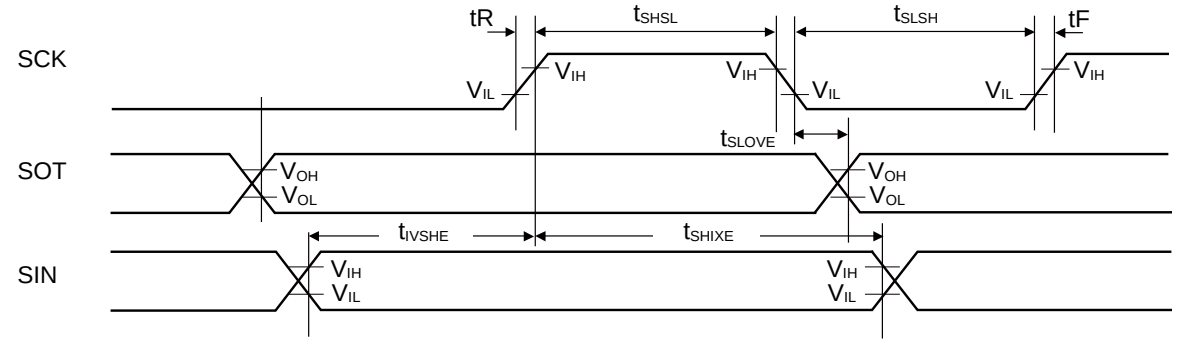
| Parameter | Symbol | Pin name | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Baud rate | - | - | - | - | 8 | - | 8 | Mbps |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Internal shift clock operation | $4t_{CYCP}$ | - | $4t_{CYCP}$ | - | ns |
| SCK↓→SOT delay time | $t_{SLOVI}$ | SCKx, SOTx | | - 30 | + 30 | - 20 | + 20 | ns |
| SIN→SCK↑ setup time | $t_{IVSHI}$ | SCKx, SINx | | 50 | - | 30 | - | ns |
| SCK↑→SIN hold time | $t_{SHIXI}$ | SCKx, SINx | | 0 | - | 0 | - | ns |
| SOT→SCK↑ delay time | $t_{SOVHI}$ | SCKx, SOTx | | $2t_{CYCP}$ - 30 | - | $2t_{CYCP}$ - 30 | - | ns |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCKx | External shift clock operation | $2t_{CYCP}$ - 10 | - | $2t_{CYCP}$ - 10 | - | ns |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK↓→SOT delay time | $t_{SLOVE}$ | SCKx, SOTx | | - | 50 | - | 30 | ns |
| SIN→SCK↑ setup time | $t_{IVSHE}$ | SCKx, SINx | | 10 | - | 10 | - | ns |
| SCK↑→SIN hold time | $t_{SHIXE}$ | SCKx, SINx | | 20 | - | 20 | - | ns |
| SCK falling time | tF | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | tR | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

- *The above characteristics apply to CLK synchronous mode.*
- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *These characteristics only guarantee the same relocate port number.*
  *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance $C_L$ = 30pF.*




MS bit = 0




MS bit = 1

### When using synchronous serial chip select (SCINV = 0, CSLVL = 1)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCS↓→SCK↓setup time | $t_{CSSI}$ | Internal shift clock operation | (*1)-50 | (*1)+0 | (*1)-50 | (*1)+0 | ns |
| SCK↑→SCS↑ hold time | $t_{CSHI}$ | | (*2)+0 | (*2)+50 | (*2)+0 | (*2)+50 | ns |
| SCS deselect time | $t_{CSDI}$ | | (*3)-50 +5$t_{CYCP}$ | (*3)+50 +5$t_{CYCP}$ | (*3)-50 +5$t_{CYCP}$ | (*3)+50 +5$t_{CYCP}$ | ns |
| SCS↓→SCK↓setup time | $t_{CSSE}$ | External shift clock operation | 3$t_{CYCP}$+30 | - | 3$t_{CYCP}$+30 | - | ns |
| SCK↑→SCS↑ hold time | $t_{CSHE}$ | | 0 | - | 0 | - | ns |
| SCS deselect time | $t_{CSDE}$ | | 3$t_{CYCP}$+30 | - | 3$t_{CYCP}$+30 | - | ns |
| SCS↓→SUT delay time | $t_{DSE}$ | | - | 40 | - | 40 | ns |
| SCS↑→SUT delay time | $t_{DEE}$ | | 0 | - | 0 | - | ns |

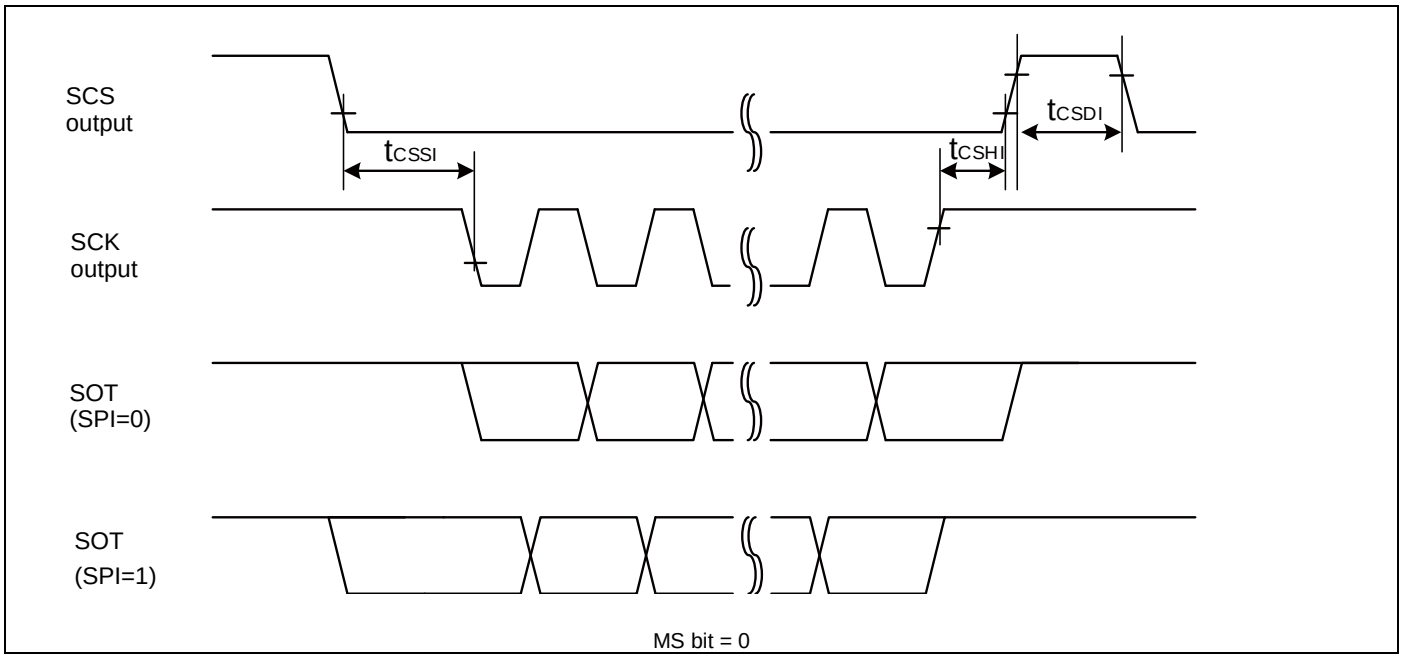
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

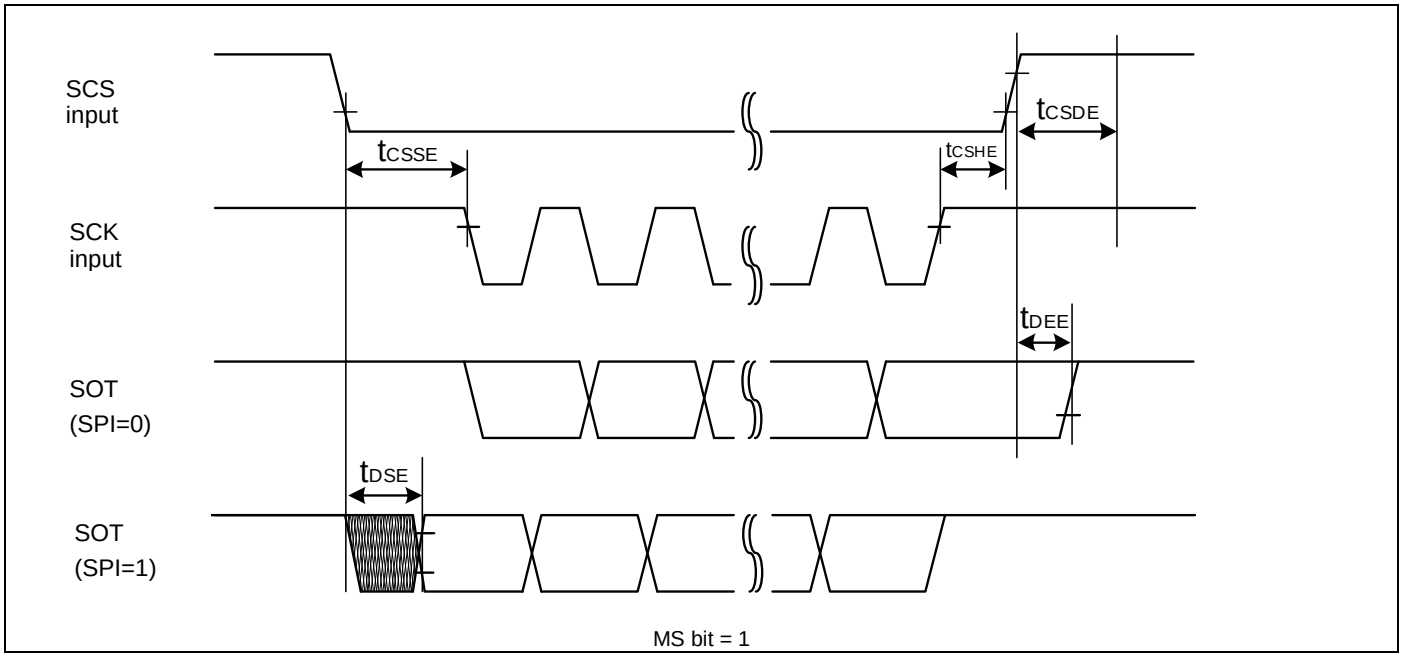
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

***Notes:***

- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM4 Family Peripheral Manual".*
- *When the external load capacitance $C_L$ = 30pF.*




MS bit = 0




MS bit = 1

### When using synchronous serial chip select (SCINV = 1, CSLVL = 1)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCS↓→SCK↑setup time | $t_{CSSI}$ | Internal shift clock operation | (*1)-50 | (*1)+0 | (*1)-50 | (*1)+0 | ns |
| SCK↓→SCS↑ hold time | $t_{CSHI}$ | | (*2)+0 | (*2)+50 | (*2)+0 | (*2)+50 | ns |
| SCS deselect time | $t_{CSDI}$ | | (*3)-50 +5$t_{CYCP}$ | (*3)+50 +5$t_{CYCP}$ | (*3)-50 +5$t_{CYCP}$ | (*3)+50 +5$t_{CYCP}$ | ns |
| SCS↓→SCK↑setup time | $t_{CSSE}$ | External shift clock operation | 3$t_{CYCP}$+30 | - | 3$t_{CYCP}$+30 | - | ns |
| SCK↓→SCS↑ hold time | $t_{CSHE}$ | | 0 | - | 0 | - | ns |
| SCS deselect time | $t_{CSDE}$ | | 3$t_{CYCP}$+30 | - | 3$t_{CYCP}$+30 | - | ns |
| SCS↓→SOT delay time | $t_{DSE}$ | | - | 40 | - | 40 | ns |
| SCS↑→SOT delay time | $t_{DEE}$ | | 0 | - | 0 | - | ns |

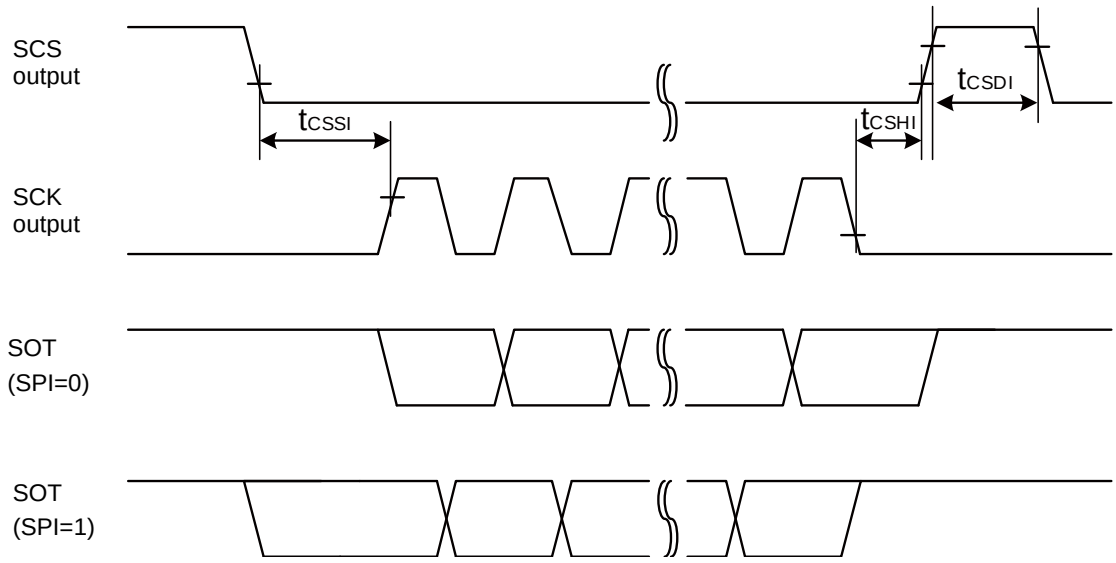
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

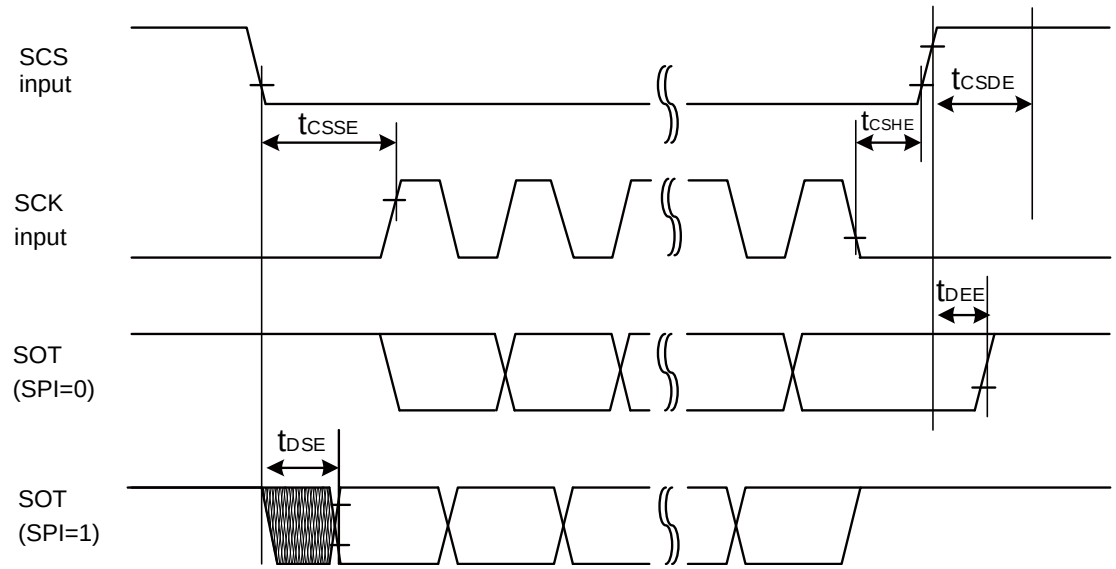
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

***Notes:***

- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM4 Family Peripheral Manual".*
- *When the external load capacitance $C_L$ = 30pF.*




MS bit = 0




MS bit = 1

### When using synchronous serial chip select (SCINV = 0, CSLVL = 0)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCS↑→SCK↓setup time | $t_{CSSI}$ | Internal shift clock operation | (*1)-50 | (*1)+0 | (*1)-50 | (*1)+0 | ns |
| SCK↑→SCS↓ hold time | $t_{CSHI}$ | | (*2)+0 | (*2)+50 | (*2)+0 | (*2)+50 | ns |
| SCS deselect time | $t_{CSDI}$ | | (*3)-50 +5$t_{CYCP}$ | (*3)+50 +5$t_{CYCP}$ | (*3)-50 +5$t_{CYCP}$ | (*3)+50 +5$t_{CYCP}$ | ns |
| SCS↑→SCK↓setup time | $t_{CSSE}$ | External shift clock operation | 3$t_{CYCP}$+30 | - | 3$t_{CYCP}$+30 | - | ns |
| SCK↑→SCS↓ hold time | $t_{CSHE}$ | | 0 | - | 0 | - | ns |
| SCS deselect time | $t_{CSDE}$ | | 3$t_{CYCP}$+30 | - | 3$t_{CYCP}$+30 | - | ns |
| SCS↑→SOT delay time | $t_{DSE}$ | | - | 40 | - | 40 | ns |
| SCS↓→SOT delay time | $t_{DEE}$ | | 0 | - | 0 | - | ns |

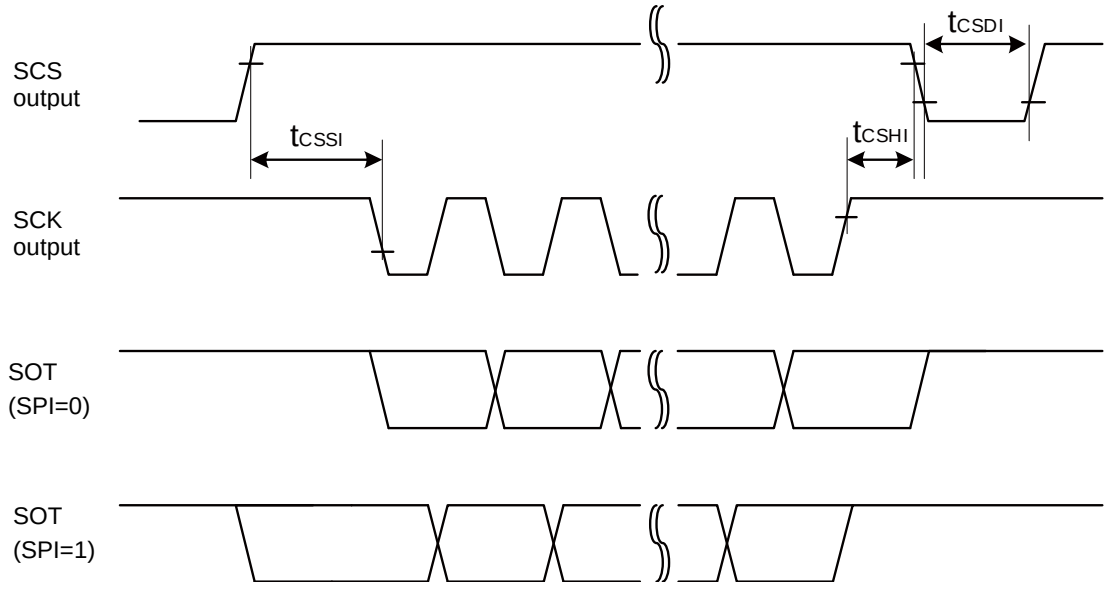
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

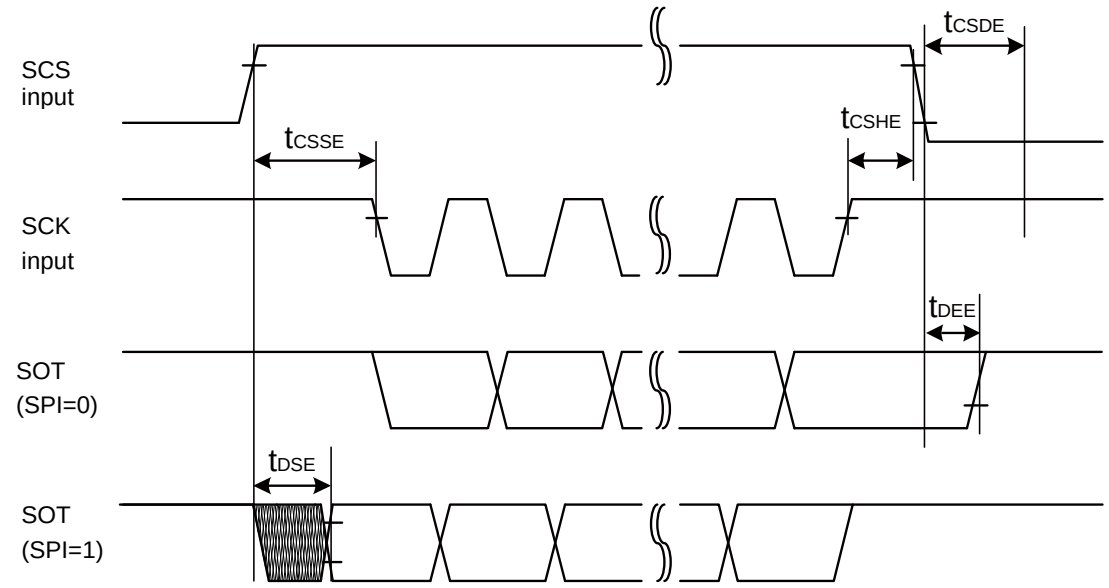
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

***Notes:***

- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM4 Family Peripheral Manual".*
- *When the external load capacitance $C_L$ = 30pF.*




MS bit = 0




MS bit = 1

### When using synchronous serial chip select (SCINV = 1, CSLVL = 0)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCS↑→SCK↑setup time | $t_{CSSI}$ | Internal shift clock operation | (*1)-50 | (*1)+0 | (*1)-50 | (*1)+0 | ns |
| SCK↓→SCS↓ hold time | $t_{CSHI}$ | | (*2)+0 | (*2)+50 | (*2)+0 | (*2)+50 | ns |
| SCS deselect time | $t_{CSDI}$ | | (*3)-50 +5$t_{CYCP}$ | (*3)+50 +5$t_{CYCP}$ | (*3)-50 +5$t_{CYCP}$ | (*3)+50 +5$t_{CYCP}$ | ns |
| SCS↑→SCK↑setup time | $t_{CSSE}$ | External shift clock operation | 3$t_{CYCP}$+30 | - | 3$t_{CYCP}$+30 | - | ns |
| SCK↓→SCS↓ hold time | $t_{CSHE}$ | | 0 | - | 0 | - | ns |
| SCS deselect time | $t_{CSDE}$ | | 3$t_{CYCP}$+30 | - | 3$t_{CYCP}$+30 | - | ns |
| SCS↑→SOT delay time | $t_{DSE}$ | | - | 40 | - | 40 | ns |
| SCS↓→SOT delay time | $t_{DEE}$ | | 0 | - | 0 | - | ns |

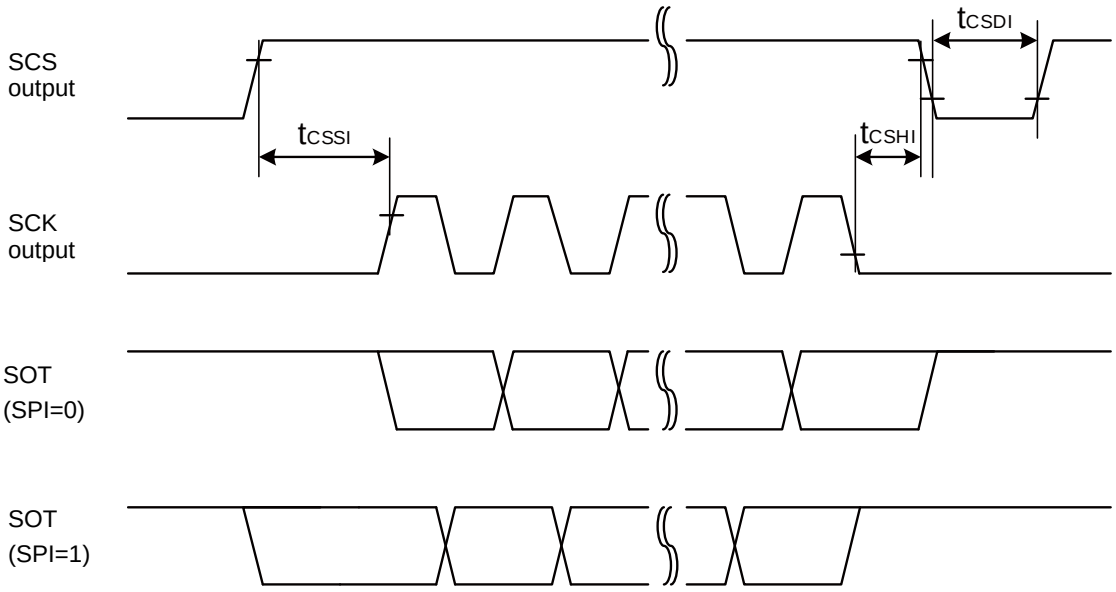
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

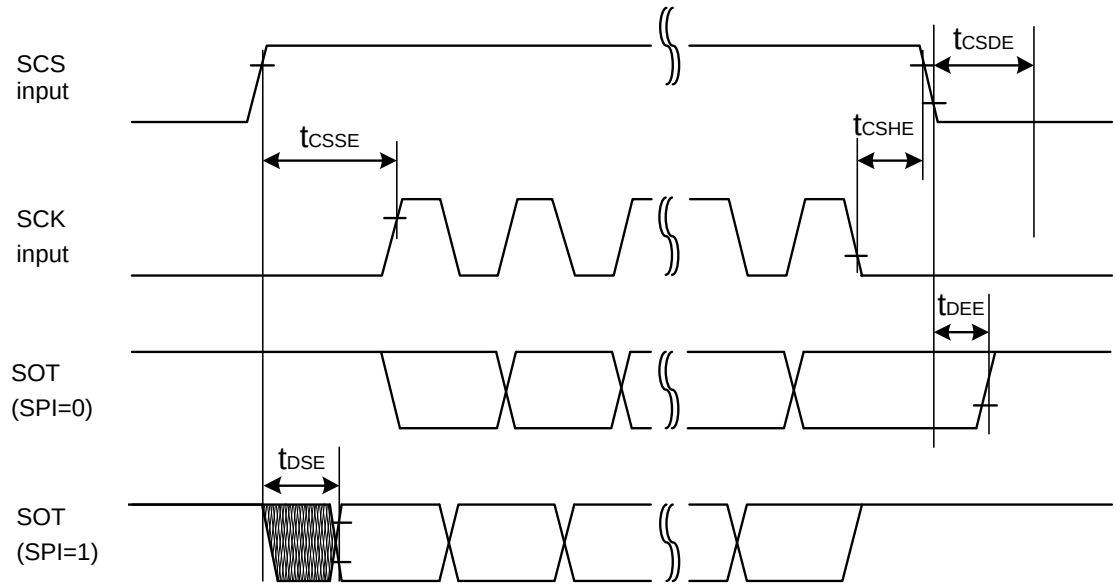
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

***Notes:***

- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM4 Family Peripheral Manual".*
- *When the external load capacitance $C_L$ = 30pF.*




MS bit = 0




MS bit = 1

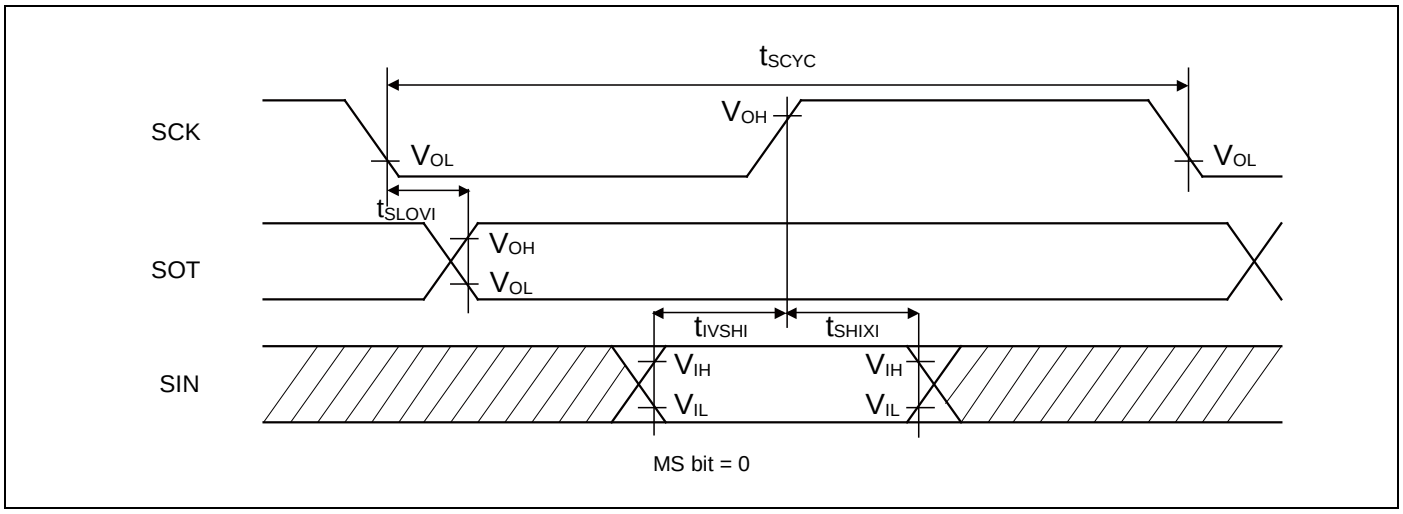
### High-speed synchronous serial (SPI = 0, SCINV = 0)

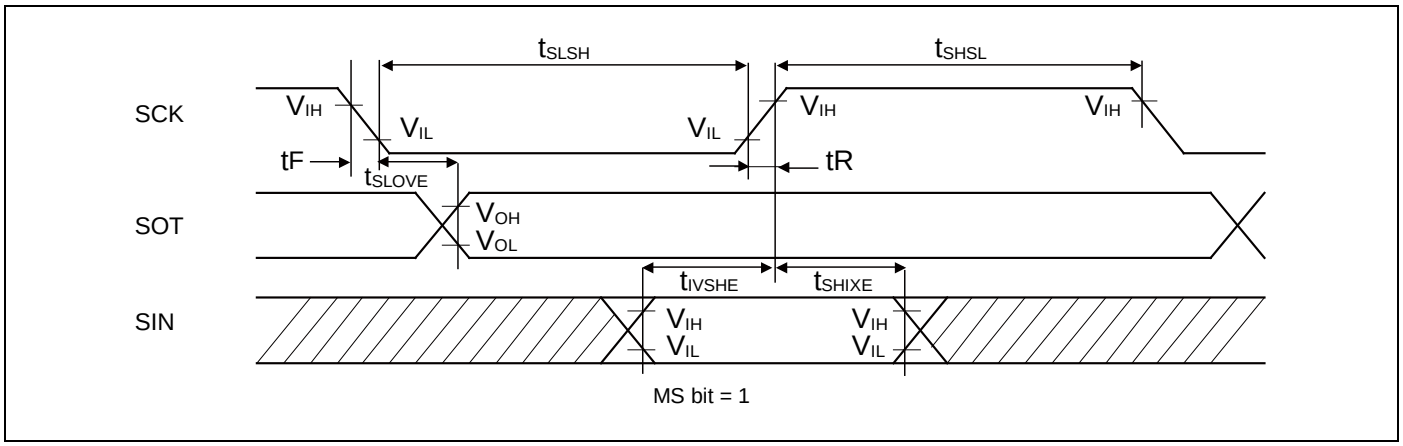
($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Internal shift clock operation | $4t_{CYCP}$ | - | $4t_{CYCP}$ | - | ns |
| SCK↓→SOT delay time | $t_{SLOVI}$ | SCKx, SOTx | | -10 | +10 | -10 | +10 | ns |
| SIN→SCK↑ setup time | $t_{IVSHI}$ | SCKx, SINx | | 14 / 12.5* | - | 12.5 | - | ns |
| SCK↑→SIN hold time | $t_{SHIXI}$ | SCKx, SINx | | 5 | - | 5 | - | ns |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCKx | External shift clock operation | $2t_{CYCP}$ – 5 | - | $2t_{CYCP}$ – 5 | - | ns |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK↓→SOT delay time | $t_{SLOVE}$ | SCKx, SOTx | | - | 15 | - | 15 | ns |
| SIN→SCK↑ setup time | $t_{IVSHE}$ | SCKx, SINx | | 5 | - | 5 | - | ns |
| SCK↑→SIN hold time | $t_{SHIXE}$ | SCKx, SINx | | 5 | - | 5 | - | ns |
| SCK falling time | tF | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | tR | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

- *The above characteristics apply to CLK synchronous mode.*
- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN4_1, SOT4_1, SCK4_1*
  - *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance $C_L$ = 30pF. (For *, when $C_L$ = 10pF)*


tSCYC
SCK
VOH
VOL
VOL
tSLOVI
SOT
VOH
VOL
tIVSHI
tSHIXI
SIN
VIH
VIL
VIH
VIL
MS bit = 0


tSLSH
tSHSL
SCK
VIH
VIL
VIL
VIH
VIH
tF
tSLOVE
tR
SOT
VOH
VOL
tIVSHE
tSHIXE
SIN
VIH
VIL
VIH
VIL
MS bit = 1

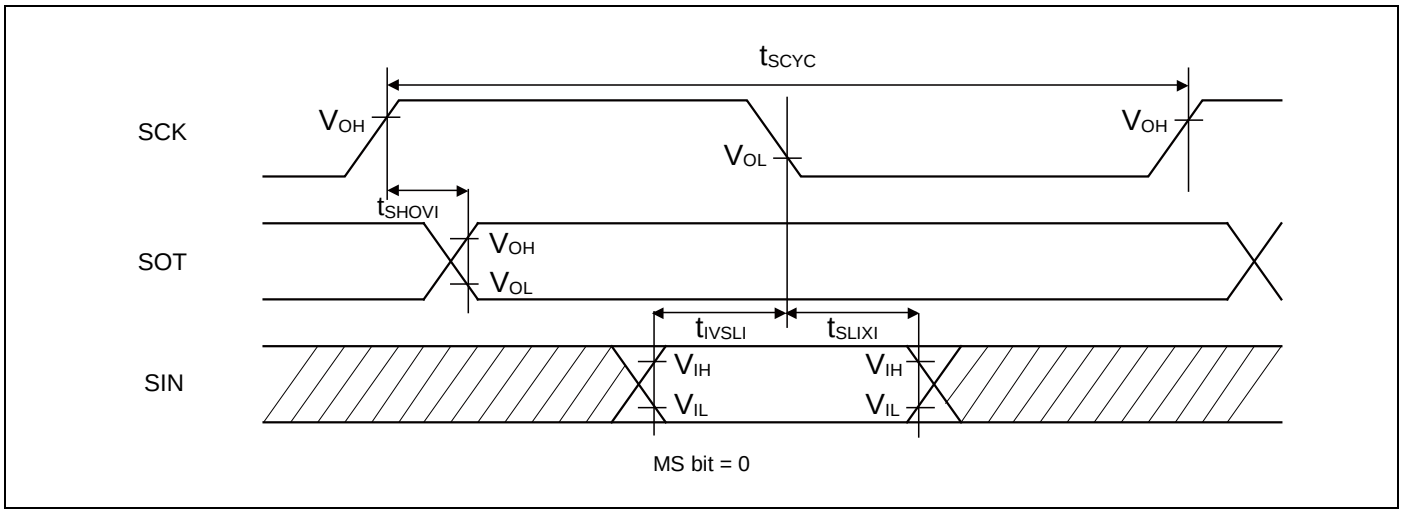
### High-speed synchronous serial (SPI = 0, SCINV = 1)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

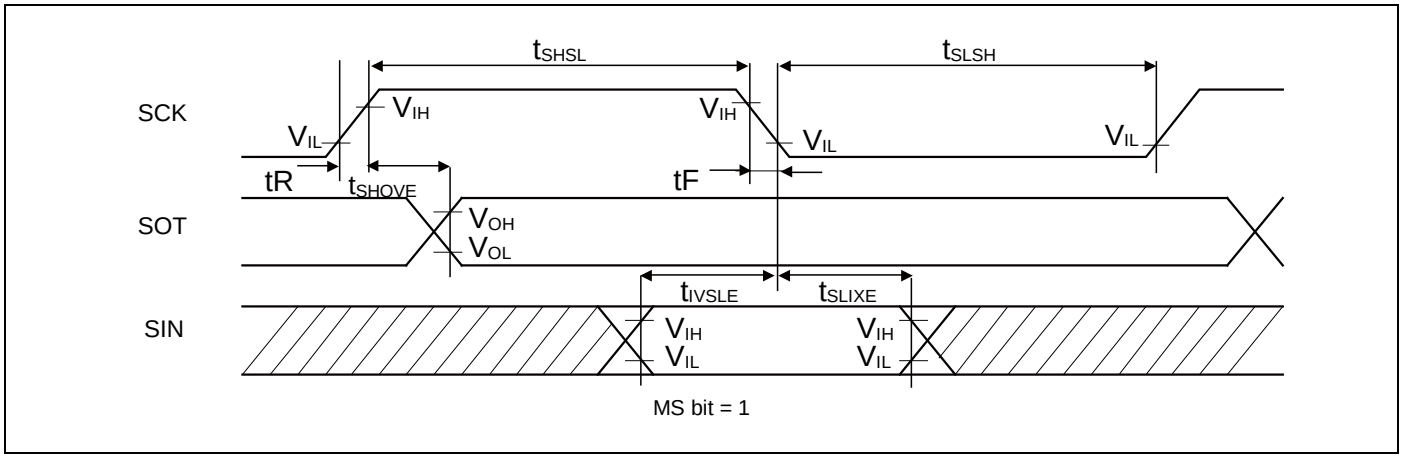
| Parameter | Symbol | Pin name | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Internal shift clock operation | $4t_{CYCP}$ | - | $4t_{CYCP}$ | - | ns |
| SCK↑→SOT delay time | $t_{SHOVI}$ | SCKx, SOTx | | -10 | +10 | -10 | +10 | ns |
| SIN→SCK↓ setup time | $t_{IVSLI}$ | SCKx, SINx | | 14<br>12.5* | - | 12.5 | - | ns |
| SCK↓→SIN hold time | $t_{SLIXI}$ | SCKx, SINx | | 5 | - | 5 | - | ns |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCKx | External shift clock operation | $2t_{CYCP}$ – 5 | - | $2t_{CYCP}$ – 5 | - | ns |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK↑→SOT delay time | $t_{SHOVE}$ | SCKx, SOTx | | - | 15 | - | 15 | ns |
| SIN→SCK↓ setup time | $t_{IVSLE}$ | SCKx, SINx | | 5 | - | 5 | - | ns |
| SCK↓→SIN hold time | $t_{SLIXE}$ | SCKx, SINx | | 5 | - | 5 | - | ns |
| SCK falling time | tF | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | tR | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

- *The above characteristics apply to CLK synchronous mode.*
- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN4_1, SOT4_1, SCK4_1*
  - *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance $C_L$ = 30pF. (For *, when $C_L$ = 10pF)*




MS bit = 0




MS bit = 1

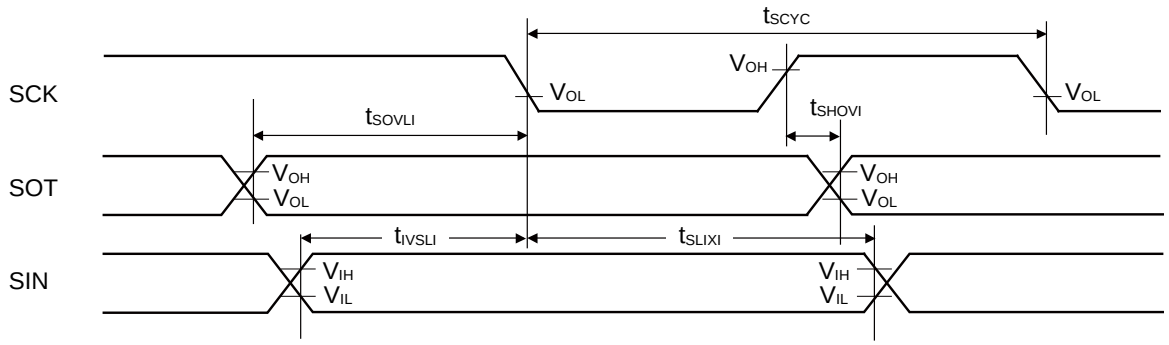
### High-speed synchronous serial (SPI = 1, SCINV = 0)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

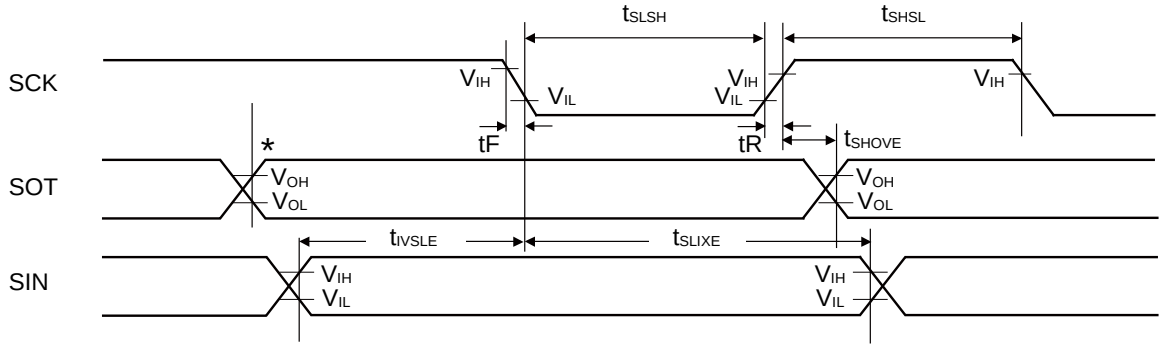
| Parameter | Symbol | Pin name | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Internal shift clock operation | $4t_{CYCP}$ | - | $4t_{CYCP}$ | - | ns |
| SCK↑→SOT delay time | $t_{SHOVI}$ | SCKx, SOTx | | -10 | +10 | -10 | +10 | ns |
| SIN→SCK↓ setup time | $t_{IVSLI}$ | SCKx, SINx | | 14<br>12.5* | - | 12.5 | - | ns |
| SCK↓→SIN hold time | $t_{SLIXI}$ | SCKx, SINx | | 5 | - | 5 | - | ns |
| SOT→SCK↓ delay time | $t_{SOVLI}$ | SCKx, SOTx | | $2t_{CYCP}$ – 10 | - | $2t_{CYCP}$ – 10 | - | ns |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCKx | External shift clock operation | $2t_{CYCP}$ – 5 | - | $2t_{CYCP}$ – 5 | - | ns |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK↑→SOT delay time | $t_{SHOVE}$ | SCKx, SOTx | | - | 15 | - | 15 | ns |
| SIN→SCK↓ setup time | $t_{IVSLE}$ | SCKx, SINx | | 5 | - | 5 | - | ns |
| SCK↓→SIN hold time | $t_{SLIXE}$ | SCKx, SINx | | 5 | - | 5 | - | ns |
| SCK falling time | tF | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | tR | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

- *The above characteristics apply to CLK synchronous mode.*
- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN4_1, SOT4_1, SCK4_1*
  - *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance $C_L$ = 30pF. (For *, when $C_L$ = 10pF)*




MS bit = 0




MS bit = 1

*: Changes when writing to TDR register

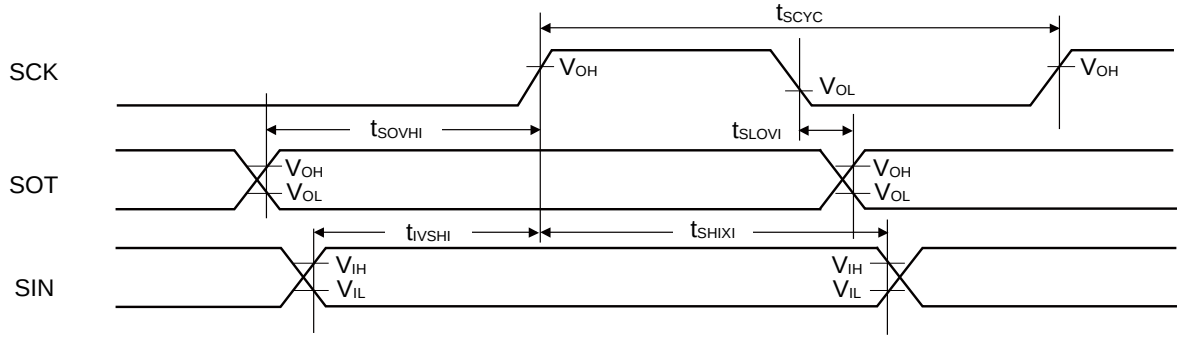
### High-speed synchronous serial (SPI = 1, SCINV = 1)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

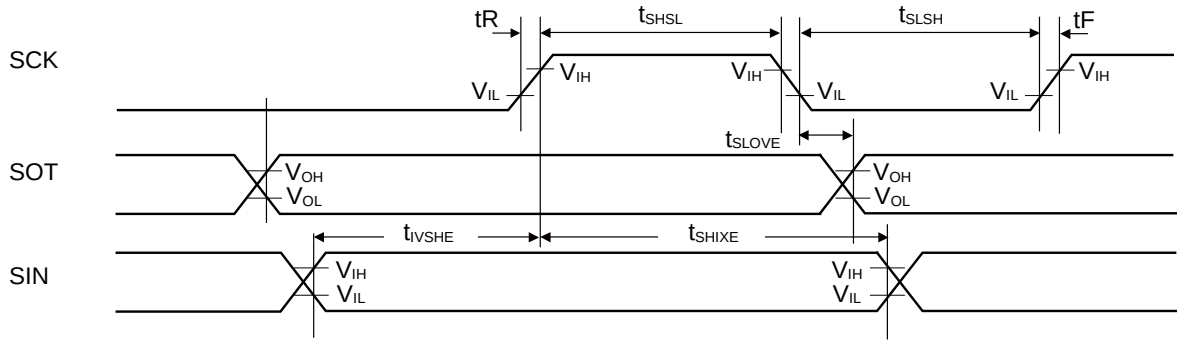
| Parameter | Symbol | Pin name | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Internal shift clock operation | $t_{SCYC}$ | SCKx | Internal shift clock operation | $4t_{CYCP}$ | - | $4t_{CYCP}$ | - | ns |
| SCK↓→SOT delay time | $t_{SLOVI}$ | SCKx, SOTx | | -10 | +10 | -10 | +10 | ns |
| SIN→SCK↑ setup time | $t_{IVSHI}$ | SCKx, SINx | | 14<br>12.5* | - | 12.5 | - | ns |
| SCK↑→SIN hold time | $t_{SHIXI}$ | SCKx, SINx | | 5 | - | 5 | - | ns |
| SOT→SCK↑ delay time | $t_{SOVHI}$ | SCKx, SOTx | | $2t_{CYCP}$ – 10 | - | $2t_{CYCP}$ – 10 | - | ns |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCKx | External shift clock operation | $2t_{CYCP}$ – 5 | - | $2t_{CYCP}$ – 5 | - | ns |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK↓→SOT delay time | $t_{SLOVE}$ | SCKx, SOTx | | - | 15 | - | 15 | ns |
| SIN→SCK↑ setup time | $t_{IVSHE}$ | SCKx, SINx | | 5 | - | 5 | - | ns |
| SCK↑→SIN hold time | $t_{SHIXE}$ | SCKx, SINx | | 5 | - | 5 | - | ns |
| SCK falling time | tF | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | tR | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

- *The above characteristics apply to CLK synchronous mode.*
- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN4_1, SOT4_1, SCK4_1*
  - *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance $C_L$ = 30pF. (For *, when $C_L$ = 10pF)*




MS bit = 0




MS bit = 1

### When using high-speed synchronous serial chip select (SCINV = 0, CSLVL = 1)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCS↓→SCK↓setup time | $t_{CSSI}$ | Internal shift clock operation | (*1)-20 | (*1)+0 | (*1)-20 | (*1)+0 | ns |
| SCK↑→SCS↑ hold time | $t_{CSHI}$ | | (*2)+0 | (*2)+20 | (*2)+0 | (*2)+20 | ns |
| SCS deselect time | $t_{CSDI}$ | | (*3)-20 +5$t_{CYCP}$ | (*3)+20 +5$t_{CYCP}$ | (*3)-20 +5$t_{CYCP}$ | (*3)+20 +5$t_{CYCP}$ | ns |
| SCS↓→SCK↓setup time | $t_{CSSE}$ | External shift clock operation | 3$t_{CYCP}$+15 | - | 3$t_{CYCP}$+15 | - | ns |
| SCK↑→SCS↑ hold time | $t_{CSHE}$ | | 0 | - | 0 | - | ns |
| SCS deselect time | $t_{CSDE}$ | | 3$t_{CYCP}$+15 | - | 3$t_{CYCP}$+15 | - | ns |
| SCS↓→SOT delay time | $t_{DSE}$ | | - | 25 | - | 25 | ns |
| SCS↑→SOT delay time | $t_{DEE}$ | | 0 | - | 0 | - | ns |

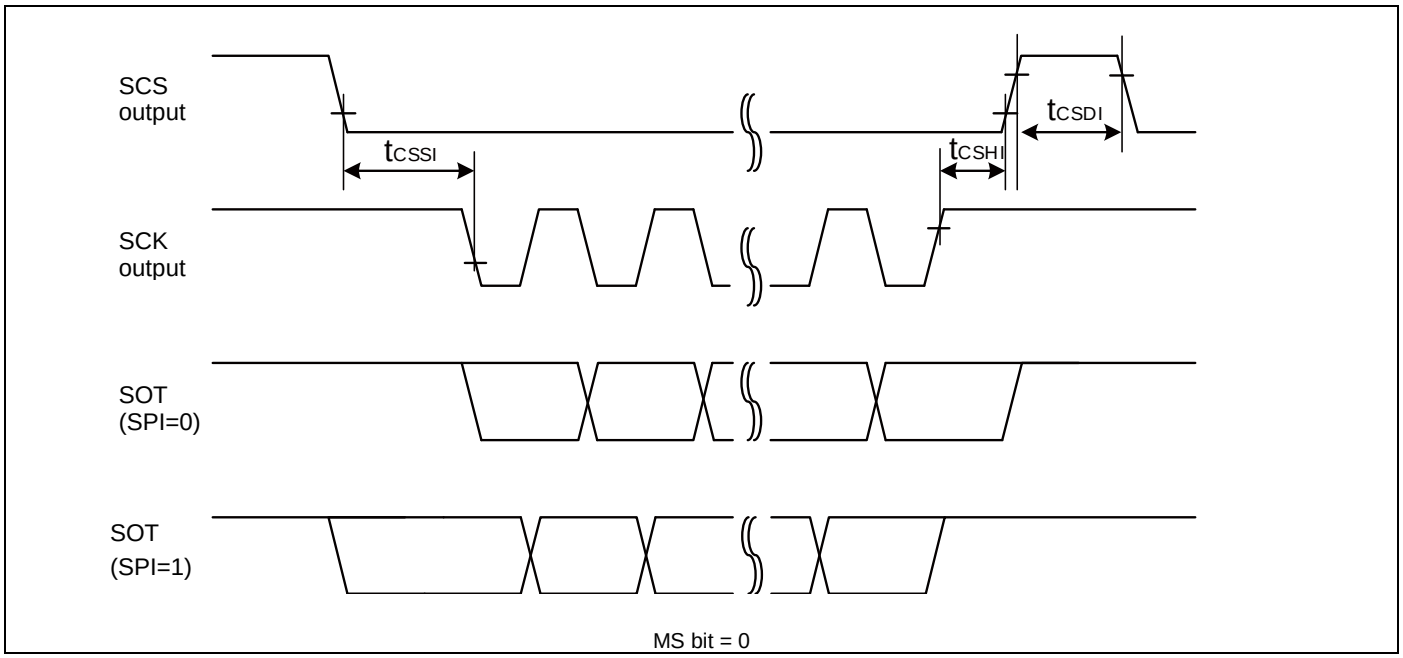
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

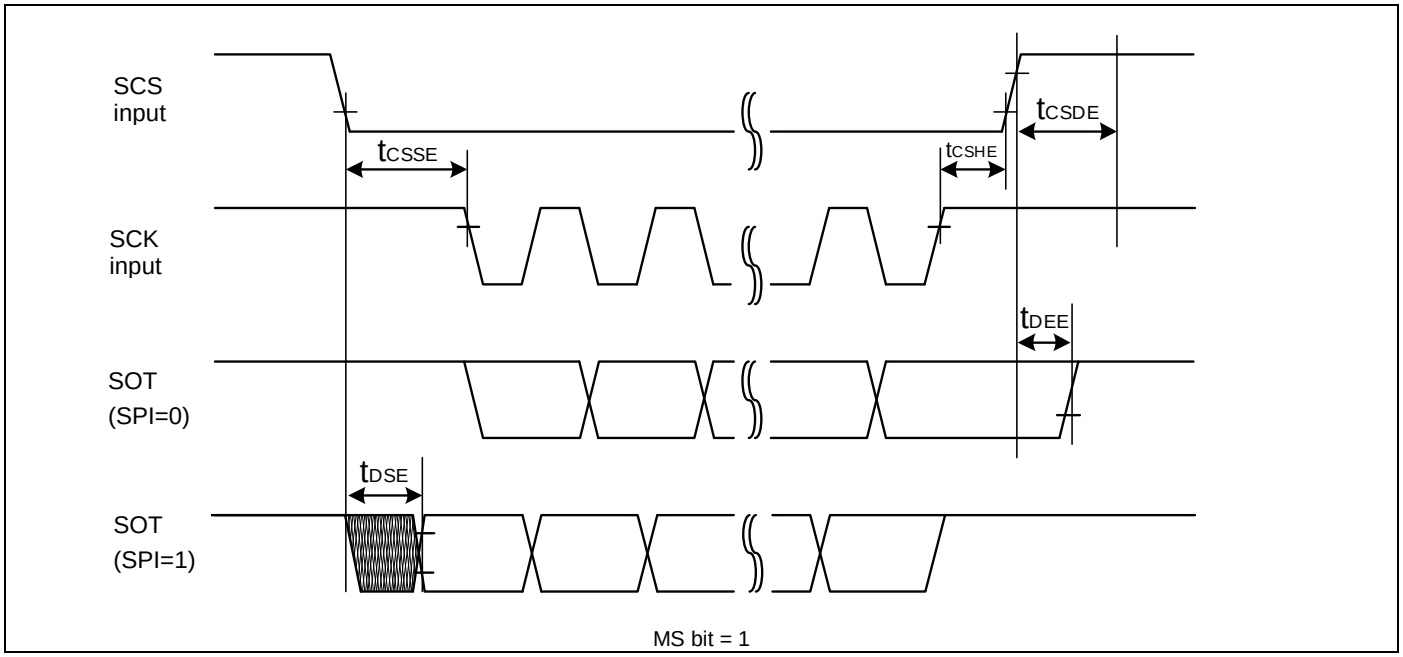
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

***Notes:***

- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM4 Family Peripheral Manual".*
- *When the external load capacitance $C_L$ = 30pF.*




MS bit = 0




MS bit = 1

### When using high-speed synchronous serial chip select (SCINV = 1, CSLVL = 1)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCS↓→SCK↑setup time | $t_{CSSI}$ | Internal shift clock operation | (*1)-20 | (*1)+0 | (*1)-20 | (*1)+0 | ns |
| SCK↓→SCS↑ hold time | $t_{CSHI}$ | | (*2)+0 | (*2)+20 | (*2)+0 | (*2)+20 | ns |
| SCS deselect time | $t_{CSDI}$ | | (*3)-20 +5$t_{CYCP}$ | (*3)+20 +5$t_{CYCP}$ | (*3)-20 +5$t_{CYCP}$ | (*3)+20 +5$t_{CYCP}$ | ns |
| SCS↓→SCK↑setup time | $t_{CSSE}$ | External shift clock operation | 3$t_{CYCP}$+15 | - | 3$t_{CYCP}$+15 | - | ns |
| SCK↓→SCS↑ hold time | $t_{CSHE}$ | | 0 | - | 0 | - | ns |
| SCS deselect time | $t_{CSDE}$ | | 3$t_{CYCP}$+15 | - | 3$t_{CYCP}$+15 | - | ns |
| SCS↓→SOT delay time | $t_{DSE}$ | | - | 25 | - | 25 | ns |
| SCS↑→SOT delay time | $t_{DEE}$ | | 0 | - | 0 | - | ns |

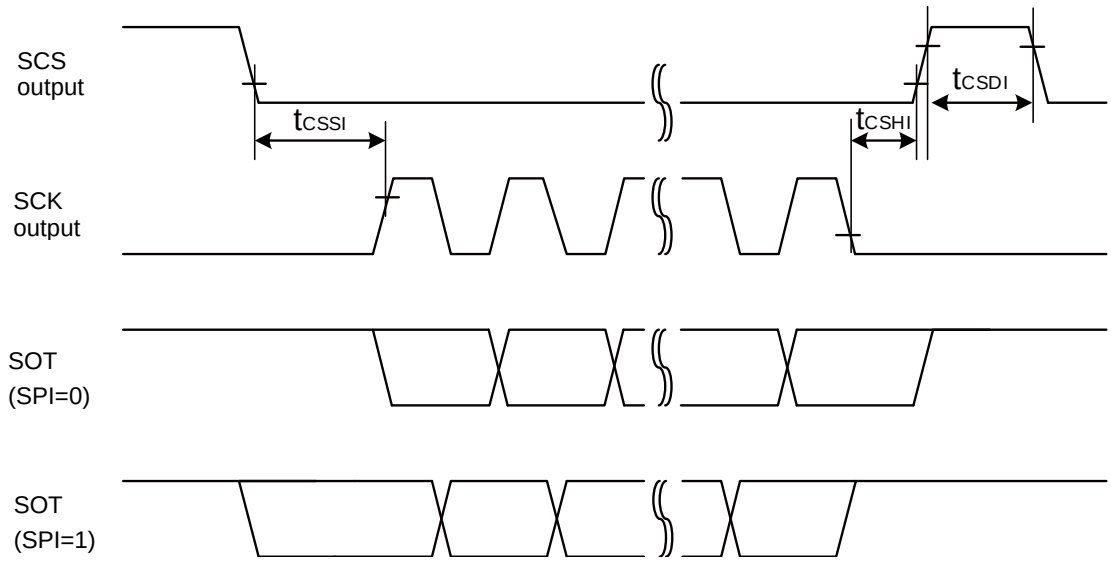
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

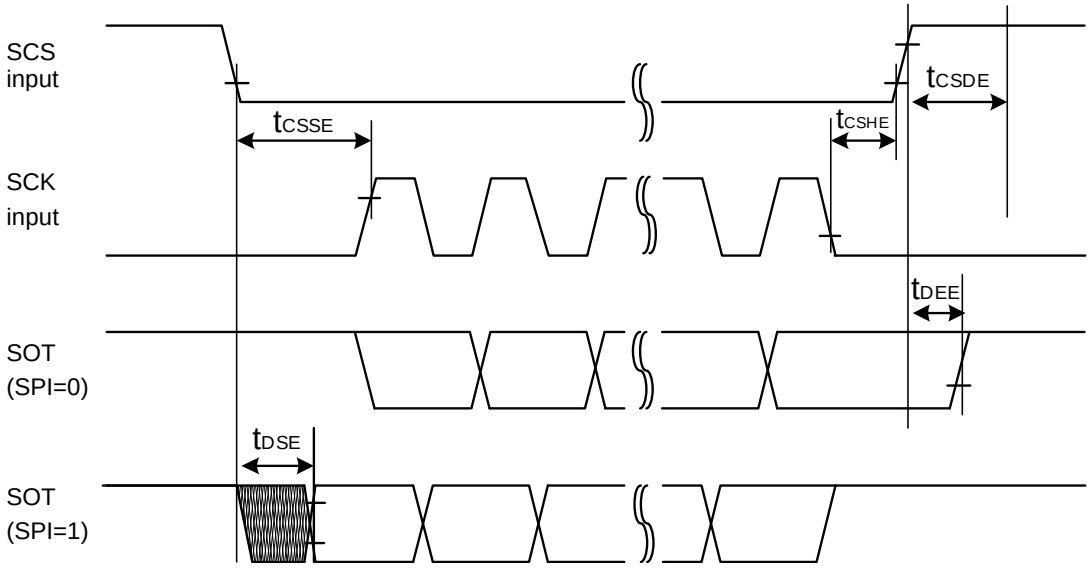
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

***Notes:***

- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM4 Family Peripheral Manual".*
- *When the external load capacitance $C_L$ = 30pF.*




MS bit = 0




MS bit = 1

### When using high-speed synchronous serial chip select (SCINV = 0, CSLVL = 0)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCS↑→SCK↓setup time | $t_{CSSI}$ | Internal shift clock operation | (*1)-20 | (*1)+0 | (*1)-20 | (*1)+0 | ns |
| SCK↑→SCS↓ hold time | $t_{CSHI}$ | | (*2)+0 | (*2)+20 | (*2)+0 | (*2)+20 | ns |
| SCS deselect time | $t_{CSDI}$ | | (*3)-20 +5$t_{CYCP}$ | (*3)+20 +5$t_{CYCP}$ | (*3)-20 +5$t_{CYCP}$ | (*3)+20 +5$t_{CYCP}$ | ns |
| SCS↑→SCK↓setup time | $t_{CSSE}$ | External shift clock operation | 3$t_{CYCP}$+15 | - | 3$t_{CYCP}$+15 | - | ns |
| SCK↑→SCS↓ hold time | $t_{CSHE}$ | | 0 | - | 0 | - | ns |
| SCS deselect time | $t_{CSDE}$ | | 3$t_{CYCP}$+15 | - | 3$t_{CYCP}$+15 | - | ns |
| SCS↑→SOT delay time | $t_{DSE}$ | | - | 25 | - | 25 | ns |
| SCS↓→SOT delay time | $t_{DEE}$ | | 0 | - | 0 | - | ns |

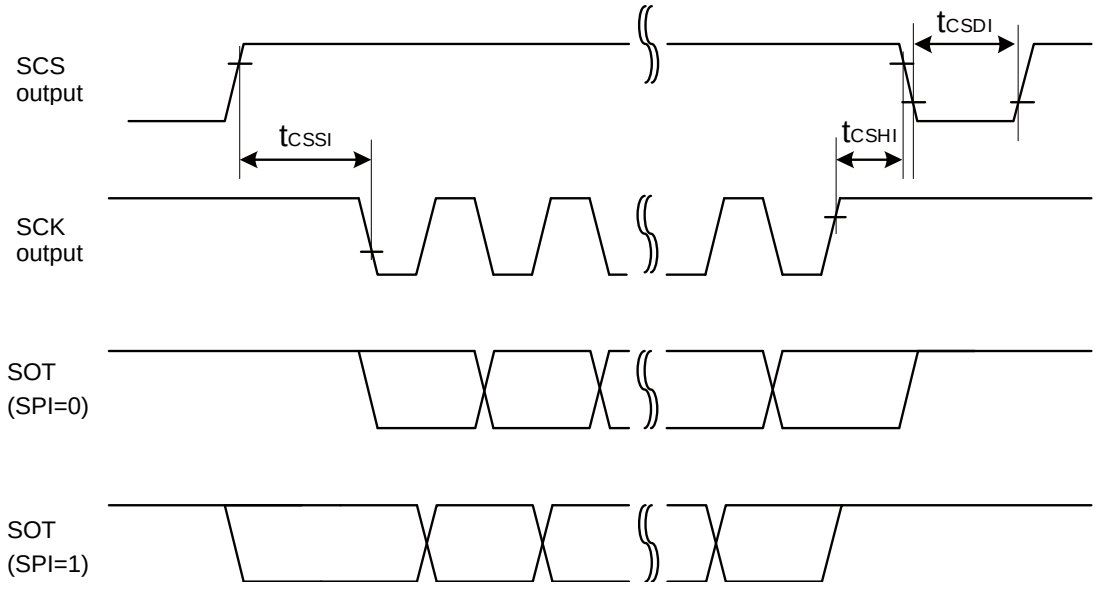
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

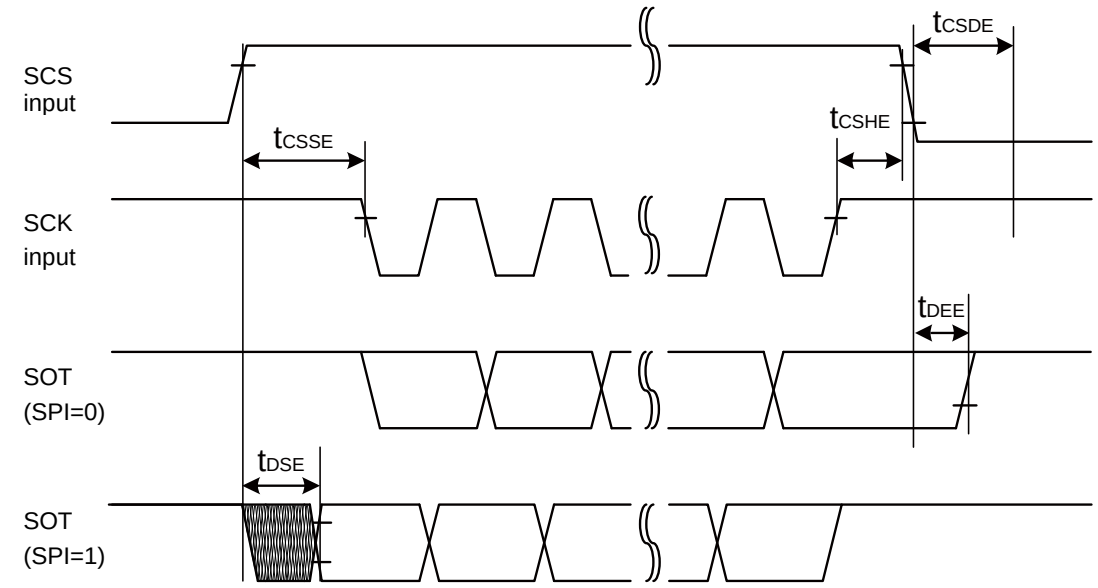
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

***Notes:***

- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM4 Family Peripheral Manual".*
- *When the external load capacitance $C_L$ = 30pF.*




MS bit = 0




MS bit = 1

### When using high-speed synchronous serial chip select (SCINV = 1, CSLVL = 0)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCS↑→SCK↑setup time | $t_{CSSI}$ | Internal shift clock operation | (*1)-20 | (*1)+0 | (*1)-20 | (*1)+0 | ns |
| SCK↓→SCS↓ hold time | $t_{CSHI}$ | | (*2)+0 | (*2)+20 | (*2)+0 | (*2)+20 | ns |
| SCS deselect time | $t_{CSDI}$ | | (*3)-20 +5$t_{CYCP}$ | (*3)+20 +5$t_{CYCP}$ | (*3)-20 +5$t_{CYCP}$ | (*3)+20 +5$t_{CYCP}$ | ns |
| SCS↑→SCK↑setup time | $t_{CSSE}$ | External shift clock operation | 3$t_{CYCP}$+15 | - | 3$t_{CYCP}$+15 | - | ns |
| SCK↓→SCS↓ hold time | $t_{CSHE}$ | | 0 | - | 0 | - | ns |
| SCS deselect time | $t_{CSDE}$ | | 3$t_{CYCP}$+15 | - | 3$t_{CYCP}$+15 | - | ns |
| SCS↑→SOT delay time | $t_{DSE}$ | | - | 25 | - | 25 | ns |
| SCS↓→SOT delay time | $t_{DEE}$ | | 0 | - | 0 | - | ns |

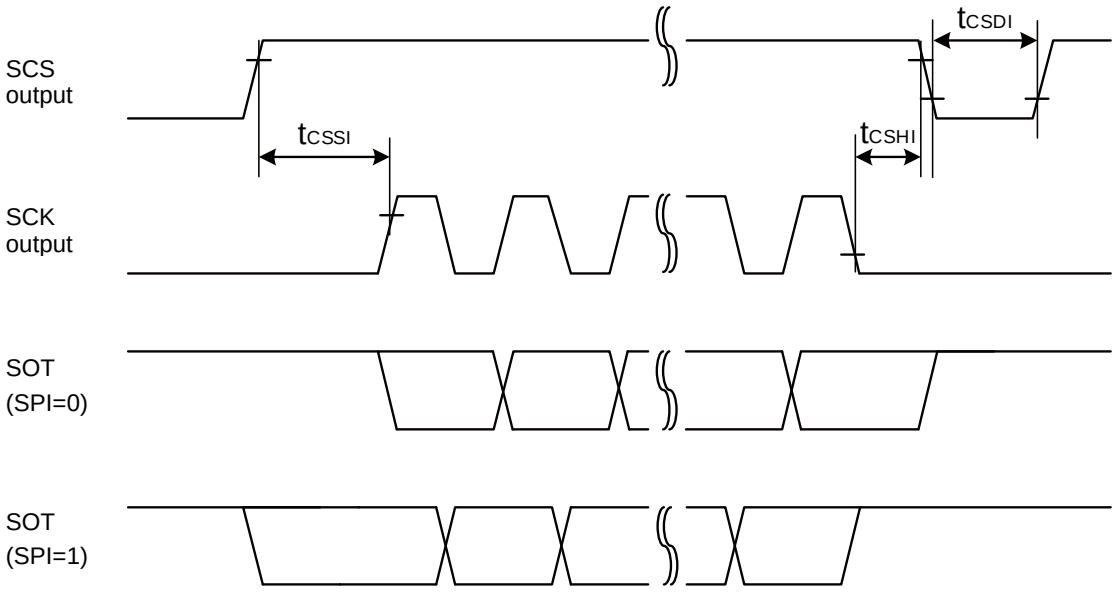
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

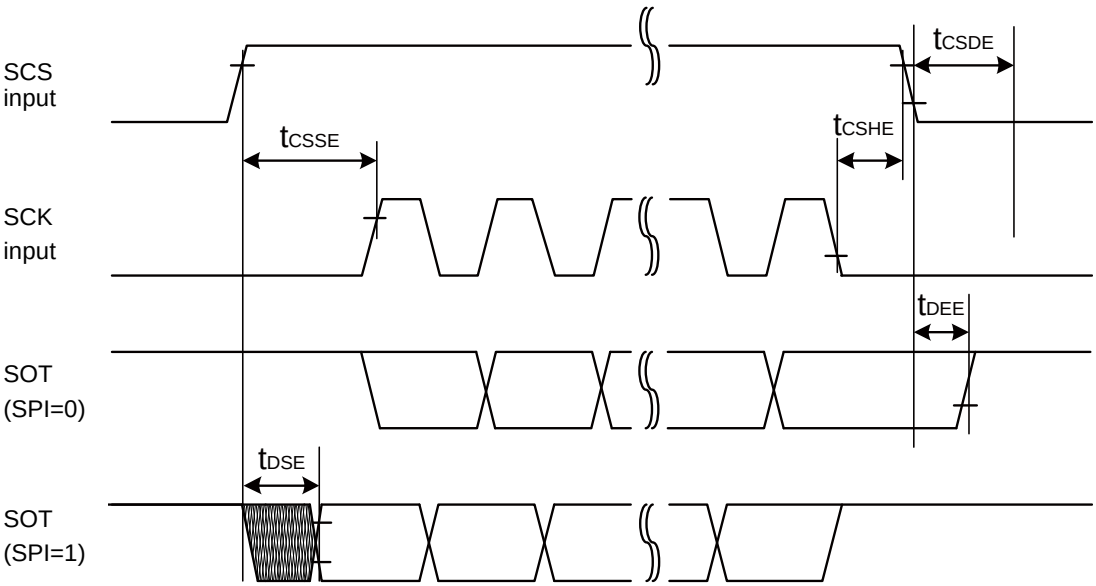
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

***Notes:***

- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.*
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM4 Family Peripheral Manual".*
- *When the external load capacitance $C_L$ = 30pF.*




MS bit = 0

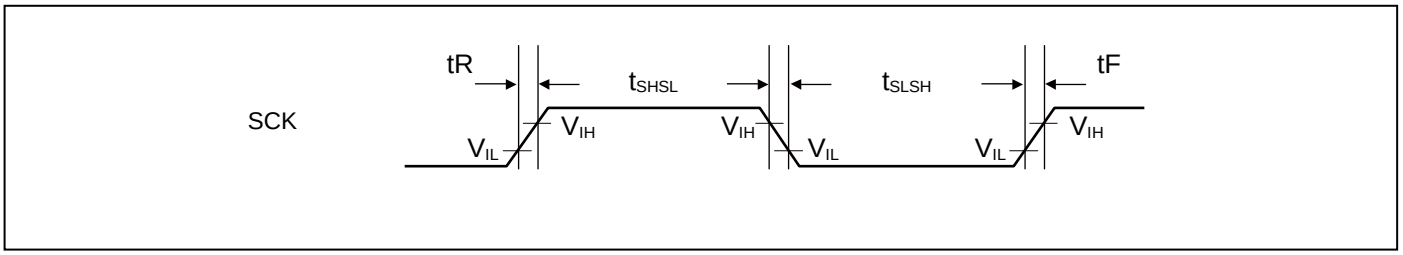



MS bit = 1

### External clock (EXT = 1) : when in asynchronous mode only

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Serial clock "L" pulse width | $t_{SLSH}$ | $C_L$ = 30pF | $t_{CYCP}$ + 10 | - | ns | |
| Serial clock "H" pulse width | $t_{SHSL}$ | | $t_{CYCP}$ + 10 | - | ns | |
| SCK falling time | tF | | - | 5 | ns | |
| SCK rising time | tR | | - | 5 | ns | |



### 12.4.12 External Input Timing

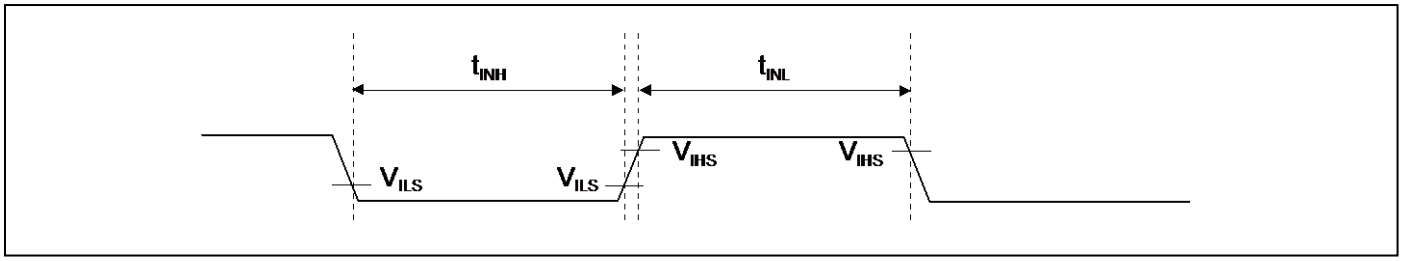
($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{INH}$, $t_{INL}$ | ADTG | - | $2t_{CYCP}$*1 | - | ns | A/D converter trigger input |
| | | FRCKx | | | | | Free-run timer input clock |
| | | ICxx | | | | | Input capture |
| | | DTTIxX | - | $2t_{CYCP}$*1 | - | ns | Waveform generator |
| | | INT00 to INT31, NMIX | - | $2t_{CYCP}$ + 100*1 | - | ns | External interrupt, NMI |
| | | | | 500*2 | - | ns | |
| | | WKUPx | - | 500*3 | - | ns | Deep standby wake up |

*1: $t_{CYCP}$ indicates the APB bus clock cycle time except stop when in STOP mode, in timer mode. About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see “Block Diagram” in this data sheet.

*2: When in STOP mode, in timer mode.

*3: When in deep standby RTC mode, in deep standby STOP mode.

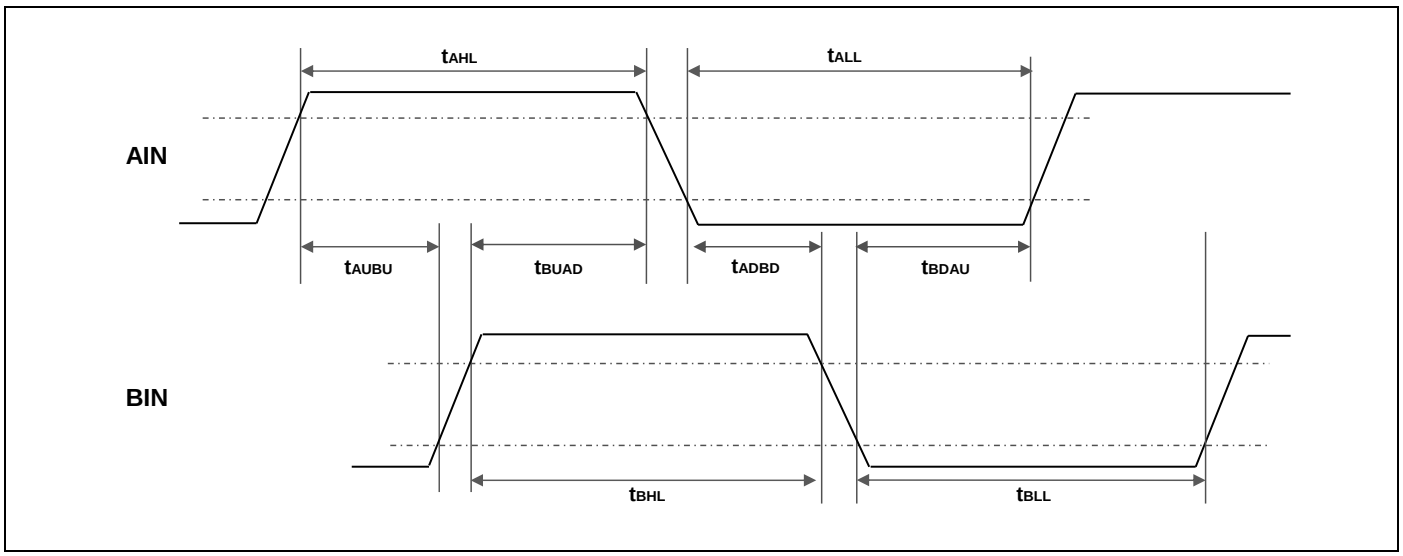


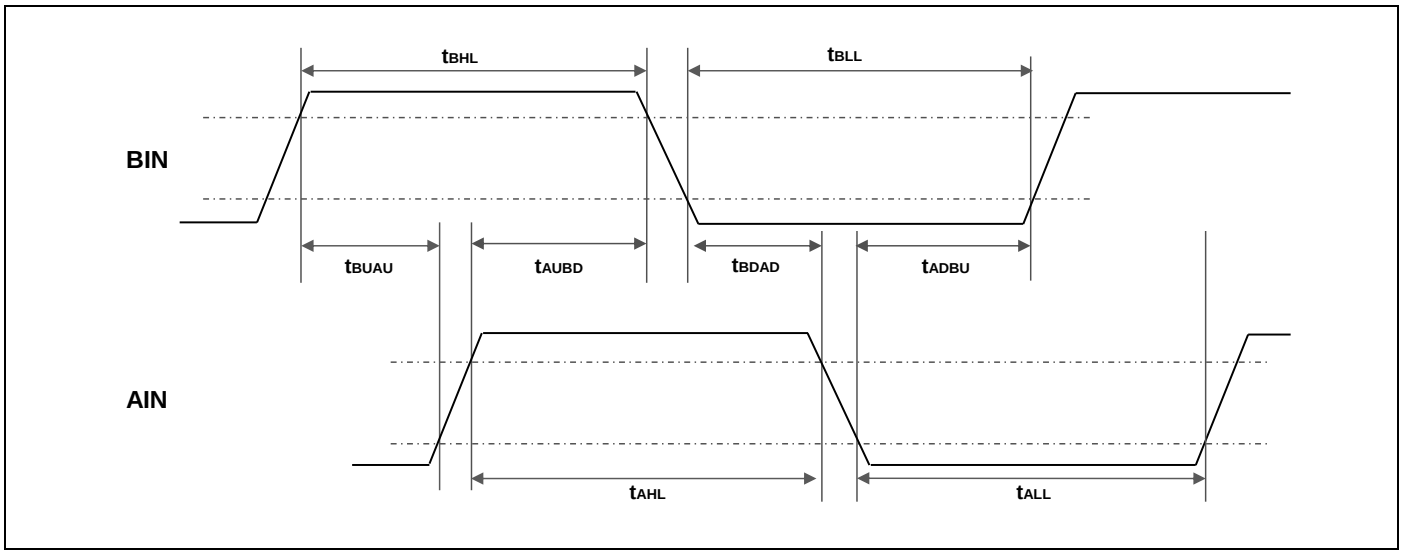
### 12.4.13 Quadrature Position/Revolution Counter Timing

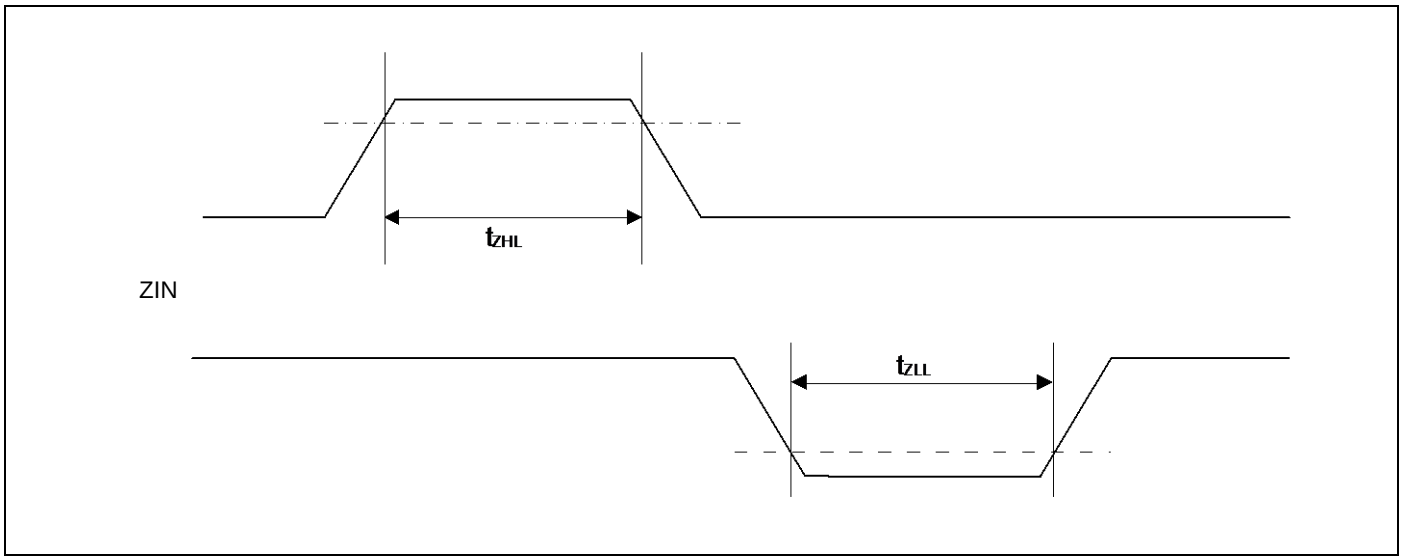
($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

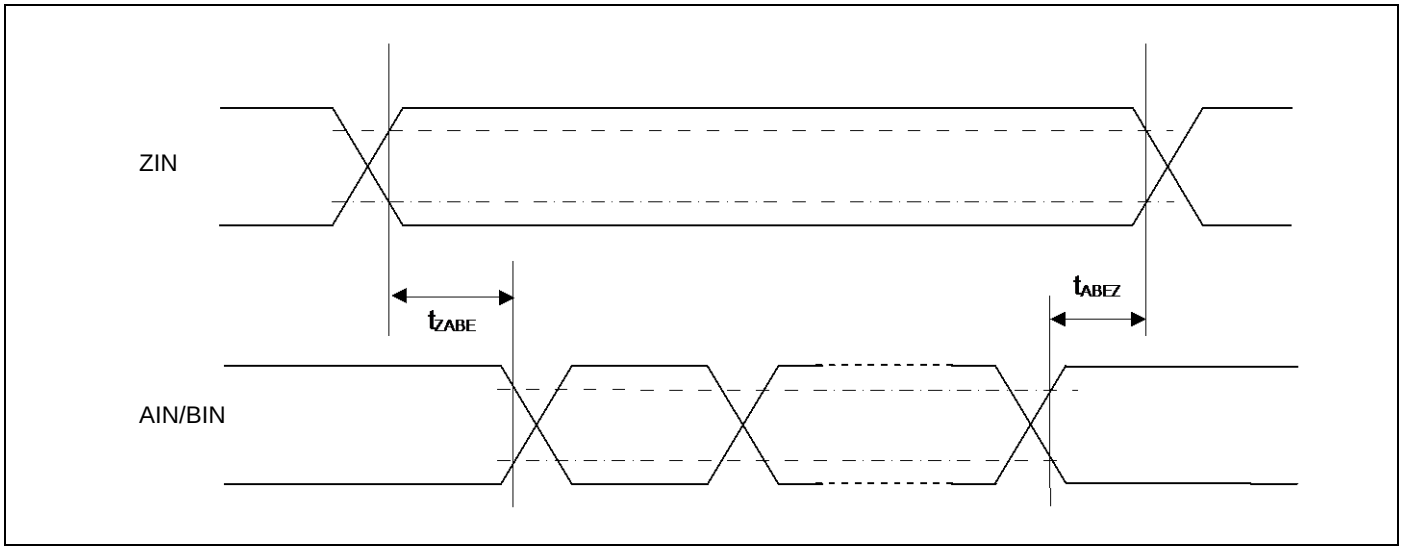
| Parameter | Symbol | Conditions | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| AIN pin "H" width | $t_{AHL}$ | - | $2t_{CYCP}$* | - | ns |
| AIN pin "L" width | $t_{ALL}$ | - | | | |
| BIN pin "H" width | $t_{BHL}$ | - | | | |
| BIN pin "L" width | $t_{BLL}$ | - | | | |
| BIN rising time from AIN pin "H" level | $t_{AUBU}$ | PC_Mode2 or PC_Mode3 | | | |
| AIN falling time from BIN pin "H" level | $t_{BUAD}$ | PC_Mode2 or PC_Mode3 | | | |
| BIN falling time from AIN pin "L" level | $t_{ADBD}$ | PC_Mode2 or PC_Mode3 | | | |
| AIN rising time from BIN pin "L" level | $t_{BDAU}$ | PC_Mode2 or PC_Mode3 | | | |
| AIN rising time from BIN pin "H" level | $t_{BUAU}$ | PC_Mode2 or PC_Mode3 | | | |
| BIN falling time from AIN pin "H" level | $t_{AUBD}$ | PC_Mode2 or PC_Mode3 | | | |
| AIN falling time from BIN pin "L" level | $t_{BDAD}$ | PC_Mode2 or PC_Mode3 | | | |
| BIN rising time from AIN pin "L" level | $t_{ADBU}$ | PC_Mode2 or PC_Mode3 | | | |
| ZIN pin "H" width | $t_{ZHL}$ | QCR:CGSC = "0" | | | |
| ZIN pin "L" width | $t_{ZLL}$ | QCR:CGSC = "0" | | | |
| AIN/BIN rising and falling time from determined ZIN level | $t_{ZABE}$ | QCR:CGSC = "1" | | | |
| Determined ZIN level from AIN/BIN rising and falling time | $t_{ABEZ}$ | QCR:CGSC = "1" | | | |

*: $t_{CYCP}$ indicates the APB bus clock cycle time except stop when in STOP mode, in timer mode.
About the APB bus number which Quadrature Position/Revolution Counter is connected to, see “Block Diagram” in this data sheet.




tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

### *12.4.14 I²C Timing*

#### Standard-mode, Fast-mode

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Conditions | Standard-mode | | Fast-mode | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | | |
| SCL clock frequency | $F_{SCL}$ | $C_L$ = 30pF, R = ($V_p/I_{OL}$)*1 | 0 | 100 | 0 | 400 | kHz | |
| (Repeated) START condition hold time SDA ↓ → SCL ↓ | $t_{HDSTA}$ | | 4.0 | - | 0.6 | - | µs | |
| SCL clock "L" width | $t_{LOW}$ | | 4.7 | - | 1.3 | - | µs | |
| SCL clock "H" width | $t_{HIGH}$ | | 4.0 | - | 0.6 | - | µs | |
| (Repeated) START condition setup time SCL ↑ → SDA ↓ | $t_{SUSTA}$ | | 4.7 | - | 0.6 | - | µs | |
| Data hold time SCL ↓ → SDA ↓ ↑ | $t_{HDDAT}$ | | 0 | 3.45*2 | 0 | 0.9*3 | µs | |
| Data setup time SDA ↓ ↑ → SCL ↑ | $t_{SUDAT}$ | | 250 | - | 100 | - | ns | |
| STOP condition setup time SCL ↑ → SDA ↑ | $t_{SUSTO}$ | | 4.0 | - | 0.6 | - | µs | |
| Bus free time between "STOP condition" and "START condition" | $t_{BUF}$ | | 4.7 | - | 1.3 | - | µs | |
| Noise filter | $t_{SP}$ | 2MHz ≤ $t_{CYCP}$<40MHz | $2t_{CYCP}$*4 | - | $2t_{CYCP}$*4 | - | ns | *5 |
| | | 40MHz ≤ $t_{CYCP}$<60MHz | $4t_{CYCP}$*4 | - | $4t_{CYCP}$*4 | - | ns | |
| | | 60MHz ≤ $t_{CYCP}$<80MHz | $6t_{CYCP}$*4 | - | $6t_{CYCP}$*4 | - | ns | |
| | | 80MHz ≤ $t_{CYCP}$<100MHz | $8t_{CYCP}$*4 | - | $8t_{CYCP}$*4 | - | ns | |
| | | 100MHz ≤ $t_{CYCP}$<120MHz | $10t_{CYCP}$*4 | - | $10t_{CYCP}$*4 | - | ns | |
| | | 120MHz ≤ $t_{CYCP}$<140MHz | $12t_{CYCP}$*4 | - | $12t_{CYCP}$*4 | - | ns | |
| | | 140MHz ≤ $t_{CYCP}$<160MHz | $14t_{CYCP}$*4 | - | $14t_{CYCP}$*4 | - | ns | |
| | | 160MHz ≤ $t_{CYCP}$<180MHz | $16t_{CYCP}$*4 | - | $16t_{CYCP}$*4 | - | ns | |

*1: R and $C_L$ represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and $I_{OL}$ indicates $V_{OL}$ guaranteed current.

*2: The maximum $t_{HDDAT}$ must satisfy that it does not extend at least "L" period ($t_{LOW}$) of device's SCL signal.

*3: A Fast-mode $I^2C$ bus device can be used on a Standard-mode $I^2C$ bus system as long as the device satisfies the requirement of "$t_{SUDAT}$ ≥ 250 ns".

*4: $t_{CYCP}$ is the APB bus clock cycle time.
About the APB bus number that $I^2C$ is connected to, see "Block Diagram" in this data sheet.

*5: The noise filter time can be changed by register settings.
Change the number of the noise filter steps according to APB bus clock frequency.

### Fast-mode Plus (Fm+)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Conditions | Fast-mode Plus (Fm+)*6 | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| SCL clock frequency | $F_{SCL}$ | $C_L$ = 30pF, R = (Vp/$I_{OL}$)*1 | 0 | 1000 | kHz | |
| (Repeated) START condition hold time SDA ↓ → SCL ↓ | $t_{HDSTA}$ | | 0.26 | - | µs | |
| SCL clock "L" width | $t_{LOW}$ | | 0.5 | - | µs | |
| SCL clock "H" width | $t_{HIGH}$ | | 0.26 | - | µs | |
| SCL clock frequency | $t_{SUSTA}$ | | 0.26 | - | µs | |
| (Repeated) START condition hold time SDA ↓ → SCL ↓ | $t_{HDDAT}$ | | 0 | 0.45*2, *3 | µs | |
| Data setup time SDA ↓ ↑ → SCL ↑ | $t_{SUDAT}$ | | 50 | - | ns | |
| STOP condition setup time SCL ↑ → SDA ↑ | $t_{SUSTO}$ | | 0.26 | - | µs | |
| Bus free time between "STOP condition" and "START condition" | $t_{BUF}$ | | 0.5 | - | µs | |
| Noise filter | $t_{SP}$ | 60MHz ≤ $t_{CYCP}$<80MHz | 6 $t_{CYCP}$*4 | - | ns | *5 |
| | | 80MHz ≤ $t_{CYCP}$<100MHz | 8 $t_{CYCP}$*4 | - | ns | |
| | | 100MHz ≤ $t_{CYCP}$<120MHz | 10 $t_{CYCP}$*4 | - | ns | |
| | | 120MHz ≤ $t_{CYCP}$<140MHz | 12 $t_{CYCP}$*4 | - | ns | |
| | | 140MHz ≤ $t_{CYCP}$<160MHz | 14 $t_{CYCP}$*4 | - | ns | |
| | | 160MHz ≤ $t_{CYCP}$<180MHz | 16 $t_{CYCP}$*4 | - | ns | |

*1: R and $C_L$ represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and $I_{OL}$ indicates $V_{OL}$ guaranteed current.

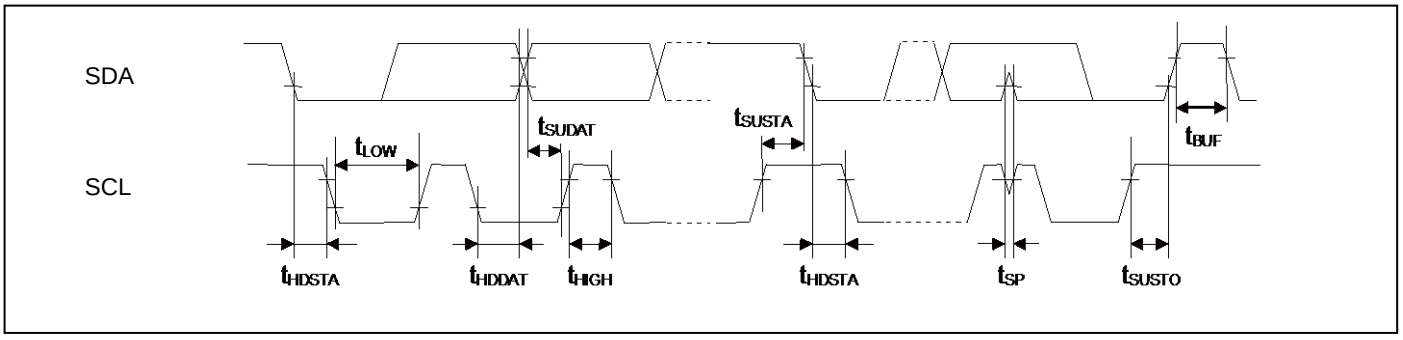
*2: The maximum $t_{HDDAT}$ must satisfy that it does not extend at least "L" period ($t_{LOW}$) of device's SCL signal.

*3: A Fast-mode $I^2C$ bus device can be used on a Standard-mode $I^2C$ bus system as long as the device satisfies the requirement of "$t_{SUDAT}$ ≥ 250 ns".

*4: $t_{CYCP}$ is the APB bus clock cycle time.
About the APB bus number that $I^2C$ is connected to, see “Block Diagram” in this data sheet.
To use Fast-mode Plus (Fm+), set the peripheral bus clock at 64 MHz or more.

*5: The noise filter time can be changed by register settings.
Change the number of the noise filter steps according to APB bus clock frequency.

*6: When using Fast-mode Plus (Fm+), set the I/O pin to the mode corresponding to $I^2C$ Fm+ in the EPFR register.
See “Chapter: I/O Port” in “FM4 Family Peripheral Manual” for the details.



### *12.4.15 SD Card Interface Timing*

#### Default-Speed Mode

■Clock CLK (All values are referred to $V_{IH}$ and $V_{IL}$)

($V_{CC}$ = 2.7V to 3.6V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Remarks |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Clock frequency Data Transfer Mode | $f_{PP}$ | S_CLK | $C_{CARD}$ ≤ 10pF (1card) | 0 | 16 | MHz |
| Clock frequency Identification Mode | $f_{OD}$ | S_CLK | | 0*/100 | 400 | kHz |
| Clock low time | $t_{WL}$ | S_CLK | | 10 | - | ns |
| Clock high time | $t_{WH}$ | S_CLK | | 10 | - | ns |
| Clock rising time | $t_{TLH}$ | S_CLK | | - | 10 | ns |
| Clock falling time | $t_{THL}$ | S_CLK | | - | 10 | ns |

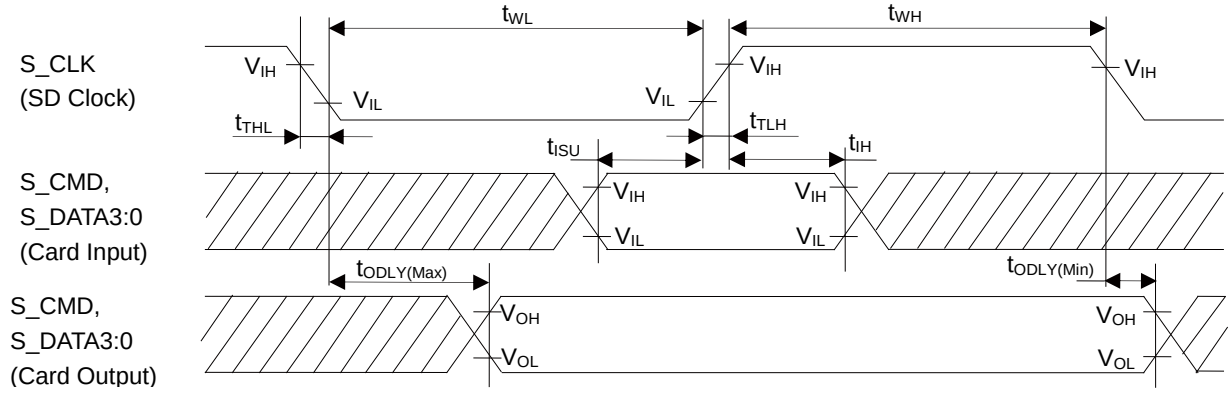
*: 0Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

■Card Inputs CMD, DAT (referenced to Clock CLK)

| Parameter | Symbol | Pin name | Conditions | Value | | Remarks |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Input set-up time | $t_{ISU}$ | S_CMD, S_DATA3:0 | $C_{CARD}$ ≤ 10pF (1card) | 5 | - | ns |
| Input hold time | $t_{IH}$ | S_CMD, S_DATA3:0 | | 5 | - | ns |

■Card Outputs CMD, DAT (referenced to Clock CLK)

| Parameter | Symbol | Pin name | Conditions | Value | | Remarks |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Output Delay time during Data Transfer Mode | $t_{ODLY}$ | S_CMD, S_DATA3:0 | $C_{CARD}$ ≤ 40pF (1card) | 0 | 22 | ns |
| Output Delay time durinn Identification Mode | $t_{ODLY}$ | S_CMD, S_DATA3:0 | | 0 | 50 | ns |




Defalt-Speed Mode

***Note:***

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*

### High-Speed Mode

■Clock CLK (All values are referred to $V_{IH}$ and $V_{IL}$)

($V_{CC}$ = 2.7V to 3.6V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Remarks |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Clock frequency Data Transfer Mode | $f_{PP}$ | S_CLK | $C_{CARD}$ ≤ 10pF (1card) | 0 | 32 | MHz |
| Clock low time | $t_{WL}$ | S_CLK | | 7 | - | ns |
| Clock high time | $t_{WH}$ | S_CLK | | 7 | - | ns |
| Clock rising time | $t_{TLH}$ | S_CLK | | - | 3 | ns |
| Clock falling time | $t_{THL}$ | S_CLK | | - | 3 | ns |

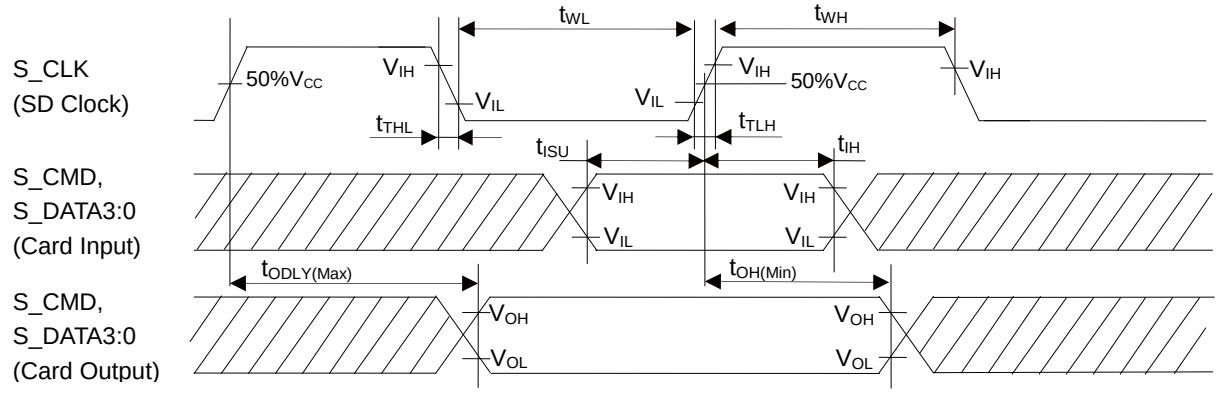
■Card Inputs CMD, DAT (referenced to Clock CLK)

| Parameter | Symbol | Pin name | Conditions | Value | | Remarks |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Input set-up time | $t_{ISU}$ | S_CMD, S_DATA3:0 | $C_{CARD}$ ≤ 10pF (1card) | 8 | - | ns |
| Input hold time | $t_{IH}$ | S_CMD, S_DATA3:0 | | 2 | - | ns |

■Card Outputs CMD, DAT (referenced to Clock CLK)

| Parameter | Symbol | Pin name | Conditions | Value | | Remarks |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Output Delay time during Data Transfer Mode | $t_{ODLY}$ | S_CMD, S_DATA3:0 | $C_L$ ≤ 40pF (1card) | - | 22 | ns |
| Output Hold time | $t_{OH}$ | S_CMD, S_DATA3:0 | $C_L$ ≥ 15pF (1card) | 2.5 | - | ns |
| Total System capacitance for each line* | $C_L$ | - | 1card | - | 40 | pF |

*: In order to satisfy severe timing, host shall drive only one card.




High-Speed Mode

***Notes:***

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *In high-speed mode, set the Clock frequency ($f_{PP}$) and the AHB Bus Clock frequency to the same values.*

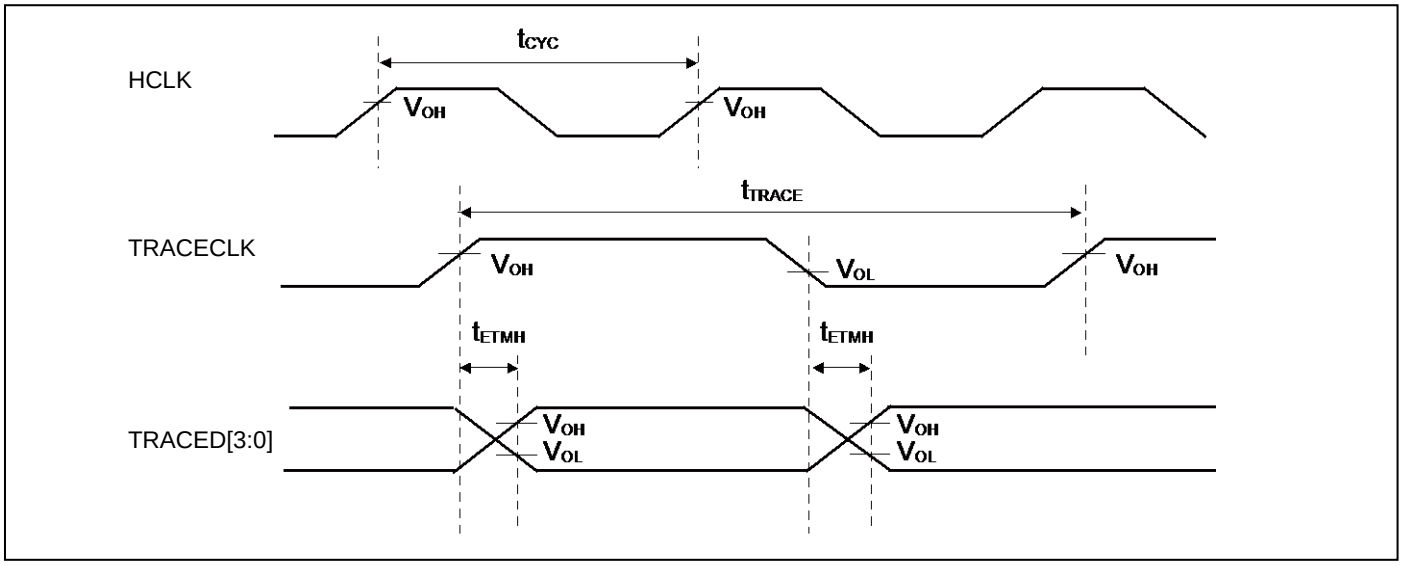
### 12.4.16 ETM Timing

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Data hold | $t_{ETMH}$ | TRACECLK, TRACED[3:0] | $V_{CC} \geq 4.5V$ | 2 | 9 | ns | |
| | | | $V_{CC} < 4.5V$ | 2 | 15 | | |
| TRACECLK frequency | 1/ $t_{TRACE}$ | TRACECLK | $V_{CC} \geq 4.5V$ | - | 50 | MHz | |
| | | | $V_{CC} < 4.5V$ | - | 32 | MHz | |
| TRACECLK clock cycle | $t_{TRACE}$ | | $V_{CC} \geq 4.5V$ | 20 | - | ns | |
| | | | $V_{CC} < 4.5V$ | 31.25 | - | ns | |

***Note:***

- *When the external load capacitance $C_L$ = 30pF.*



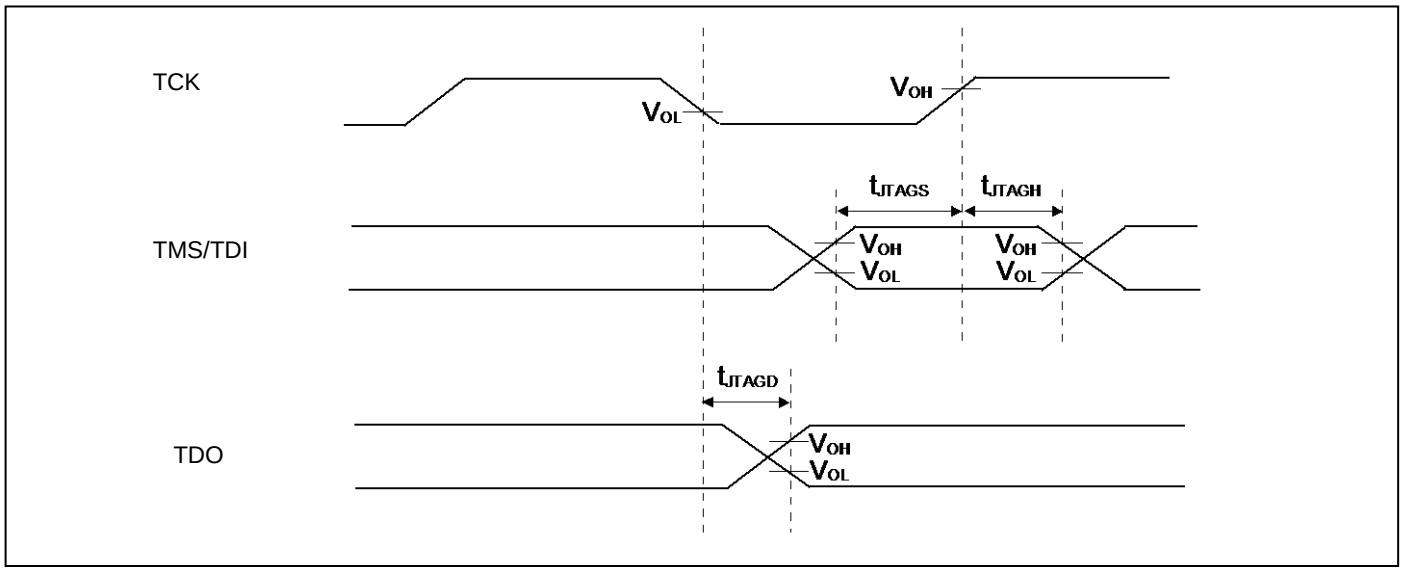
### 12.4.17 JTAG Timing

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| TMS, TDI setup time | $t_{JTAGS}$ | TCK, TMS, TDI | $V_{CC} \geq 4.5V$ | 15 | - | ns | |
| | | | $V_{CC} < 4.5V$ | | | | |
| TMS, TDI hold time | $t_{JTAGH}$ | TCK, TMS, TDI | $V_{CC} \geq 4.5V$ | 15 | - | ns | |
| | | | $V_{CC} < 4.5V$ | | | | |
| TDO delay time | $t_{JTAGD}$ | TCK, TDO | $V_{CC} \geq 4.5V$ | - | 25 | ns | |
| | | | $V_{CC} < 4.5V$ | - | 45 | | |

***Note:***

- *When the external load capacitance $C_L$ = 30pF.*



## 12.5 12-bit A/D Converter

### Electrical Characteristics for the A/D Converter

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = AVRL = 0V)

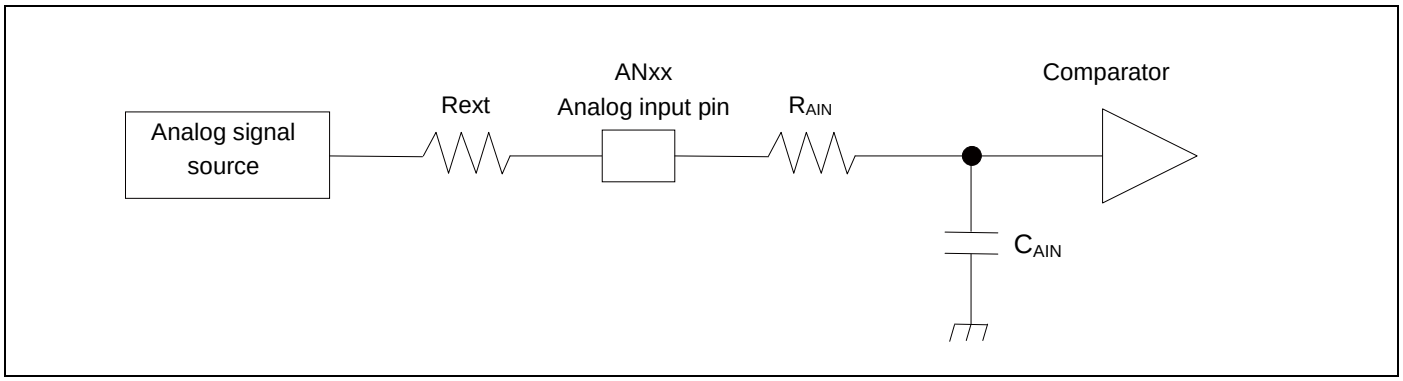
| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | - | - | - | - | 12 | bit | |
| Integral Nonlinearity | - | - | - 4.5 | - | + 4.5 | LSB | AVRH = 2.7V to 5.5V |
| Differential Nonlinearity | - | - | -2.5 | - | + 2.5 | LSB | |
| Zero transition voltage | $V_{ZT}$ | ANxx | - 15 | - | + 15 | mV | |
| Full-scale transition voltage | $V_{FST}$ | ANxx | AVRH - 15 | - | AVRH + 15 | mV | |
| Conversion time | - | - | 0.5*1 | - | - | µs | $AV_{CC}$ ≥ 4.5V |
| Sampling time*2 | Ts | - | 0.15 | - | 10 | µs | $AV_{CC}$ ≥ 4.5V |
| | | | 0.3 | - | | | $AV_{CC}$ < 4.5V |
| Compare clock cycle*3 | Tcck | - | 25 | - | 1000 | ns | $AV_{CC}$ ≥ 4.5V |
| | | | 50 | - | 1000 | | $AV_{CC}$ < 4.5V |
| State transition time to operation permission | Tstt | - | - | - | 1.0 | µs | |
| Power supply current (analog + digital) | - | AVCC | - | 0.69 | 0.92 | mA | A/D 1unit operation |
| | | | - | 1.0 | 18 | µA | When A/D stop |
| Reference power supply current (AVRH) | - | AVRH | - | 1.1 | 1.97 | mA | A/D 1unit operation AVRH = 5.5V |
| | | | | 0.3 | 6.3 | µA | When A/D stop |
| Analog input capacity | $C_{AIN}$ | - | - | - | 12.05 | pF | |
| Analog input resistance | $R_{AIN}$ | - | - | - | 1.2 | kΩ | $AV_{CC}$ ≥ 4.5V |
| | | | | | 1.8 | | $AV_{CC}$ < 4.5V |
| Interchannel disparity | - | - | - | - | 4 | LSB | |
| Analog port input leak current | - | ANxx | - | - | 5 | µA | |
| Analog input voltage | - | ANxx | $AV_{SS}$ | - | AVRH | V | |
| Reference voltage | - | AVRH | 4.5 | - | $AV_{CC}$ | V | Tcck < 50ns |
| | | | 2.7 | - | $AV_{CC}$ | | Tcck ≥ 50ns |

*1: The conversion time is the value of sampling time (Ts) + compare time (Tc).
The condition of the minimum conversion time is when the value of sampling time: 150ns, the value of compare time: 350ns ($AV_{CC}$ ≥ 4.5V). Ensure that it satisfies the value of sampling time (Ts) and compare clock cycle (Tcck). For setting*4 of sampling time and compare clock cycle, see "Chapter: A/D Converter" in "FM4 Family PERIPHERAL MANUAL Analog Macro Part". The register setting of the A/D Converter is reflected by the peripheral clock timing. The sampling and compare clock are set at Base clock (HCLK).

*2: A necessary sampling time changes by external impedance. Ensure that it set the sampling time to satisfy (Equation 1).

*3: The compare time (Tc) is the value of (Equation 2).

*4: The register setting of the A/D Converter is reflected by the timing of the APB bus clock. The sampling clock and compare clock are set in base clock (HCLK). About the APB bus number which the A/D Converter is connected to, see “Block Diagram” in this data sheet.




(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

Ts: Sampling time

$R_{AIN}$: Input resistance of A/D = 1.2kΩ at 4.5V $\leq AV_{CC} \leq$ 5.5V

Input resistance of A/D = 1.8kΩ at 2.7V $\leq AV_{CC} \leq$ 4.5V

$C_{AIN}$: Input capacity of A/D = 12.05pF at 2.7V $\leq AV_{CC} \leq$ 5.5V

Rext: Output impedance of external circuit

(Equation 2) $Tc = Tcck \times 14$

Tc: Compare time

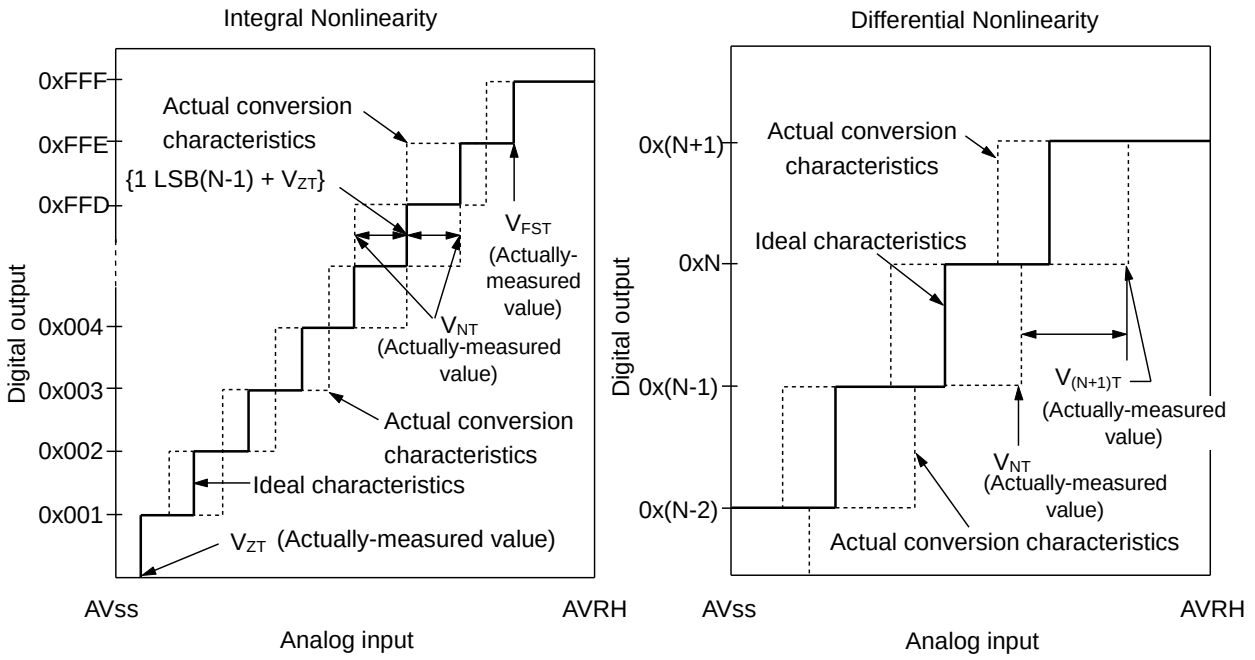
Tcck: Compare clock cycle

### Definition of 12-bit A/D Converter Terms

■Resolution: Analog variation that is recognized by an A/D converter.

■Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.

■Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.




$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.

$V_{ZT}$: Voltage at which the digital output changes from 0x000 to 0x001.

$V_{FST}$: Voltage at which the digital output changes from 0xFFE to 0xFFF.

$V_{NT}$: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

## 12.6 12-bit D/A Converter

### Electrical Characteristics for the D/A Converter

($V_{CC}$ = $AV_{CC}$ = 2.7Vto5.5V, $V_{SS}$ = $AV_{SS}$ = 0V)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | - | DAx | - | - | 12 | bit | |
| Conversion time | tc20 | | 0.56 | 0.69 | 0.81 | µs | Load 20pF |
| | tc100 | | 2.79 | 3.42 | 4.06 | µs | Load 100pF |
| Integral Nonlinearity* | INL | | - 16 | - | + 16 | LSB | |
| Differential Nonlinearity* | DNL | | - 0.98 | - | + 1.5 | LSB | |
| Output voltage offset | $V_{OFF}$ | | - | - | 10.0 | mV | When setting 0x000 |
| | | | - 20.0 | - | + 1.4 | mV | When setting 0xFFF |
| Analog output impedance | $R_O$ | | 3.10 | 3.80 | 4.50 | kΩ | D/A operation |
| | | | 2.0 | - | - | MΩ | When D/A stop |
| Power supply current* | IDDA | AVCC | 260 | 330 | 410 | µA | D/A 1unit operation $AV_{CC}$ = 3.3V |
| | | | 400 | 510 | 620 | µA | D/A 1unit operation $AV_{CC}$ = 5.0V |
| | IDSA | | - | - | 14 | µA | When D/A stop |

*: During no load

## 12.7 Low-Voltage Detection Characteristics

### *12.7.1 Low-Voltage Detection Reset*

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Detected voltage | VDL | - | 2.25 | 2.45 | 2.65 | V | When voltage drops |
| Released voltage | VDH | - | 2.30 | 2.50 | 2.70 | V | When voltage rises |

### *12.7.2 Interrupt of Low-Voltage Detection*

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Detected voltage | VDL | SVHI = 00111 | 2.58 | 2.8 | 3.02 | V | When voltage drops |
| Released voltage | VDH | | 2.67 | 2.9 | 3.13 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 00100 | 2.76 | 3.0 | 3.24 | V | When voltage drops |
| Released voltage | VDH | | 2.85 | 3.1 | 3.34 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01100 | 2.94 | 3.2 | 3.45 | V | When voltage drops |
| Released voltage | VDH | | 3.04 | 3.3 | 3.56 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01111 | 3.31 | 3.6 | 3.88 | V | When voltage drops |
| Released voltage | VDH | | 3.40 | 3.7 | 3.99 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01110 | 3.40 | 3.7 | 3.99 | V | When voltage drops |
| Released voltage | VDH | | 3.50 | 3.8 | 4.10 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01001 | 3.68 | 4.0 | 4.32 | V | When voltage drops |
| Released voltage | VDH | | 3.77 | 4.1 | 4.42 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01000 | 3.77 | 4.1 | 4.42 | V | When voltage drops |
| Released voltage | VDH | | 3.86 | 4.2 | 4.53 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 11000 | 3.86 | 4.2 | 4.53 | V | When voltage drops |
| Released voltage | VDH | | 3.96 | 4.3 | 4.64 | V | When voltage rises |
| LVD stabilization wait time | $T_{LVDW}$ | - | - | - | 4480×$t_{CYCP}$* | µs | |

*: $t_{CYCP}$ indicates the APB2 bus clock cycle time.

## 12.8 MainFlash Memory Write/Erase Characteristics

($V_{CC}$ = 2.7V to 5.5V)

| Parameter | | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Sector erase time | Large Sector | - | 0.7 | 3.7 | s | Includes write time prior to internal erase |
| | Small Sector | | 0.3 | 1.1 | | |
| Half word (16-bit) write time | Write cycles ≤ 100 times | - | 12 | 100 | µs | Not including system-level overhead time |
| | Write cycles > 100 times | | | 200 | | |
| Chip erase time | | - | 13.6 | 68 | s | Includes write time prior to internal erase |

### Write cycles and data hold time

| Erase/Write cycles (cycle) | Data hold time (year) |
|---|---|
| 1,000 | 20 * |
| 10,000 | 10 * |
| 100,000 | 5 * |

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C) .

## 12.9 WorkFlash Memory Write/Erase Characteristics

($V_{CC}$ = 2.7V to 5.5V)

| Parameter | Value | | | Unit | Remarks |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Sector erase time | - | 0.3 | 1.5 | s | Includes write time prior to internal erase |
| Half word (16-bit) write time | - | 20 | 200 | µs | Not including system-level overhead time |
| Chip erase time | - | 1.2 | 6 | s | Includes write time prior to internal erase |

### Write cycles and data hold time

| Erase/Write cycles (cycle) | Data hold time (year) |
|---|---|
| 1,000 | 20 * |
| 10,000 | 10 * |
| 100,000 | 5 * |

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C) .

## 12.10 Standby Recovery Time

### *12.10.1 Recovery cause: Interrupt/WKUP*

The time from recovery cause reception of the internal circuit to the program operation start is shown.

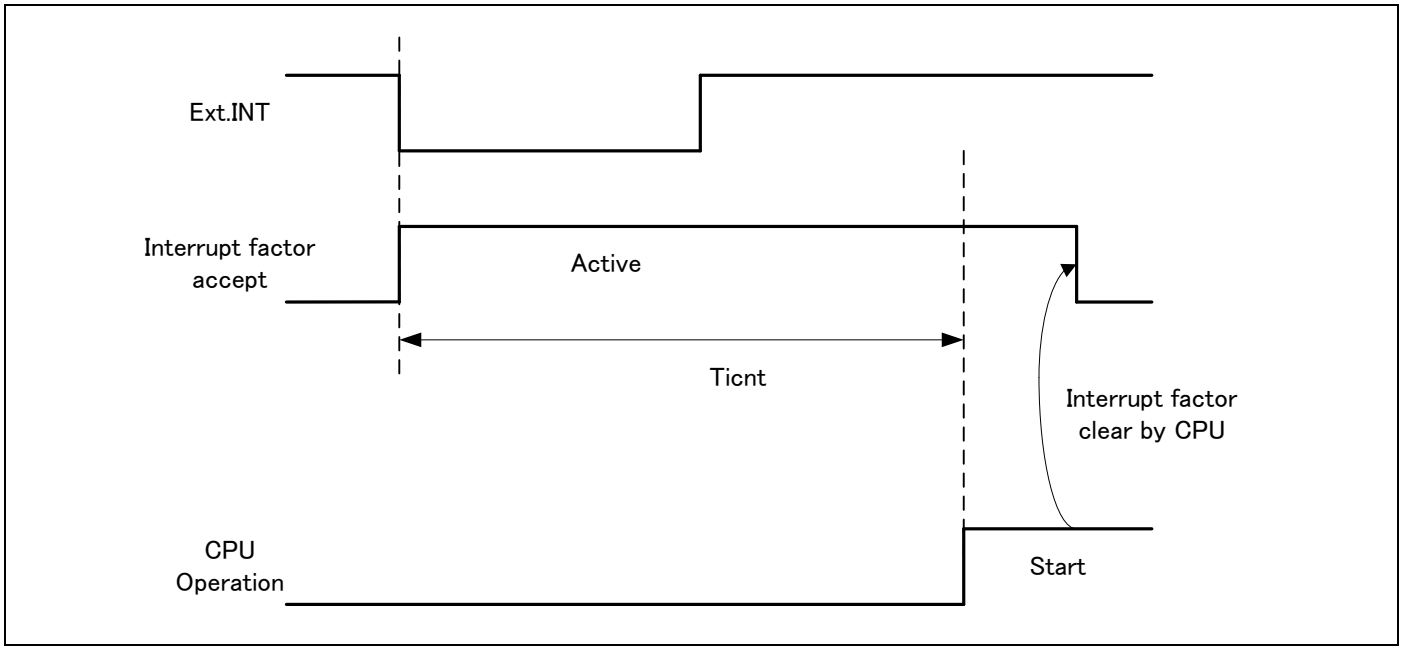
**Recovery count time**

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Typ | Max* | | |
| Sleep mode | Ticnt | HCLK×1 | | µs | |
| High-speed CR Timer mode<br>Main Timer mode<br>PLL Timer mode | | 40 | 80 | µs | |
| Low-speed CR timer mode | | 450 | 900 | µs | |
| Sub timer mode | | 896 | 1136 | µs | |
| RTC mode<br>stop mode<br>(High-speed CR /Main/PLL run mode return) | | 316 | 581 | µs | |
| RTC mode<br>stop mode<br>(Low-speed CR/sub run mode return) | | 270 | 540 | | |
| Deep standby RTC mode with RAM retention | | 365 | 667 | µs | without RAM retention |
| Deep standby stop mode with RAM retention | | 365 | 667 | µs | with RAM retention |

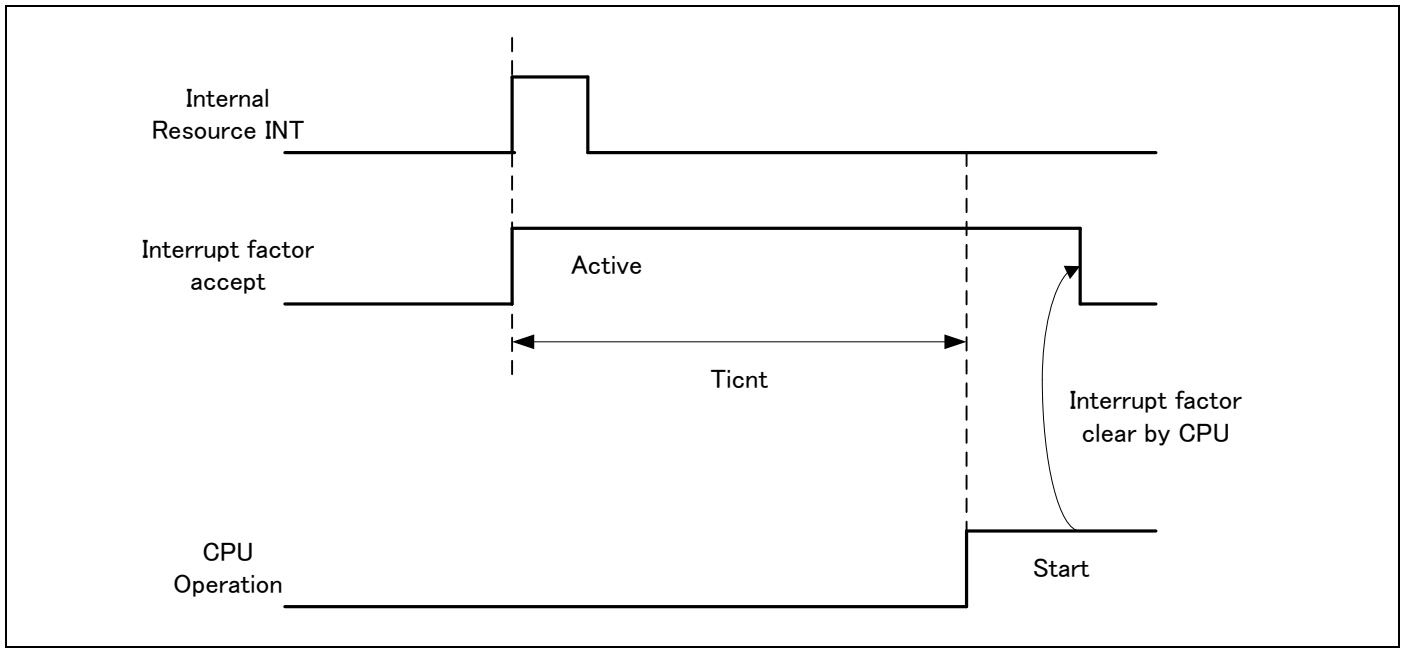
*: The maximum value depends on the built-in CR accuracy.

**Example of standby recovery operation (when in external interrupt recovery*)**




*: External interrupt is set to detecting fall edge.

**Example of standby recovery operation (when in internal resource interrupt recovery*)**




*: Depending on the standby mode, interrupt from the internal resource is not included in the recovery cause.

***Notes:***

- *The return factor is different in each Low-Power consumption modes.*
  *See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM4 Family Peripheral Manual.*
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM4 Family Peripheral Manual".*

### *12.10.2 Recovery cause: Reset*

The time from reset release to the program operation start is shown.

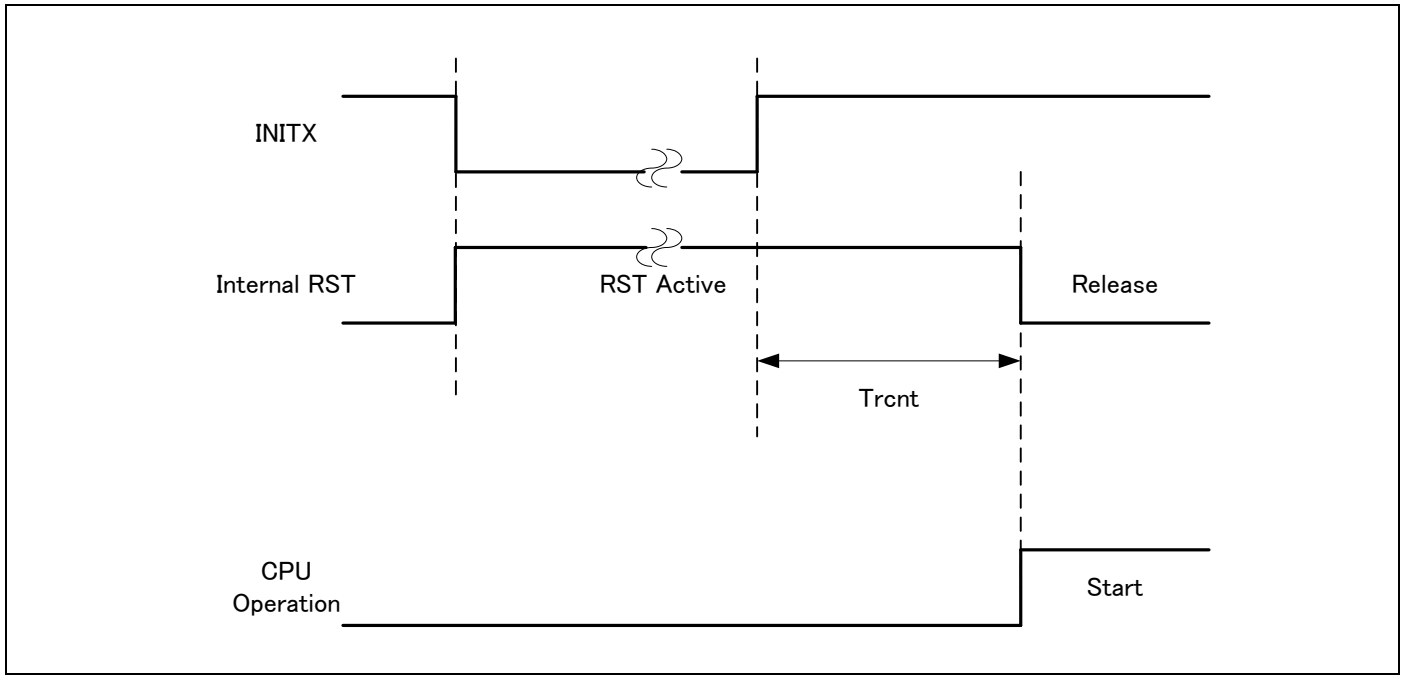
**Recovery count time**

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

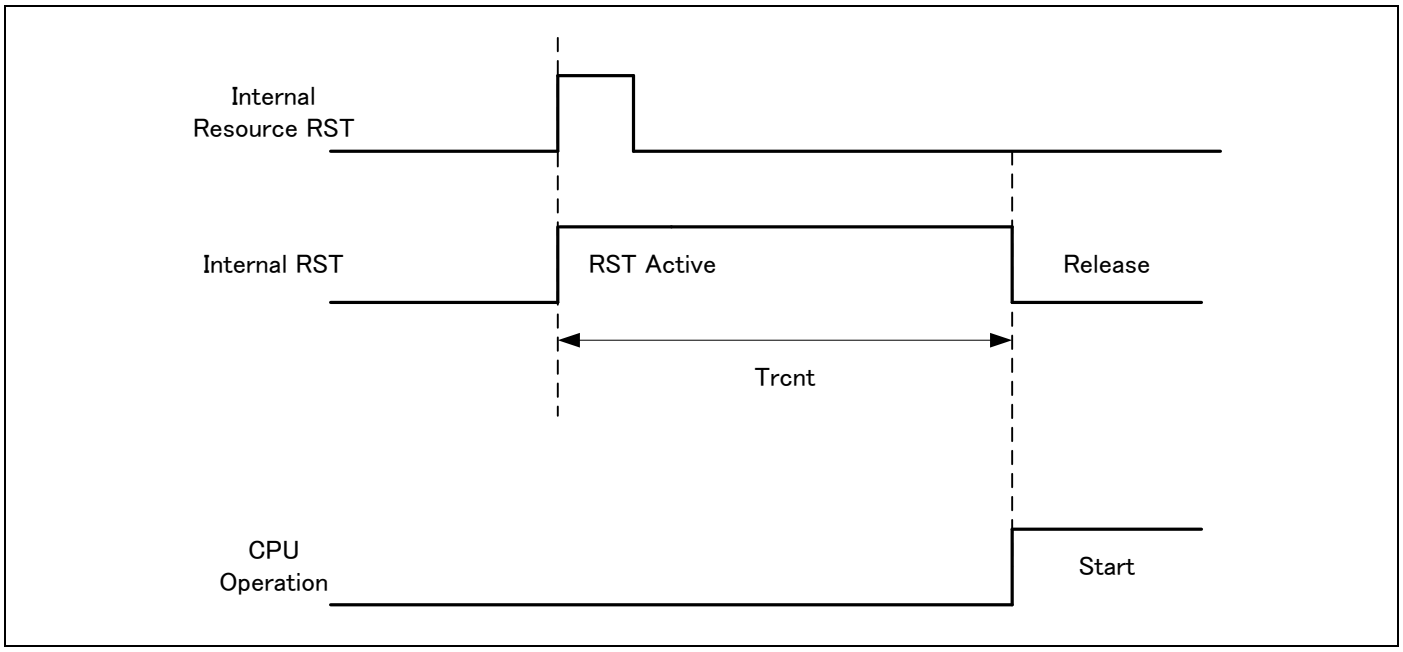
| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Typ | Max* | | |
| Sleep mode | Trcnt | 155 | 266 | µs | |
| High-speed CR Timer mode<br>Main Timer mode<br>PLL Timer mode | | 155 | 266 | µs | |
| Low-speed CR timer mode | | 315 | 567 | µs | |
| Sub timer mode | | 315 | 567 | µs | |
| RTC mode<br>stop mode | | 315 | 567 | µs | |
| Deep standby RTC mode with RAM retention | | 336 | 667 | µs | without RAM retention |
| Deep standby stop mode with RAM retention | | | | µs | with RAM retention |

*: The maximum value depends on the built-in CR accuracy.

**Example of standby recovery operation (when in INITX recovery)**



**Example of standby recovery operation (when in internal resource reset recovery*)**




*: Depending on the standby mode, the reset issue from the internal resource is not included in the recovery cause.

***Notes:***

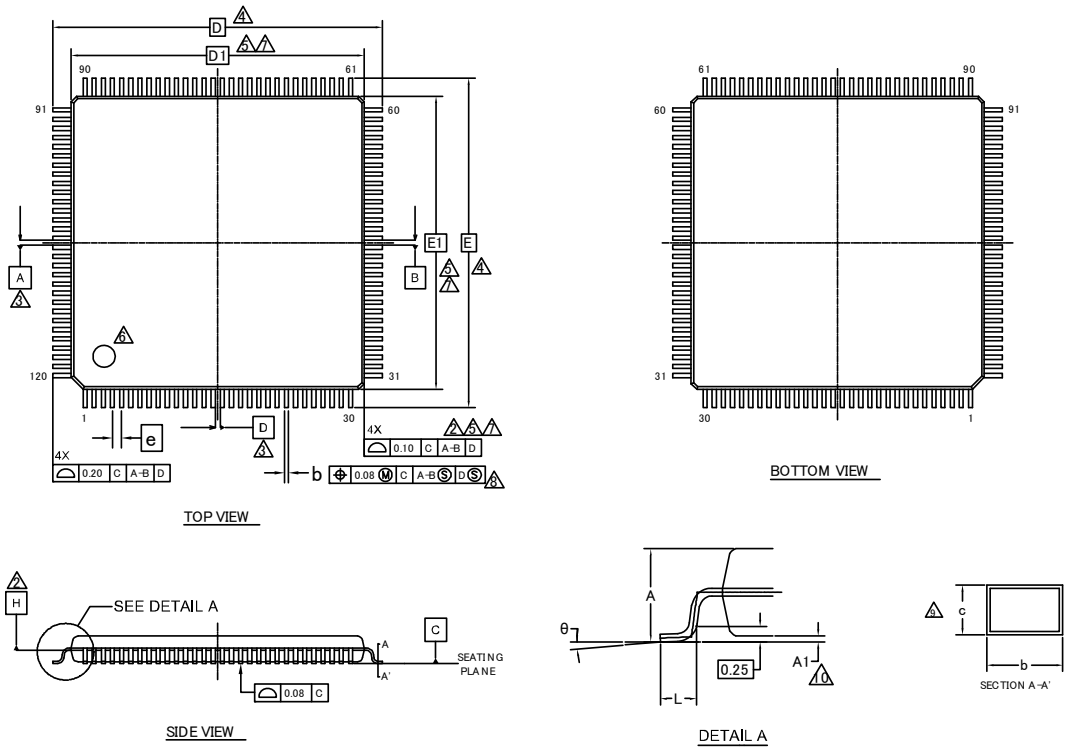
- *The return factor is different in each Low-Power consumption modes.*
  *See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM4 Family Peripheral Manual.*
- *The time during the power-on reset/low-voltage detection reset is excluded to the recovery source. See "12.4.7 Power-on Reset Timing" in "12.4. AC Characteristics" in "12.Electrical Characteristics" for the detail on the time during the power-on reset/low-voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

## 13. Ordering Information

| Part Number | Flash | RAM | Package |
|---|---|---|---|
| MB9BF168MPMC-G-JNE2 | 1 MB | 128 KB | Plastic・LQFP (0.5 mm pitch), 80 pin (LQH080) |
| MB9BF167MPMC-G-JNE2 | 768 KB | 96 KB | |
| MB9BF166MPMC-G-JNE2 | 512 KB | 64 KB | |
| MB9BF168MPMC1-G-JNE2 | 1 MB | 128 KB | Plastic・LQFP (0.65 mm pitch), 80 pin (LQJ080) |
| MB9BF167MPMC1-G-JNE2 | 768 KB | 96 KB | |
| MB9BF166MPMC1-G-JNE2 | 512 KB | 64 KB | |
| MB9BF168NPMC-G-JNE2 | 1 MB | 128 KB | Plastic・LQFP (0.5 mm pitch), 100 pin (LQI100) |
| MB9BF167NPMC-G-JNE2 | 768 KB | 96 KB | |
| MB9BF166NPMC-G-JNE2 | 512 KB | 64 KB | |
| MB9BF168RPMC-G-JNE2 | 1 MB | 128 KB | Plastic・LQFP (0.5 mm pitch), 120 pin (LQM120) |
| MB9BF167RPMC-G-JNE2 | 768 KB | 96 KB | |
| MB9BF166RPMC-G-JNE2 | 512 KB | 64 KB | |
| MB9BF168NBGL-GE1 | 1 MB | 128 KB | Plastic・PFBGA (0.5 mm pitch), 112 pin (LDC112) |
| MB9BF167NBGL-GE1 | 768 KB | 96 KB | |
| MB9BF166NBGL-GE1 | 512 KB | 64 KB | |
| MB9BF168RBGL-GK7E1 | 1 MB | 128 KB | Plastic・PFBGA (0.5 mm pitch), 144 pin (LDC144) |
| MB9BF167RBGL-GK7E1 | 768 KB | 96 KB | |
| MB9BF166RBGL-GK7E1 | 512 KB | 64 KB | |
| MB9BF168NPQC-G-JNE2 | 1 MB | 128 KB | Plastic・QFP (0.65 mm pitch), 100 pin (PQH100) |
| MB9BF167NPQC-G-JNE2 | 768 KB | 96 KB | |
| MB9BF166NPQC-G-JNE2 | 512 KB | 64 KB | |

## 14. Package Dimensions

| Package Type | Package Code |
|---|---|
| LQFP-120 | LQM120 |



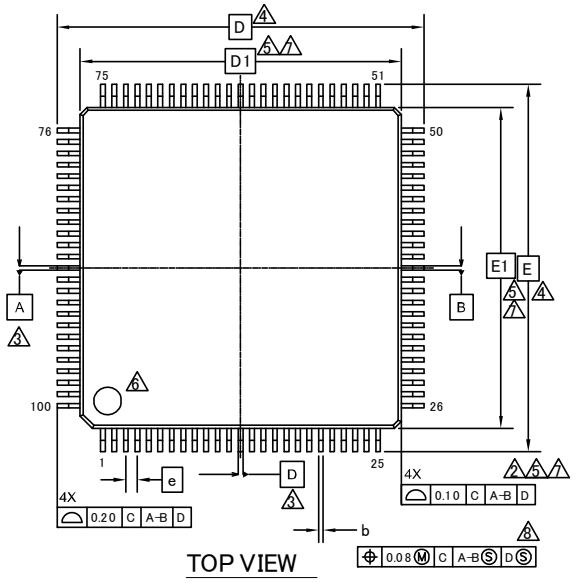

| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.115 | — | 0.195 |
| D | 18.00 BSC | | |
| D1 | 16.00 BSC | | |
| e | 0.50 BSC | | |
| E | 18.00 BSC | | |
| E1 | 16.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| θ | 0° | — | 8° |

NOTES

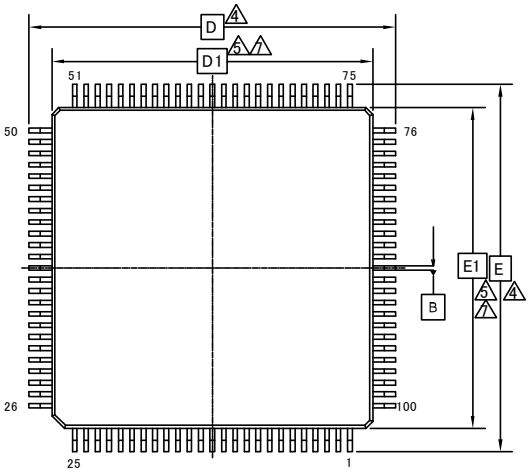
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

PACKAGE OUTLINE, 120 LEAD LQFP
18.0X18.0X1.7 MM LQM120 REV**

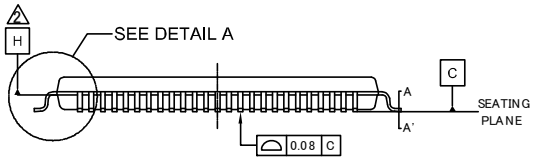
| Package Type | Package Code |
|---|---|
| LQFP-100 | LQI100 |



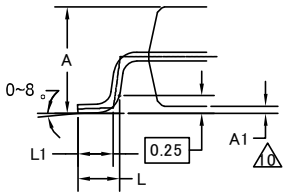

TOP VIEW



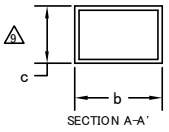

BOTTOM VIEW




SIDE VIEW




DETAIL A




SECTION A-A'

| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| b | 0.15 | — | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 16.00 BSC | | |
| D1 | 14.00 BSC | | |
| e | 0.50 BSC | | |
| E | 16.00 BSC | | |
| E1 | 14.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |

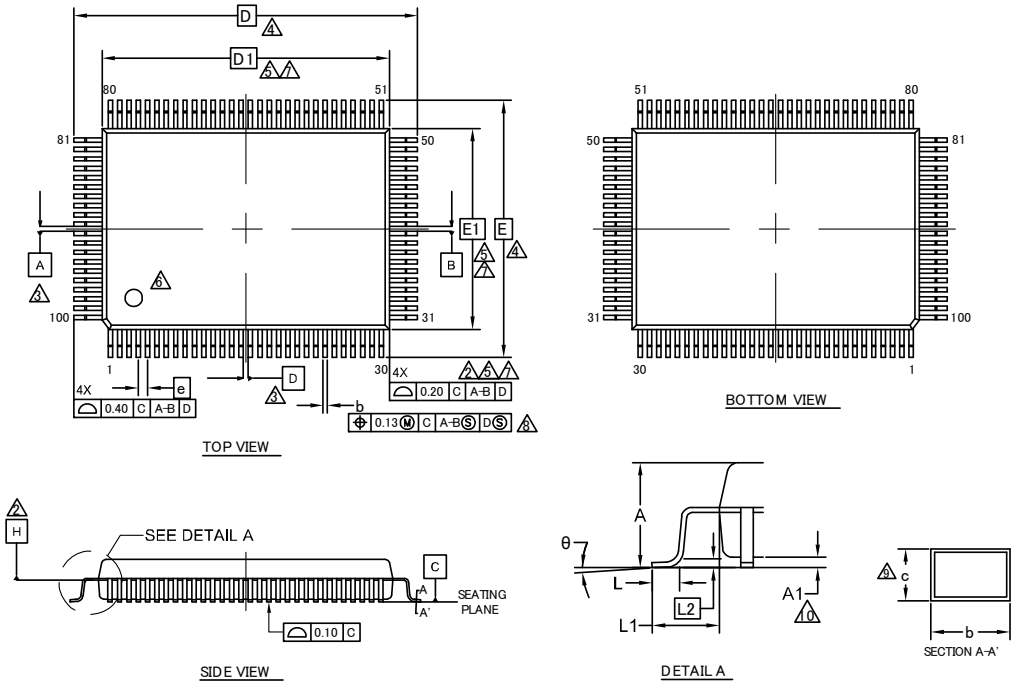
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 REV*A

002-11500 *A

| Package Type | Package Code |
|---|---|
| QFP-100 | PQH100 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 3.35 |
| A1 | 0.05 | — | 0.45 |
| b | 0.27 | 0.32 | 0.37 |
| c | 0.11 | — | 0.23 |
| D | 23.90 BSC | | |
| D1 | 20.00 BSC | | |
| e | 0.65 BSC | | |
| E | 17.90 BSC | | |
| E1 | 14.00 BSC | | |
| θ | 0° | — | 8° |
| L | 0.73 | 0.88 | 1.03 |
| L1 | 1.95 REF | | |
| L2 | 0.25 BSC | | |

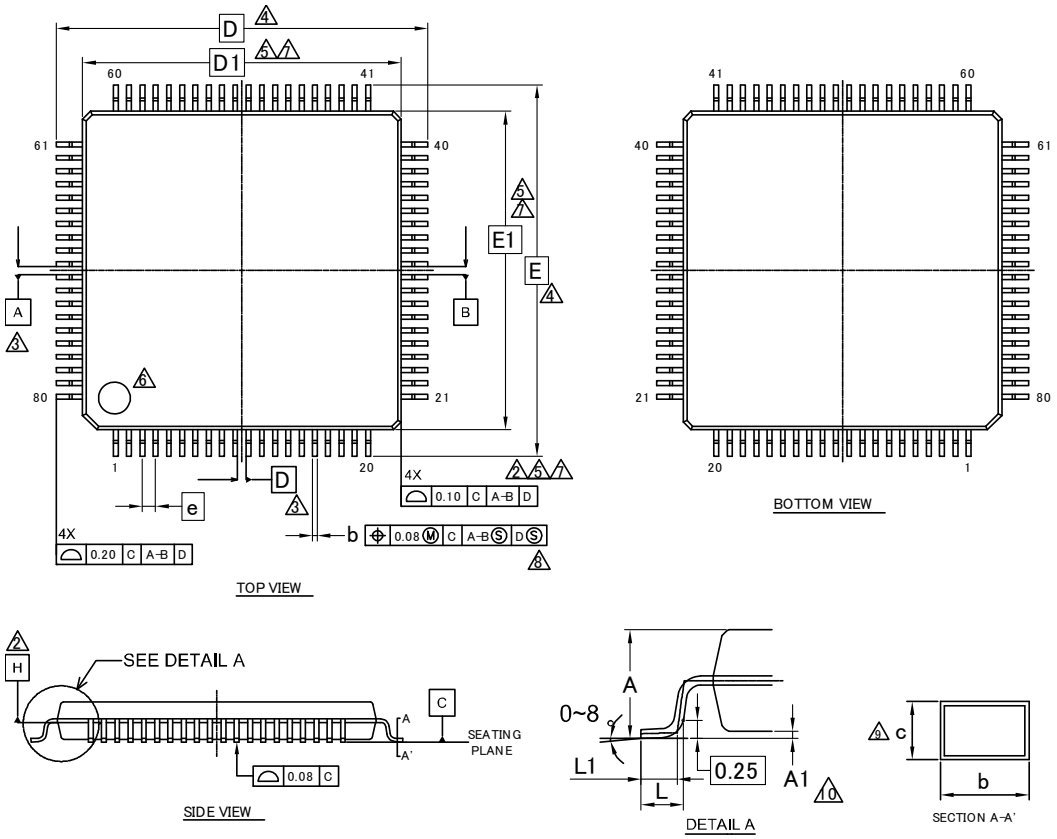
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 100 LEAD QFP
20.00X14.00X3.35 MM PQH100 REV**

002-15156 **

| Package Type | Package Code |
|---|---|
| LQFP-80 | LQH080 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| b | 0.15 | — | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 14.00 BSC. | | |
| D1 | 12.00 BSC. | | |
| e | 0.50 BSC | | |
| E | 14.00 BSC. | | |
| E1 | 12.00 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |

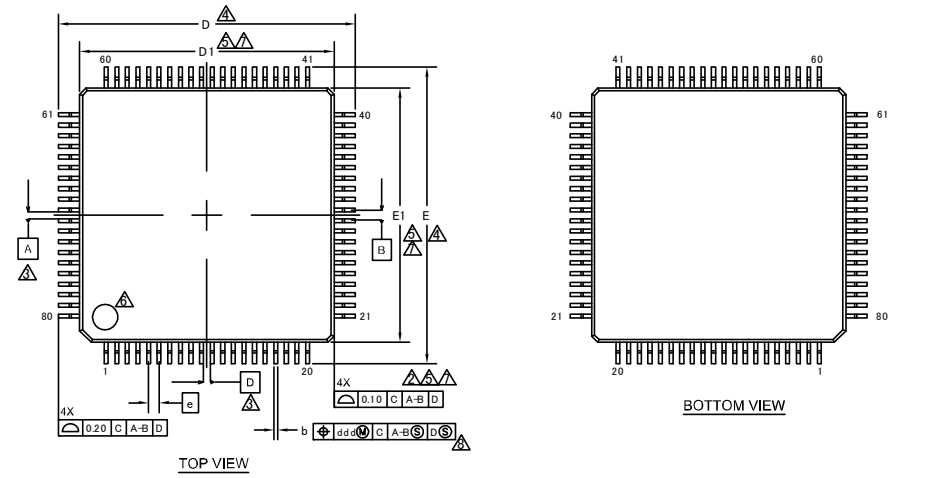
NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 80 LEAD LQFP
12.0X12.0X1.7 MM LQH080 Rev **

002-11501 **

| Package Type | Package Code |
|---|---|
| LQFP-80 | LQJ080 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.00 | — | 0.20 |
| b | 0.16 | 0.32 | 0.38 |
| c | 0.09 | — | 0.20 |
| D | 16.00 BSC | | |
| D1 | 14.00 BSC | | |
| e | 0.65 BSC | | |
| E | 16.00 BSC | | |
| E1 | 14.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |
| θ | 0° | — | 8° |

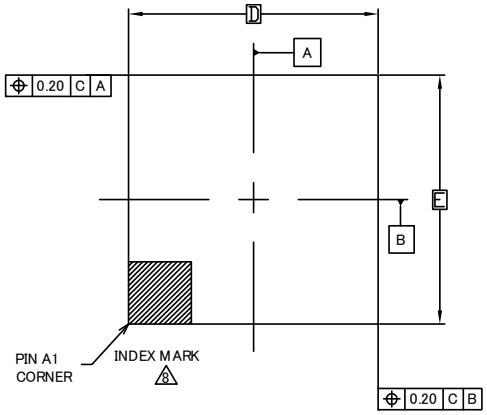
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

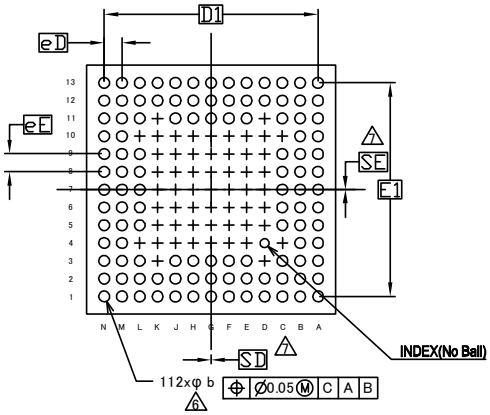
PACKAGE OUTLINE, 80 LEAD LQFP
14.0X14.0X1.7 MM LQJ080 REV**

002-14043 **

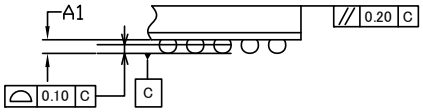
| Package Type | Package Code |
|---|---|
| BGA-112 | LDC112 |



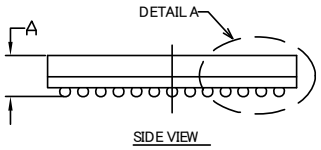

TOP VIEW




BOTTOM VIEW




DETAIL A




SIDE VIEW

| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | —— | —— | 1.35 |
| $A_1$ | 0.15 | 0.25 | 0.35 |
| D | | 7.00 BSC | |
| E | | 7.00 BSC | |
| D1 | | 6.00 BSC | |
| E1 | | 6.00 BSC | |
| MD | | 13 | |
| ME | | 13 | |
| n | | 112 | |
| Φb | 0.20 | 0.30 | 0.40 |
| eD | | 0.50 BSC | |
| eE | | 0.50 BSC | |
| SD / SE | | 0.00 | |

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

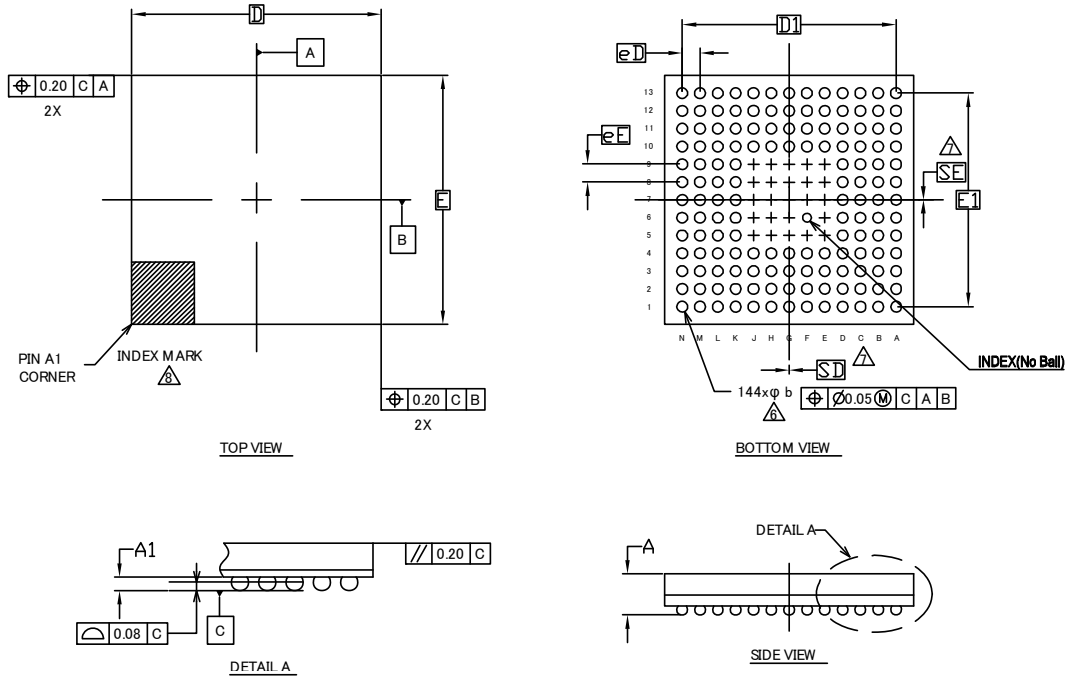
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.

8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

PACKAGE OUTLINE, 112 BALL FBGA
7.0X7.0X1.35 MM LDC112 REV**

002-16663 **

| Package Type | Package Code |
|---|---|
| BGA-144 | LDC144 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | —— | —— | 1.30 |
| A1 | 0.15 | 0.25 | 0.35 |
| D | | 7.00 BSC | |
| E | | 7.00 BSC | |
| D1 | | 6.00 BSC | |
| E1 | | 6.00 BSC | |
| MD | | 13 | |
| ME | | 13 | |
| n | | 144 | |
| Φb | 0.20 | 0.30 | 0.40 |
| eD | | 0.50 BSC | |
| eE | | 0.50 BSC | |
| SD / SE | | 0.00 | |

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.

8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

PACKAGE OUTLINE, 144 BALL FBGA
7.0X7.0X1.3 MM LDC144 REV**

002-16662 **

## 15. Major Changes

**Spansion Publication Number: DS709-00004**

| Page | Section | Change Results |
|---|---|---|
| - | - | Preliminary → Data Sheet |
| 1 | Description | Deleted the following description :<br>The products which are described in this data sheet are placed into TYPE4 product categories in "FM4 Family PERIPHERAL MANUAL". |
| 3 | Features<br>Multi-Function Serial Interface<br>[$I^2C$] | Revised the following description :<br>Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.3 and ch.7) supported<br>→Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.3=ch.A and ch.7=ch.B) supported |
| 7 | Features<br>Unique Id | Added new section |
| 9 | Product Lineup<br>Function | Added “Unique ID” |
| 51, 52 | I/O Circuit Type | Revised the remarks of “Type O, P, Q” |
| 59 | Handling Devices<br>Handling When Using Debug Pins | Added new section |
| 60 | Block Diagram | Revised the block diagram |
| 72 | Electrical Characteristics<br>2. Recommended Operating Conditions | Revised “Table for package thermal resistance and maximum permissible power” |
| 75 to 80 | Electrical Characteristics<br>3. Dc Characteristics<br>(1) Current Rating | • Revised the value of TBD<br>• Added the note to “ICCVBAT” |
| 85 | Electrical Characteristics<br>4. Ac Characteristics<br>(2) Sub Clock Input Characteristics | Revised the waveform chart |
| 85 | Electrical Characteristics<br>4. Ac Characteristics<br>(3) Built-In Cr Oscillationcharacteristics | • Revised the value of TBD<br>• Revised the table and the note of “Built-in High-speed CR” |
| 144 | Electrical Characteristics<br>5. 12-Bit A/D Converter<br>Electrical Characteristics For The A/D Converter | • Revised the value of TBD<br>• Revised the condition of the electrical characteristics table |
| 147 | Electrical Characteristics<br>6. 12-Bit D/A Converter<br>Electrical Characteristics For The D/A Converter | • Revised the value of TBD<br>• Revised the condition and Remarks of the electrical characteristics table |
| 150 | Electrical Characteristics<br>10. Standby Recovery Time<br>(1) Recovery Cause: Interrupt/Wkup | • Revised the value of TBD<br>• Revised the table of Recovery count time |
| 152 | Electrical Characteristics<br>10. Standby Recovery Time<br>(2) Recovery Cause:Reset | • Revised the value of TBD<br>• Revised the table of Recovery count time |

Note: Please see “Document History” about later revised information.

## Document History

**Document Title: MB9B160R Series 32-bit ARM® Cortex®-M4F FM4 Microcontroller**
**Document Number: 002-04918**

| Revision | MB9B160R Series ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | – | AKIH | 06/27/2013 | Migrated to Cypress and assigned document number 002-04918.<br>No change to document contents or format. |
| *A | 5162380 | AKIH | 03/07/2016 | Updated to Cypress format. |
| *B | 5516291 | YSKA | 02/02/2017 | Updated “12.4.7 Power-On Reset Timing”. Changed parameter from “Power Supply rise time(Tr)[ms]” to “Power ramp rate(dV/dt)[mV/us]” and add some comments (Page 84)<br>Modified the Chapter name “12.4.11 UART Timing” to “12.4.11 CSIO/UART Timing”. (Page 97)<br>Modified “12.4.11 CSIO/UART Timing)”. Deleted “SPI=1, MS=0” in the titles and added MS=0,1 in the schematic (Page 105-112, 121-128)<br>Added the Baud rate spec in “12.4.12 CSIO/UART Timing”.(Page 97, 99, 101, 103)<br>“Modified RTC description in “Features, Real-Time Clock(RTC)” Changed starting count value from 01 to 00. Deleted “second , or day of the week” in the Interrupt function (Page 3)<br>Added Maximum Access size in “Features”(Page 1)<br>Modifications related to the VBAT in the following chapter. “7. Handling Devices” Notes on Power-on (Page 54) “11. Pin Status in Each CPU State” List of VBAT Domain Pin Status (Page 66) “12.3.1 Current Rating” Table12-9. Typical and Maximum Current Consumption in Deep Standby STOP Mode, Deep Standby RTC Mode and VBAT (Page 77)<br>Added Notes for JTAG (Page 42), Changed “J-TAG” to” JTAG” in “4 List of Pin Functions” (Page 30)<br>Modify typo in number of power supply(Three -> Two) (Page 4)<br>Updated Package code and dimensions as follows (Page 8-14, 68, 150-156)<br>FPT-120P-M37 -> LQM120, FPT-100P-M23 -> LQI100,<br>FPT-100P-M36 -> PQH100, FPT-80P-M37 -> LQH080,<br>FPT-80P-M40 -> LQJ080, BGA-112P-M05 -> LDC112,<br>BGA-144P-M09 -> LDC144<br>Changed the mode name of I2C as follows (Page 2, 133-134)<br>Typical mode -> Standard-mode, High-speed mode -> Fast-mode<br>Modified from “Analog port input current” to “Analog port input leak current” in “12.5 12-bit A/D Converter” (Page 139)<br>Modified according to the Datasheet Errata as below (No.1-9)<br>1. Modified Reference voltage value in “Electrical Characteristics for the A/D Converter” in “12.5 12-bit A/D Converter” (Page 139)<br>2. Modified typo in “Features, Processor version” (Page 1)<br>3. Updated Remarks of Type H, I in “5. I/O Circuit Type” (Page 45)<br>4. Updated “List of VBAT Domain Pin Status” (Page 66)<br>5. Modified “12.2 Recommended Operating Conditions” (Page 68)<br>6. Added “Frequency stabilization time” spec in “12.4.3 Built-in CR Oscillation |

| Revision | MB9B160R Series ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| | | | | Characteristics" (Page 82)<br>7. Added "Conversion time" spec in "12.6 12-bit D/A Converter" (Page 142)<br>8. Modified some spec values in "12.10.1 Recovery cause: Interrupt/WKUP" (Page 145) and "12.10.2 Recovery cause: Reset" (Page 147)<br>9. Modified the "sampling time" and "State transition time to operation permission" spec values in "12.5 12-bit A/D Converter"(Page 139)<br>Deleted MPNs below from "13. Ordering Information" (Page 149)<br>MB9BF166RBGL-GE1, MB9BF167RBGL-GE1, MB9BF168RBGL-GE1<br>Added MPNs below to "13. Ordering Information" (Page 149)<br>MB9BF166RBGL-GK7E1, MB9BF167RBGL-GK7E1, MB9BF168RBGL-GK7E1<br>Updated IO circuit (type A, N, O) (Page 43)<br>Modified the expression of the "Reference power supply current" "12.5 12-bit A/D Converter" (Page 139)<br>Modified the expression of the "Built-in CR" and add Note in the "1. Product Lineup"(Page 7)<br>Modified typo(SCLKx_0 -> SCKx_0)(Page 97, 99, 101, 103) |
| *C | 5738077 | YSAT | 05/16/2017 | Adapted new Cypress logo |
| *D | 5873294 | HUAL | 09/25/2017 | Fix minor issues listed in CDT 270742:<br>1.new note format had been updated from *x to *$^{x}$<br>2.double heading number had been cancelled on chapter 12.2<br>3.some chapter number missed in reference<br>4.change this sentence "In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only" to sentence "Between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate" |

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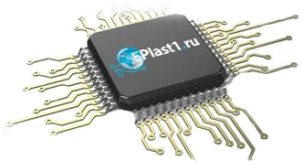


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