74HC2G125; 74HCT2G125

Dual buffer/line driver; 3-state

Rev. 04 — 4 July 2008 Product data sheet

1. General description

The 74HC2G125; 74HCT2G125 is a high-speed, Si-gate CMOS device.

The 74HC2G125; 74HCT2G125 provides two non-inverting buffer/line drivers with 3-state output. The 3-state output is controlled by the output enable input (pin $n\overline{OE}$). A HIGH level at pin $n\overline{OE}$ causes the output to assume a high-impedance OFF-state.

The bus driver output currents are equal compared to the 74HC125 and 74HCT125.

2. Features

- Wide supply voltage range from 2.0 V to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power consumption
- Balanced propagation delays
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC2G125DP	–40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HCT2G125DP				
74HC2G125DC	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74HCT2G125DC				
74HC2G125GD	–40 °C to +125 °C	XSON8U	plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 × 2 × 0.5 mm	SOT996-2
74HCT2G125GD				

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4. Marking

Table 2. Marking

Type number	Marking code
74HC2G125DP	H25
74HCT2G125DP	T25
74HC2G125DC	H25
74HCT2G125DC	T25
74HC2G125GD	H25
74HCT2G125GD	T25

5. Functional diagram

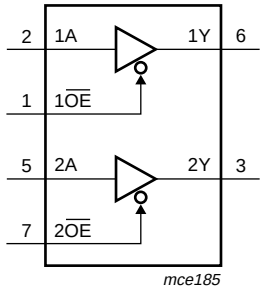


Fig 1. Logic symbol

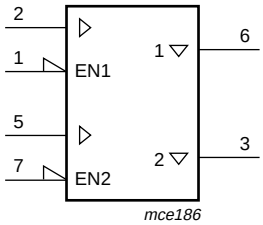


Fig 2. IEC logic symbol

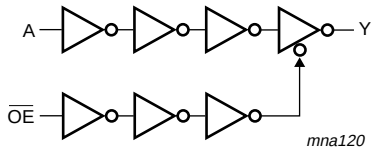


Fig 3. Logic diagram (one driver)

6. Pinning information

6.1 Pinning

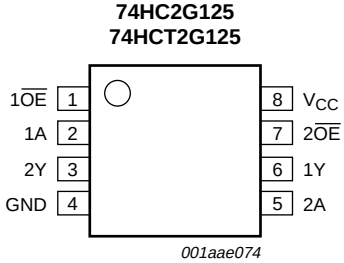
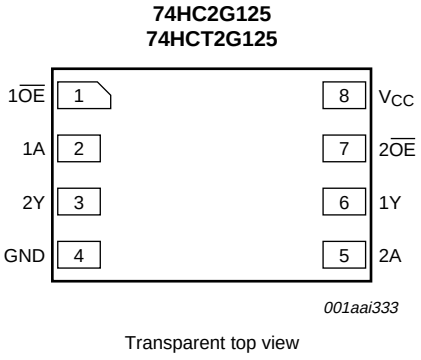


Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)



Transparent top view

Fig 5. Pin configuration SOT996-2 (XSON8U)

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6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$	1, 7	output enable input (active LOW)
1A, 2A	2, 5	data input
GND	4	ground (0 V)
1Y, 2Y	6, 3	data output
V_{CC}	8	supply voltage

7. Functional description

Table 4. Function table[1]

Control	Input	Output
$n\overline{OE}$	**nA**	**nY**
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O = –0.5$ V to $(V_{CC} + 0.5$ V)	[1]	-	35	mA
I_{CC}	supply current			-	70	mA
I_{GND}	ground current			–70	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = –40$ °C to +125 °C	[2]	-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.
For XSON8U package: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

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9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC2G125			74HCT2G125			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V). All typical values are measured at T_{amb} = 25 °C.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC2G125								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		I_O = –6.0 mA; V_{CC} = 4.5 V	3.84	4.32	-	3.7	-	V
		I_O = –7.8 mA; V_{CC} = 6.0 V	5.34	5.81	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±5.0	-	±10	µA

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Table 7. Static characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). All typical values are measured at T_{amb} = 25 °C.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	10	-	20	µA
C_I	input capacitance		-	1.0	-	-	-	pF
C_O	output capacitance		-	1.5	-	-	-	pF
74HCT2G125								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V						
		I_O = –20 µA	4.4	4.5	-	4.4	-	V
		I_O = –6.0 mA	3.84	4.32	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V						
		I_O = 20 µA	-	0	0.1	-	0.1	V
		I_O = 6.0 mA	-	0.16	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±5.0	-	±10	
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	10	-	20	µA
ΔI_{CC}	additional supply current	per input; V_{CC} = 4.5 V to 5.5 V; $V_I = V_{CC}$ – 2.1 V; I_O = 0 A	-	-	375	-	410	µA
C_I	input capacitance		-	1.0	-	-	-	pF
C_O	output capacitance		-	1.5	-	-	-	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 8.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC2G125								
t_{pd}	propagation delay	nA to nY; see Figure 6 [2]						
		V_{CC} = 2.0 V	-	35	115	-	135	ns
		V_{CC} = 4.5 V	-	11	23	-	27	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	10	-	-	-	ns
		V_{CC} = 6.0 V	-	8	20	-	23	ns

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Table 8. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 8.

Symbol	Parameter	Conditions		T_{amb} = −40 °C to +85 °C			T_{amb} = −40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{en}	enable time	$n\overline{OE}$ to nY; see Figure 7	[2]						
		V_{CC} = 2.0 V		-	40	115	-	135	ns
		V_{CC} = 4.5 V		-	11	23	-	27	ns
		V_{CC} = 6.0 V		-	8	20	-	23	ns
t_{dis}	disable time	$n\overline{OE}$ to nY; see Figure 7	[2]						
		V_{CC} = 2.0 V		-	24	125	-	150	ns
		V_{CC} = 4.5 V		-	12	25	-	30	ns
		V_{CC} = 6.0 V		-	10	21	-	26	ns
t_t	transition time	see Figure 6	[2]						
		V_{CC} = 2.0 V		-	18	75	-	90	ns
		V_{CC} = 4.5 V		-	6	15	-	18	ns
		V_{CC} = 6.0 V		-	5	13	-	15	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC}	[3]						
		output enabled		-	11	-	-	-	pF
		output disabled		-	1	-	-	-	pF
74HCT2G125									
t_{pd}	propagation delay	nA to nY; see Figure 6	[2]						
		V_{CC} = 4.5 V		-	15	31	-	38	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	12	-	-	-	ns
t_{en}	enable time	$n\overline{OE}$ to nY; see Figure 7; V_{CC} = 4.5 V	[2]	-	15	35	-	42	ns
t_{dis}	disable time	$n\overline{OE}$ to nY; see Figure 7; V_{CC} = 4.5 V	[2]	-	15	31	-	38	ns
t_t	transition time	see Figure 6; V_{CC} = 4.5 V	[2]	-	6	15	-	18	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} − 1.5 V	[3]						
		output enabled		-	11	-	-	-	pF
		output disabled		-	1	-	-	-	pF

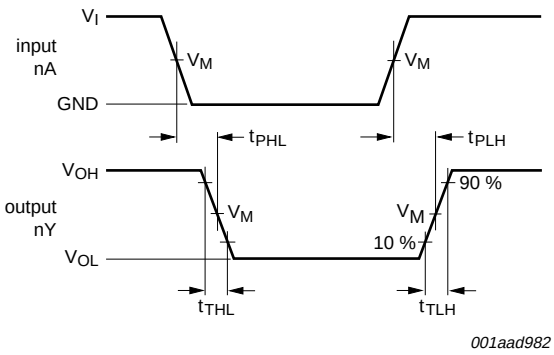
[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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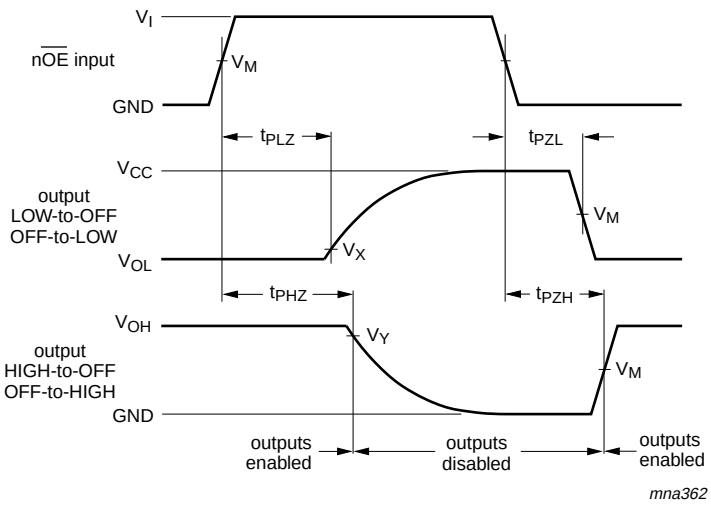
12. Waveforms



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. Propagation delays data input (nA) to output (nY)



Measurement points are given in Table 9.

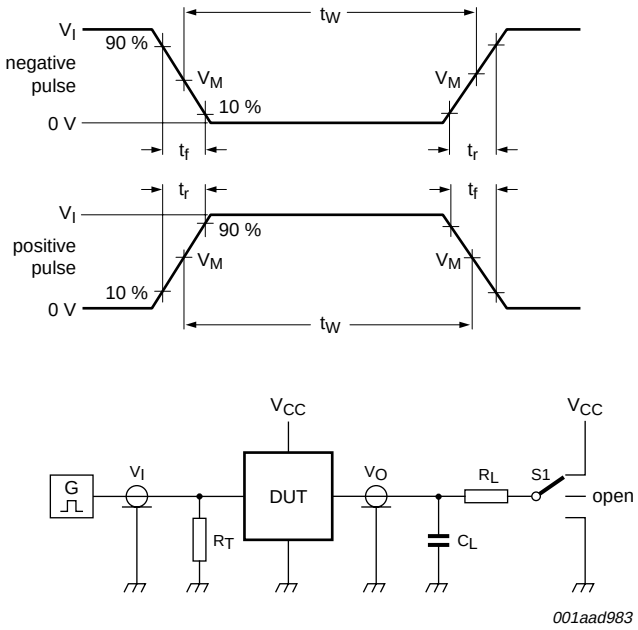
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. Enable and disable times

Table 9. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC2G125	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V
74HCT2G125	1.3 V	1.3 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V

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Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 8. Load circuitry for measuring switching times

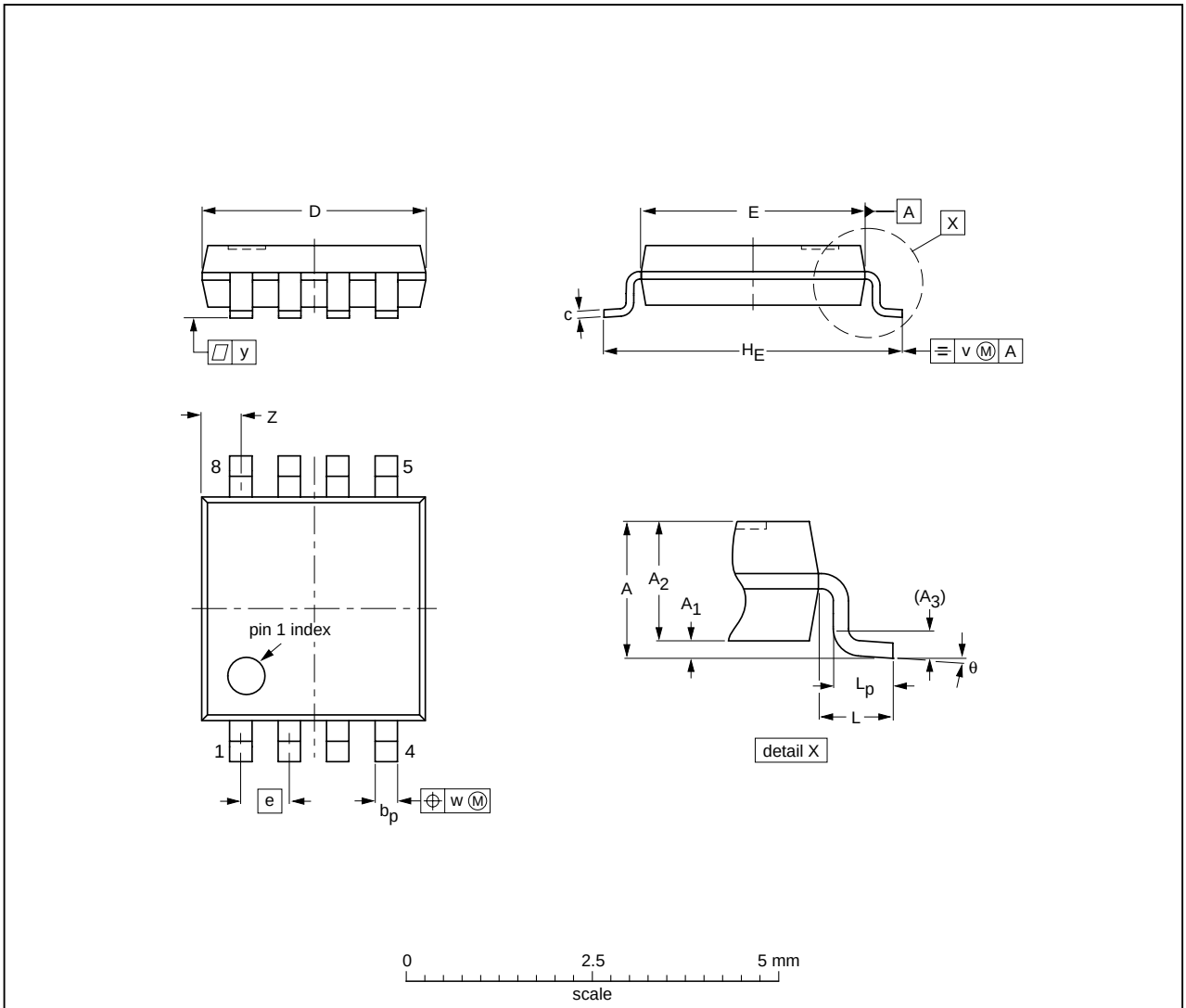
Table 10. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC2G125	V_{CC}	≤ 6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74HCT2G125	3 V	≤ 6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

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13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

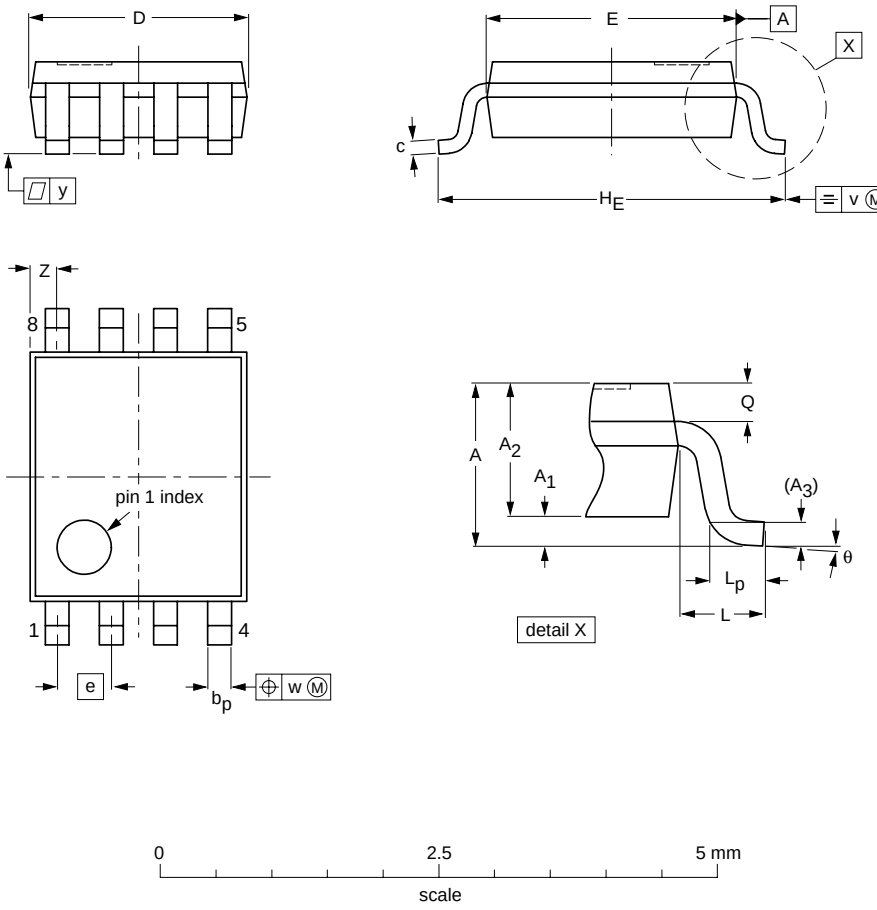
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig 9. Package outline SOT505-2 (TSSOP8)

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VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

Notes

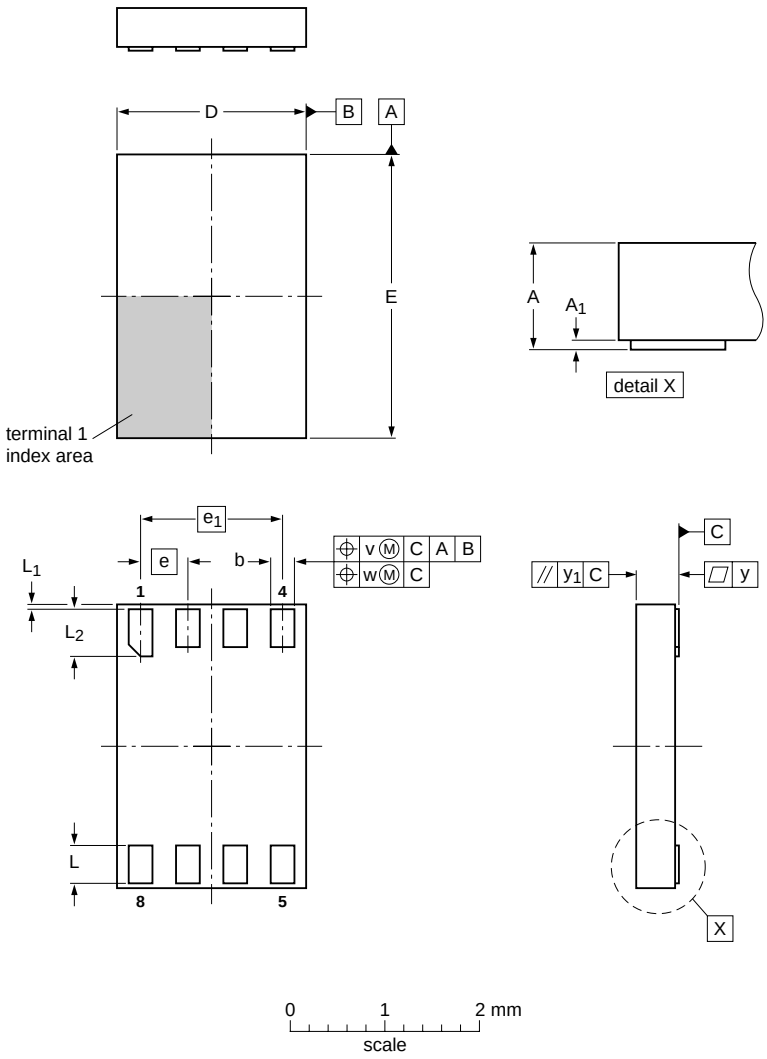
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 10. Package outline SOT765-1 (VSSOP8)

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XSON8U: plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 x 2 x 0.5 mm **SOT996-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	E	e	e_1	L	L_1	L_2	v	w	y	y_1
mm	0.5	0.05 0.00	0.35 0.15	2.1 1.9	3.1 2.9	0.5	1.5	0.5 0.3	0.15 0.05	0.6 0.4	0.1	0.05	0.05	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT996-2	- - -		- - -			~~07-12-18~~ 07-12-21

Fig 11. Package outline SOT996-2 (XSON8U)

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14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT2G125_4	20080704	Product data sheet	-	74HC_HCT2G125_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 8: derating factor for TSSOP8, VSSOP8 and XSON8U package added • Added type numbers 74HC2G125GD and 74HCT2G125GD (XSON8U package)			
74HC_HCT2G125_3	20060102	Product data sheet	-	74HC_HCT2G125_2
74HC_HCT2G125_2	20030303	Product specification	-	74HC_HCT2G125_1
74HC_HCT2G125_1	20030131	Product specification	-	-

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16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

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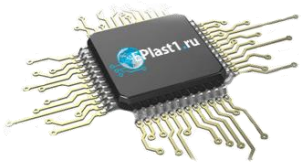
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