LM7332 Dual Rail-to-Rail Input/Output 30V, Wide Voltage Range, High Output Operational Amplifier

Check for Samples: LM7332

FEATURES

- **(V_S = ±15V, T_A = 25°C, Typical Values Unless Specified.)**
- **Wide Supply Voltage Range 2.5V to 32V**
- **Wide Input Common Mode Voltage 0.3V Beyond Rails**
- **Output Short Circuit Current >100 mA**
- **High Output Current (1V from Rails) ±70 mA**
- **GBWP 21 MHz**
- **Slew Rate 15.2 V/µs**
- **Capacitive Load Tolerance Unlimited**
- **Total Supply Current 2.0 mA**
- **Temperature Range −40°C to +125°C**
- **Tested at −40°C, +125°C, and 25°C at 5V, ±5V, ±15V**

APPLICATIONS

- **MOSFET and Power Transistor Driver**
- **Replaces Discrete Transistors in High Current Output Circuits**
- **Instrumentation 4-20 mA Current Loops**
- **Analog Data Transmission**
- **Multiple Voltage Power Supplies and Battery Chargers**
- **High and Low Side Current Sensing**
- **Bridge and Sensor Driving**
- **Digital to Analog Converter Output**

DESCRIPTION

The LM7332 is a dual rail-to-rail input and output amplifier with a wide operating temperature range (−40°C to +125°C) which meets the needs of automotive, industrial and power supply applications. The LM7332 has the output current of 100 mA which is higher than that of most monolithic op amps. Circuit designs with high output current requirements often need to use discrete transistors because many op amps have low current output. The LM7332 has enough current output to drive many loads directly, saving the cost and space of the discrete transistors.

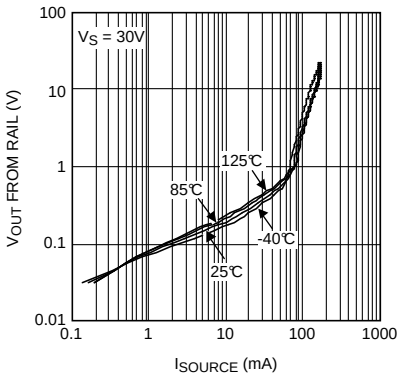
The exceptionally wide operating supply voltage range of 2.5V to 32V alleviates any concerns over functionality under extreme conditions and offers flexibility of use in a multitude of applications. Most of this device's parameters are insensitive to power supply variations; this design enhancement is another step in simplifying usage. Greater than rail-to-rail input common mode voltage range allows operation in many applications, including high side and low side sensing, without exceeding the input range.

The LM7332 can drive unlimited capacitive loads without oscillations.

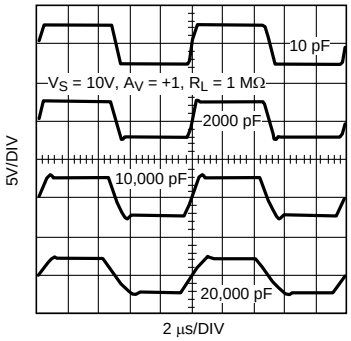
The LM7332 is offered in the 8-pin VSSOP and SOIC packages.

Key Graphs

Output Swing vs. Sourcing Current



Large Signal Step Response for Various Capacitive Loads



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	Human Body Model	2 kV
	Machine Model	200V
V_{IN} Differential		±10V
Output Short Circuit Duration		See (4), (5)
Supply Voltage ($V_S = V^+ - V^-$)		35V
Voltage at Input/Output pins		V^+ +0.3V, V^- −0.3V
Storage Temperature Range		−65°C to +150°C
Junction Temperature (6)		+150°C
Soldering Information:	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(5) Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S \leq 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5 ms.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings

Supply Voltage ($V_S = V^+ - V^-$)		2.5V to 32V
Temperature Range (1)		−40°C to +125°C
Package Thermal Resistance, θ_{JA}, (1)	8-Pin VSSOP	235°C/W
	8-Pin SOIC	165°C/W

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

5V Electrical Characteristics (1)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 0.5V, V_O = 2.5V, and R_L > 1 MΩ to 2.5V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V and V_{CM} = 4.5V	−4 **−5**	±1.6	+4 **+ 5**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = 0.5V and V_{CM} = 4.5V (4)		±2		µV/°C
I_B	Input Bias Current	See (5)	−2.0 **−2.5**	±1.0	+2.0 +2.5	µA
I_{OS}	Input Offset Current			20	250 **300**	nA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3V	67 **65**	80		dB
		0V ≤ V_{CM} ≤ 5V	62 **60**	70		
PSRR	Power Supply Rejection Ratio	5V ≤ V^+ ≤ 30V	78 **74**	100		dB
CMVR	Input Common Mode Voltage Range	CMRR > 50 dB		−0.3	−0.1 **0.0**	V
			5.1 **5.0**	5.3		
A_{VOL}	Large Signal Voltage Gain	0.5V ≤ V_O ≤ 4.5V R_L = 10 kΩ to 2.5V	70 **65**	77		dB
V_O	Output Swing High	R_L = 10 kΩ to 2.5V V_{ID} = 100 mV		60	150 **200**	mV from either rail
		R_L = 2 kΩ to 2.5V V_{ID} = 100 mV		100	300 **350**	
	Output Swing Low	R_L = 10 kΩ to 2.5V V_{ID} = −100 mV		5	150 **200**	
		R_L = 2 kΩ to 2.5V V_{ID} = −100 mV		20	300 **350**	
I_{SC}	Output Short Circuit Current	Sourcing from V^+, V_{ID} = 200 mV (6)	60	90		mA
		Sinking to V^-, V_{ID} = −200 mV (6)	60	90		
I_{OUT}	Output Current	V_{ID} = ±200 mV, V_O = 1V from rails		±55		mA
I_S	Total Supply Current	No Load, V_{CM} = 0.5V		1.5	2.3 **2.6**	mA
SR	Slew Rate (7)	A_V = +1, V_I = 5V Step, R_L = 1 MΩ, C_L = 10 pF		12		V/µs
f_u	Unity Gain Frequency	R_L = 10 MΩ, C_L = 20 pF		7.5		MHz
GBWP	Gain Bandwidth Product	f = 50 kHz		19.3		MHz
e_n	Input Referred Voltage Noise	f = 2 kHz		14.8		nV/√HZ

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing in the device.
(6) Short circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5 ms.
(7) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

5V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 0.5V, V_O = 2.5V, and R_L > 1 MΩ to 2.5V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
i_n	Input Referred Current Noise	f = 2 kHz		1.35		pA/√HZ
THD+N	Total Harmonic Distortion +Noise	A_V = +2, R_L = 100 kΩ, f = 1 kHz, V_O = 4 V_{PP}		−84		dB
CT Rej.	Crosstalk Rejection	f = 3 MHz, Driver R_L = 10 kΩ		68		dB

±5V Electrical Characteristics (1)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, V_O = 0V, and R_L > 1 MΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	V_{CM} = −4.5V and V_{CM} = 4.5V	−4 **−5**	±1.6	+4 **+5**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = −4.5V and V_{CM} = 4.5V (4)		±2		µV/°C
I_B	Input Bias Current	See (5)	−2.0 **−2.5**	±1.0	+2.0 **+2.5**	µA
I_{OS}	Input Offset Current			20	250 **300**	nA
CMRR	Common Mode Rejection Ratio	−5V ≤ V_{CM} ≤ 3V	74 **75**	88		dB
		−5V ≤ V_{CM} ≤ 5V	70 **65**	74		
PSRR	Power Supply Rejection Ration	5V ≤ V^+ ≤ 30V, V_{CM} = −4.5V	78 **74**	100		dB
CMVR	Input Common Mode Voltage Range	CMRR > 50 dB		−5.3	−5.1 **−5**	V
			5.1 **5.0**	5.3		
A_{VOL}	Large Signal Voltage Gain	−4V ≤ V_O ≤ 4V R_L = 10 kΩ to 0V	72 **70**	80		dB
V_O	Output Swing High	R_L = 10 kΩ to 0V V_{ID} = 100 mV		75	250 **300**	mV from either rail
		R_L = 2 kΩ to 0V V_{ID} = 100 mV		125	350 **400**	
	Output Swing Low	R_L = 10 kΩ to 0V V_{ID} = −100 mV		10	250 **300**	
		R_L = 2 kΩ to 0V V_{ID} = −100 mV		30	350 **400**	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing in the device.

±5V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, V_O = 0V, and R_L > 1 MΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
I_{SC}	Output Short Circuit Current	Sourcing from V^+, V_{ID} = 200 mV (6)	90	120		mA
		Sinking to V^-, V_{ID} = −200 mV (6)	90	100		
I_{OUT}	Output Current	V_{ID} = ±200 mV, V_O = 1V from rails		±65		mA
I_S	Total Supply Current	No Load, V_{CM} = −4.5V		1.5	2.4 **2.6**	mA
SR	Slew Rate (7)	A_V = +1, V_I = 8V Step, R_L = 1 MΩ, C_L = 10 pF		13.2		V/µs
R_{OUT}	Close Loop Output Resistance	A_V = +1, f = 100 kHz		3		Ω
f_u	Unity Gain Frequency	R_L = 10 MΩ, C_L = 20 pF		7.9		MHz
GBWP	Gain Bandwidth Product	f = 50 kHz		19.9		MHz
e_n	Input Referred Voltage Noise	f = 2 kHz		14.7		nV/√HZ
i_n	Input Referred Current Noise	f = 2 kHz		1.3		pA/√HZ
THD+N	Total Harmonic Distortion +Noise	A_V = +2, R_L = 100 kΩ, f = 1 kHz V_O = 8 V_{PP}		−87		dB
CT Rej.	Crosstalk Rejection	f = 3 MHz, Driver R_L = 10 kΩ		68		dB

(6) Short circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5 ms.
(7) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

±15V Electrical Characteristics (1)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, V_O = 0V, and R_L > 1 MΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	V_{CM} = −14.5V and V_{CM} = 14.5V	−5 **−6**	±2	+5 **+6**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = −14.5V and V_{CM} = 14.5V (4)		±2		µV/°C
I_B	Input Bias Current	See (5)	−2.0 **−2.5**	±1.0	+2.0 **+2.5**	µA
I_{OS}	Input Offset Current			20	250 **300**	nA
CMRR	Common Mode Rejection Ratio	−15V ≤ V_{CM} ≤ 12V	74 **74**	88		dB
		−15V ≤ V_{CM} ≤ 15V	72 **72**	80		
PSRR	Power Supply Rejection Ratio	−10V ≤ V^+ ≤ 15V, V_{CM} = −14.5V	78 **74**	100		dB
CMVR	Input Common Mode Voltage Range	CMRR > 50 dB		−15.3	−15.1 **−15**	V
			15.1 **15**	15.3		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing in the device.

±15V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, V_O = 0V, and R_L > 1 MΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
A_{VOL}	Large Signal Voltage Gain	−14V ≤ V_O ≤ 14V R_L = 10 kΩ to 0V	72 **70**	80		dB
V_O	Output Swing High	R_L = 10 kΩ to 0V V_{ID} = 100 mV		100	350 **400**	mV from either rail
		R_L = 2 kΩ to 0V V_{ID} = 100 mV		200	550 **600**	
	Output Swing Low	R_L = 10 kΩ to 0V V_{ID} = −100 mV		20	450 **500**	
		R_L = 2 kΩ to 0V V_{ID} = −100 mV		25	550 **600**	
I_{SC}	Output Short Circuit Current	Sourcing from V^+, V_{ID} = 200 mV (6)		140		mA
		Sinking to V^-, V_{ID} = −200 mV (6)		140		
I_{OUT}	Output Current	V_{ID} = ±200 mV, V_O = 1V from rails		±70		mA
I_S	Total Supply Current	No Load, V_{CM} = −14.5V		2.0	2.5 **3.0**	mA
SR	Slew Rate (7)	A_V = +1, V_I = 20V Step, R_L = 1 MΩ, C_L = 10 pF		15.2		V/µs
f_u	Unity Gain Frequency	R_L = 10 MΩ, C_L = 20 pF		9		MHz
GBWP	Gain Bandwidth Product	f = 50 kHz		21		MHz
e_n	Input Referred Voltage Noise	f = 2 kHz		15.5		nV/√HZ
i_n	Input Referred Current Noise	f = 2 kHz		1		pA/√HZ
THD+N	Total Harmonic Distortion +Noise	A_V = +2, R_L = 100 kΩ, f = 1 kHz V_O = 25 V_{PP}		−93		dB
CT Rej.	Crosstalk Rejection	f = 3 MHz, Driver R_L = 10 kΩ		68		dB

(6) Short circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5 ms.
(7) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

Connection Diagram

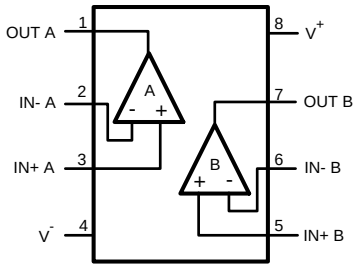


Figure 1. 8-Pin VSSOP (Top View)

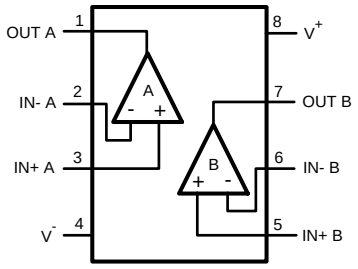


Figure 2. 8-Pin SOIC (Top View)

Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C.

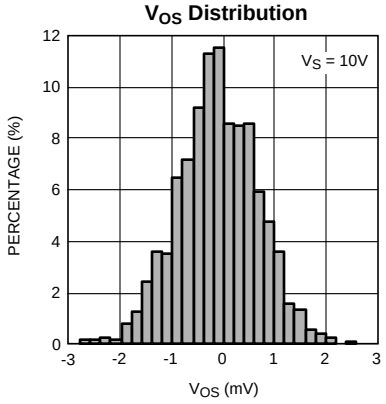


Figure 3.

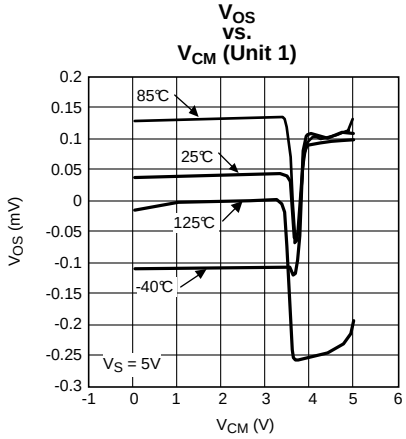


Figure 4.

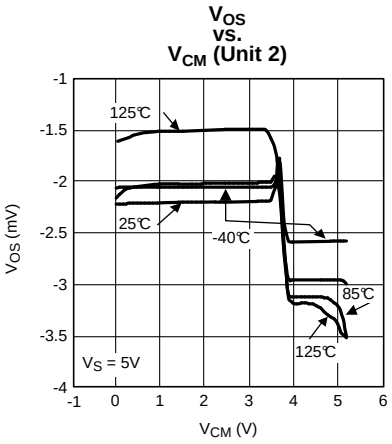


Figure 5.

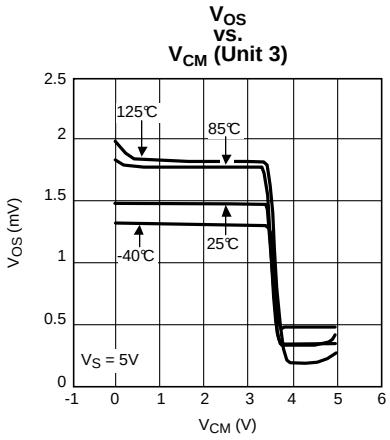


Figure 6.

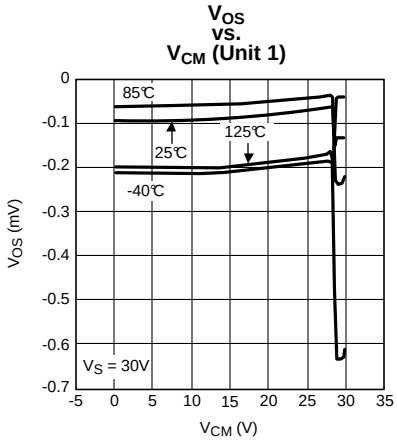


Figure 7.

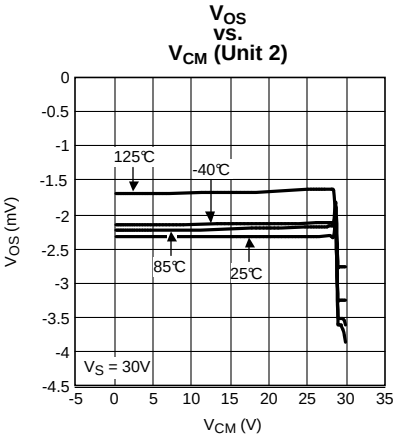


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

V_{OS} vs. V_{CM} (Unit 3)

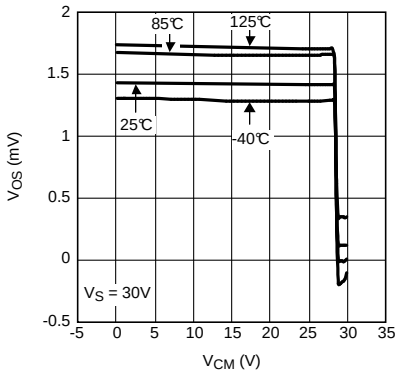


Figure 9.

V_{OS} vs. V_S (Unit 1)

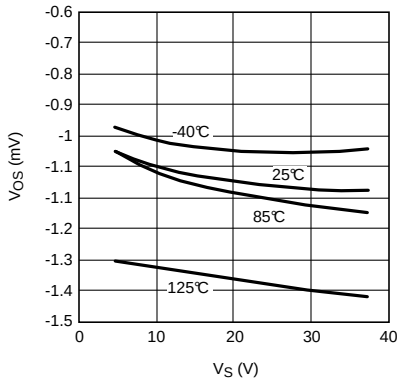


Figure 10.

V_{OS} vs. V_S (Unit 2)

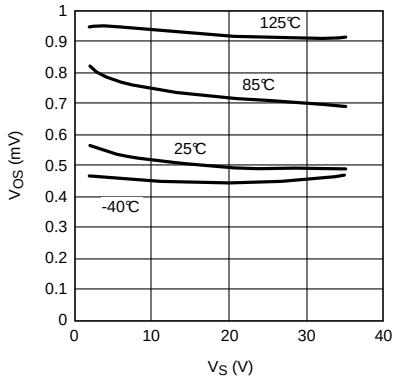


Figure 11.

V_{OS} vs. V_S (Unit 3)

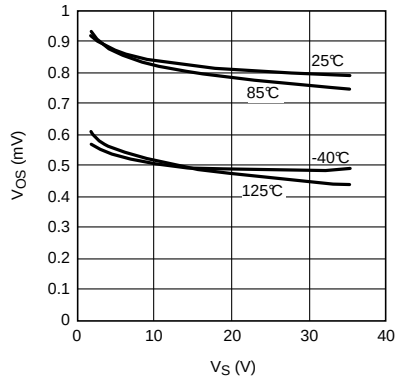


Figure 12.

I_{BIAS} vs. V_{CM}

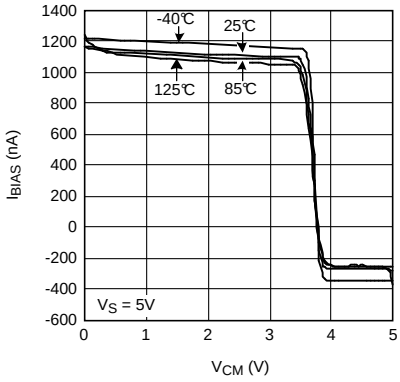


Figure 13.

I_{BIAS} vs. Supply Voltage

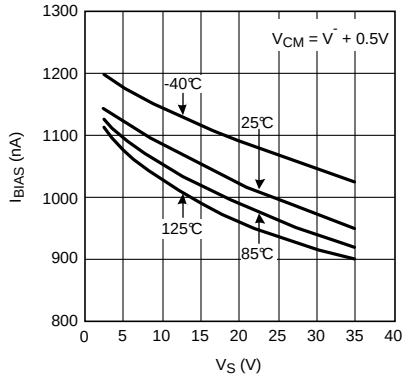


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

I_S vs. V_{CM}

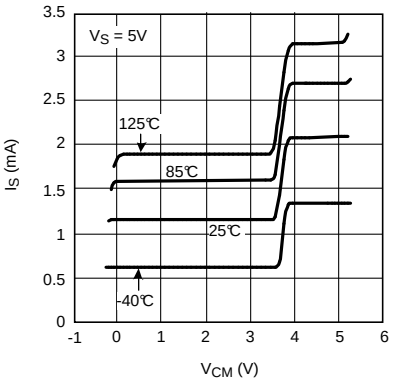


Figure 15.

I_S vs. V_{CM}

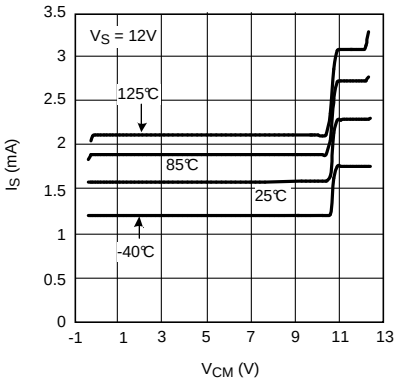


Figure 16.

I_S vs. V_{CM}

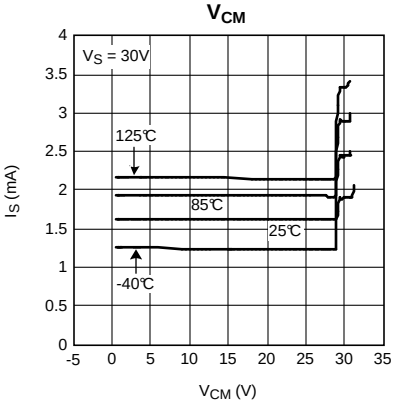


Figure 17.

I_S vs. Supply Voltage

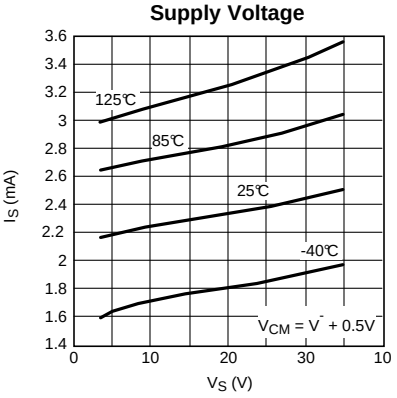


Figure 18.

I_S vs. Supply Voltage

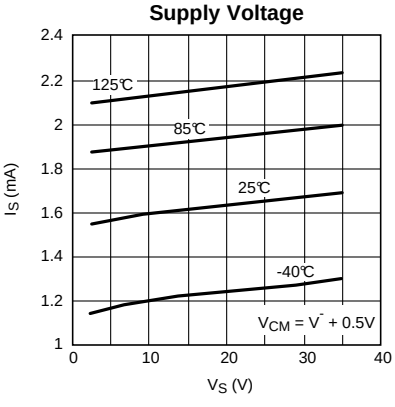


Figure 19.

Output Swing vs. Sinking Current

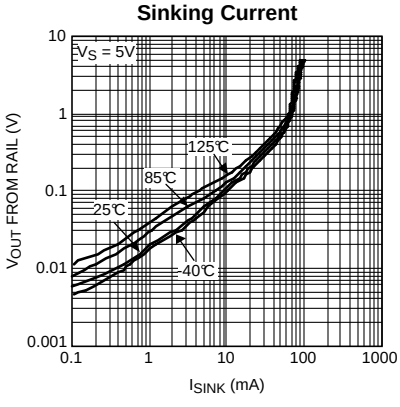


Figure 20.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

Output Swing vs. Sinking Current

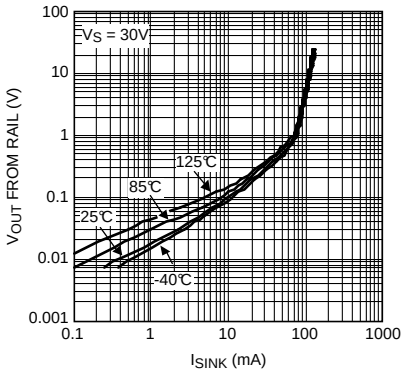


Figure 21.

Output Swing vs. Sourcing Current

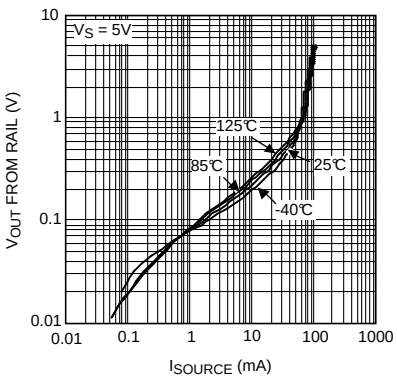


Figure 22.

Output Swing vs. Sourcing Current

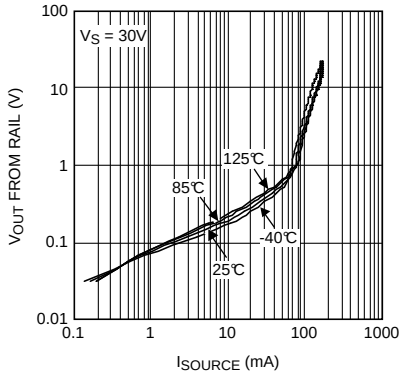


Figure 23.

Positive Output Swing vs. Supply Voltage

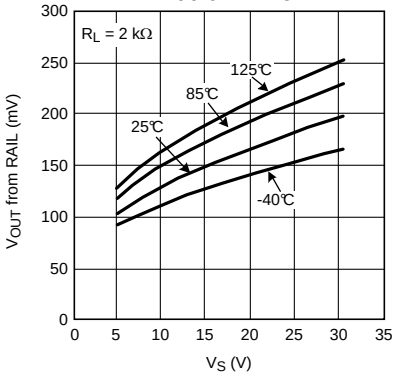


Figure 24.

Positive Output Swing vs. Supply Voltage

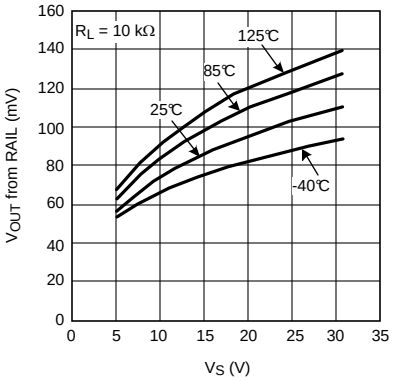


Figure 25.

Negative Output Swing vs. Supply Voltage

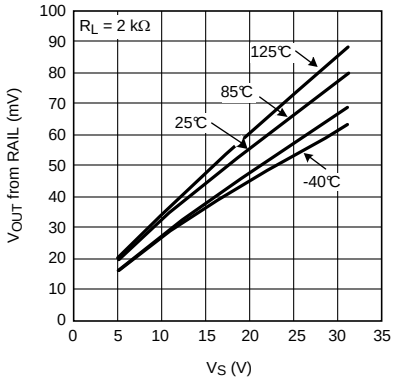


Figure 26.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

Negative Output Swing vs. Supply Voltage

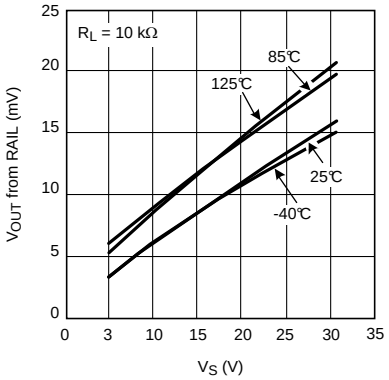


Figure 27.

Open Loop Frequency Response with Various Capacitive Loads

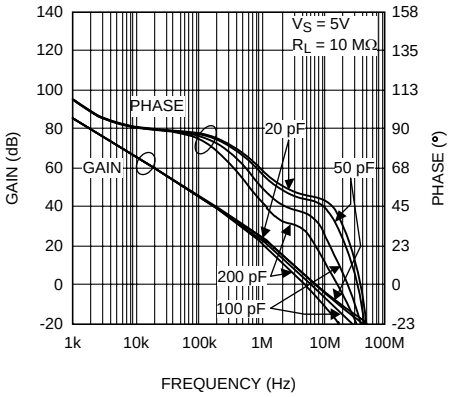


Figure 28.

Open Loop Frequency Response with Various Capacitive Loads

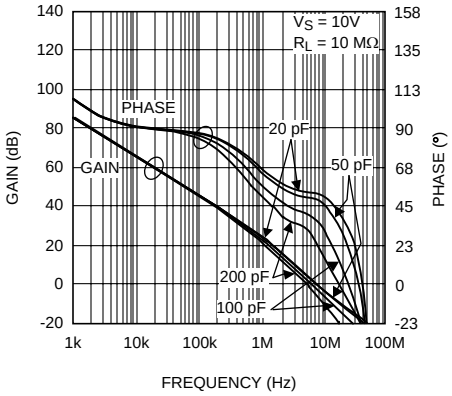


Figure 29.

Open Loop Frequency Response with Various Capacitive Loads

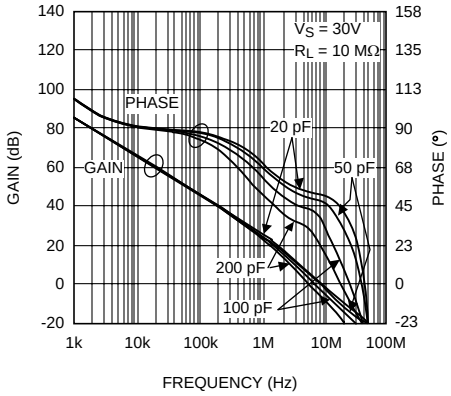


Figure 30.

Open Loop Frequency Response vs. with Various Resistive Loads

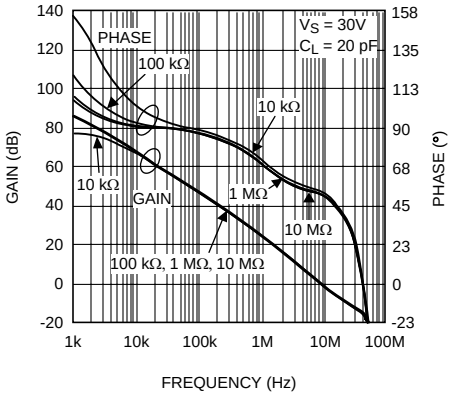


Figure 31.

Open Loop Frequency Response vs. with Various Supply Voltages

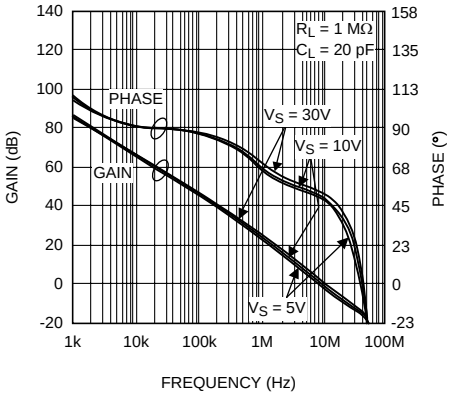


Figure 32.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

Open Loop Frequency Response at Various Temperatures

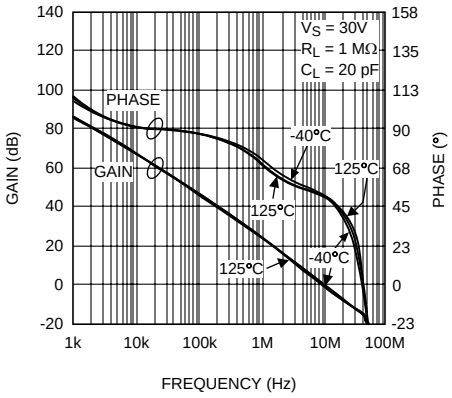


Figure 33.

Phase Margin vs. Capacitive Load

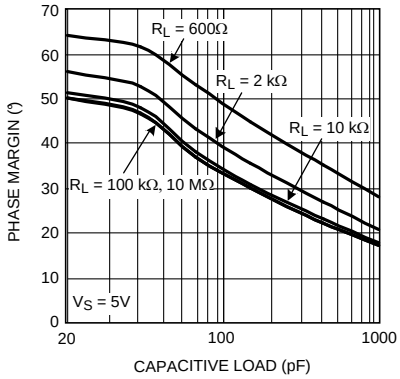


Figure 34.

Phase Margin vs. Capacitive Load

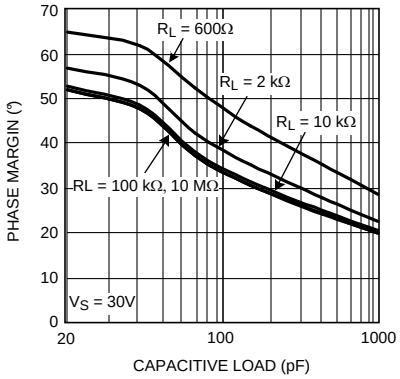


Figure 35.

CMRR vs. Frequency

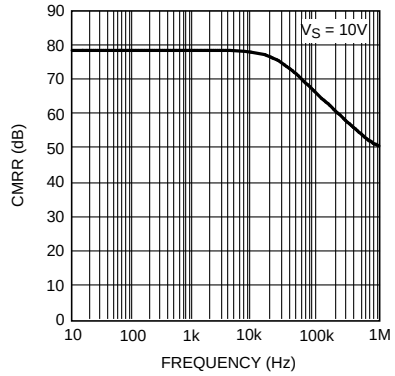


Figure 36.

+PSRR vs. Frequency

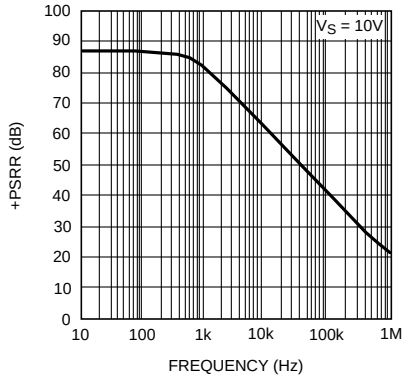


Figure 37.

−PSRR vs. Frequency

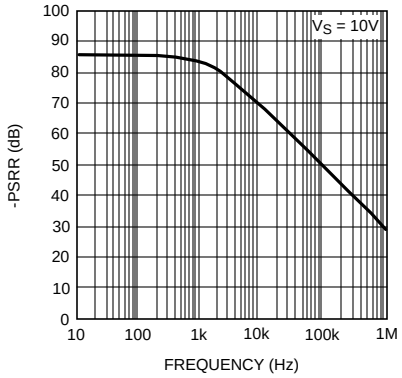


Figure 38.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

Step Response for Various Amplitudes

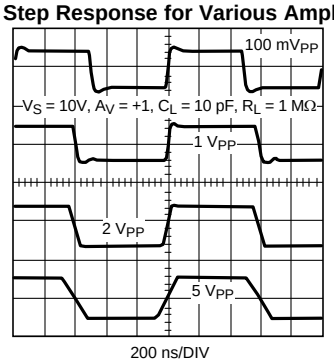


Figure 39.

Step Response for Various Amplitudes

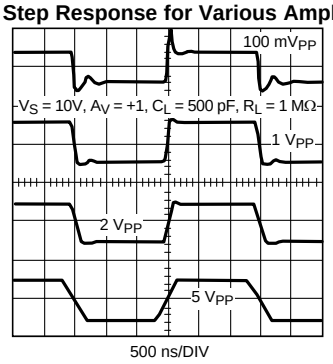


Figure 40.

Large Signal Step Response for Various Capacitive Loads

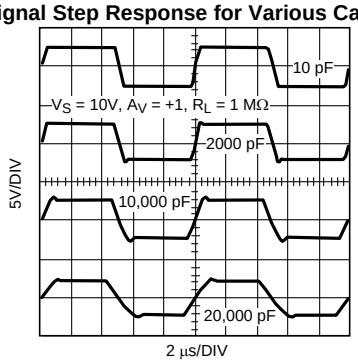


Figure 41.

Input Referred Noise Density vs. Frequency

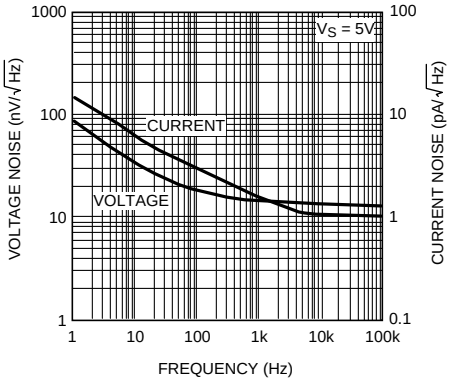


Figure 42.

Input Referred Noise Density vs. Frequency

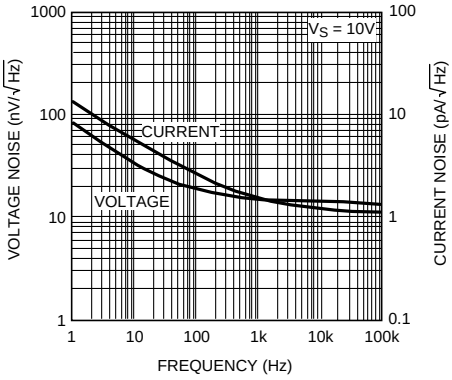


Figure 43.

Input Referred Noise Density vs. Frequency

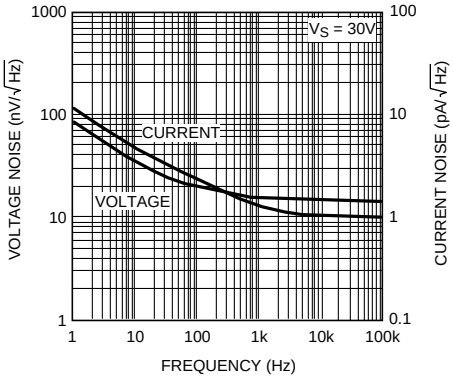


Figure 44.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

THD+N vs. Output Amplitude (V_{PP})

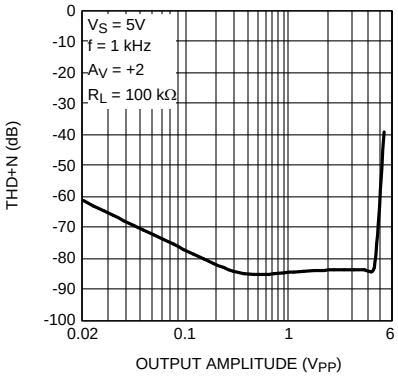


Figure 45.

THD+N vs. Output Amplitude (V_{PP})

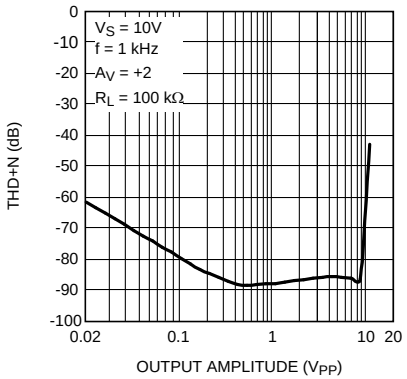


Figure 46.

THD+N vs. Output Amplitude (V_{PP})

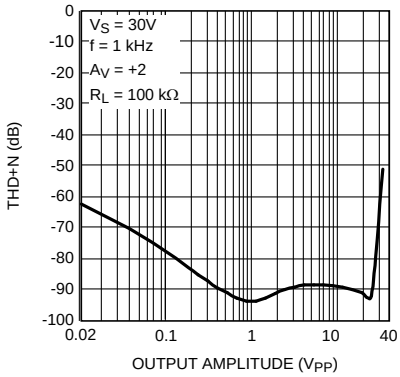


Figure 47.

Crosstalk vs. Frequency

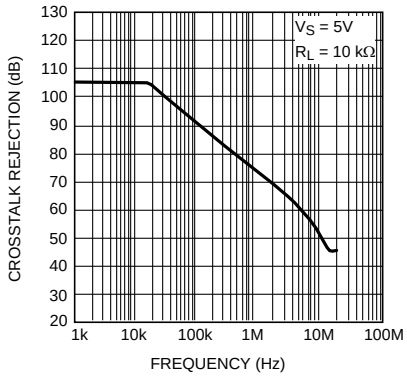


Figure 48.

APPLICATION INFORMATION

ADVANTAGES OF THE LM7332

Wide Operating Voltage Range

The LM7332 has an operating voltage from 2.5V to 32V which makes it suitable for industrial and automotive applications.

RRIO with 100 mA Output Current

The LM7332 takes advantages of Texas Instruments' VIP3 process which enables high current driving from the rails. Rail-to-rail output swing provides the maximum possible output dynamic range. The LM7332 eliminates the need to use extra transistors when driving large capacitive loads, therefore reducing the application cost and space.

-40°C to 125°C Operating Temperature Range

The LM7332 has an operating temperature ranging from -40°C to 125°C, which is Automotive Grade 1, and also meets most industrial requirements.

SOIC and VSSOP Packages

The LM7332 are offered in both the standard SOIC package and the space saving VSSOP package. Please refer to the Physical Dimensions on page 17 for details.

OUTPUT VOLTAGE SWING CLOSE TO V^-

The LM7332's output stage design allows voltage swings to within millivolts of either supply rail for maximum flexibility and improved useful range. Because of this design architecture, with output approaching either supply rail, the output transistor Collector-Base junction reverse bias will decrease. With output less than a V_{be} from either rail, the corresponding output transistor operates near saturation. In this mode of operation, the transistor will exhibit higher junction capacitance and lower f_t which will reduce phase margin. With the Noise Gain (NG = 1 + R_F/R_G, R_F and R_G are external gain setting resistors) of 2 or higher, there is sufficient phase margin that this reduction in phase margin is of no consequence. However, with lower Noise Gain (<2) and with less than 150 mV to the supply rail, if the output loading is light, the phase margin reduction could result in unwanted oscillations.

In the case of the LM7332, due to inherent architectural specifics, the oscillation occurs only with respect to the output transistor at V^- when output swings to within 150 mV of V^-. However, if this output transistor's collector current is larger than its idle value of a few microamps, the phase margin loss becomes insignificant. In this case, 300 µA is the required output transistor's collector current to remedy this situation. Therefore, when all the aforementioned critical conditions are present at the same time (NG < 2, V_{OUT} < 150 mV from supply rails, & output load is light) it is possible to ensure stability by adding a load resistor to the output to provide the output transistor the necessary minimum collector current (300 µA).

For 12V (or ±6V) operation, for example, add a 39 kΩ resistor from the output to V^+ to cause 300 µA output sinking current and ensure stability. This is equivalent to about 15% increase in total quiescent power dissipation.

DRIVING CAPACITIVE LOADS

The LM7332 is specifically designed to drive unlimited capacitive loads without oscillations. In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads as shown in Figure 49. The combination of these features is ideal for applications such as TFT flat panel buffers, A/D converter input amplifiers and power transistor driver.

However, as in most op amps, addition of a series isolation resistor between the op amp and the capacitive load improves the settling and overshoot performance.

Output current drive is an important parameter when driving capacitive loads. This parameter will determine how fast the output voltage can change. Referring to Figure 49, two distinct regions can be identified. Below about 10,000 pF, the output Slew Rate is solely determined by the op amp's compensation capacitor value and available current into that capacitor. Beyond 10 nF, the Slew Rate is determined by the op amp's available output current. An estimate of positive and negative slew rates for loads larger than 100 nF can be made by dividing the short circuit current value by the capacitor.

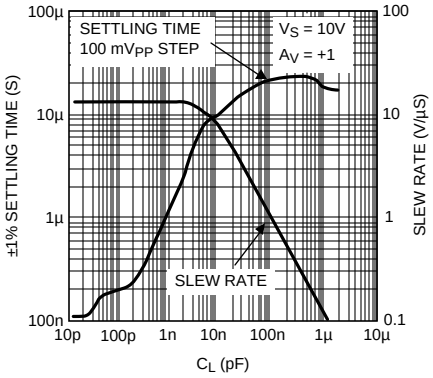


Figure 49. Settling Time and Slew Rate vs. Capacitive Load

ESTIMATING THE OUTPUT VOLTAGE SWING

It is important to keep in mind that the steady state output current will be less than the current available when there is an input overdrive present. For steady state conditions, Figure 50 and Figure 51 plots can be used to predict the output swing. These plots also show several load lines corresponding to loads tied between the output and ground. In each case, the intersection of the device plot at the appropriate temperature with the load line would be the typical output swing possible for that load. For example, a 600Ω load can accommodate an output swing to within 100 mV of V^- and to 250 mV of V^+ (V_S = ±5V) corresponding to a typical 9.65 V_{PP} unclipped swing.

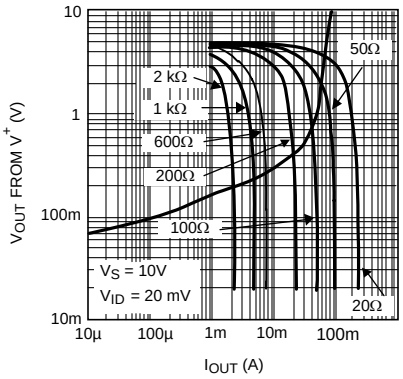


Figure 50. Steady State Output Sourcing Characteristics with Load Lines

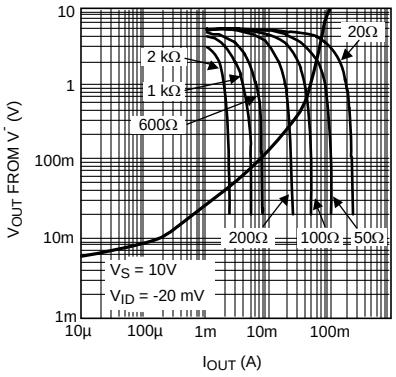


Figure 51. Steady State Output Sinking Characteristics with Load Lines

OUTPUT SHORT CIRCUIT CURRENT AND DISSIPATION ISSUES

The LM7332 output stage is designed for maximum output current capability. Even though momentary output shorts to ground and either supply can be tolerated at all operating voltages, longer lasting short conditions can cause the junction temperature to rise beyond the absolute maximum rating of the device, especially at higher supply voltage conditions. Below supply voltage of 6V, the output short circuit condition can be tolerated indefinitely.

With the op amp tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power itself could include an average value (due to a DC load current) and an AC component. DC load current would flow if there is an output voltage offset, or the output AC average current is non-zero, or if the op amp operates in a single supply application where the output is maintained somewhere in the range of linear operation. Therefore:

$P_{TOTAL} = P_Q + P_{DC} + P_{AC}$

$P_Q = I_S \cdot V_S$ Op Amp Quiescent Power Dissipation

$P_{DC} = I_O \cdot (V_r - V_o)$ DC Load Power

P_{AC} = See Table 1 Below AC Load Power

where:

- I_S: Supply Current
- V_S: Total Supply Voltage ($V^+ - V^-$)
- V_O: Average Output Voltage
- V_r: V^+ for sourcing and V^- for sinking current

Table 1 below shows the maximum AC component of the load power dissipated by the op amp for standard Sinusoidal, Triangular, and Square Waveforms:

Table 1. Normalized AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} ($W.\Omega/V^2$)		
Sinusoidal	Triangular	Square
50.7×10^{-3}	46.9×10^{-3}	62.5×10^{-3}

The table entries are normalized to V_S^2/R_L. To figure out the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor V_S^2/R_L. For example, with ±12V supplies, a 600Ω load, and triangular waveform power dissipation in the output stage is calculated as:

$$P_{AC} = (46.9 \times 10^{-3}) \cdot [24^2/600] = 45.0 \text{ mW} \quad (1)$$

The maximum power dissipation allowed at a certain temperature is a function of maximum die junction temperature ($T_{J(MAX)}$) allowed, ambient temperature T_A, and package thermal resistance from junction to ambient, θ_{JA}.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (2)$$

For the LM7332, the maximum junction temperature allowed is 150°C at which no power dissipation is allowed. The power capability at 25°C is given by the following calculations:

For VSSOP package:

$$P_{D(MAX)} = \frac{150℃ - 25℃}{235℃/W} = 0.53W \quad (3)$$

For SOIC package:

$$P_{D(MAX)} = \frac{150℃ - 25℃}{165℃/W} = 0.76W \quad (4)$$

Similarly, the power capability at 125°C is given by:

For VSSOP package:

$$P_{D(MAX)} = \frac{150℃ - 125℃}{235℃/W} = 0.11W \quad (5)$$

For SOIC package:

$$P_{D(MAX)} = \frac{150℃ - 125℃}{165℃/W} = 0.15W \quad (6)$$

Figure 52 shows the power capability vs. temperature for VSSOP and SOIC packages. The area under the maximum thermal capability line is the operating area for the device. When the device works in the operating area where P_{TOTAL} is less than $P_{D(MAX)}$, the device junction temperature will remain below 150°C. If the intersection of ambient temperature and package power is above the maximum thermal capability line, the junction temperature will exceed 150°C and this should be strictly prohibited.

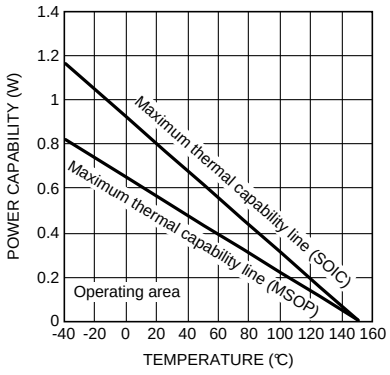


Figure 52. Power Capability vs. Temperature

When high power is required and ambient temperature can't be reduced, providing air flow is an effective approach to reduce thermal resistance therefore to improve power capability.

APPLICATION HINTS ON SUPPLY DECOUPLING

The use of supply decoupling is mandatory in most applications. As with most relatively high speed/high output current op amps, best results are achieved when each supply line is decoupled with two capacitors; a small value ceramic capacitor (~0.01 µF) placed very close to the supply lead in addition to a large value Tantalum or Aluminum capacitor (> 4.7 µF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at high frequencies while the large capacitor will act as the charge “bucket” for fast load current spikes at the op amp output. The combination of these capacitors will provide supply decoupling and will help keep the op amp oscillation free under any load.

SIMILAR HIGH CURRENT OUTPUT DEVICES

The LM6172 has a higher GBW of 100 MHz and over 80 mA of current output. There is also a single version, the LM6171. The LM7372 has 120 MHz of GBW and 150 mA of current output. The LM7372 is available in an 8-pin SO PowerPAD, and 16-pin SOIC packages with higher power dissipation.

The LME49600 buffer has 250 mA of current out and a 110 MHz bandwidth. The LME49600 is available in a DDPAK/TO-263 package for higher power dissipation.

The LM7322 is a rail-to-rail input and output part with a slightly higher GBW of 20 MHz. It has current capability of 40 mA sourcing and 65 mA sinking, and can drive unlimited capacitive loads. The LM7322 is available in both VSSOP and SOIC packages.

Detailed information on these parts can be found at www.ti.com.

REVISION HISTORY

Changes from Original (March 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM7332MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM733 2MA	Samples
LM7332MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM733 2MA	Samples
LM7332MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AA5A	Samples
LM7332MME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AA5A	Samples
LM7332MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AA5A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

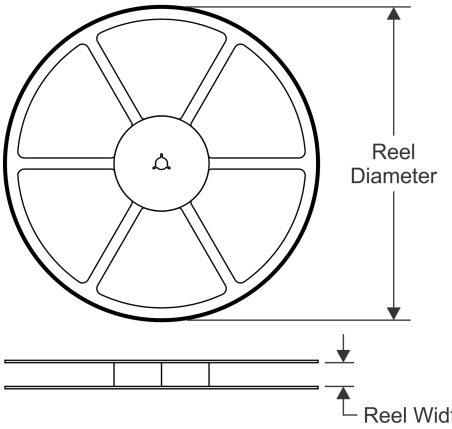
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

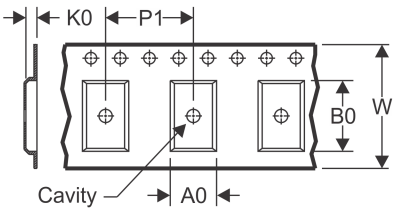
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

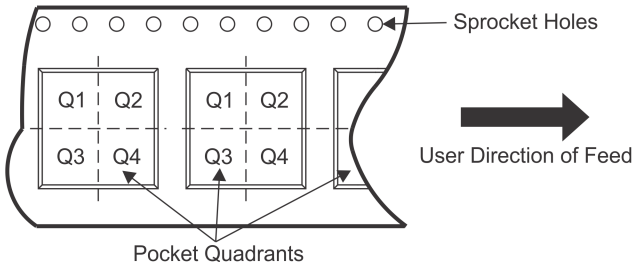


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

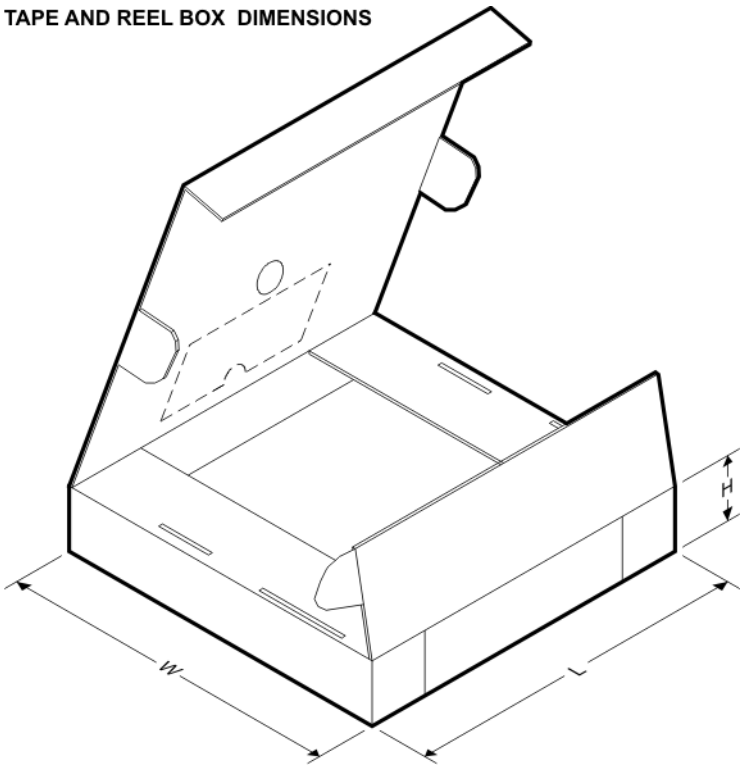
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7332MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM7332MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM7332MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM7332MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

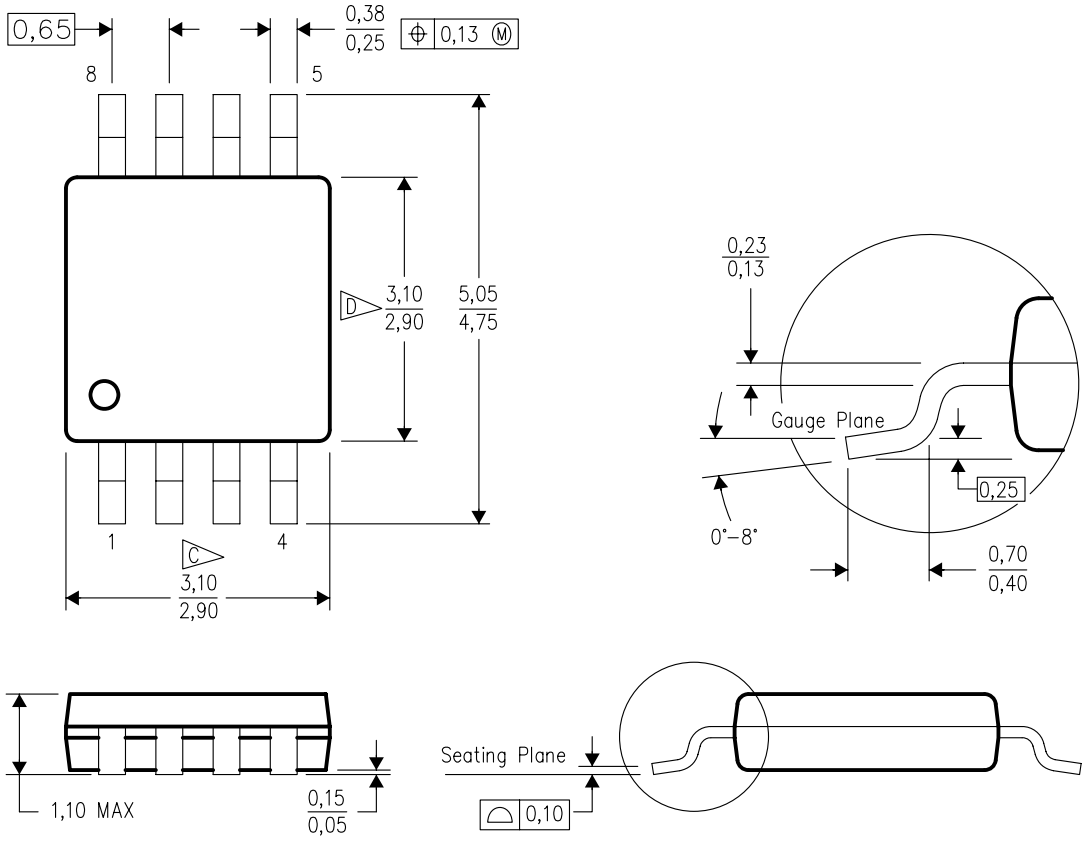
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7332MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM7332MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM7332MME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LM7332MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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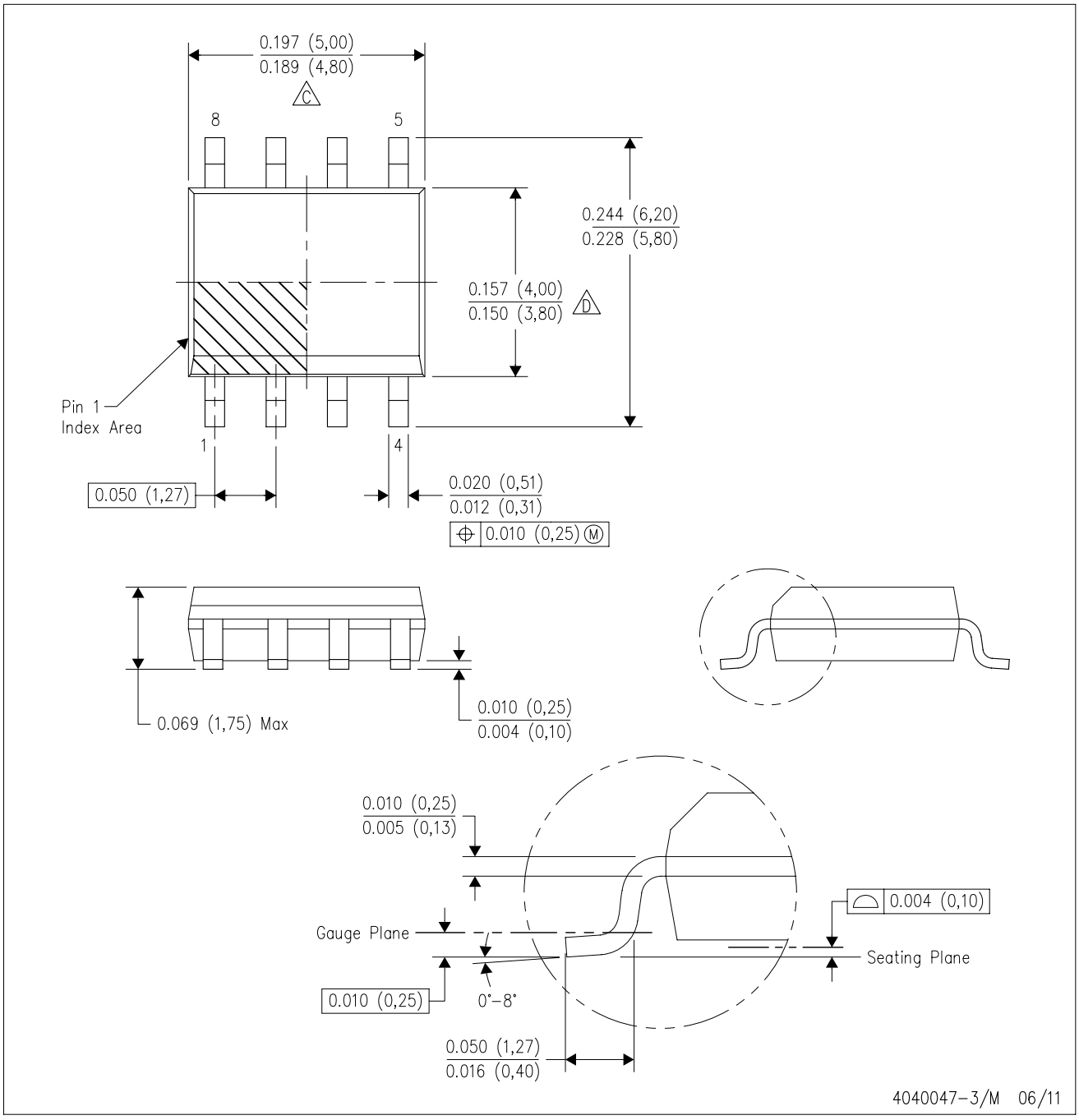
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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- Техническая поддержка проекта;
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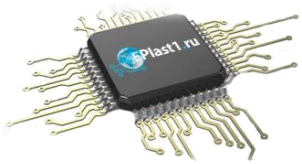

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